

---

**MDmesh™ M2-EP: an additional improvement to MDmesh™ M2  
ST super-junction technology**

---

Alfio Scuto, Antonino Gaito, Carlo Brusca, Giuseppe Sorrentino, Maurizio Melito, Santina Leo

## **Introduction**

The new MDmesh™ M2-EP series represents the latest generation of ST high voltage power MOSFETs designed according to the revolutionary super-junction (SJ) principle. The series is the result of the experience gained as the leading SJ MOSFET supplier and innovation focusing on high efficiency solutions.

The MDmesh™ M2-EP technology is tailored to provide high performance hard and soft switching topologies (e.g., PFC, LLC), without sacrificing the ease of use.

Every application has specific requirements and optimization criteria which must be satisfied by the available technologies and innovative package solutions. Factors like efficiency, power density, EMI, layout parasitic elements, commutation behavior and cost cannot all be fulfilled simultaneously, so it is necessary to develop different technologies and solutions.

The advanced MDmesh™ M2-EP series allows extremely low switching losses, especially under light load conditions, enabling switching applications to achieve target certification levels with more compact and lighter designs.

In this document, we analyze certain aspects of the MDmesh™ M2-EP series that render these devices suitable for both soft and hard switching applications. This is not only due to the very low total gate charge (already an advantage of the previous M2 series), but also due to the turn-off switching loss reduction, especially in the low current range. This feature is essential for boosting the efficiency under light load conditions, which is subject to increasingly stringent certification rules.

The optimization of both the shape and the absolute value of the output capacitance completes the set of features that render the MDmesh™ M2-EP series highly suitable for target applications.

# Contents

|          |                                                   |           |
|----------|---------------------------------------------------|-----------|
| <b>1</b> | <b>Super-junction (SJ) principle</b>              | <b>4</b>  |
| <b>2</b> | <b>Technology comparison</b>                      | <b>6</b>  |
| 2.1      | Electrical characteristic comparison              | 6         |
| 2.2      | Gate charge improvement                           | 6         |
| 2.3      | Output capacitance profile improvement            | 8         |
| 2.4      | M2 vs M2 EP switching losses comparison           | 8         |
| 2.5      | Energy stored in output capacitance ( $E_{oss}$ ) | 10        |
| <b>3</b> | <b>Measurement results</b>                        | <b>13</b> |
| 3.1      | Efficiency measurement in a 500 W PFC             | 13        |
| 3.2      | Efficiency measurement in a 500 W LLC stage       | 15        |
| 3.3      | Efficiency measurement in a 200 W PFC             | 17        |
| 3.4      | Efficiency measurement in a 150 W LLC             | 19        |
| <b>4</b> | <b>Conclusion</b>                                 | <b>21</b> |
| <b>5</b> | <b>References</b>                                 | <b>22</b> |
| <b>6</b> | <b>Revision history</b>                           | <b>23</b> |

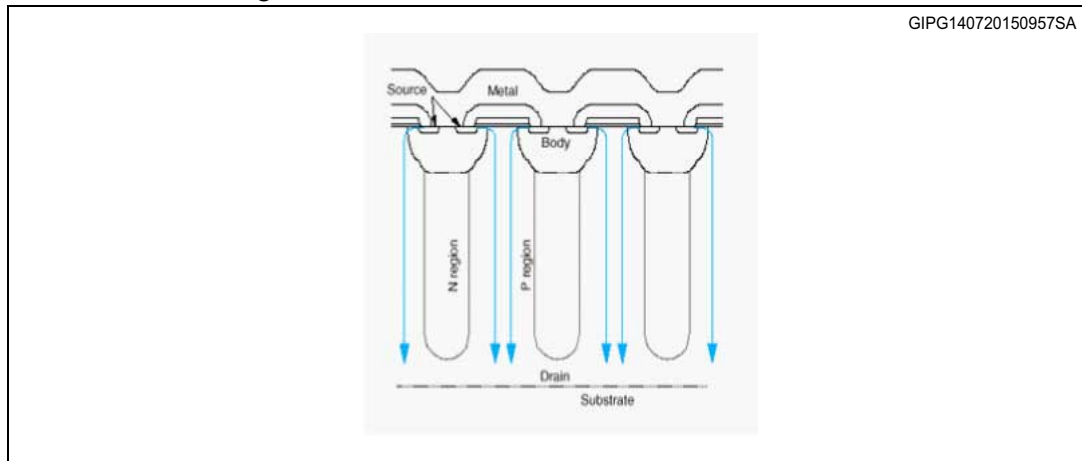
## List of figures

|            |                                                                                                                               |    |
|------------|-------------------------------------------------------------------------------------------------------------------------------|----|
| Figure 1.  | Cross section of SJ MOSFET in on-state . . . . .                                                                              | 4  |
| Figure 2.  | Cross section of SJ MOSFET in off-state . . . . .                                                                             | 4  |
| Figure 3.  | Gate charge comparison @ 480 V, 5 A for M2, M2-EP devices; $V_{GS}=10$ V/div,<br>$V_{DS}=100$ V/div, $Q_g=8$ nC/div . . . . . | 7  |
| Figure 4.  | Gate charge comparison @ 480 V, 5 A for M2, M2-EP devices, $V_{GS}=10$ V/div,<br>$V_{DS}=10$ V/div, $Q_g=8$ nC/div . . . . .  | 8  |
| Figure 5.  | M2 vs M2-EP $C_{oss}$ comparison. . . . .                                                                                     | 9  |
| Figure 6.  | M2 vs M2-EP $C_{rss}$ comparison . . . . .                                                                                    | 9  |
| Figure 7.  | $E_{off}$ vs $I_d$ at $V_{DS}=400$ V, $R_{goff}=22$ . . . . .                                                                 | 10 |
| Figure 8.  | $E_{off}$ vs $I_d$ in LLC converter . . . . .                                                                                 | 10 |
| Figure 9.  | Comparison of midpoint voltage . . . . .                                                                                      | 11 |
| Figure 10. | LLC circuit behavior at ZVS transition . . . . .                                                                              | 12 |
| Figure 11. | Efficiency for 230 Vac (PFC CCM, 60 kHz, diode STPSC1006D) . . . . .                                                          | 14 |
| Figure 12. | Efficiency difference for 230 Vac (PFC CCM, 60 kHz, diode STPSC1006D) . . . . .                                               | 14 |
| Figure 13. | Efficiency for 230 Vac (LLC) . . . . .                                                                                        | 16 |
| Figure 14. | Efficiency difference for 230 Vac . . . . .                                                                                   | 16 |
| Figure 15. | Efficiency for 230 Vac (PFC CCM, 100 kHz, diode STTH8R06) . . . . .                                                           | 18 |
| Figure 16. | Efficiency difference for 230 Vac (PFC CCM, 100 kHz, diode STTH8R06) . . . . .                                                | 18 |
| Figure 17. | Efficiency for 230 Vac (LLC) . . . . .                                                                                        | 20 |
| Figure 18. | Efficiency difference for 230 Vac (LLC) . . . . .                                                                             | 20 |

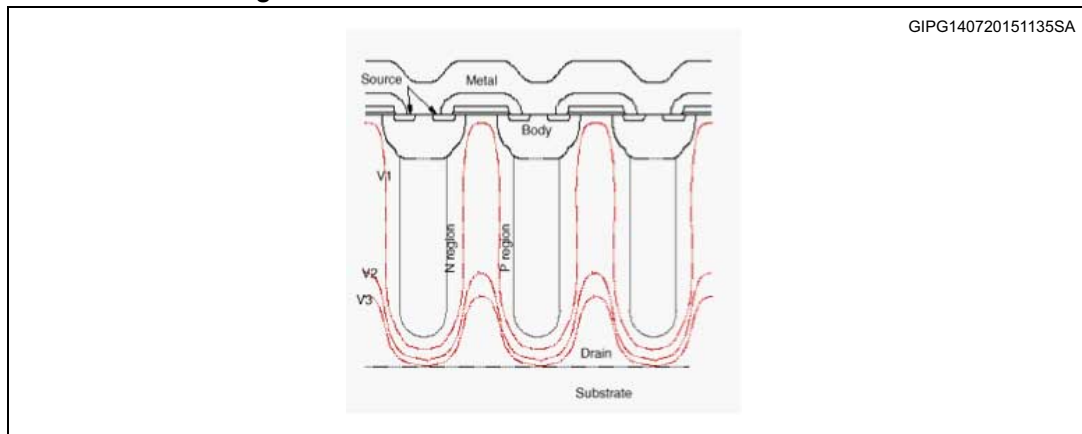
# 1 Super-junction (SJ) principle

The basic idea [1] [2] of the well-known Super Junction principle is quite simple: in the on-state (*Figure 1*), the electrons flow through a very low resistive N-area, while in the blocking state (*Figure 2*) no electron flow is allowed due to space-charge expansion between the P-doped columns. The practical implementation of this very attractive idea however requires the most sophisticated manufacturing technologies due to the necessity for perfect compensation of the additional N-charge between adjacent P-columns.

**Figure 1. Cross section of SJ MOSFET in on-state**



**Figure 2. Cross section of SJ MOSFET in off-state**



The SJ principle overcomes intrinsic silicon limitations to allow smaller chip sizes than conventional Power MOSFETs with the same  $R_{DS(on)}$ . As a consequence, all the phenomena associated with surface area decrease directly with chip size. Some parameters, however, are also strongly linked to the underlying technology.

An example, not present in standard Power MOSFETs, is in the sudden decrease of output capacitance from low to high drain voltage. This is related to the structure of the output capacitance, which changes from a thin very large surface capacitor, due to the space surface layer at low voltage drain, to capacitance which is smaller by orders of magnitude due to the full depletion of the space charge layer, leading to surface capacitor decrease and width increase. The lower the voltage under which this transitions occurs, the faster and

lower losses the device is subject to. Similar behavior occurs with reverse capacitance, albeit with some differences.

## 2 Technology comparison

### 2.1 Electrical characteristic comparison

The following table reports a summary of the main static and dynamic electrical characteristics of both an M2 and an M2-EP device. They seem very similar, and the advantages owing to the technological optimizations are not immediately apparent from the values given.

In the next sections, the deeper analysis of some key parameters will demonstrate and explain the technological improvements achieved by the M2-EP devices.

**Table 1. M2 and M2-EP device comparison**

| Symbol        | Parameter                         | Test condition                                                      | STP40N60M2 | STP42N60M2-EP | Unit |
|---------------|-----------------------------------|---------------------------------------------------------------------|------------|---------------|------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$                             | 600        | 600           | V    |
| $I_D$         | Drain current                     |                                                                     |            |               | A    |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS}=10\text{ V}$ , $I_D=17\text{ A}$                            | 78         | 76            | mΩ   |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$                      | 3          | 3             | V    |
| $R_G$         | Intrinsic gate resistance         |                                                                     | 4.4        | 4.5           | Ω    |
| $Q_G$         | Total gate-charge                 | $V_{DD}=480\text{ V}$ , $I_D=34\text{ A}$ ,<br>$V_{GD}=10\text{ V}$ | 57         | 55            | nC   |
| $Q_{GS}$      | Gate-source charge                |                                                                     | 10         | 8.5           |      |
| $Q_{GD}$      | Gate-drain charge                 |                                                                     | 25.5       | 25            |      |
| $C_{iss}$     | Input capacitance                 | $V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ ,<br>$f=1\text{ MHz}$   | 2500       | 2370          | pF   |
| $C_{oss}$     | Output capacitance                |                                                                     | 117        | 112           |      |
| $C_{rss}$     | Reverse capacitance               |                                                                     | 2.4        | 2.5           |      |

### 2.2 Gate charge improvement

The gate-charge curve is the main tool for quickly comparing the on-field behavior of different devices in terms of gate driving energy requirements and switching losses.

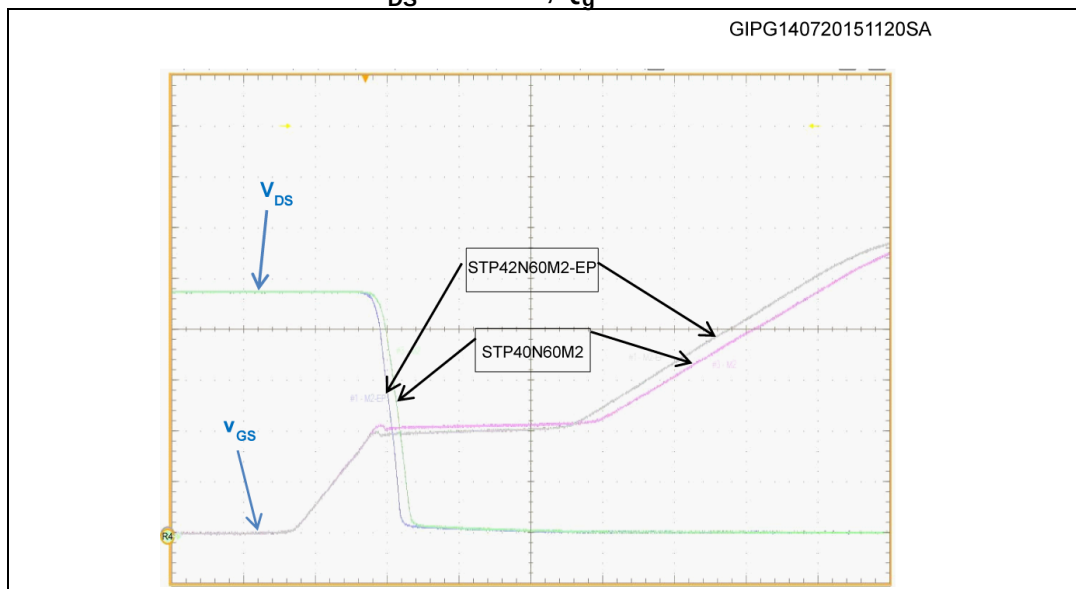
The datasheet information in [Table 2](#), [Figure 3](#) and [Figure 4](#) show the relatively minor differences in the  $Q_{gs}$ ,  $Q_{gd}$  and  $Q_g$  values. But the numeric values alone give no enough information regarding the benefits of the  $E_{off}$  reduction in the low current range, which is essential for boosting efficiency under light load conditions, for which certification rules are becoming increasingly stringent.

Table 2. STP40N60M2 and STP42N60M2-EP gate-charge comparison

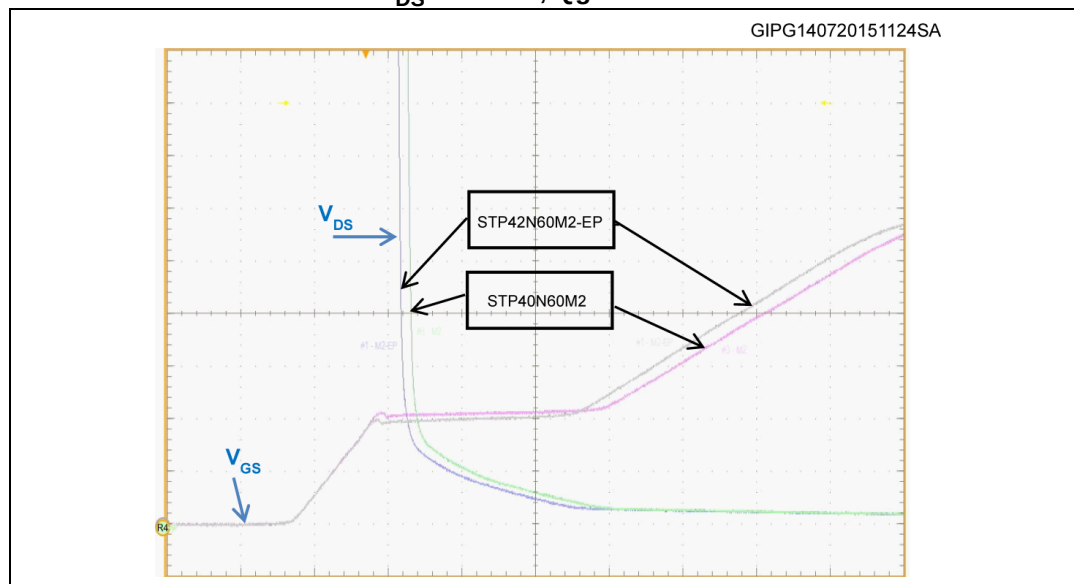
| Symbol   | Parameter          | Test condition                                                      | Value |       | Unit |
|----------|--------------------|---------------------------------------------------------------------|-------|-------|------|
|          |                    |                                                                     | M2    | M2-EP |      |
| $Q_g$    | Total gate-charge  | $V_{DD}=480\text{ V}$ , $I_D=34\text{ A}$ ,<br>$V_{GS}=10\text{ V}$ | 57    | 55    | nC   |
| $Q_{gs}$ | Gate-source charge |                                                                     | 10    | 8.5   | nC   |
| $Q_{gd}$ | Gate-drain charge  |                                                                     | 25.5  | 25    | nC   |

Besides the very low  $Q_g$  typical of both series, M2-EP features up to 20%  $E_{off}$  reduction under light load conditions, thus reducing the turn-off switching losses by the same percentage in hard switching converters. The decrease of the  $V_{DS}$ - $I_D$  overlap area only partially explains the reduction in switching losses in M2-EP devices, so a more detailed analysis in the following sections is required to understand this behavior, which is mainly related to the different shape of the capacitance profile.

Figure 3. Gate charge comparison @ 480 V, 5 A for M2, M2-EP devices;  $V_{GS}=10\text{ V/div}$ ,  $V_{DS}=100\text{ V/div}$ ,  $Q_g=8\text{ nC/div}$



**Figure 4. Gate charge comparison @ 480 V, 5 A for M2, M2-EP devices,  $V_{GS}=10$  V/div,  $V_{DS}=10$  V/div,  $Q_g= 8$  nC/div**



## 2.3 Output capacitance profile improvement

The next two figures compare the  $C_{oss}$  and the  $C_{rss}$  of the MDmesh™ M2 and M2-EP series. The improvement is due to an optimization of the overall column aspect. The height to width ratio and the horizontal structure pitch remain more or less the same, while a sharper capacitance transition from low to high  $V_{DS}$  voltage is observed. The emphasis in the non-linearity of the capacitance characteristic, typical of the SJ structure, helps in achieving lower switching losses. The exact reason for the achieved improvement is analyzed in the following sections.

## 2.4 M2 vs M2-EP switching loss comparison

The following figures compare the switching losses for both hard ([Figure 7](#)) and soft switching ([Figure 8](#)) conditions. In both cases, the M2-EP technology suffers lower losses with respect to its M2 counterpart due to gate charge and output capacitance profile optimization.

As turn-on and on losses remain very similar, M2-EP devices are superior in terms of overall efficiency. However, as M2-EP devices are technologically more sophisticated, they are also more expensive. With other aspects like ruggedness and reliability being virtually equivalent, the best tradeoff can be determined by considering efficiency and cost factors alone.

In [Section 3](#) some real examples of obtainable efficiency improvements are given.



Figure 5. M2 vs M2-EP  $C_{oss}$  comparison

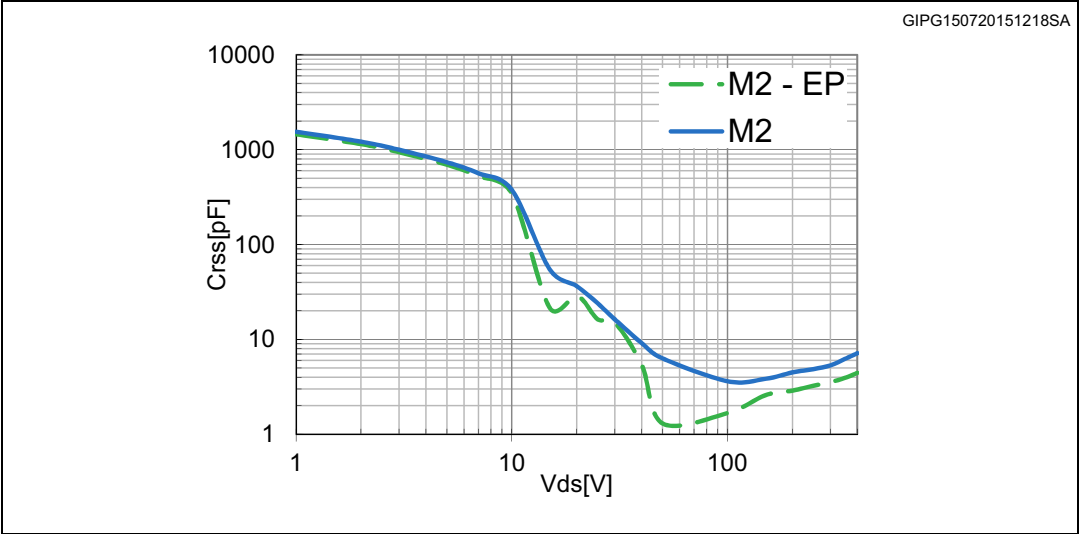


Figure 6. M2 vs M2-EP  $C_{rss}$  comparison

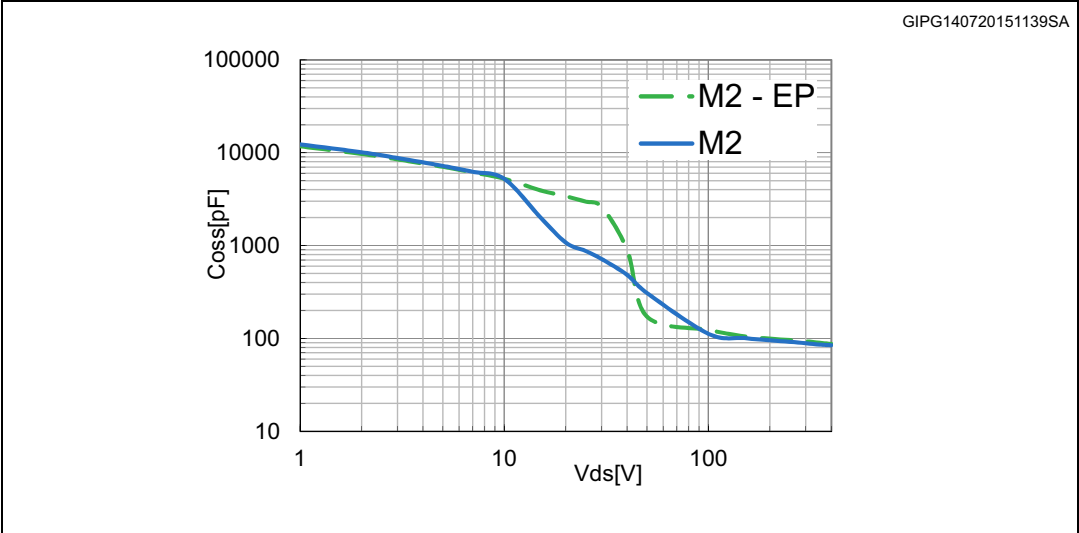
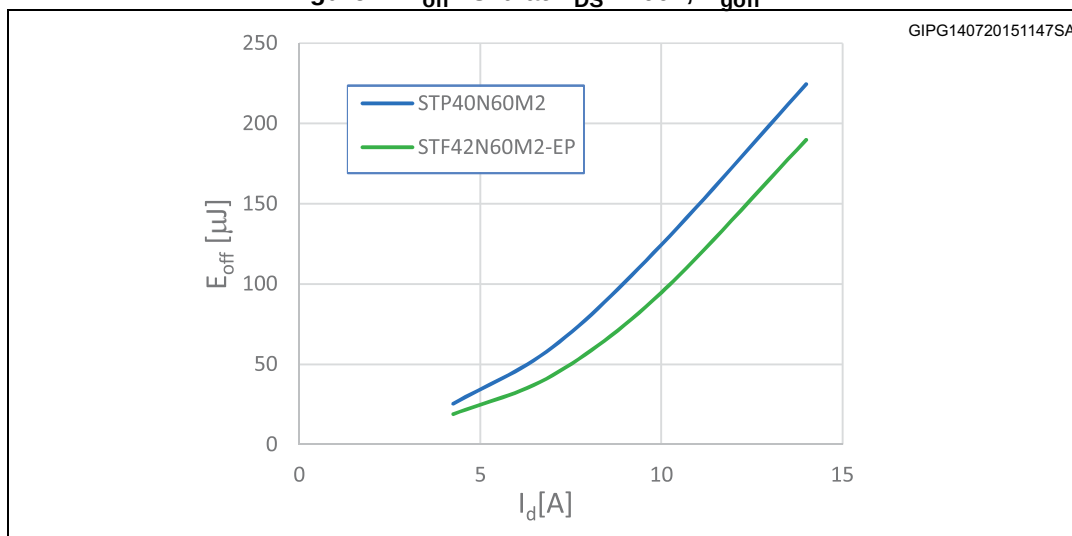
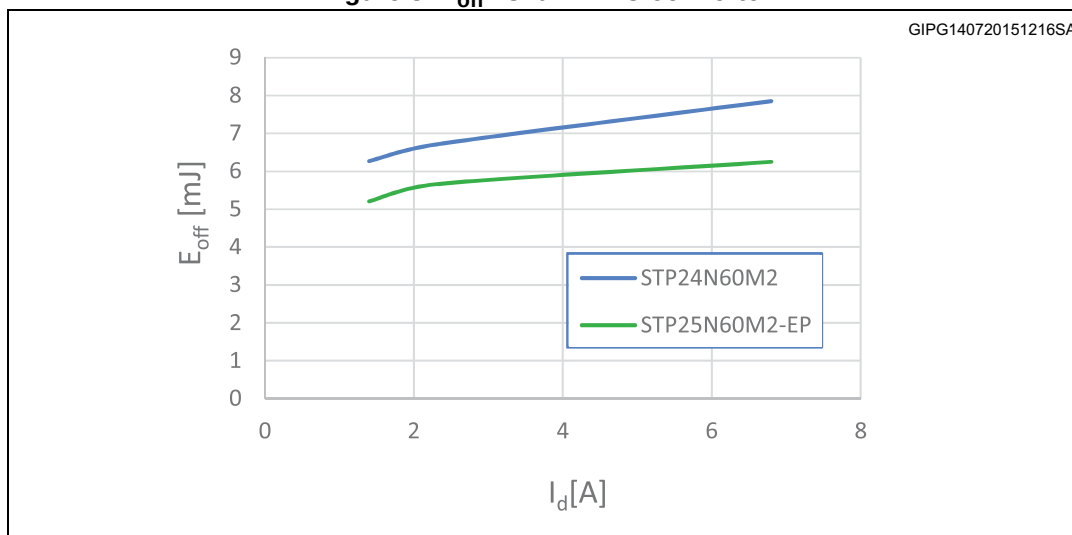


Figure 7.  $E_{off}$  vs  $I_d$  at  $V_{DS}=400V$ ,  $R_{goff}=22$ Figure 8.  $E_{off}$  vs  $I_d$  in LLC converter

## 2.5 Energy stored in output capacitance ( $E_{oss}$ )

The energy stored in the output capacitance is another factor to be considered for efficiency improvement. As the output capacitance is a voltage-dependent capacitance, the stored charge depends on the shape of the capacitance itself versus the applied voltage.

In hard switching applications, the energy stored in the output capacitance at turn-off is completely lost during the next turn-on, so the lower the stored energy, the higher the resulting efficiency. As it is not related to drain-current values, energy loss due to output capacitance is more important at light loads because of the considerable decrease in other switching losses.

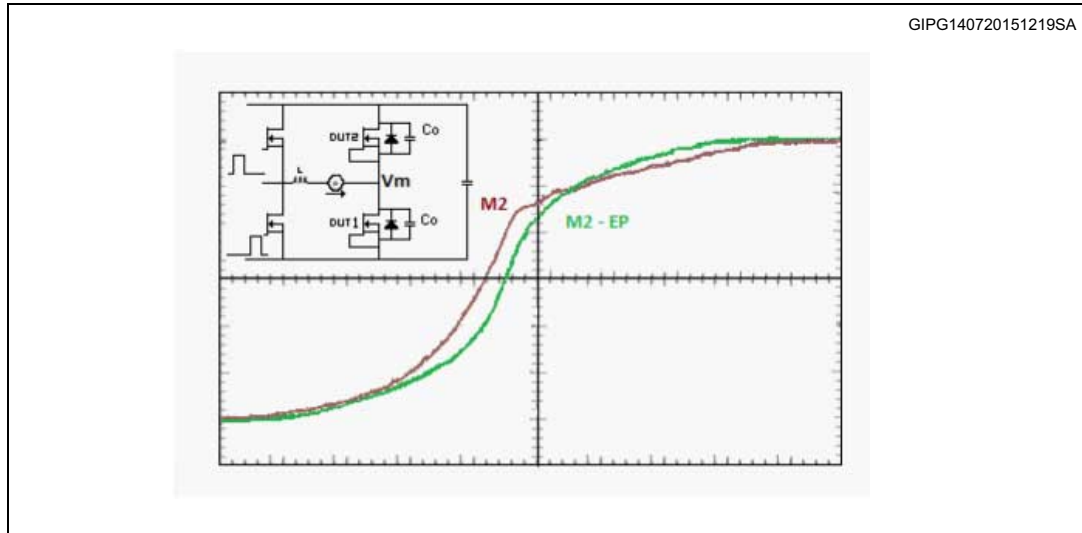
In soft switching (as in LLC resonance converters), the stored energy is sent back to the power supply, so ideally there is no energy loss. In reality there is some dissipation due to the non-ideal output capacitance leading to efficiency degradation. The amount of energy

loss is related to the “ideality” of the output capacitance i.e., to the different shape of the  $V_{DS}$  during charge and discharge of the output capacitance [3] [4] [5].

Figure 9 compares the  $V_{DS}$  voltage of an M2-EP with an M2 device during the low to high transition of DUT1, corresponding to the charge of the output capacitance of DUT1 and discharge of DUT2.

Despite the symmetry of the circuit topology, the  $V_{DS}$  voltage is not symmetrical with respect to the voltage midpoint, showing a sort of capacitance hysteresis. The M2-EP device does however show a more “ideal” symmetric shape than the M2 device.

**Figure 9. Comparison of midpoint voltage**



M2-EP devices therefore perform better than M2 devices in ZVS applications because of the more ideal output capacitance. In Section 3, the results for both hard and soft switching applications are given.

Another positive aspect of having a low output capacitance at lower  $V_{DS}$  voltages is the possibility of achieving the ZVS condition more easily. In Figure 10, which shows the simplified schematic of the output stage of an LLC converter with relative waveforms during ZVS transition, the current value required for achieving ZVS is:

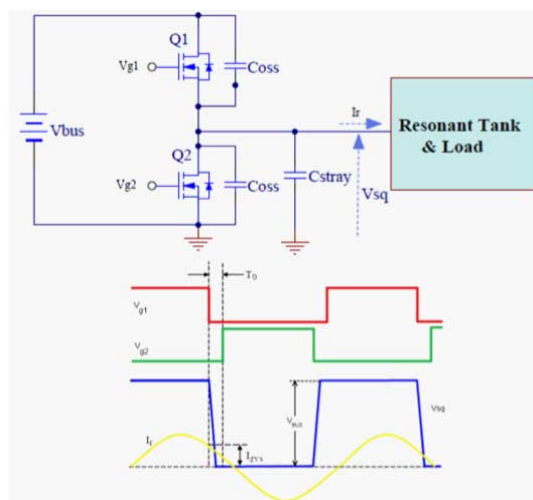
#### Equation 1

$$I_{ZVS} = i_{rt} \left( \frac{T_{sw}}{2} \right) = C_{ZVS} \frac{\Delta V}{T_D} = (2C_{oss} + C_{stray}) \frac{V_{DC}}{T_D}$$

The minimum inductor current required for ZVS, necessary to charge/discharge the effective capacitance appearing in parallel with drain-sources of the power switches in half-bridge LLC, is related to the capacitance itself. The lower the output capacitance value, the lower the need for magnetizing current and less dead time. For further details, refer to [6] [7] [8].

Figure 10. LLC circuit behavior at ZVS transition

GIPG140720151224SA



### 3 Measurement results

In this section, we compare the new M2-EP with standard M2 devices and direct competitors in some typical applications.

#### 3.1 Efficiency measurement in a 500 W PFC

In this section, the devices with principal characteristics provided in [Table 3](#) are compared. The test vehicle is the PFC section of an STEVAL-ISA147V2, a 500 W fully digital AC-DC power supply (D-SMPS) based on the STM32F334C8 microcontroller [9].

The test conditions are:

- $V_{\text{mains}} = 90 - 264 \text{ Vac}$
- $V_{\text{OUT}} = 430 \text{ V}$
- $P_{\text{OUT}} = 0 \text{ to } 500 \text{ W}$
- $f_{\text{SW}} = 60 \text{ kHz}$

The efficiency measurements in [Figure 11](#) and [12](#) show the advantage of using M2-EP devices over not only M2 devices, but also over the best competition. Under light load conditions, a 0.3% efficiency improvement is measured.

**Table 3. Electrical characteristics of compared devices (STW40N60M2, STW42N60M2-EP and competitors)**

|                                                                  | STW40N60M2 | STW42N60M2-EP | Best competitor | Direct competitor |
|------------------------------------------------------------------|------------|---------------|-----------------|-------------------|
| $BV_{\text{dss min}} [\text{V}] @ 1 \text{ mA}$                  | 600        | 600           | 600             | 600               |
| $V_{\text{th}} [\text{V}] @ 250 \mu\text{A}$                     | 2 - 4      | 2 - 4         | 2.5 - 3.5       | 2.7 - 3.7         |
| $R_{\text{on max}} [\text{m}\Omega] @ 10 \text{ V}/17 \text{ A}$ | 88         | 87            | 99              | 88                |
| $Q_{\text{g}} [\text{nC}]$                                       | 57         | 55            | 60              | 86                |
| $C_{\text{iss}} [\text{pF}] @ 100 \text{ V}$                     | 2500       | 2370          | 2800            | 3000              |
| $C_{\text{oss}} [\text{pF}] @ 100 \text{ V}$                     | 117        | 112           | 130             | 115               |

Figure 11. Efficiency for 230 Vac (PFC CCM, 60 kHz, diode STPSC1006D)

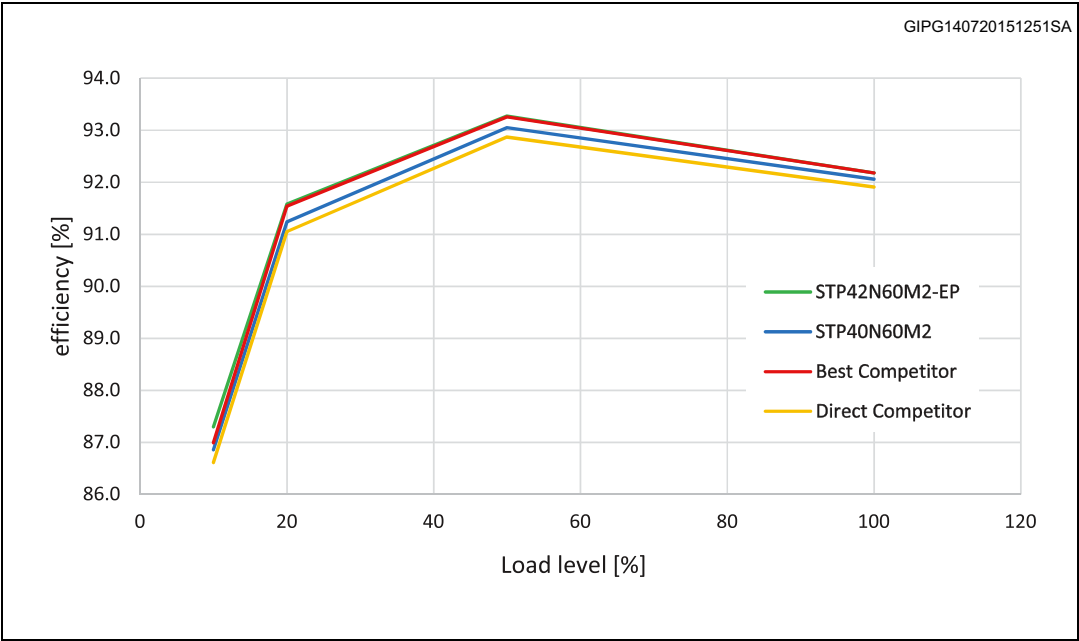
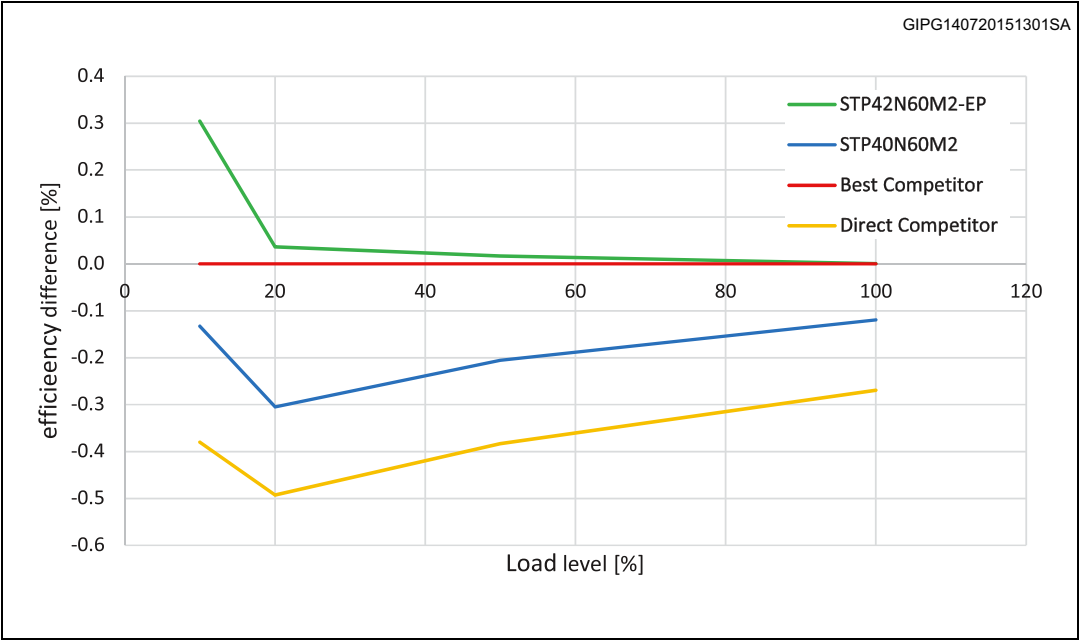


Figure 12. Efficiency difference for 230 Vac (PFC CCM, 60 kHz, diode STPSC1006D)



### 3.2 Efficiency measurement in a 500 W LLC stage

In this section, the devices with principal characteristics given in [Table 4](#) are compared. The test vehicle is the LLC section of an STEVAL-ISA147V2, a 500 W fully digital AC-DC power supply (D-SMPS) based on the STM32F334C8 microcontroller [9].

The test conditions are:

- $V_{\text{mains}} = 90 - 264 \text{ Vac}$
- $V_{\text{OUT}} = 12 \text{ V}$
- $P_{\text{OUT}} = 0 \text{ to } 500 \text{ W}$
- $f_{\text{SW}} = 70 \text{ kHz up to } 130 \text{ kHz}$

The efficiency measurements in [Figure 13](#) and [14](#) show the higher efficiency of M2-EP devices across the whole load range over the M2 devices and the direct competition. The performance of the best competitors are not far from the M2-EP devices.

**Table 4. Electrical characteristics of compared devices (STP24N60M2, STP25N60M2-EP and competitors)**

|                                                         | STP24N60M2 | STP25N60M2-EP | Direct competitor | Best competitor |
|---------------------------------------------------------|------------|---------------|-------------------|-----------------|
| $BV_{\text{dss min}}[\text{V}] @ 1 \text{ mA}$          | 600        | 600           | 600               | 600             |
| $V_{\text{th}} [\text{V}] @ 250 \mu\text{A}$            | 2 - 4      | 2 - 4         | 3.5 - 4.5         | 2.5 - 3.5       |
| $R_{\text{on max}} [\text{m}\Omega] @ 10 \text{ V/9 A}$ | 190        | 188           | 190               | 199             |
| $Q_g [\text{nC}]$                                       | 29         | 29            | 37                | 32              |
| $C_{\text{iss}} [\text{pF}] @ 100 \text{ V}$            | 1060       | 1090          | 1750              | 1500            |
| $C_{\text{oss}} [\text{pF}] @ 100 \text{ V}$            | 55         | 56            | 76                | 72              |

Figure 13. Efficiency for 230 Vac (LLC)

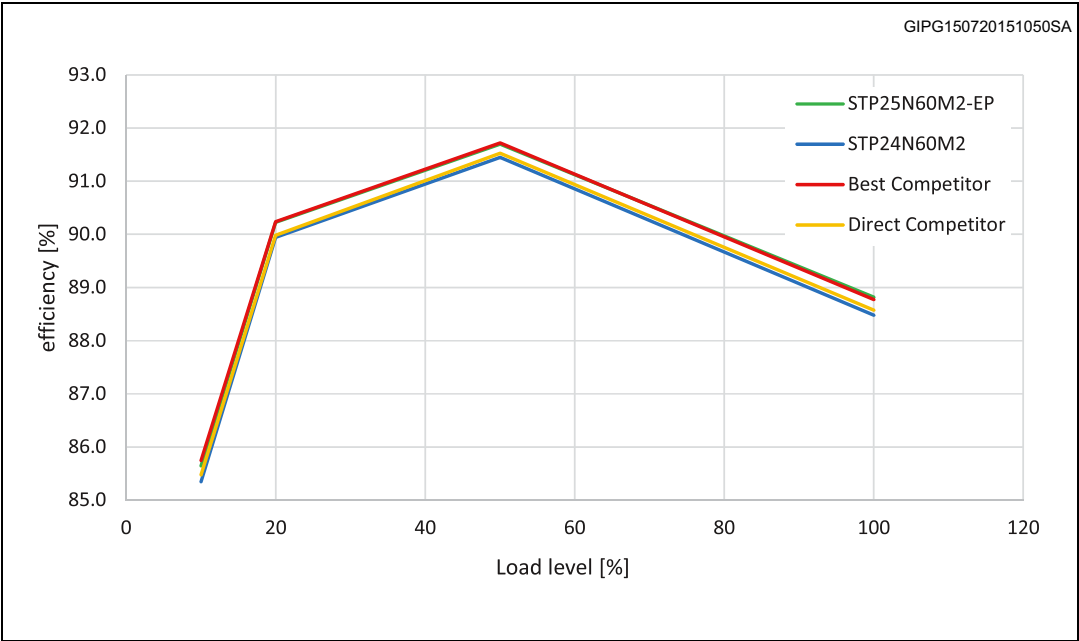
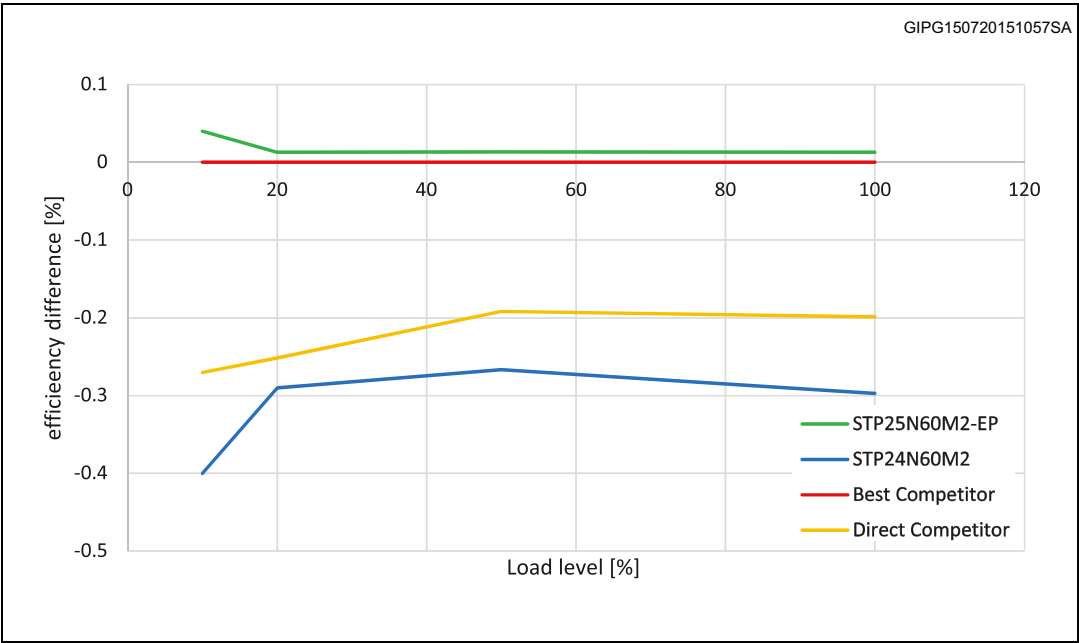


Figure 14. Efficiency difference for 230 Vac





### 3.3 Efficiency measurement in a 200 W PFC

In this section, the devices with principal characteristics in [Table 5](#) are compared. The test vehicle is the PFC section of an EVAL6599 board.

The test conditions are:

- $V_{\text{mains}} = 90 - 264 \text{ Vac}$
- $V_{\text{OUT}} = 430 \text{ V}$
- $P_{\text{OUT}} = 0 \text{ to } 200 \text{ W}$
- $f_{\text{SW}} = 100 \text{ kHz}$

The efficiency measurements in [Figure 15](#) and [16](#) again demonstrate the advantages of the M2-EP devices over not only the M2 devices but also over the best competition. The more significant improvement in efficiency is measured under light load conditions, where  $Q_g$  and  $C_{\text{OSS}}$  play a decisive role.

**Table 5. Electrical characteristics of compared devices (STP24N60M2, STP25N60M2-EP and competitors)**

|                                                                | STP24N60M2 | STP25N60M2-EP | Best competitor | Main competitor |
|----------------------------------------------------------------|------------|---------------|-----------------|-----------------|
| $BV_{\text{dss min}}[\text{V}] @ 1 \text{ mA}$                 | 600        | 600           | 600             | 600             |
| $V_{\text{th}}[\text{V}] @ 250 \mu\text{A}$                    | 2 - 4      | 2 - 4         | 2.5 - 3.5       | 2.5 - 3.5       |
| $R_{\text{on max}}[\text{m}\Omega] @ 10 \text{ V}/9 \text{ A}$ | 190        | 188           | 199             | 190             |
| $Q_g[\text{nC}]$                                               | 29         | 29            | 32              | 63              |
| $C_{\text{iss}}[\text{pF}] @ 100 \text{ V}$                    | 1060       | 1090          | 1520            | 1400            |
| $C_{\text{OSS}}[\text{pF}] @ 100 \text{ V}$                    | 55         | 56            | 72              | 85              |

Figure 15. Efficiency for 230 Vac (PFC CCM, 100 kHz, diode STTH8R06)

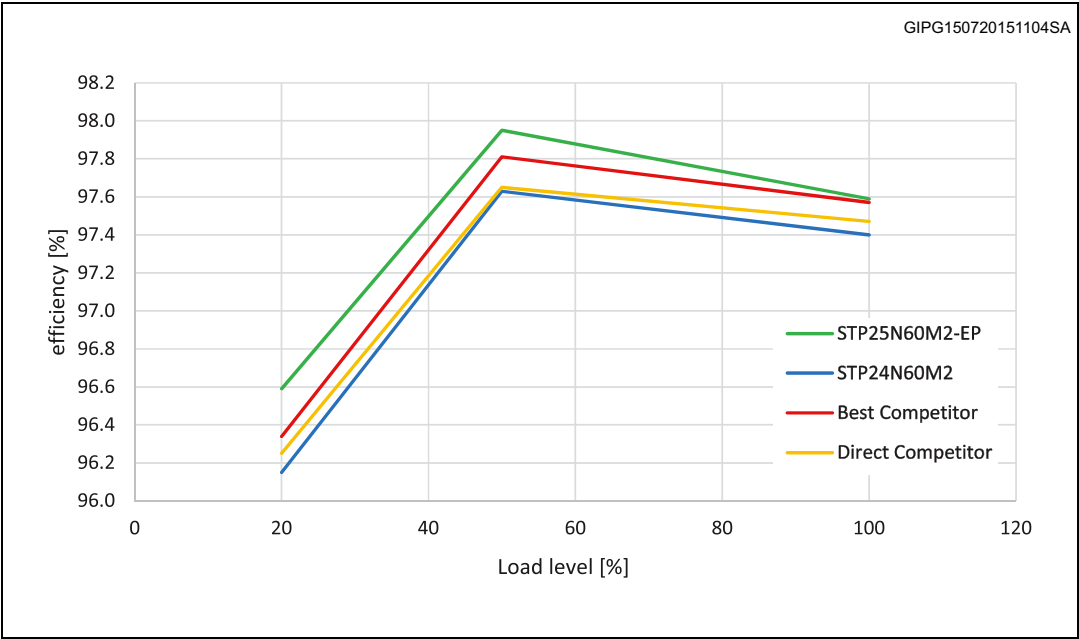
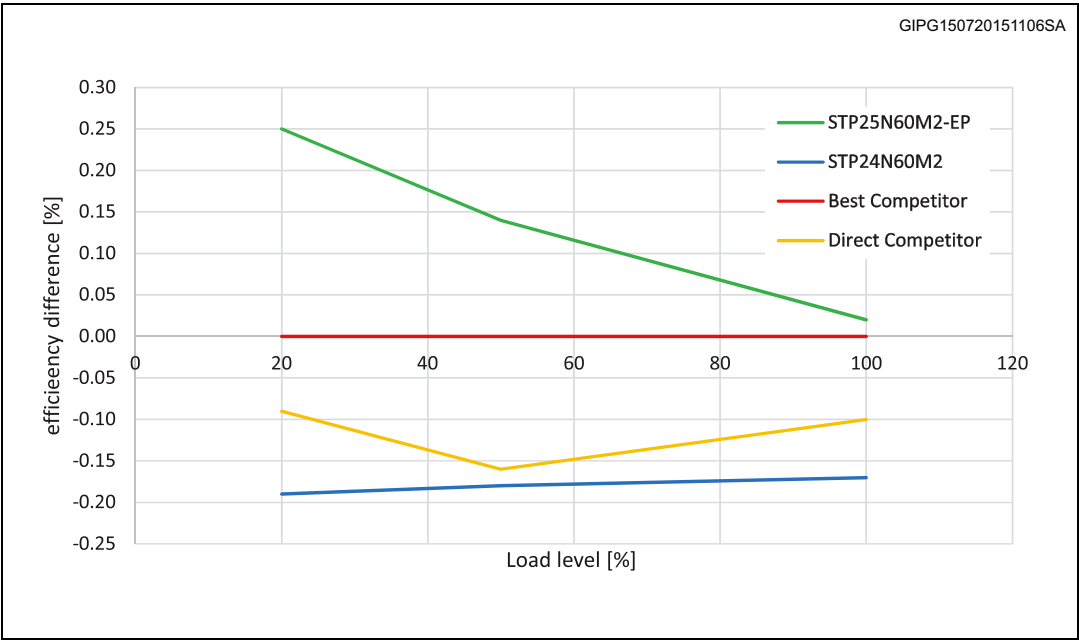


Figure 16. Efficiency difference for 230 Vac (PFC CCM, 100 KHz, diode STTH8R06)



### 3.4 Efficiency measurement in a 150 W LLC

In this section, the devices with principal characteristics in [Table 6](#) are compared. The test vehicle is the LLC section of an STEVAL-ISA143V1, a 12 V - 150 W resonant converter with synchronous rectification using the L6563H, L6699 and SRK2000 [\[10\]](#).

The test conditions are:

- $V_{\text{mains}} = 230 \text{ Vac}$
- $V_{\text{OUT}} = 12 \text{ V}$
- $P_{\text{OUT}} = 0 \text{ to } 150 \text{ W}$

The efficiency measurement in [Figure 17](#) and [18](#) demonstrates the advantage of M2-EP devices over not only the M2 devices, but also over the best competition. Under light load conditions a 0.3% and 0.15% efficiency improvement is measured with respect to M2 and best competitor devices.

**Table 6. Electrical characteristics of compared devices (STF13N60M2, STF15N60M2-EP and competitors)**

|                                                                 | STF13N60M2 | STF15N60M2-EP | Best competitor | Direct competitor |
|-----------------------------------------------------------------|------------|---------------|-----------------|-------------------|
| $BV_{\text{dss min}}[\text{V}] @ 1 \text{ mA}$                  | 600        | 600           | 600             | 600               |
| $V_{\text{th}} [\text{V}] @ 250 \mu\text{A}$                    | 2 - 4      | 2 - 4         | 2.5 - 3.5       | 2.5 - 3.5         |
| $R_{\text{on max}} [\text{m}\Omega] @ 10 \text{ V}/5 \text{ A}$ | 380        | 378           | 385             | 380               |
| $Q_{\text{g}} [\text{nC}]$                                      | 17         | 17            | 17              | 32                |
| $C_{\text{iss}} [\text{pF}] @ 100 \text{ V}$                    | 580        | 585           | 790             | 700               |
| $C_{\text{oss}} [\text{pF}] @ 100 \text{ V}$                    | 32         | 33            | 38              | 46                |

Figure 17. Efficiency for 230 Vac (LLC))

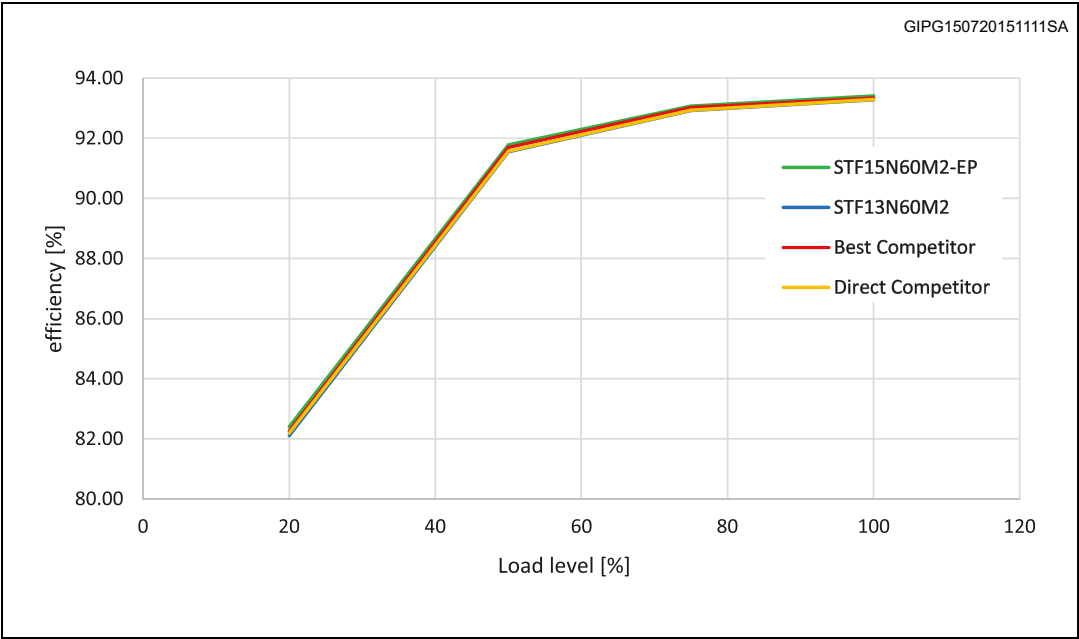
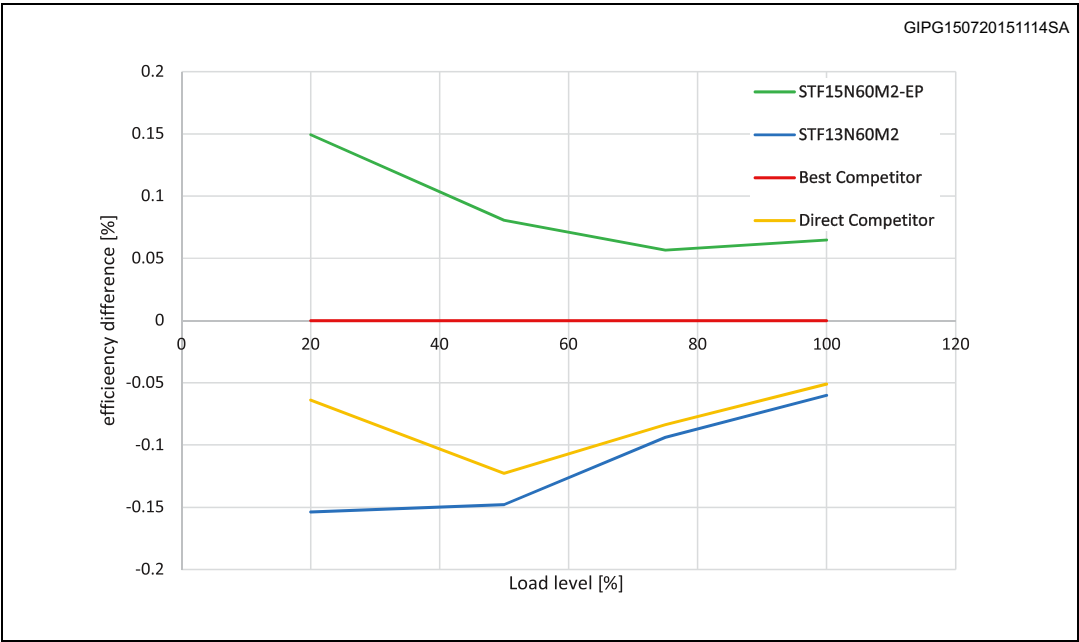


Figure 18. Efficiency difference for 230 Vac (LLC)



## 4 Conclusion

This application note presents the new M2-EP STMicroelectronics super-junction technology and compares it against both the previous M2 and other competitor solutions. This technology represents an evolution in the preceding M2 series obtained via the optimization of the overall column aspect, thus leading to gate charge and output capacitance improvements and efficiency increases in hard and soft switching applications.

Tests were performed on several application boards to compare device performance. The results show that the output capacitance profile influences the switching operation and determines the total efficiency of the system. The optimization of this aspect in MDmesh™ M2 EP devices allows higher efficiency, especially when the system operates under light load conditions.

## 5 References

1. X. Chen. US Patent 5 216 275, 1993.
2. F. Frisina. US Patent 6 586 798, 2003.
3. J. Fedison, M. Fornage, M. Harrison and D. Zimmanck, "Coss related energy loss in power MOSFETs used in zero-voltage-switched applications," in APEC 2014, Fort Worth, TX, 2014.
4. D. Pattanayak and O. Tornblad, "Large-signal and small-signal output capacitances of Super Junction MOSFETs," in ISPSD 2013, Kanazawa, 2013.
5. J. Strydom, J. van Wyk and J. Ferreira, "Capacitor Measurements for Power Electronic Application," in 34th IAS Annual Meeting, Phoenix, US, 1999.
6. STMicroelectronics, AN2450 - LLC resonant half-bridge converter design guideline, 2014.
7. STMicroelectronics, AN2644 - An introduction to LLC resonant half-bridge converter, 2008.
8. STMicroelectronics, AN4720 Half Bridge Resonant LLC Converters and Primary Side MOSFET Failure Mechanism, 2015.
9. STMicroelectronics, "500 W fully digital AC-DC power supply (D-SMPS) based on STM32F334C8 microcontroller".
10. STMicroelectronics, "12 V - 150 W resonant converter with synchronous rectification using the L6563H, L6699 and SRK2000,".

## 6 Revision history

**Table 7. Document revision history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 27-Jul-2015 | 1        | Initial release. |

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved