AN4823
Application note

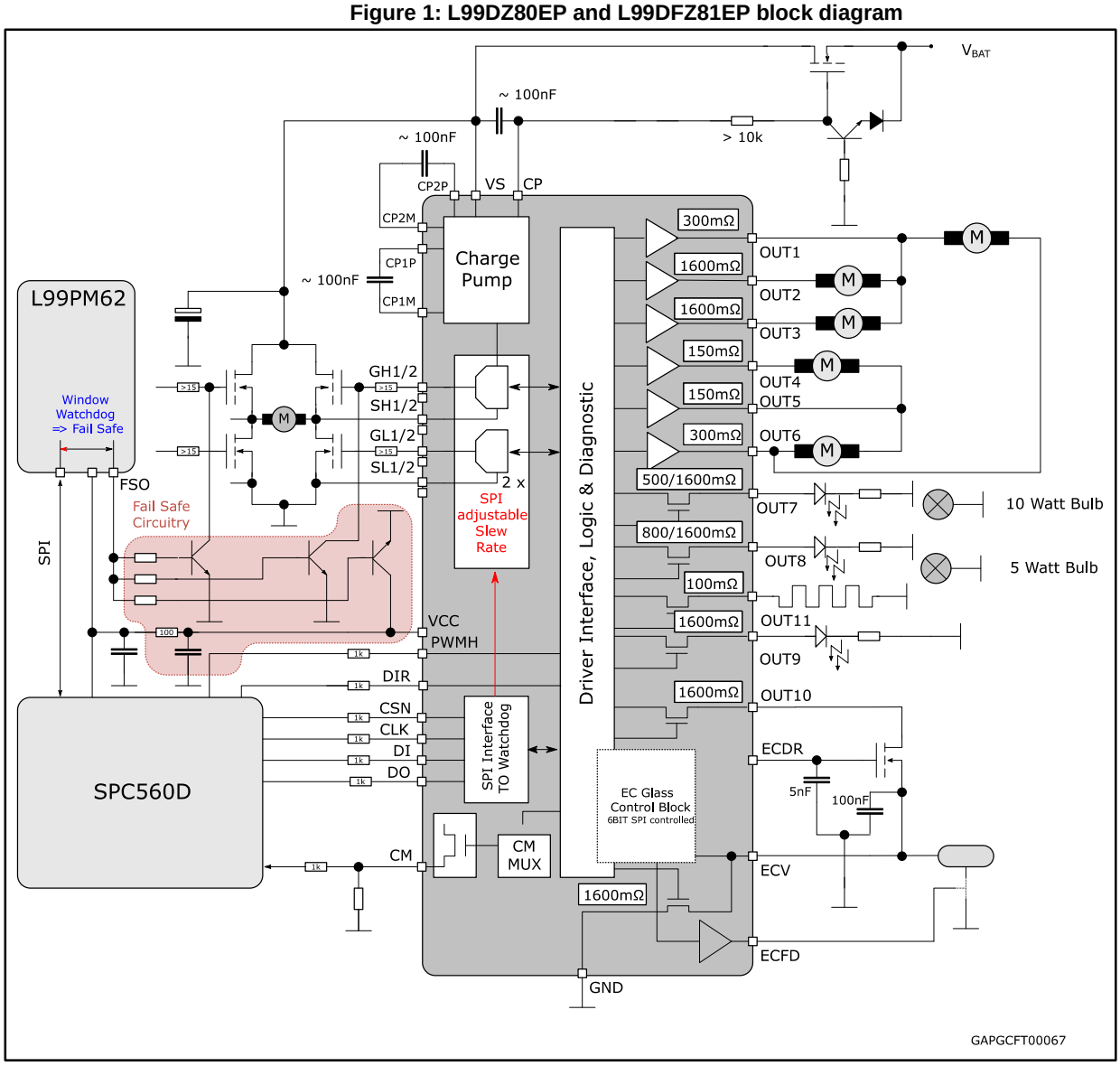
L99DZ80EP/L99DZ81EP H-bridge driver switching consideration and Rgate calculation

Introduction

This document gives information about H-bridge driver embedded in the L99DZ80EP and L99DZ81EP: those devices include an SPI-programmable slew-rate circuit that drives 4 external MOSFETs in a H-bridge configuration supporting electric-window applications.

1 Block diagram

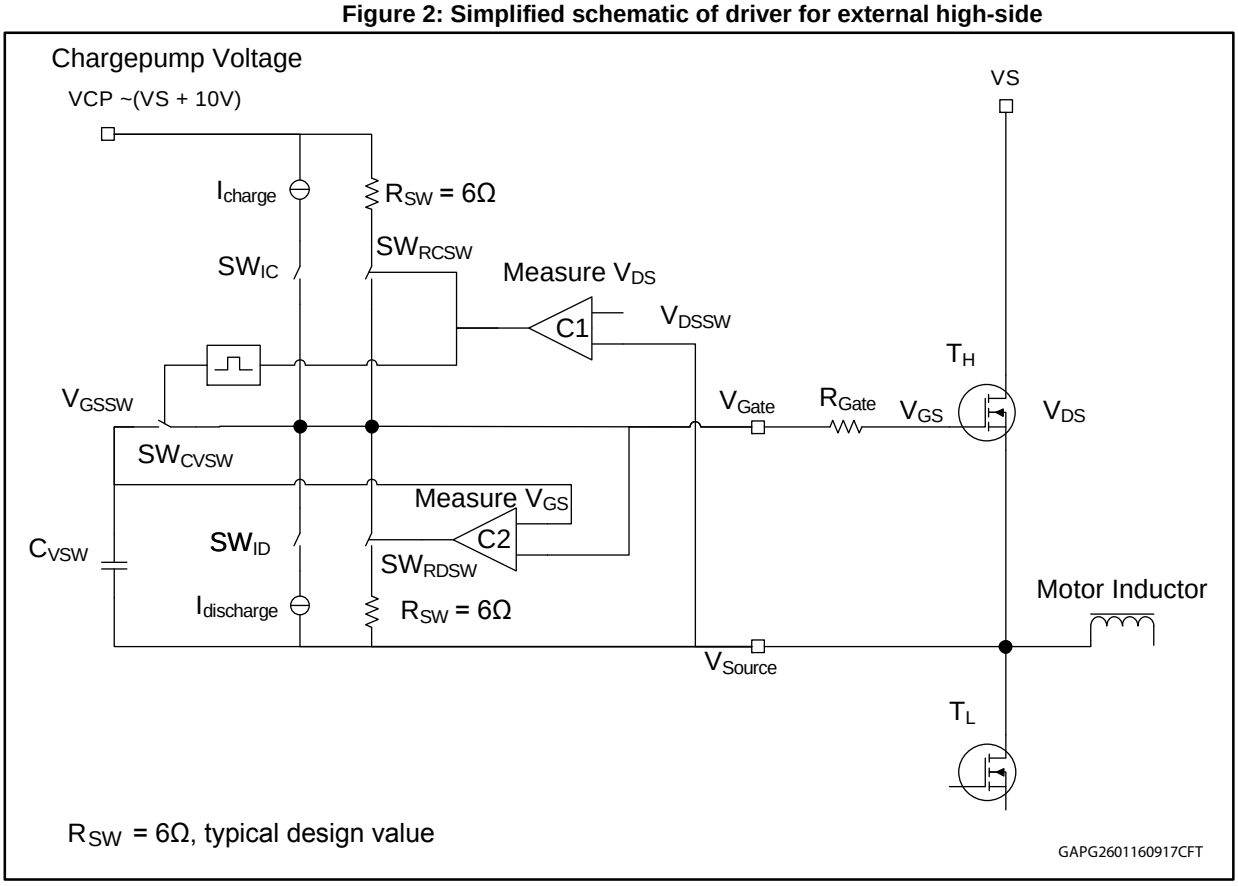
Figure 1: L99DZ80EP and L99DFZ81EP block diagram



L99DZ80EP and L99DZ81EP devices provide, through pins GH1/2, GL1/2 and SL1/2, dedicated driving signals to the external 4 MOSFETs.

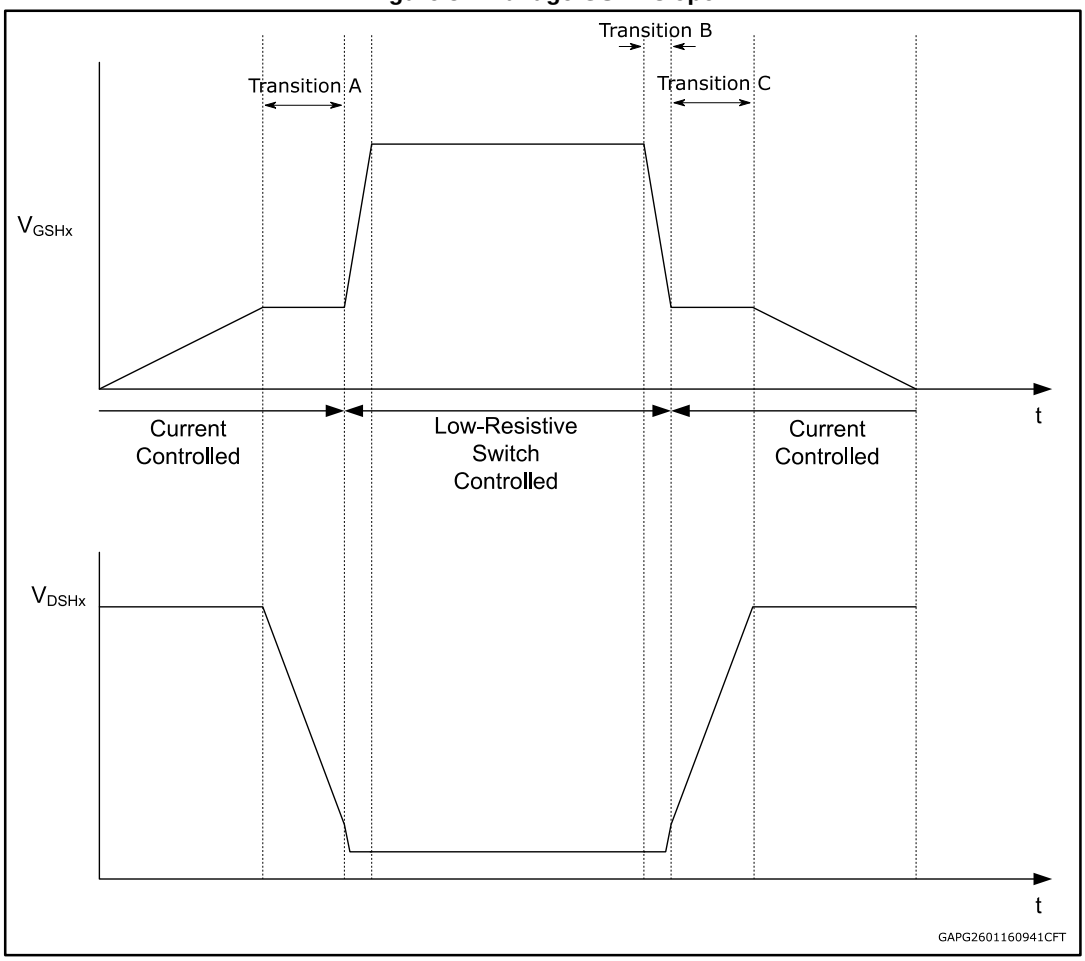
2 L99DZ80EP/L99DZ81EP smart switching details

Figure 2: Simplified schematic of driver for external high-side



Typical curves are described in the following figure.

Figure 3: H-bridge GSHx slope



Some transitions are now analyzed:

Transition A

Threshold voltage ext FET sampled and stored in C_{VSW} during Miller Plateau ↔ V_{TH}.

During this phase, threshold stored in C_{VSW} during Miller Plateau is increased by I_{Charge} * R_{Gate} in reference to V_{TH} of the external MOSFET

Transition B

Switch-off started with R_{SW}, "hard switching".

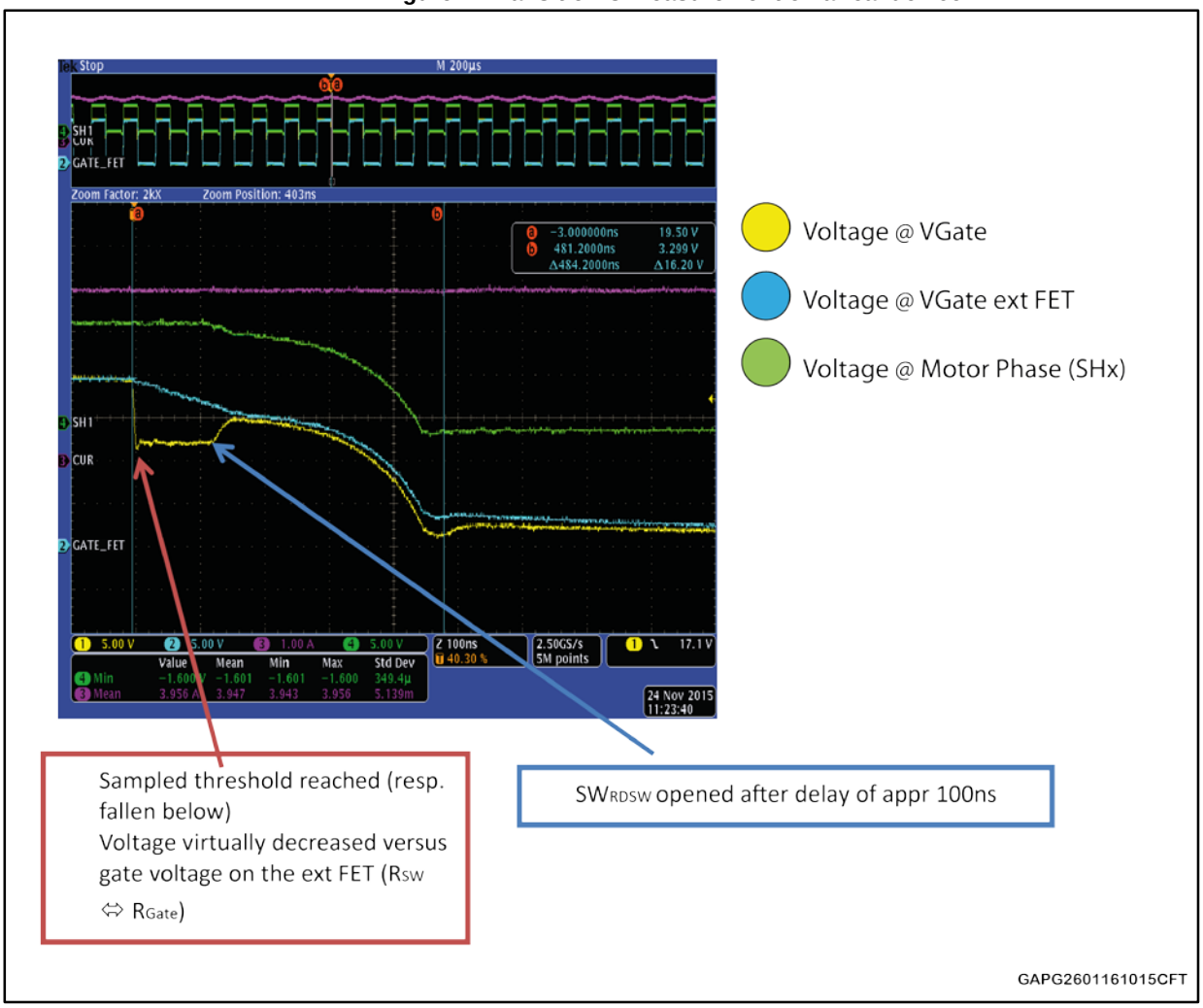
Transition C

- Reaching V_{TH}, R_{SW} is turned-off by opening SW_{RDSW}
- Opening of SW_{RDSW} is done with a certain delay
- Afterwards gate discharge is done by the programmed current source ($I_{discharge}$)

During this phase, V_{Gate} is decreased by resistive divider R_{SW} ↔ R_{gate} and "Virtually" the threshold to switch from switch mode to current mode is lower than real gate source voltage on external FET.

Figure 4: "Transition C measurement on a real device" shows measurements performed on a real device.

Figure 4: Transition C measurement on a real device



2.1 How to choose a proper Rgate resistance

Charge in the beginning of turn-off phase is discharged by the hard switch in series with the external gate resistance. Average current during this phase is approximately (5V + V_{TH}/2) / (R_{SW} + R_{Gate}).

Due to virtual decreased sample voltage (by resitive divider R_{SW} & R_{Gate}) the transistion from switch mode to current control mode is started almost immediately after start of turn-off of ext FET (depending on size of R_{Gate}).

Delay of opening SW_{RDSW} is approximately 100 ns (typical value).

During this time Q_{gate} must NOT be discharged to ensure to enter Q_{GD} plateau. As rule of thumb the according R_{gate} can be calculated by the following formula:

$R_{Gate} \geq (5V + VTH/2) * 100ns / Q_{Gate} - R_{SW}$

That value of R_{Gate} is needed to enter current source mode.

Table 1: Rgate values as per different MOSFET choice

MOSFET	Q_{Total} (nC)	Q_{GD} (nC)	Q_{GS} (nC)	$Q_{Total} - Q_{GD} - Q_{GS}$ (nC)	V_{TH} @ 40A (V)	Calculated $R_{Gate} \approx$ (Ω)
ST STD64N4F6AG	44	15	12	18	5.5	38
ST STD80N4F6AG	36	9	11	16	4.8	41
ST VNH7013	36	5	8,5	22.5	Not specified (2 ... 4)	28 (@VTH = 5V)
Supplier A	45	12.6	10	22.4	4V	26
Supplier B	17.2	2.4	8	6.8	5.5V	109

3 Revision history

Table 2: Document revision history

Date	Revision	Changes
17-Feb-2016	1	Initial release.
29-Feb-2016	2	Updated *Figure 2: "Simplified schematic of driver for external high-side"* *Section 2.1: "How to choose a proper Rgate resistance"*: • Updated equation

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