AN4831
Application note

Migrating from STM32F2x5 line to STM32L4 Series and STM32L4+ Series microcontrollers

Introduction

For the designers of STM32 microcontroller applications, being able to easily replace one microcontroller type by another in the same product family is an important asset. Migrating an application to a different microcontroller is often needed, when the product requirements grow, putting extra demands on the memory size, or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and to shrink the PCB area.

This application note analyzes the steps required to migrate an existing design from STM32F2x5 line devices to STM32L4 Series and STM32L4+ Series devices. It groups together the most important information and lists the vital aspects that need to be addressed.

This document lists the “full set” of features available for the STM32F2x5 line and the equivalent features on the STM32L4 Series and STM32L4+ Series (some products may have less features depending on their part number).

In order to migrate an application to the STM32L4 Series or STM32L4+ Series, four aspects need to be considered: the hardware migration, the peripheral migration, the firmware migration and the software migration.

To fully benefit from this application note, the user must be familiar with the STM32 microcontroller documentation available on *www.st.com*, with a particular focus on:

- The STM32F205/215 line reference manuals:
  - *STM32F205xx, STM32F207xx, STM32F215xx and STM32F217xx advanced Arm®-based 32-bit MCUs* (RM0033)
- The STM32F205/215 line datasheets.
  - *Arm®-based 32-bit MCU, 150DMIPs, up to 1 MB Flash/128+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm.interfaces & camera* (DS6329)
  - *Arm®-based 32-bit MCU, 150DMIPs, up to 1MB Flash/128+4KB RAM, crypto, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs,, 15 comm. interfaces & camera* (DS6697)
- The STM32L4 Series reference manuals:
  - RM0351 (STM32L4x6xx, STM32L4x5xx)
  - RM0394 (STM32L41xxx, STM32L42xxx, STM32L43xxx, STM32L44xxx, STM32L45xxx, STM32L46xxx)
  - RM0392 (STM32L471xx)
- The STM32L4 Series datasheets
- The STM32L4+ Series reference manuals:
  - RM0432 (STM32L4+ Series)
- The STM32L4+ Series datasheets

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1 STM32L4 Series and STM32L4+ Series overview

STM32L4 Series and STM32L4+ Series have a perfect fit in terms of ultra-low-power, performances, memory size, and peripherals at a cost effective price.

In particular, both STM32L4 Series and STM32L4+ Series allow a high frequency/performance operation, including an Arm®[a] Cortex®-M4 @ up to 120 MHz and an optimized Flash memory access through the adaptive real-time memory accelerator (ART Accelerator™).

The STM32L4 Series and STM32L4+ Series devices increase the low-power efficiency in Dynamic mode (µA/MHz) still reaching a very low level of static power consumption on various available low-power modes.

The detailed list of available features and packages for each product can be found in the respective datasheet.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 1 lists the memory availability for each product.

Table 1. STM43L4 Series and STM32L4+ Series memory availability

Part number	Flash size		RAM size		
	Size	Bank	SRAM1	SRAM2	SRAM3
STM32L4S9xx	2 Mbytes	Dual	192 Kbytes	64 Kbytes	384 Kbytes
STM32L4R9xx					
STM32L4S7xx					
STM32L4R7xx					
STM32L4S5xx					
STM32L4R5xx					
STM32L496xx	1 Mbyte		256 Kbytes	64 Kbytes	-
STM32L4A6xx					-
STM32L476xx	1 Mbyte		96 Kbytes	32 Kbytes	-
STM32L486xx					-
STM32L471xx					-
STM32L475xx					-
STM32L451xx	512 Kbytes	Single	128 Kbytes		-
STM32L452xx					-
STM32L462xx					-
STM32L433xx	256 Kbytes		48 Kbytes	16 Kbytes	-
STM32L443xx					-
STM32L432xx					-
STM32L442xx					-
STM32L431xx					-
STM32L422xx	128 Kbytes		32 Kbytes	8 Kbytes	-
STM32L412xx					-

The STM32L4 Series and STM32L4+ Series devices include a larger set of peripherals with advanced features compared to the STM32F2x5 line, such as:

- Advanced encryption hardware accelerator (AES)
- Touch sensing controller (TSC)
- Controller area network (bxCAN)
- Single wire protocol interface (SWPMI)
- Serial audio interface (SAI)
- Low-power UART (LPUART)
- Infrared interface (IRTIM)
- Low-power timer (LPTIM)
- Liquid crystal display controller (LCD)
- Digital filter for sigma delta modulators (DFSDM) (for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L47xxx/48xxx and STM32L45xxx/46xxx)
- Operational amplifiers (OPAMP)
- Voltage reference buffer (VREFBUF)
- Digital to analog converter with low power Sample and Hold feature (DAC)
- Quad-SPI interface (QUADSPI)
- Octo-SPI (OCTOPSI) (for STM32L4+ Series)
- OCTOSPI IO Manager (OCTOSPIM) (for STM32L4+ Series)
- Display serial interface (DSI) (for STM32L4R9xx/4S9xx)
- LCD-TFT Display Controller (LTDC) (for STM32L4R7xx/4S7xx/4R9xx/4S9xx)
- DMA request multiplexer (DMAMUX) (for STM32L4+ Series)
- Graphic MMU (GFXMMU) (for STM32L4+ Series)
- Flexible memory controller (FMC) (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices)
- Firewall (FW)
- Clock recovery system (CRS) for USB (for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices)
- SRAM1 size is different on the various STM32L4xxxx devices:
  - 192 Kbytes for STM32L4+ Series
  - 256 Kbytes for STM32L49xxx/4Axxx
  - 96 Kbytes for STM32L47xxx/48xxx
  - 128 Kbytes for STM32L45xxx/46xxx
  - 48 Kbytes for STM32L43xxx/44xxx
  - 32 Kbytes for STM32L41xxx/42xxx
- Additional SRAM2 with data preservation in Standby mode:
  - 64 Kbytes for STM32L4+ Series and STM32L49xxx/4Axxx
  - 32 Kbytes for STM32L47xxx/48xxx and STM32L45xxx/46xxx
  - 16 Kbytes for STM32L43xxx/44xxx
  - 8 Kbytes for STM32L41xxx/42xxx
- Additional SRAM3 for STM32L4+ Series:
  - 384 Kbytes
- Dual bank boot and 8-bit ECC on Flash memory (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx)
- Rail-to-rail comparators (COMP)

The STM32L4 Series and STM32L4+ Series also provide an optimized power consumption and enriched set of low-power modes.

The STM32F2x5 line contains a few peripherals that are not available on all the STM32L4 Series / STM32L4+ Series, but that are present only in some STM32L4xxxx devices such as: DCMI (present on STM32L4+ Series, STM32L496xx/L4A6xx), HASH (present on STM32L4Sxxx and STM32L4A6xx), CRYPT, ETH, USB OTG-HS, DMA2D, DSI (present on STM32L4R9xx/4S9xx), OCTOSPI (present on STM32L4R9xx/4S9xx), LTDC (present on STM32L4R9xx/4S9xx), DMAMUX (present on STM32L4R9xx/4S9xx), GFXMMU (present on STM32L4R9xx/4S9xx).

The STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices implement an USB FS device only instead of an USB OTG FS. They also implement reduced Flash size (512 Kbytes for STM32L45xxx/46xxx devices, 256 Kbytes for STM32L43xxx/44xxx, 128 Kbytes for STM32L43xxx/44xxx devices).

This migration guide is only covering the migration from the STM32F2x5 line to the STM32L4 Series or STM32L4+ Series devices and as a consequence the new features present on STM32L4 Series / STM32L4+ Series but not already present on the STM32F2x5 line are not covered in this document (refer to the STM32L4 Series and STM32L4+ Series reference manuals and datasheets for an exhaustive picture).

2 Hardware migration

2.1 Package availability

The STM32F2 Series and STM32L4 Series / STM32L4+ Series devices have a wide selection of packages. The STM32F2x5 line offers spreads from 64 to 176 pin packages while the STM32L4 Series / STM32L4+ Series products offer spreads from 32 to 169 pin packages.

The available packages in the STM32L4 Series are listed in *Table 2*.

Table 2. Packages available on STM32L4 Series and STM32L4+ Series

Package(1)	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
UFQFPN32	-	-	-	-	X	X	(5 x 5)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L432xx, STM32L442xx
LQFP32	-	-	-	-	-	X	(5 x 5)	STM32L412xx, STM32L422xx
LQFP48	-	-	-	-	X	X	(7 x 7)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx
UFQFPN48	-	-	-	X	X	X	(7 x 7)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx
WLCSP36	-	-	-	-	-	X	(2.85 x 3.07)	STM32L412xx, STM32L422xx
WLCSP49	-	-	-	-	X	-	(3.141 x 3.127)	STM32L431xx, STM32L433xx, STM32L443xx
WLCSP64	-	-	-	-	X	-	(3.141 x 3.127)	STM32L431xx, STM32L433xx, STM32L443xx

Table 2. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[(1)]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
LQFP64	-	X	X	X	X	X	(10 x 10)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx
UFBGA64	-	-	-	X	X	X	(5 x 5)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx
WLCSP64	-	-	-	X	-	-	(3.357 x 3.657)	STM32L451xx, STM32L452xx, STM32L462xx
WLCSP72	-	-	X	-	-	-	(4.4084 x 3.7594)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx
WLCSP81	-	-	X	-	-	-	(4.4084 x 3.7594)	STM32L476xx
WLCSP100	-	X	-	-	-	-	(4.618 x 4.142)	STM32L496xx, STM32L4A6xx

Table 2. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package(1)	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
LQFP100	X	X	X	X	X	-	(14 x 14)	STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx
UFBGA100	-	-	X	X	X	-	(7 x 7)	STM32L431xx, STM32L433xx, STM32L443xx
UFBGA132	X	X	X	-	-	-	(7 x 7)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4S5xx
UFBGA144	X	-	-	-	-	-	(10 x 10)	STM32L4R9xx, STM32L4S9xx
LQFP144	X	X	X	-	-	-	(20 x 20)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx

Table 2. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package(1)	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
WLCSP144	X	-	-	-	-	-	(5.24 x 5.24)	STM32L4R5xx, STM32L4R7xx, STM32L4R9xx, STM32L4S5xx, STM32L4S7xx, STM32L4S9xx
UFBGA169	X	X	-	-	-	-	(7 x 7)	STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx

1. X = supported.

The available packages in the STM32F2x5 line are listed in *Table 3*.

Table 3. Packages available on STM32F2x5 line

Package(1)	STM32F2x5 line	
	STM32F205xx	STM32F215xx
UFQFPN32	-	-
UFQFPN48	-	-
WLCSP49	-	-
WLCSP64	-	-
WLCSP64+2	X	-
WLCSP72	-	-
WLCSP81	-	-
LQFP48	-	-
LQFP64	X	X
LQFP100	X	X
LQFP144	X	X
LQFP176	X	X
UFBGA64	-	-
UFBGA100	-	-
UFBGA 132	-	-
UFBGA176	X	X

1. X = supported.

For a detailed package availability and package selection, refer to the STM32F2 Series and STM32L4 Series / STM32L4+ Series microcontroller documentation available on *www.st.com.*

Both families present a high level of pin compatibility. Most peripherals share the same pins. The transition between the two families is easy since only a few pins are different.

Table 4 compares the pinout between the STM32F2x5 line and the STM32FL4 Series devices for the 64, 100, and 144 pin packages.

Table 4. STM32F2x5 line and STM32L4 Series / STM32L4+ Series pinout differences (QFP)

STM32F2X5 line				STM32L4 Series / STM32L4+ Series			
QFP64	QFP100	QFP144	Pinout	QFP64	QFP100	QFP144	Pinout
-	19	30	**VDD**	-	19	30	**VSSA**(1)(2)(3)(4)
-	20	31	**VSSA**	-	20	31	**VREF-**(1)(2)(3)(4)
12	-	-	**VSSA**	12	-	-	**VSSA/VREF-**(1)(2)(3)(4)(5)
13	-	-	**VDDA**	13	-	-	**VDDA/VREF+**(1)(2)(3)(4)(5)
31	49	71	**VCAP_1**	31	49	71	**VSS**(1)(2)(3)(4)(5)
47	-	-	**VCAP_2**	47	-	-	**VSS**(1)(2)(3)(4)(5)
48	-	-	**VDD**	48	-	-	**VDDUSB**(1)(2)(3)(5)(6)
-	-	95	**VDD**	-	-	95	**VDDIO2**(1)(2)(6)
-	73	106	**VCAP_2**	-	73	106	**VDDUSB**(1)(2)(3)(4)(6)
-	-	131	**VDD**	-	-	131	**VDDIO2**(1)(2)(6)
60	94	138	**BOOT0**	60	94	-	**PH3/BOOT0**(1)(2)(3)(4)(5)
-	99	143	**RFU**	-	99	143	**VSS**(1)(2)(3)(4)

1. For STM32L49xxx/4Axxx devices.
2. For STM32L47xxx/48xxx devices.
3. For STM32L45xxx/46xxx devices.
4. For STM32L43xxx/44xxx devices.
5. For STM32L41xxx/42xxx devices.
6. VDDUSB and VDDIO2 pins can be connected externally to VDD.

Note: STM32L4R9xx/4S9xx are not compatible with STM32L4 Series / STM32L4+ Series, for more details refer to the application note "Migration between STM32L476xx/486xx and STM32L4+ Series microcontrollers" (AN5017).

Recommendations to migrate from the STM32F2x5 line board to the STM32L4 Series and STM32L4+ Series boards

The VDD pin (pin 19 on QFP100) is now used as VSSA in STM32L4 Series / STM32L4+ Series.

A dedicated V_{DDUSB} supply is used in STM32L4 Series / STM32L4+ Series. It must be connected to the VDDUSB pin (pin 48 on QFP64, pin 73 on QFP100, pin 36 on QFPN48 and pin C11 on BGA100). In the STM32F2x5 line the pin was used for VCAP_2 (QFP100, BGA100) (not needed for STM32L4 Series / STM32L4+ Series) or VDD (QFP64, QFPN48).

Figure 1, *Figure 2* and *Figure 3* show examples of board designs migrating from the STM32F2x5 line to the STM32L4 Series / STM32L4+ Series.

See also *Getting started with STM32L4 Series and STM32L4+ Series hardware development* application note (AN4555).

Figure 1. Compatible board design: LQFP144

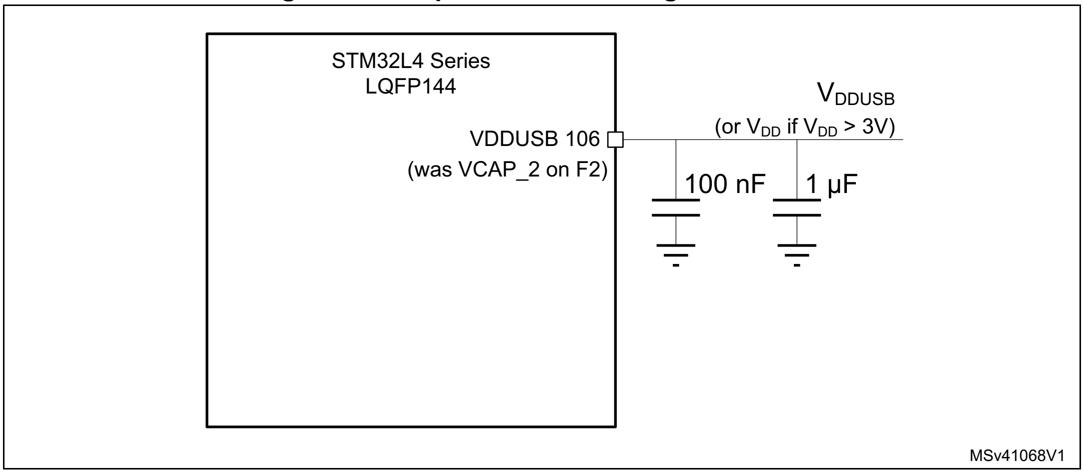


Figure 2. Compatible board design: LQFP100

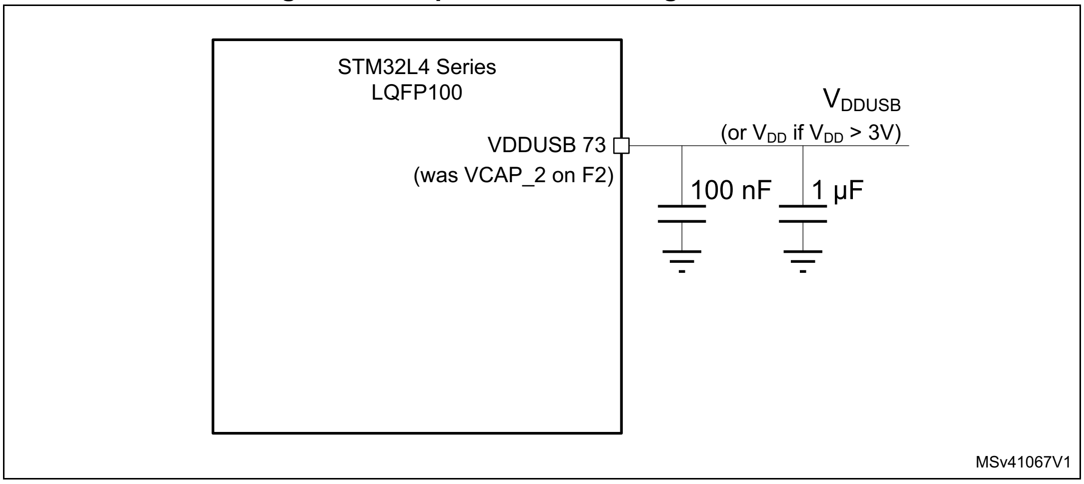
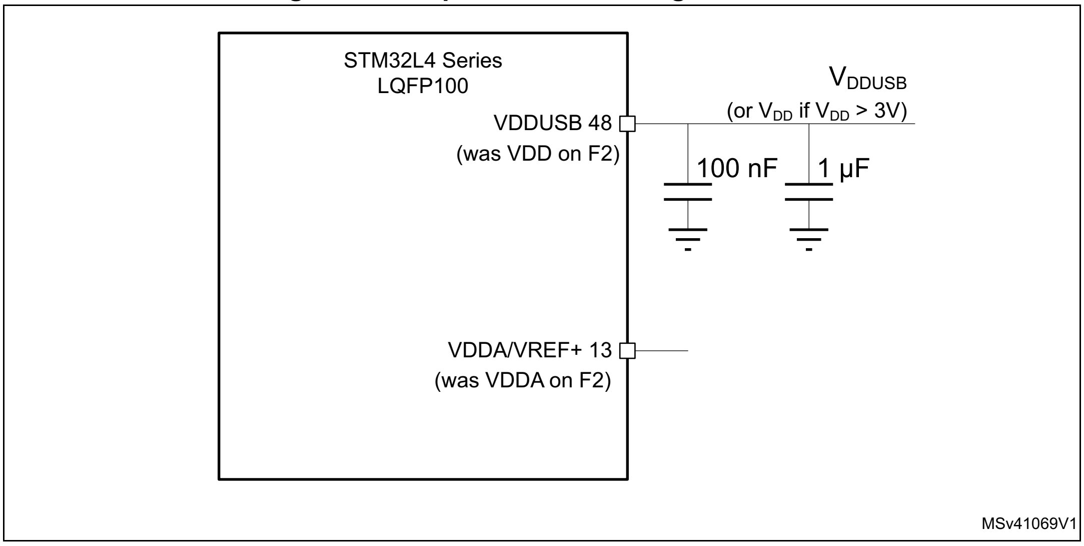


Figure 3. Compatible board design: LQFP64



SMPS packages

Some STM32L4 Series and STM32L4+ Series devices offer a package option allowing the connection of an external SMPS. This is done through two VDD12 pins that are replacing two existing pins in the package baseline.

The compatibility is kept between the STM32L4 Series / STM32L4+ Series derivatives regarding those two pins (the replaced pins are different across the package types but are the same for all the derivatives on similar packages). Refer to the product datasheet for details.

3 Boot mode selection

The STM32F2x5 line and the STM32L4 Series / STM32L4+ Series devices can select the boot modes between three options: boot from the main Flash memory, boot from SRAM or boot from the system memory.

However, the way to select the boot mode differs between the products.

In the STM32F2x5 line, the boot mode is selected with two pins: BOOT0 and BOOT1.

In the STM32L47xxx/48xxx devices, the boot mode is selected with one pin (BOOT0) and the nBOOT1 option bit located in the user option bytes at memory address 0x1FFF7800.

In the STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices, the boot mode is selected with the nBOOT1 option bit and the pin BOOT0 or the nBOOT0 option bit depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register as shown in *Table 6*.

Table 5 and *Table 6* summarize the different configurations available for selecting the boot mode.

Table 5. Boot modes for STM32L47xxx/48xxx devices and STM32F2x5 line

STM32L47xxx/48xxx devices and STM32F2x5 line boot mode selection		Boot mode	Aliasing
BOOT1(1)	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM1	Embedded SRAM1 is selected as boot space

1. The BOOT1 value is the opposite of the nBOOT1 option bit.

Table 6. Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices

nBOOT1 FLASH_OPTR [23]	nBOOT0 FLASH_OPTR [27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR [26]	Main Flash empty(1)	Boot memory space alias
X	X	0	1	0	Main Flash memory is selected as boot area
X	X	0	1	1	System memory is selected as boot area
X	1	X	0	X	Main Flash memory is selected as boot area
0	X	1	1	X	Embedded SRAM1 is selected as boot area
0	0	X	0	X	Embedded SRAM1 is selected as boot area
1	X	1	1	X	System memory is selected as boot area
1	0	X	0	X	System memory is selected as boot area

1. Only for the STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices: a Flash empty check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed (0xFFFF FFFF) and if the boot selection is configured to boot from the main Flash memory.

Embedded bootloader

On the STM32F2x5 line devices, the bootloader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through the DFU (device firmware upgrade).

The embedded bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

Table 7. Bootloader interfaces

Peripheral	Pin	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
DFU	USB_DM (PA11) USB_DP (PA12)	X	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	-	-
	USART2_TX (PA2) USART2_RX (PA3)	-	X

Table 7. Bootloader interfaces (continued)

Peripheral	Pin	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
USART3	USART3_TX (PB10) USART3_RX (PB11)	X	-
	USART3_TX (PC10) USART3_RX (PC11)	X	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	-	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	-	X
I2C3	I2C3_SCL (PA8) I2C3_SDA (PB4)	-	-
	I2C3_SCL (PC0) I2C3_SDA (PC1)	-	X
I2C4	I2C4_SCL (PD12) I2C4_SDA (PD13)	-	X(1)
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	-	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	-	X
CAN1	CAN1_RX (PB8) CAN1_TX (PB9)	-	X(2)
CAN2	CAN2_RX (PB5) CAN2_TX (PB6)	X	X(3)

1. Only for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L45xxx/46xxx.
2. Not available on STM32L41xxx/42xxx.
3. Only for STM32L49xxx/4Axxx.

For more details on the bootloader, refer to *STM32 microcontroller system boot mode* application note (AN2606).

For smaller packages, it is important to check the pin and peripheral availability.

4 Peripheral migration

4.1 STM32 product cross-compatibility

The STM32 series embed a set of peripherals that can be classified in three groups:

- The first group is for the peripherals that are common to all products. Those peripherals are identical on all the products, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second group is for the peripherals that present minor differences from one product to another (usually differences due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third group is for peripherals which have been considerably modified from one product to another (new architecture, new features...). For this category of peripherals, migration will require new development at application level.

Table 8 gives a general overview of this classification.

The “software compatibility” mentioned in *Table 8* only refers to the register description for “low level” drivers.

The STMCube™ hardware abstraction layer (HAL) between the STM32F2x5 line and the STM32L4 Series / STM32L4+ Series devices is compatible.

Table 8. STM32 peripheral compatibility analysis STM32F2x5 line versus STM32L4 Series / STM32L4+ Series

Peripheral	Number of instances in STM32							Compatibility (migrating from STM32F2x5 line to STM32L4 Series / STM32L4+ Series)		
	F205/ F215	L4Rxxx /4Sxxx	L49xxx /4Axxx	L47xxx /48xxx	L45xxx /46xxx	L43xxx /44xxx	L41xxx /42xxx	Software	Pinout	Comments
SPI	3	3					2	Partial	Partial	– I2S is no longer supported by SPI, but it is replaced by a dedicated serial audio interface (SAI) on STM32L4 Series / STM32L4+ Series – Some alternate functions are not mapped on the same GPIO for SPI2/SPI3
I2S (full duplex)	2	0								
WWDG	1	1						Full	NA	-
IWDG	1	1						Full	NA	-
DBGMCU	1	1						Full	NA	-
CRC	1	1						Partial	NA	Additional features on STM32L4 Series / STM32L4+ Series

Table 8. STM32 peripheral compatibility analysis STM32F2x5 line versus STM32L4 Series / STM32L4+ Series (continued)

<table>
<tr><th rowspan="2">Peripheral</th><th colspan="7">Number of instances in STM32</th><th colspan="3">Compatibility
(migrating from STM32F2x5 line to STM32L4 Series / STM32L4+ Series)</th></tr>
<tr><th>F205/
F215</th><th>L4Rxxx
/4Sxxx</th><th>L49xxx
/4Axxx</th><th>L47xxx
/48xxx</th><th>L45xxx
/46xxx</th><th>L43xxx
/44xxx</th><th>L41xxx
/42xxx</th><th>Software</th><th>Pinout</th><th>Comments</th></tr>
<tr><td>EXTI</td><td>1</td><td colspan="6">1</td><td>Partial</td><td>Full</td><td>Only PH2 GPIO is not available as EXTI input on STM32L4 Series / STM32L4+ Series</td></tr>
<tr><td>USB OTG FS</td><td>1</td><td colspan="3">1</td><td colspan="3">0</td><td>Partial</td><td>Partial</td><td>Additional features on STM32L4 Series / STM32L4+ Series</td></tr>
<tr><td>USB OTG HS</td><td>1</td><td colspan="6">0</td><td>NA</td><td>NA</td><td>-</td></tr>
<tr><td>USB FS</td><td>0</td><td colspan="3">0</td><td colspan="3">1</td><td>NA</td><td>NA</td><td>-</td></tr>
<tr><td>DMA</td><td>2</td><td colspan="6">2</td><td>None</td><td>NA</td><td>– Different devices have different features
– DMA mapping requests differ
– See Section 4.3: Direct memory access controller (DMA) for details</td></tr>
<tr><td>TIM
Basic
General P.
Advanced
Low-power
IRTIM</td><td>2
10
2
0
0</td><td colspan="3">2
7
2
2
1</td><td>2
4
1
2
1</td><td>2
3
1
2
1</td><td>1
3
1
2
1</td><td>Full</td><td>Partial</td><td>– Some pins are not mapped on the same GPIO
– The timer instance names may differ
– Internal connections may differ</td></tr>
<tr><td>SDIO/ SDMMC</td><td>1</td><td colspan="5">1</td><td>0</td><td>Full</td><td>Full</td><td>Some pins are not mapped on the same GPIO</td></tr>
<tr><td>PWR</td><td>1</td><td colspan="6">1</td><td>Partial</td><td>NA</td><td>-</td></tr>
<tr><td>RCC</td><td>1</td><td colspan="6">1</td><td>Partial</td><td>NA</td><td>-</td></tr>
<tr><td>USART
UART
LPUART</td><td>4
2
0</td><td colspan="3">3
2
1</td><td>3
1
1</td><td colspan="2">3
0
1</td><td>Partial</td><td>Full</td><td>– Additional features on STM32L4 Series / STM32L4+ Series
– Fully compatible pinout for USART1/2/3</td></tr>
<tr><td>I2C</td><td>3</td><td colspan="2">4</td><td>3</td><td>4</td><td colspan="2">3</td><td>None</td><td>Partial</td><td>– Fully compatible pinout for I2C1/2
– I2C3 mapped on different GPIOs
– Additional features on STM32L4 Series / STM32L4+ Series</td></tr>
</table>

Table 8. STM32 peripheral compatibility analysis STM32F2x5 line versus STM32L4 Series / STM32L4+ Series (continued)

Peripheral	Number of instances in STM32							Compatibility (migrating from STM32F2x5 line to STM32L4 Series / STM32L4+ Series)		
	F205/ F215	L4Rxxx /4Sxxx	L49xxx /4Axxx	L47xxx /48xxx	L45xxx /46xxx	L43xxx /44xxx	L41xxx /42xxx	Software	Pinout	Comments
ADC	1	1	3	3	1	1	2	None	Partial	– Additional features on STM32L4 Series / STM32L4+ Series – Some pins are mapped on different GPIOs
RTC	1	1						Partial	Partial	Additional features on STM32L4 Series / STM32L4+ Series
FLASH	1	1	2	2	1	1	1	None	NA	New peripheral
GPIO	Up to 114 IOs	Up to 140 IOs	Up to 136 IOs	Up to 114 IOs	Up to 83 IOs	Up to 83 IOs	Up to 52 IOs	Full	Full	At reset the STM32F2x5 line devices are configured in Input-floating mode while the STM32L4 Series / STM32L4+ Series devices are configured on Analog mode
SYSCFG	1	1						Partial	NA	-
CAN	2	1	2	1			0	Partial	Full	– CAN1 pins fully compatible – CAN2 is present only on STM32L496xx/4A6xx
DAC channels	2	2			1	2	0	Partial	Partial	Additional features on STM32L4 Series / STM32L4+ Series
DCMI	1	1		0				NA	NA	DCMI is present on STM32L496xx/4A6xx and STM32L4+ Series
HASH **CRYPT**	1 1	1 0		0 0				NA	NA	HASH is present on STM32L4Sxxx and STM32L496xx/4A6xx
ETH	1	0						NA	NA	-
SDIO	1	0						NA	NA	-

Color key:
- = No compatibility (new feature or new architecture)
- = Partial compatibility (minor changes)
- = Not applicable

4.2 Memory mapping

The peripheral address mapping has been changed in STM32L4 Series / STM32L4+ Series compared to STM32F2x5 line.

Table 9 provides the peripheral address mapping correspondence between STM32F2x5 line and STM32L4 Series / STM32L4+ Series.

Table 9. Peripheral address mapping differences (1)

Peripheral	STM32F2x5 line		STM32L4 Series / STM32l4+ Series	
	Bus	Base address	Bus	Base address
FSMC control register	AHB3	0xA000 0000	AHB3	0xA000 0000
RNG	AHB2	0x5006 0800	AHB2	0x5006 0800
HASH	AHB2	0x5006 0400	AHB2	0x5006 0400
CRYP	AHB2	0x5006 0000	-	-
AES	-	-	AHB2	0x5006 0000
DCMI	AHB2	0x5005 0000	AHB2	0x5005 0000
USB OTG FS	AHB2	0x5000 0000	AHB2	0x5000 0000
USB OTG HS	AHB1	0x4004 0000	-	-
ETHERNET MAC	AHB1	0x4002 9000	-	-
ETHERNET MAC	AHB1	0x4002 8C00	-	-
ETHERNET MAC	AHB1	0x4002 8800	-	-
ETHERNET MAC	AHB1	0x4002 8400	-	-
ETHERNET MAC	AHB1	0x4002 8000	-	-
DMA2	AHB1	0x4002 6400	AHB1	0x4002 0400
DMA1	AHB1	0x4002 6000	AHB1	0x4002 0000
BKPSRAM	AHB1	0x4002 4000	-	
TSC	-	-	AHB1	0x4002 4000
Flash interface	AHB1	0x4002 3C00	AHB1	0x4002 2000
RCC	AHB1	0x4002 3800	AHB1	0x4002 1000
CRC	AHB1	0x4002 3000	AHB1	0x4002 3000
GPIOI	AHB1	0x4002 2000	AHB2	0x4800 2000
GPIOH	AHB1	0x4002 1C00	AHB2	0x4800 1C00
GPIOG	AHB1	0x4002 1800	AHB2	0x4800 1800
GPIOF	AHB1	0x4002 1400	AHB2	0x4800 1400
GPIOE	AHB1	0x4002 1000	AHB2	0x4800 1000
GPIOD	AHB1	0X4002 0C00	AHB2	0x4800 0C00
GPIOC	AHB1	0x4002 0800	AHB2	0x4800 0800
GPIOB	AHB1	0x4002 0400	AHB2	0x4800 0400

Table 9. Peripheral address mapping differences (continued)(1)

Peripheral	STM32F2x5 line		STM32L4 Series / STM32l4+ Series	
	Bus	Base address	Bus	Base address
GPIOA	AHB1	0x4002 0000	AHB2	0x4800 0000
DFSDM	-	-	APB2	0x4001 6000
SAI2	-	-	APB2	0x4001 5800
SAI1	-	-	APB2	0x4001 5400
TIM17	-	-	APB2	0x4001 4800
TIM16	-	-	APB2	0x4001 4400
TIM15	-	-	APB2	0x4001 4000
TIM11	APB2	0x4001 4800	-	-
TIM10	APB2	0x4001 4400	-	-
TIM9	APB2	0x4001 4000	-	-
EXTI	APB2	0x4001 3C00	APB2	0x4001 0400
SYSCFG	APB2	0x4001 3800	APB2	0x4001 0000
SPI1	APB2	0x4001 3000	APB2	0x4001 3000
SDIO	APB2	0x4001 2C00	-	-
SDMMC1	-	-	APB2	– 0x4001 2800 – 0x5006 2400 AHB2 For STM32L4Rxxx/ 4Sxxx
FIREWALL	-	-	APB2	0x4001 1C00
ADC1 - ADC2 - ADC3	APB2	0x4001 2000	AHB2	0x5004 0000
USART6	APB2	0x4001 1400	-	-
USART1	APB2	0x4001 1000	APB2	0x4001 3800
TIM8	APB2	0x4001 0400	APB2	0x4001 3400
COMP	-	-	APB2	0x4001 0200
VREFBUF	-	-	APB2	0x4001 0030
TIM1	APB2	0x4001 0000	APB2	0x4001 2C00
LPTIM2	-	-	APB1	0x4000 9400
SWPMI1	-	-	APB1	0x4000 8800
LPUART1	-	-	APB1	0x4000 8000
LPTIM1	-	-	APB1	0x4000 7C00
OPAMP	-	-	APB1	0x4000 7800
DAC	APB1	0x4000 7400	APB1	0x4000 7400
PWR	APB1	0x4000 7000	APB1	0x4000 7000

Table 9. Peripheral address mapping differences (continued)[(1)]

Peripheral	STM32F2x5 line		STM32L4 Series / STM32l4+ Series	
	Bus	Base address	Bus	Base address
bxCAN	APB1	0x4000 6400	-	-
CAN1	-	-	APB1	0x4000 6400
CAN2	-	-	APB1	0x4000 6800
I2C4	-	-	APB1	0x4000 8400
I2C3	APB1	0x4000 5C00	APB1	0x4000 5C00
I2C2	APB1	0x4000 5800	APB1	0x4000 5800
I2C1	APB1	0x4000 5400	APB1	0x4000 5400
UART5	APB1	0x4000 5000	APB1	0x4000 5000
UART4	APB1	0x4000 4C00	APB1	0x4000 4C00
USART3	APB1	0x4000 4800	APB1	0x4000 4800
USART2	APB1	0x4000 4400	APB1	0x4000 4400
SPI3 / I2S3	APB1	0x4000 3C00	APB1	0x4000 3C00
SPI2 / I2S2	APB1	0x4000 3800	APB1	0x4000 3800
IWDG	APB1	0x4000 3000	APB1	0x4000 3000
WWDG	APB1	0x4000 2C00	APB1	0x4000 2C00
RTC & BKP Registers	APB1	0x4000 2800	APB1	0x4000 2800
LCD	-	-	APB1	0x4000 2400
TIM14	APB1	0x4000 2000	-	-
TIM13	APB1	0x4000 1C00	-	-
TIM12	APB1	0x4000 1800	-	-
TIM7	APB1	0x4000 1400	APB1	0x4000 1400
TIM6	APB1	0x4000 1000	APB1	0x4000 1000
TIM5	APB1	0x4000 0C00	APB1	0x4000 0C00
TIM4	APB1	0x4000 0800	APB1	0x4000 0800
TIM3	APB1	0x4000 0400	APB1	0x4000 0400
TIM2	APB1	0x4000 0000	APB1	0x4000 0000
USB SRAM	-	-	APB1	0x40006C00
USB FS	-	-	APB1	0x40006800
CRS	-	-	APB1	0x40006000
OCTOSPI2	-	-	AHB3	0xA000 1400
OCTOSPI1	-	-		0xA000 1000
OCTOSPIM	-	-	AHB2	0x5006 1C00

Table 9. Peripheral address mapping differences (continued)(1)

Peripheral	STM32F2x5 line		STM32L4 Series / STM32l4+ Series	
	Bus	Base address	Bus	Base address
GFXMMU	-	-	AHB1	0x4002 C000
DMAMUX1	-	-		0x4002 0800
DSIHOST	-	-	APB2	0x4001 6C00
LCD-TFT	-	-		0x4001 6800

Color key:
= base address or bus change
= not applicable, new peripheral

1. On the STM32L4 Series / STM32L4+ Series devices on which the peripheral is not implemented, the memory address is reserved.

The system memory mapping has been updated between the STM32F2x5 line and the STM32L4 Series / STM32L4+ Series devices, refer to the device's reference manuals or datasheets for more details.

Regarding the SRAM

All the STM32F20/21xxx devices embed:
- Up to 128 Kbytes of **system SRAM.**
- 4 Kbytes of **backup SRAM**. The content of this area is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

STM32L4 Series and STM32L4+ Series devices feature an additional SRAM (SRAM2) of 64 Kbytes on STM32L4+ Series and STM32L49xxx/4Axxx, 32 Kbytes on STM32L47xxx/48xxx and STM32L45xxx/46xxx, 16 Kbytes on STM32L43xxx/44xxx, 8 Kbytes on STM32L41xxx/42xxx and an additional SRAM (SRAM3) of 384 Kbytes available only in STM324Rxxx/4Sxxx.

The SRAM2 includes the additional features listed below:
- Maximum performance through ICode bus access without physical remap
- Parity check option (32-bit + 4-bit parity check)
- Write protection with 1 Kbyte granularity
- Readout protection (RDP)
- Erase by system reset (option byte) or by software
- Content is preserved in Low-power run, Low-power sleep, Stop 0, Stop 1, Stop 2 mode
- Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1).

Bit-banding on Cortex-M3

Both the STM32F2x5 line and STM32L4 Series / STM32L4+ Series devices support bit-banding on the lowest 1 Mbyte of the SRAM and on the peripheral memory region.

However the peripherals mapped in this bit-banding region are not the same on each series of products.

Peripherals accessible with bit-banding:

- STM32F2x5 line: all the peripherals except FSMC, RNG, HASH, CRYPT, DCMI, USB OTG FS registers.
- STM32L4 Series / STM32L4+ Series: all the peripherals except FSMC, RNG, AES, USB OTG FS, GPIOx, ADC registers.

4.3 Direct memory access controller (DMA)

The STM32F2x5 line devices implement a “general purpose enhanced” DMA compared to the STM32L4 Series / STM32L4+ Series.

For STM32L4+ Series, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer. In STM32L476xx/486xx, the DMA request line is connected directly to the peripherals.

The DMAMUX request multiplexer allows a DMA request line to be routed between the peripherals and the DMA controllers of the product. The routine function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

Table 10 shows the main differences.

Table 10. DMA differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

DMA	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Architecture	Dual AHB master: – 1 DMA controller for memory accesses – 1 DMA controller for peripheral accesses	Both DMA controllers can access the memory and the peripherals
Streams	– 8 streams per controller – 8 channels per stream	– 7 channels per controller (“streams” in STM32F2x5 line) – 8 requests per channel (“channels” in STM32F2x5 line)
Data management	4-word depth 32 first-in, first-out memory buffers (FIFOs) per stream, that can be used in FIFO mode or Direct mode	NA
Color key: = Feature not available (NA) = Highlights a difference between STM32F2x5 line and STM32L4 Series / STM32l4+ Series		

Table 11 presents the correspondence between the peripheral DMA requests in the STM32F2x5 line and in the STM32L4 Series / STM32L4+ Series devices.

Table 11. DMA request differences migrating STM32F2x5 line to STM32L4 Series / STM32L4+ Series

Peripheral	DMA request	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
ADC	ADC1	DMA2_Stream0 DMA2_Stream4	DMA1_Channel1 DMA2_Channel3
	ADC2	DMA2_Stream2 DMA2_Stream3	DMA1_Channel2 DMA2_Channel4
	ADC3	DMA2_Stream0 DMA2_Stream1	DMA1_Channel3 DMA2_Channel5
DAC	DAC1_CH1	DMA1_Stream5	DMA2_Channel4 DMA1_Channel3
	DAC1_CH2	DMA1_Stream6	DMA2_Channel5 DMA1_Channel4
DFSDM	DFSDM0	NA	DMA1_Channel4
	DFSDM1		DMA1_Channel5
	DFSDM2		DMA1_Channel6
	DFSDM3		DMA1_Channel7
DCMI	DCMI	NA	DMA2_Channel7 DMA2_Channel5
CRYPT	CRYPT_OUT	DMA2_Stream5	NA
	CRYPT_IN	DMA2_Stream6	
HASH	HASH_IN	NA	DMA2_Channel7
AES	AES_IN	NA	DMA2_Channel1 DMA2_Channel5
	AES_OUT		DMA2_Channel2 DMA2_Channel3
SDIO	SDIO	DMA2_Stream3 DMA2_Stream6	NA
SDMMC	SDMMC1	NA	DMA2_Channel4 DMA2_Channel5
LPUART	LPUART_RX	NA	DMA2_Channel7
	LPUART_TX		DMA2_Channel6
UART	UART4_RX	DMA1_Stream2	DMA2_Channel5
	UART4_TX	DMA1_Stream4	DMA2_Channel3
	UART5_RX	DMA1_Stream0	DMA2_Channel2
	UART5_TX	DMA1_Stream7	DMA2_Channel1

Table 11. DMA request differences migrating STM32F2x5 line to STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
USART	USART1_RX	DMA2_Stream2 DMA2_Stream5	DMA1_Channel5 DMA2_Channel7
	USART1_TX	DMA2_Stream7	DMA1_Channel4 DMA2_Channel6
	USART2_RX	DMA1_Stream5	DMA1_Channel6
	USART2_TX	DMA1_Stream6	DMA1_Channel7
	USART3_RX	DMA1_Stream1	DMA1_Channel3
	USART3_TX	DMA1_Stream3 DMA1_Stream4	DMA1_Channel2
	USART6_RX	DMA2_Stream1 DMA2_Stream2	NA
	USART6_TX	DMA2_Stream6 DMA2_Stream7	
SPI	SPI1_RX	DMA2_Stream0 DMA2_Stream2	DMA1_Channel2 DMA2_Channel3
	SPI1_TX	DMA2_Stream3 DMA2_Stream5	DMA1_Channel3 DMA2_Channel4
	SPI2_RX	DMA1_Stream3	DMA1_Channel4
	SPI2_TX	DMA1_Stream4	DMA1_Channel5
SPI	SPI3_RX	DMA1_Stream0 DMA1_Stream2	DMA2_Channel1
	SPI3_TX	DMA1_Stream5 DMA1_Stream7	DMA2_Channel2
	QUADSPI	NA	DMA2_Channel7 DMA1_Channel5
I2C	I2C1_RX	DMA1_Stream0 DMA1_Stream5	DMA1_Channel7 DMA2_Channel6
	I2C1_TX	DMA1_Stream6 DMA1_Stream7	DMA1_Channel6 DMA2_Channel7
	I2C2_RX	DMA1_Stream2 DMA1_Stream3	DMA1_Channel4
	I2C2_TX	DMA1_Stream7	DMA1_Channel4
	I2C3_RX	DMA1_Stream2	DMA1_Channel3
	I2C3_TX	DMA1_Stream4	DMA1_Channel2
	I2C4_RX	NA	DMA2_Channel1
	I2C4_TX		DMA2_Channel2

Table 11. DMA request differences migrating STM32F2x5 line to STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
I2S	**I2S2_ext_RX**	DMA1_Stream3	NA
	I2S2_ext_TX	DMA1_Stream4	
	I2S3_ext_RX	DMA1_Stream2 DMA1_Stream0	
	I2S3_ext_TX	DMA1_Stream5	
TIM1	**TIM1_CH1**	DMA2_Stream6	DMA1_Channel2
	TIM1_CH2	DMA2_Stream6	DMA1_Channel3
	TIM1_CH3	DMA2_Stream6	NA
	TIM1_TRIG	DMA2_Stream0	
	TIM1_CH1	DMA2_Stream1	
	TIM1_CH2	DMA2_Stream2	
	TIM1_CH1	DMA2_Stream3	
	TIM1_CH4	DMA2_Stream4	DMA1_Channel4
	TIM1_TRIG	DMA2_Stream4	DMA1_Channel4
	TIM1_COM	DMA2_Stream4	DMA1_Channel4
	TIM1_UP	DMA2_Stream5	DMA1_Channel6
	TIM1_CH3	DMA2_Stream6	DMA1_Channel7
TIM2	**TIM2_UP**	DMA1_Stream1	DMA1_Channel2
	TIM2_CH3	DMA1_Stream1	DMA1_Channel1
	TIM2_CH1	DMA1_Stream5	DMA1_Channel5
	TIM2_CH2	DMA1_Stream6	DMA1_Channel7
	TIM2_CH4	DMA1_Stream6	DMA1_Channel7
	TIM2_UP	DMA1_Stream7	NA
	TIM2_CH4	DMA1_Stream7	
TIM3	**TIM3_CH4** **TIM3_UP** **TIM3_CH1** **TIM3_TRIG** **TIM3_CH2** **TIM3_CH3**	DMA1_Stream2 DMA1_Stream2 DMA1_Stream4 DMA1_Stream4 DMA1_Stream5 DMA1_Stream7	DMA1_Channel3 DMA1_Channel3 DMA1_Channel6 DMA1_Channel6 NA DMA1_Channel2
TIM4	**TIM4_CH1** **TIM4_CH2** **TIM4_UP** **TIM4_CH3**	DMA1_Stream0 DMA1_Stream3 DMA1_Stream6 DMA1_Stream7	DMA1_Channel1 DMA1_Channel4 DMA1_Channel7 DMA1_Channel5

Table 11. DMA request differences migrating STM32F2x5 line to STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
TIM5	TIM5_CH3	DMA1_Stream0	DMA2_Channel2
	TIM3_UP	DMA1_Stream0	DMA2_Channel2
	TIM5_CH4	DMA1_Stream1	DMA2_Channel1
	TIM5_TRIG	DMA1_Stream1	DMA2_Channel1
	TIM5_CH1	DMA1_Stream2	DMA2_Channel5
	TIM5_CH4	DMA1_Stream3	NA
	TIM5_TRIG	DMA1_Stream3	
	TIM5_CH2	DMA1_Stream4	DMA2_Channel4
	TIM5_UP	DMA1_Stream6	NA
	TIM5_COM	NA	DMA2_Channel1
TIM6	TIM6_UP	DMA1_Stream1	DMA2_Channel4 DMA1_Channel3
TIM7	TIM7_UP	DMA1_Stream2 DMA1_Stream4	DMA2_Channel5 DMA1_Channel4
TIM8	TIM8_CH1	DMA2_Stream2	DMA2_Channel6
	TIM8_CH2	DMA2_Stream2	DMA2_Channel7
	TIM8_CH3	DMA2_Stream2	DMA2_Channel1
	TIM8_UP	DMA2_Stream1	DMA2_Channel1
	TIM8_CH1	DMA2_Stream2	NA
	TIM8_CH2	DMA2_Stream3	
	TIM8_CH3	DMA2_Stream4	
	TIM8_CH4	DMA2_Stream7	DMA2_Channel2
	TIM8_TRIG	DMA2_Stream7	DMA2_Channel2
	TIM8_COM	DMA2_Stream7	DMA2_Channel2
TIM15	TIM15_CH1 TIM15_UP TIM15_TRIG TIM15_COM	NA	DMA1_Channel5 DMA1_Channel5 DMA1_Channel5 DMA1_Channel5
TIM16	TIM16_CH1 TIM16_UP TIM16_CH1 TIM16_UP		DMA1_Channel3 DMA1_Channel3 DMA1_Channel6 DMA1_Channel6
TIM17	TIM17_CH1 TIM17_UP TIM17_CH1 TIM17_UP		DMA1_Channel1 DMA1_Channel1 DMA1_Channel7 DMA1_Channel7

Table 11. DMA request differences migrating STM32F2x5 line to STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
SAI	SAI1_A	NA	DMA2_Channel1 DMA2_Channel6
	SAI1_B		DMA2_Channel2 DMA2_Channel7
	SAI2_A		DMA1_Channel6 DMA2_Channel3
	SAI2_B		DMA1_Channel7 DMA2_Channel4
SWPMI	SWPMI_RX		DMA2_Channel1
	SWPMI_TX		DMA2_Channel2

Color key:

= Feature not available (NA)

= Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

1. On the STM32L4 Series and STM32L4+ Series devices on which the peripheral is not implemented, the DMA request is reserved.

4.4 Interrupts

Table 12 presents the interrupt vectors in the STM32F2x5 line devices compared to the STM32L4 Series / STM32L4+ Series devices.

Table 12. Interrupt vector differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series

Position	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
0	WWDG	WWDG
1	PVD	PVD / PVM
2	TAMP_ STAMP	TAMPER / CSS
3	RTC_WKUP	RTC_WKUP
4	FLASH	FLASH
5	RCC	RCC
6	EXTI0	EXTI0
7	EXTI1	EXTI1
8	EXTI2	EXTI2
9	EXTI3	EXTI3
10	EXTI4	EXTI4
11	DMA1_Stream0	DMA1_Channel1

Table 12. Interrupt vector differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series (continued)

Position	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
12	DMA1_Stream1	DMA1_Channel2
13	DMA1_Stream2	DMA1_Channel3
14	DMA1_Stream3	DMA1_Channel4
15	DMA1_Stream4	DMA1_Channel5
16	DMA1_Stream5	DMA1_Channel6
17	DMA1_Stream6	DMA1_Channel7
18	ADC	ADC1_2
19	CAN1_TX	CAN1_TX
20	CAN1_RX0	CAN1_RX0
21	CAN1_RX1	CAN1_RX1
22	CAN1_SCE	CAN1_SCE
23	EXTI9_5	EXTI9_5
24	TIM1_BRK / TIM9	TIM1_BRK / TIM15
25	TIM1_UP / TIM10	TIM1_UP / TIM16
26	TIM1_TRG_COM / TIM11	TIM1_TRG_COM / TIM17
27	TIM1_CC	TIM1_CC
28	TIM2	TIM2
29	TIM3	TIM3
30	TIM4	TIM4
31	I2C1_EV	I2C1_EV
32	I2C1_ER	I2C1_ER
33	I2C2_EV	I2C2_EV
34	I2C2_ER	I2C2_ER
35	SPI1	SPI1
36	SPI2	SPI2
37	USART1	USART1
38	USART2	USART2
39	NA	USART3
40	EXTI15_10	EXTI15_10
41	RTC_Alarm	RTC_Alarm
42	OTG_FS_WKUP	DFSDM3
43	TIM8_BRK	TIM8_BRK
44	TIM8_UP	TIM8_UP

Table 12. Interrupt vector differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series (continued)

Position	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
45	TIM8_TRG_COM	TIM8_TRG_COM
46	TIM8_CC	TIM8_CC
47	DMA1_Stream7	ADC3
48	FSCM	FMC
49	SDIO	SDMMC
50	TIM5	TIM5
51	SPI3	SPI3
52	UART4	UART4
53	UART5	UART5
54	TIM6_DAC	TIM6_DACUNDER
55	TIM7	TIM7
56	DMA2_Stream0	DMA2_Channel1
57	DMA2_Stream1	DMA2_Channel2
58	DMA2_Stream2	DMA2_Channel3
59	DMA2_Stream3	DMA2_Channel4
60	DMA2_Stream4	DMA2_Channel5
61	ETH	DFSDM0
62	ETH_WKUP	DFSDM1
63	CAN2_TX	DFSDM2
64	CAN2_RX0	COMP
65	CAN2_RX1	LPTIM1
66	CAN2_SCE	LPTIM2
67	OTG_FS	– OTG_FS (STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices) – USB_FS (STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices)
68	DMA2_Stream5	DMA2_CH6
69	DMA2_Stream6	DMA2_CH7
70	DMA2_Stream7	LPUART1
71	USART6	– QUADSPI – OCTOSPI 1(STM32L4+ Series)
72	I2C3_EV	I2C3_EV
73	I2C3_ER	I2C3_ER

Table 12. Interrupt vector differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series (continued)

Position	STM32F2x5 line	STM32L4 Series / STM32L4+ Series(1)
74	OTG_HS_EP1_OU	SAI1
75	OTG_HS_EP1_IN	SAI2
76	OTG_HS_WKUP	– SWPMI1 – OCTOSPI2 (STM32L4+ Series)
77	OTG_HS	TSC
78	DCMI	– LCD – DSIHOST (STM32L4R9xx/4S9xx)
79	CRYPT	AES
80	HASH_RNG	RNG
81	NA	FPU
82		HASH and CRS
83		I2C4_EV
84		I2C4_ER
85		DCMI
86		CAN2_TX
87		CAN2_RX0
88		CAN2_RX1
89		CAN2_SCE
90		DMA2D
91		LCD-TFT
92		LCD-TFT_ER
93		GFXMMU
94		DMAMUX1_OVR

Color key:

- (blue) = Same feature, but specification change or enhancement
- (grey) = Feature not available (NA)
- (yellow) = Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

1. On the STM32L4 Series / STM32L4+ Series devices on which the peripheral is not implemented, the interrupt is not applicable.

4.5 Reset and clock control (RCC)

The main differences related to the RCC (reset and clock controller), between the STM32L4 Series / STM32L4+ Series and the STM32F2x5 line devices are presented in *Table 13*.

Table 13. RCC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

RCC	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
MSI	NA	– MSI is a low-power oscillator with a programmable frequency up to 48 MHz. – It can replace PLL as system clock (faster wakeup, lower consumption) – It can be used as USB device clock (no need for external high speed crystal oscillator) – Multi speed RC factory and user trimmed (100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz) – Auto calibration from LSE
HSI16	16 MHz RC factory and user trimmed	
LSI	Around 32 kHz	– 32 kHz RC – Lower consumption, higher accuracy (refer to the product datasheet)
HSE	4 to 26 MHz	4 to 48 MHz
LSE	– 32.768 kHz – Configurable drive/consumption (only in STM32L4 Series) – Available in backup domain (VBAT)	
HSI48	NA	– 48 MHz RC (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx) – Can drive USB Full Speed, SDMMC and RNG

Table 13. RCC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

RCC	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
PLL	– Main PLL for system – 1 PLL (PLLI2S) for I2S – PLL sources are HSI, HSE.	– Main PLL for system – 2 PLLs for SAI1/2, ADC, RNG, SDMMC and OTG FS clock (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) – 1 PLL for SAI1, ADC, RNG, SDMMC, USB FS clock (for STM32L45xxx/46xxx and STM32L43xxx/44xxx) – Each PLL can provide up to 3 independent outputs – The PLL multiplication/division factors are different for STM32F2x5 line – PLL clock sources: MSI, HSI16, HSE
System clock source	HSI, HSE or PLL	MSI, HSI16, HSE or PLL
System clock frequency	– Up to 120 MHz – 16 MHz after reset using HSI	– Up to 80 MHz or 120 MHz for STM32L4+ Series – 4 MHz after reset using MSI
AHB frequency	Up to 120 MHz	Up to 80 MHz or 120 MHz for STM32L4+ Series
APB1 frequency	Up to 30 MHz	Up to 80 MHz or 120 MHz for STM32L4+ Series
APB2 frequency	Up to 60 MHz	Up to 80 MHz or 120 MHz for STM32L4+ Series
RTC clock source	LSI, LSE or HSE (1 MHz. Division factor set in RTCPRE field)	LSI, LSE or HSE/32
MCO clock source	– MCO1 pin (PA8): HSI, LSE, HSE, PLLCLK – MCO2 pin (PC9): HSE, PLLCLK, SYSCLK, PLLI2S With configurable prescaler from 1, 2, 3, 4 or 5 for each output	– MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI or HSI48 (for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx) With configurable prescaler from 1, 2, 4, 8 or 16 for each output
CSS	– CSS (Clock Security System) – CSS on HSE	– CSS (Clock Security System) – CSS on LSE

Table 13. RCC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

RCC	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Internal oscillator measurement / calibration	– LSE connected to TIM5 CH4 IC: can measure HSI with respect to LSE clock high precision – LSI connected to TIM5 CH4 IC: can measure LSI with respect to HSI clock precision – HSE_RTC connected to TIM11 CH1 IC: can measure HSE with respect to HSI clock	– LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision – LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision – HSE/32 connected to TIM17 CH1 IC: can measure HSE with respect to LSE/HSI16 clock – MSI connected to TIM17 CH1 IC: can measure MSI with respect to HSI16/HSE clock – On STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx, HSE/32 and MSI are connected to TIM16 CH1 IC
Interrupt	– CSS (linked to NMI IRQ) – PLLI2SRDY, PLLRDY, HSERDY, HSIRDY, LSERDY, LSIRDY (linked to RCC global IRQ)	– CSS (linked to NMI IRQ) – LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, PLLSAI1RDY, PLLSAI2RDY (only on STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) (linked to RCC global IRQ)

Color key:

= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F2x5 line and STM32L4 Series highlight

In addition to the differences described in *Table 13*, the following subsections present some additional adaptation steps that may be needed for the migration.

4.5.1 Performance versus V_{CORE} ranges

In STM32L4 Series / STM32L4+ Series the maximum CPU clock frequency and number of Flash memory wait state depend on the selected voltage range V_{CORE}.

Table 14. STM32L4 Series / STM32L4+ Series performance versus V_{CORE} ranges(1)

CPU performance	Power performance	V_{CORE} performance	Typical value (V)	Max frequency (MHz)					
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS
STM32L4 Series									
High	Medium	1	1.2	-	80	64	48	32	16
Medium	High	2	1.0	-	26	26	18	12	6
STM32L4+ Series									
High	Medium	1 boost mode	1.28	120	100	80	60	40	20
		1 normal mode	1.2	-	-	80	60	40	20
Medium	High	2	1.0	-	-	-	26	16	8

1. WS = wait state.

In the STM32F2x5 line devices the maximum CPU clock frequency and the number of Flash memory wait state depend on the selected voltage range V_{DD}.

Table 15. Number of wait states according to CPU clock (HCLK) frequency

Wait states (WS) (LATENCY)	HCLK (MHz) for STM32F2x5 line			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.8 V(1) - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK ≤ 30	0 < HCLK ≤ 24	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	30 < HCLK ≤ 60	24 < HCLK ≤ 48	18 < HCLK ≤ 36	16 < HCLK ≤ 32
2 WS (3 CPU cycles)	60 < HCLK ≤ 90	48 < HCLK ≤ 72	36 < HCLK ≤ 54	32 < HCLK ≤ 48
3 WS (4 CPU cycles)	90 < HCLK ≤ 120	72 < HCLK ≤ 96	54 < HCLK ≤ 72	48 < HCLK ≤ 64
4 WS (5 CPU cycles)	-	96 < HCLK ≤ 120	72 < HCLK ≤ 90	64 < HCLK ≤ 80
5 WS (6 CPU cycles)	-	-	90 < HCLK ≤ 108	80 < HCLK ≤ 96
6 WS (7 CPU cycles)	-	-	108 < HCLK ≤ 120	96 < HCLK ≤ 112
7 WS (8 CPU cycles)	-	-	-	112 < HCLK ≤ 120

1. If IRROFF is set to VDD on STM32F205xx devices, this value can be lowered to 1.65 V when the device operates in a reduced temperature range.

4.5.2 Peripheral access configuration

Since the address mapping of some peripherals has been changed in the STM32L4 Series / STM32L4+ Series compared to the STM32F2x5 line devices, different registers need to be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from Reset mode].

Table 16. RCC registers used for peripheral access configuration

Bus	Register STM32F2x5 line	Register STM32L4 Series / STM32L4+ Series	Comments
AHB	RCC_AHBRSTR	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2) RCC_AHB3RSTR (AHB3)	Used to [enter/exit] the AHB peripheral from reset
	RCC_AHBENR	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2) RCC_AHB3ENR (AHB3)	Used to [enable/disable] the AHB peripheral clock
	RCC_AHBLPENR	RCC_AHB1SMENR (AHB1) RCC_AHB2SMENR (AHB2) RCC_AHB3SMENR (AHB3)	Used to [enable/disable] the AHB peripheral clock in Sleep mode
APB1	RCC_APB1RSTR	RCC_APB1RSTR1 RCC_APB1RSTR2	Used to [enter/exit] the APB1 peripheral from reset
	RCC_APB1ENR	RCC_APB1ENR1 RCC_APB1ENR2	Used to [enable/disable] the APB1 peripheral clock
	RCC_APB1LPENR	RCC_APB1SMENR1 RCC_APB1SMENR2	Used to [enable/disable] the APB1 peripheral clock in Sleep mode
APB2	RCC_APB2RSTR		Used to [enter/exit] the APB2 peripheral from reset
	RCC_APB2ENR		Used to [enable/disable] the APB2 peripheral clock
	RCC_APB2LPENR	RCC_APB2SMENR	Used to [enable/disable] the APB2 peripheral clock in Sleep mode

4.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source, which is independent from the system clock that is used to generate the clock required for their operation.

- **USB**:
  - In STM32F2x5 line:
    The USB OTG FS 48 MHz clock is derived from the PLL48CLK output.
    The USB 48 MHz clock is derived from the PLL48CLK output.
  - In STM32L4 Series / STM32L4+ Series:
    The USB 48 MHz clock is derived from one of the following sources:
    Main PLL VCO (PLLUSB1CLK)
    PLLSAI1 VCO (PLLUSB2CLK)
    MSI clock: when the MSI clock is auto-trimmed with the LSE, it can be used by the

USB OTG FS device, or HSI48 internal oscillator (only on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx).

- **SDIO/SDMMC:**
  - In STM32L4 Series / STM32L4+ Series: the SDMMC clock is derived from one of the following sources:
    Main PLL VCO (PLLUSB1CLK)
    PLLSAI1 VCO (PLLUSB2CLK)
    MSI clock or HSI48 internal oscillator (only on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx).
- **RTC:**
  - In STM32F2x5 line the RTC clock is derived from one of the three following sources: LSE, LSI or HSE.
  - In STM32L4 Series / STM32L4+ Series the RTC (and LCD Glass clock) is derived from one of the three following sources: LSE clock, LSI clock or HSE clock divided by 32 (PCLK frequency must always be greater than or equal to RTC Clock frequency).
- **ADC:**
  - In STM32F2x5 line, the ADC clock is the ADCCLK (APB2) clock divided by a programmable factor (2, 4, 6, 8).
  - In STM32L4 Series / STM32L4+ Series, the input clock of the ADCs (master and slave) can be selected between different clock sources (two for STM32L43xxx/44xxx and STM32L45xxx/46xxx; three for STM32L47xxx/48xxx):
    The ADC clock can be derived (selected by software) from one of the following sources: system clock (SYSCLK), PLLSAI1 VCO[a] (PLLADC1CLK) or PLLSAI2 VCO (PLLADC2CLK)[b]. In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to bits PREC[3:0]).
    The ADC clock can be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). In this mode, a programmable divider factor can be selected (1, 2 or 4 according to bits CKMODE[1:0]) (refer to the STM32L4 Series and STM32L4+ Series reference manuals for more details).

a. Not available on STM32L41xxx/42xxx, only SYSCLK could be used on those devices.

b. PLLSAI2VCO (PLLADC2CLK) is a clock source only on STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices.

- **DAC:**

  In STM32L4 Series and STM32L4+ Series, in addition to the PCLK1 clock, the LSI clock is used for the sampling and hold operation.
- **U(S)ARTs:**
  - In STM32F2x5 line, the U(S)ART clock is APB1 or APB2 clock (depending on which APB bus is mapped the U(S)ART).
  - In STM32L4 Series and STM32L4+ Series, the U(S)ART clock is derived from one of the four following sources: system clock (SYSCLK), HSI16, LSE, APB1 or APB2 clock (depending on which APB bus the U(S)ART is mapped).
    Using a source clock independent from the system clock (example: HSI16) allows to change the system clock on the fly without a need to reconfigure U(S)ART peripheral baud rate prescalers.
- **I2Cs:**
  - In STM32F2x5 line, the I2C clock is APB1 clock (PCLK1).
  - In STM32L4 Series and STM32L4+ Series, the I2C clock is derived from one of the three following sources: system clock (SYSCLK), HSI16 or APB1 (PCLK1).
    Using a source clock independent from the system clock (example: HSI16) allows to change the system clock on the fly without a need to reconfigure I2C peripheral timing register.
- **I2S/SAI:**
  - In STM32F2x5 line, the I2S clocks are derived from one of the three following sources: HSI clock, HSE clock or PLL clock.
  - In STM32L4 Series and STM32L4+ Series, the I2S peripherals are not available and replaced by SAIs.

  The SAI clocks are derived from one of the four following sources:
  - For STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices: an external clock mapped on SAI1_EXTCLK or SAI2_EXTCLK, PLLSAI1 VCO (PLLSAI1CLK), PLLSAI2 VCO (PLLSAI2CLK) or main PLL VCO (PLLSAI3CLK).
  - For STM32L45xxx/46xxx and STM32L43xxx/44xxx devices: an external clock mapped on SAI1_EXTCLK for SAI1, PLLSAI1 (P) divider output (PLLSAI1CLK), main PLL (P) divider output (PLLSAI2CLK) or HSI16 clock.

4.6 Power control (PWR)

In STM32L4 Series / STM32L4+ Series the PWR controller presents some differences compared to STM32F2x5 line, these differences are summarized in *Table 17*.

Table 17. PWR differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

PWR	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Power supplies	– V_{DD} = 1.8 to 3.6 V: external power supply for I/Os, Flash memory and internal regulator. It is provided externally through VDD pins – On STM32F205xx, LCSP64+2 package, if IRROFF is set to VDD, the supply voltage can drop to 1.7 V when the device operates in the 0 to 70°C temperature range using an external power supply supervisor	V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, Flash memory and internal regulator. It is provided externally through VDD pins.
	– V_{CORE} = 1.2 V. – V_{CORE} is the power supply for digital peripherals. It is generated by an internal voltage regulator The voltage regulator requires one or two external capacitors connected to dedicated pins VCAP_1, VCAP_2 – In application Standby mode, the voltage regulator output voltage is powered down to save power consumption	– V_{CORE} = 1.0 to 1.2 V – V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator – Two V_{CORE} ranges can be selected by software depending on target frequency
	V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock, 32 kHz oscillator and backup registers (through power switch) when VDD is not present	V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present
	V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively	– Independent power supplies (V_{DDA}, V_{DDUSB}, V_{DDIO2}) allow to improve power consumption by running MCU at lower supply voltage than analog and USB. – Note that V_{DDIO2} is only present on STM32L47xxx/48xxx devices
	V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL	– V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DAC/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V – V_{DDA} is the external analog power supply for A/D and D/A converters, voltage reference buffer, operational amplifiers and comparators – The V_{DDA} voltage level is independent from the V_{DD} voltage

Table 17. PWR differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Power supplies (continuation)	NA	– V_{LCD} = 2.5 to 3.6 V – The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter
	– N/A – USB OTG FS/HS powered by V_{DD}. V_{DD} must be > 3.0 V (or degraded electrical characteristic between 2.7 V to 3V)	– V_{DDUSB} = 3.0 to 3.6 V – V_{DDUSB} is the external independent power supply for USB transceivers – The V_{DDUSB} voltage level is independent from the V_{DD} voltage
	– N/A No V_{DDIO2} supply in STM32F2x5 line	– V_{DDIO2} = 1.08 V to 3.6 V – V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]) – The V_{DDIO2} voltage level is independent from the V_{DD} voltage. Not applicable for STM32L45xxx/46xxx, STM32L43xxx/44xxx nor STM32L41xxx/42xxx.
	-	– Available only on SM32L4R9xx/4S9xx – V_{DDDSI} is independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY. This supply must be connected to the global VDD
	-	– Available only on SM32L4R9xx/4S9xx – V_{CAPDSI} is the output of the DSI regulator (1.2V) which must be connected externally to $V_{DD12DSI}$
	-	– Available only on SM32L4R9xx/4S9xx – $V_{DD12DSI}$ is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. An external capacitor of 2.2 µF must be connected on the $V_{DD12DSI}$ pin
Battery backup domain	– RTC with backup registers (80 bytes) – LSE – PC13 to PC15 I/Os, plus PI8 I/O (when available)	– RTC with backup registers (128 bytes) – LSE – PC13 to PC15 I/Os

Table 17. PWR differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Power supply supervisor	– Integrated POR / PDR circuitry – Programmable voltage detector	– Integrated POR / PDR circuitry – Programmable voltage detector (PVD)
	– Brownout reset (BOR) – BOR can be disabled after power-on	– Brownout reset (BOR) – BOR is always enabled, except in Shutdown mode
	NA	Four peripheral voltage monitoring (PVM) – PVM1 for V_{DDUSB} – PVM2 for V_{DDIO2} – PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V)
Low-power modes	Sleep mode	Sleep mode
	NA	Low-power run mode – System clock is limited to 2 MHz – I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz – The consumption is reduced at lower frequency thanks to LP regulator usage
		Low-power Sleep mode – System clock is limited to 2 MHz – I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz – The consumption is reduced at lower frequency thanks to LP regulator usage
	Stop mode (all clocks are stopped)	Stop 0, Stop1 and Stop2 mode Some additional functional peripherals (cf wakeup source)
	Standby mode (V_{CORE} domain powered off)	Standby mode (V_{CORE} domain powered off) – Optional SRAM2 retention – Optional I/O pull-up or pull-down configuration
	NA	Shutdown mode (V_{CORE} domain powered off and power monitoring off)
External SMPS	NA	Support for external SMPS for high-power efficiency. Refer to AN4978.

Table 17. PWR differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Wake-up sources	Sleep mode – Any peripheral interrupt/wakeup event	Sleep mode – Any peripheral interrupt/wakeup event
	Stop mode – Any EXTI line event/interrupt – PVD, RTC, USB OTG FS/HS, Ethernet	Stop 0, Stop 1 and Stop 2 mode – Any EXTI line event/interrupt – BOR, PVD, PVM, COMP, RTC, USB, IWDG, – U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
	Standby mode – NRST external reset – IWDG reset – WKUP pin (PA0) rising edge – RTC event	Standby mode – 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin – IWDG reset
	NA	Shutdown mode – 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin
Wake-up clocks	Wake-up from Stop – HSI RC clock	Wake-up from Stop – HSI16 16 MHz or MSI (all ranges up to 48 MHz) allowing 5 µs wakeup at high speed without waiting for PLL startup time
	Wake-up from Standby – HSI RC clock	Wake-up from Standby – MSI (ranges from 1 to 8 MHz)
	NA	Wake-up from Shutdown – MSI 4 MHz

Table 17. PWR differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Configuration	-	In STM32L4 Series / STM32L4+ Series the registers are different: From 2 registers in STM32F2x5 line to 23 registers in STM32L4 Series / STM32L4+ Series – 4 control registers – 2 status registers – 1 status clear register – 2 registers per GPIO port (A,B,..H) for controlling pull-up and pull-down (16registers) Most configuration bits from STM32F2x5 line can be found in STM32L4 Series / STM32L4+ Series (but sometime may have different programming mode)

Color key:

= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

4.7 Real-time clock (RTC)

STM32L4 Series / STM32L4+ Series and STM32F2x5 line implement almost the same features on the RTC.

Table 18 shows the differences.

Table 18. RTC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

RTC	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Features	Coarse digital calibration. Kept for compatibility only, new developments must only use a smooth calibration.	Only smooth calibration available
	1 tamper pin (available in VBAT)	3 tamper pins (available in VBAT)
	80 bytes backup registers	128 byte backup registers

Table 18. RTC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

RTC	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Configuration	-	Coarse digital calibration not available in STM32L4 Series / STM32L4+ Series: – RTC_CR/DCE not available – RTC_CALIBR register not available – RTC_TAFCR --> RTC_TAMPCR except a few bits
Color key: (blue) = Same feature, but specification change or enhancement (grey) = Feature not available (NA)		

For more information about the STM32L4 Series RTC features, refer to the RTC section of the STM32L4 Series and STM32L4+ Series reference manuals.

4.8 System configuration controller (SYSCFG)

The STM32L4 Series / STM32L4+ Series SYSCFG implements additional features compared to the STM32F2x5 line.

Table 19 shows the differences.

Table 19. SYSCFG differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

SYSCFG	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Features	– Remapping memory areas – Managing the external interrupt line connection to the GPIOs – IO compensation	– Remapping memory areas – Managing the external interrupt line connection to the GPIOs – Managing robustness feature – Setting SRAM2 write protection and software erase – Configuring FPU interrupts – Enabling the firewall – Enabling /disabling I2C Fast-mode Plus driving capability on some I/Os and voltage booster for I/Os analog switches
Configuration	-	– Most registers from STM32F2x5 line are identical in STM32L4 Series / STM32L4+ Series – A few bits are different and EXTI configuration may differ (number of GPIO is different depending on product)
Color key: (blue) = Same feature, but specification change or enhancement		

4.9 General-purpose I/O interface (GPIO)

The STM32L4 Series / STM32L4+ Series GPIO peripheral embeds identical features compared to the STM32F2x5 line GPIO.

The GPIO code written for the STM32F2x5 line devices may require minor adaptations for the STM32L4 Series and STM32L4+ Series devices. This is due to the mapping of particular functions on different GPIOs (refer to *Section 2* for the pinout differences, and to the product datasheet for detailed alternate function mapping differences).

The main GPIO features are:

- GPIO mapped on AHB bus for better performance
- I/O pin multiplexer and mapping: pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) connected to an I/O pin at a time. In this way, there cannot be any conflict between peripherals sharing the same I/O pin.

At reset, the STM32F2x5 line GPIOs are configured in Input-floating mode while the STM32L4 Series / STM32L4+ Series GPIOs are configured in Analog mode (to avoid consumption through the IO schmitt trigger).

For more information about STM32L4 Series and STM32L4+ Series GPIO programming and usage, refer to the "I/O pin multiplexer and mapping" subsection in the GPIO section of the STM32L4 Series and STM32L4+ Series reference manuals and to the product datasheet for a detailed description of the pinout and alternate function mapping.

4.10 Extended interrupts and events controller (EXTI) source selection

The external interrupt/event controller (EXTI) is very similar on STM32F2x5 line and STM32L4 Series / STM32L4+ Series. *Table 20* shows the main differences.

Table 20. EXTI differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series

EXTI	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Nb of event/interrupt lines	Up to 23 configurable lines	– Up to 41 lines – 12 direct, 26 configurable on STM32L4+ Series – 15 direct, 26 configurable on STM32L49xxx/4Axxx – 14 direct, 26 configurable on STM32L47xxx/48xxx – 12 direct, 25 configurable on STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx
Configuration	-	Registers are slightly different to cope with different number of interrupts
Color key: = Same feature, but specification change or enhancement		

4.11 Flash memory

Table 21 presents the difference between the Flash memory interface of STM32F2x5 line and STM32L4 Series / STM32L4+ Series devices.

The STM32L4 Series / STM32L4+ Series devices instantiates a different Flash module both in terms of architecture/technology and interface, consequently the STM32L4 Series and STM32L4+ Series Flash programming procedures and the registers are different from the STM32F2x5 line ones. Any code written for the Flash interface in the STM32F2x5 line needs to be rewritten to run in the STM32L4 Series / STM32L4+ Series.

The STM32F205xx devices embed a 128-bit wide Flash memory of 128 Kbytes, 256 Kbytes, 512 Kbytes, 768 Kbytes or 1 Mbyte, available for storing programs and data.

The devices also feature 512 bytes of OTP memory that can be used to store critical user data such as Ethernet MAC addresses or cryptographic keys.

For more information on the programming, the erasing and protection of the STM32L4 Series / STM32L4+ Series Flash memory, refer to the STM32L4 Series reference manuals

Table 21. FLASH differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

FLASH	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Main/ program memory	0x0800 0000 to (up to) 0x080F FFFF	– 0x0800 0000 to up to 0x080F FFFF – 0x0800 0000 to up to 0x081F FFFF (only for STM32L4+ Series)
	– Up to 1 Mbyte – 1 bank – 4 sectors of 16 Kbytes – 1 sector of 64 Kbytes – 0 sector of 128 Kbytes – Programming granularity: 8, 16, 32, 64-bit – Read granularity: 128-bit	– For STM32L4+ Series: Up to 2 Mbytes Split in 2 banks When dual bank is enabled each bank: 256 pages of 4 Kbytes and each page: 8 rows of 512 bytes When dual bank is disabled memory block contains 256 pages of 8 Kbytes and each page contains 8 rows of 1024 bytes – For STM32L49xxx/4Axxx and STM32L47xxx/48xxx: Up to 1 Mbyte Split in 2 banks Each bank: 256 pages of 2 Kbytes Each page: 8 rows of 256 bytes – For STM32L45xxx/46xxx: 512 Kbytes 1 bank 256 pages of 2 Kbytes Each page: 8 rows of 256 bytes – For STM32L43xxx/44xxx: Up to 256 Kbytes 1 bank 128 pages of 2 Kbytes Each page: 8 rows of 256 bytes – For STM32L41xxx/42xxx: Up to 128 Kbytes 1 bank 64 pages of 2 Kbytes Each page: 8 rows of 256 bytes Programming and read granularity: 72 bits (including 8 ECC bits)

Table 21. FLASH differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

FLASH	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Features	NA	– Read while write (RWW) – Dual bank boot (only for STM32L49xxx/4Axxx and STM32L47xxx/48xxx)
	NA	– ECC – Flash empty check (for STM32L4+ Series, STM32L49xxx/4Axxx STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
Wait state	Up to 7 (depending on the supply voltage and frequency)	Up to 5(depending on the core voltage and frequency)
ART Accelerator™	Allowing 0 wait state when executing from the cache	Allowing 0 wait state when executing from the cache
One time programmable (OTP)	512 OTP bytes	1 Kbyte OTP bytes (bank1)
Erase granularity	Sector and mass erase	Page erase (2 Kbytes), bank erase and mass erase (both banks)
Read protection (RDP)	Level 0 no protection RDP = 0xAA	Level 0 no protection RDP = 0xAA
	Level 1 memory protection RDP ≠ {0xAA, 0xCC}	Level 1 memory protection RDP ≠ {0xAA, 0xCC}
	Level 2 RDP = 0xCC(1)	Level 2 RDP = 0xCC(1)
Proprietary code readout protection (PCROP)	NA	– 1 PCROP area per bank – Granularity: 64-bit – PCROP_RDP option: PCROP area preserved when RDP level decreased – For STM32L4+ Series: Dual bank: 1 PCROP area per bank Single bank: 2 PCROP area
Write protection (WRP)	– Granularity: 1 sector – Sectors 0 up to 11 can be write protected	– 2 write protection area per bank – Granularity: 2 Kbytes – For STM32L4+ Series: Dual bank: 2 areas per bank Single bank: 4 areas

Table 21. FLASH differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

FLASH	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
User option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	NA	nRST_SHDW
	WDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
		WWDG_SW
	BOR_LEV[1:0]	BOR_LEV[2:0]
	NA	BFB2 (except for STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
		nBOOT1
		SRAM2_RST, SRAM2_PE
		DUAL BANK (except for STM32L4+ Series, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
User option bytes	NA	nBOOT0 (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
		nSWBOOT0 (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
		DBANK (only for STM32L4+ Series)
		DB1M (only for STM32L4+ Series)

Color key:

= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

1. Memory read protection level 2 is an irreversible operation. When level 2 is activated, the level of protection cannot be decreased to level 0 or level 1.

4.12 Universal synchronous asynchronous receiver transmitter (U(S)ART)

The STM32L4 Series and STM32L4+ Series devices implement several new features on the U(S)ART compared to the STM32F2x5 line devices.

Table 22 shows the differences.

Table 22. U(S)ART differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

U(S)ART	STM32F2x5 line	STM32L4 Series STM32L4+ Series
Instances	– 4 x USART – 2 x UART	– 3 x USART – 2 x UART for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx – 1 x UART for STM32L45xxx/46xxx devices – 1 x LPUART
Baud rate	– Up to 2 x 7.5 Mbit/s (USART 1/6) – Up to 4x 3.75 Mbit/s (other)	Up to 10 Mbit/s when the clock frequency is 80 MHz and oversampling is by 8
Clock	Single clock domain	Dual clock domain allowing: – UART functionality and wakeup from Stop mode – Convenient baud rate programming independent from the PCLK reprogramming
Data	Word length: programmable (8 or 9 bits)	– Word length: programmable (7, 8 or 9 bits) – Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	– 14 interrupt sources with flags – 23 interrupt sources with flags for STM32L4+ Series
Features	– Hardware flow control (CTS/RTS) – Continuous communication using DMA – Multiprocessor communication – Single-wire half-duplex communication – IrDA SIR ENDEC block – LIN mode – SPI master	
	– Smartcard mode T = 0 and T = 1 has to be implemented by software – Number of stop bits: 0.5, 1, 1.5, 2	– Smartcard mode T = 0 and T = 1 supported (features are added to support T = 1 such as receiver timeout, block length, end of block detection, binary data inversion, among others) – Number of stop bits: 1, 1.5, 2

Table 22. U(S)ART differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

U(S)ART	STM32F2x5 line	STM32L4 Series STM32L4+ Series
Features (continued)	NA	– Wakeup from Stop mode (Start bit, received byte, address match) – Support for ModBus communication Timeout feature CR/LF character recognition – Receiver timeout interrupt – Auto baud rate detection – Driver Enable – Swappable Tx/Rx pin configuration – Two internal FIFOs for transmit and receive data for STM32L4+ Series – SPI slave for STM32L4+ Series LPUART does not support synchronous mode (SPI Master), smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt, auto baud rate detection.
		– STM32F2x5 line registers and associated bits are not identical in STM32L4 Series / STM32L4+ Series – Refer to STM32L4 Series and STM32L4+ Series reference manuals for details

Color key:

= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series highlight

4.13 Inter-integrated circuit (I2C) interface

The STM32L4 Series and STM32L4+ Series devices implement a different I2C peripheral allowing easy software management.

Table 23 shows the differences.

Table 23. I2C differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

I2C	STM32F2x5 line	STM32L4 Series STM32L4+ Series
Instances	x3	– x3 on STM32L47xxx/48xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx – x4 on STM32L49xxx/4Axxx and STM32L45xxx/46xxx
Features	– 7-bit and 10-bit Addressing mode – SMBus – Standard mode (Sm, up to 100 kHz) – Fast mode (Fm, up to 400 kHz)	
	NA	– Fast mode Plus (Fm+, up to 1 MHz) – Independent clock – Wakeup from STOP on address match
Configuration	-	– Register configuration is very different in STM32F2x5 line and STM32L4 Series / STM32L4+ Series devices – Refer to STM32L4 Series and STM32L4+ Series reference manuals for details

Color key:

= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

= Feature not available (NA)

= Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

4.14 Serial peripheral interface (SPI) / IC to IC sound (I2S) /serial audio interface (SAI)

The STM32L4 Series / STM32L4+ Series and STM32F2x5 line devices implement almost the same features on SPI (apart from I2S).

Table 24 shows the differences.

Table 24. SPI differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

SPI	STM32F2x5 line	STM32L4 Series STM32L4+ Series
Instances	x3	– x3 – x2 for STM32L41xxx/42xxx
Features	3 x SPI 2 x I2S	– I2S feature is not supported by SPI in STM32L4 Series / STM32L4+ Series – SAI interfaces are available instead: x2 for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx x1 for STM32L45xxx/46xxx and STM32L43xxx/44xxx
Data size	Fixed, configurable to 8 or 16 bits	Programmable from 4 to 16-bit
Data buffer	Tx & Rx 16-bit buffers (single data frame)	32-bit Tx & Rx FIFOs (up to 4 data frames)
Data packing	No (16-bit access only)	Yes (8-bit, 16-bit or 32-bit data access, programmable FIFOs data thresholds)
Mode	– SPI TI mode – SPI Motorola mode	– SPI TI – SPI Motorola mode – NSSP mode
Speed	Up to 30 Mbit/s.	Up to 40 Mbits/s (APB at 80 MHz)
Configuration	-	The data size and Tx/Rx flow handling are different in STM32F2x5 line and STM32L4 Series / STM32L4+ Series hence requiring a different software sequence

Color key:

= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

= Same feature, but specification change or enhancement

= Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

Migrating from I2S to SAI:

The STM32L4 Series and STM32L4+ Series devices do not include the I2S interface part of the SPI peripheral, instead it includes a serial audio interface (SAI).

Table 25 shows the main differences between I2S and SAI, considering here only the full duplex I2S instances.

Table 25. Migrating from I2S to SAI

I2S/SAI	STM32F2x5 line (I2S)	STM32L4 Series STM32L4+ Series (SAI)
Instances Full duplex I2S	x2	– x2 SAI1, SAI2 for STM32L49xxx/4Axxx and STM32L47xxx/48xxx – x1 SAI1 for STM32L45xxx/46xxx and STM32L43xxx/44xxx
Features	Full-duplex communication	Two independent audio sub-blocks (per SAI) which can be transmitters or
	Master or slave operations	– Synchronous or Asynchronous mode between the audio sub-blocks – Possible synchronization between multiple SAIs – Master or slave configuration independent for both audio sub-blocks
	8-bit programmable linear prescaler to reach accurate audio sample frequencies (from 8 kHz to 192 kHz)	Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in Master mode
	– Data format may be 16-bit, 24-bit or 32-bit – Data direction is always MSB first.	– Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit – First active bit position in the slot is configurable – LSB first or MSB first for data transfer
	Channel length is fixed to 16-bit (16-bit data size) or 32-bit (16-bit, 24-bit, 32-bit data size) by audio channel	– Up to 16 slots available with configurable size – Number of bits by frame can be configurable – Frame synchronization active level configurable (offset, bit length, level) – Stereo/Mono audio frame capability
	Programmable clock polarity (steady state).	Communication clock strobing edge configurable (SCK)
	16-bit register for transmission and reception with one data register for both channel sides	8-word integrated FIFOs for each audio sub-block (facilitating Interrupt mode)

Table 25. Migrating from I2S to SAI (continued)

I2S/SAI	STM32F2x5 line (I2S)	STM32L4 Series STM32L4+ Series (SAI)
Features (continued)	Supported I2S protocols: – I2S Philips standard – MSB-justified standard (left-justified) – LSB-justified standard (right-justified) – PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)	Audio protocols: – I2S, LSB or MSB-justified, PCM/DSP, TDM (up to 16 channels), AC'97 – SPDIF output – Mute mode – PDM interface (for STM32L4+ Series)
	DMA capability for transmission and reception (16-bit wide)	2-channel DMA per SAI
	– Master clock may be output to drive an external audio component. – Ratio is fixed at 256 × F_S (where F_S is the audio sampling frequency)	
	Interruption sources when enabled: – Errors, – Tx Buffer Empty, Rx Buffer not Empty.	Interruption sources when enabled: – Errors, – FIFO requests.
	Error flags with associated interrupts if enabled respectively. – Overrun and underrun detection – Anticipated frame synchronization signal detection in Slave mode – Late frame synchronization signal detection in Slave mode	Same characteristics than STM32F2x5 line + protection against misalignment in case of underrun and overrun
Configuration	-	There is no compatibility between STM32F205/216 I2S and STM32L4 Series / STM32L4+ Series SAI. The user has to configure the SAI interface for the target protocol. Refer to the STM32L4 Series and STM32L4+ Series reference manuals for details.

Color key:

(green) = New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

(blue) = Same feature, but specification change or enhancement

(yellow) = Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

The SAI peripheral improves the robustness of communication in Slave mode compared to the I2S peripheral (in case of data clock glitch for example).

In Master mode, while migrating an application from STM32F2x5 line to STM32L4 Series and STM32L4+ Series, the user must review the possible master clock (MCLK), data bit clock (SCK) and frame synchronization (FS) frequency reachable. The user must use the STM32L4 Series / STM32L4+ Series PLL multiplication factors and the SAI internal clock divider for a given external oscillator (which can be different than with the STM32F2x5 line I2S).

In STM32L4 Series / STM32L4+ Series, the SAI1 and SAI2 input clocks are derived (selected by software) from one of the following sources:

- For STM32L49xxx/4Axxx and STM32L47xxx/48xxx:
  - An external clock mapped on SAI1_EXTCLK for SAI1 and SAI2_EXTCLK for SAI2.
  - PLLSAI1 (P) divider output (PLLSAI1CLK)
  - PLLSAI2 (P) divider output (PLLSAI2CLK)
  - Main PLL (P) divider output (PLLSAI3CLK)
- For STM32L45xxx/46xxx and STM32L43xxx/44xxx devices:
  - An external clock mapped on SAI1_EXTCLK for SAI1
  - PLLSAI1 (P) divider output (PLLSAI1CLK)
  - Main PLL (P) divider output (PLLSAI2CLK)
  - HSI16 clock

When the clock is derived from one of the internal PLLs, the three PLL inputs are either HSI16, HSE or MSI (between 4 and 48 MHz) divided by a programmable factor PLLM (from 1 to 8 (or from1 to 16 for STM32L4+ Series)).

This input is then multiplied by PLLN (from 8 to 86 (or from 8 to 127 for STM32L4+ Series)) to reach PLL VCO frequency (must be between 64 and 344 MHz). It is finally divided by PLLP (7 or 17 on STM32L47xxx/48xxx, or [2 to 31] on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx) to provide the input clock of the SAI (max 80 MHz (or 120 MHz for STM32L4+ Series)).

For STM32L4+ Series, when the clock is derived from one of the internal PLLs, the three PLL inputs are either HSI16, HSE or MSI divided by its own programmable factor (PLLM, PLLSAI1M and PLLSAI2M) (from 1 to 16).

When the master clock MCLK is used by the external slave audio peripheral, the PLL output is divided by the SAI internal master clock divider factor (1, 2, 4, 6, 8, ..., 30) to provide the master clock (MCLK). The data bit clock is then derived from MCLK with the following formula:

$$SCK = MCLK \times (FRL + 1) / 256 = (MCLK) / (256 / (FRL + 1))$$

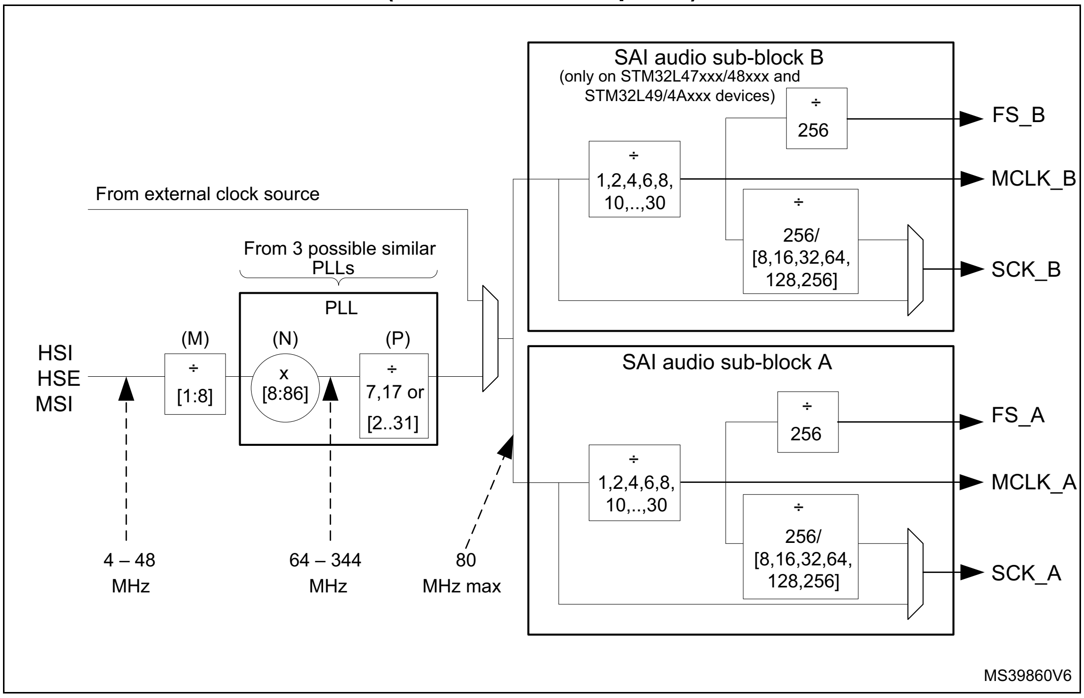
Where:

- FRL is the number of bit clock cycles - 1 in the audio frame (0 to 255)
- (FRL + 1) must be a power of 2 higher or equal to 8
- (FRL + 1) = 8, 16, 32, 64, 128, 256

SCK can also be directly connected to the input clock of the SAI when MCLK output is not needed. The frame synchronization (FS) frequency is always MCLK/256.

Figure 4 shows the clock generation scheme in the STM32L4 Series / STM32L4+ Series. Refer to the STM32L4 Series and STM32L4+ Series reference manuals for more details.

Figure 4. STM32L4 Series / STM32L4+ Series generation of clock for SAI Master mode (when MCLK is required)



4.15 Cyclic redundancy check calculation unit (CRC)

The cyclic redundancy check (CRC) calculation unit is very similar in the STM32F2x5 line and in the STM32L4 Series / STM32L4+ Series devices.

Table 26 shows the differences.

Table 26. CRC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

CRC	STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Features	– Single input/output 32-bit data register – CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size – General-purpose 8-bit register (can be used for temporary storage)	– Single input/output 32-bit data register – CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size – General-purpose 8-bit register (can be used for temporary storage)
	– Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7 – Handles 32-bit data size	– Fully programmable polynomial with programmable size (7, 8, 16, 32-bit) – Handles 8-,16-, 32-bit data size – Programmable CRC initial value – Input buffer to avoid bus stall during calculation – Reversibility option on input and output

Table 26. CRC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

<table>
<tr><th>CRC</th><th>STM32F2x5 line</th><th>STM32L4 Series / STM32L4+ Series</th></tr>
<tr><td>Configuration</td><td>-</td><td>– The configuration registers in STM32F2x5 line and STM34L4 Series are identical.
– STM32L4 Series and STM32L4+ Series devices include additional registers for new features
– Refer to the STM32L4 Series and STM32L4+ Series reference manuals for details</td></tr>
<tr><td colspan="3">Color key:
= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)</td></tr>
</table>

4.16 USB on-the-go full speed (USB OTG FS)

The STM32L4+ Series, and the STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices from STM32L4 Series as well as the STM32F2x5 line implement very similar USB OTG FS peripherals. The key differences are listed in *Table 27*.

Table 27. USB OTG FS differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

<table>
<tr><th>USB OTG FS</th><th>STM32F2x5 line</th><th>STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx</th></tr>
<tr><td rowspan="5">Features</td><td colspan="2">– Universal serial bus revision 2.0
– Full support for the USB on-the-go (USB OTG)</td></tr>
<tr><td><u>FS mode</u>:
– 1 bidirectional control endpoint
– 3 IN endpoints (bulk, interrupt, isochronous)
– 3 OUT endpoints (bulk, interrupt, isochronous)</td><td><u>FS mode</u>:
– 1 bidirectional control endpoint
– 5 IN endpoints (bulk, interrupt, isochronous)
– 5 OUT endpoints (bulk, interrupt, isochronous)</td></tr>
<tr><td colspan="2">USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line</td></tr>
<tr><td rowspan="2">NA</td><td>– Attach detection protocol (ADP)
– Battery charging detection (BCD)</td></tr>
<tr><td>Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB</td></tr>
<tr><td>Mapping</td><td colspan="2">AHB2</td></tr>
</table>

Table 27. USB OTG FS differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

USB OTG FS	STM32F2x5 line	STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx
Buffer memory	– 1.25 Kbyte data FIFOs – Management of up to four Tx FIFOs (one for each IN end point) + one Rx FIFO	– 1.25 Kbyte data FIFOs – Management of up to six Tx FIFOs (one for each IN end point) + one Rx FIFO
Low-power modes	USB suspend and resume	– USB suspend and resume Link power management (LPM) support
Configuration	-	– Registers are different in STM32L4 Series / STM32L4+ Series. – Refer to the STM32L4 Series and STM32L4+ Series reference manuals for details

Color key:

= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

On the STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices, the USB is Full Speed only. The main features are listed in *Table 28*.

On the STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices, a clock recovery system (CRS) block is included so it can provide a precise clock to the USB peripheral.

Table 28. USB FS on STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices

USB FS	STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxxdevices
Features	Universal serial bus revision 2.0, including link power management (LPM) support
	– Configurable number of endpoints from 1 to 8 – Cyclic redundancy check (CRC) generation/checking, non-return-to-zero Inverted (NRZI) encoding/decoding and bit-stuffing – Isochronous transfers support – Double-buffered bulk/isochronous endpoint support – USB Suspend/Resume operations – Frame locked clock pulse generation
	– Attach detection protocol (ADP) – Battery charging detection (BCD) – USB connect / disconnect capability (controllable embedded pull-up resistor on USB_DP line)
	Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB
Mapping	APB1
Buffer memory	1024 bytes of dedicated packet buffer memory SRAM
Low-power modes	– USB suspend and resume – Link power management (LPM) support
Configuration	– In STM32L4 Series / STM32L4+ Series, the registers are different – Refer to the STM32L4 Series and STM32L4+ Series reference manuals for details

Color key:

= New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Difference between STM32F2 line and STM32L4 Series / STM32L4+ Series highlight

4.17 Analog-to-digital converters (ADC)

Table 29 presents the differences between the STM32F2x5 line and the STM32L4 Series / STM32L4+ Series ADC peripherals. These differences are based on new digital interface, new architecture and new features.

Table 29. ADC differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series

<table>
<tr><th>ADC</th><th colspan="2">STM32F2x5 line</th><th colspan="2">STM32L4 Series
STM32L4+ Series</th></tr>
<tr><td>ADC Type</td><td colspan="2">SAR structure</td><td colspan="2">SAR structure</td></tr>
<tr><td>Instances</td><td colspan="2">1 instance</td><td colspan="2">– 3 instances for STM32L49xxx/4Axxx and STM32L47xxx/48xxx
– 2 instances for STM32L41xxx/42xxx
– 1 instance for STM32L4+ Series, STM32L45xxx/46xxx and STM32L43xxx/44xxx</td></tr>
<tr><td>Maximum sampling frequency</td><td colspan="2">2 Msps</td><td colspan="2">– 5.1 Msps (Fast channels)
– 4.8 Msps (Slow channels)</td></tr>
<tr><td>Number of channels</td><td colspan="2">Up to 19 channels</td><td colspan="2">Up to 19 channels per ADC</td></tr>
<tr><td>Resolution</td><td colspan="2">12-bit</td><td colspan="2">12-bit + digital oversampling up to 16-bit</td></tr>
<tr><td>Conversion modes</td><td colspan="2">Single / Continuous / Scan / Discontinuous</td><td colspan="2">– Single / Continuous / Scan / Discontinuous
– Dual mode</td></tr>
<tr><td>DMA</td><td colspan="2">Yes</td><td colspan="2">Yes</td></tr>
<tr><td rowspan="2">External Trigger</td><td colspan="2">Yes</td><td colspan="2">Yes</td></tr>
<tr><td><u>External event for regular group:</u>
TIM1_CH1
TIM1_CH2
TIM1_CH3
TIM2_CH2
TIM2_CH3
TIM2_CH4
TIM2_TRGO
TIM3_CH1
TIM3_TRGO
TIM4_CH4
TIM5_CH1
TIM5_CH2
TIM5_CH3
TIM8_CH1
TIM8_TRGO
EXTI line11</td><td><u>External event for injected group:</u>
TIM1_CH4
TIM1_TRGO
TIM2_CH1
TIM2_TRGO
TIM3_CH2
TIM3_CH4
TIM4_CH1
TIM4_CH2
TIM4_CH3
TIM4_TRGO
TIM5_CH4
TIM5_TRGO
TIM8_CH2
TIM8_CH3
TIM8_CH4
EXTI line15</td><td><u>External event for regular group:</u>
TIM1 CC1
TIM1 CC2
TIM1 CC3
TIM2 CC2
TIM3 TRGO
TIM4 CC4(1)
EXTI line 11
TIM8_TRGO(1)
TIM8_TRGO2(1)
TIM1_TRGO
TIM1_TRGO2
TIM2_TRGO
TIM4_TRGO(1)
TIM6_TRGO
TIM15_TRGO
TIM3_CC4(1)</td><td><u>External event for injected group:</u>
TIM1 TRGO
TIM1 CC4
TIM2 TRGO
TIM2 CC1
TIM3 CC4(1)
TIM4 TRGO(1)
EXTI line15
TIM8_CC4(1)
TIM1_TRGO2
TIM8_TRGO(1)
TIM8_TRGO2(1)
TIM3_CC3(1)
TIM3_TRGO(1)
TIM3_CC1(1)
TIM6_TRGO
TIM15_TRGO</td></tr>
</table>

Table 29. ADC differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series (continued)

ADC	STM32F2x5 line	STM32L4 Series STM32L4+ Series
Supply requirement	– 1.8 V to 3.6 V – (1.7 V with external power-supply supervisor)	– 1.62 V to 3.6 V – Independent power supply (V_{DDA})
Reference voltage	– External – The higher/positive reference voltage for the ADC: 1.8 V ≤ VREF+ ≤ VDDA – Analog power supply equal to VDD and: – 2.4 V ≤ VDDA ≤ VDD (3.6 V) for full speed – 1.8 V ≤ VDDA ≤ VDD (3.6 V) for reduced speed – The lower/negative reference voltage for the ADC: VREF– = VSSA – Recommendation: VDDA - VREF+ < 1.8 V	Reference voltage for STM32L4 Series / STM32L4+ Series external (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)
Electrical Parameters	– 300 µA (Typ) on V_{REF} DC current – 1.6 mA (Typ) on V_{DDA} DC current	The consumption is proportional to the conversion speed: 200 µA/Msps
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	$V_{REF-} \leq V_{IN} \leq V_{REF+}$

Color key:

(green) = New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)

(blue) = Same feature, but specification change or enhancement

1. Except for STM32L43xxx/44xxx.

4.18 Digital-to-analog converter (DAC)

The STM32L4 Series and STM32L4+ Series implement an enhanced DAC compared to the one present in STM32F2x5 line.

Table 30 shows the differences.

Table 30. DAC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

DAC	STM32F2x5 line	STM32L4 Series STM32L4+ Series
Number of channels	2	– x2 on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L47xxx/48xxx and STM32L43xxx/44xxx – x1 on STM32L45xxx/46xxx
Resolution	12 bits	
Features	– Left or right data alignment in 12-bit mode – Noise-wave and triangular-wave generation – DAC with 2 channels for independent or simultaneous conversions	
	NA	– Buffer offset calibration – DAC1_OUTx can be disconnected from output pin – Sample and Hold mode for low-power operation in Stop mode
DMA	Yes	Yes
External trigger	Yes	Yes
	– TIM6 TRGO – TIM8 TRGO – TIM7 TRGO – TIM5 TRGO – TIM2 TRGO – TIM4 TRGO – EXTI line9 – SWTRIG	– TIM6 TRGO – TIM8 TRGO(1) – TIM7 TRGO – TIM5 TRGO(1) – TIM2 TRGO – TIM4 TRGO(1) – EXTI line9 – SW TRIG Additional trigger for STM32L4+ Series: – TIM1_TRGO – TIM15_TRGO – LPTIM1_OUT – LPTMI2_OUT

Table 30. DAC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series (continued)

DAC	STM32F2x5 line	STM32L4 Series STM32L4+ Series
Supply requirement	1.8 V to 3.6 V	– 1.8 V to 3.6 V – Independent power supply (V_{DDA})
Reference Voltage	External 1.8 V ≤ V_{REF+} ≤ V_{DDA}	External (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)
Configuration	-	SW compatible except for output buffer management

Color key:
- (green) = New feature or new architecture (difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series)
- (blue) = Same feature, but specification change or enhancement
- (grey) = Feature not available (NA)
- (yellow) = Difference between STM32F2x5 line and STM32L4 Series / STM32L4+ Series highlight

1. Except on STM32L43xxx/44xxx.

4.19 Controller area network (bxCAN)

The STM32L4 Series and STM32L4+ Series devices implement the same bxCAN (basic extended CAN interface) as the STM32F2x5 line devices.

Table 31 shows the differences.

Table 31. bxCAN differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series

<table>
<tr><th>bxCAN</th><th>STM32F2x5 line</th><th>STM32L4 Series
STM32L4+ Series</th></tr>
<tr><td>Instances</td><td>x2</td><td>– x1 on STM32L4+ Series, STM32L47xxx/48xxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx
– x2 on STM32L49xxx/4Axxx</td></tr>
<tr><td rowspan="2">Feature</td><td colspan="2">– Supports CAN protocol version 2.0 A, B Active
– Bit rates up to 1 Mbit/s
– Supports the time triggered communication option
– Tx: 3 transmit mailboxes, configurable priority, time stamp on SOF transmission
– Rx: 2 receive FIFOs with 3 stages, scalable filter banks, identifier list, configurable FIFO overrun, time stamp on SOF reception
– Time-triggered communication options:
Disable Automatic-retransmission mode
16-bit free running timer
Time Stamp sent in last two data bytes management
Maskable interrupts
Software-efficient mailbox mapping at a unique address space</td></tr>
<tr><td>Dual CAN</td><td>NA</td></tr>
<tr><td>Configuration</td><td>-</td><td>Refer to the STM32L4 reference manuals for details.</td></tr>
<tr><td colspan="3">Color key:
= Same feature, but specification change or enhancement
= Feature not available (NA)</td></tr>
</table>

5 Software migration

5.1 References

- The definitive guide to Arm® Cortex®-M3 and Cortex®-M4 processors
- *STM32F10xxx/20xxx/21xxx/L1xxxx Cortex®-M3* programming manual (PM0056)
- *STM32F3 Series, STM32F4 Series, STM32L4 Series and STM32L4+ Series Cortex®-M4 programming manual (PM0214)*
- Cortex®-M3 Technical Reference Manual, available on http://infocenter.arm.com
- Cortex®-M4 Technical Reference Manual, available from http://infocenter.arm.com

5.2 Cortex®-M3 and Cortex®-M4 overview

5.2.1 STM32 Cortex®-M3 processor and core peripherals

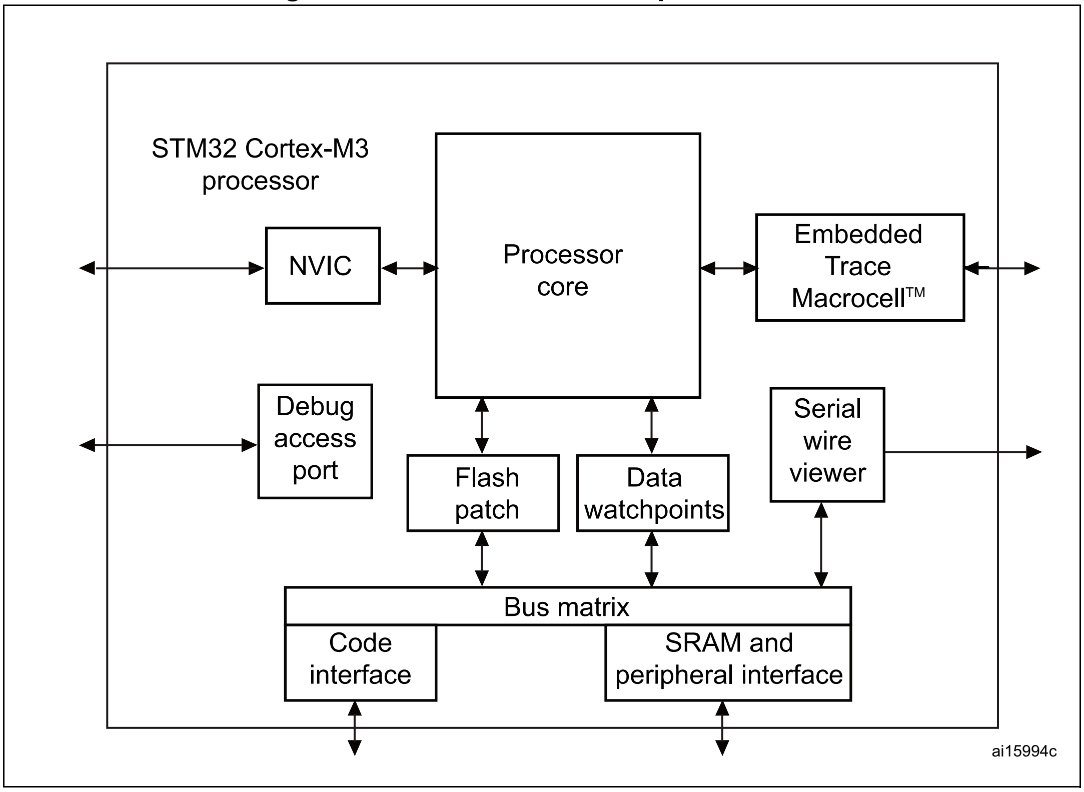
The Cortex®-M3 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers an exceptional power efficiency through an efficient instruction set and extensively optimized design, providing a high-end processing hardware including single-cycle 32x32 multiplications and a dedicated hardware division.

Cortex®-M3 processor features:

- Tight integration of system peripherals reducing the area and development costs
- Thumb instruction set combining a high code density with 32-bit performance
- Code-patch ability for ROM system update
- Power control optimization of system components
- Integrated sleep modes for a low-power consumption
- Fast code execution permitting a slower processor clock or increasing the sleep mode time
- Hardware division and fast multiplier
- Deterministic, high-performance interrupt handling for time-critical applications
- Extensive debug and trace capabilities.

Figure 5 shows the STM32 Cortex®-M3 implementation schema.

Figure 5. STM32 Cortex®-M3 implementation



Cortex®-M3 key features

- Architecture 32 bits RISC ARMv7-M.
- 3-stage pipeline with branch speculation
- Instruction set:
  - Thumb, Thumb-2
  - Hardware multiply, hardware divide, saturated arithmetic

5.2.2 STM32 Cortex®-M4 processor and core peripherals

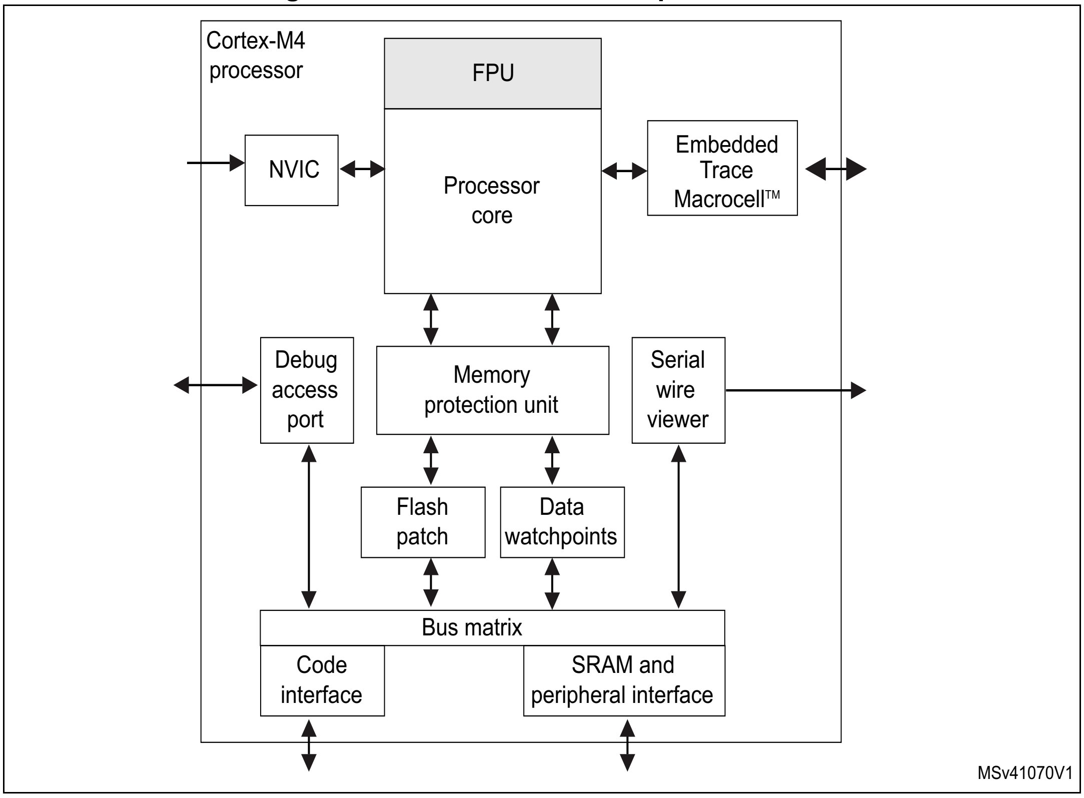
The Cortex®-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to the developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultra-low power consumption with integrated sleep modes
- Platform security robustness, with integrated memory protection unit (MPU).

The Cortex®-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers an exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, a saturating arithmetic and dedicated hardware division.

Figure 6 shows the STM32 Cortex®-M4 implementation schema.

Figure 6. STM32 Cortex®-M4 implementation



Cortex®-M4 key features

- Architecture 32 bits RISC ARMv7E-M.
- 3-stage pipeline with branch speculation
- Instruction set:
  - Thumb, Thumb-2
  - Hardware multiply, Hardware divide, saturated arithmetic
  - DSP extensions:
    - Single cycle 16/32-bit MAC
    - Single cycle dual 16-bit MAC
    - 8/16-bit SIMD arithmetic.
  - FPU (VFPv4-SP)

5.2.3 Software point of view

In addition to the Cortex®-M3, the Cortex®-M4 provides:

- SIMD, or Single Instruction Multiple Data, operations
- Additional fast MAC and multiply instructions
- Saturating arithmetic instructions
- Single precision FPU, or Floating Point Unit, instructions.

This means on software point of view, the Cortex®-M3 software can be run on the Cortex®-M4.

To improve on and speed-up the STM32F2 Series software on the new STM32L4 platforms, the user must not forget to switch on the FPU. This can be done on the makefile side or using below software development tools:

- On Keil® µVision®
  - On “Project” open “Option for Target”
  - Go to “Target”...“Code Generation”
  - Set “Floating Point Hardware” to “Use Single Precision”
- On IAR Systems®
  - On “Project” open “Options...”
  - Go to “General Options”...“Target”
  - Set “Floating point settings”, ‘FPU” to “VFPv4 single precision”

5.3 Cortex mapping overview

Except for the floating point unit, the mapping is similar on the Cortex®-M3 and the Cortex®-M4.

Table 32. Cortex overview mapping

		STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Core	Architecture	Cortex®-M3	Cortex®-M4
	Nested vectored interrupt controller (NVIC)	81 maskable interrupt channels	Maskable interrupt channel: – 94 on STM32L4+ Series – 91 on STM32L49xxx/4Axxx – 82 on STM32L47xxx/48xxx – 67 on STM32L45xxx/46xxx and STM32L43xxx/44xxx
	Extended interrupts and events controller (EXTI)	Up to 23 event/interrupt	– Up to 41 event/interrupt for STM32L49xxx/4Axxx – Up to 40 event/interrupt for STM32L47xxx/48xxx – Up to 37 event/interrupt for STM32L45xxx/46xxx – Up to 37 event/interrupt for STM32L43xxx/44xxx

Table 32. Cortex overview mapping (continued)

		STM32F2x5 line	STM32L4 Series / STM32L4+ Series
Mapping	System timer	0xE000E010 to 0xE000E01F	0xE000E010 to 0xE000E01F
	Nested vectored interrupt controller	0xE000E100 to 0xE000E4EF	0xE000E100 to 0xE000E4EF
	System control block	0xE000ED00 to 0xE000ED3F	0xE000ED00 to 0xE000ED3F
	Floating point unit coprocessor access control	NA	0xE000ED88 to 0xE000ED8B
	Memory protection unit	0xE000ED90 to 0xE000EDB8	0xE000ED90 to 0xE000EDB8
	Nested vectored interrupt controller	0xE000EF00 to 0xE000EF03	0xE000EF00 to 0xE000EF03
	Floating point unit	NA	0xE000EF30 to 0xE000EF44

Color key:

= Feature not available (NA)

6 Revision history

Table 33. Document revision history

Date	Revision	Changes
11-Apr-2016	1	Initial release.
13-Feb-2017	2	Updated the whole document with reference to: – STM32L49xxx/4Axxx devices – STM32L47xxx/48xxx devices – STM32L45xxx/46xxx devices – STM32L43xxx/44xxx devices Updated STM32L4 Series reference manual list in cover. Updated *Table 1: STM43L4 Series and STM32L4+ Series memory availability*. Updated *Figure 4: STM32L4 Series / STM32L4+ Series generation of clock for SAI master mode (when MCLK is required)*. Updated *Section 2.1: Package availability*: – Added *Table 2: Packages available on STM32L4 Seriesand STM32L4+ Series*. – Updated *Table 3: Packages available on STM32F2x5 line*. – Added *Table 4: STM32F2x5 line and STM32L4 Series / STM32L4+ Series pinout differences (QFP)*. – Added *Section : SMPS packages*. Updated *Table 6: Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx devices* note 1. Added I2C4 in – *Table 10: DMA differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series*. – *Table 12: Interrupt vector differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series*. – *Table 14: STM32L4 Series / STM32L4+ Series performance versus VCORE ranges*. Updated *Table 21: FLASH differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series* Flash empty check mechanism feature.
01-Sep-2017	3	Updated the whole document to add STM32L4+ Series devices information.

Table 33. Document revision history (continued)

Date	Revision	Changes
13-Apr-2018	4	Updated: – *Table 7: Bootloader interfaces* – DAC naming: 1 DAC with 2 channels instead of 2 DACs
20-Sep-2018	5	Added – Information related to STM32L41xxx/42xxx to the whole document Updated – Cover page – *Section 1: STM32L4 Series and STM32L4+ Series overview* – *Section 3: Boot mode selection* – *Section : Regarding the SRAM on page 28* – *Section 4.5.3: Peripheral clock configuration* – *Section 5.1: References* – *Table 1: STM43L4 Series and STM32L4+ Series memory availability* – *Table 2: Packages available on STM32L4 Series and STM32L4+ Series* – *Table 6: Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices* – *Table 7: Bootloader interfaces* – *Table 8: STM32 peripheral compatibility analysis STM32F2x5 line versus STM32L4 Series / STM32L4+ Series* – *Table 11: DMA request differences migrating STM32F2x5 line to STM32L4 Series / STM32L4+ Series* – *Table 12: Interrupt vector differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series* – *Table 13: RCC differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series* – *Table 17: PWR differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series* – *Table 20: EXTI differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series* – *Table 21: FLASH differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series* – *Table 23: I2C differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series* – *Table 24: SPI differences between STM32F2x5 line and STM32L4 Series / STM32L4+ Series* – *Table 28: USB FS on STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices* – *Table 29: ADC differences between STM32F2x5 line and STM32L4 Series/ STM32L4+ Series*