STEVAL-ISA174V1: VIPer0P 7 W double output non-isolated flyback

Introduction

The STEVAL-ISA174V1 is a 7 W double output power supply (-5 V/+7 V) set in a non-isolated flyback topology using VIPer0P, STMicroelectronics' latest innovative IC for building smart power supplies with energy green management.

The evaluation board has the following characteristics:

- Zero-power input consumption ratified as per IEC62301 Clause 4.5 (P_{IN_ZPM} < 5 mW at 230 V_{AC})
- Five-star energy efficiency when operating under no load ($P_{IN\_no\_load}$ < 10 mW at 230 V_{AC})
- Compliant with the ErP Lot 6 Tier 2 requirements for household and office equipment in off mode
- Compliant with the 10% load efficiency and 4-point average active-mode efficiency targets prescribed by the European CoC ver. 5 Tier 2
- Meets European regulation 1275/2008 regarding eco-design requirements for standby and off-mode electric power consumption for household and office equipment
- Meets IEC55022 Class B conducted EMI even with reduced EMI filter, thanks to the frequency jittering feature
- RoHS compliant

These targets are achieved because of the following features of the VIPer0P:

- 800 V avalanche rugged Power MOSFET
- Embedded HV start-up
- Zero-Power Mode function
- Pulse frequency modulation (PFM) and ultra-low standby consumption of the internal circuitry under light load conditions
- 60 kHz fixed switching frequency with jittering

Other VIPer0P features facilitating system design with minimum component counts are:

- On-board trans-conductance error amplifier internally referenced to 1.2 V ± 2% with separate ground to easily set a negative output
- Self-biasing option to avoid auxiliary winding and bias components
- Current mode PWM controller with drain current limit protection for easy compensation

Enhanced system reliability is ensured by the built-in soft start function and by the following set of protections:

- Pulse skip mode to avoid flux-runaway
- delayed overload protection (OLP)
- max. duty cycle counter
- V_{CC} clamp
- thermal shutdown

All protections are auto restart mode, except for pulse-skip mode.

1 Adapter features

Table 1. STEVAL-ISA174V1 electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	[$85V_{AC}$; $265V_{AC}$]
Output voltage 1	V_{OUT1}	-5 V
Max output current 1	I_{OUT1}	0.84 A
Output voltage 2	V_{OUT2}	+7 V
Max output current 2	I_{OUT2}	0.4 A
Total output power (P_{OUT1}+P_{OUT2})	P_{OUT_tot}	7 W
Precision of output 1 regulation	Δ_{VOUT1_LF}	± 5%
High frequency output 1 voltage ripple	Δ_{VOUT1_HF}	50 mV
Max ambient operating temperature	T_{AMB}	60 °C
Switching frequency	FOSC	60 kHz

Figure 1. STEVAL-ISA174V1 top view

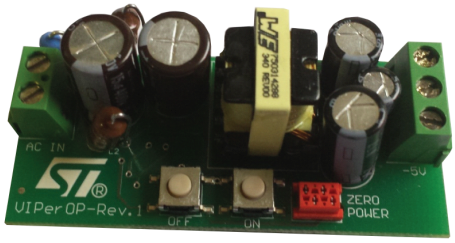
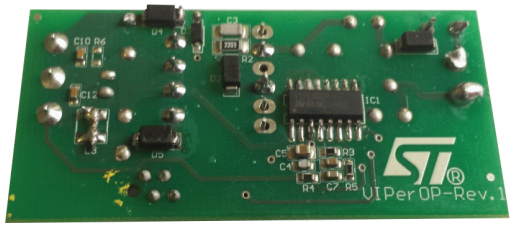


Figure 2. STEVAL-ISA174V1 bottom view



2 Circuit description

The power supply is set in non-isolated flyback topology, schematic is given in Figure 5. STEVAL-ISA174V1 schematic diagram, bill of materials in Table 2. STEVAL-ISA174V1 bill of materials . The input section includes a resistor R1 for inrush current limiting, a diode D1 and a Pi filter for EMC suppression. The FB pin is the inverting input of an error amplifier and is an accurate 1.2 V voltage reference respect to EAGND. This pin is a separate ground which can float down to -12.5 V with respect to the ground of the device (SGND). This allows the negative output voltage V_{OUT1} to be set and tightly regulated by simply connecting EAGND to the negative rail and a voltage divider between FB, EAGND and SGND, according to the following formula (with reference to the schematic in Figure 5. STEVAL-ISA174V1 schematic diagram):

$$\left|V_{OUT1}\right| = 1.2V \cdot \left(1 + \frac{R3}{R4}\right) \quad (1)$$

The secondary output V_{OUT2} is semi-regulated to +7 V by magnetic coupling through the turn ratio of the two output windings. The C-R-C network from COMP (the output of the error amplifier) to SGND pin provides frequency compensation to the feedback loop that regulates the voltage of the main output. PGND, the ground reference of the power section, is connected to SGND with the shortest track and with the lowest impedance, in order to avoid mismatches between the ground references of the signal part and the power part of the IC. At power-up, as V_{DRAIN} exceeds $V_{HVSTART}$, the internal HV current generator charges the V_{CC} capacitor, C5, to V_{CCon}, the Power MOSFET starts switching, the current generator is turned off and the IC is powered by the energy stored in C5.

Generally speaking, the VIPer0P can be self-biased or externally biased. If V_{CC} can fall down to V_{CSon}, the IC biasing is referred to as "self-biasing"; as soon as this happens, the HV source is activated until V_{CC} is recharged to V_{CCon}; this results in a sawtooth V_{CC} shape between V_{CSon} and V_{CCon} (see Figure 4. V_{CC} waveforms self-biasing (diode D3 not connected)). The use of self-biasing allows ommitting the transformer auxiliary winding and auxiliary rectifier (only a capacitor across V_{CC} and SGND is needed), at the expense of higher power dissipation and worse standby performance. If V_{CC} is prevented from falling down to V_{CSon}, the IC biasing is referred to as "external biasing". Since the maximum value of V_{CSon} (from the VIPer0P datasheet) is 4.5 V, this is easily obtained by simply connecting the small signal diode D3 from the +7 V output, V_{OUT2}, to VCC (see Figure 3. V_{CC} waveforms external biasing (diode D3 connected)) . The HV current source is never activated and, thanks to the low consumption of the internal blocks of the VIPer0P and to an adequate design, very low input power consumption in no load condition is reached (less than 10 mW at 230V_{AC}).

Another key feature of the IC is Zero-Power-Mode: an idle state during which the device is totally shut down and the residual consumption from the mains at 230 V_{AC} is kept below 5 mW. The IC enters ZPM by forcing OFF to SGND for more than 10 ms, and exits ZPM (resuming normal switching) forcing ON to SGND for more than 20 µs. This function can be tested by pressing the tactile switches connected across ON and OFF vs SGND.

Figure 3. V_{CC} waveforms external biasing (diode D3 connected)

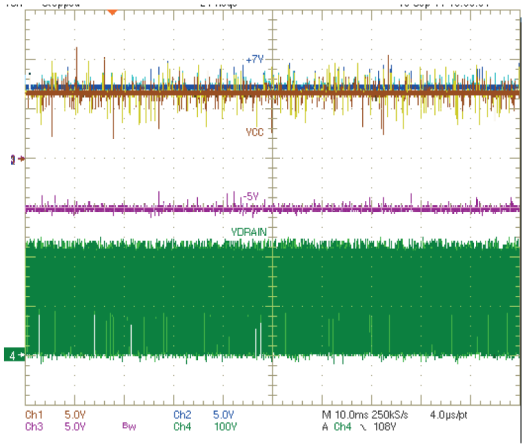
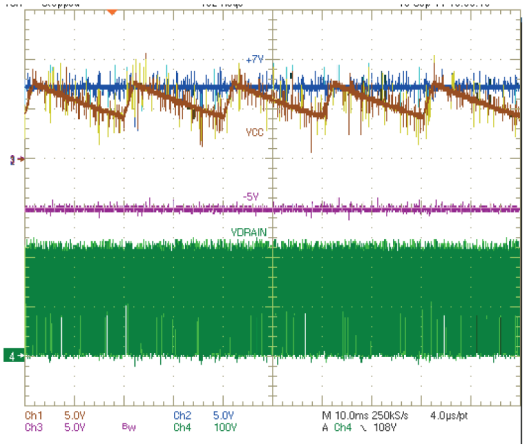
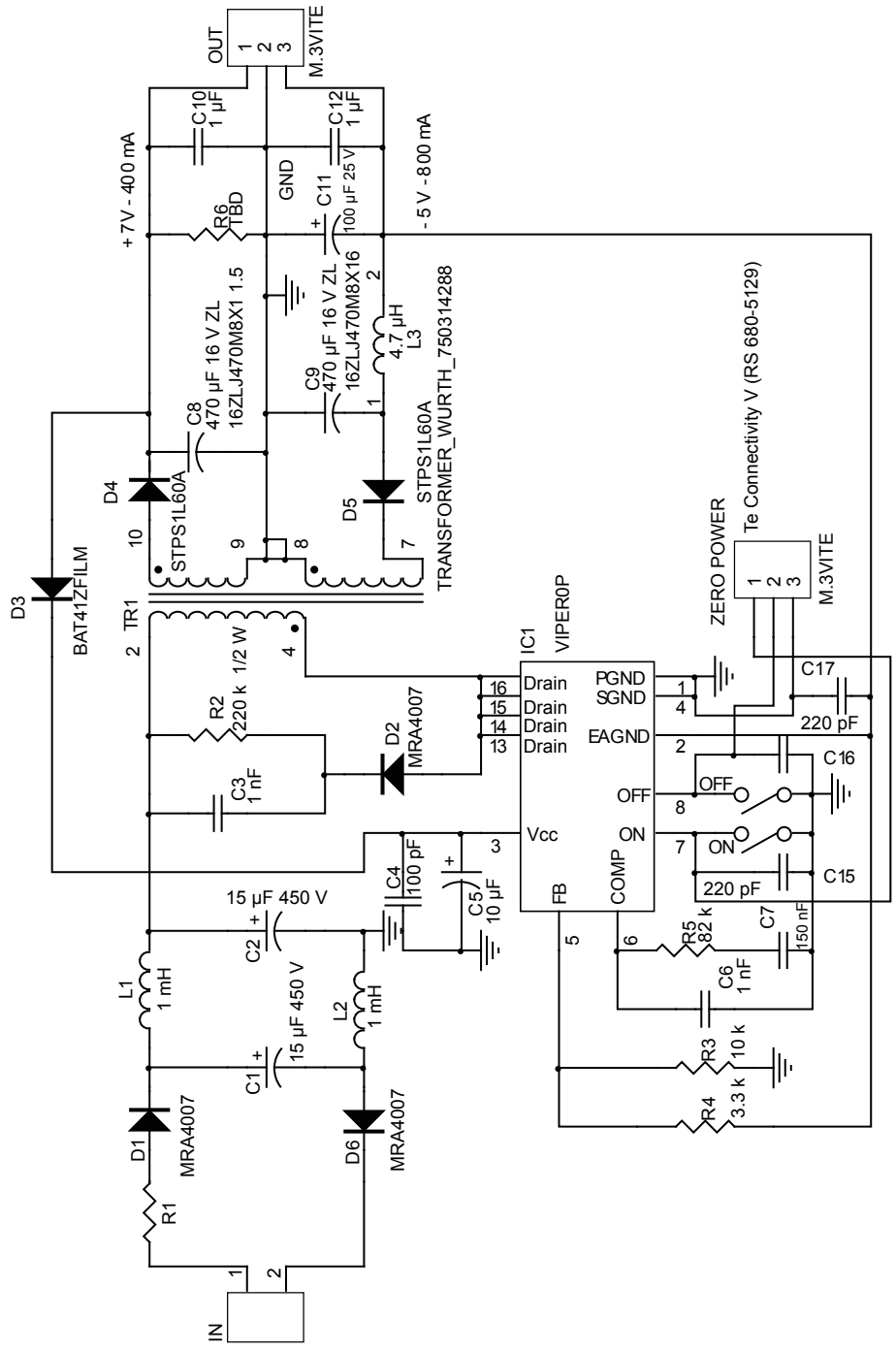


Figure 4. V_{CC} waveforms self-biasing (diode D3 not connected)



3 Schematic diagram

Figure 5. **STEVAL-ISA174V1 schematic diagram**



4 Bill of materials

Table 2. **STEVAL-ISA174V1 bill of materials**

Ref	Part number	Manufacturer	Description	Package
R1	ROX1SJ10R	TE Connectivity	10 Ω 1 W flameproof	Ø3 mm - p9 mm
R2	ERJ-P08J224V	Panasonic	220 kΩ±5% - 0.33 W - 200 V	1206
R3	ERJP03F1002V	Panasonic	10 kΩ±1% - 0.2 W	0603
R4	ERJP03F3301V	Panasonic	3.3 kΩ ±1% - 0.2 W	0603
R5	ERJP03F8202V	Panasonic	82 kΩ ±1% - 0.2 W	0603
R6				
C1	UVC2G150MPD	Nichicon	Elcap 15 µF - 400 V	Ø10 mm - p5 mm - h18 mm
C2	UVC2G150MPD	Nichicon	Elcap 15 µF - 400 V	Ø10 mm - p5 mm - h18 mm
C3	C3216C0G2J102J085 AA	TDK	MLCC capacitor 1 nF - 630 V	1206
C4	GRM1885C1H101JA0 1D	Murata	MLCC capacitor 100 pF - 50 V	0603
C5	C2012X5R1E106K125 AB	TDK	MLCC capacitor 10 µF - 25 V	0805
C6	C1608C0G1H102J080 AA	TDK	MLCC capacitor 1 nF - 50 V	0603
C7	06035C153KAT2A	AVX	MLCC capacitor 15 nF - 50 V	0603
C8	16ZLJ470M8X11.5	Rubycon	Elcap 470 µF - 16 V	Ø8 mm - p5 mm - h11.5 mm
C9	16ZLK470M8X16	Rubycon	Elcap 470 µF - 16 V	Ø8 mm - p5 mm - h16 mm
C10	GRM188C81E105KA ADD	Murata	MLCC capacitor 1 µF - 25 V	0603
C11	16YXF100M6.3X11	Rubycon	MLCC capacitor 100 µF - 16 V	Ø6.3 mm - p2.5 mm - h11 mm
C12	GRM188C81E105KA ADD	Murata	MLCC capacitor 1 µF - 25 V	0603
C15	C0805C221J5GACTU	Kemet	MLCC capacitor 220 pF 50 V	0603
C16	C0805C221J5GACTU	Kemet	MLCC capacitor 220 pF 50 V	0603
C17	C0805C221J5GACTU	Kemet	MLCC capacitor 220 pF 50 V	0603
D1	MRA4007T3G	ON Semiconductor	1 A-1000 V Power rectifier diode	SMA
D2	MRA4007T3G	ON Semiconductor	1 A-1000 V Power rectifier diode	SMA
D3	BAT41ZFILM	STMictroelectronics	0.15 A-100 V Signal schottky	SOD-123
D4	STPS1L60A	STMictroelectronics	1 A-60 V Power schottky	SMA
D5	STPS2L60A	STMictroelectronics	2 A-60 V Power schottky	SMA
D6	MRA4007T3G	ON Semiconductor	1 A-1000 V Power rectifier diode	SMA
L1	B82144A2105J	Epcos	1 mH axial inductor	
L2	B82144A2105J	Epcos	1 mH axial inductor	
L3	74404042033	Wurth	Power induction 3.3 µA	(4x4x1.8) mm
IC1	VIPer0PL	STMicroelectronics	Power Switcher	SO-16
TF	750314288 Rev0	Wurth Elektronik	Flyback transformer	E16

5 Transformer

Table 3. Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	WURTH	
Part number	750314288 Rev0	
Primary inductance (pins 3 - 4)	2.5 mH ±10%	Meas. at 10 kHz, 0.1V_{AC}
Leakage inductance	42 µH to 84 µH	Meas. at 10 kHz, 0.1V_{AC}
Primary to sec 1 turn ratio (4 - 2)/(8 - 7)	(14.23):(1.00), ±1%	
Primary to sec 2 turn ratio (4 - 2)/(10 - 9)	(10.27):(1.00), ±1%	

Figure 6. Transformer: electric and pins diagram (a)

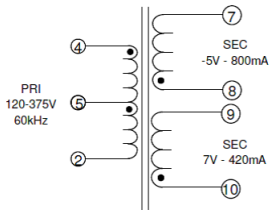


Figure 7. Transformer: electric and pins diagram (b)

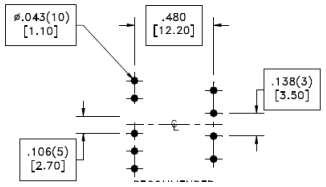


Figure 8. Transformer size in mm (bottom view)

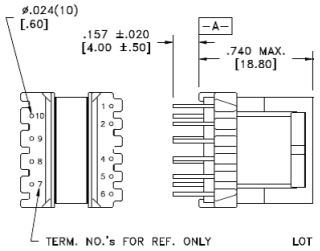
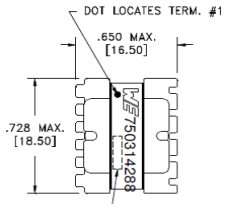


Figure 9. Transformer size in mm(top view)



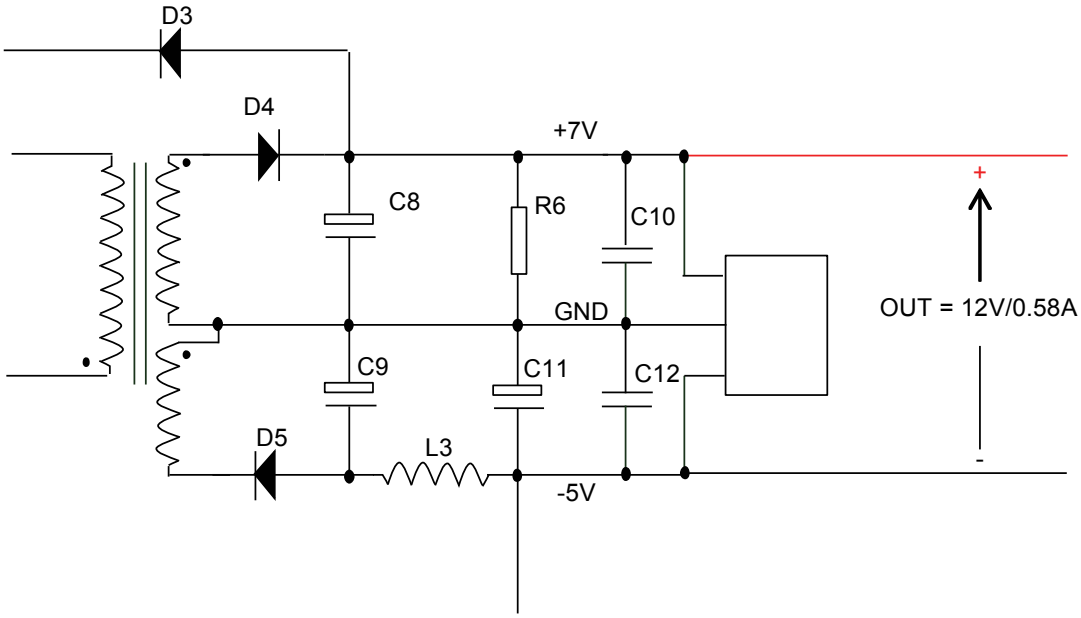
6 Testing the board

6.1 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}). External power supplies (in a separate housing from the devices they are powering) need to comply with the code of conduct, version 5 "Active mode efficiency" criterion requiring, for a power throughput of 7 W, an active mode efficiency higher than 77% (CoC5 tier1, effective since January 2014) and 80% (CoC5 tier2, starting from January 2016). Another applicable standard is the United States Department of Energy (DOE) recommendation, whose active mode efficiency requirement for the same power throughput is 79.8%.

The abovementioned requirements only refer to single output converters, which is not the case for the STEVAL-ISA174V1, which has two outputs. However, just to give an indication of its performance, the measurements were conducted on the equivalent single-output 12 V/7 W converter, simply obtained by connecting the load across the V_{OUT1} and V_{OUT2} lines, as shown in the following figure.

Figure 10. Output load connection of STEVAL-ISA174V1 for board performances evaluation



From the following table, the equivalent single-output SMPS is code of conduct 5 (Tier1 and Tier2) and DOE compliant, despite its efficiency being adversely affected by the double voltage drop across D4 and D5. In a true 12 V/7 W SMPS (with a single secondary rectifier) it is reasonable to expect 3-4% higher efficiency values.

Table 4. STEVAL-ISA174V1 evaluation board performance

Active mode efficiency				
CoC5 requirements (P_{OUT} = 7 W)		DOE requirement (P_{OUT} = 7 W)	Board performance	
Tier 1	Tier 2		V_{IN}= 115V_{AC}	81.60%
77%	80%	79.80%	V_{IN}= 230V_{AC}	81.50%

6.2 Light load performance

CoC5 also has efficiency requirements when the output load is 10% of the nominal output power. The equivalent single-output SMPS is compliant with both Tier 1 and Tier2 requirements, as shown in the following table.

Table 5. CoC5 requirement and performance at 10% output load

Minimum efficiency requirement at 10% of full load			
V_{IN}	Board performance		CoC5 requirements for P_{OUT} = 7 W
		Tier 1	Tier 2
115 V_{AC}	78.01%	66.7%	70.0%
230 V_{AC}	71.40%		

In version 5 of the code of conduct, the power consumption of the power supply when it is not loaded is also considered. The compliance criteria for EPS converters with nominal output power below 49 W and the no-load input power consumption measurements of the evaluation board at nominal input voltages (115 V_{AC} and 230 V_{AC}), are given in the following table. The performance results are well above both Tier 1 and Tier 2 requirements.

In the same table the consumption in Zero Power Mode (ZPM) is also given (see Section 7.7 Zero power mode).

Table 6. CoC5 Energy consumption criteria for no load & evaluation board performances

Max P_{IN} req. in no load (0.3 W < Pno < 49 W)		Evaluation board P_{IN} consumption		
Tier 1	Tier 2		No load	ZPM
150 mW	75 mW	V_{IN} = 115V_{AC}	6.5 mW	0.8 mW
		V_{IN} = 230V_{AC}	9.1 mW	3.5 mW

Depending on the equipment being powered, there may be several criteria for measuring converter performance. In particular, one requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The evaluation board can satisfy this requirement, as it can be seen from following table, where the efficiencies measured under other light load conditions, P_{OUT} = 25 mW and P_{OUT} = 50 mW, are also provided.

Table 7. Light load performance

V_{IN} [V_{AC}]	eff [%]		
	@ P_{OUT} = 25 mW	@ P_{OUT} = 50 mW	@ P_{OUT} = 250 mW
115	55.6	60.8	72.2
230	51.3	57.0	66.3

Another criterion is the measurement of the output power (or the efficiency) when the input power is equal to one watt (see following table).

Table 8. **Efficiency @ P_{IN} = 1 W**

V_{IN} [V_{AC}]	eff @ P_{IN} = 1 W[%]
115	78.3
230	71.1

6.3 Typical waveforms

Drain voltage and current waveforms under full load conditions for the two nominal input voltages are reported in Figure 11. Drain current/voltage @ 115V_{AC}, max load and Figure 12. Drain current/voltage @ 230V_{AC}, max load , and for minimum and maximum input voltage in Figure 13. Drain current/voltage @ 90V_{AC}, max load and Figure 14. Drain current/voltage @ 265V_{AC}, max load respectively.

Figure 11. **Drain current/voltage @ 115V_{AC}, max load**

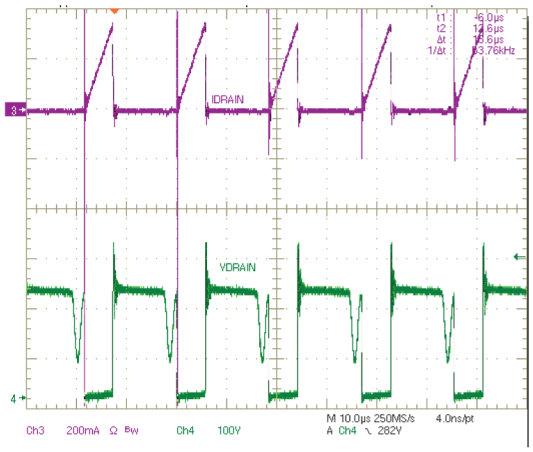


Figure 12. **Drain current/voltage @ 230V_{AC}, max load**

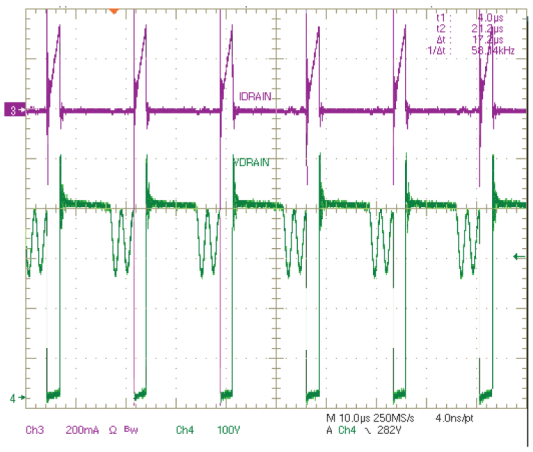


Figure 13. **Drain current/voltage @ 90V_{AC}, max load**

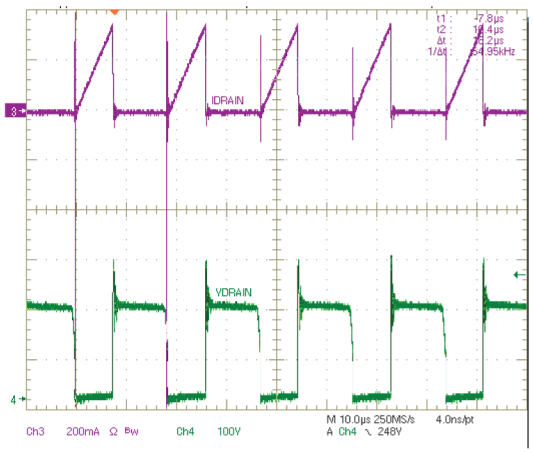
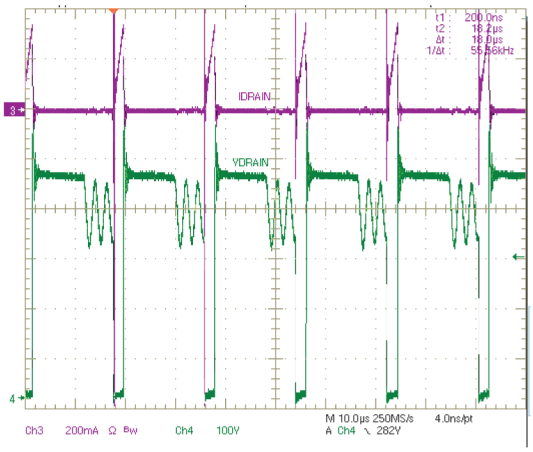


Figure 14. **Drain current/voltage @ 265V_{AC}, max load**

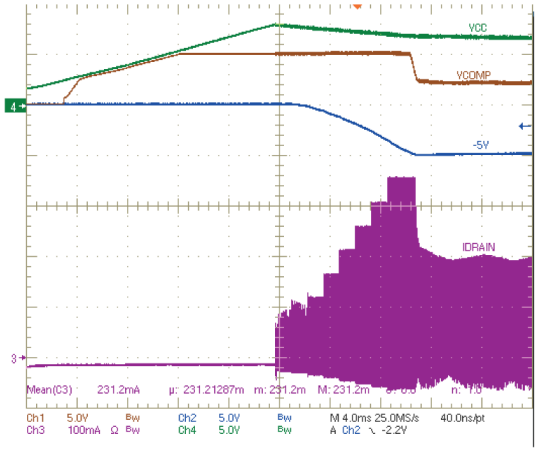


7 ICs features

7.1 Soft start

An internal soft-start function progressively increases the cycle-by-cycle current limitation point from zero up to I_{DLIM} in eight 50 mA steps. In this way, the drain current is limited during the output voltage increase, thus reducing the stress on the secondary diode. The soft-start time t_{SS} (the time needed for the current limitation point to reach its final value) is internally fixed at 8 ms. This function is activated at any converter startup attempt and after a fault event. The soft start phase is shown in the following figure.

Figure 15. Soft start



7.2 Overload protection

In case of overload or short circuit, the drain current value reaches I_{DLIM}. For every cycle where this condition is met, an internal OCP counter is incremented; if the overload continues for the time t_{OVL} (50 ms typical, internally fixed), the protection is triggered (Figure 16. OLP: fault applied during steady state operation; t_{OVL}); the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 s typical). After this time has elapsed, the IC resumes switching and, if the fault is still present, the protection persists indefinitely in the same way (Figure 17. OLP: fault applied during steady state operation; $t_{RESTART}$). This ensures restart attempts of the converter at a low repetition rate so that it works safely with extremely low power throughput and avoids IC overheating due to repeated overload events.

Furthermore, for any startup following a triggered protection, the internal soft start-up function is invoked (Figure 18. OLP: fault maintained; t_{SS} and t_{OVL}) to reduce the stress on the secondary diode. After the fault removal, the IC resumes working normally. If the fault is removed during t_{SS} or t_{OVL} (before the protection is triggered), the counter counts on a cycle-by-cycle basis down to zero and the protection is not tripped. If the short circuit is removed during $t_{RESTART}$, the IC still waits for $t_{RESTART}$ to elapse before resuming switching (Figure 19. OLP: fault removed and autorestart).

Figure 16. OLP: fault applied during steady state operation; t_{OVL}

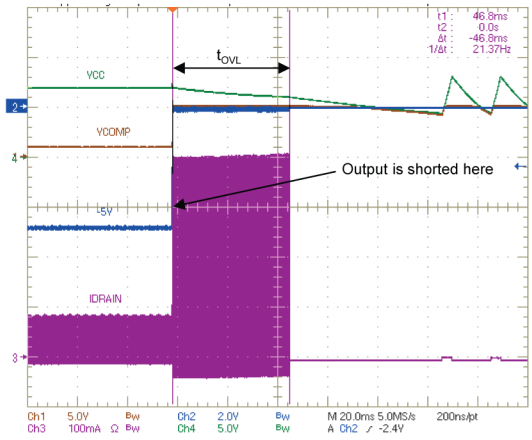


Figure 17. OLP: fault applied during steady state operation; $t_{RESTART}$

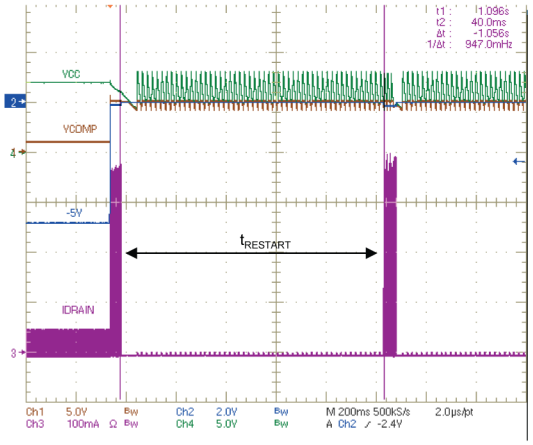


Figure 18. OLP: fault maintained; t_{SS} and t_{OVL}

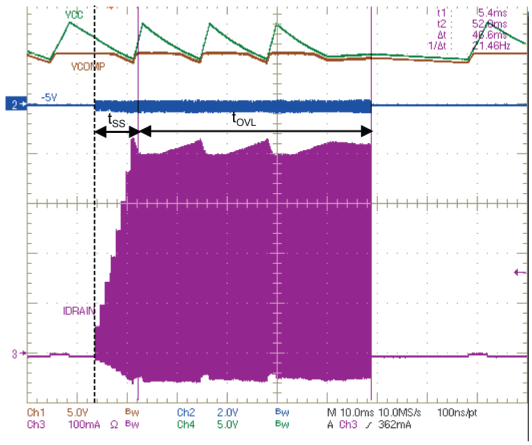
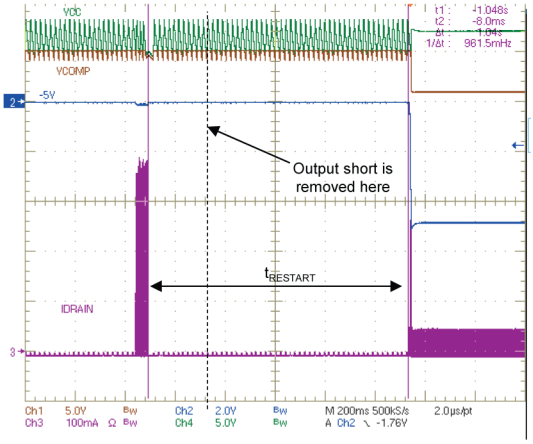


Figure 19. OLP: fault removed and autorestart



7.3 Pulse skip mode

Any time the drain peak current, I_{DRAIN}, exceeds I_{DLIM} within the minimum on-time t_{ON_MIN}, one switching cycle is skipped. The check is made on a cycle-by-cycle basis, and the cycles can be skipped down to the minimum switching frequency F_{OSC_MIN} (15 kHz, typ). If the above condition persists indefinitely, when the internal OCP counter reaches its end-of-count, the IC is stopped for $t_{RESTART}$ (1 s, typical) and activated again, with a soft-start phase. Whenever I_{DRAIN} does not exceed I_{DLIM} within t_{ON_MIN}, one switching cycle is restored. The check is made on a cycle-by-cycle basis, and the cycles can be restored until reaching the nominal switching frequency, F_{OSC}.

Providing, when needed, an inductor discharge time longer than what would be allowed at nominal switching frequency, the protection helps limit the so called "flux runaway" effect, often present at converter startup when the primary MOSFET, charged during the minimum on-time through the input voltage, cannot discharge the same amount during the off-time because the output voltage is very low. The result is a net increase of average inductor current, that can reach dangerously high values where the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance.

In order to test this protection, the secondary diodes D4 and D5 were shorted while the converter was operated at $265V_{AC}$. In Figure 20. V_{IN} = $265V_{AC}$, D4 and D5 shorted, steady-state and Figure 21. V_{IN} = $265V_{AC}$, D4 and D5 shorted, steady-state, the first part of the protection intervention is captured.

In figure Figure 21. V_{IN} = $265V_{AC}$, D4 and D5 shorted, steady-state:

- I_{DLIM} is exceeded in the first cycle so the next one is skipped, resulting in a 30 kHz switching frequency
- I_{DLIM} is exceeded again and the switching frequency is further halved to 15 kHz
- I_{DLIM} is exceeded again and the switching frequency is kept at 15 kHz indefinitely.

Figure 20. V_{IN} = 265V_{AC}, D4 and D5 shorted, steady-state

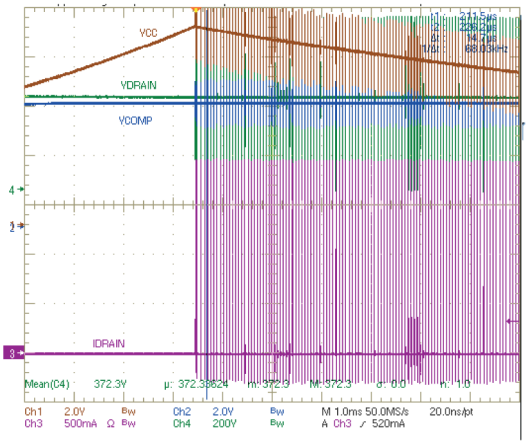
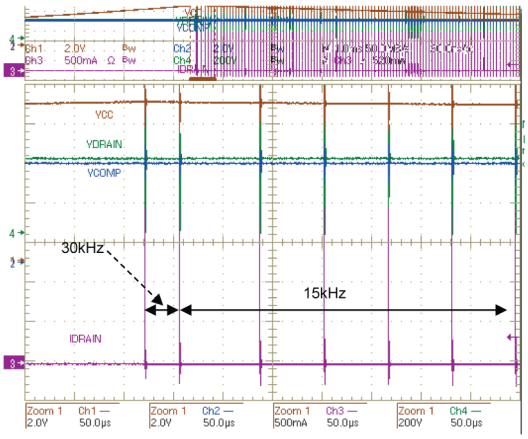


Figure 21. V_{IN} = 265V_{AC}, D4 and D5 shorted, steady-state



A magnification of one of the switching cycles of Figure 21. V_{IN} = 265V_{AC}, D4 and D5 shorted, steady-state shows the DRAIN current rising very quickly so as to exceed I_{DLIM} within t_{ON_MIN} (Figure 22. V_{IN} = 265V_{AC}, D4 and D5 shorted, zoom). The converter will operate indefinitely at 15 kHz and the OCP internal counter will increment at every switching cycle. As it is designed to reach its end of count (defining t_{OVL}) after 50 ms at 60 kHz operation, the overload time will be incremented to 200 ms, as shown in Figure 23. V_{IN} = 265V_{AC}, D4 and D5 shorted, steady-state.

Figure 22. V_{IN} = 265V_{AC}, D4 and D5 shorted, zoom

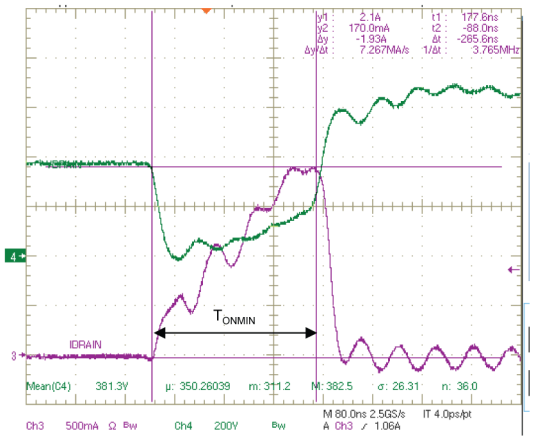
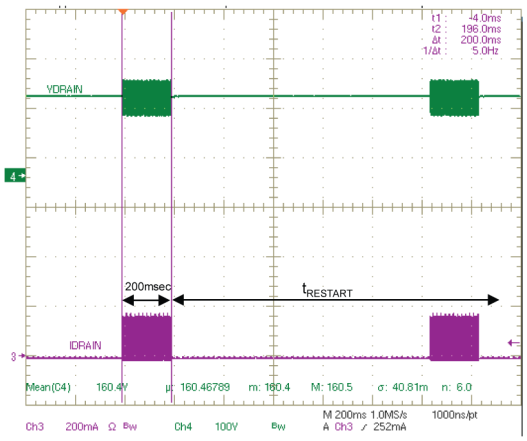


Figure 23. V_{IN} = 265V_{AC}, D4 and D5 shorted, steady-state



7.4 VCC clamp protection

V_{CC} clamp protection can be used as an overvoltage protection of sorts. In fact, if the IC is supplied by a diode from the output voltage (or by auxiliary winding as well), an output overvoltage will produce a V_{CC} increase. If V_{CC} reaches the clamp voltage $V_{CCclamp}$ (30 V min. with respect to EAGND), the current I_{CC} injected into the pin is monitored and, if it exceeds the internal threshold I_{clamp_max} (30mA, typ.) for more than t_{clamp_max} (5 ms, typ.), the IC is stopped for $t_{RESTART}$ (1 s, typ.) and then activated again with soft-start phase until the fault is removed. During $t_{RESTART}$, V_{CC} is maintained between the V_{CSon} and V_{CCon} levels by the HV current source periodical activation. If the fault is removed during $t_{RESTART}$, the IC has to wait for $t_{RESTART}$ to elapse before resume switching. The protection is disabled during the soft start time.

In this evaluation board, the output overvoltage and consequent protection activation was produced by shorting R4 to EAGND. The resulting operation is shown in Figure 24. V_{CC} clamp protection: tripping and Figure 25. V_{CC} clamp protection: tripping, autorestart and resume operation after fault removal .

Figure 24. V_{CC} clamp protection: tripping

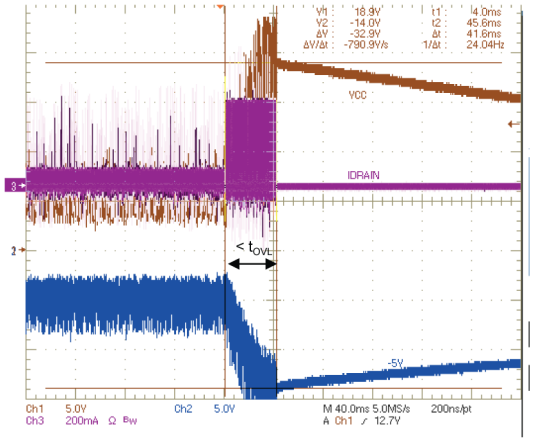
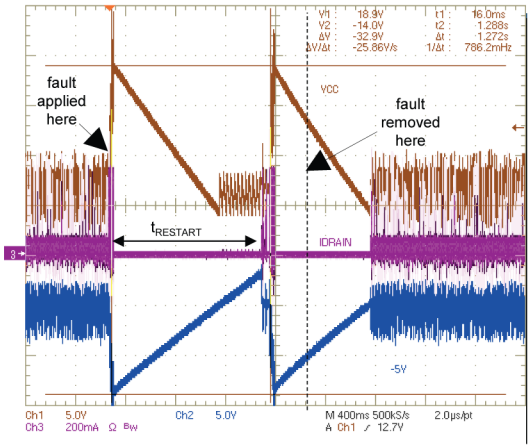


Figure 25. V_{CC} clamp protection: tripping, autorestart and resume operation after fault removal



7.5 Max duty cycle counter protection

The IC embeds a max. duty-cycle counter, which disables the PWM if the MOSFET is turned off by maximum duty cycle (70% min., 80% max.) for ten consecutive switching cycles. Following protection tripping, the PWM is disabled for $t_{RESTART}$ and reactivated with soft-start phase until the fault condition is removed.

In some cases (e.g., breaking of the loop at low input voltage) even if V_{COMP} is saturated high, the OLP cannot be triggered because, at every switching cycle, the PWM is turned off by the max. duty cycle before the DRAIN peak current can reach I_{DLIM}. As a result, the output voltage V_{OUT} may increase uncontrollably and be maintained indefinitely at a value far higher than the nominal one, with the risk of damaging the output capacitor, the output diode and the IC itself, as the 800 V breakdown threshold may be exceeded.

The max. duty cycle counter protection prevents this kind of failure. To test this protection, heavy load and low input voltage were selected. The IC is protected in autorestart mode for $t_{RESTART}$ (1 s typ.), then attempts startup with soft-start phase until the fault condition is removed (Figure 26. Shut down by max. duty cycle counter (first tripping and restart) and Figure 27. Shut down by max. duty cycle counter (steady state)).

Figure 26. Shut down by max. duty cycle counter (first tripping and restart)

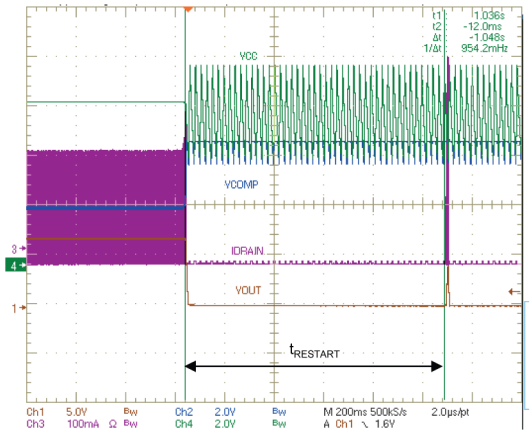
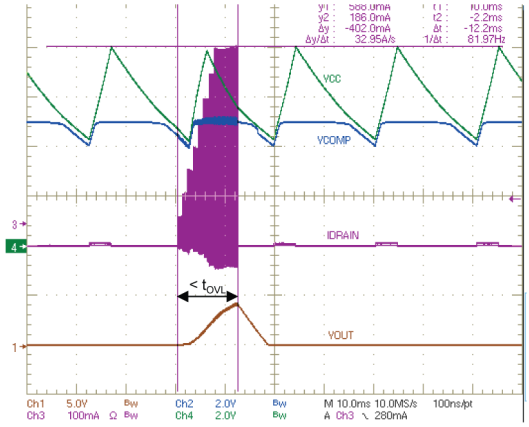


Figure 27. Shut down by max. duty cycle counter (steady state)



In Figure 28. Shut down by max. duty cycle counter (zoom of Figure 27) , the ten cycles causing the protection intervention are highlighted; in Figure 29. First of the 10 consecutive switching cycles at max. duty cycle (zoom of Figure 28) the magnification of one of them is shown, with the duty cycle measurement: 11.4 / (11.4 + 4.2) = 73.1%.

Figure 28. Shut down by max. duty cycle counter (zoom of Figure 27)

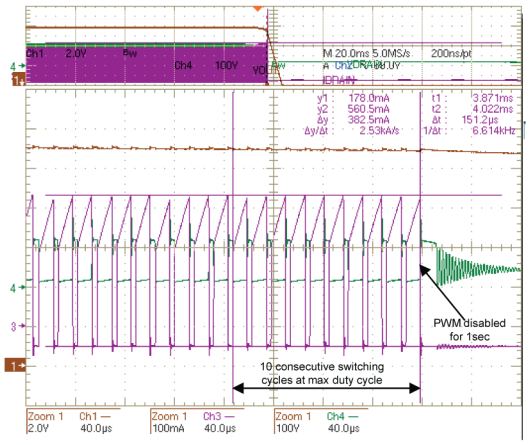
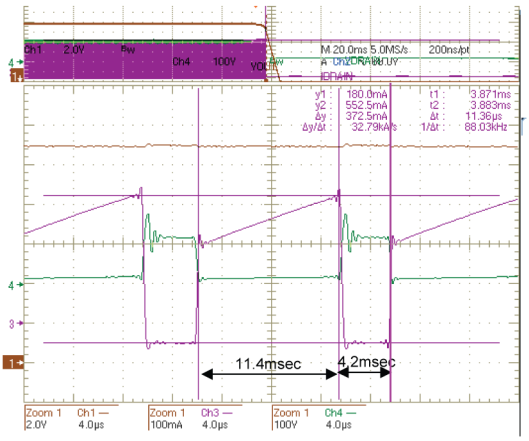


Figure 29. First of the 10 consecutive switching cycles at max. duty cycle (zoom of Figure 28)



7.6 Overtemperature protection

If the VIPer0P junction temperature rises higher than the internal threshold T_{SD} (160 °C, typ.), the PWM is disabled for $t_{RESTART}$. Following this, a single switching cycle is performed, during which the temperature sensor embedded in the Power MOSFET section is checked. If the measured junction temperature is still above T_{SD}, the PWM is kept disabled for $t_{RESTART}$ time (Figure 30. OTP tripping and steady-state and Figure 31. Turn on for thermal check during OTP).

On the evaluation board, overheating was produced after several minutes at low input voltage (60 V_{DC}) and heavy load (12 V / 0.55 A). The IC shuts down when a case temperature of approximately 152 °C is measured (through a thermal camera). As the load is decreased, the converter restarts with the soft start phase when the case temperature reaches about 120 °C.

Figure 30. OTP tripping and steady-state

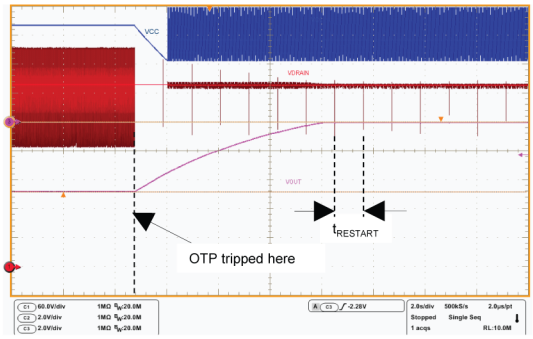
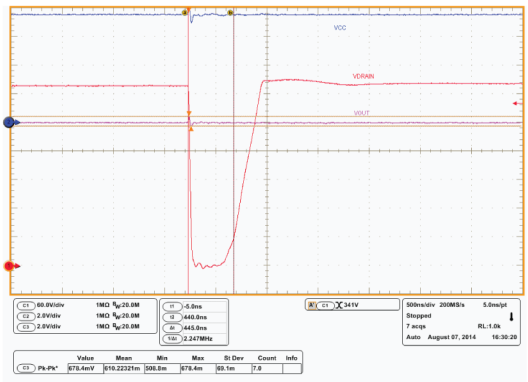


Figure 31. Turn on for thermal check during OTP



7.7 Zero power mode

The Zero power mode is an idle state of the converter characterized by the following features:

- no switching activity, and so no voltage nor power available at the output

- the HV current source charges the V_{CC} voltage at 13 V and does not perform its usual functions
- all the IC circuits except those needed to exit ZPM are turned off, reducing controller consumption to very low values

In ZPM, the power supply can draw less than 5 mW @ 230V_{AC} from the mains, which is regarded as a “zero power consumption” condition. The IC enters ZPM when, by pressing on the relevant tactile switch in Section 3 Schematic diagram, the OFF pin is forced to SGND for more than t_{DEB_OFF} (10 ms typ.): switching is stopped, V_{CC} is charged to 13 V (see Figure 32. Entering ZPM and Figure 33. entering ZPM (zoom)).

Figure 32. Entering ZPM

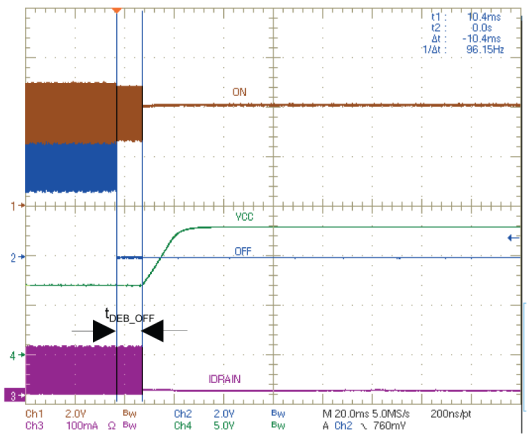
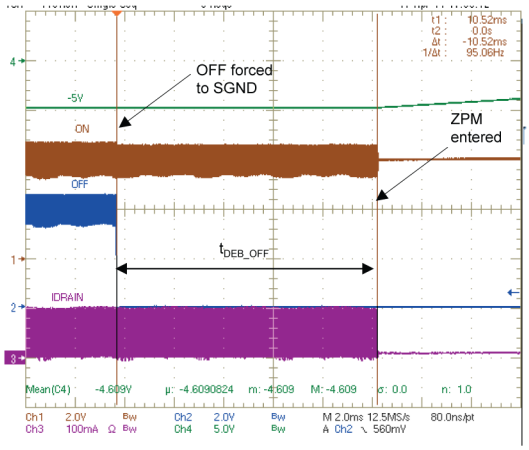


Figure 33. entering ZPM (zoom)



The IC exits ZPM when, by pressing the relevant tactile switch in Section 3 Schematic diagram, the ON pin is forced to SGND for more than t_{DEB_ON} (20 µs typ.); the device resumes switching (with soft start phase) and the delivery of power to the output (see Figure 34. Exiting ZPM and Figure 35. Exiting ZPM (zoom)) resumes. At startup, the pulse skip mode may also be invoked (Figure 36. Exiting ZPM: t_{DEB_ON} and pulse skip mode and Figure 37. Exiting ZPM: pulse skip mode).

Figure 34. Exiting ZPM

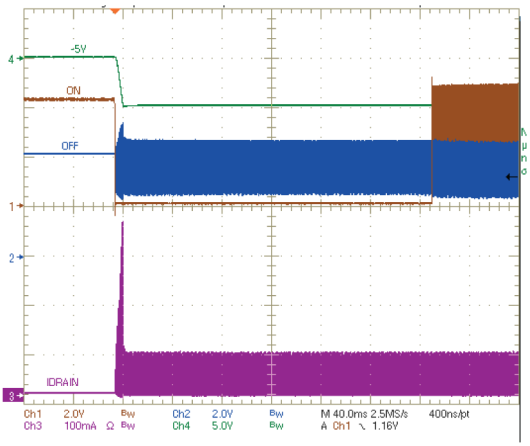


Figure 35. Exiting ZPM (zoom)

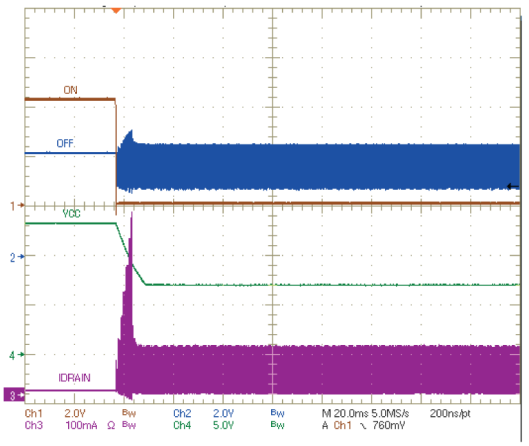


Figure 36. Exiting ZPM: t_{DEB_ON} and pulse skip mode

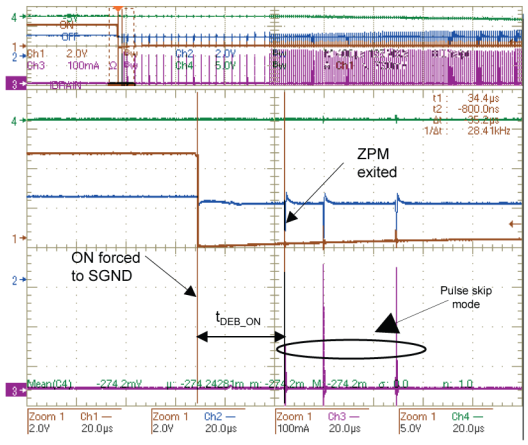
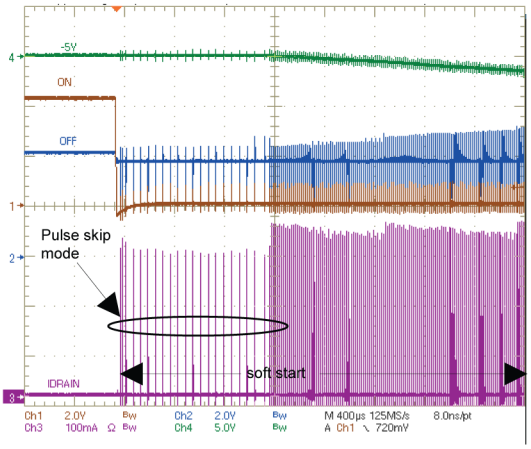


Figure 37. Exiting ZPM: pulse skip mode



In real appliances such as dishwashers or washing machines, ZPM can be managed by a microcontroller (MCU), supervising the operation of the appliance and entering OFF mode when the end of the working cycle is recognized. Once in this state, the SMPS delivers no voltage at its output terminals (consuming less than 5 mW from the power line at 230 V_{AC}) and waits for a manual restart from the user.

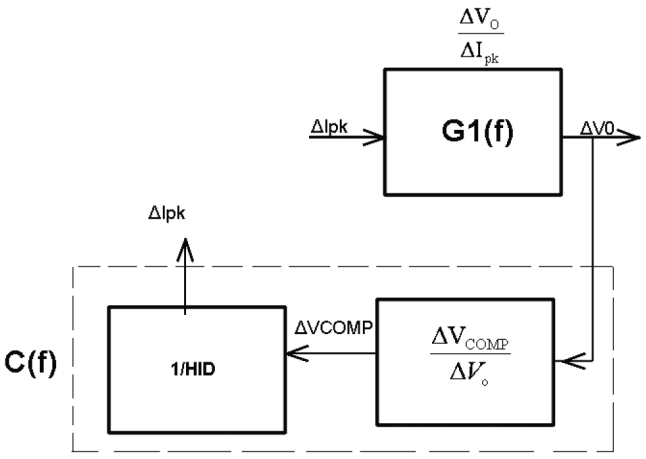
If the MCU is rated for a 3.3 V supply voltage and features an ultra-low consumption standby mode, it can be powered during ZPM also using the resistive pull-up available at the ON pin (R_{ON}, 41 kΩ typ.). In this case, the MCU shuts the SMPS down by pulling the OFF pin low and wakes it up by pulling the ON pin low.

8 Feedback loop calculation guidelines

8.1 Transfer function

In the following diagram, the set PWM modulator plus power stage is indicated by G1(f), while C(f) is the controller; i.e., the network which ensures the stability of the system.

Figure 38. Control loop block diagram



The mathematical expression of the power system G1(f) is:

$$G1(f) = \frac{\Delta V_O}{\Delta I_{pk}} = \frac{\left|V_{OUT1}\right| \cdot \left(1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z}\right)}{Ipkp\left(fsw, Vdc\right) \cdot \left(1 + \frac{j \cdot 2 \cdot \pi \cdot f}{2}\right)} = \frac{\left|V_{OUT1}\right| \cdot \left(1 + \frac{j \cdot f}{fz}\right)}{Ipkp\left(fsw, Vdc\right) \cdot \left(1 + \frac{j \cdot f}{fp}\right)} \quad (2)$$

fp is the pole due to the output load and fz the zero due to the ESR of the output capacitor:

$$fp = \frac{1}{\pi \cdot C_{OUT\_eq} \cdot \left(R_{OUT\_eq} + 2 \cdot ESR\_eq\right)} \quad (3)$$

$$fz = \frac{1}{2 \cdot \pi \cdot C_{OUT\_eq} \cdot ESR_{\_eq}} \quad (4)$$

where C_{OUT_eq}, $ESR_{\_eq}$ and R_{OUT_eq} are obtained referencing the output capacitance, ESR and output resistance of the unregulated output, V_{OUT2}, to the regulated output, V_{OUT1}, through the turn ratio of the transformer:

$$C_{OUT\_eq} = C_{OUT1} + C_{OUT2\_eq} \quad (5)$$

$$R_{OUT\_eq} = \frac{1}{\frac{1}{R_{OUT1}} + \frac{1}{R_{OUT2\_eq}}} \quad (6)$$

$$ESR_{\_eq} = \frac{1}{\frac{1}{ESR1} + \frac{1}{ESR2_{\_eq}}} \quad (7)$$

The mathematical expression of the compensator C(f) is:

$$C(f) = \frac{\Delta I_{pk}}{\Delta V_o} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{\left(2 \cdot \pi \cdot f \cdot j\right) \cdot \left(1 + \frac{f \cdot j}{fPc}\right)} \quad (8)$$

where:

$$C_0 = \frac{G_M}{C6 + C7} \cdot \frac{R4}{R3 + R4} \quad (9)$$

$$fZc = \frac{1}{2 \cdot \pi \cdot R5 \cdot C7} \quad (10)$$

$$fPc = \frac{1}{2 \cdot \pi \cdot R5} \cdot \frac{C6 + C7}{C7 \cdot C6} \quad (11)$$

are to be chosen in order to censure the stability of the overall system. G_M is the VIPer0P transconductance, $H_{COMP} = (V_{COMPH} - V_{COMPL})/(I_{DLIM} – I_{DLIM\_PFM})$ is the slope of the V_{COMP} vs I_{DRAIN} characteristic.

8.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossing frequency:

$$fZc = x \cdot fp \quad (12)$$

$$fPc = y \cdot fp \quad (13)$$

$$fcross \leq \frac{fsw}{10} \quad (14)$$

where x and y are arbitrarily chosen. G1(fcross) can be calculated from equation (2) and, since by definition $\left| C(fcross)*G1(fcross) \right| = 1$, C_0 is obtained from equation (8) thus:

$$C_0 = \frac{\left|2 \cdot \pi \cdot fcross \cdot j\right| \cdot \left|1 + \frac{fcross \cdot j}{fPc}\right|}{\left|1 + \frac{fcross \cdot j}{fZc}\right|} \cdot \frac{H_{COMP}}{|G1(fcross)|} \quad (15)$$

At this point the bode diagram of G1(f)*C(f) can be plotted to check the phase margin for stability. If the margin is not sufficiently high, alternative values should be chosen for fZc, fPc and fcross and the procedure repeated. Once stability is achieved, the values of the schematic components to implement C(f) are chosen as follows:

- R3 is set in the range of some ten kohms
- R4 is calculated from (1)

$$R4 = \frac{R3}{\frac{|V_{OUT1}|}{V_{REF\_FB}} - 1} \quad (16)$$

- C6 is calculated combining (9), (10) and (11):

$$C6 = \frac{fZc}{fPc} \cdot \frac{G_M}{|C_0|} \cdot \frac{R4}{R3 + R4} \quad (17)$$

- C7 is obtained from the combination of (10) and (11):

$$C7 = C6 \cdot \left(\frac{fPc}{fZc} - 1\right) \quad (18)$$

- Finally, R5 is derived from (11)

$$R5 = \frac{1}{2 \cdot \pi \cdot fPc} \cdot \frac{C6 + C7}{C6 \cdot C7} \quad (19)$$

After selecting commercial values for R3, R4, C6, C7 and R5, the actual values of C_0, fZc and fPc should be calculated using equations (9), (10) and (11), to obtain C_0_act , fZc_act and fPc_act respectively. Substituting these values in equation (8), the actual compensator, C_act(f), is obtained.

The Bode diagram of G1(f)*C_act(f) can be plotted to check whether the phase margin for the stability is still ensured.

9 Thermal measurements

A thermal analysis of the board was performed using an IR camera for 90 V_{AC}, 115 V_{AC}, 230 V_{AC} and 265 V_{AC} mains input, under full load condition. The results are shown in the following figures.

Figure 39. Thermal camera @ V_{IN} = 90V_{AC}, max load, T_{AMB} = 25 °C, VIPer0P side

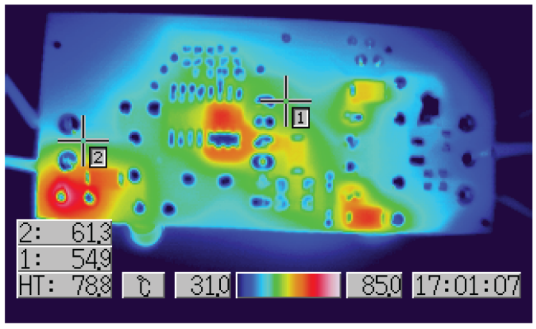


Figure 40. Thermal camera @ V_{IN} = 90V_{AC}, max load, T_{AMB} = 25 °C, transformer side

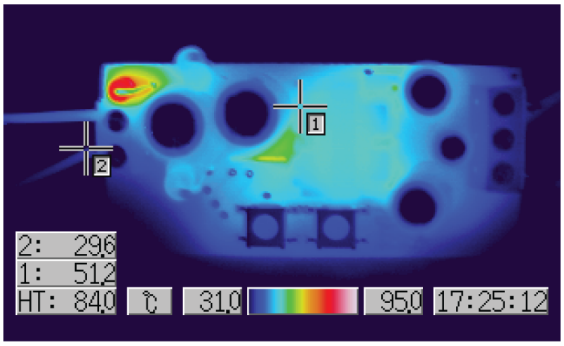


Figure 41. Thermal camera @ V_{IN} = 115V_{AC}, max load, T_{AMB} = 25 °C, VIPer0P side

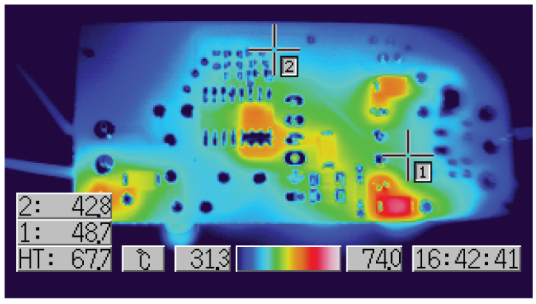


Figure 42. Thermal camera @ V_{IN} = 115V_{AC}, max load, T_{AMB} = 25 °C, transformer side

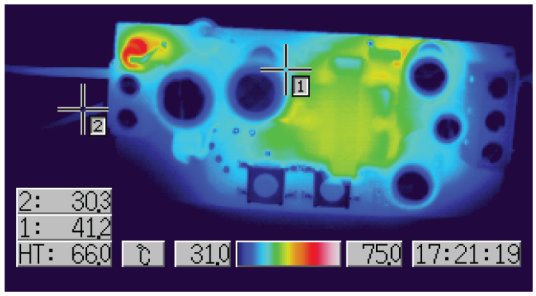


Figure 43. Thermal camera @ V_{IN} = 230V_{AC}, max load, T_{AMB} = 25 °C, VIPer0P side

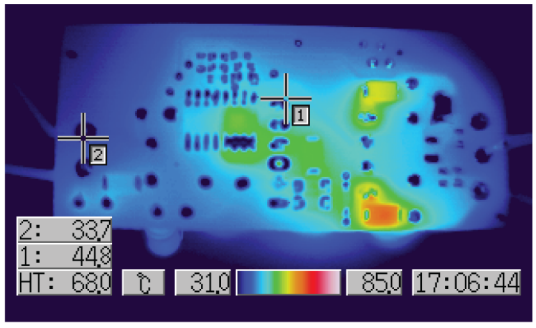


Figure 44. Thermal camera @ V_{IN} = 230V_{AC}, max load, T_{AMB} = 25 °C, transformer side

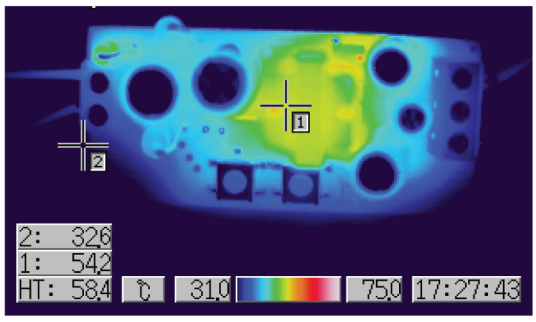


Figure 45. Thermal camera @ V_{IN} = 265V_{AC}, max load, T_{AMB} = 25 °C, VIPer0P side

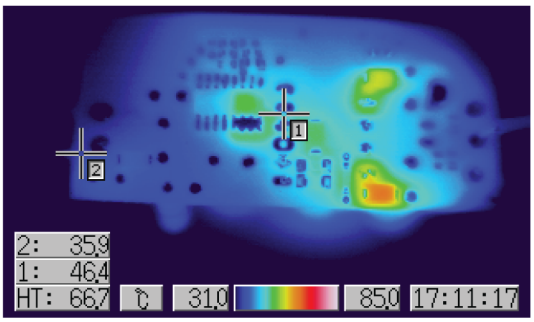
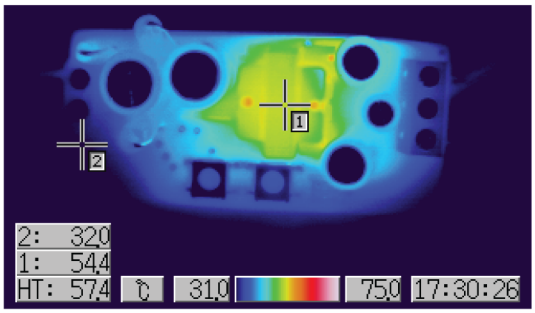


Figure 46. Thermal camera @ V_{IN} = 265V_{AC}, max load, T_{AMB} = 25 °C, transformer side



10 EMI measurements

A pre-compliance test against the EN55022 (Class B) European normative with average detector was performed using an EMC analyzer and a LISN. The results are shown in the following figures.

Figure 47. Average measurements @ 115 V_{AC}, full load, T_{AMB} = 25 °C

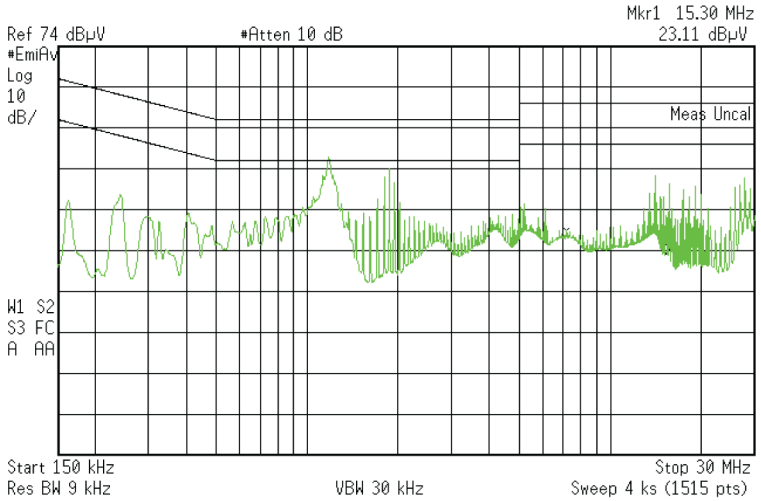
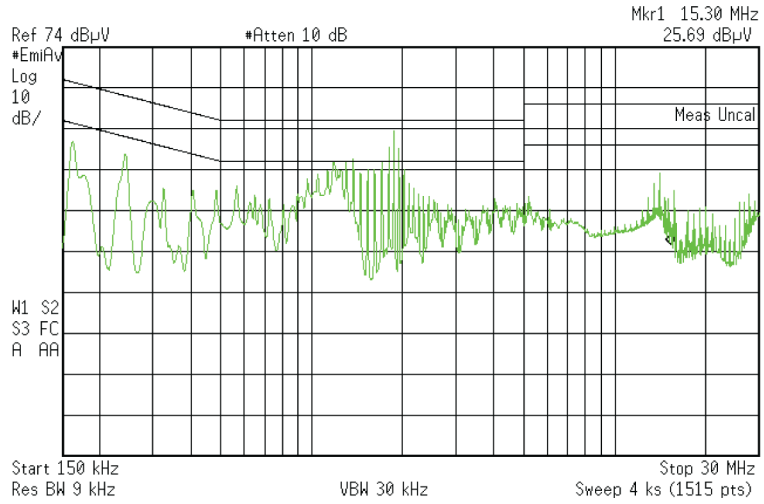


Figure 48. Average measurements @ 230 V_{AC}, full load, T_{AMB} = 25 °C



11 Immunity tests

The board has been submitted to immunity tests according IEC61000 and the results are presented in the following sections.

The results are classified according the criterions reported in the standard and listed in the following table:

Table 9. Classification of the tests

A	Normal performance
B	Temporary degradation or loss of function or performance, with automatic return to normal operation
C	Temporary degradation or loss of function with external intervention to re-cover normal operation
D	Degradation or loss of function, need substitution of damaged components to recover normal operation

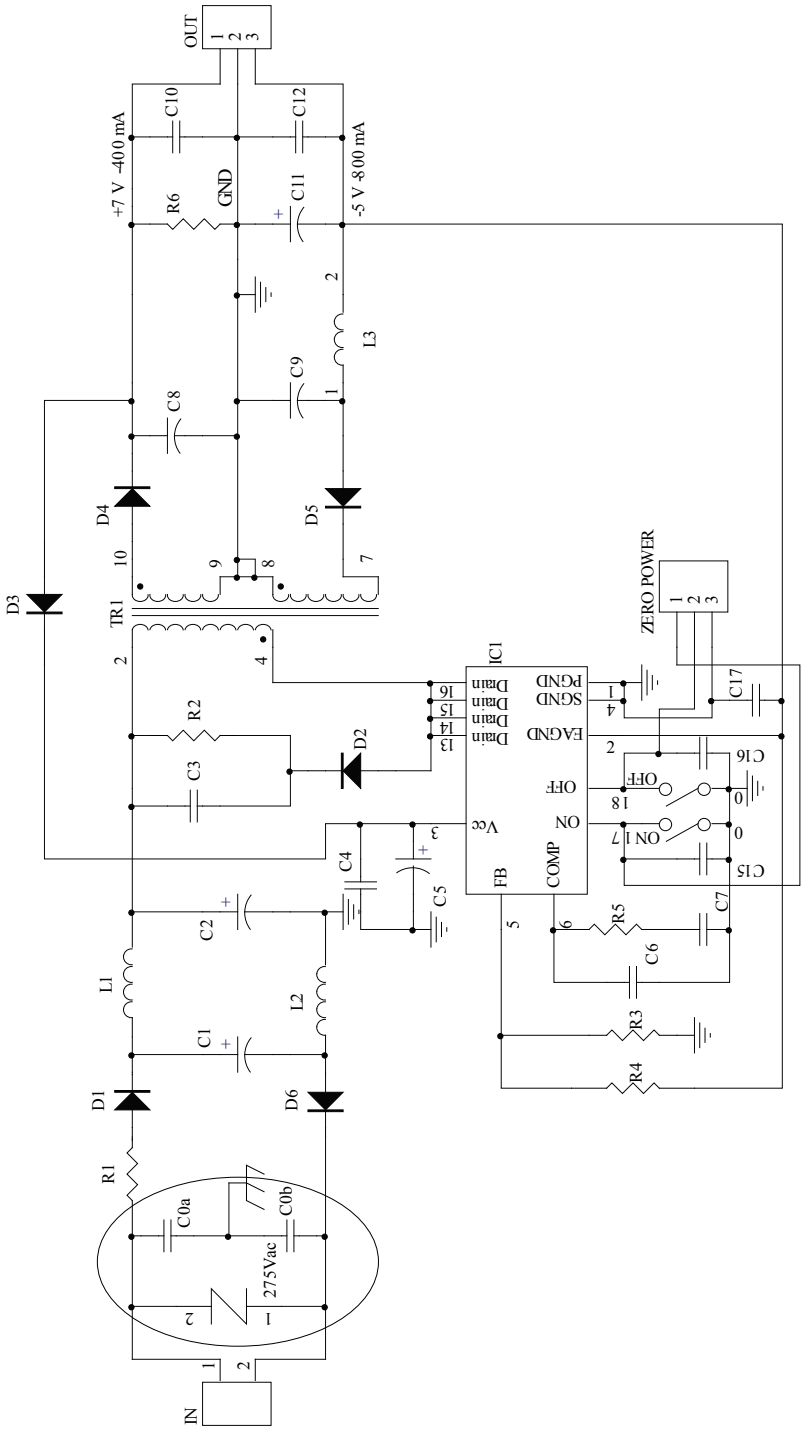
11.1 SURGE immunity test (IEC 61000-4-5)

The surge test conditions are as below:

- Repetition rate: 1 minute (5 positive and 5 negative surges)
- Applied to: input lines vs. EARTH – Common Mode
- Applied to: both input line (L vs. N) – Differential Mode
- Reference plane connected to Protected Earth according to the normative

In order to pass the test, the STEVAL-ISA174V1 schematic has been modified with the additions highlighted in the following figure, consisting of an input filter made up of a 275 V_{AC} varistor and two 2.2 nF Y1 capacitor in series. The common point of the capacitors is the Protected Earth, which during the tests is to be connected to the reference plane, according to the normative recommendation.

Figure 49. **STEVAL-ISA174V1 surge-improved schematic**



The input voltage has been set to 230 V_{AC} and the output at 10% of full load, proper operation has been checked through a current probe connected on the output. The test results are listed in the following tables.

Table 10. **Common mode surge test results**

Noise injection	Surge level	Polarity	Result	Criterion
L vs. PE	2 kV	Positive	PASS	A

Noise injection	Surge level	Polarity	Result	Criterion
N vs. PE	2 kV	Positive	PASS	A
L vs. PE	2 kV	Negative	PASS	A
N vs. PE	2 kV	Negative	PASS	A

Table 11. Differential mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. N	2 kV	Positive	PASS	A
L vs. N	2 kV	Negative	PASS	A

Performed tests show that the tested board is able to withstand the lightning disturbances applied to input line in Common Mode and Differential Mode for each severity level.

11.2 ESD immunity test (IEC 61000-4-2)

The test conditions are as below:

- Contact discharge and Air discharge methods
- Discharge circuit: 150 pF / 330 ohm
- Polarity: positive / negative

The setting of Figure 49. STEVAL-ISA174V1 surge-improved schematic allows ESD to be passed as well . The key point is the filtering of the sensitive pins ON, OFF and EAGND through 220 pF ceramic capacitors to SGND. The purpose of the input filter (varistor + series of the 2.2 nF Y1 capacitors C0a and C0b) is only to provide the Protected Earth (common point of the capacitors) for the correct coupling of the ESD signal according to the IEC 61000-4-2 normative.

The input voltage has been set to 230 V_{AC} and the output at 10% of full load, proper operation has been checked through a current probe connected on the output. The test results are listed in the following tables.

Table 12. ESD contact discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
L vs. PE	10 kV	Positive	PASS	A
L vs. PE	10 kV	Negative	PASS	A
N vs. PE	10 kV	Positive	PASS	A
N vs. PE	10 kV	Negative	PASS	A

Table 13. ESD air discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
Horizontal coupling plane	20 kV	Positive	PASS	A
Horizontal coupling plane	20 kV	Negative	PASS	A
Vertical coupling plane	20 kV	Positive	PASS	A
Vertical coupling plane	20 kV	Negative	PASS	A

11.3 Burst immunity test (IEC 61000-4-4)

The test conditions are as below:

- Polarity: positive/negative
- Burst duration: 15 ms ± 20 % at 5 kHz
- Burst period: 300 ms ± 20 %
- Duration time: 1 minute
- Applied to: AC lines through integrated capacitive coupling clamp

The tests can be passed with the original setting (Section 3 Schematic diagram), the key point is the filtering of the sensitive pins ON, OFF and EAGND through 220 pF ceramic capacitors to SGND . The input voltage has been set to 230 V_{AC} and the output at 10% of full load, proper operation has been checked through a current probe connected on the output.

The test results are listed in the following table.

Table 14. Burst test results

Noise injection	Burst level	Polarity	Result	Criterion
L / PE	8 kV	Positive	PASS	B
N / PE	8 kV	Positive	PASS	B
L / N	8 kV	Positive	PASS	B
L / PE	8 kV	Negative	PASS	B
N / PE	8 kV	Negative	PASS	B
L / N	8 kV	Negative	PASS	B

11.4 Summary and conclusion

In the following Figure and Table, the EMC board behavior with the above mentioned filters is summarized.

Figure 50. **STEVAL-ISA174V1 filtering to pass EMC tests**

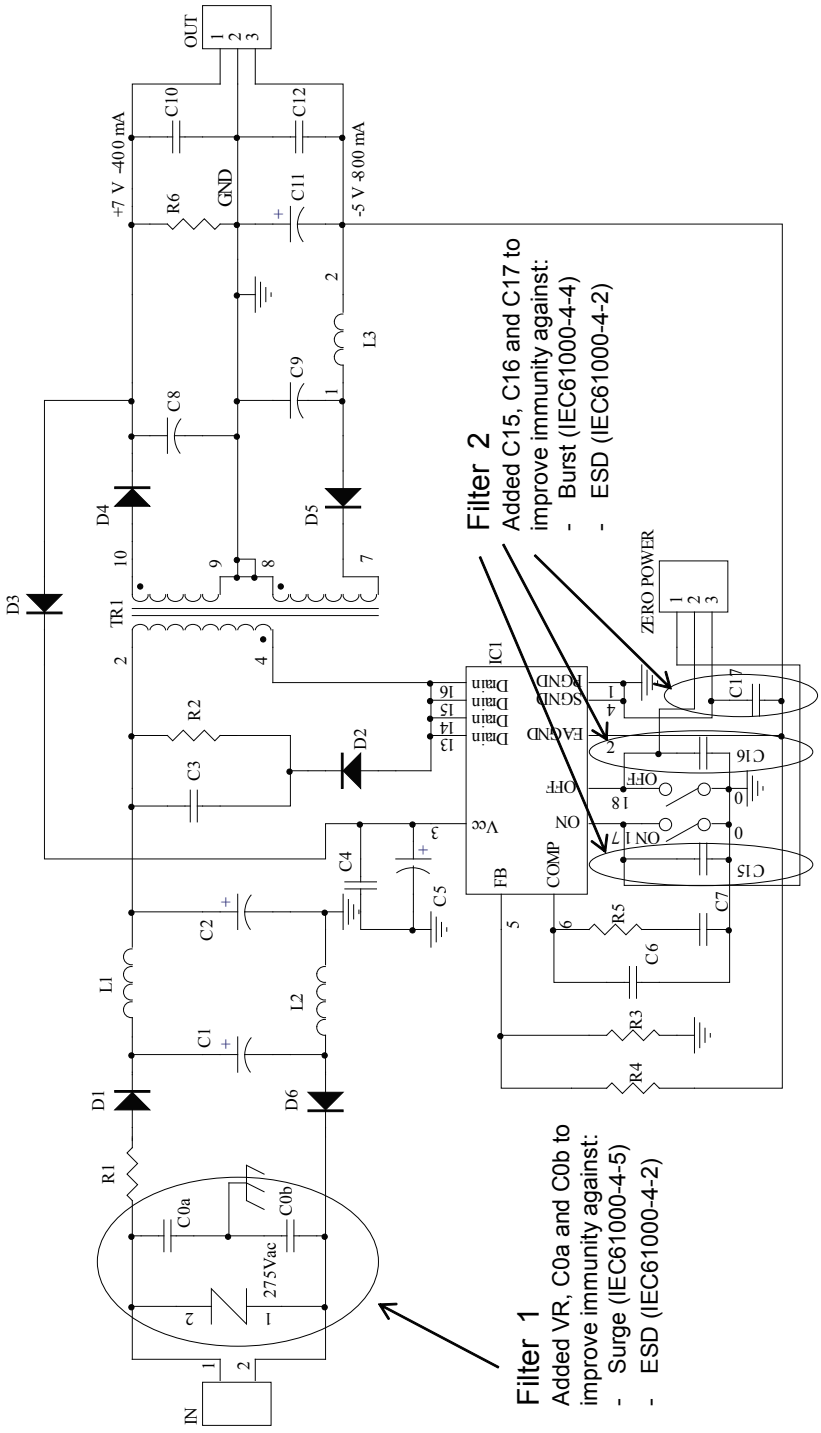


Table 15. **EMC summary**

	VIPer0P + Filter 1 + Filter 2		
EN/IEC 61000-4-2 (Applicative ESD)	air discharge	contact discharge	
	20 kV (1)	10 kV (1)	10 kV (1)

	VIPer0P + Filter 1 + Filter 2			
EN/IEC 61000-4-4 (BURST simulation)	common mode		differential mode	
	6 kV (1)	8 kV (2)	6 kV (1)	8 kV (2)
EN/IEC 61000-4-5 (SURGE simulation)	common mode		differential mode	
	2 kV (1)		2 kV (1)	

1. *criterion A: normal performance.*
2. *criterion B: temporary degradation or loss of function or performance, with automatic return to normal operation.*

Note: criterion C: temporary degradation or loss of function, with external intervention to re-cover normal operation.
criterion D: degradation or loss of function, substitution of damaged components is needed to recover normal operation.

12 Board layout

Figure 51. **Board layout - complete**

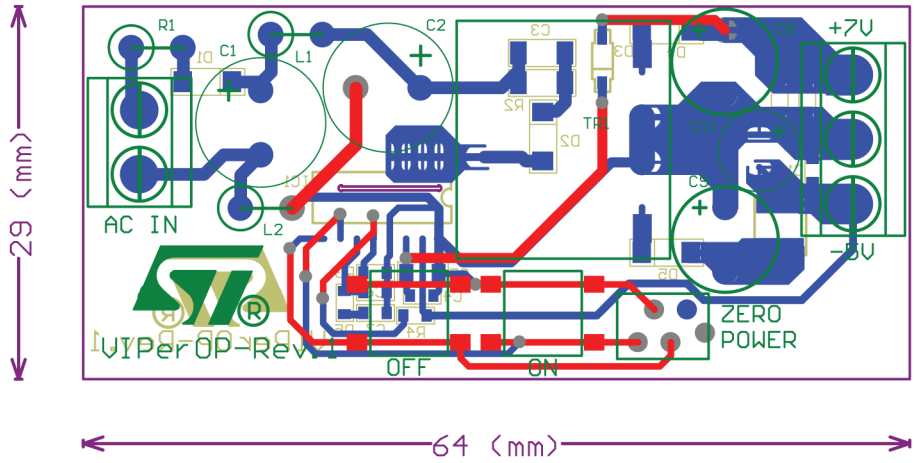


Figure 52. **Board layout - top layer + top overlay**

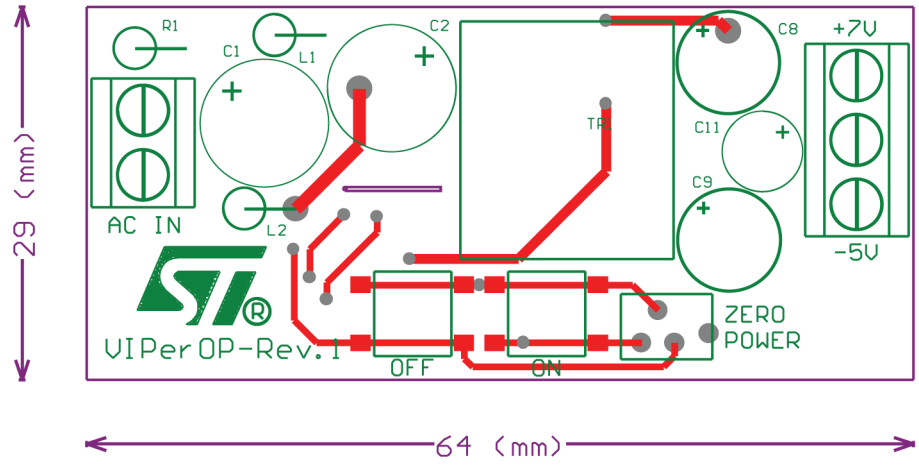
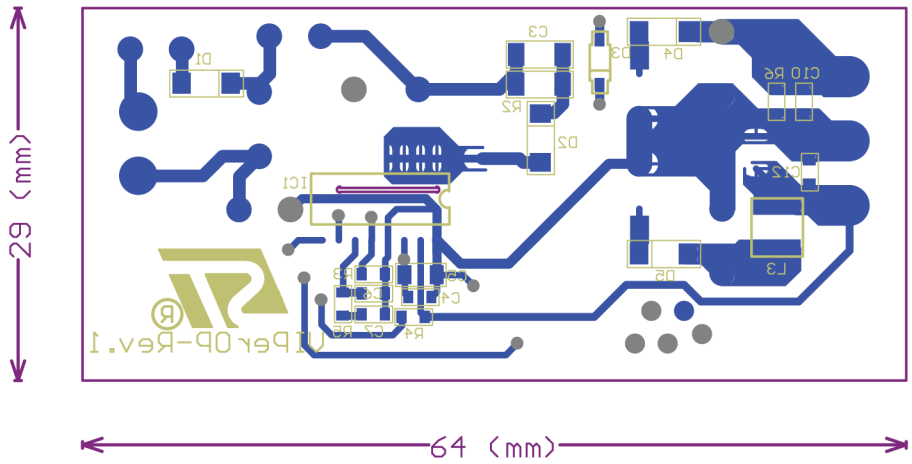


Figure 53. **Board layout - bottom layer + top overlay**



13 Conclusions

The STEVAL-ISA174V1 two-output converter set in flyback non-isolated topology, demonstrates that the VIPer0P facilitates the design of a non-isolated converter compliant with the most stringent energy regulations, with relatively few external components. The STEVAL-ISA174V1 in fact consumes less than 10 mW at 230 V_{AC} mains under no load condition and even less than 5 mW in the special ZPM idle state that can be optionally managed by a microcontroller. The 800 V avalanche rugged Power MOSFET and the embedded protections add reliability to the power converter, making VIPer0P the ideal choice when both robustness and energy saving performance are required.

14 Appendix A - Test equipment and measurement of efficiency and low load performance

The converter input power was measured using a wattmeter. The wattmeter simultaneously measures the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). Being a digital instrument, it samples the current and voltage at 20 kHz frequency (or higher, depending on the instrument) and converts them into digital forms. Digital samples are then multiplied to give the instantaneous measured power. The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 s typ.).

Figure 54. Connections of the UUT to the wattmeter for power measurements shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram. An electronic load is connected to the output of the power converter (UUT), allowing the setting and measurement of the converter load current, while the output voltage is measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously mentioned, and the input power, measured by the wattmeter, represents the converter efficiency.

The measurements were taken under different input/output conditions set on the AC source and on the electronic load.

Measuring input power notes:

With reference to Figure 54. Connections of the UUT to the wattmeter for power measurements , the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT. If the switch of Figure 54. Connections of the UUT to the wattmeter for power measurements is in position 1 (see the simplified schematic in Figure 55. Switch in position 1 - setting for standby measurements) this voltage drop causes an input measured voltage higher than the input voltage at the UUT input which, of course, affects the measured power.

The voltage drop is generally negligible if the UUT input current is low (e.g., when we are measuring the input power of UUT under light load condition). In case of high UUT input current, the voltage drop can be significant (compared to the UUT real input voltage); if this is the case, the switch in Figure 54. Connections of the UUT to the wattmeter for power measurements can be set to position 2 (see simplified schematic in Figure 56. Switch in position 2 - setting for efficiency measurements) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

The voltage across the voltmeter causes a leakage current inside the voltmeter itself (which is not ideal and so doesn't have an infinite input resistance). If the switch in Figure 54. Connections of the UUT to the wattmeter for power measurements is in position 2 the voltmeter leakage current is measured by the ammeter together with the UUT input current, causing a measurement error. The error is negligible when the UUT input current is much higher than the voltmeter leakage. If not, it may be preferable to set the switch in Figure 54. Connections of the UUT to the wattmeter for power measurements to position 1. If you are not certain which measurement scheme less affects the result, you can try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT should be operated at 100% of the nameplate output current output for at least 30 minutes (warm up period) immediately prior to conducting efficiency measurements. After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% of the maximum observed value, the UUT is considered stable and the measurements can be recorded at the end of the 5 minute period. If the AC input power is not stable over a 5 minute period, the average power or accumulated energy is measured over time for both AC input and DC output. Some wattmeter models allow the integration of the measured input power over a time interval and then measure the energy absorbed by the UUT during the integration time. Dividing by this very integration time gives the calculated average input power.

Figure 54. **Connections of the UUT to the wattmeter for power measurements**

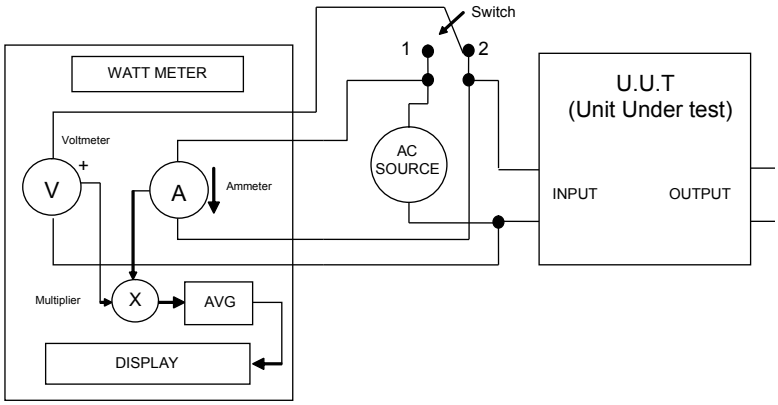


Figure 55. **Switch in position 1 - setting for standby measurements**

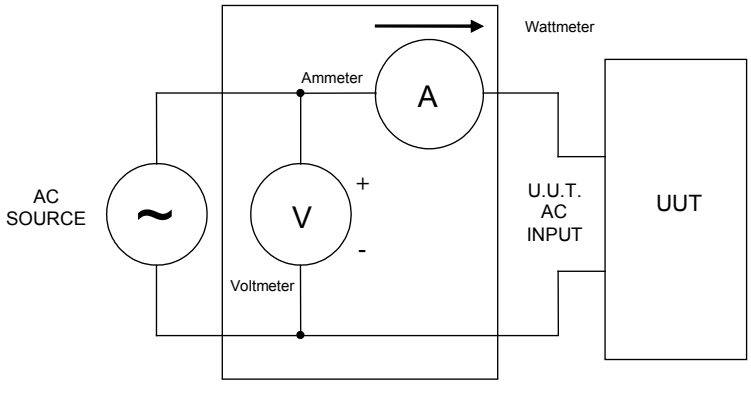
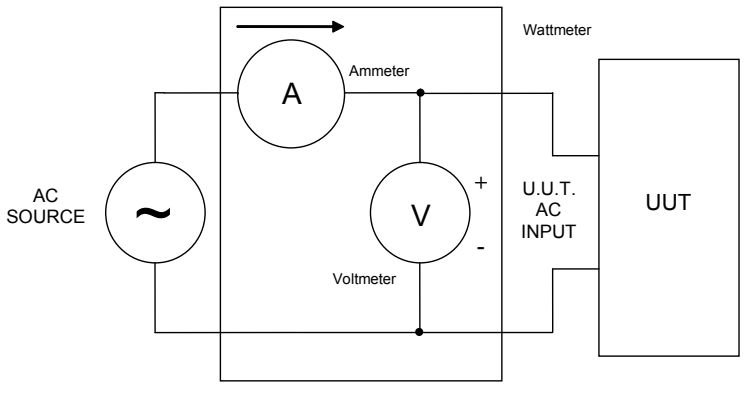


Figure 56. **Switch in position 2 - setting for efficiency measurements**



15 References

1. VIPER0P - datasheet
2. IEC 61000-4-2
3. IEC 61000-4-4
4. IEC 61000-4-5

Revision history

Table 16. **Document revision history**

Date	Version	Changes
14-Apr-2016	1	Initial release.
22-Feb-2018	2	Updated Figure 5. STEVAL-ISA174V1 schematic diagram

Contents

List of tables

List of figures

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved