SPC58xx hardware design guideline

Introduction

This application note complements the information in the device datasheets (see Appendix A: Reference documents) describing useful requirements for a hardware implementation of the development board features such as power supply, reset control, clock management, boot mode setting, debug management, and I/Os settings.

Note: The EMC performance of applications based on microcontrollers is dependent on a number of factors that are outside the control of STMicroelectronics. These factors include but are not limited to industrial design, mechanical design, printed circuit board design and layout, components, connectors, and cables. In no way, this document implies a guarantee of the performances in the final application. Careful consideration must be made when designing any application to ensure the necessary level of EMC. An evaluation with test and measurements is always recommended as soon as possible during the application development process.

This application note applies to the devices listed in the following Appendix A: Reference documents.

Table 1. Device summary

Reference	Part number
SPC582Bx	SPC582B50x, SPC582B54x, and SPC582B60x
SPC584Bx	SPC584B60x, SPC584B64x, and SPC584B70x
SPC584Cx, SPC58ECx	SPC584C70x, SPC584C74x, SPC584C80x, SPC58EC70x, SPC58EC74x, and SPC58EC80x
SPC584Gx, SPC58NGx, SPC58EGx	SPC584G80x, SPC584G84x, SPC58EG80x, SPC58EG84x, SPC58NG80x, and SPC58NG84x
SPC58EHx, SPC58NHx	SPC58EH92x, SPC58EH90x, SPC58EH84x, SPC58NH92x, SPC58NH90x, and SPC58NH84x
SPC58EEx, SPC58NEx	SPC58EE80x, SPC58NE80x, SPC58EE84x, and SPC58NE84x
SPC584Nx, SPC58ENx, SPC58NNx	SPC584N80x, SPC58EN80x, SPC58EN84x, and SPC58NN84x

1 Preface

The SPC58xx devices belong to a wide family of automotive microcontroller products, which offers the needed scalability to implement platform approaches and delivers the performance and features required by increasing sophisticated body applications.

The sections of this document briefly describe certain device features without describing the device blocks in detail. For a detailed description of these features, refer to the device datasheets, reference manuals, and errata sheets (see Appendix A: Reference documents).

These devices are members of a microcontroller family based on power architecture technology that targets automotive applications like:

- Automotive powertrain controllers for six to eight cylinder gasoline, diesel engines
- Advanced combustion systems as well as high-end hybrid and transmission control
- Integrated chassis control, high-end steering, and braking
- In general, any safety critical application requiring a very high level of safety integrity
- Vehicle body
- Gateway applications.

Inside this family, the device is available only as single core, both single and symmetrical dual/triple core and operates at speeds of up to 200 MHz enabling the customer to adjust the performance and consumption to the application needs.

All the electrical characteristics of the SPC58xx, including the absolute maximum ratings and recommended operating conditions (such as threshold voltages, maximum and minimum supply voltages), as well as the package mechanical drawings and pin assignments, can be found in the device datasheets (see Appendix A: Reference documents).

Note: This document provides target electrical specifications, based on previous designs, design simulations, or initial evaluation. Target electrical specification may not be guaranteed at this early stage of the product life cycle, however they are built to provide enough margin, ensuring production silicon meets customer requirements.

Finalized specifications will be published after completion of device characterization and device qualifications.

2 Power supplies

2.1 Introduction

The SPC58xx family devices require a 3.3 V or 5.0 V operating voltage supply (high voltage).

Up to seven different independent voltage regulators can provide the 1.2 V digital power supply in the SPC58xx. Depending on the specific SPC58xx device, there can be the following different kinds and numbers of available regulators.

The Table 2 shows, for each device, the possible regulator configuration that can be used.

Table 2. Power management regulators

Device	External regulator with (1)	Internal regulator with external ballast	Internal regulator with internal ballast	Auxiliary regulator (2)	Clamp regulator (2)	Internal standby regulator (3)	Internal SMPS regulator
SPC58EHx, SPC58NHx	X	X	–	X	X	X	-
SPC584Gx, SPC58NGx, SPC58EGx	–	X	–	X	X	X	–
SPC584Cx, SPC58ECx	–	X	X (4)	X	X	X	–
SPC584Bx	–	X(4)	X	X	X	X	–
SPC582Bx	–	–	X	–	–	X	–
SPC58EEx, SPC58NEx	X	X(5)	-	X	X	X (5)	X (6)(7)
SPC584Nx, SPC58ENx, SPC58NNx	X	-	-		X	-(8)	X(6)

1. *The application can select between the internal or external regulator mode, by controlling the EXTREG_SEL pin of the device. If EXTREG_SEL is connected to VDD_HV_IO_MAIN, the external regulator mode is selected.*
2. *In external regulator mode, the auxiliary and clamp regulators can be optionally enabled, to support the compensation of overshoots and undershoots in the supply. In internal regulator mode, the auxiliary and clamp regulators are always active.*
3. *Standby regulator is automatically activated when the device enters standby mode. Except for the SPC58EHx, SPC58NHx device, the standby mode is not supported if the device operates in external regulator mode. Emulation device calibration and trace features are not supported in standby mode.*
4. *This option is supported only upon commercial and technical agreement with ST.*
5. *Except eLQFP176*
6. *Parts with SMPS enabled can only be used in this mode and EXTREG_SEL has to be set to VSS.*
7. *Except LFBGA292*
8. *Standby mode is not present on the SPC584Nx, SPC58ENx, SPC58NNx device.*

The supported regulators are:

- External regulator
  - External VDD_LV supply is provided from outside and no internal regulator is required.

- Internal regulator–HPREG or SMPS
  - An internal high power voltage regulator (HPREG) used during normal operations using
  - An external NPN bipolar as the ballast device
  - An internal ballast transistor (DREG)
  - An internal switching mode power supply (SMPS) regulator using external PMOS, NMOS, and inductance.
- Low power regulator - LPREG
  - When the device is in standby, the supply is provided by the internal LPREG and the HPREG/DREG is off, with a reduced maximum driving capability.
- Auxiliary and clamp regulators
  - For fast current transients, auxiliary and clamp regulators (not available on SPC582Bx devices) improve the load regulation by compensating voltage overshoots and under-shoots. They operate with the internal or external regulator.

Note: Please refer to the device data sheet for the electrical characteristics of the regulators, the monitors, and the list of external components required.

The Table 3 shows the supply signals.

Table 3. Device power management controller external signals

Signal name	Reference	Description
VDD_HV_ADR_S	Reference	SAR ADC reference high input
VDD_HV_ADV	Supply	ADC supply voltage
VDD_HV_FLA	Supply	Flash memory supply
VDD_HV_IO_MAIN	Supply	Main I/O voltage supply
VDD_HV_OSC	Supply	Oscillator voltage supply
VDD_HV_EMMC	Supply	EMMC voltage supply(1)
VDD_HV_IO_ETH	Supply	Ethernet I/O segment voltage supply(2)
VDD_HV_IO_FLEX	Supply	FlexRay/Ethernet I/O segment voltage supply(3)
VDD_LV(4)	Supply	Core logic voltage supply
VDD_HV_IO_BD	Supply	Buddy device I/O voltage supply(5)
VDD_LV_BD	Supply	Buddy device core logic low voltage supply (5)
VDD_HV_IO_JTAG	Supply	JTAG I/O voltage supply (5)
VDD_HV_ADR_D	Reference	Sigma-delta ADC reference high input (5)
VSS	Ground	Ground supply for the device / I/O. This is covering both VSS_LV and VSS_HV in the case of the exposed pad device.
VSS_HV_ADR_S	Reference	SAR ADC reference low input
VSS_HV_ADV	Supply	Analog ground supply
VSS_HV_ADR_D	Supply	Sigma-delta ADC reference low input (5)

1. *Present only on SPC58EHx, SPC58NHx device.*
2. *Present only SPC58EHx, SPC58NHx device, and SPC584Bx device.*
3. *Present on all SPC58xx family but SPC58EHx, SPC58NHx device, and SPC584Bx device.*
4. *The external capacitors on the VDD_LV pins shall be interconnected so to ensure the stability of the internal regulator.*
5. *Present only on SPC58EEx, SPC58NEx, SPC584Nx, SPC58ENx, SPC58NNx device.*

Note: VDD_HV_IO_ETH0, VDD_HV_IO_ETH1 on SPC58EHx, SPC58NHx device, and VDD_HV_IO_ETH on SPC584Bx device.

The internal regulators are supplied by VDD_HV_IO_MAIN supply and are used to generate VDD_LV supply.

External capacitors connected between the VDD_LV/VSS_LV pin pairs ensure the stability of the internal 1.2 V HPREG and LPREG regulators.

For the values of capacitances shown in the following figures, CE, CFLA, CBV, CADC, and CHVN, refer to the device datasheet (see Appendix A: Reference documents).

According to the chosen regulator configuration, the following device circuitry has to be used.

Note: The BCTRL pin shall be left floating in external regulator mode and internal regulator with internal ballast mode.

Note: It is forbidden to connect the BCTRL pin at VDD.

Figure 1. External regulator

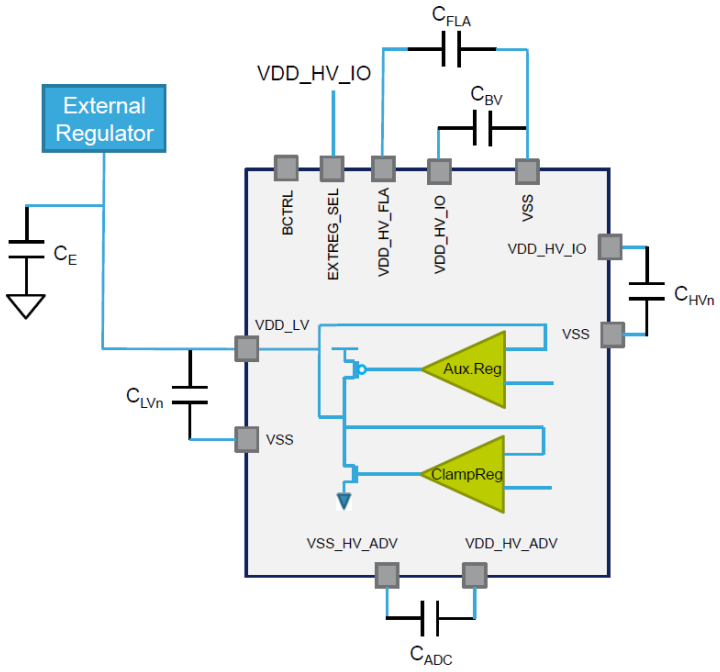


Figure 2. Internal regulator with external ballast mode

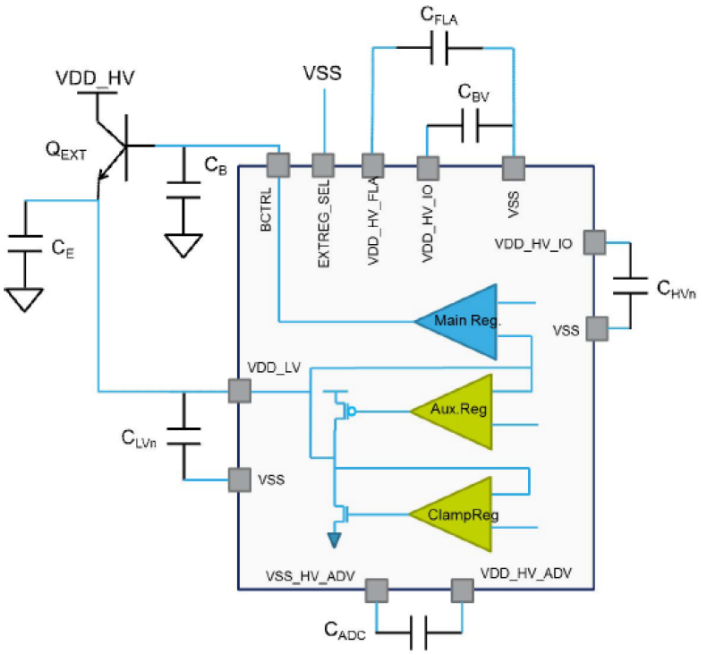


Figure 3. **Internal regulator with internal ballast mode**

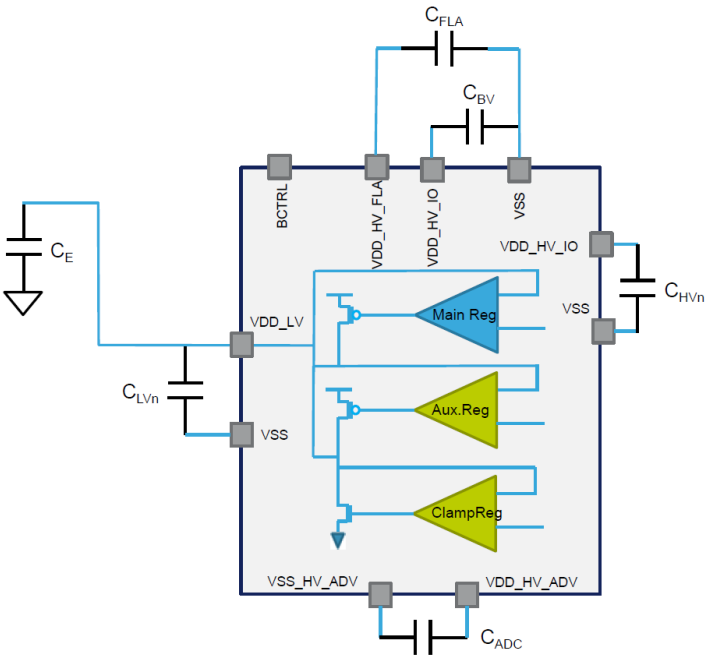


Figure 4. **Standby regulator with external ballast mode**

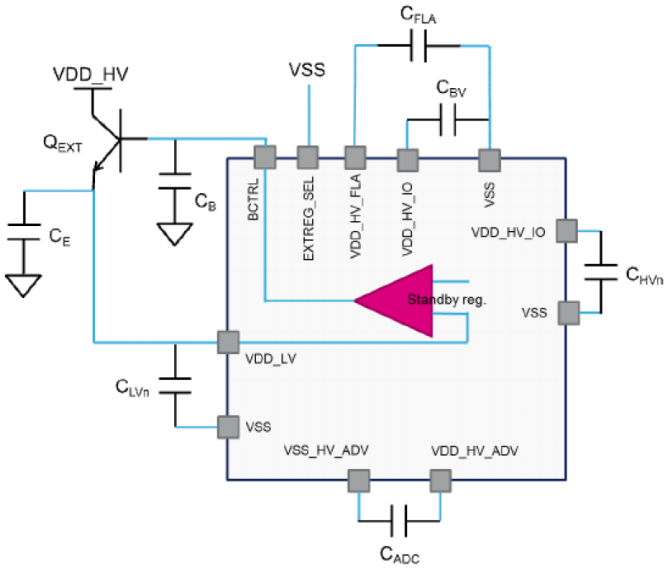


Figure 5. **Standby regulator with internal ballast mode**

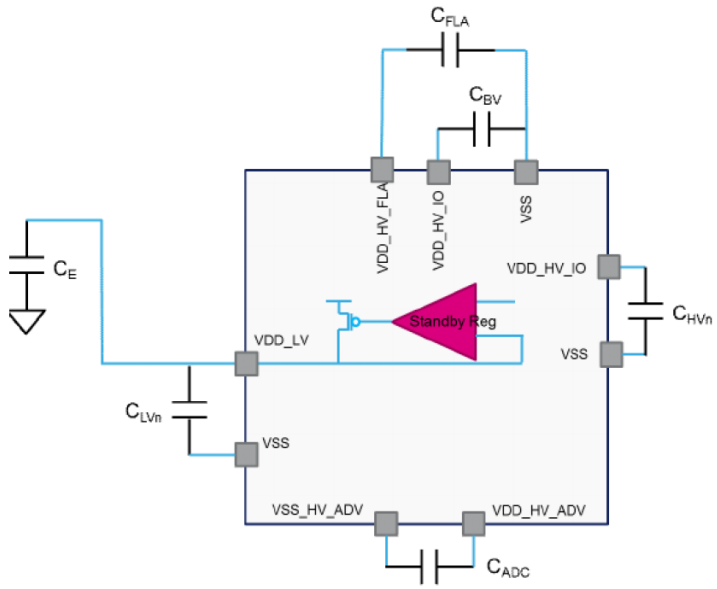
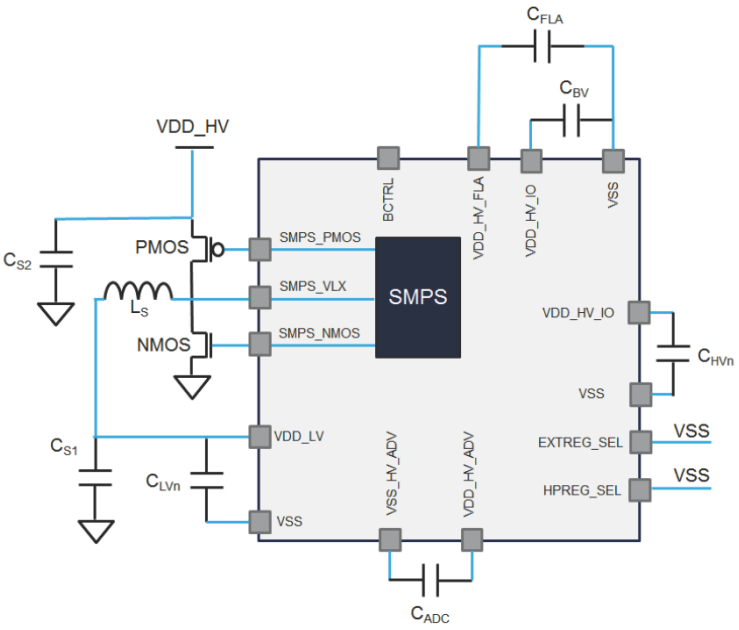


Figure 6. **SMPS regulator mode**



For a detailed list of supply-related pins for the specific device and package, please refer to the voltage supply pins section in the device reference manual (see Appendix A: Reference documents).

2.2 Power supply scheme

The circuit is powered by a stabilized power supply VDD_HV. All the supply pins related to the high voltage and low voltage must be connected to a supply with external decoupling capacitors. Regarding the minimum recommended configuration and the values of the capacitors see the device datasheets (see Appendix A: Reference documents).

Hardware designers must pay particular attention to place the decoupling capacitors beside the respective pins and limit the serial inductance of the board to less than 5 nH.

Place only one CBV capacitance for all the VDD_HV pins.

Caution: Regarding the constraints and relationships for the different power domains, see the device datasheet the section “Power domains and power up/down sequencing” (see Appendix A: Reference documents).

The Table 4 gives an example for a SPC58NHx device.

Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting 'ok'. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Table 4. Device supply relation during power-up/down sequence for SPC58ENHx, SPC58NHx

Supply 1	Supply 2						
	V_{DD_LV}	$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO\_ETH0}$	$V_{DD\_HV\_IO\_ETH1}$	$V_{DD\_HV\_IO\_EMMC}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$
V_{DD_LV}		Ok	Ok	Ok	Ok	Ok	Ok
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_OSC}$	Ok		Ok	Ok	Ok	Ok	Ok
$V_{DD\_HV\_IO\_ETH0}$	Ok	Not allowed		Ok	Ok	Ok	Ok
$V_{DD\_HV\_IO\_ETH1}$	Ok	Not allowed	Ok		Ok	Ok	Ok
$V_{DD\_HV\_IO\_EMMC}$	Ok	Not allowed	Ok	Ok		Ok	Ok
$V_{DD\_HV\_ADV}$	Ok	Not allowed	Ok	Ok	Not allowed		Ok
$V_{DD\_HV\_ADR}$	Ok	Not allowed	Ok	Ok	Not allowed	Not allowed	

1. *V_{DD_LV} can be higher than V_{DD_HV} supplies only during power-up/down transient ramps, in the case of an external LV regulator and if the V_{DD_HV} supply voltage level is lower than the V_{DD_LV} allowed max operating condition.*
2. *The application shall grant that these supplies are always at the same voltage level.*

Table 5. Device supply relation during power-up/power-down sequence for SPC584Nx, SPC58ENx, SPC58NNx

Supply1	Supply2							
	V_{DD_LV}	$V_{DD\_HV\_IO\_FLEX}$	$V_{DD\_HV\_IO\_JTAG}$	$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$	$V_{DD\_LV\_BD}$	$V_{DD\_HV\_BD}$
V_{DD_LV}		Ok	Ok	Ok	Ok	Ok	Ok	Ok
$V_{DD\_HV\_IO\_FLEX}$	Ok		Ok	Not allowed	Ok	Ok	Ok	Ok
$V_{DD\_HV\_IO\_JTAG}$	Ok	Ok		Not allowed	Ok	Ok	Ok	Ok
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$	Ok	Ok	Ok		Ok	Ok	Ok	Ok
$V_{DD\_HV\_ADV}$	Ok	Ok	Ok	Not allowed		Ok	Ok	Ok
$V_{DD\_HV\_ADR}$	Ok	Ok	Ok	Not allowed	Not allowed		Ok	Ok
$V_{DD\_LV\_BD}$	Ok	Ok	Ok	Ok	Ok	Ok		Ok
$V_{DD\_HV\_BD}$	Ok	Ok	Ok	Ok	Ok	Ok	Ok	

1. *V_{DD_LV} can be higher than V_{DD_HV} supplies only during power-up/down transient ramps, in the case of an external LV regulator and if the V_{DD_HV} supply voltage level is lower than the V_{DD_LV} allowed max operating condition.*

2.2.1 Recommended power-up sequence

The power-up reset cell of a microcontroller ensures that the microcontroller is put into a well-defined state only in case that a complete power-on cycle is performed.

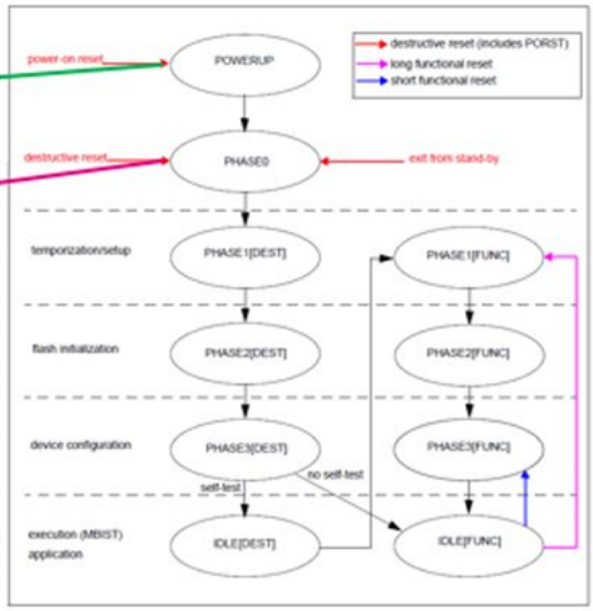
In fact, most of the modules of the device are reset with a destructive reset. But the following blocks are 'always-on' and can be reinitialized only with a power-on reset event:

- IRCOSC
- PMC = power management unit controller
- FUSE
- MC_RGM = reset generation module, managing the reset-exit sequence.

The Figure 7 shows the RGM reset phases and the status of each block across them.

Figure 7. Modules status during reset phases

Module	PHASE								
	P0	P1 [DEST]	P2 [DEST]	P3 [DEST]	IDLE [DEST]	P1 [FUNC]	P2 [FUNC]	P3 [FUNC]	IDLE [FUNC]
IRCOSC	ON	ON	ON	ON	ON	ON	ON	ON	ON
PMC	ON	ON	ON	ON	ON	ON	ON	ON	ON
FUSE	ON	ON	ON	ON	ON	ON	ON	ON	ON
MC_RGM	ON[1]	ON	ON	ON	ON	ON	ON	ON	ON
System watch dog	RESET	RESET	ON	RESET	IDLE	RESET	ON	RESET	ON
Flash module	RESET	RESET	ON	ON	IDLE	RESET	ON	ON	ON
XOSC	RESET	RESET	RESET	ON	ON	ON	ON	ON	ON
DEVICE CONFIG	RESET	RESET	RESET	LOAD	HOLD	HOLD	HOLD	HOLD	HOLD
SSCM	RESET	RESET	RESET	ON	ON	RESET	RESET	ON	ON
FCCU	RESET	RESET	CON FIG	CON FIG	IDLE	RESET/ ON	CONFIG /ON	CON FIG/ON	ON
STCU	RESET	RESET	CON FIG	CON FIG	ON	RESET/ IDLE	CONFIG /IDLE	CON FIG/ IDLE	ON/ IDLE
MEMU	RESET	RESET	ON	ON	IDLE	RESET/ ON	ON	ON	ON
PASS	RESET	ON	ON	ON	ON	ON	ON	ON	ON
HSM	RESET	RESET	RESET	RESET	IDLE	RESET	RESET	RESET	ON
Boot CPU	RESET	RESET	RESET	RESET	IDLE	RESET	RESET	RESET	ON
PIT	RESET	RESET	RESET	RESET	IDLE	IDLE/ON	IDLE /ON	IDLE/ ON	IDLE/ ON
Other modules including cores	RESET	RESET	RESET	RESET	IDLE	RESET	RESET	RESET	ON
—	—	—	—	—	—	—	—	Short functional reset	—
—	—	—				functional reset			—
—	destructive reset								—



In some specific scenarios, if previous 'always-on' blocks are not reset, the device could hang in an undefined state. This highlight shows that only the POR cycle guarantees a full device recovery.

2.2.1.1 *POR versus VDD_HV/LV thresholds*

The recommended POR sequence is strictly dependent on the control of the maximum residual voltage level on VDD_HV/LV supply domains, in particular in a case of brown-out management on which the MCU is powered-down/up in a very short time (less than 1 ms).

The following two thresholds need to be both fulfilled at the same time, in order to have a clean POR sequence:

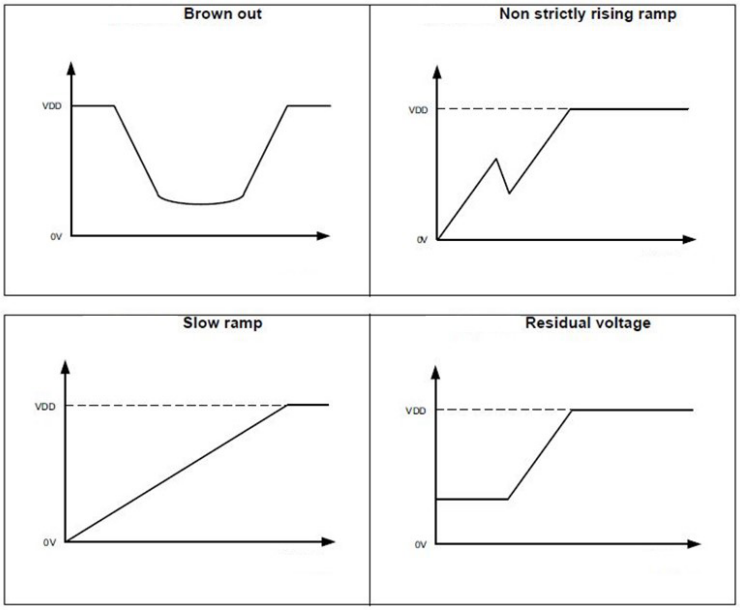
- VDD_HV < 1.5 V
- VDD_LV < 0.4 V

2.2.1.2 *Failing scenarios: Brown-out example*

In a typical real implementation, it is recommended to use an external supervisor module (system basis chip, SBC) to be able to issue a POR cycle and to control the minimum voltage levels to supply.

When SBC drives an MCU power supply, the conditions in the Figure 8 should be avoided.

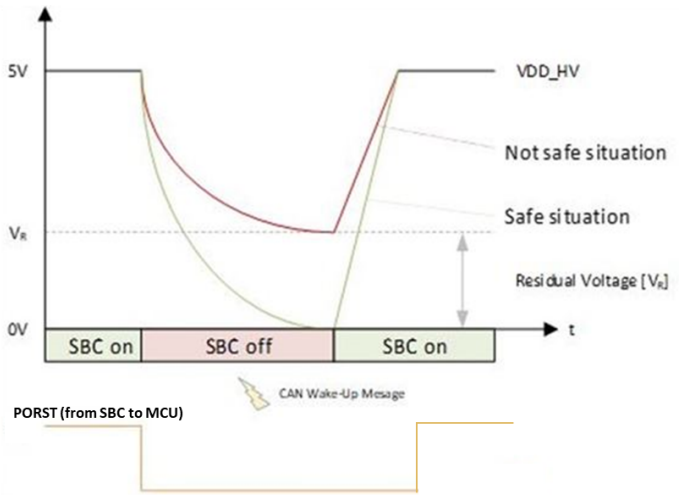
Figure 8. Conditions to avoid during MCU power-up



The specific case of the brown-out scenario happens when the MCU is power-off and powered-on so quickly that the VDD_HV and VDD_LV maintain a residual voltage instead of falling under the previously mentioned VDD_HV/LV thresholds.

In such case, strongly depending on process, temperature and event duration, a marginality can occur and the device stays in reset.

Figure 9. Failure condition during brown-out condition



In the showed example, the SBC goes off/on quickly avoiding the VDD_HV to fall to zero (red wave in the picture) and this residual voltage can prevent the VDD_LV from falling below the critical threshold causing a stuck in the MCU reset sequence.

2.2.1.3 How SBC should monitor the MCU

SBC usually monitors the MCU status via a watchdog, which takes some actions in case the MCU does not provide the ack (a SPI signal, for example) before the timeout expires.

The safety manual (SM) of each device usually reports about the way that the external device monitors the MCU misbehavior.

For example, referring to the SPC58xC device, the safety mechanism entry SM_MCU_6_3 reports: an external watchdog must detect and handle a microcontroller that cannot execute the safety function in case of wrong behavior. That is the microcontroller does not trigger the external watchdog in the expected time.

So, the external supervisor of the operations must provide a watchdog to cover common-cause failures of the device for ASIL x applications.

Because the explained brown-out error condition let system remain in a safe context, it is recommended to use the same watchdog to issue a clean POR cycle to ensure a proper restart of the application also in case of unexpected behavior of the device induced by a corner case condition in the supplies.

Other SBC strategies that could be adopted to avoid this failing scenario are:

- WD failure counter in combination with power supply switch-off
- Delayed power-on
- Fast discharge

2.3 Current consumption and voltage regulator

In order to select a suitable external voltage regulator and design a supply circuit, the designer of the application must consider:

1. The maximum consumption in steady state
2. The maximum inrush current during device startup

Note: In-rush current heavily depends on the LBIST/MBIST execution during the power-up sequence. It also grows depending on the quantity of used memory and the clock frequency.

The maximum consumption in steady state depends on the frequency of the CPU, the usage of the peripheral and the current drawn by the outputs. It can be estimated by referring to the device datasheet (see Appendix A: Reference documents).

2.4 Layout recommendations

The basic rule in the decoupling layout is to minimize the inductance associated with the loop device pin/ decoupling capacitor and the total inductance of the connection to the power supply.

All the supply connections, including pads, tracks, and vias, must have impedance as low as possible (less than 5 nH). This is typically achieved by using copper areas, rather than tracks, and a dedicated power supply plane is preferable in multilayer PCBs.

Moreover, it is recommended to use both low equivalent series resistors (ESR) and low equivalent series inductance (ESL) capacitors.

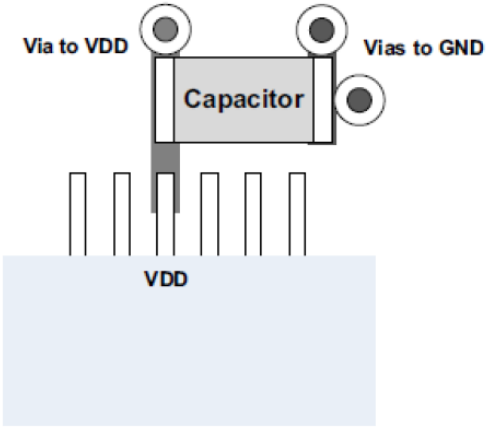
Some not-so-low ESR capacitor should be used in the application to insert loss useful to dump the cavity resonances of the VDD/VSS couple of planes. Low ESR is recommended for the high frequency local decoupling of the microcontroller.

The capacitors must be placed as close as possible to, or below, the corresponding pins on the underside of the PCB.

Again, the goal is to obtain the minimum loop inductance for each decoupling resource.

The Figure 10 shows the typical layout of such a VDD/GND pair.

Figure 10. Typical layout for VDD/VSS pair



3 External oscillator

3.1 Introduction

The product offers four clock sources to cover the various types of application:

- Fast internal RC oscillator
- Fast external crystal oscillator
- Slow internal RC oscillator
- Slow external crystal oscillator

Dual PLL is available to provide separate system and peripheral clocks and to optimize the oscillator choice versus the required system frequency.

The following table describes the clock sources available on the SPC58xx family:

Table 6. Clock sources

Mode	Oscillator	SPC58EHx, SPC58NHx	SPC584Gx, SPC58NGx, SPC58EGx	SPC584Cx SPC58ECx	SPC584Bx	SPC582Bx	SPC58EEx, SPC58NEx	SPC584Nx, SPC58ENx, SPC58NNx
Run	External crystal oscillator (XOSC)	X	X	X	X	X	X	X
	Internal RC oscillator (RCOSC)	X	X	X	X	X	X	X
	External clock (EXTAL bypass)	X	X	X	X	X	X	X
	PLL0	X	X	X	X	X	X	X
	PLL1	X	X	X	X	X	X	X
Standby	Internal RC 1024 kHz (SIRC)	X	X	X	X	X	X	-
	External crystal oscillator 32 kHz	X	X	X	X	-	X	-

This section is focused on the two external oscillators:

- The fast external crystal oscillator for the system clock covering 4 MHz to 40 MHz
- The slow external crystal oscillator for the 32 kHz low power clock

3.2 Fast external crystal oscillator (4 to 40 MHz)

The fast external crystal oscillator must be in the frequency range from 4 MHz to 40 MHz.

Please refer to the crystal manufacturer's specification for recommended load capacitor (CL) values.

The selection of internal or external load capacitors on the XTAL/EXTAL pins is determined by means of the XOSC_EXT_CLOAD bit in the UTEST miscellaneous DCF client in the UTEST row of flash memory.

XOSC_EXT_CLOAD is managed as follows:

- 0: Selects XOSC internal cap (recommended for 20 MHz <= frequency <= 40 MHz)
- 1: Selects XOSC external cal (recommended for 4 MHz <= frequency <= 20 MHz)

A further recommendation is to verify the required size of capacitances with the crystal supplier.

Note: The use of internal capacitances can be guaranteed for SPC584Bx and SPC58EHx, SPC58NHx devices only. It is not recommended to use a trim value different from 0 for all other SPC58xx devices. Please refer to the device errata sheet for more details (for example, DAN-0042615 on SPC582Bx cut2.1).

For more details about the XOSC features, please refer to the reference manual of each device (see Appendix A: Reference documents). To review the configuration and limitations of XOSC, please contact an ST representative.

The XOSC can be started with 4 MHz - 40 MHz crystal but it requires that the right frequency range is selected by programming the XOSC_FREQ_SEL[2:0] field bit in a UTEST miscellaneous DCF.

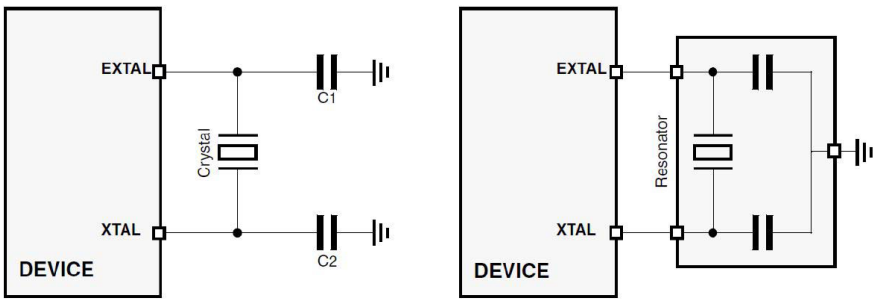
Note: The default value of this field is for a 35 MHz - 40 MHz: UTEST miscellaneous[19:21] = 111b (XOSC_FREQ_SEL).

To reduce EMC emissions, it is recommended to use the slowest crystal (resonator) together with the internal PLL (If possible with the spread spectrum feature enabled), thus achieving the proper system operating frequency.

The drawback of using a slow crystal is the longer startup time.

The Figure 11 shows the external circuit needed to use the oscillator with a crystal or a resonator.

Figure 11. Reference oscillator circuit



3.2.1 Recommended crystals (4 to 40 MHz)

As an example, the crystal NDK's NX5032GA can be selected.

Please work with the manufacturer of the chosen crystal to ensure compatibility in order to match the crystal manufacturer's specifications with the oscillator electrical specifications present in the device datasheet.

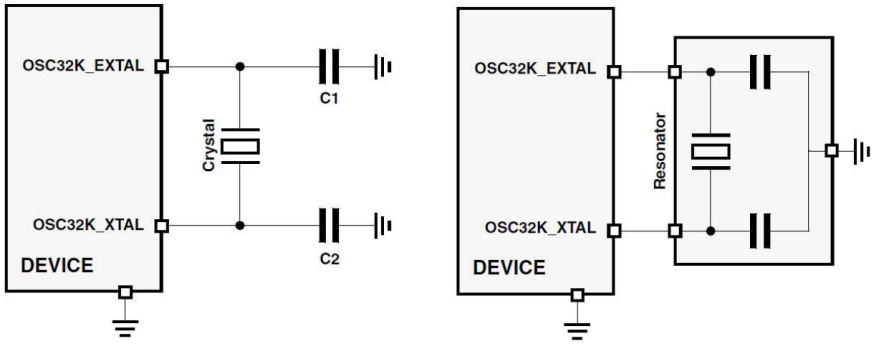
Note: It should be ensured that the testing includes all the parasitic capacitances (due to the probe, crystal, PCB board traces, etc.).

3.3 Slow external crystal oscillator (32 kHz)

The OSC32K circuit includes an internal oscillator driver and an external crystal circuitry.

The Figure 12 shows the external circuit needed for using the low power oscillator with a 32 kHz crystal.

Figure 12. Low power oscillator and resonator connection scheme



After system reset, the oscillator is put to power down state and the software has to switch on when required.

For additional information, please refer to the slow external crystal oscillator (32 kHz) electrical characteristics section in the device datasheet (see Appendix A: Reference documents).

3.3.1 Recommended crystals (32 KHz)

As an example, the crystal MC-30A can be selected.

Please work with the manufacturer of the chosen crystal to ensure compatibility in order to match the crystal manufacturer's specifications with the oscillator electrical specifications present in the device datasheet.

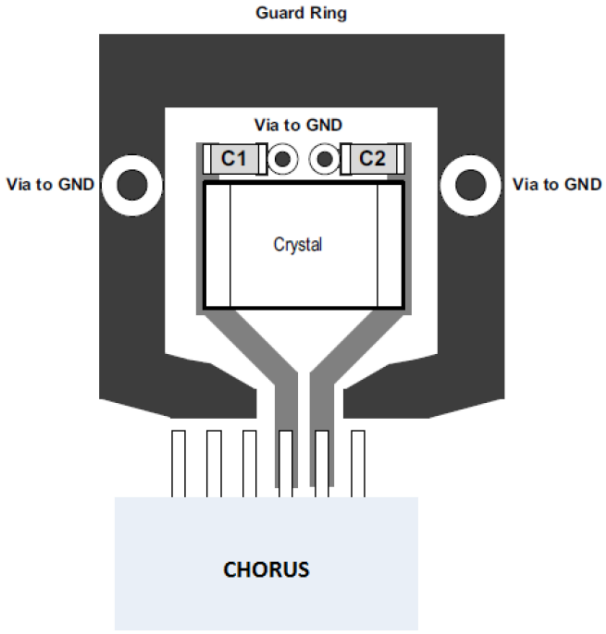
Note: It should be ensured that the testing includes all the parasitic capacitances (due to the probe, crystal, PCB board traces, etc).

3.4 Oscillator layout recommendations

To optimize performance and minimize EMC (electromagnetic compatibility) susceptibility the following recommendations should be observed to design the oscillator circuitry layout:

- A current flow at the crystal-fundamental frequency runs through the oscillator circuit. If the oscillator is clipped, then the high-order harmonics are present. To minimize the emissions generated by these currents and enhance the electromagnetic immunity, the oscillator circuits should be kept as compact as possible
- Configure the GND supply at low impedance
- Avoid routing other high frequency signals near the oscillator circuitry
- Do not route signals near the area of the oscillator. Analyze crosstalk between different layers.
- Shield the crystal with an additional ground plane underneath the crystal. This has an impact on the oscillation margin of the oscillator: the layout must be carefully characterized.
- If the shield mentioned above is not implemented, open all inner layers in correspondence of the oscillator to reduce capacitance.
- If the crystal package is metallic, it should be connected directly to GND
- To isolate the noise to or from the oscillator, it is possible to put a “guard ring” around the oscillator. This ring must be as small as possible and frequently contacted with GND.
- Capacitors should be placed between both ends of the crystal and GND (solid plane)
- Avoid placing the oscillator near the edges of the application PCB

Figure 13. PCB layout example



4 Reset

4.1 Introduction

SPC58xx family reset interface implements:

- The PORST pin, which is an input/output pin (a dedicated bidirectional reset pin), is used to trigger an internal destructive reset.
- The ESR0 functionality(a):
- – In the SPC58xx family but SPC584Gx, SPC58NGx, SPC58EGx, SPC58EEx, SPC58NEx, and SPC584Nx, SPC58ENx, SPC58NNx device, the PC[1] can be configured as the ESR0 output external reset by programming the DCF client ESR0_CONFIG. In this way, this pin can be used to report an internal reset (both destructive and functional) to the external.
  – Dedicated bidirectional ESR0 pin on SPC584Gx, SPC58NGx, SPC58EGx, SPC58EEx, SPC58NEx, and SPC584Nx, SPC58ENx, SPC58NNx device.

Table 7. Reset pads

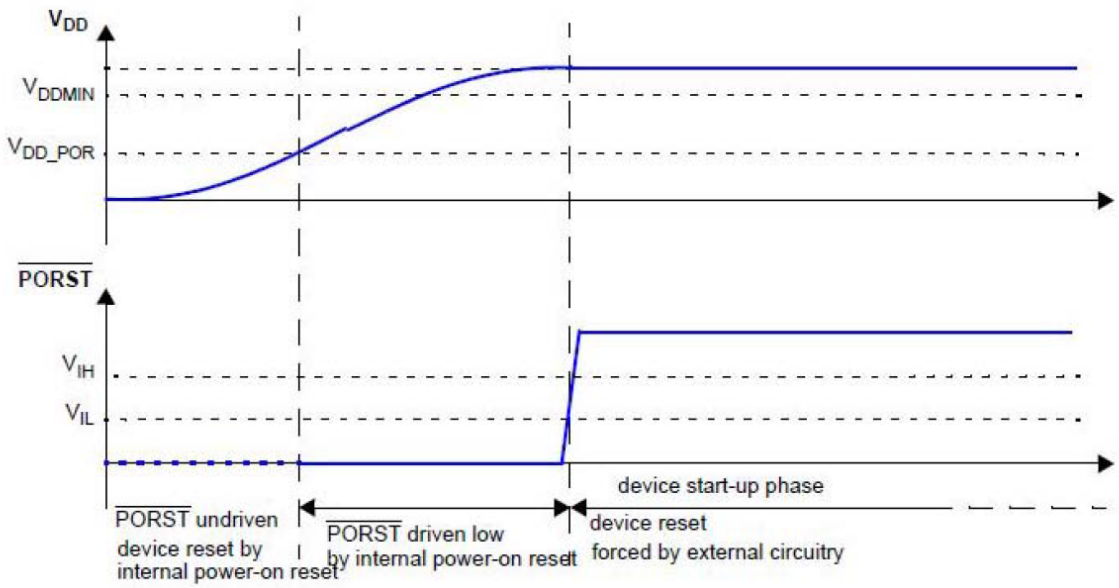
Reset pads	Description	Direction
PORST	Power on reset with Schmitt trigger characteristics and noise filter. PORST is active low and acts as destructive reset.	Bidirectional
ESR0	Reset monitor (on port C[1])	Output
ESR1	Reset monitor (on port A[4])	Input

1. *Dedicated ESR0 pin on: SPC584Gx, SPC58NGx, SPC58EGx, SPC58EEx, SPC58NEx and SPC584Nx, SPC58ENx, SPC58NNx.*
2. *PA[4] can be configured as the ESR1 input external reset through WKPU registers.*

4.2 RESET electrical characteristics

The device implements dedicated bidirectional reset pins as shown in the Figure 14. PORST pin does not require active control. It is possible to implement an external pull-up to ensure a correct reset exit sequence. The recommended value is 4.7 KΩ.

Figure 14. Startup reset requirements



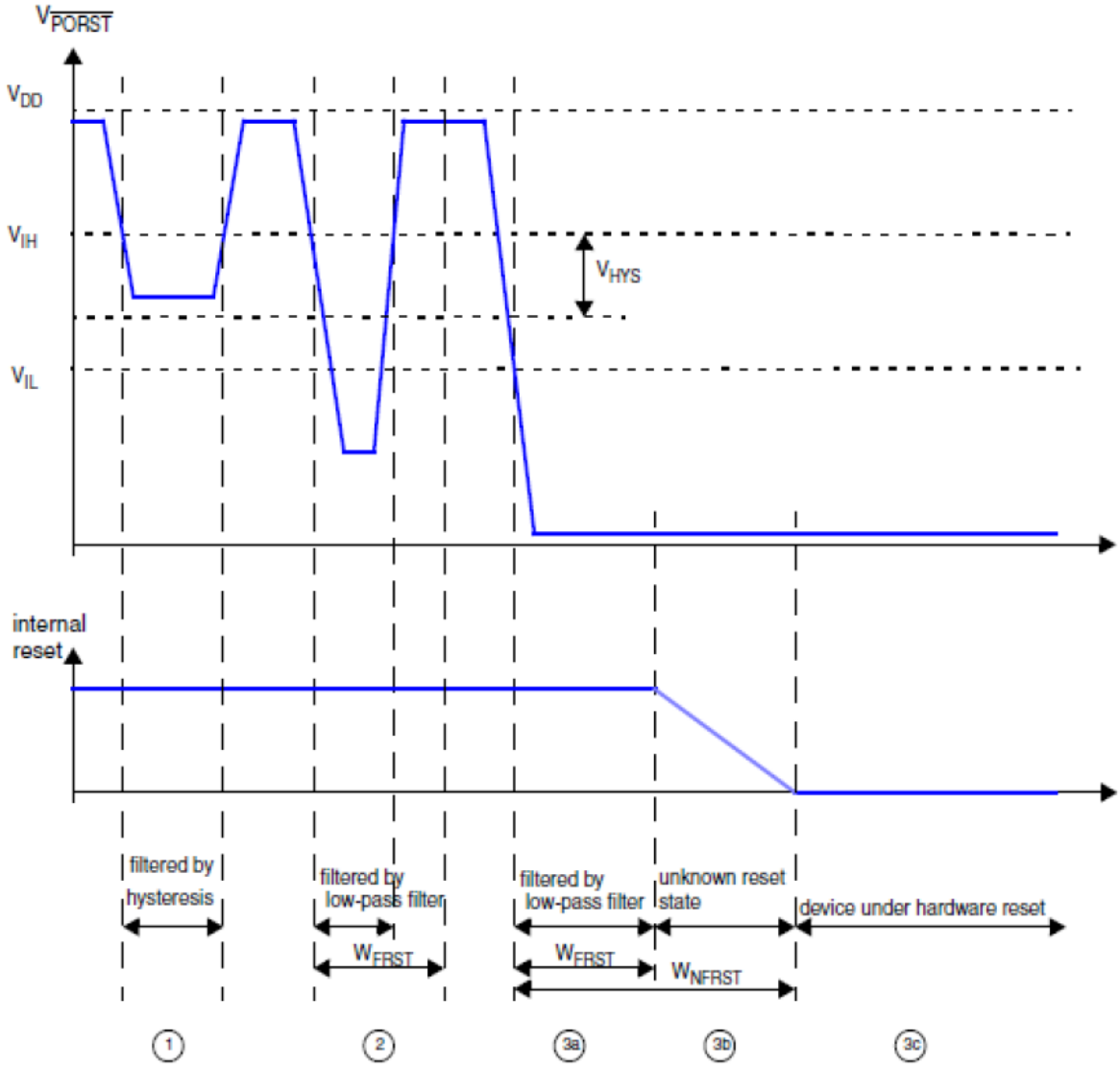
To prevent noise on the reset signal from wrongly generating a reset, the PORST pad includes an analog filter.

To enhance EM immunity, the reset circuitry must be compact and close to the PORST pin, keeping connections short and providing local decoupling.

The Figure 15 describes the device behavior depending on the supply signal on PORST (see Appendix A: Reference documents).

1. PORST does not go low enough: it is filtered by input buffer hysteresis. The device remains in the current state.
2. PORST goes low enough, but not for long enough: it is filtered by a low pass filter. The device remains in the current state.
3. PORST generates a reset:
   a. PORST low but initially filtered during at least WFRST. Device remains initially in current state.
   b. PORST potentially filtered until WNFRST. Device state is unknown. It may either be reset or remains in the current state depending on extra conditions (PVT—process, voltage, and temperature).
   c. PORST asserted for longer than WNFRST. The device is under hardware reset.

Figure 15. Noise filtering on reset signal



The external reset signal (pulse) of a PORST pin must be greater than WNFRST (2000 ns) to generate an internal reset. Pulses less than WFRST (500 ns) do not generate an internal reset. An internal reset may, or may not, be generated for pulses between WFRST and WNFRST.

4.2.1 Device behavior across resets

Software issued or hardware triggered resets (destructive or functional) inevitably introduce interdependencies with the external hardware by design. This occurs both in terms of actual signal propagation outside the chip via the PORST/ESR0 signals and due to impact on power supply.

Some peripherals and memories (such as PIT or system memory) are designed to retain certain information across resets. While ST can test that specific properties are indeed maintained after a reset, it is not possible to test dynamic device behavior including actual peripheral or memory usage across resets under all possible circumstances, especially with specific external hardware design.

It is advised to carefully monitor use case scenarios entailing active interaction with such devices during reset, with the previously mentioned property retention feature. Please contact ST sales representative for further guidance on this topic.

4.3 ESR0 pin functionality

SPC58xx family but SPC58NGx (SPC584Gx, SPC58NGx, SPC58EGx) SPC584Nx, SPC58ENx, SPC58NNx andSPC584Nx, SPC58ENx, SPC58NNx devices do not implement a dedicated pin to output a reset signal.

Note: ESR0 is a dedicated bidirectional reset pin only on SPC58NGx, SPC584Nx, SPC58ENx, SPC58NNx andSPC584Nx, SPC58ENx, SPC58NNx.

Nevertheless, it is possible to statically configure one pin to act as an output reset. The operation is done by reading a specific DCF record ESR0_CONFIG. The DCF is read during the reset phase 3 destructive and the read value is maintained until the next power on reset.

The following list summarizes the static pin configuration:

- One dedicated GPIO shall have a double function:
  1. ESR0 reset output only
  2. GPIO/AF
- The choice between 1) and 2) is done via DCF reading at every reset
- The value uploaded via DCF is maintained throughout the next destructive or functional reset
- After a Power-On-Reset the default value is GPIO
- After a destructive or functional reset, the default value is the last one being uploaded via DCF
- In case the pin is configured as GPIO, during a reset phase the pin shall maintain the same under-reset safe configuration as for all the other GPIOs
- In case the pin is configured as ESR0, during the reset phase, the pin is driven to “0” by the RGM module, while out of reset, the pin is not driven (the pad “obe” signal is deasserted) and a weak pull-up will set it to “1”
- The ESR0 pin has the same electrical characteristic as a GPIO.

4.4 Reset scheme

This section is under development.

4.5 Power-on reset (POR) and low voltage detectors (LVDs)

The function of the POR and LVD circuits is to hold the device in reset regardless of how slow the supply voltage rise is, until the point at which the POR and LVDs are released.

The POR and LVD circuits function correctly even if the input voltage is non monotonic.

Please refer to the device reference manual and datasheet for more details (see Appendix A: Reference documents).

Table 8. Voltage monitors configurability

Monitor type	Reset event enable	Reset event slect	Event pending register	Interrupt enable	FCCU event enable (1)	Reset event enable DCF (1)
MVDs	No	No	No	No	No	No
LVDs	Yes	Yes	Yes	Yes	Yes	Yes
HVDs	Yes	Yes	Yes	Yes	Yes	Yes
UVDs	No	No	No	No	No	No

1. *All samples of SPC58x family are delivered with:*
   - *PMC_REE_BUS DCF = 0x0000_0000 and*
   - *PMCDIG_REE_LVx/HVx = 0*
   - *PMCDIG_FEE_LVx/HVx = 0.*
2. *By default the reset value of the PMC_REE_BUS DCF and REE bits in PMCDIG_REE_xxx registers is equal to '0' thus when the voltages pass the trigger event (voltage monitoring threshold) all configurable resets events and FCCU events are disabled.*

The Table 9 gives an example describing the relationship between bits of PMC_REE_BUS DCF record and PMCDIG_REE_xxx registers.

Table 9. Configurable VDs on SPC584Cx, SPC58ECx

Bit	PMC_REE_BUS	PMCDIG_REE_xxx	VD NAME	VD MEANING
15	LVD14_AS	REE_HV1[REE14_AS]	LVD400_AS	HV detector asserts when SAR ADC supply < 4.00 V
16	LVD14_IF	REE_HV1[REE14_IF]	LVD400_IF	HV detector asserts when IO FLEXRAY supply < 4.00 V
18	LVD14_IM	REE_HV1[REE14_IM]	LVD400_IM	HV detector asserts when IO MAINS supply < 4.00 V
19	HVD13_IF	REE_HV1[REE13_IF]	HVD400_IF	HV detector asserts when IO FLEXRAY supply > 4.00 V
23	LVD11_AS	REE_HV0[REE11_AS]	LVD290_AS	HV detector asserts when SAR ADC supply < 2.90 V
24	LVD11_IF	REE_HV0[REE11_IF]	LVD290_IF	HV detector asserts when IO FLEXRAY supply < 2.90 V
26	LVD11_FL	REE_HV0[REE11_FL]	LVD290_FL	HV detector asserts when FLASH supply < 2.90 V
27	LVD11_C	REE_HV0[REE11_C]	LVD290_C	HV detector asserts when PMU supply < 2.90 V
28	HVD6_C	REE_LV1[REE6_C]	HVD134_C	LV detector asserts when PMU supply > 1.34 V
29	LVD3_SB	REE_LV0[REE3_SB]	LVD100_SB	LV detector asserts when standby supply < 1.0 V
30	LVD3_FL	REE_LV0[REE3_FL]	LVD100_FL	LV detector asserts when FLASH supply < 1.0 V
31	LVD3_C	REE_LV0[REE3_C]	LVD100_C	LV detector asserts when PMU supply < 1.0 V

1. *REE_LVx/HVx bits are loaded during the boot sequence based on programmed PMC_REE_BUS DCF record value.*

5 ADC

5.1 Introduction

The shows the ADC modules present in the devices of the SPC58xx family and the number of analog channels.

Table 10. ADC modules

Converter type	12-bit SAR ADC					10-bit SAR ADC(1)			16-bit sigma delta ADC					
	SAR_ADC_12bit_SUPERVISOR	12-bit SAR_0	12-bit SAR_1	12-bit SAR_2	12-bit SAR_3	10-bit SAR_0	10-bit SAR_1	10-bit SAR_1	16-bit SD_ADC_0	16-bit SD_ADC_1	16-bit SD_ADC_2	16-bit SD_ADC_3	16-bit SD_ADC_4	16-bit SD_ADC_5
SPC58EHx, SPC58NHx	95	16	16	16	16			24						
SPC584Gx, SPC58NGx, SPC58EGx	82	8	8	15	16			8						
SPC584Cx, SPC58ECx	95	16	16		16			24						
SPC584Bx	63	11	11					9						
SPC582Bx	27	16												
SPC58EEx, SPC58NEx	82	8	8	15	15			8	2	2	4	8	2	2
SPC584Nx, SPC58ENx, SPC58NNx	84	12	12	13	15	6	6		2	2	4	8	2	2

1. *In addition, + 4 BIAS test ch*
2. *Temp-Sensor (TSENS) + digital bandgap + external ch*
3. *In addition, only external ch (no TSENS)*
4. *7 ADCQ modules to support enhanced command queue control mode*

Note: The table describes the maximum number of available channels per dedicated silicon but the available number of channels per package might be different (see device pinout definition).

*Note: The ADCBIAS block provides four different voltage levels defined as GND, Vref/3, 2*Vref/3, and Vref. The self-test internal reference voltage precision is provided in the SAR ADC electrical specification table of the device datasheet.*

Caution: Regarding the constraints and relationships for the different power domains, see the device datasheet the section “Power domains and power up/down sequencing” (see Reference documents).

5.2 Analog Input pins

There are three different ADC input channel types:

- Analog input channels (called “internal channels”) that include programmable pull-up / pull-down resistors to detect an open or short circuit condition. This allows for application testing of the mux input logic.
- External multiplexed channels (called “external channels”) mapped to any internal channel through static programming by software, thus allowing it to perform conversions like any other channel of the ADC.
- Internal test channels (called “test channels”) to be used for self-diagnosis of the converter and diagnosis of the analog signal path up to the external circuitry.

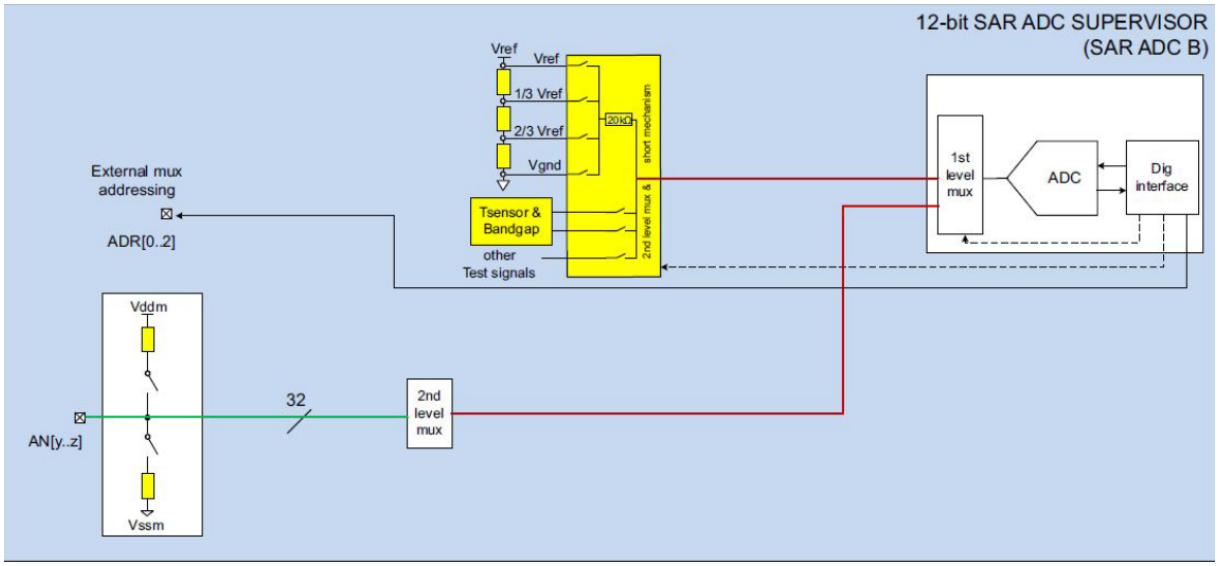
ADC channels are divided in two groups:

- Precise channels
- Other channels

For features, mapping, and channel characteristics, please refer to device datasheets (see Appendix A: Reference documents).

The Figure 16 gives an example of SPC582Bx device.

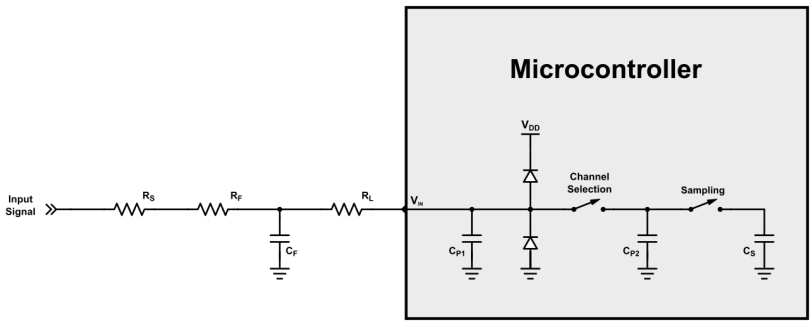
Figure 16. ADC System



5.3 ADC performances optimization

The Figure 17 shows an example of an external network connected to the input equivalent circuit for SARn and SARB channels.

Figure 17. External network and input equivalent circuit



To preserve the accuracy of the ADC conversion, it is necessary that the analog input pins have the AC impedance as low as possible. A very large capacitor CF with good high frequency characteristics at the input pin can attenuate the noise. Furthermore, the charge it accumulates will flow to the sampling capacitance CS during the sampling phase, which will cause a drop in the voltage at the input pin. This drop has a negligible effect on the measure if C_F > 8192*C*S.

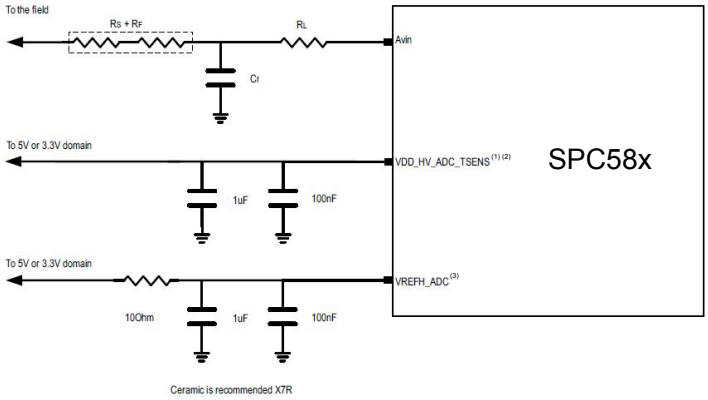
A current limiter resistance RL in series with the RC filter formed by CF and its parasite resistance RF is often necessary to minimize the current request and attenuate the noise on the input pin. This external network can generate accuracy problems for the ADC conversion and limit its sample rate, so it is important to invest time in reaching the right adaptation. RL should be sized so that the rising transient of the voltage on CS is much shorter than the sampling period:

$$\tau = R_L \cdot (C_S + C_{P1} + C_{P2}) \quad (1)$$

This time constant must allow the sampling capacitor to charge within 1/2 LSB within the sampling window.

For more information on these design constraints and help to find the best configuration to optimize the device, please refer to the application note AN4413 and AN5527 as guideline for the SARADC features (see Reference documents).

Figure 18. ADC application setup



(1) The device datasheet reports the actual value of external components to be used.
(2) It is possible to add bypass capacitance of 100 nF for improved noise filtering.
(3) If VDD_HV_ADR (VREFH_ADC) is not shorted with VDD_HV_ADV (VDD_HV_ADC_TSENS) in the PCB a capacitance of 1 µF shall be added.
If VDD_HV_ADR is shorted with VDD_HV_ADV in the PCB 1 µF is not required because the CADC (refer to datasheet) on VDD_HV_ADV is enough.
It is possible to add bypass capacitance of 100 nF for improved noise filtering.

6 Boot configuration

6.1 Introduction

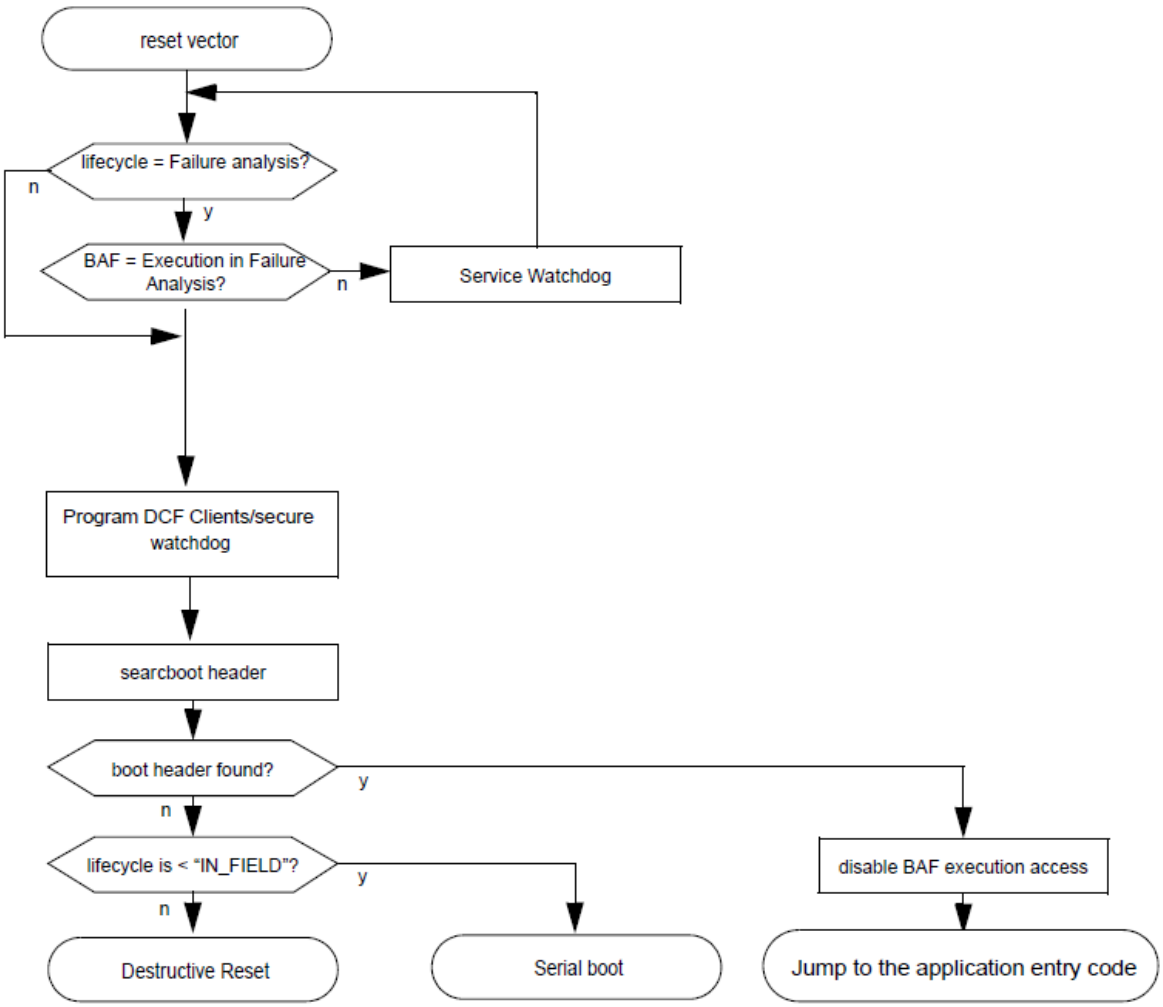
The boot of the device is managed by Boot Assist Flash (BAF) code programmed by ST into UTest block so to provide a serial bootloader feature or to boot from internal flash.

The following serial boot modes are supported:

- MCAN (MCAN_1/2)
- LIN/UART (LINFlexD_0/2)

Note: There are no longer any FAB or ABS pins on these devices as there were on previous families (SPC56xx and SPC57xx) so serial boot mode is only entered if no valid RCHW (reset configuration half word) is found.

Figure 19. Flow of control



6.2 Boot mode selection

No pin has to be configured to select the serial boot mode.

The BAF code checks the life cycle (LC) of the device. If no valid boot header is found in internal flash memory and the current life cycle phase of the device is less than “In Field”, an attempt is made to download the application by a serial protocol using the LINFlexD modules or M_CAN modules. The downloaded code is then executed by the CPU boot.

The BAF bootloader code enables the Rx-channels of all four serial interfaces at start of serial boot sequence and it shall take care of polling all four Rx-channels to detect the valid serial boot message. All Tx-channels have to be disabled during this phase. After a successful detection of the active Rx-channel the corresponding Tx-channel shall be enabled and the three inactive Rx-channels shall be disabled.

6.3 LINFlexD and MCAN pins configuration

The package pins used by LINFlexDs are the same pins used by the M_CAN modules.

Table 11. LINFlexD and MCAN pin configuration

Pads	Initial serial boot mode		Serial boot mode after a valid CAN message received	Serial boot mode after a valid LINFlexD message received
	Function	Pad configuration	Function	Function
PA[10]	MCAN_2 Tx	Output: : Push/Pull medium drive no pull-up/pull-down	MCAN_2 Tx	LINFlexD_2 Tx
PA[11]	LINFlexD_2 Rx and MCAN_2 Rx	Input: high-Z hysteresis CMOS level	MCAN_2 Rx	LINFlexD_2 Rx
PB[10]	MCAN_1 Tx	Output: Push/Pull medium drive no pull-up/pull-down	MCAN_1 Tx	LINFlexD_0 Tx
PB[9]	LINFlexD_0 Rx and MCAN_1 Rx	Input:— high-Z hysteresis CMOS level	MCAN_1 Rx	LINFlexD_0 Rx

1. *Pad is set to output configuration as described in the table. Output buffer is enabled for the whole duration of the BAF serial boot.*

Please refer to the boot assist flash (BAF) chapter in the device reference manual (see Appendix A: Reference documents) for additional information.

7 Debug

SPC58xx microcontrollers have a comprehensive feature set to assist debug and trace (see Appendix A: Reference documents).

7.1 Introduction

Two interfaces are used to support debug and trace functionality. These are the JTAG port and the nexus auxiliary port (NAP). The JTAG port is used for debug and test purposes while the NAP is used to transfer trace data streams.

7.2 JTAG I/O

The SPC58xx feature a JTAG port with a 4-pin interface. The supported signals are TDI, TDO, TCK, and TMS.

Table 12. JTAG signals

Signal	Description	Direction
TDI	Test data input	Input
TDO	Test data output	Output
TCK	Test clock	Input
TMS	Test mode select	Input

Table 13. JTAG pads

Signal	JTAG Connector PAD
TDI	1
VSS	2
TDO	3
VSS	4
TCK	5
VSS	6
EVTI	7
PORST	8
ESR0	9
TMS	10
VREF	11
VSS	12
EVTO	13
JCOMP	14

1. *If ESR0 signal is not available (because not configured through DCF), please short Pin 9 to PORST pad.*

7.3 Nexus Auxiliary port

SPC58xx has got Nexus 3+ module.

8 I/Os

8.1 Introduction

The device features a unique pad technology to sustain a current injection of IINJPAD (refer to device datasheet, see Appendix A: Reference documents) on digital and analog inputs.

The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume a typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.

8.2 I/O types

The following table describes the different pad type configurations.

Table 14. I/O pad specification descriptions

Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
Strong configuration	Provides fast transition speed; used for fast interface.
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface including Ethernet and FlexRay interfaces requiring fine control of rising/ falling edge jitter.
Ultra strong configuration	Provides very high speed interfaces till 125 MHz
Differential configuration	A few pads provide differential capability providing very fast interface together with good EMC performances.
Input only pads	These low input leakage pads are associated with the ADC channels.
Standby pads	These pads (LP pads) are active during STANDBY Mode, with following logic configuration: • On SPC58EC80x/SPC584C80x cut1.1, SPC58NHx/SPC58EHx and SPC584Bx they are configured in CMOS level logic and this configuration cannot be changed • On all others dies/cuts, they are configurable in the running modes while are TTL (not configurable) in STANDBY mode. *Note: In such case, if a LP pad is used to wakeup from STANDBY, it should be configured as TTL also in running mode in order to prevent device wrong behavior in STANDBY.*

1. *Only for SPC58NHx (SPC58EHx, SPC58NHx).*
2. *Not available for SPC584Nx, SPC58ENx, SPC58NNx.*

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

PMC_DIG_VSIO register has to be configured to select the voltage level (3.3 V or 5.0 V) for each IO segment.

Note: All output types have a slope control (current) to reduce the EMI.

In order to reduce the noise generated on the I/O power, it is recommended to select the slowest configuration compatible with the functionality required. A series resistor in the range of few tenths of an ohm can be effective as filter, combined with the parasitic capacitance of the connection.

High toggling rates and signals used as clocks for external devices or peripherals could require reinforced decoupling and filtering.

Please refer to the device datasheet and reference manual (see Appendix A: Reference documents) for the detailed I/O electrical characteristics and I/O definitions.

8.3 Pad configuration after reset

This SPC58xx devices contain safety mechanisms to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins (see Appendix A: Reference documents).

To avoid activating external components while under reset, all pads are forced to high impedance inputs, with the following exceptions:

Table 15. Pins status reset

Port	Name	I/O	Reset state	Pull
PA[5]	JCOMP	Input		Down
PA[6]	TCK	Input		Down
PA[7]	TMS	Input		Up
PA[8]	TDI	Input		Up
PA[9]	TDO	Output	High Z(1)	

1. *When JTAG is enabled (JCOMP asserted) during reset, the TDO pin is pulled up during reset, but Hi-Z after. If JTAG is disabled, the TDO pin defaults to input/pull-up during and after reset.*

8.4 Maximum output current

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a VDD/VSS supply pair as described in the pinout Microsoft Excel file attached to the IO_Definition document.

In order to ensure the device reliability, the average current of the I/O on a single segment should remain below the IRMSSEG maximum value.

In order to ensure the device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the IDYNSEG maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided on the I/O Signal Description table.

8.5 I/O characteristic in standby mode

The IO pins in standby mode can be divided in 2 types:

- Not low power pin (NLP): These pins are not active in standby. When standby is entered, both input and output buffers inside the pins are disabled. Thus, also internal pull-up/down are disabled.

Note: Floating state do not affect the power consumption because of isolation within the pad is automatically applied.

- Low power pin (LP): These pins are active during standby. When the device enters the standby mode, the pad-keeper feature is activated for all LP pins (for more details refer to PAD-keeper). The handling of low power I/O depends on the features available on this LP I/O and the function used by the application during STBY.

The following low power features are available:

- Wake-up/pad-keeper
- Output port control
- Port digital comparator
- Analog input

In standby mode the low power I/Os offer the following features, which require special considerations:

- The wake-up lines are inputs that can be used as external interrupt sources in normal run mode or as system wake-up sources in all low down modes.
- The “OPC” is used to set the output level of a digital port pin to a desired level, in order to let the customer open/close some external switches.
- The “PDC” is used to measure the level of a set of pin and to trigger a system wake-up event when the level is acknowledged at a specified level.
- The “ADC standby” is a reduced, low-power version of the analog-to-digital converter. Its main functionality is to compare the converted value towards a watchdog, and trigger a wake-up event in case the value is out of the intended range.
- The “DSPI_LP” (low power DSPI) is used to send one DSPI frame to an external device during the standby mode, without processing any message reception. The DSPI_LP module can be fully working like a regular DSPI when in non-stand-by mode.

Note: OPC, PDC, ADC standby and DSPI_LP features are available by means of the SSWU smart standby wake-up unit (SSWU). These features are present on all SPC58xx family devices with the following exceptions:

- *DSPI_LP module is only available on the SPC58NHx device.*
- *SPC582Bx device only supports the latching feature on PAD25-PB9 and PAD53-PD5.*

Caution: Analog inputs on LP I/O with digital features should be handled very carefully as they cause extra consumption in case the input voltage is between V_IL and V_IH.

Note: Unbonded LP I/O must be configured as unused I/O.

The TDO pad is part of the standby domain in order to provide a handshaking mechanism with a debugger in standby mode and it is the LP pin with a pad-keeper feature always enabled (for more details refer to PAD-keeper).

Externally connecting the TDO pad to the VDD or GND, this pad must be tied by means of an external pull-up (or pull-down) resistor of 4.7 KΩ.

Note: This section is not applicable for the SPC584Nx, SPC58ENx, SPC58NNx device.

8.5.1 PAD-keeper

When the device enters in STANDBY mode, the pad-keeper feature is activated for all LP pads. It means that:

- If the pad voltage level is above the pad-keeper high threshold (PK_h), a weak pull-up resistor is automatically enabled.
- If the pad voltage level is below the pad-keeper low threshold (PK_l), a weak pull-down resistor is automatically enabled.

For the pad-keeper high/low thresholds please consider the CMOS threshold for SPC58EC80x/SPC584C80x cut1.1, SPC58NHx/SPC58EHx and SPC584Bx. On all others dies/cuts, these thresholds are TTL (not configurable) in STANDBY mode.

Regarding the pad-keeper weak pull-up/down, these are the same as the ones configurable through SIUL2_MSCR_IO register in running mode, and their values (RWPU/RWPD) are showed in the device datasheet.

Refer to the device pinout excel file (package sheets) for the list of LP pins. Full list of the LP pins can be found in the device pinout excel file, not in this document.

Caution: Pad-keeper feature can be disabled for a subset of devices (e.g. SPC584Bx cut1.2). To disable the latter feature user needs to set the WKPU.WIPUER[x] = 1 (for more details please refer to the device specific RM). For all other devices on which pad-keeper feature is not customizable (so it's always enabled) in case of leakage on the pad, to avoid the undesired transition, it's necessary to do the following (Please refer to device errata sheet for more details (e.g. PS3022 on SPC584Cx, SPC58ECx, cut1.1):

- By HW to add an external pull-up on pad configured to wake-up from STANDBY Mode in order to avoid false wake-up event
- By SW it is required that WKPU.WIPUER is set to 0, to avoid contention with external pull components.

Note: *In running mode, by setting to 1 the WKPU.WIPUER[x] = 1 without enabling the pull-up/down IO configuration through SIUL2 registers the internal pull-down on pad is activated.*

In case of pad-keeper disabled, we need external pull-up/down on the used LP pads to avoid false wakeup events; this because internal pull-up/down is no more available.

Internal pull-down is required for Unused/Unbonded LP pads, achieved by setting the SIUL2.MSCR_IO [x].WPDE bit while WKPU.WIPUER has to be set to 1: this to force pad level during transition in STANDBY Mode.

Note: *This section is not applicable for SPC584Nx, SPC58ENx, SPC58NNx.*

Full details about PAD-keeper can be found in the relative application note (see Appendix A: Reference documents).

8.6 General consideration for I/O

- Pins adjacent to single ended clocks, like DSPI SCK, clock outputs and so on, can experiment high crosstalk. Possibly use them as semi-static outputs, configured at low impedance. Avoid to route these pins with long traces and drive outside harness.

Note: The SPC58EHx, SPC58NHx microcontroller has many GPIOs in double bonding; this feature is in place for all packages but FPBGA386. Some IO PADS are bonded together within the package, to provide different alternative functions for same pin/ball. The application shall enable only one pad at a time for each pin/ball in double bonding, by ensuring also the disabling of the I/O buffers for other pin/ball [i.e IBE = ODC = 0x0] so to avoid high current consumption, due to electrical contention, and reliability issues of the pad drivers. Please refer to the SPC58EHx, SPC58NHx IO definition document, where double bonded pin/balls are clearly identified, paying attention (during software design) to avoid the described electrical contention.

- Configure the driving strength of the digital outputs as low as compatible with the functionality.
- Consider the possibility to insert an optional low value resistor in series to pins used as digital clocks (see above). The resistor plus the parasitic capacitance creates a low pass filter reducing the high frequency ringing and the correspondent emissions.
- Distribute the toggling pins on different power segments, so to avoid having them insisting on the same power segment.
- Testmode pin, disabled for customer, needs to be put to low state (GND).
  - Example: SPC58xGx 144pin, pin 94 needs to be set to GND

During the application design the absolute maximum voltage on I/O must be considered.

For more details please refer to the device datasheet (see Appendix A: Reference documents).

8.6.1 Unused and unbounded pin management

In some applications, not all pins of the device may be needed.

To improve the reliability of the application it is recommended to keep the unused NLP I/O in the default configuration:

- Hiz with input buffer off for SPC58EHx, SPC58NHx, SPC584Gx, SPC58NGx, SPC58EGx, SPC584Cx, SPC58ECx, SPC584Bx, SPC582Bx.
- Input Weak Pull Up for SPC58EEx, SPC58NEx and SPC584Nx, SPC58ENx, SPC58NNx device.

Particular care is required for the Low Power I/O as they may cause significant extra consumption (several mA) due to their Schmitt Trigger logic. This may be very critical in particular in STBY mode.

To avoid extra consumption the unused LP I/O must be configured so to enable internal pull-down. To force pad level during transition in STANDBY Mode:

- If a wakeup line is mapped on an unused LP I/O, set the SIUL2.MSCR_IO [x].WPDE bit and WKPU.WIPUER[x] bit to 1.
- If no wakeup line is mapped on an unused LP I/O, only set the SIUL2.MSCR_IO [x].WPDE bit.

Note: In smaller packages some pads are unbounded (not connected to a package pin), therefore it is also important to configure unbounded pads as unused I/O. Unbounded LP I/O must be configured as unused LP I/O as aforementioned.

8.7 I/O PAD block diagrams

Here are reported the I/O PAD block diagrams and the pad characteristics.
Running mode and standby modes are covered.

8.7.1 Running mode

Figure 20. I/O Pad diagram with analog input

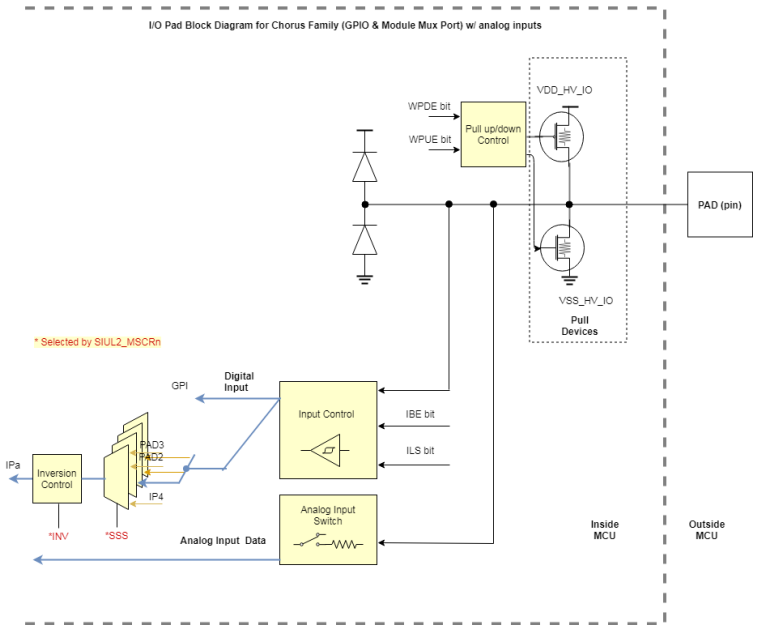
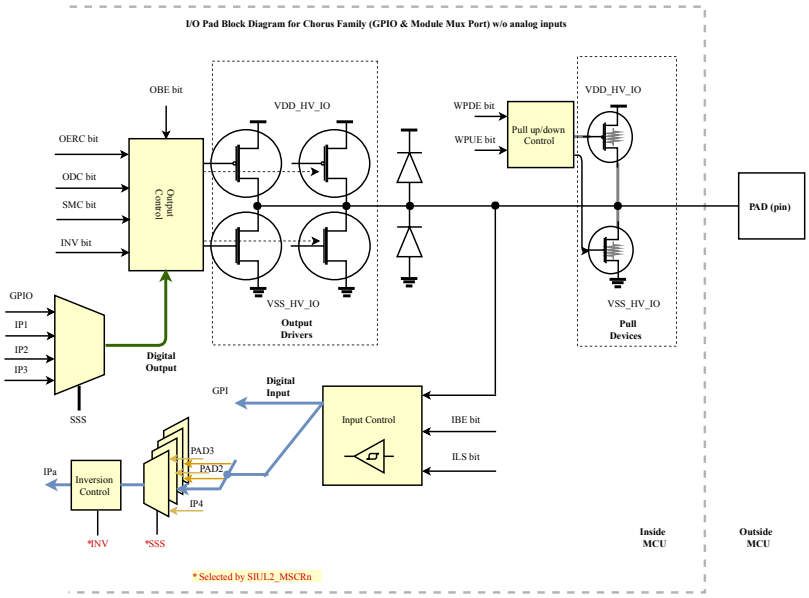
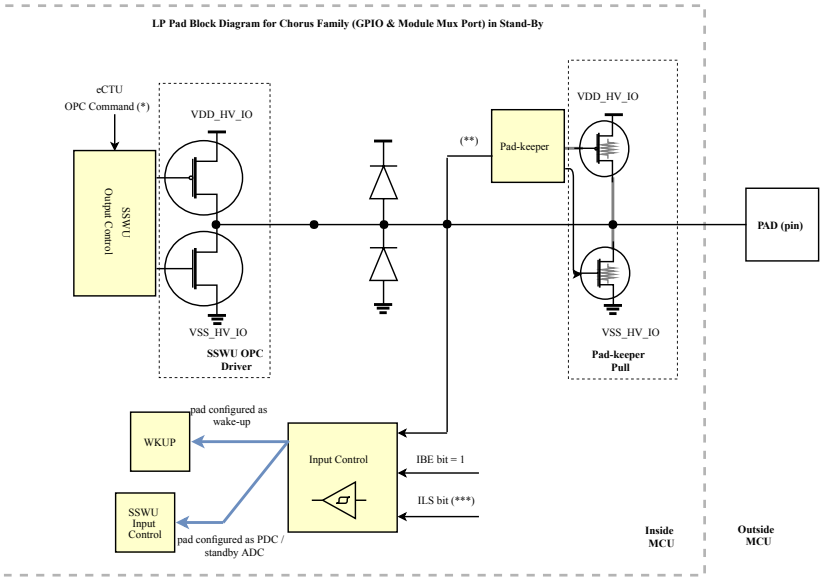


Figure 21. I/O Pad diagram without analog input



8.7.2 Standby mode

Figure 22. LP pads diagram



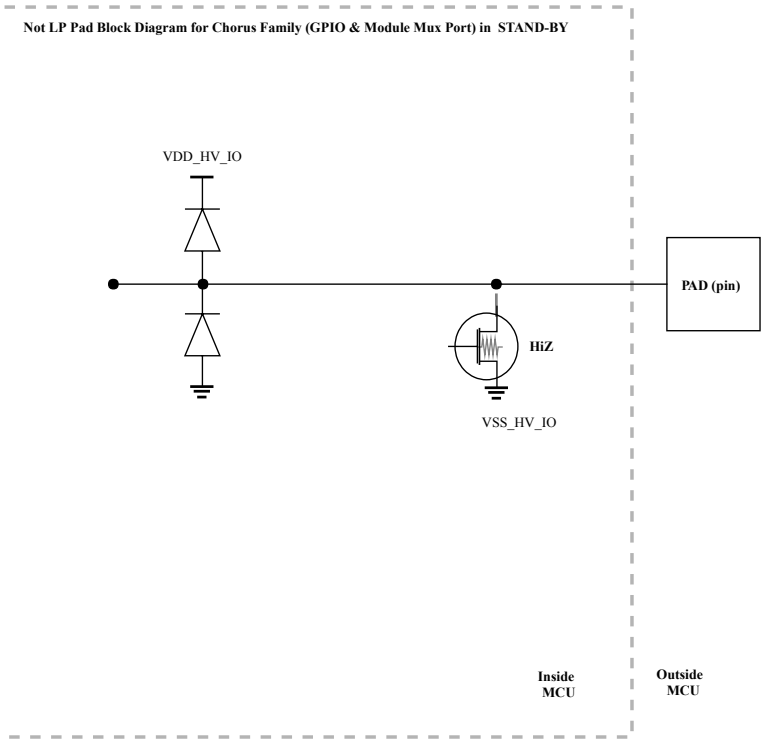
(*) eCTU will drive the pad as output in case that it has been configured as OPC through SSWU

(**) Padkeeper Pull-up/Down application depends on the pad voltage level at last active driver on the pad

(***) Input logic depends on specific die:

- CMOS for SPC58EC80x/SPC584C80x cut1.1, SPC58NHx/SPC58EHx and SPC584Bx
- TTL for the others dies

Figure 23. Not LP pads diagram



8.7.3 Pads summary in running/standby modes

Table 16. Pads summary

Pads	After reset		Running mode		Standby	
	Impedance	Leakage	Impedance	Leakage	Impedance	Leakage
Not LP	Hiz: Min Pad Impedance @ (0°C to 150°C)>5.5 MΩ	Supply leakage current can vary in different PVTs depending on voltage established on floating Io pad but max leakage is 1 µA@150°C (5.5 V/5.5 MΩ)	Refer to DS for input/output impedance	see Table 17	Hiz: Mini Pad impedance at (0°C to 150°C)>5.5 MΩ	Supply leakage current can vary in different PVTs depending on voltage established on floating Io pad but max leakage is 1 µA@150°C (5.5 V/5.5 MΩ)
LP					Pad-keeper values Pull-up: Min = 35.23 KΩ, Max = 56.69 KΩ Pull-down: Min = 31.16 KΩ, Max = 49.43 KΩ	

Table 17. Pins status reset

Leakage	
Pad Input Leakage values (T_j =150°C)	Value
INPUT-ONLY pads	200 nA
STRONG pads	1 nA
VERY Strong pads	1 nA
BIDIRECTIONAL (either Input or Output)	1 µA

9 EMC guidelines

This section summarizes the main recommendations for the system designers to improve the electromagnetic compatibility (EMC). Particular attention is given to the way to reduce the radiated emissions of a system based on the SPC58xx devices.

The recommendations reported in this document should be considered additional to the standard industry practices and not intended to be an exhaustive list of precautions in the application designs.

Note: It is expected that the application boards are designed according to good Signal and Power integrity practice. Providing a solid reference to every digital signal is particularly important.

9.1 SPC58xx software configurations

The SPC58xx family offers some features that allow, by means of software configurations, to cover some requests for the reduction in the electromagnetic interference (or EMI) emissions:

- The system clock should be chosen to avoid overlapping with the fundamental and the first three harmonics known critical frequency bands (like the car radio international FM band). Avoid any harmonics in the GNSS bands (GPS, Glonas, Galileo, Beidou....) because of the very severe limits permitted.
- The FMPLL gives the possibility to modulate the system clock so to reduce the peaks of emission.

Note: FM is not available in SPC582Bx.

- Choose the lowest possible slew rate and driving capability of the output pins according with the functionality chosen for the pins.
- The peripherals that are not used in the application should be disabled and the clock gated.
- Configure the unused pins as described in Unused and unbounded pin management.

In the following sections, each feature is deeply described.

9.1.1 Clock Tree planning

The higher emissions in a microcontroller can be typically expected from the clocks used in the chip at the fundamental, second, and third harmonics, in particular.

A careful plan of the clock frequencies is the first measure to achieve the electromagnetic compatibility of a modern application.

It is difficult finding a frequency band not critical in the congested spectrum today. However, some frequency bands are much more critical than others and it should be avoided to have clocks with harmonics falling inside them.

The narrow bands assigned to global navigation satellite systems (GNSS in the following) are between the most critical because of the severe limits imposed. Also, high order harmonics are potentially able to cause limit violations.

Popular frequencies like 160 MHz, 200 MHz, 400 MHz, 800 MHz, 1.2 GHz, 1.6 GHz must be avoided, being able to directly disturb the 1.2 GHz and 1.6 GHz (GLONASS) services.

Being the GNSS bands very narrow, it is enough to choose the clock a few MHz apart to avoid affecting the offended band.

A safe system clock selection for the SPC58xx family is in the range of 162.5 MHz - 192.5 MHz.

Particular attention must be paid to the PLL configuration, being the PLL the IP with the higher frequency operation in the chip and so the closer to the GNSS bands.

As the matter is still in evolution, the application designer is invited to consult the GNSS allocation frequency and plan the clock tree configuration accordingly.

Note: The previously mentioned considerations about the clocks apply to every continuous square wave with a duty cycle close to 50%.

Note: The clock distributed on chip to the IPs, the clock of the communication lines (that is, DSPI-CLK), the oscillator VCO, the clock-out on the package pin are all potential source of unwanted emission to take care of.

9.1.2 Clock gating and IP disable

The clock generation module (MC_CGM) generates reference clocks for all the modules on the chip (IP) and it selects one of the possible clock sources to supply the system clock.

A set of MC_CGM registers controls the clock dividers, which are used to distribute the clock to CPU and peripherals.

Most peripherals on SPC58xx devices can be disabled, while not requested to implement functionality in a specific application. Disabling unused modules results in lower current drawn through the supply, which reduces emissions.

Note: An interesting feature is the possibility to gate the clock blocking the propagation to the disabled modules, further reducing current consumption and emissions.

9.1.3 Frequency Modulation

It is recommended to enable the frequency modulation (spread spectrum) on the clock distributed to the CPUs.

Attention: *FM is not available in SPC582Bx.*

Note: The SPC58xx architecture has two separate PLLs. The key feature of the dual PLL architecture is the ability to drive peripherals from the PLL0 PHI output, which is non-modulated and independent of the core clock frequency. The core and platform clocks are driven by PLL1 PHI frequency modulated output, allowing to distribute a non-modulated clock to the peripherals that are jitter sensitive, like the CAN, and a modulated clock to the logic cores, combining lower emission with proper functionality.

9.1.4 Switching GPIO and driving strength

The output edge rate control (SILUL2.MSCR_IO.B.OERC) specifies the output impedance, drive strength, and slew rate of the associated pin.

Note: It is very important to select the appropriate drive mode for the specific application.

The outputs should be configured so that their driven capability is as slow as possible while still ensuring the performance requirements. Driving the I/O stronger than necessary creates additional emissions.

Note: It is recommended to use the weakest drive strength required from the capacitive load and timing requirements.

The traces transmitting periodic signals must have a solid ground covering the trace path without interruption on the adjacent PCB layer.

Note: The "3W rule" must be respected in any case (the ground should extend three times the height of the trace on the ground layer). The clock output, SIPI/LFAST, DSPI-SCK belongs to this category.

9.1.5 Crosstalk minimization in GPIO

In the EMC tests it has been observed that the pin next to the outputs generating clock with high driving strength can have a significant crosstalk in terms of emission levels.

Since we are talking about a millivolt noise, this does not affect the digital operation state driven, it could eventually pose risks in edge driven operation.

It is suggested to avoid the following usage of the pins next to a clocks-like switching pins:

- Digital inputs working edge driven or sensible to slew rate in any way
- Analog input with low resolution
- GPIO with long routing (prone to inject noise in the PCB)
- GPIO routed to the board I/O connectors (prone to inject noise in the car harness)

9.2 Hardware guidelines

Some recommendations to design a system layout are listed below:

- VDD decoupling capacitors: Decoupling capacitors must be used to decouple all HV and ADC supply pins from GND. To avoid that the decoupling capacitors parasitic inductance couples with the capacitance plane of the supply planes, certain measures of precaution should be taken:
  - Place the capacitors recommended by the datasheet as close as possible to the VDD pins on the SPC58xx device. The bulk decoupling capacitors can be placed further
  - Use power planes or wide traces to connect from the SPC58xx device to the capacitor. Check that the cavity resonances of the VDD/VSS structure do not overlap operating frequencies and their harmonics and that they are correctly dumped
  - Use as many vias as possible in the connections from the SPC58xx device to the capacitors. For example, use at least two vias to connect the positive side of the capacitor to the power plane and to GND.
- Clock generation: To reduce EMC emissions, it is recommended to use the slowest crystal (resonator) together with the internal PLL, thus achieving the proper system operating frequency. The drawback of using a slow crystal is the longer startup time. In order to minimize the number of emissions, generated from the currents flowing in the oscillator circuit at the crystal's fundamental frequency and the susceptibility, the oscillator circuit should be kept as compact as possible. The VCO frequency should be selected as low as possible, compatible with the output frequency wished. Carefully implement the layout recommendation of Oscillator layout recommendations
- Grounding: Usually in a system it is possible to identify different parts of circuits including digital, analog, high current switching circuitry, I/O, and the main power supply. If these different parts of the circuit use isolated grounds, they are connected at a single point. As a general rule, it is not recommended to split the ground on the application board. Splitting the positive supply rail is acceptable and, in some cases, recommendable
- Clock output: The usage of a microcontroller pin to clock other devices on the application board rises the conducted emissions and therefore is not recommended. When such feature is implemented, for a sake of minimum bill of material or other reasons, extra care should be reserved to the decoupling of the interested supply segment. A series resistor could be considered to give some control on rise/fall time. Keep the load capacitance at the minimum on the pin used for that function
- PCB considerations:
  - For single-chip applications, a minimum of four layers is recommended. For expanded mode applications, a minimum of six layers is recommended.
  - There is at least one ground plane.
  - There is at least one power plane. When this is not possible, a star routing is recommended using wide tracks and shorter possible length to the supply source.
  - Avoid structures, which obstruct the flow of current, such as via overlapping (that is, it is not allowed having three via anti-pads to merged). Furthermore, vias should be staggered as much as possible because aligned vias create slots that obstruct the flow of current.

9.2.1 Power supply distribution

The decoupling inside the Power Distribution Network plays a fundamental role in the definition of the EMC performances of the application.

As a starting point, when low emission and low susceptibility are required, it is expected that the decoupling recommendation contained in the datasheet must be fulfilled. The EMC performance of the application depends on a lot of system level parameters and constrains. The most of them are only under the control of the Application Designer.

From an EMC point of view, a relatively flat impedance profile Z(f) is wished.

Considering the constrains it should be at least avoided that impedance peaks overlap critical frequencies in the system like clock, clock/2, clock/4, the main integer harmonics and the clock of the main communication lines.

It is recommended to interconnect the VDD_LV decoupling capacitors with copper areas to reduce the total assembly parasitic inductance. A solid ground, wide enough at least to overlap the VDD_LV copper, should be adjacent in the PCB stack-up.

Some spare unpopulated sites should be made available in the PCB layout. Considering that they are intended to enhance the bulk decoupling in case of need, the placement is not critical.

9.2.2 Deal with power plane resonances

The power distribution via plane or solid areas do a great job in simplifying the layout and minimize the inductance but potentially it has a drawback: the cavity resonances.

In order of dump the cavity resonances that could be created by the couple of planes VDD/VSS, it is recommended to spread on the PCB surface spare 0402 footprints for optional ceramic capacitors.

It is better placing them in a regular grid but it is not strictly mandatory and can be fitted in the layout.

The pre-manufacturing PCB simulation and/or measurements done on the prototype can assist to get better results.

9.2.3 ADC filtering

The datasheet reports the minimum recommended decoupling for each device.

For a better performance it is also recommended to implement an RC filter to clean the voltage reference from conducted noise injected by the board supply, see Figure 17.

Also in this case the spare 0402 sites in the layout are a good precaution on the voltage reference and the ADC supply.

When a large number of channels are used, the ADC clock could inject noise on the power supply at fundamental and harmonics frequencies. It is recommended to forecast a footprint able to host a capacitor of some µF.

9.2.4 Oscillator filtering

The crystal oscillator has a dedicated supply isolated on-die and package from the VDD-HV of the I/O pins.

The datasheet reports the minimum recommended decoupling for each device.

It is expected that the recommendations in External oscillator are carefully implemented.

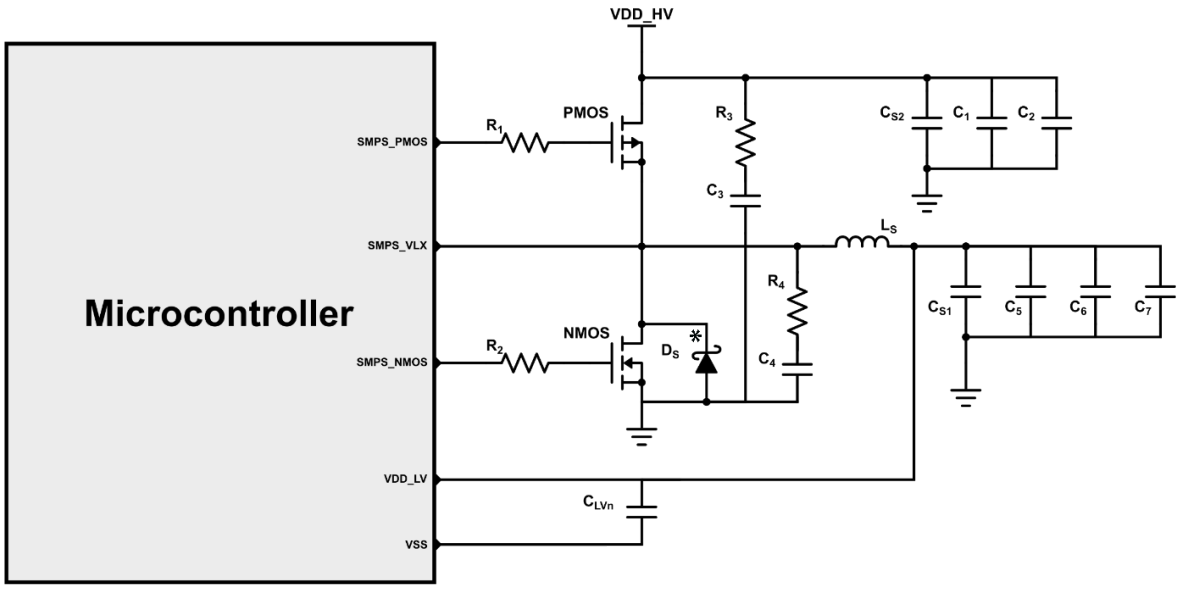
For the better immunity performance, it is suggested to forecast a footprint able to host a capacitor of some uF on the oscillator supply pin.

9.3 SMPS recommendations

While the switching mode power supply offers great benefit in power efficiency and reducing consumption, its high current - fast switching operating mode can create emission problems over a wide frequency range so the basic implementation of the external network shown in the following figure will be expanded with additional components to minimize them.

9.3.1 SMPS layout guidelines

Figure 24. SMPS regulator mode with extra components



* Recommended a ceramic capacitor in range between 1nF to 100nF in parallel with diode Ds. It is also possible to remove the Ds but the ceramic capacitor shall be added.

The components value is a trade-off between cost, efficiency, and EMC performance. The best course of action is usually to leave spare spots on the design and then use an empiric trial-and-fix procedure to find the sweet spot. Some broad suggestions are given below:

- Keep all the connections as short as possible, in order to keep the parasitic impedance as low as possible. – in particular, CS2 must be as close as possible to the SoC.
  - The common ground point must be on the NMOS source.
  - C5 and C6 must have very low equivalent series resistance and inductance, possibly less than 5 mΩ and 600 pH, respectively.
- The capacitors in parallel with CS1 and CS2 with sizes between 47 and 100 nF should have a self-resonance frequency as high as possible, in order to filter out the high frequency components.
- Resistors R1 and R2 form an RC filter with their own parasitic capacitance, and their value is usually between 10 and 100 Ω. Usually a zero Ohm resistor is placed in the PCB layout to allow later usage of R1, R2 in case of need.
- The values of the snubber components (R3, R4, C3, and C4) depend on the parasitic values of the board the layout. Some reasonable values to start from are 10 - 100 Ω for the resistors and 470 pF - 2.2 nF for the capacitors.

The SMPS components should be surrounded with a guard ring extended on all the PCB layers, with frequent vias connecting the layers. VLX and the MOSFET gate traces should also be shielded.

High side power MOSFET (Pmos) and the device's SMPS supply input pin should be as close as possible to the external supply source. Low side power MOSFET (NMOS) and device SMPS ground pin should be as close as possible to PCB ground.

Placing VLX as close as possible to the inductor is recommended, in order to reduce resistance on such path, impacting on SMPS efficiency.

10 Reference schematic

Here are two examples of schematics with and without external ballast.

Figure 25. Schematics with external ballast for SPC58xGx

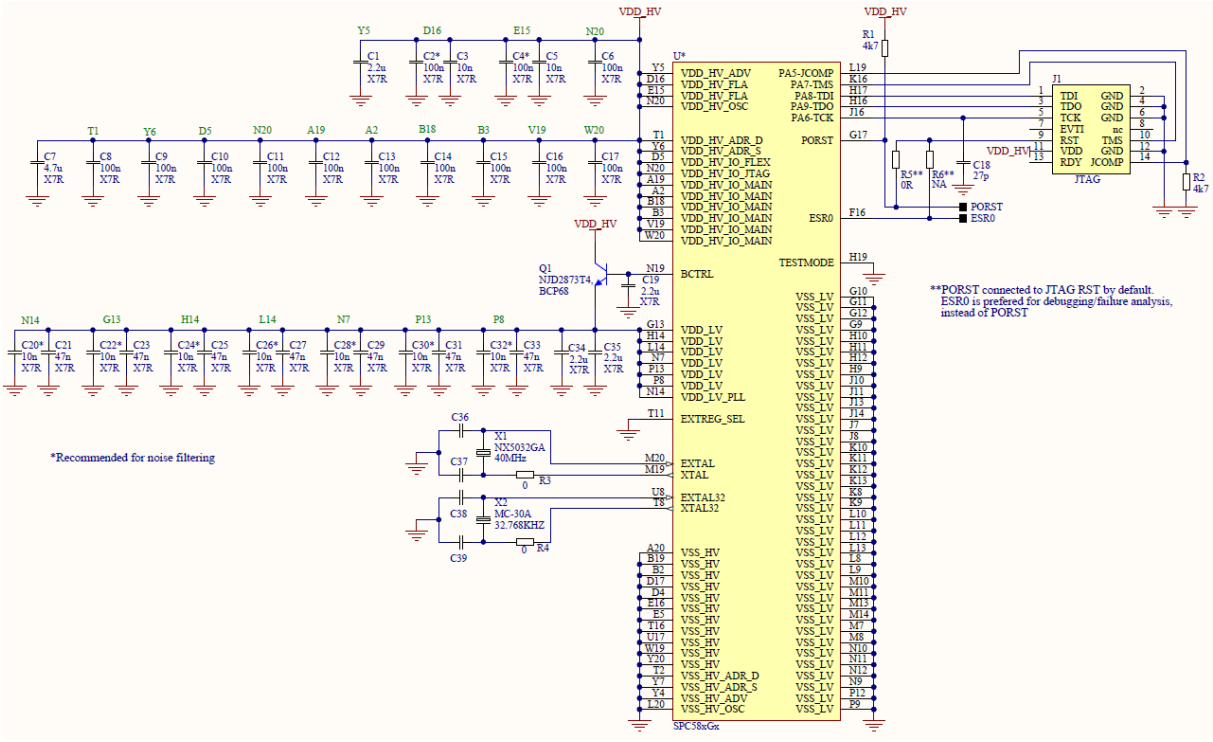
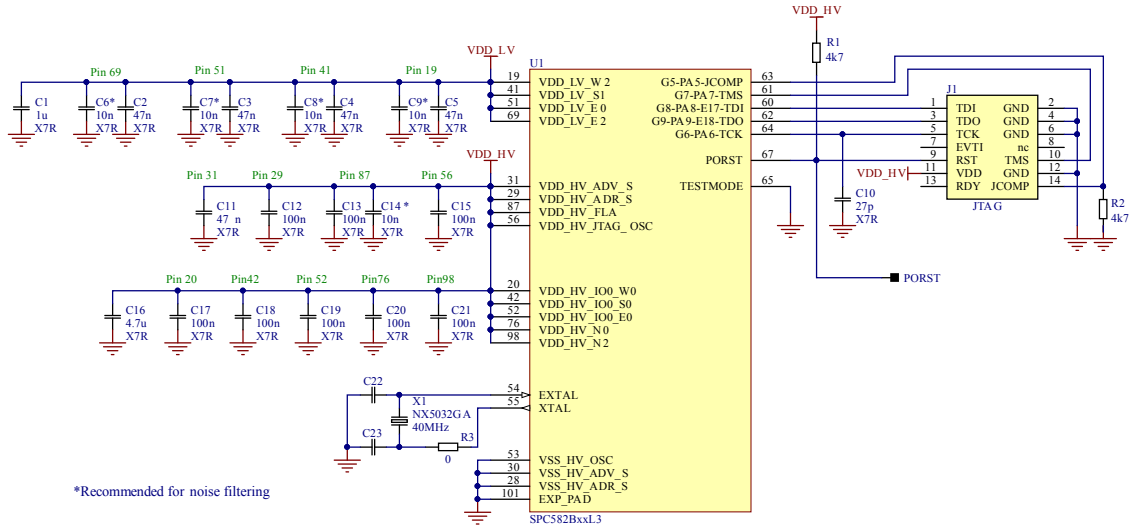


Figure 26. Schematics without external ballast for SPC582B



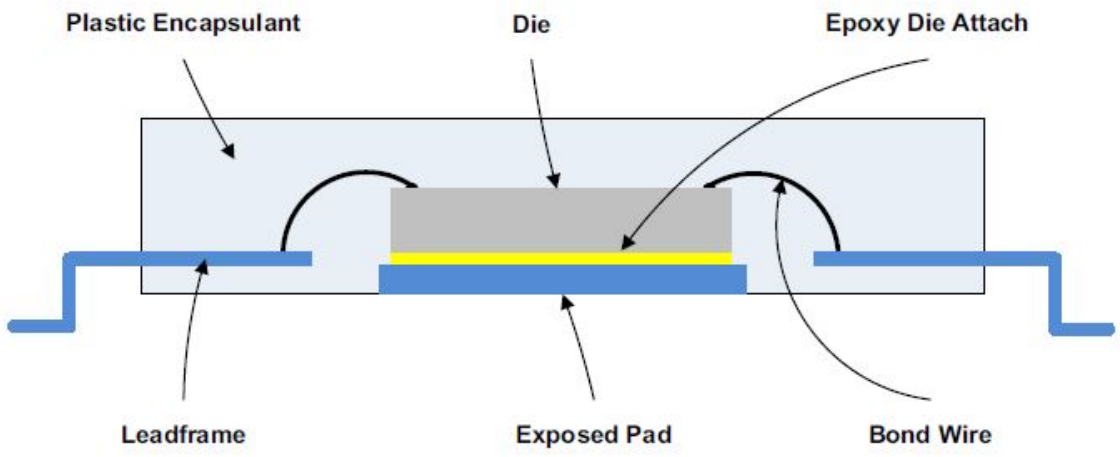
11 Exposed pad

11.1 Introduction

The exposed pad on the bottom of the package provides a very efficient heat sink as well as electrical ground to the PCB board (it also provides a reliable mechanical connection for the chip and a reliable ground plane for EMC purposes). The package structure also provides an extremely low thermal resistance path between the device junction and the exterior of the package. The exposed pad must be soldered to a PCB land or land pattern that has sufficient connections to heat sinking areas of copper on the PCB. These connections should include thermal vias under the exposed pad to bond the land pattern to the heat sinking copper.

Note: The exposed pad must never be connected to a potential other than MCU ground.

Figure 27. eTQFP cross section



11.2 Design guidelines

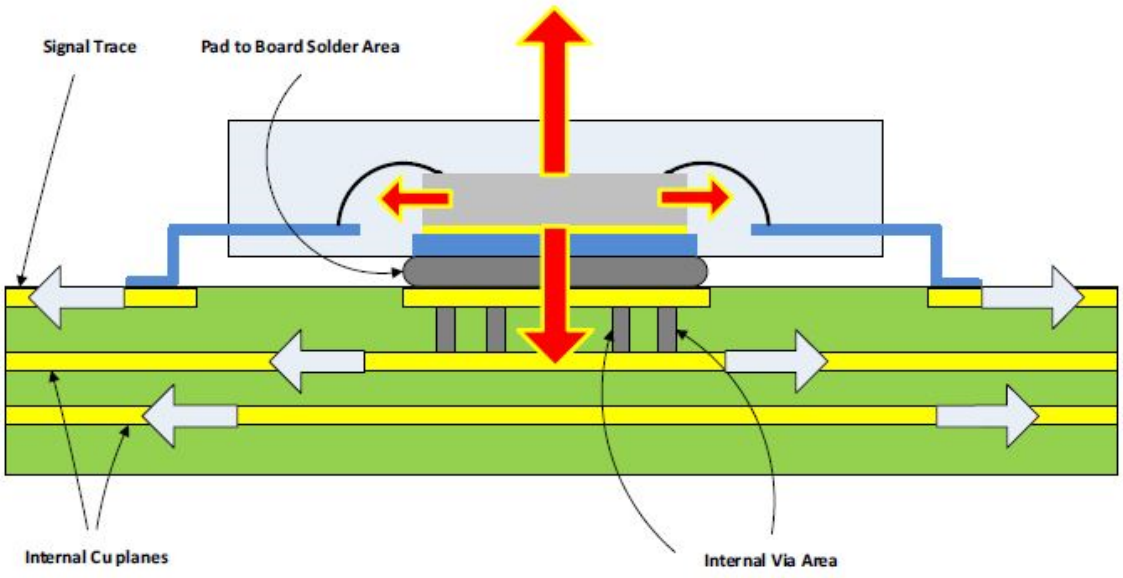
Caution: These recommendations are to be used as a guideline only.

A proper PCB footprint and stencil designs are critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package.

General guidelines for eTQFP packages:

- Lead foot should be approximately centered on the pad with equal pad extension from the toe and the foot.
- Typically, the pad is extended 0.5 mm beyond the eTQFP foot at both the heel and the toe.
- Care should be taken that PCB pads do not extend under the eTQFP body, which can cause issues in assembly.
- Pad width should be approximately 60% of the lead pitch: PCB pad width should be designed at 0.30 mm for this 0.50 mm lead pitch package.

Figure 28. eTQFP cross-section with heat transfer schematic



In order to maximize both heat removal from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad on the package. It is suggested that the solderable area, as defined by the solder mask, should be at least the same size/shape as the exposed pad area on the package to maximize the thermal/electrical performance. The PCB should be designed with a clearance of at least 0.25 mm between the outer edges of the land pattern and the inner edges of the lead pads to avoid any shorts.

11.2.1 Thermal vias

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct heat from the surface of the PCB to the ground planes. The vias act as "heat pipes" and the number required is application specific and dependent upon the package power dissipation as well as the electrical conductivity requirements.

Note: Thermal and electrical analysis and/or testing is recommended to determine the minimum number of vias required.

Typically the maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern based on a 1.2 mm grid. In order to avoid any solder wicking inside the via during the soldering process (which may result in solder voids between the exposed pad and the thermal land), it is also recommended that the diameter of the vias should be between 0.30 to 0.33 mm with 1.0 oz. copper barrel plating. If the copper plating does not plug the vias, the thermal vias can be "tented" with a solder mask on the top surface of the PCB to prevent solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4.0 mils) larger than the via diameter.

Appendix A Reference documents

Table 18. **Reference documents**

Doc name	ID	Title
AN4413	025610	SPC57xx ADC device
AN5484	034218	SPC58x - Configurable PAD - Keeper feature
AN5527	034453	SPC58xx SAR ADC
DS11597	029210	SPC58 2B Line - 32 bit Power Architecture automotive MCU Single core 80Mhz, 1MByte Flash, ASIL-B
DS11701	029439	32-bit Power Architecture microcontroller for automotive ASIL-B applications
DS11620	029264	SPC58 C Line - 32 bit Power Architecture automotive MCU Dual z4 cores 180 MHz, 4 MBytes Flash, HSM, ASIL-B
DS11758	029572	32-bit Power Architecture microcontroller for automotive ASIL-D applications
DS11646	029333	32-bit Power Architecture microcontroller for automotive ASIL-D applications
DS12304	031027	SPC58 H Line - 32 bit Power Architecture automotive MCU Triple z4 cores 200 MHz, 10 MBytes Flash, HSM, ASIL-D
DS11734	029507	32-bit Power Architecture microcontroller for automotive ASIL-D applications
RM0403	027949	SPC58 2B Line - 32 bit Power Architecture automotive MCU z2 core 80 MHz, 1 MByte Flash, ASIL-B
RM0449	030699	SPC584Bx 32-bit MCU family built on the Power Architecture for automotive body electronics applications
RM0407	028117	SPC584Cx/SPC58ECx 32-bit MCU family built on the Power Architecture for automotive body electronics applications
RM0391	027214	SPC58 E/G Line - 32 bit Power Architecture automotive MCU Triple z4 cores 180 MHz, 6 MBytes Flash, HSM, ASIL-D
RM0452	031241	SPC58 H Line - 32 bit Power Architecture automotive MCU Triple z4 cores 200 MHz, 10 MBytes Flash, HSM, ASIL-D
RM0421	028528	SPC58xNx 32-bit Power Architecture microcontroller for automotive ASILD applications

Revision history

Table 19. **Document revision history**

Date	Version	Changes
27-Oct-2016	1	Initial release.
18-Apr-2016	2	Updated Table 2: Power management regulators ,Table 3: Device power management controller external signals . Added Figure 1: External regulator and Figure 6: SMPS Regulator mode, Figure 19: Flow of control. Added Table 3: Device power management controller external signals and Table 4: Device supply relation during power-up/power-down sequence for SPC58EHx, SPC58NHx. Added Figure 5: Standby regulator with internal ballast mode. Updated Section 3.2: Fast external crystal oscillator (4 to 40 MHz), Section 3.2.1: Recommended crystals(4 to 40 MHz), Added Section 3.3.1: Recommended crystals(32 KHz) and Updated Table 7: Reset pads Added Figure 14: Startup reset requirements. Updated Section 4.3: ESR0 pin functionality Updated Section 6: Boot configuration and Section 6.2: Boot mode selection Added Section Table 13.: JTAG pads: JTAG pads and updated Table 14: I/O pad specification descriptions. Updated Section 8.3: Pad configuration after reset, Section 8.5: ISection 8.5: I/O characteristic in STANDBY mode Added Section 8.5.1: PAD-keeper. Updated Section 8.6.1: Section 8.6.1: Unused and unbounded pin management Updated Section Appendix A: Reference documents. Minor text changes.
19-Jun-2018	3	Changed status from St Confidential to St Restricted.
15-Feb-2019	4	Updated Section 3.2: Fast external crystal oscillator (4 to 40 MHz). Updated Section 3.2.1: Recommended crystals (4 to 40 MHz) and Section 3.3.1: Recommended crystals (32 KHz) Updated Section 8.6: General consideration for I/O. Updated Section 8.5.1: PAD-keeper and updated Section 8.7.3: Pads summary in running/standby modes. Updated Section 10: Reference schematic. Added Figure 25: Schematics with external ballast for SPC58xGx and Figure 26: Schematics without external ballast for SPC582B. Minor text changes.
15-Jan-2020	5	Changed status from ST Restricted to public. Added Section 11: Exposed pad and Section 9.3: SMPS recommendations. Updated Section 5.3: ADC performances optimization Minor text changes.
16-Jun-2020	6	Added rpns SPC58EEx,SPC58NEx, SPC584Nx, SPC58ENx, SPC58NNx in all the document. Updated Section 1: Preface. Updated Section 2.2: Power supply scheme and Table 2: Power management regulators . Table 4: Device supply relation during power-up/powerdown sequence for SPC58ENHx, SPC58NHx Updated Table 7: Reset pads Updated Figure 10: Typical layout for VDD/VSS pair Added table Table 8: Voltage monitors configurability and Table 9: Configurable VDs on SPC584Cx, SPC58ECx.

Date	Version	Changes
		Updated Table 10: ADC modules.
23-Feb-2021	7	Added Section 2.2.1: Recommended power-up sequence. Updated: • Section : Introduction • Section 3.2: Fast external crystal oscillator (4 to 40 MHz) • Section 8.6.1: Unused and unbounded pin management • Section 9: EMC guidelines • Section Appendix A: Reference documents • Figure 7: Modules status during reset phases • Figure 9: Failure condition during Brown-out condition. Minor text changes.
11-Oct-2021	8	Updated: • Section 2.1: Introduction • Section 8.5: I/O characteristic in STANDBY mode • Table 10: ADC modules • Figure 18: ADC application setup; • Figure 24: SMPS Regulator mode with extra components.
07-Jul-2022	9	Added Section 4.2.1 Device behavior across resets. Updated Section 9.3.1 SMPS layout guidelines. Minor text changes.

Contents

1 **Preface** 2
2 **Power supplies** 3
2.1 Introduction 3
2.2 Power supply scheme 8
2.2.1 Recommended power-up sequence 10
2.3 Current consumption and voltage regulator 12
2.4 Layout recommendations 13
3 **External oscillator** 14
3.1 Introduction 14
3.2 Fast external crystal oscillator (4 to 40 MHz) 15
3.2.1 Recommended crystals (4 to 40 MHz) 15
3.3 Slow external crystal oscillator (32 kHz) 16
3.3.1 Recommended crystals (32 KHz) 16
3.4 Oscillator layout recommendations 17
4 **Reset** 18
4.1 Introduction 18
4.2 RESET electrical characteristics 18
4.2.1 Device behavior across resets 20
4.3 ESR0 pin functionality 20
4.4 Reset scheme 20
4.5 Power-on reset (POR) and low voltage detectors (LVDs) 21
5 **ADC** 22
5.1 Introduction 22
5.2 Analog Input pins 23
5.3 ADC performances optimization 24
6 **Boot configuration** 25
6.1 Introduction 25
6.2 Boot mode selection 26
6.3 LINFlexD and MCAN pins configuration 26
7 **Debug** 27
7.1 Introduction 27
7.2 JTAG I/O 27
7.3 Nexus Auxiliary port 27
8 **I/Os** 28

8.1 Introduction . . . 28
8.2 I/O types . . . 28
8.3 Pad configuration after reset . . . 29
8.4 Maximum output current . . . 29
8.5 I/O characteristic in standby mode . . . 30
8.5.1 PAD-keeper . . . 31
8.6 General consideration for I/O . . . 32
8.6.1 Unused and unbounded pin management . . . 32
8.7 I/O PAD block diagrams . . . 33
8.7.1 Running mode . . . 33
8.7.2 Standby mode . . . 34
8.7.3 Pads summary in running/standby modes . . . 35
9 EMC guidelines . . . 36
9.1 SPC58xx software configurations . . . 36
9.1.1 Clock Tree planning . . . 36
9.1.2 Clock gating and IP disable . . . 37
9.1.3 Frequency Modulation . . . 37
9.1.4 Switching GPIO and driving strength . . . 37
9.1.5 Crosstalk minimization in GPIO . . . 37
9.2 Hardware guidelines . . . 38
9.2.1 Power supply distribution . . . 38
9.2.2 Deal with power plane resonances . . . 39
9.2.3 ADC filtering . . . 39
9.2.4 Oscillator filtering . . . 39
9.3 SMPS recommendations . . . 39
9.3.1 SMPS layout guidelines . . . 39
10 Reference schematic . . . 41
11 Exposed pad . . . 42
11.1 Introduction . . . 42
11.2 Design guidelines . . . 43
11.2.1 Thermal vias . . . 43
Appendix A Reference documents . . . 44
Revision history . . . 45

List of tables

Table 1. Device summary . . . 1
Table 2. Power management regulators . . . 3
Table 3. Device power management controller external signals . . . 4
Table 4. Device supply relation during power-up/down sequence for SPC58ENHx, SPC58NHx . . . 8
Table 5. Device supply relation during power-up/power-down sequence for SPC584Nx, SPC58ENx, SPC58NNx . . . 9
Table 6. Clock sources . . . 14
Table 7. Reset pads . . . 18
Table 8. Voltage monitors configurability . . . 21
Table 9. Configurable VDs on SPC584Cx, SPC58ECx . . . 21
Table 10. ADC modules . . . 22
Table 11. LINFlexD and MCAN pin configuration . . . 26
Table 12. JTAG signals . . . 27
Table 13. JTAG pads . . . 27
Table 14. I/O pad specification descriptions . . . 28
Table 15. Pins status reset . . . 29
Table 16. Pads summary . . . 35
Table 17. Pins status reset . . . 35
Table 18. Reference documents . . . 44
Table 19. Document revision history . . . 45

List of figures

Figure 1. External regulator . . . 5
Figure 2. Internal regulator with external ballast mode . . . 5
Figure 3. Internal regulator with internal ballast mode . . . 6
Figure 4. Standby regulator with external ballast mode . . . 6
Figure 5. Standby regulator with internal ballast mode . . . 7
Figure 6. SMPS regulator mode . . . 7
Figure 7. Modules status during reset phases . . . 10
Figure 8. Conditions to avoid during MCU power-up . . . 11
Figure 9. Failure condition during brown-out condition . . . 11
Figure 10. Typical layout for VDD/VSS pair . . . 13
Figure 11. Reference oscillator circuit . . . 15
Figure 12. Low power oscillator and resonator connection scheme . . . 16
Figure 13. PCB layout example . . . 17
Figure 14. Startup reset requirements . . . 18
Figure 15. Noise filtering on reset signal . . . 19
Figure 16. ADC System . . . 23
Figure 17. External network and input equivalent circuit . . . 24
Figure 18. ADC application setup . . . 24
Figure 19. Flow of control . . . 25
Figure 20. I/O Pad diagram with analog input . . . 33
Figure 21. I/O Pad diagram without analog input . . . 33
Figure 22. LP pads diagram . . . 34
Figure 23. Not LP pads diagram . . . 34
Figure 24. SMPS regulator mode with extra components . . . 39
Figure 25. Schematics with external ballast for SPC58xGx . . . 41
Figure 26. Schematics without external ballast for SPC582B . . . 41
Figure 27. eTQFP cross section . . . 42
Figure 28. eTQFP cross-section with heat transfer schematic . . . 43