
Low voltage MOSFET technology behavior in FBSOA

Introduction

Modern power MOSFET technologies are characterized by strong improvement in specific $R_{DS(on)}$ and continuous die shrinking. In this way, both switching and on-state losses are optimized. The device can work with outstanding performance in high power and/or high switching frequency systems, maximizing overall efficiency. On the other hand, smaller die size means lower device power capability, which can be risky when it is working in linear mode region, as it must handle high power dissipation. In this critical condition, these high power values could push the device to failure (thermal runaway). The aim of this application note is to explain the V_{DS} and R_{TH} impact on MOSFET thermal stability, with the help of thermal measurements at die level. Furthermore, a complete comparison between ST MOSFET technologies is carried out to highlight the best performances in linear mode.

Nowadays, many systems use power MOSFETs operating mainly in linear mode (or active region). For example, in a fan controller the MOSFET works permanently as constant current source, with the fan connected in a high side position. The fan speed can be adjusted by varying the current value and therefore the MOSFET gate-source voltage (V_{GS}). In other applications, the device can work in linear mode for short time intervals, passing from ON state to OFF state conditions, and vice-versa. The slower this transition, the more critical the device power dissipation; so high power capability is required for MOSFETs working in linear mode. With new MOSFET technologies, huge enhancements in conduction and switching losses have been reached thanks to drastic specific $R_{DS(on)}$ and Q_g minimization, linked to smaller and smaller device die sizes. These features allow the achievement of considerable efficiency gains in high switching-frequency applications. On the other hand, they can be very risky when the MOSFET works in linear mode due to the reduced power capability.

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1 Explanation of power MOSFET linear mode operation and safe operating area

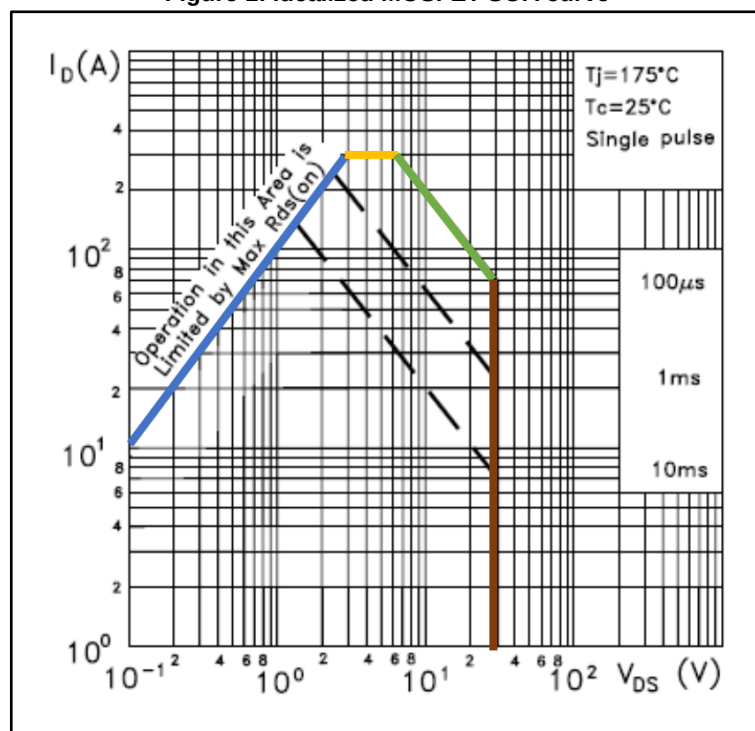
There are basically two main operation modes for a power MOSFET working in ON state:

1. *Ohmic (or triode) region*: linear relationship between drain current (I_D) and drain-source voltage (V_{DS}); the device works as a voltage-controlled resistor

$$\left(I_D = \frac{V_{DS}}{R_{DS(on)}} \right)$$
2. *Saturation (or linear) region*: the drain current is nearly independent of the drain-source voltage (V_{DS}), while it can be adjusted by properly varying the gate-source voltage (V_{GS}) ($I_D = k \cdot (V_{GS} - V_{TH})^2$).

MOSFETs working in linear mode can withstand very high power dissipation levels, due to simultaneous high current (I_D) and the voltage across it (V_{DS}). When a MOSFET works as a switch, it passes continuously from OFF state (high V_{DS} but zero current) to ON state (ohmic or $R_{DS(on)}$ region). During these transients, the device stays in linear mode for a short time interval. If these transitions become slower (i.e. high R_G in the gate driving circuit), the device can dissipate large amounts of energy. For a power MOSFET, the SOA curve (or "safe operating area") defines the maximum value of drain-source voltage (V_{DS}) and drain current (I_D) for correct functioning of the device. In [Figure 1: "Idealized MOSFET SOA curve"](#), an idealized SOA curve for a 30 V power MOSFET is shown.

Figure 1: Idealized MOSFET SOA curve

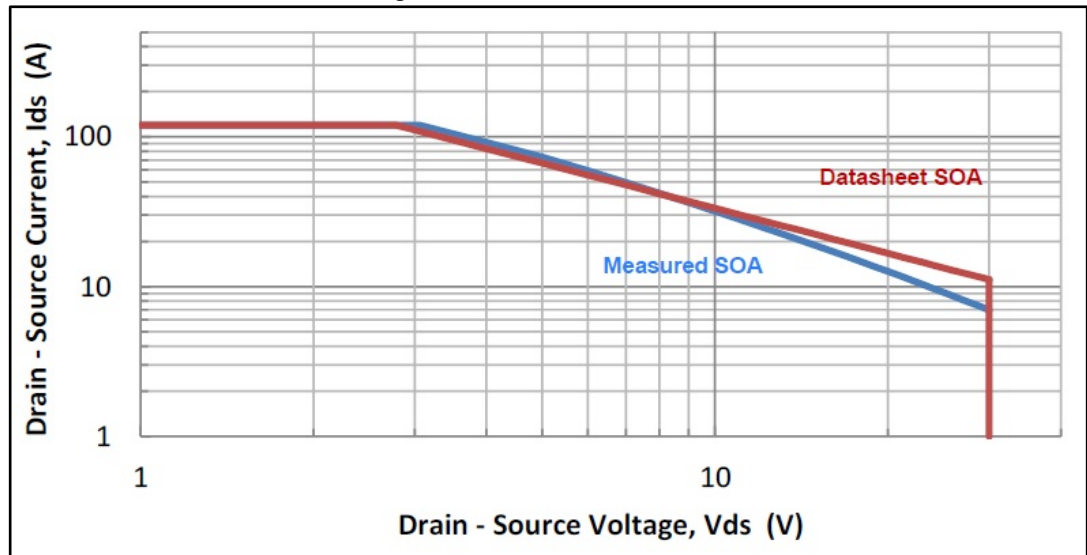


In the above illustration, the colored lines represent the SOA limits:

1. *$R_{DS(on)}$ limit* (blue line): for a given V_{DS} , I_D value is limited by the maximum $R_{DS(on)}$
2. *Maximum I_D limit* (yellow line): maximum current value that the package can manage
3. *Maximum power limit* (green line): maximum power level allowed for $T_J = T_{Jmax}$
4. *Maximum V_{DS} limit* (brown line): SOA limit defined by device breakdown voltage

Unfortunately, real devices show different behavior in the “maximum power” zone of the SOA at high drain-source voltage. This is linked to the “*thermal instability*” phenomenon, which affects power MOSFETs working in linear mode. In fact, when the electrical power generated in the device is larger than the power dissipated, the device is not able to sustain the power pulse. This failure phenomenon can occur even within the idealized or theoretical SOA curve and also at low drain current values [1]. The difference between theoretical and measured SOA for a 30 V device is explained in [Figure 2: “Measured SOA curve”](#):

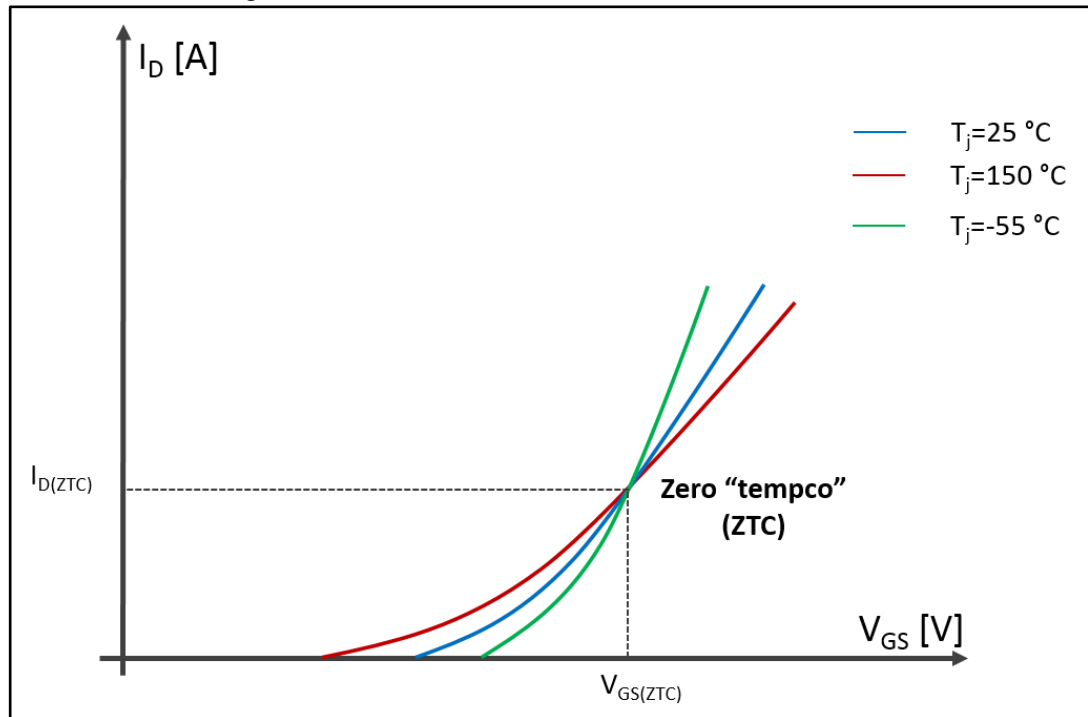
Figure 2: Measured SOA curve



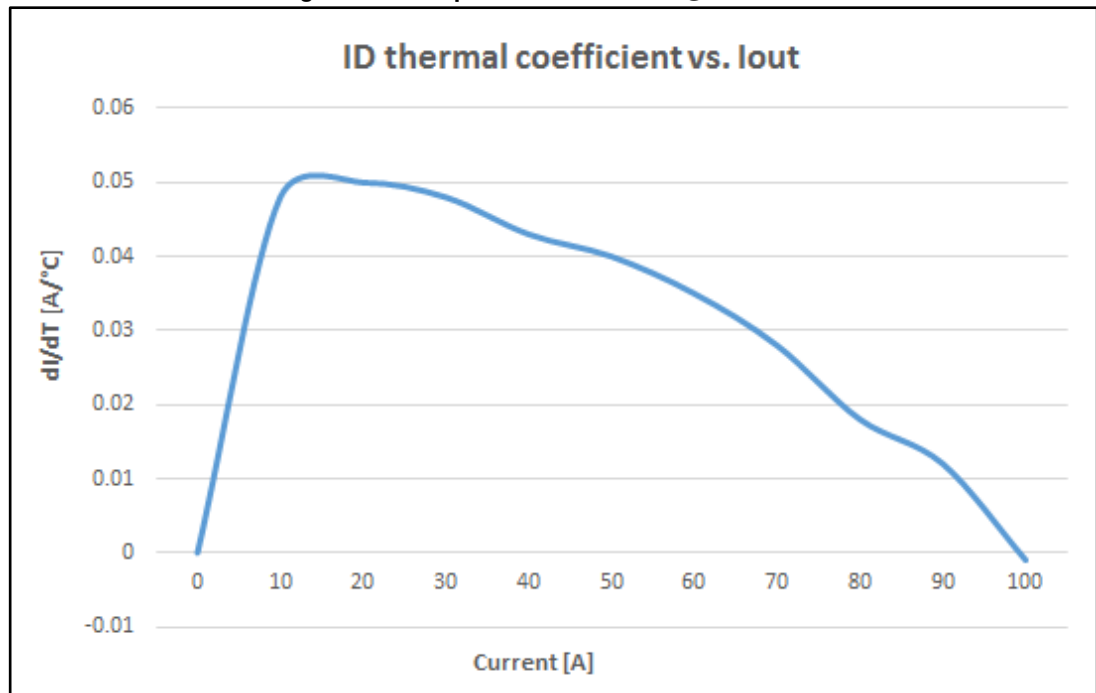
2 Thermal coefficient of drain current (dI_D/dT)

The transfer characteristic of a power MOSFET shows the drain current (I_D) as a function of gate-source voltage (V_{GS}) at a fixed junction temperature (T_J). This curve is a common datasheet parameter. Considering the negative temperature coefficient of the threshold voltage ($\frac{\Delta V_{GS(th)}}{\Delta T}$), the transfer characteristics at three different junction temperatures (-55 °C, 25 °C and 150 °C) are plotted in [Figure 3: "MOSFET transfer curves and ZTC identification"](#).

Figure 3: MOSFET transfer curves and ZTC identification



The three curves intersect at a cross-over point called *zero temperature coefficient* (or “zero tempco”, ZTC). In other words, for $V_{GS} = V_{GS(ZTC)}$, the device current remains stable with the temperature. For $V_{GS} > V_{GS(ZTC)}$, when the device temperature rises, the drain current tends to decrease, reaching thermal stability condition. Conversely, for $V_{GS} < V_{GS(ZTC)}$, the drain current thermal coefficient is positive: when a small die zone becomes hotter than the adjacent area, it conducts more drain current, creating more heat. This, in turn, allows more current to flow due to lower threshold voltage (negative $V_{GS(th)}$ temperature coefficient). Finally, this die area can conduct huge amounts of current, which can push the device to failure (*thermal runaway*) if appropriate limitations have not been implemented. Lower voltage and current values of ZTC reduce the zone with a positive temperature coefficient, increasing the device thermal stability. Deep analysis on MOSFET technologies and silicon characteristics highlight that there is a strict link between ZTC and MOSFET transconductance (g_{fs}): the higher the g_{fs} , the higher the ZTC. Consequently, it is more likely that the device will work in the unstable zone [2]. Modern MOSFET technologies, which guarantee excellent performance in high switching-frequency and high power applications, show ever growing g_{fs} values and tend to be inherently less robust to thermal runaway or hot spot phenomena. In [Figure 4: "ID temperature coefficient @ T = 25 °C"](#) the drain current temperature coefficient as a function of the drain current (T = 25 °C) is depicted.

Figure 4: I_D temperature coefficient @ T = 25 °C

The thermal instability phenomenon occurs when the device cannot dissipate all of the electrical power generated. In other words, if P_G is the electrical (or generated) power and P_D is the thermally dissipated power, thermal instability condition is [3]:

Equation 1

$$\frac{\partial P_G}{\partial T} \geq \frac{\partial P_D}{\partial T}$$

Substituting in equation 1 the relevant formulas for P_D and P_G ($P_D = \frac{\Delta T}{R_{th}(t)}$, $P_G = V_{DS} \cdot I_D$):

Equation 2

$$V_{DS} \cdot \frac{\partial I_D}{\partial T} \geq \frac{1}{R_{th}(t)}$$

Equation 3

$$\alpha_T = \frac{\partial I_D}{\partial T} \geq \frac{1}{V_{DS} \cdot R_{th}(t)}$$

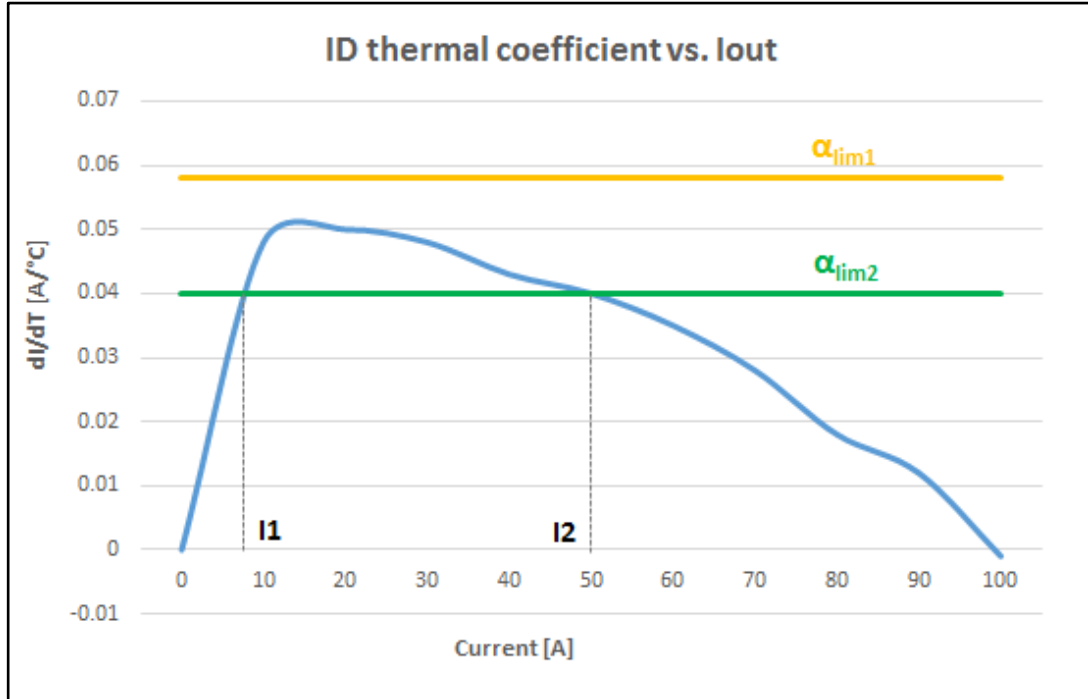
where $R_{th}(t)$ is the time-dependent thermal resistance, while α_T is the drain current thermal coefficient. From equation 3, if V_{DS} and $R_{th}(t)$ are known, the maximum drain current thermal coefficient before failure is given by:

Equation 4

$$|\alpha_T|_{lim} = \frac{1}{V_{DS} \cdot R_{th}^*}$$

From this formula, the impact of V_{DS} and R_{th} on thermal stability is clear: the higher the V_{DS} (R_{th}), the lower the thermal coefficient limit, so the device would be more likely to fall into thermal instability conditions. A simple graphical method of evaluating the onset of thermal instability is to combine the thermal coefficient curve with equations 3 and 4 (see [Figure 5: "Graphical approach to evaluating thermal instability ruggedness"](#)).

Figure 5: Graphical approach to evaluating thermal instability ruggedness

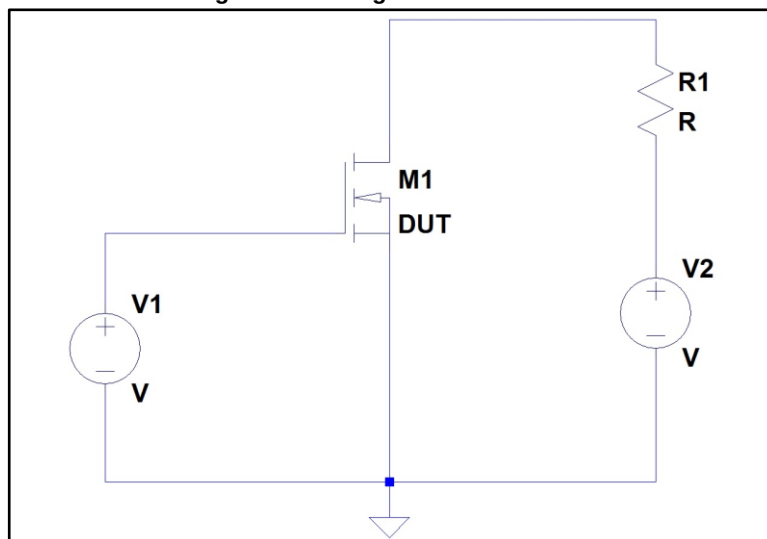


The orange and green lines represent two different “thermal coefficient” limit values (fixing V_{DS} and R_{th}). α_{lim1} is above the thermal coefficient curve within the entire drain current range, which indicates a thermally stable operating point. The green line (α_{lim2}) crosses the thermal coefficient curve at two points: for $I = I_1$, the device enters the thermal instability zone ($\frac{\partial I_D}{\partial T} > \alpha_{lim2}$). At the end of the power pulse, if the device does not fail during thermal transient, the device current is I_2 .

3 Testing circuit

In [Figure 6: "Testing circuit schematic"](#), the testing circuit used to check the device ruggedness in linear mode is illustrated. By varying the voltage sources (V_1 , V_2) and the load resistance (R), it is possible to set the D.U.T. operating point (V_{DS} , I_D).

Figure 6: Testing circuit schematic



Device thermal mapping is achieved by using an infrared thermal imaging microscope ([Figure 7](#)). This performs an exact temperature measurement at die level, catching any current focusing. The device case is placed on a liquid-cooled chill plate (Nitrogen cooled). The liquid cooling is used when air cooling cannot be used due to either thermal or footprint requirements. The plate has a flow path that moves liquid under the device; after the heat is transferred to the liquid, it is taken out of the plate.

Figure 7: Infrared thermal imaging microscope with liquid-cooled plate

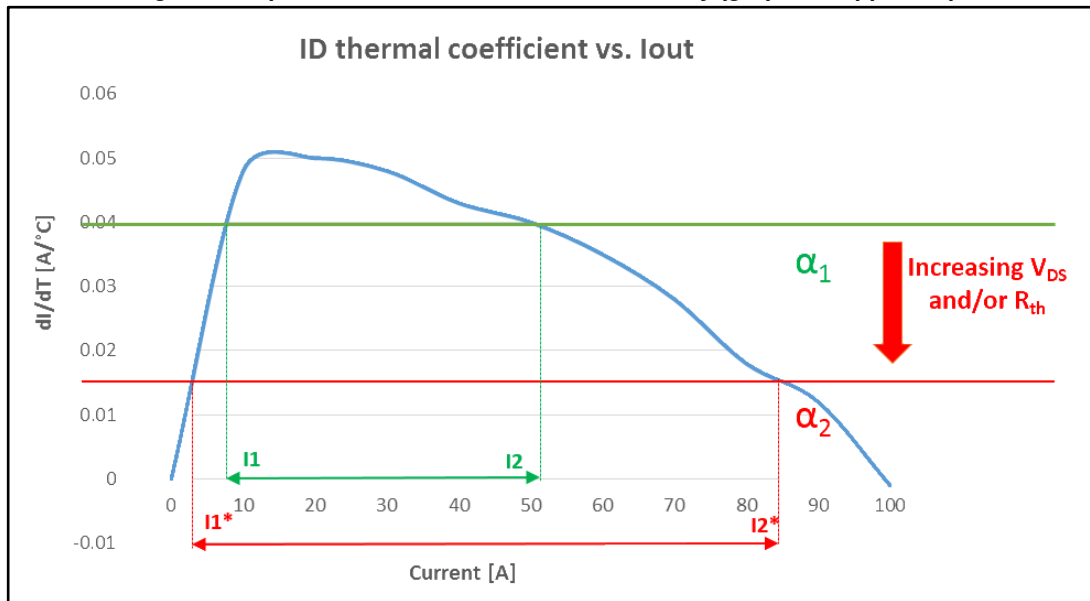


4 V_{DS} and R_{TH} impact on MOSFET thermal stability

Low voltage power MOSFET ruggedness to thermal instability phenomena is strongly affected by two factors:

1. Drain-source voltage (V_{DS})
2. Thermal resistance (R_{TH})

Figure 8: Impact of V_{DS} and R_{TH} on thermal stability (graphical approach)



When V_{DS} and/or R_{TH} increases, the device enters the thermal unstable zone at lower drain current ($I_1^* < I_1$) and moreover the potentially risky current range ($\frac{\partial I_D}{\partial T} > \alpha_{LIM}$) is larger ($(I_2^* - I_1^*) > (I_2 - I_1)$). So thermal instability becomes more likely.

4.1 Drain-source voltage (V_{DS})

The power and heat generated in the device when it works in linear mode increase with drain source voltage level ($P_G = V_{DS} \cdot I_D$). So, if its thermal coefficient curve is fixed, the device will become potentially more unstable at high V_{DS} level. From equation 3, the thermal instability condition can also be written as:

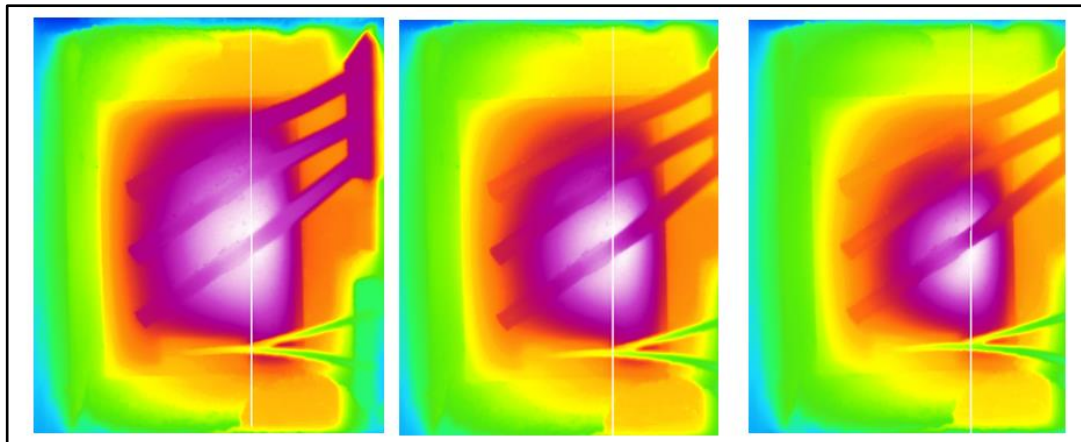
Equation 5

$$V_{DS} \geq \frac{1}{\alpha_T \cdot R_{th}}$$

The higher the α_T , the lower the V_{DS} operating value to preserve the device's thermal stability during linear mode operation. In other words, equation 5 implies that the device cannot work simultaneously with high V_{DS} and high thermal coefficient values ($\alpha_T = \frac{\partial I_D}{\partial T}$). For this reason, the "low I_D and high V_{DS}" region of the device SOA is less safe for linear mode operation. In fact, the low I_D region is typically where power MOSFETs have the highest positive thermal coefficient (see [Figure 4](#)), while by increasing V_{DS}, the power and heat generation grows. Observing the testing circuit shown in [Figure 6: "Testing circuit"](#)

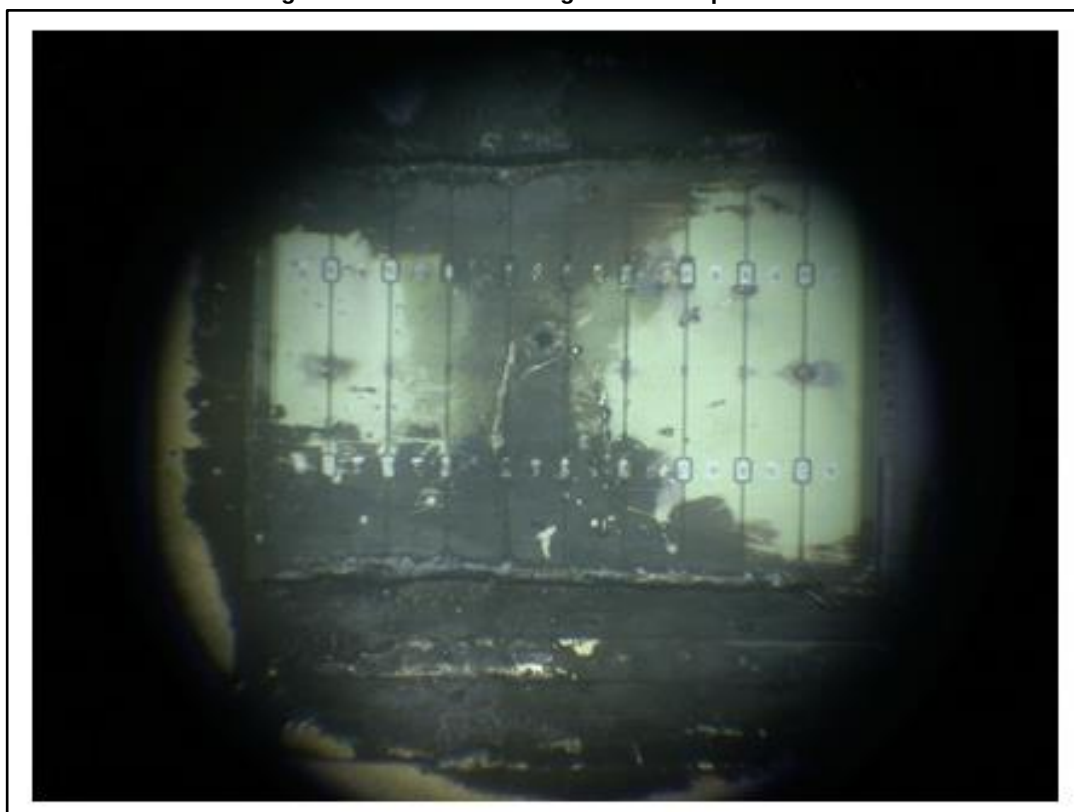
schematic" and the infrared thermal mapping (*Figure 7*), it is possible to analyze the temperature distribution of the die at different V_{DS} levels (*Figure 9*).

Figure 9: Die temperatures @ V_{DS} = 10 V (left), V_{DS} = 15 V (center) and 20 V (right)



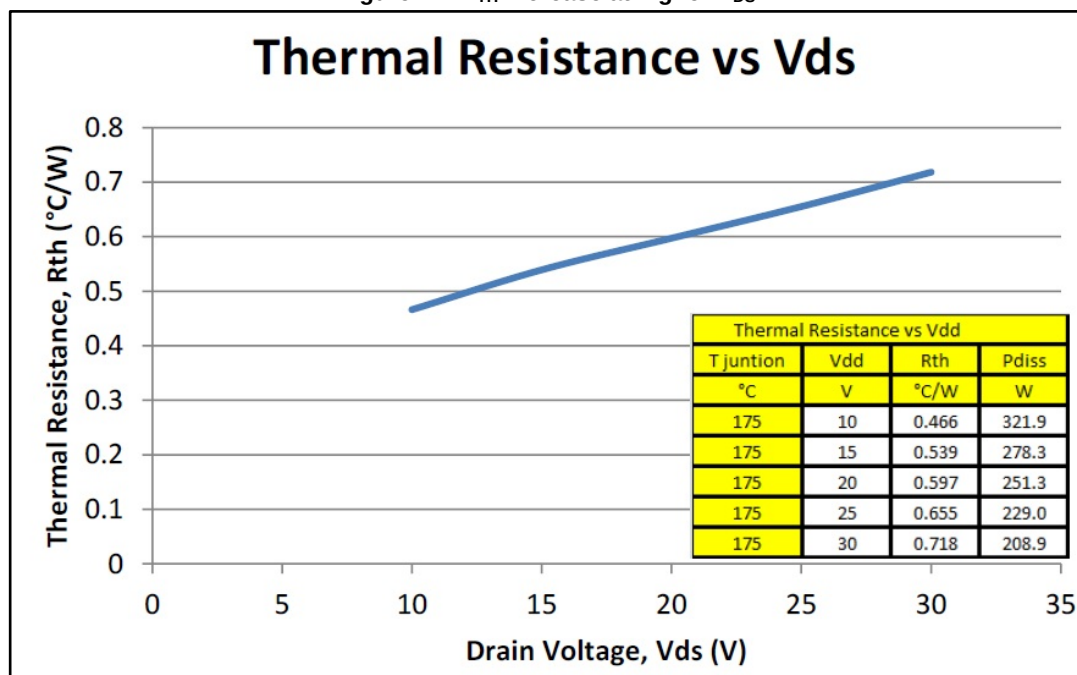
When increasing V_{DS} from 10 V to 20 V, the temperature distribution at die level becomes much less uniform, with a clear focus in a very small die area. This area heats up more than contiguous parts. Here, the localized V_{TH} reduction together with the increase of the drain current (which in turn generates more heat, further reducing the V_{TH}) could cause thermal runaway and device failure (*Figure 10*).

Figure 10: Localized damage after hot spot failure



When V_{DS} increases, due to the current focusing in a small area and therefore the reduction of the device active area, the thermal resistance grows, reducing the power level that the device can safely handle (*Figure 11: "RTH increase at higher VDS"*).

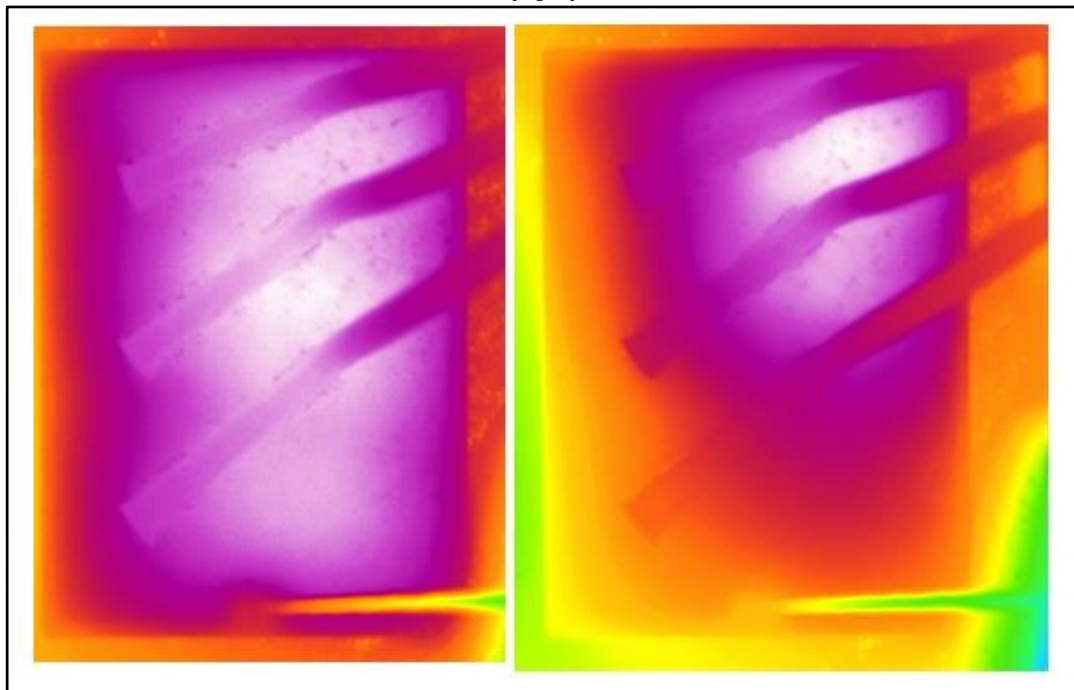
Figure 11: R_{TH} increase at higher V_{DS}



4.2 MOSFET thermal resistance (R_{TH})

The thermal resistance of the semiconductor package (R_{TH}) is the measure of the material's ability to transfer the heat far from the junction (or die) to the ambient or PCB. The lower the thermal resistance, the faster and the better the heat dissipation from the die. Low voltage power MOSFET thermal resistance is dependent on several factors: device characteristics (package type, die size, die thickness, etc.) but some imperfections of the die-attach process (voids) can also dramatically change the device thermal resistance with consequent temperature increases in small areas of the die. So, non-uniformity in die process may generate localized hot spots which may eventually cause device failure. An additional risk factor is the temperature increase. In fact, silicon thermal resistance increases with the temperature, worsening heat dissipation far from the junction. Non-uniformity in the die-attach process together with high temperatures can generate high R_{TH} values in very small die areas, creating the conditions for thermal runaway and device failure (*Figure 12*).

Figure 12: Uniform die temperature (left), local temperature increase due to the R_{TH} issue (right)



5 Characterization of ST MOSFET technologies in linear mode

There is a strict correlation between silicon technology features and MOSFET performance in linear mode. The device ruggedness to thermal runaway and resulting failure can be evaluated by properly combining the SOA curve and drain current thermal coefficient. Furthermore, The R_{TH} trend with V_{DS} and junction temperature provides additional information about device performance in linear mode. Two different technology comparisons are performed between ST MOSFET technologies. In the first, standard trench technology is compared to optimized planar technology for linear mode operation ($BV_{DSS} = 40$ V). In the second, a 100 V device manufactured using the new advanced trench technology is compared to an advanced planar device ([Table 1: "ST D.U.T. main features"](#)).

Table 1: ST D.U.T. main features

Device #	Technology	BV_{DSS} [V]	$RD_{Son,typ}$ [mΩ]
Device #1	Standard trench	>40	1.7
Device #2	Optimized planar (for linear mode)	>40	3.6
Device #3	New advanced trench	>100	2.3
Device #4	Advanced planar	>100	4.5

In the experimental tests, temperature values and distribution at die level are captured at different V_{DS} and/or junction temperatures; the measurement system is reported in [Figure 7: "Infrared thermal imaging microscope with liquid-cooled plate"](#).

- **40 V MOSFET comparison: standard trench vs. optimized planar technology**

The *Standard trench* device shows noticeable current focusing phenomena at $V_{DS} > 10$ V ([Figure 13](#), left side). The reduction of the die active area implies an increase of device R_{TH} and worse power management. On the other hand, *planar technology optimized for linear mode* shows more uniform die temperature (right side) and a softer R_{TH} trend when V_{DS} increases, with better power dissipation capability ([Figure 14](#)).

Figure 13: Die temperature @ $V_{DS} = 10$ V (standard trench technology (left) vs. optimized planar technology (right))

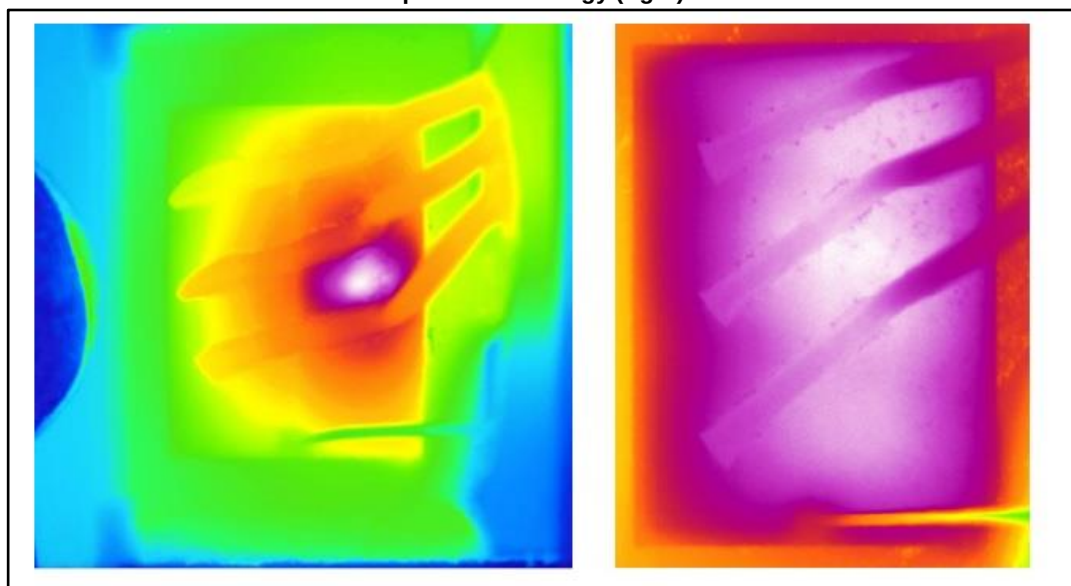
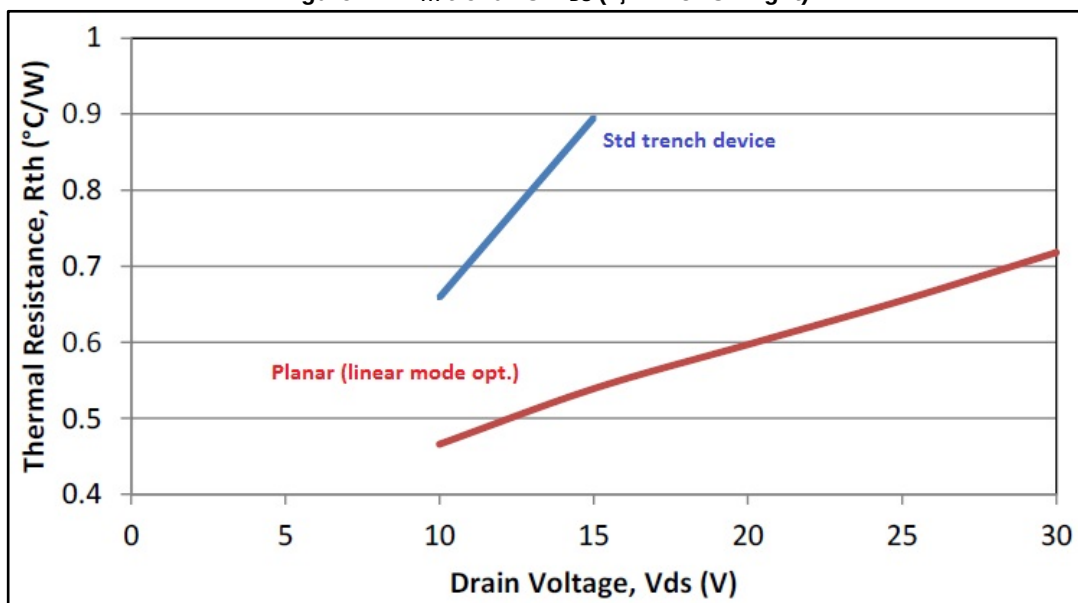


Figure 14: R_{TH} trend vs. V_{DS} ($T_j = 175$ °C - right)



The area between the DC SOA and thermal coefficient curve is the thermal instability zone (Figure 15 and 16): the larger this area is (inside the SOA), the less robust the device will be in linear mode.

Figure 15: Standard trench technology: thermal runaway boundaries

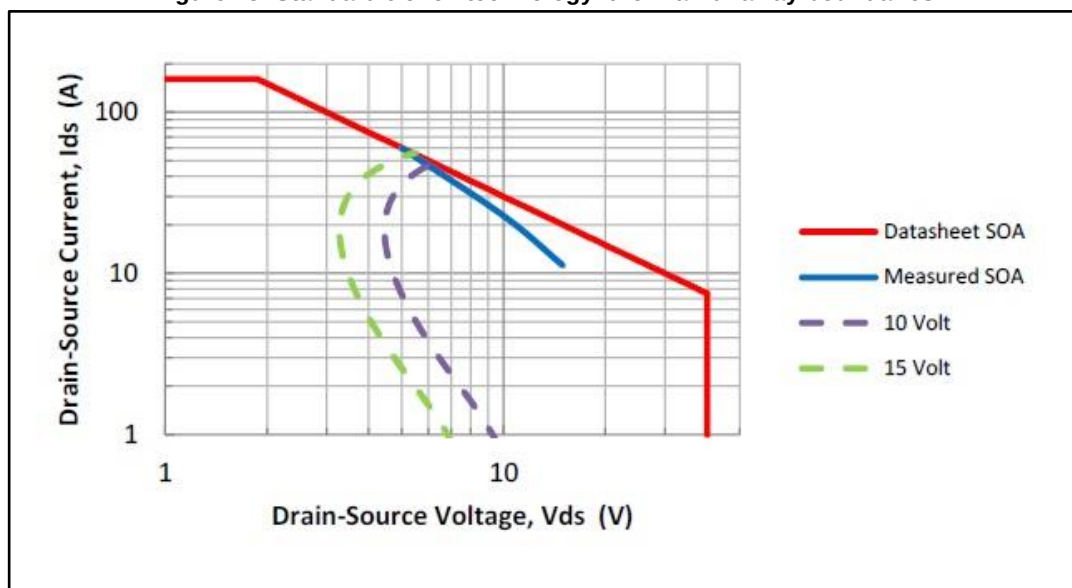
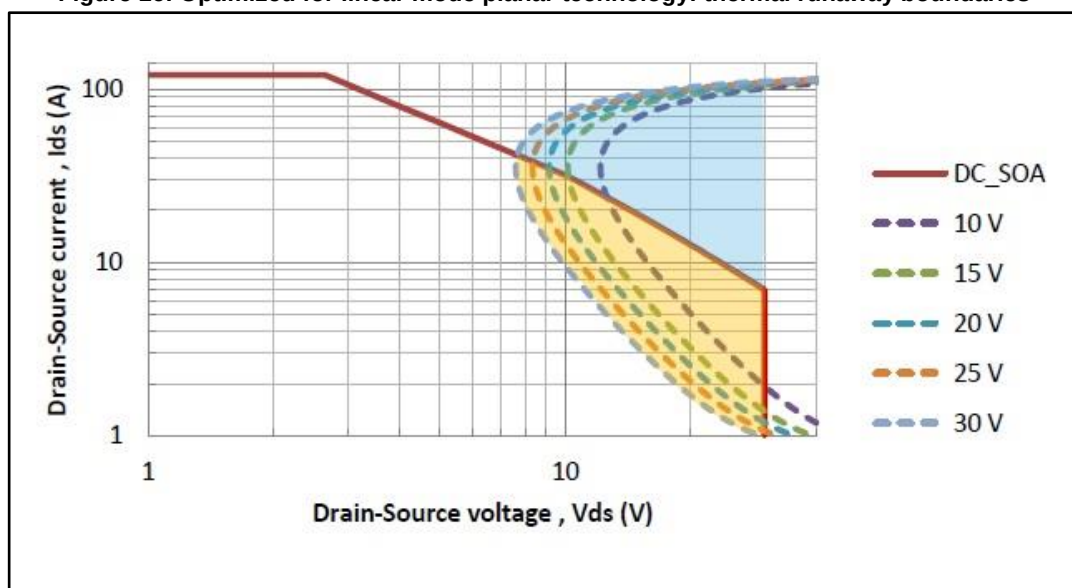


Figure 16: Optimized for linear mode planar technology: thermal runaway boundaries



Standard trench technology is capable of working in linear mode without failure only at low V_{DS} and I_D . It is not possible to test above $V_{DS} = 15$ V ($T > T_{j,max} = 175$ °C). Conversely, optimized planar technology guarantees better performance and higher power dissipation capability in linear mode even at higher voltages.

- 100 V MOSFET comparison: new advanced trench vs. advanced planar technology**

New advanced trench technology outperforms advanced planar technology in linear mode operation, and because of this it is thermally stable for a wider range of operating conditions within the SOA. In Figure 17 and 18 the measured SOA curves for the two technologies are shown.

Figure 17: Measured SOA for advanced planar device

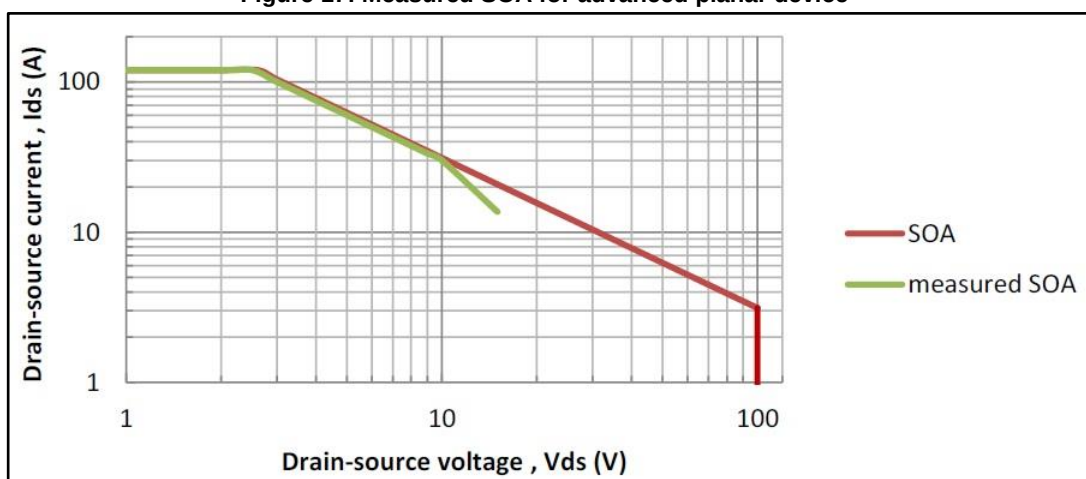
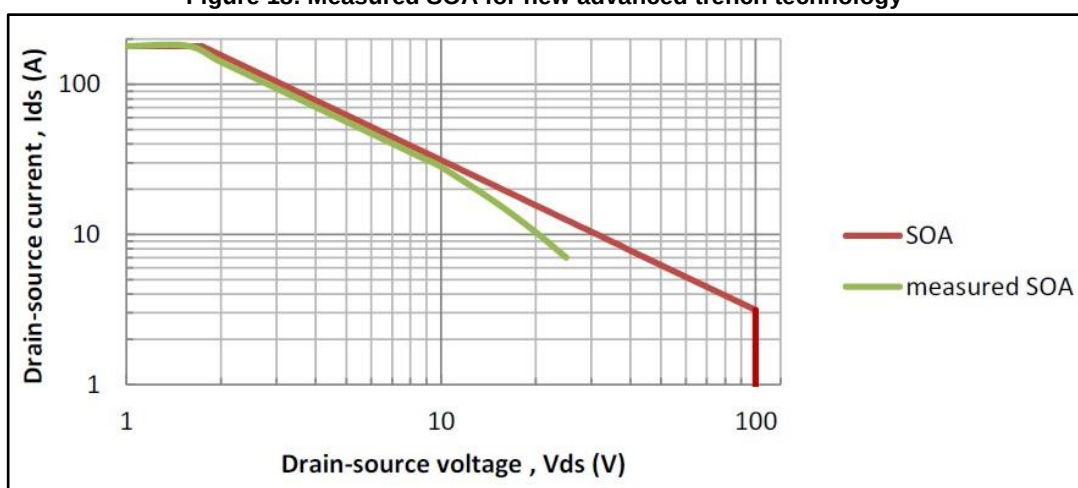
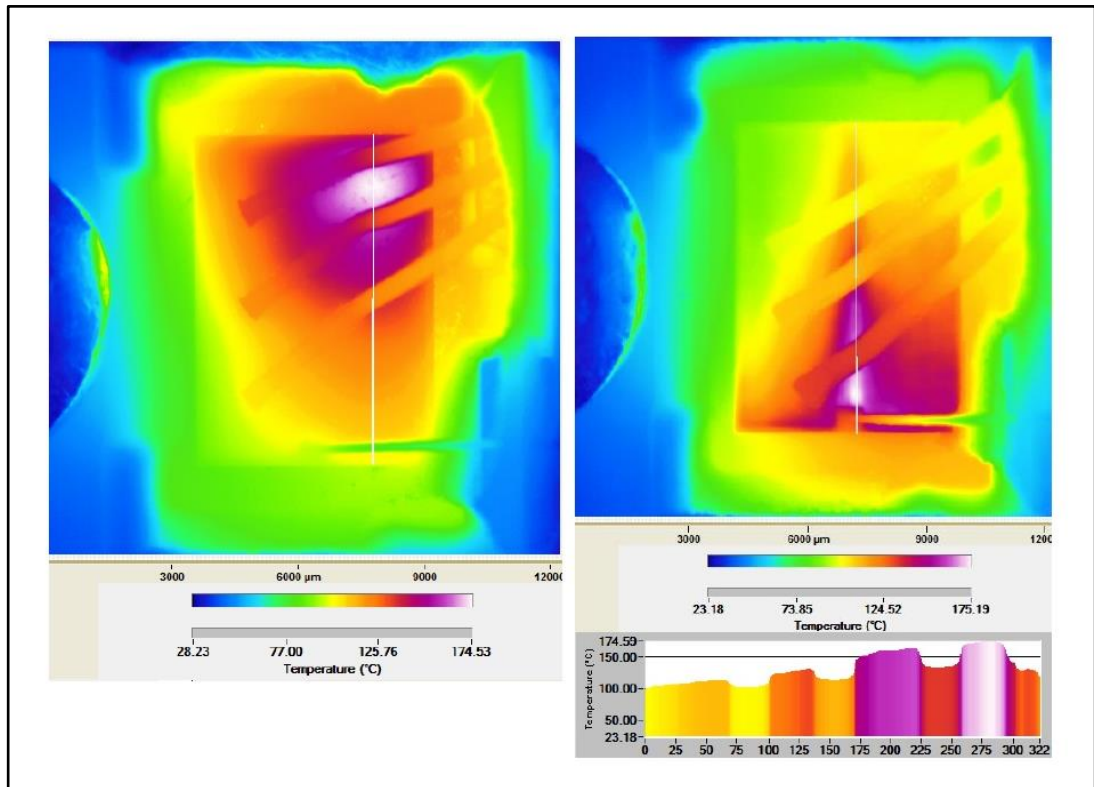


Figure 18: Measured SOA for new advanced trench technology



The new advanced trench device is able to pass the linear mode test up to 25 V, while the advanced planar device fails for $V_{DS} > 15$ V. The figure below shows the relevant thermal images at $V_{DS} = 15$ V (advanced planar device, on the left) and $V_{DS} = 25$ V (new advanced trench, on the right).

Figure 19: Thermal imaging @ $V_{DS} = 15\text{ V}$ (left) and $V_{DS} = 25\text{ V}$ (right)

New advanced trench technology achieves better performance in linear mode thanks also to its slightly higher threshold voltage (V_{TH}), ensuring sooner device turn-off and hence more ruggedness when biased in linear mode. Further technology developments are in progress with the aim to release a dedicated STMicroelectronics “wide SOA” trench technology with robustness and performance in linear mode which is in line with standard planar technology.

6 Summary

Power MOSFETs working in linear mode require correct design at silicon level in order to improve their ruggedness to thermal instability phenomena. In particular, modern silicon technologies optimized for high current and high switching-frequency environments may be less safe in linear mode than the earlier planar technologies, optimized for linear mode, due to high g_{fs} and ZTC values. Therefore, only through dedicated device design, especially for new advanced trench technologies, can performance in linear mode be enhanced, particularly under the worst operating conditions (low I_D and high V_{DS}) and when higher V_{DS} and R_{TH} values create the right conditions for current focusing and hot spot events.

7 References

1. “*Thermal instability of low voltage Power MOSFETs*”, A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor, A. Magri’ – IEEE Transactions on Power Electronics, Vol.15, N.3, May 2000
2. AN-4161, “*Practical considerations of Trench MOSFET stability when operating in linear mode*”, Fairchild Semiconductor
3. “*Analytical model for thermal instability of low voltage Power MOS and S.O.A. in pulse operation*”, P. Spirito, G. Breglio, V. D’Alessandro, N. Rinaldi

8 Revision history

Table 2: Document revision history

Date	Version	Changes
14-Sep-2016	1	Initial release.

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