AN4905
Application note

STEVAL-ISA180V1 12 V/0.6 A isolated flyback demo with VIPer0P

Introduction

The STEVAL-ISA180V1 is a 12 V/0.6 A power supply set in isolated flyback topology using the new VIPer0P innovative IC by STMicroelectronics for building smart power supplies with energy green management.

The evaluation board has the following characteristics:

- five-star energy efficiency when operating with no load ($P_{IN\_no\_load}$ < 18 mW @ 230 V_{AC});
- compliant with the 10% load efficiency and 4-point average active-mode efficiency targets prescribed by the European CoC ver. 5 Tier 2
- meets IEC55022 Class B conducted EMI even with reduced EMI filter
- RoHS compliant

These targets are achieved thanks to the following VIPer0P characteristics:

- 800 V avalanche rugged Power MOSFET
- embedded HV start-up
- 60 kHz fixed switching frequency with jittering
- pulse frequency modulation (PFM) and ultra-low stand-by consumption of the internal circuitry under light load condition
- current mode PWM controller with drain current limit protection for easy compensation
- soft-start

These features facilitate building a complete system design with a minimum component count.

Enhanced system reliability is ensured by:

- pulse skip mode to avoid flux-runaway
- delayed overload protection (OLP)
- max. duty cycle counter
- V_{CC} clamp
- thermal shutdown

All protections, except pulse skip mode, involve auto-restart mode.

Figure 1: STEVAL-ISA180V1 evaluation board (top and bottom views)

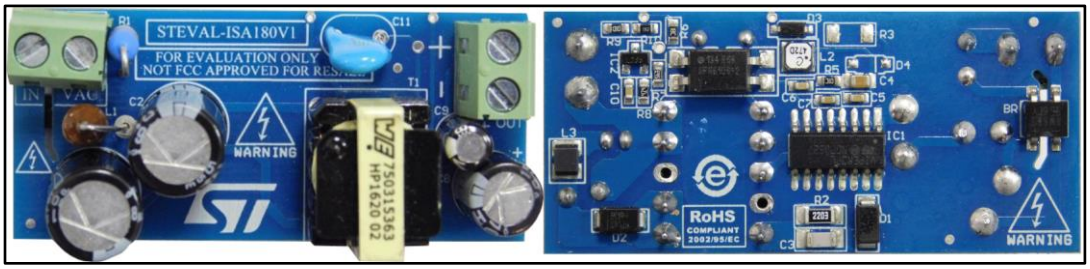

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Table 1: STEVAL-ISA180V1 electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	85 to 265 V_{AC}
Output voltage	V_{OUT}	12 V
Max. output current	I_{OUT}	0.6 A
Output power	P_{OUT}	7.2 W
Precision of output regulation	Δ_{VOUT_LF}	± 5 %
High frequency output voltage ripple	Δ_{VOUT_HF}	50 mV
Max. ambient operating temperature	T_{AMB}	60 ºC
Switching frequency	F_{OSC}	60 kHz

2 Circuit description

The power supply is set in isolated flyback topology.

The input section includes an R1 resistor for inrush current limitation, a BR diode bridge and a filter (L1, C1 and C2) for EMC suppression.

The converter is set in secondary regulation via the FB pin connected to the SGND, which disables the internal error amplifier; the output voltage is regulated through an external error amplifier (IC2) and a voltage divider connected directly to the output terminal, according to:

Equation 1

$$V_{OUT} = V_{ref} \cdot (1 + \frac{R9}{R10})$$

where Vref is the reference value specified in the IC2 datasheet.

The error signal, transferred to the primary by the optocoupler (IC3), drives the VIPer0P COMP which sets the drain peak current value needed to regulate the output voltage.

The C-R-C network from COMP (the error amplifier output) to GND pin provides feedback loop compensation.

At power-up, as V_{DRAIN} exceeds $V_{HVSTART}$, the internal HV current source charges the V_{CC} capacitor, C4, to V_{CCon} , the Power MOSFET starts switching, the HV current source is turned off and the IC is powered by the energy stored in C4.

The VIPer0P can be self-biased or externally biased. It is self-biased when V_{CC} can drop to V_{CCson}, which triggers the HV current source activation until V_{CC} is recharged to V_{CCon}. This results in the sawtooth V_{CC} shape between V_{CCson} and V_{CCon} shown in *Figure 2: "Self biasing Vcc waveforms (D3 diode not connected)"*.

Self-biasing eliminates the need for a transformer auxiliary winding and an auxiliary rectifier (only a capacitor across V_{CC} and GND is needed), but causes higher power dissipation and worse stand-by performance.

The VIPer0P is externally-biased when V_{CC} does not drop to V_{CCson}, by using an auxiliary winding and a small signal diode for rectification. Since the maximum value of V_{CSon} is 4.5 V, the auxiliary turn ratio output has to provide at least an auxiliary 5 V voltage.

Figure 3: "External biasing Vcc waveforms (D3 diode connected)" shows how the V_{CC} shape is fairly constant.

External biasing allows achieving very low input power consumption under no load and light load conditions (less than 18 mW at 230 V_{AC}), thanks to the low IC internal block consumption.

Thus, only external biasing is considered herein.

Figure 2: Self biasing Vcc waveforms (D3 diode not connected)

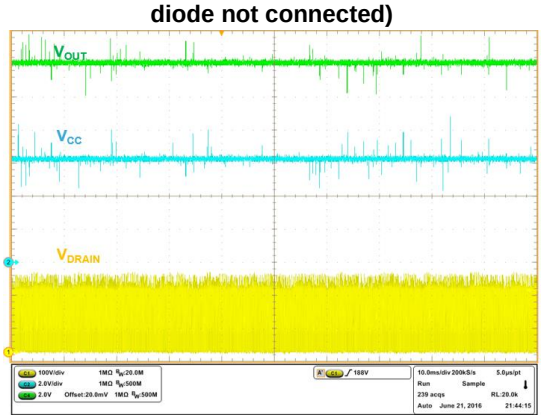
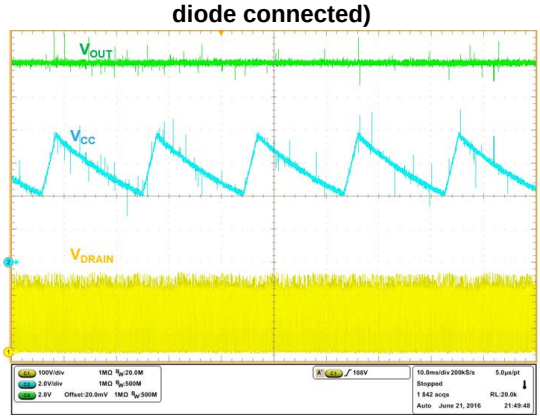


Figure 3: External biasing Vcc waveforms (D3 diode connected)



3 Schematic diagram and bill of materials

Figure 4: STEVAL-ISA180V1 application schematic diagram

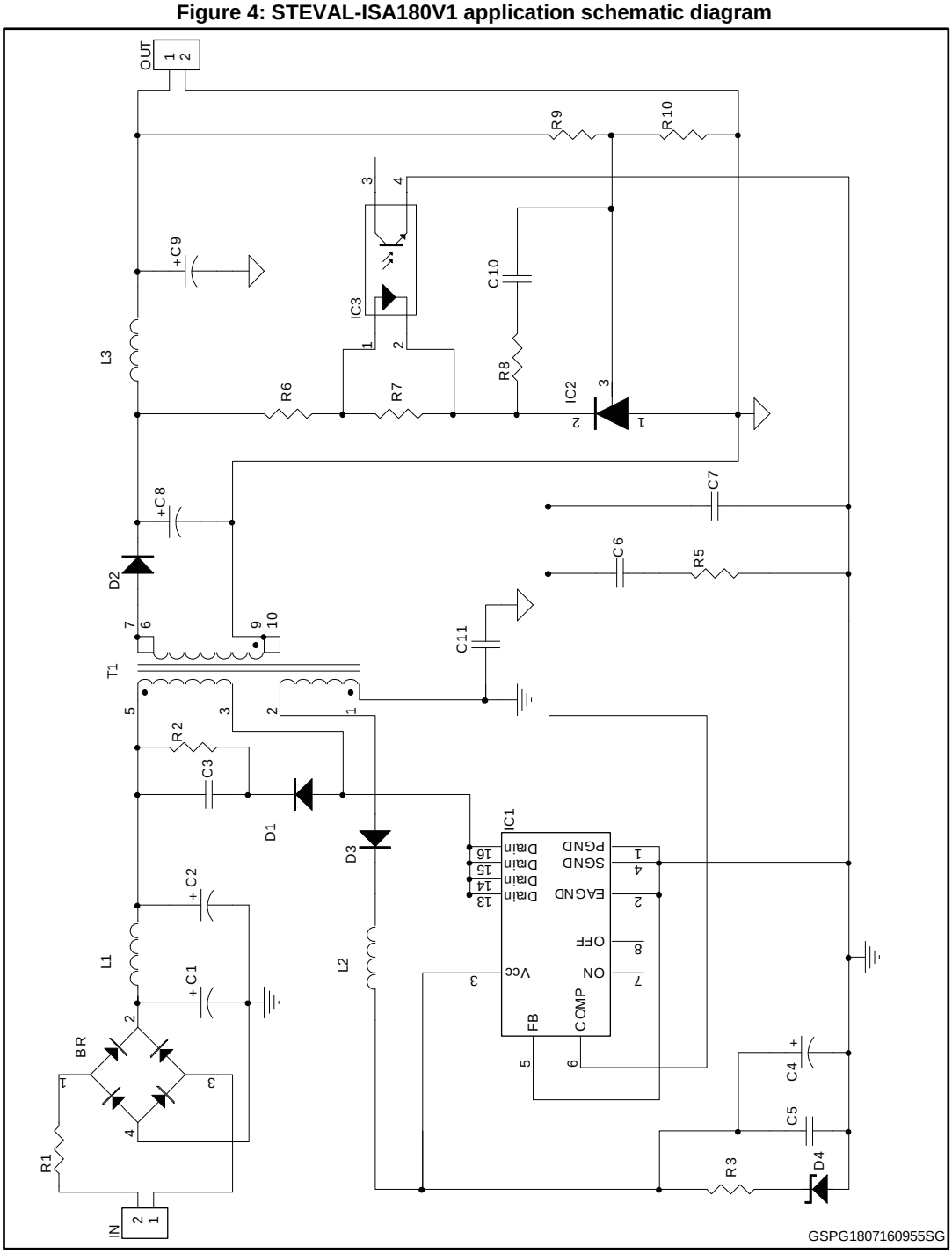


Table 2: Bill of materials

Ref	Order code	Manufacturer	Description	Package
BR	RMB6S	Taiwan Semiconductor	0.5 A-600 V bridge	SOIC-4
R1	ROX1SJ10R	TE Connectivity	10 Ω ± 5% - 1 W	
R2	ERJP08F2203V	Panasonic	220 kΩ ± 5% - 0.33 W	1206
R3			0.33 W resistor (not mounted)	1206
R5			0.1 W resistor (not mounted)	0603
R6	ERJ3GEYJ153V	Panasonic	15 kΩ ± 5% - 0.1 W	0603
R7	ERJ3GEYJ563V	Panasonic	56 kΩ ± 5% - 0.1 W	0603
R8	ERJ3GEYJ474V	Panasonic	470 kΩ ± 5% - 0.1 W	0603
R9	CRCW0603100KFKEA	TE Connectivity	100 kΩ ± 1% - 0.1 W	0603
R10	CRCW060311K5FKEA	Vishay	11.5 kΩ ± 1% - 0.1 W	0603
C1	400BXC6R8MEFC10X16	Rubycon	Elcap 6.8 µF-400 V	Ø10 mm – p 5 mm – 16 mm
C2	400BXC6R8MEFC10X16	Rubycon	Elcap 6.8 µF-400 V	Ø10 mm – p 5 mm – 16 mm
C3	GRM31A7U2J102JW31D	Murata	MLCC capacitor 1 nF-630 V	1206
C4	GRM21BR61E106KA73L	Murata	MLCC capacitor 10 µF-25 V	0805
C5	GRM188R71H104KA93D	Murata	100 nF - 50 V	0603
C6			not mounted	0603
C7	C1608C0G1H102J080AA	TDK	ceramic multilayer capacitor 1 nF 50 V	0603
C8	16ZLH470MEFC8X11.5	Rubycon	Elcap 470 µF-16 V ZLH	Ø8 mm – p 3.5 mm
C9	EEUEB1A101	Panasonic	Elcap 100 µF-10 V EB	Ø5 mm – p 2 mm
C10	GRM188R71H223KA01D	Murata	22 nF - 50 V	0603
C11	DE2E3KY222MA2BM01	Murata	2.2 nF Y2	Ø8 mm – p 5 mm
D1	MRA4007T3GOSCT-ND	ON semiconductor	general purpose diode 1 A/ 1000 V	DO-214AC, SMA
D2	STPS2H100A	STMicroelectronics	Power Schottky 2 A-100 V	SMA-2
D3	BAT46ZFILM	STMicroelectronics	Signal Schottky 0.15 A-100 V	SOD-123

Ref	Order code	Manufacturer	Description	Package
D4			Zener diode (not mounted)	SOD-123
T1	750315363r00	Wurth	flyback transformer	
IC1	VIPer0PLD	STMicroelectronics	offline primary controller, 60 kHz	S016N
IC2	TS432ILT	STMicroelectronics	low voltage adjustable shunt ref.	SOT23-3
IC3	SFH6106-2T	Vishay	optocoupler	SOP-4
L1	B82144A2105J	Epcos	1 mH ± 5% axial, 200 mA Icc, 3,8Ω Rcc	Axial
L2	LPS3008-472ML	Coilcraft	4.7 µH	LPS3008
L3	ME3220-472ML	Coilcraft	4.7 µH	ME3220
IN		TE Connectivity	two-way connector	
OUT		TE Connectivity	two-way connector	

4 Board layout

Figure 5: Layout (complete)

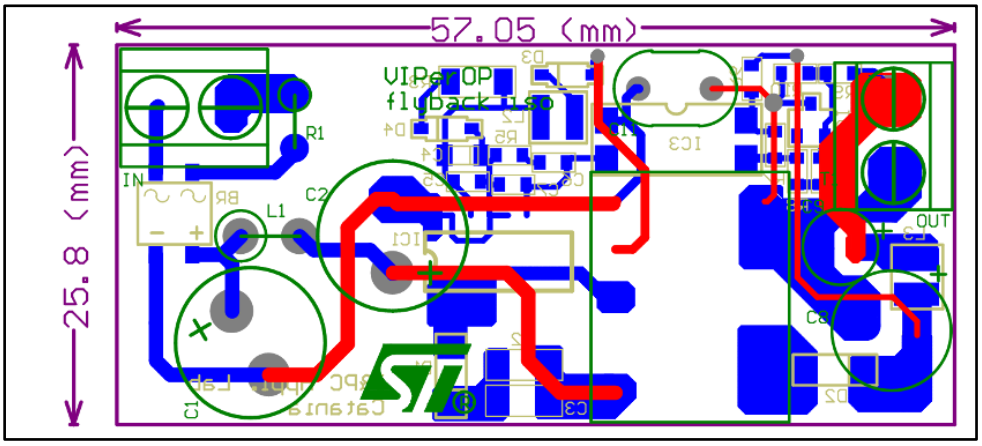


Figure 6: Layout (top layer plus top overlay)

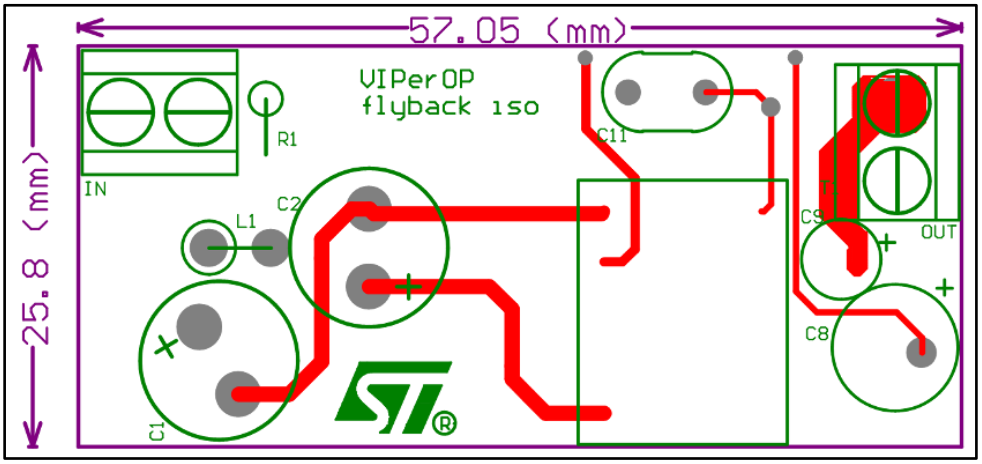
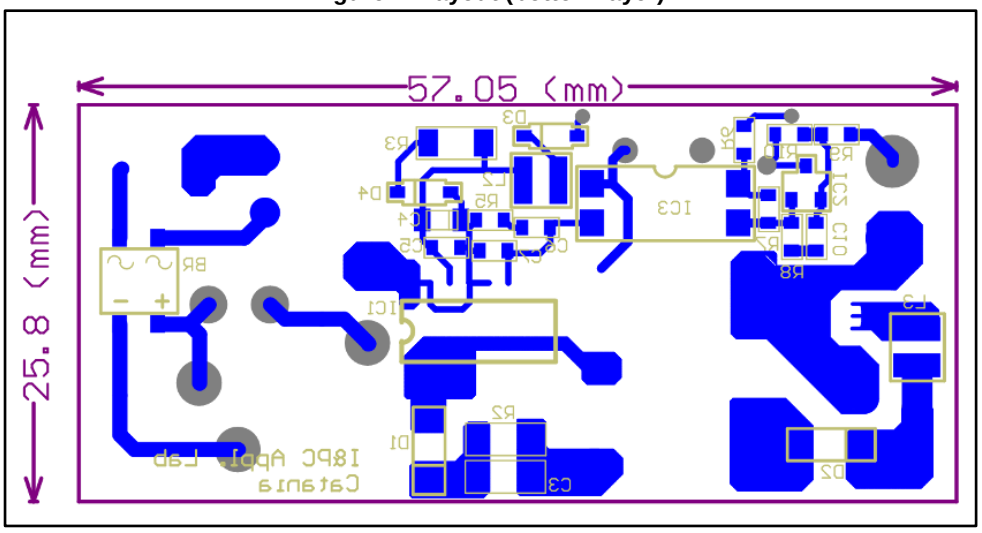


Figure 7: Layout (bottom layer)



5 Transformer

Table 3: Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Wurth	
Order code	750315363	
Primary inductance	2.0 mH ± 20%	5 – 3, 10 kHz, 100 mV
Leakage inductance	100 µH typ, 150 µH max	tie(1+2, 6+7+9+10),100 kHz, 100 mV
Primary to aux turn ratio	11.33:1, ±1%	(5 - 3):(1 - 2)
Primary to sec turn ratio	5.86:1, ±1%	(5 - 3):(10 – 7), tie (6+7, 9+10)
Saturation current	0.625 A max	20% roll off from initial, T_{AMB} = 20 ºC
Primary DC resistance	4.75 Ohms ± 10%	5 – 3, T_{AMB} = 20 ºC
Secondary DC resistance	1.4 Ohms ± 10%	1 – 2, T_{AMB} = 20 ºC
Dielectric 1 -10	Tie (2+3), 3750 V_{AC}, 1 sec	3000 V_{AC}, 1 minute
Dielectric 1 -5	625 V_{AC}, 1 sec	

Figure 8: Transformer: electrical diagram

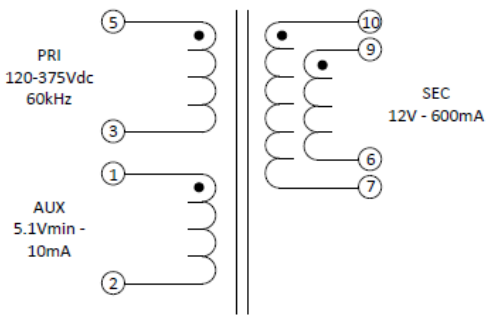


Figure 9: Transformer: pin distances in mm (bottom view)

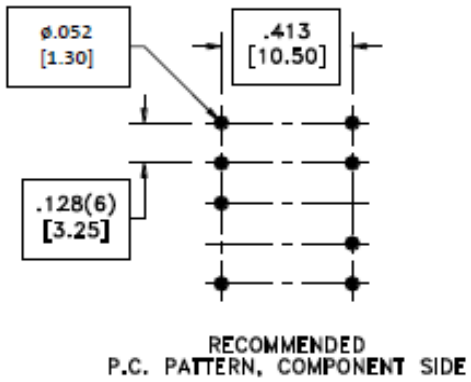
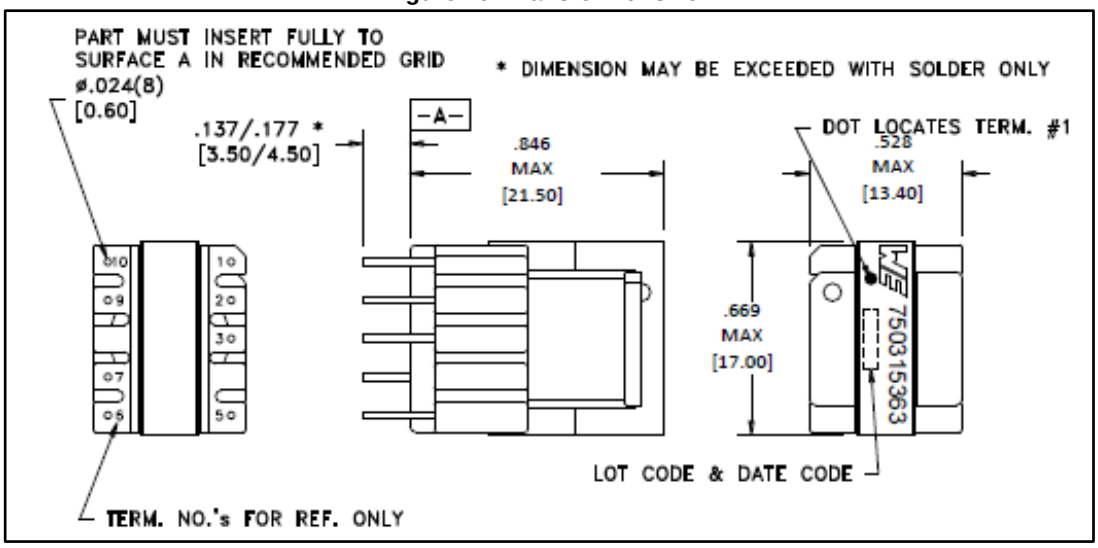


Figure 10: Transformer size



6 Testing the board

6.1 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% maximum load at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies (those housed separately from the end-use devices they are powering) need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion, whereby the active mode efficiency must be above 80.19% for a power throughput of 7.2 W (CoC5 tier2, January 2016).

The DOE (department of energy) recommendation is another standard whose active mode efficiency requirement for the same power throughput is 80.01%.

The following table shows the compliance of the STEVAL-ISA180V1 with the above standards.

Table 4: Active mode efficiency

CoC5 Tier 2 req. for P_{OUT} = 7.2 W	DOE req. for P_{OUT} = 7.2 W	STEVAL-ISA180V1 performance
80.19%	80.01%	80.48% (V_{IN} =115 V_{AC})
		81.18% (V_{IN} = 230 V_{AC})

6.2 Light load performance

CoC5 also includes requirements on the active mode efficiency when the output load is 10% of the nominal output power.

The STEVAL-ISA180V1 is compliant with Tier 2 requirements, as shown in the table below.

Table 5: CoC5 requirement and STEVAL-ISA180V1 performance at 10% output load

CoC5 efficiency requirements - P_{OUT}/10 (P_{OUT} = 7.2 W)	STEVAL-ISA180V1 performances
70.19%	78.45% (V_{IN} = 115 V_{AC})
	71.58% (V_{IN} = 230 V_{AC})

In version 5 of the Code of Conduct, the power consumption of the power supply when it is not loaded is also considered.

The compliance criteria for EPS converters with nominal output power below 49 W and the STEVAL-ISA180V1 no-load input power consumption measurements at nominal input voltages (115 V_{AC} and 230 V_{AC}), are shown in the following table.

Table 6: CoC5 energy consumption criteria for no load and STEVAL-ISA180V1 performance

Maximum no load consumption (0.3 W < Pno < 49 W)	STEVAL-ISA180V1 no load consumption
75 mW	11.8 mW (V_{IN} = 115 V_{AC})
	17.22 mW (V_{IN} = 230 V_{AC})

Depending on the equipment supplied, there are several criteria to measure the performance of a converter. In particular, one requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW.

The following table shows how the STEVAL-ISA180V1 board satisfies this requirement, along with efficiency figures for P_{OUT} = 25 mW and P_{OUT} = 50 mW light load conditions.

Table 7: Light load performance

V_{IN} [V_{AC}]	efficiency [%]		
	at P_{OUT} = 25 mW	at P_{OUT} = 50 mW	at P_{OUT} = 250 mW
115	51.4	59.0	70.4
230	42.0	50.0	66.2

The following table provides data for another output power (or the efficiency) criterion, when the input power is one watt.

Table 8: Efficiency at P_{IN} = 1 W

V_{IN} [V_{AC}]	efficiency at P_{IN} = 1 W [%]
115	77
230	69

6.3 Typical waveforms

Drain voltage and current waveforms under full load are shown in *Figure 11: "Waveforms at 115 V_{AC}, full load"*(at 115 V_{AC}), in *Figure 12: "Waveforms at 230 V_{AC}, full load "* (at 230 V_{AC}), in *Figure 13: "Waveforms at 90 V_{AC}, full load"* (at 90 V_{AC}) and in *Figure 14: "Waveforms at 265 V_{AC}, full load"* (at 265 V_{AC}).

Figure 11: Waveforms at 115 V_{AC}, full load

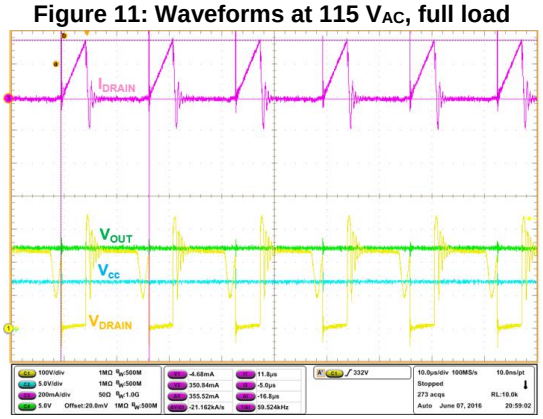


Figure 12: Waveforms at 230 V_{AC}, full load

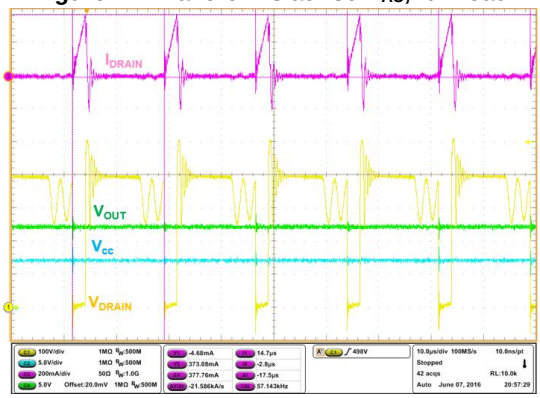


Figure 13: Waveforms at 90 V_{AC}, full load

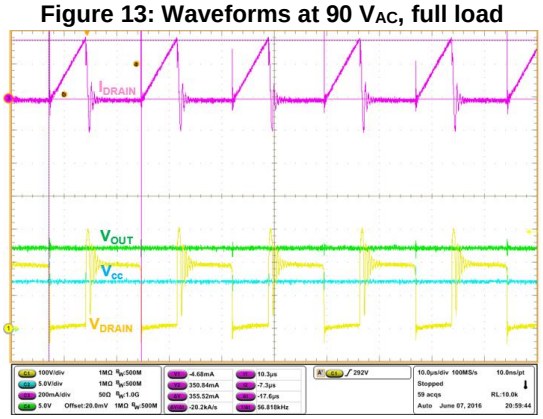
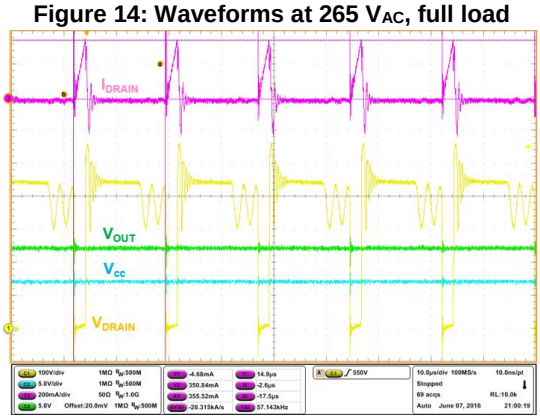


Figure 14: Waveforms at 265 V_{AC}, full load

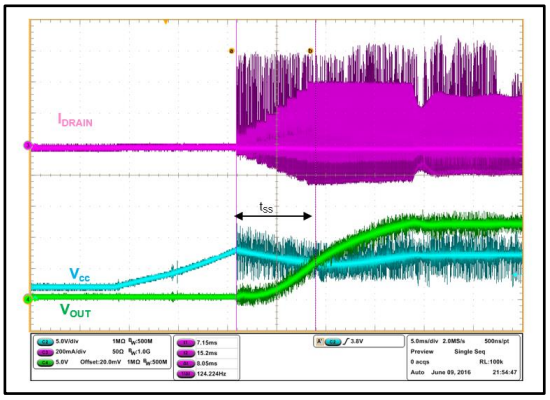


7 ICs Features

7.1 Soft start

The device features an internal soft-start function, which progressively increases the cycle-by-cycle current limitation set point from zero to I_{DLIM} in eight 50 mA steps. This limits the drain current during the output voltage increase and therefore reduces the stress on the secondary diode. The t_{ss} soft-start time (the time necessary to the current limitation set-point for reaching its final value) is internally fixed at 8 ms. This function is activated at the converter start-up and at restart after a fault event.

Figure 15: Soft start phase



7.2 Overload protection (OLP)

During an overload or short circuit, the drain current reaches I_{DLIM}. For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the fault is maintained for time t_{OVL} (50 ms typical, set internally) (see *Figure 16: "OLP: fault applied during steady state operation (t_{OVL})"*): the power section is turned off and the converter is disabled for time $t_{RESTART}$ (1 s typ.). After this time, the IC resumes switching and, if the fault is still present, the protection continuously repeats this sequence (see *Figure 17: "OLP: fault applied during steady state operation ($t_{RESTART}$)"*). This ensures restart attempts of the converter at a low repetition rate so that it works safely with extremely low power throughput and avoids IC overheating due to repeated overload events.

Moreover, every time the protection is tripped, the internal soft start-up function is invoked at restart to reduce the stress on the secondary diode (see *Figure 18: "OLP: fault maintained (t_{SS} and t_{OVL})"*).

The IC resumes normal operation when the short is removed. If the short is removed during t_{SS} or t_{OVL}, before the protection is tripped, the counter decrements each cycle down to zero and the protection is not tripped. If the short circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before resuming switching (see *Figure 19: "OLP: fault removed and autorestart"*).

Figure 16: OLP: fault applied during steady state operation (t_{OVL})

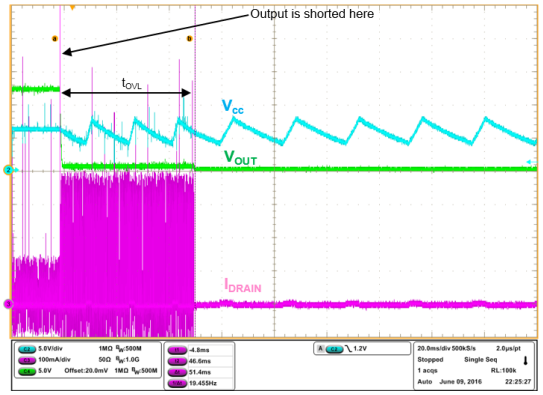


Figure 17: OLP: fault applied during steady state operation ($t_{RESTART}$)

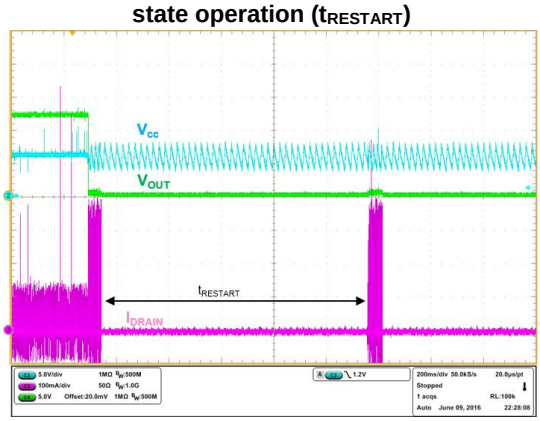


Figure 18: OLP: fault maintained (t_{SS} and t_{OVL})

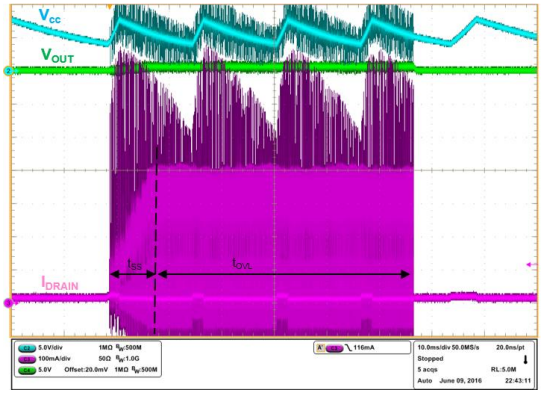
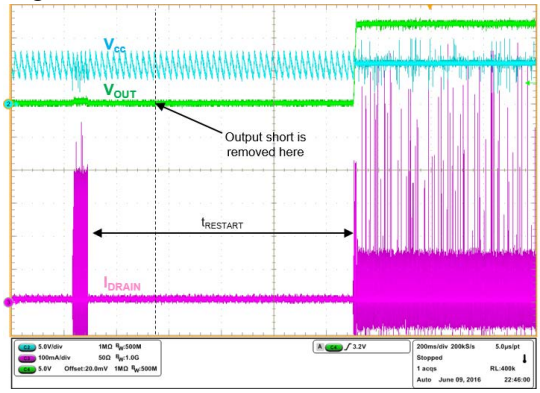


Figure 19: OLP: fault removed and autorestart



7.3 Pulse skip mode

Any time the I_{DRAIN} peak current exceeds I_{DLIM} within t_{ON_MIN} (minimum on-time), a switching cycle is skipped. Cycle-by-cycle, a check runs: the cycles can be skipped until the minimum switching frequency F_{OSC_MIN} (15 kHz, typ.) is reached.

When the internal OCP counter reaches its end-of-count, the IC is stopped for $t_{RESTART}$ (1 s, typ.) and subsequently reactivated via the soft-start phase. Whenever I_{DRAIN} does not exceed I_{DLIM} within t_{ON_MIN}, a switching cycle is restored.

The check is made on a cycle-by-cycle basis and the cycles can be restored until the nominal switching frequency F_{OSC} is reached.

By providing an inductor discharge time longer than usually allowed at nominal switching frequency, the protection helps limit the so called "flux runaway" effect which often occurs at converter startup when the primary MOSFET, charged during the minimum on-time through the input voltage, cannot discharge the same amount during off-time as the output voltage is very low. The result is a clear increase in average inductor current, which can reach dangerously high values while the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance.

To check the protection, the D2 secondary diode is shorted while the converter is operating at 265 V_{AC}.

The following two figures show first phase of the protection sequence. *Figure 21: "V_{IN} = 230 V_{AC}, D2 shorted, steady-state (2 of 3)"* shows how:

1. I_{DLIM} is exceeded at the first cycle, so the next cycle is skipped, resulting in a 30 kHz switching frequency;
2. I_{DLIM} is exceeded again, so the switching frequency is further halved to 15 kHz;
3. I_{DLIM} is exceeded again and the switching frequency is kept at 15 kHz indefinitely.

Figure 20: V_{IN} = 230 V_{AC}, D2 shorted, steady-state (1 of 3)

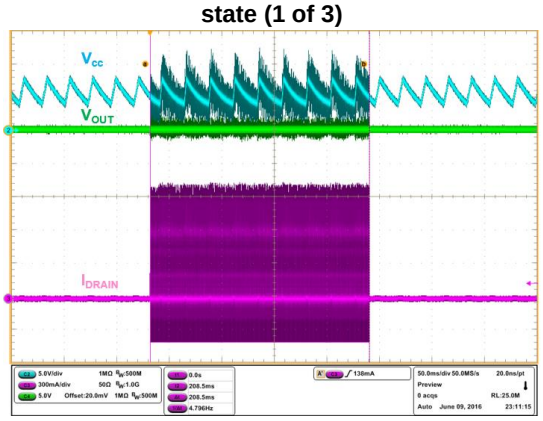


Figure 21: V_{IN} = 230 V_{AC}, D2 shorted, steady-state (2 of 3)

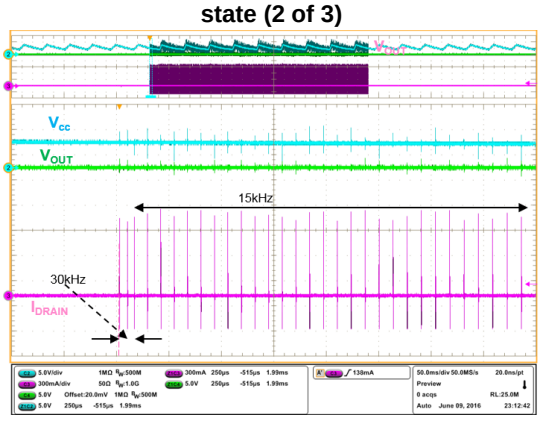


Figure 22: "V_{IN} = 230 V_{AC}, D2 shorted (zoom)" is a magnification of one of the switching cycles of *Figure 21: "V_{IN} = 230 V_{AC}, D2 shorted, steady-state (2 of 3)"* showing the drain current rising so quickly that it exceeds I_{DLIM} within t_{ON_MIN}.

The converter operates indefinitely at 15 kHz and the OCP internal counter is incremented each switching cycle. Since it is designed to reach its end of count (defining t_{OVL}) after 50 ms at 60 kHz, the overload time is incremented to 200 ms, as shown in *Figure 23: "V_{IN} = 230 V_{AC}, D2 shorted, steady-state (3 of 3)"*.

Figure 22: V_{IN} = 230 V_{AC}, D2 shorted (zoom)

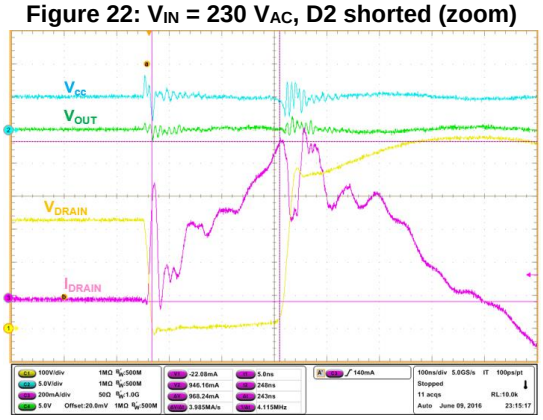
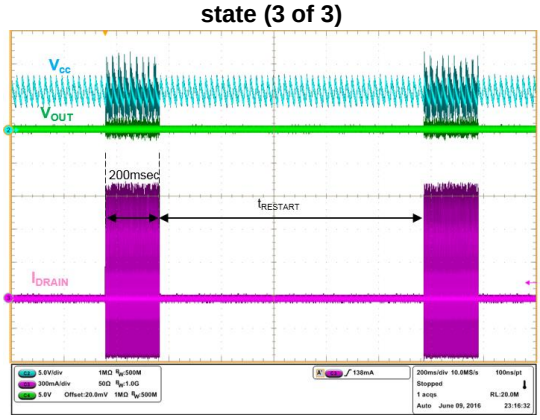


Figure 23: V_{IN} = 230 V_{AC}, D2 shorted, steady-state (3 of 3)



7.4 Maximum duty cycle counter protection

The IC embeds a maximum duty-cycle counter which disables the PWM if the MOSFET is turned off by the maximum duty cycle (70% min., 80% max.) for ten consecutive switching cycles. After protection tripping, the PWM is disabled for $t_{RESTART}$ and then reactivated via the soft-start phase until the fault condition is removed.

In some cases, such as when a loop break occurs at low input voltage, even if V_{COMP} is saturated, the OLP cannot be triggered as the PWM is turned off at every switching cycle by the maximum duty cycle before the drain peak current can reach I_{DLIM}. This can cause the output voltage V_{OUT} to rise uncontrollably and indefinitely above nominal values, placing the output capacitor, the output diode and the IC itself at risk, due to the potential breach of the 800 V breakdown threshold. The maximum duty cycle counter protection prevents this kind of failure.

Heavy load and low input voltage are used to test this protection.

The IC is protected in autorestart mode for $t_{RESTART}$ (1 sec typ), then continues attempting soft-starts until the fault condition is removed (see *Figure 24: "Shutdown due to max. duty cycle counter (initial tripping and restart)"* and *Figure 25: "Shutdown due to max. duty cycle counter (steady state)"*).

Figure 24: Shutdown due to max. duty cycle counter (initial tripping and restart)

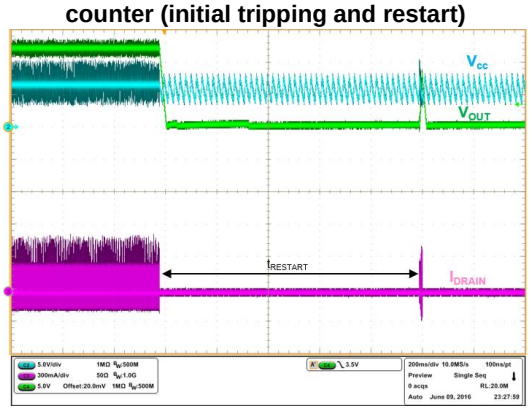


Figure 25: Shutdown due to max. duty cycle counter (steady state)

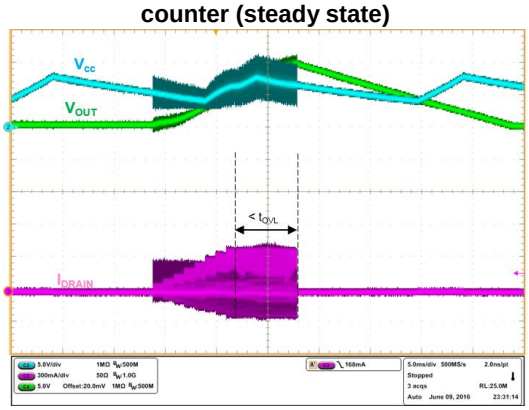


Figure 26: "Shutdown due to max. duty cycle counter (steady state) - zoom" magnifies the first cycle and shows the duty cycle measurement: 12/(12 + 4) = 75%. *Figure 27: "First of ten consecutive switching cycles at max. duty cycle"* shows the ten cycles causing the protection intervention.

Figure 26: Shutdown due to max. duty cycle counter (steady state) - zoom

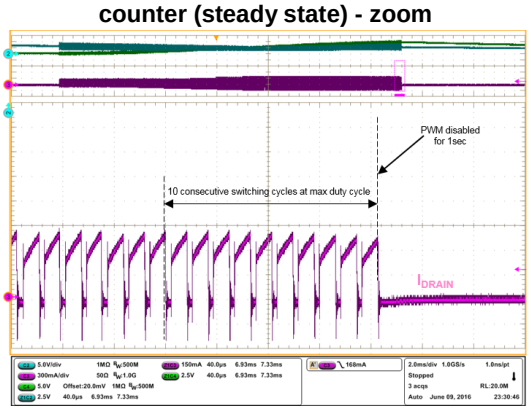
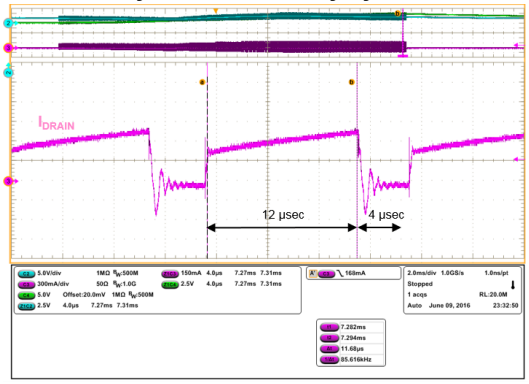


Figure 27: First of ten consecutive switching cycles at max. duty cycle



7.5 Overtemperature protection

If the VIPer0P junction temperature is higher than the internal threshold T_{SD} (160 °C, typ.), the PWM is disabled for $t_{RESTART}$. Following this, a single switching cycle is performed, during which the temperature sensor embedded in the Power MOSFET section is checked.

If a junction temperature above T_{SD} persists, the PWM is maintained disabled for $t_{RESTART}$ (*Figure 28: "OTP tripping and steady-state"* and *Figure 29: "Thermal check turn on during OTP"*).

The VIPer0P is overheated by a thermal gun air flow and it shuts down when the case temperature measures approximately 152 °C (measured by a thermal camera). The air flow temperature is then decreased at a slow rate. When the VIPer0P case temperature drops to about 120 °C, the converter resumes switching via a soft start phase.

Figure 28: OTP tripping and steady-state

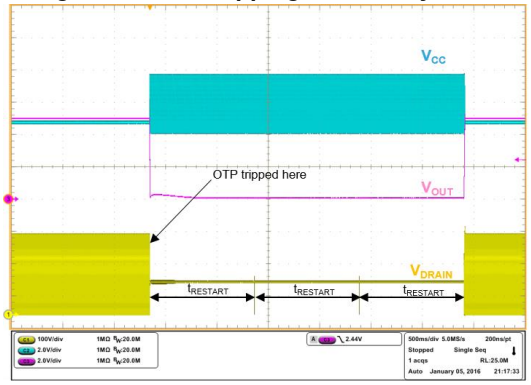
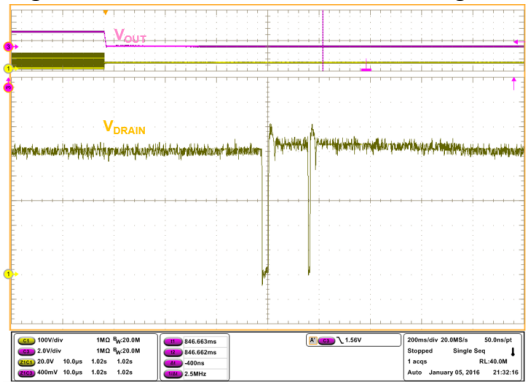


Figure 29: Thermal check turn on during OTP

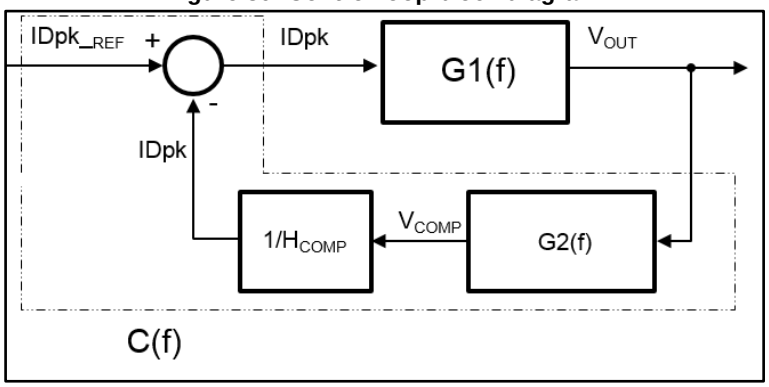


8 Feedback loop calculation guidelines

8.1 Transfer function

In the following figure, G1(f) represents the set PWM modulator plus power stage, while C(f) is the compensator network which ensures system stability.

Figure 30: Control loop block diagram



The mathematical expression for the power plant G1(f) is:

Equation 2

$$G1(f) = \frac{\Delta V_{OUT}}{\Delta I_{Dpk}} = \frac{|V_{OUT}| \cdot \left(1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z}\right)}{Ipkp(fsw, Vdc) \cdot \left(1 + \frac{j \cdot 2 \cdot \pi \cdot f}{p}\right)} = \frac{|V_{OUT}| \cdot \left(1 + \frac{j \cdot f}{fz}\right)}{Ipkp(fsw, Vdc) \cdot \left(1 + \frac{j \cdot f}{fp}\right)}$$

where fp is the pole due to the output load:

Equation 3

$$fp = \frac{1}{\pi \cdot C_{OUT} \cdot (R_{OUT} + 2 \cdot ESR)}$$

and fz is the zero due to the ESR of the output capacitor:

Equation 4

$$fz = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR}$$

The mathematical expression of the compensator C(f) is:

Equation 5

$$C(f) = \frac{\Delta I_{Dpk}}{\Delta V_{OUT}} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{(2 \cdot \pi \cdot f \cdot j) \cdot \left(1 + \frac{f \cdot j}{fPc}\right)}$$

where:

Equation 6

$$C_0 = \frac{R_{COMP(DYN)} \cdot CTR}{C10 \cdot R9 \cdot R6}$$

Equation 7

$$fZc = \frac{1}{2 \cdot \pi \cdot (R8 + R9) \cdot C10}$$

and

Equation 8

$$fPc = \frac{1}{2 \cdot \pi} \cdot \frac{1}{R_{COMP(DYN)} \cdot C7}$$

are chosen in order to ensure the stability of the overall system.

H_{COMP} = (V_{COMPH} - V_{COMPL})/(I_{DLIM} – I_{DLIM_PFM}) is the slope of the V_{COMP} vs I_{DRAIN} characteristic, $R_{COMP(DYN)}$ is specified in the VIPer0P datasheet, and CTR is the optocoupler current transfer ratio.

8.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossing frequency.

Equation 9

$$fZc = x \cdot fp$$

Equation 10

$$fPc = y \cdot fp$$

Equation 11

$$fcross \leq \frac{fsw}{10}$$

where x and y are arbitrarily chosen.

G1(fcross) can be calculated from *Equation 2* and, since by definition it is $|G1(fcross)*C(fcross)| = 1$, C_0 is obtained from equation *Equation 5* as follows:

Equation 12

$$C_0 = \frac{|2 \cdot \pi \cdot fcross \cdot j| \cdot \left|1 + \frac{fcross \cdot j}{fPc}\right|}{\left|1 + \frac{fcross \cdot j}{fZc}\right|} \cdot \frac{H_{COMP}}{|G1(fcross)|}$$

At this point the Bode diagram of the open loop transfer function G1(f)*C(f) can be plotted, in order to check the phase margin for the stability.

If the margin is not high enough, another choice should be done for fZc, fPc and fcross, and the procedure repeated.

When the stability is ensured, the values of the schematic components to implement C(f) are chosen as follows:

- R9 (high-side resistor of the output voltage divider) is set in the order of tens of kilohms;
- R10 (low-side resistor of the output voltage divider) is calculated from *Equation 1*:

Equation 13

$$R10 = \frac{R9}{\frac{V_{OUT}}{V_{ref}} - 1}$$

- C10 is calculated from *Equation 6*:

Equation 14

$$C10 = \frac{R_{COMP(DYN)} \cdot CTR}{R6 \cdot R9 \cdot C_0}$$

- R8 is obtained from *Equation 7*:

Equation 15

$$R8 = \frac{1}{2 \cdot \pi \cdot fZc \cdot C10} - R9$$

- and C7 is found from *Equation 8*:

Equation 16

$$C7 = \frac{1}{2 \cdot \pi} \cdot \frac{1}{R_{COMP(DYN)} \cdot fPc}$$

After selecting commercial values for R9, R10, C10, R8 and C7, the actual values of C_0, fZc and fPc should be calculated using equations *Equation 6, Equation 7* and *Equation 8*, thus obtaining respectively C_0_act, fZc_act and fPc_act . Substituting these values in *Equation 5*, the actual compensator, C_act(f), is obtained. The Bode diagram of G1(f)*C_act(f) can now be plotted in order to check whether the phase margin for the stability is still guaranteed.

9 Thermal measurements

Thermal analysis of the board was performed using an IR camera at 90 V_{AC}, 115 V_{AC}, 230 V_{AC} and 265 V_{AC} mains input, full load condition. The results are shown in the following figures.

Figure 31: Thermal measurements by IR camera at V_{IN} = 90 V_{AC}, full load, T_{AMB} = 25°C

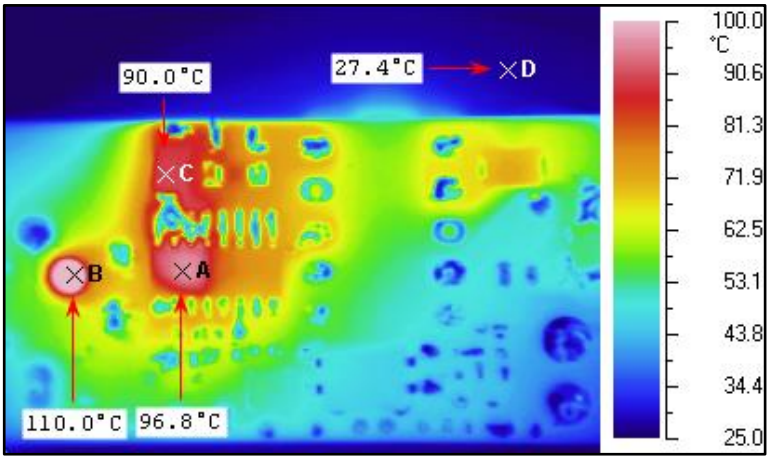


Figure 32: Thermal measurements by IR camera at V_{IN} = 115 V_{AC}, full load, T_{AMB} = 25 °C

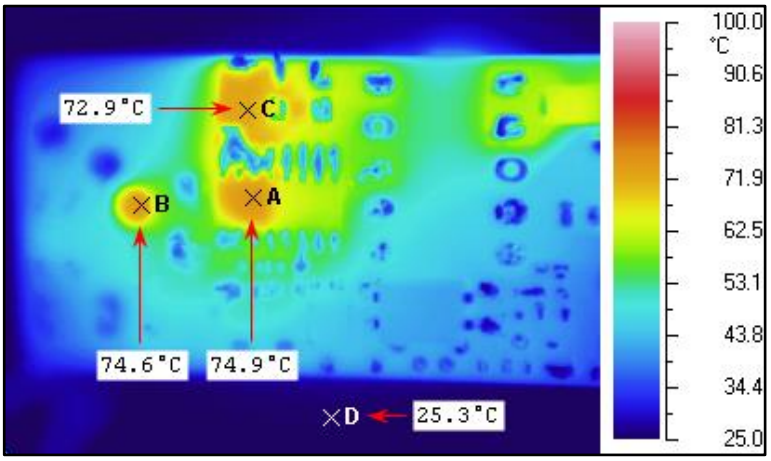


Figure 33: Thermal measurements by IR camera at V_{IN} = 230 V_{AC}, full load, T_{AMB} = 25 °C

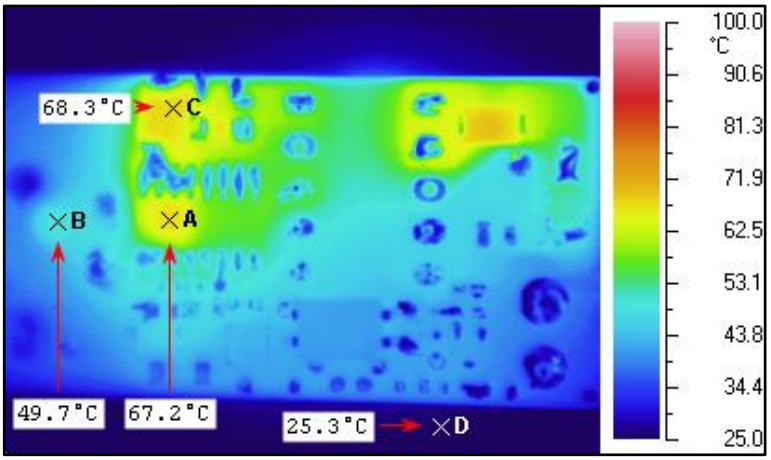
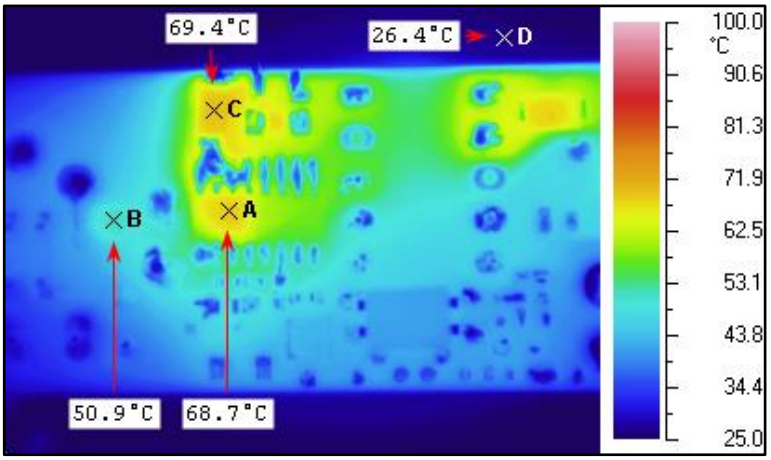


Figure 34: Thermal measurements by IR camera at V_{IN} = 265 V_{AC}, full load, T_{AMB} = 25 °C



10 EMI measurements

A pre-compliance test for European normative EN55022 (Class B) was performed using an EMC analyzer and a line impedance stabilization network (LISN).

Figure 35: EMI average measurements at 115 V_{AC}, full load, T_{AMB} = 25 °C

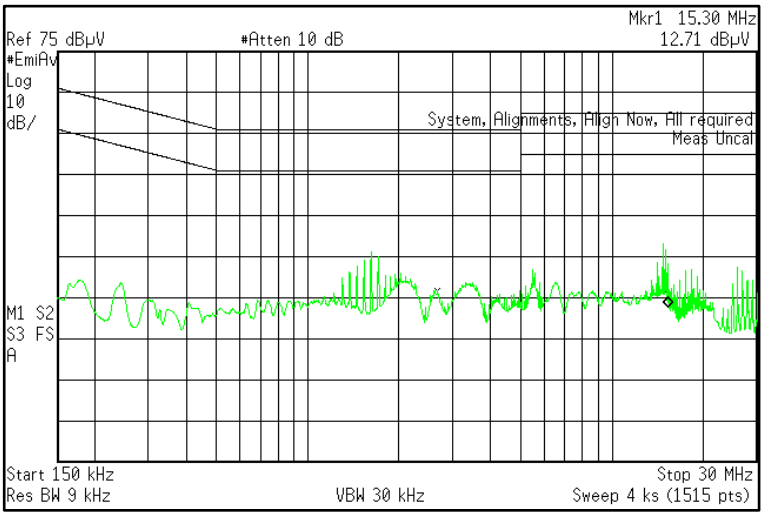
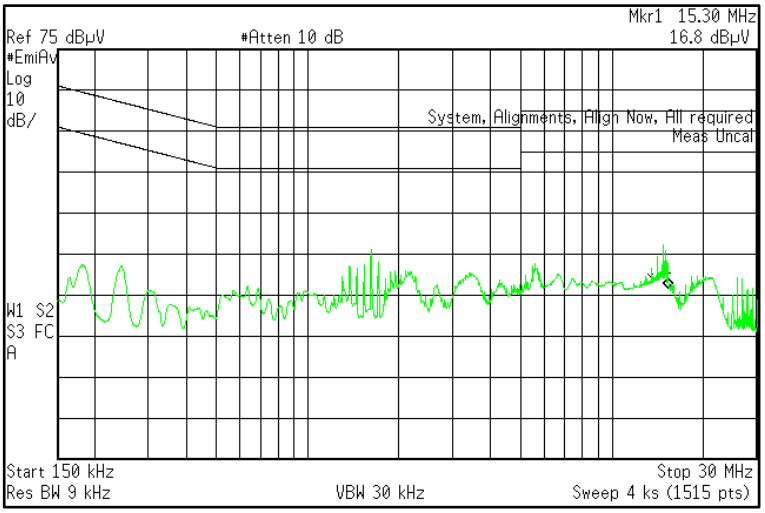


Figure 36: EMI average measurements at 230 V_{AC}, full load, T_{AMB} = 25 °C



11 Conclusions

The STEVAL-ISA180V1 demonstrates that the VIPer0P simplifies the design of isolated converters, in compliance with the most stringent energy regulations, and reduces the amount of external components required.

The STEVAL-ISA180V1 consumes less than 18 mW at 230 V_{AC} under no load condition and meets the CoC 5 and DOE external power supplies requirements for active mode and light load efficiency.

The 800 V avalanche rugged Power MOSFET and the embedded protections add reliability to the power converter, making the VIPer0P the ideal choice for applications requiring robustness and energy efficient performance.

12 Revision history

Table 9: Document revision history

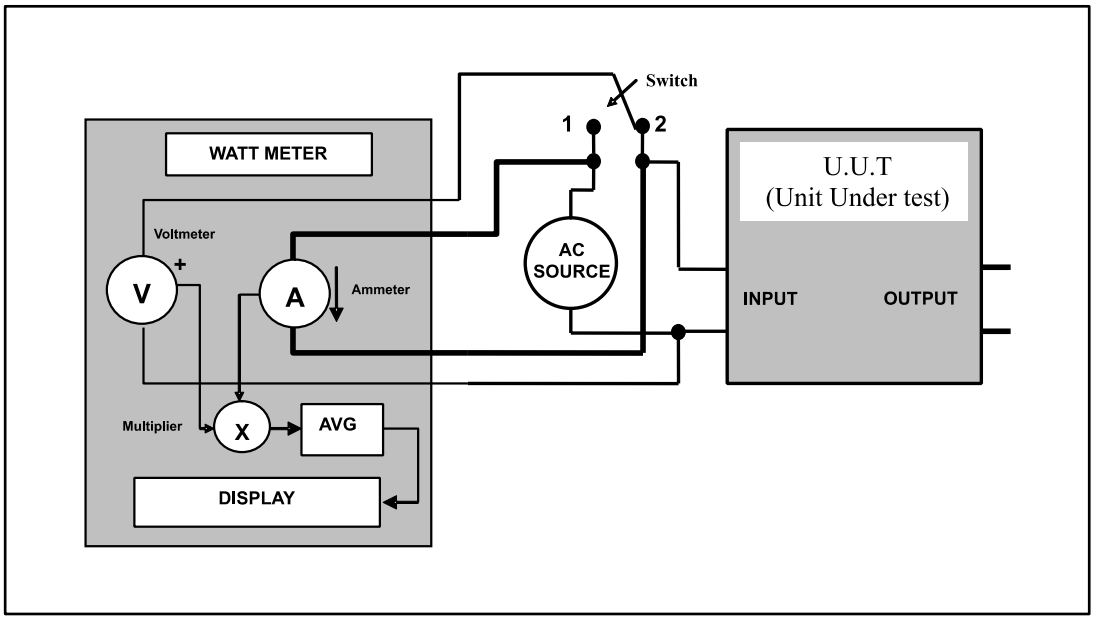
Date	Version	Changes
29-Sep-2016	1	Initial release

Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power is measured using a wattmeter. The wattmeter simultaneously measures the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The digital wattmeter samples the current and voltage and converts them in digital formats, which are then multiplied to give the instantaneous measured power. The sampling frequency is in the range of 20 kHz or higher and the average measured power over a short interval (1 s typ.) is displayed.

The following figure shows the wattmeter connection to the UUT (unit under test) and AC source, as well as the wattmeter internal block diagram.

Figure 37: Connections of the UUT to the wattmeter for power measurements



An electronic load is connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage is measured by a voltmeter. The output power is the product between load current and output voltage.

The ratio between the above output power calculation and the input power measured by the wattmeter is the converter's efficiency, measured under different input/output conditions.

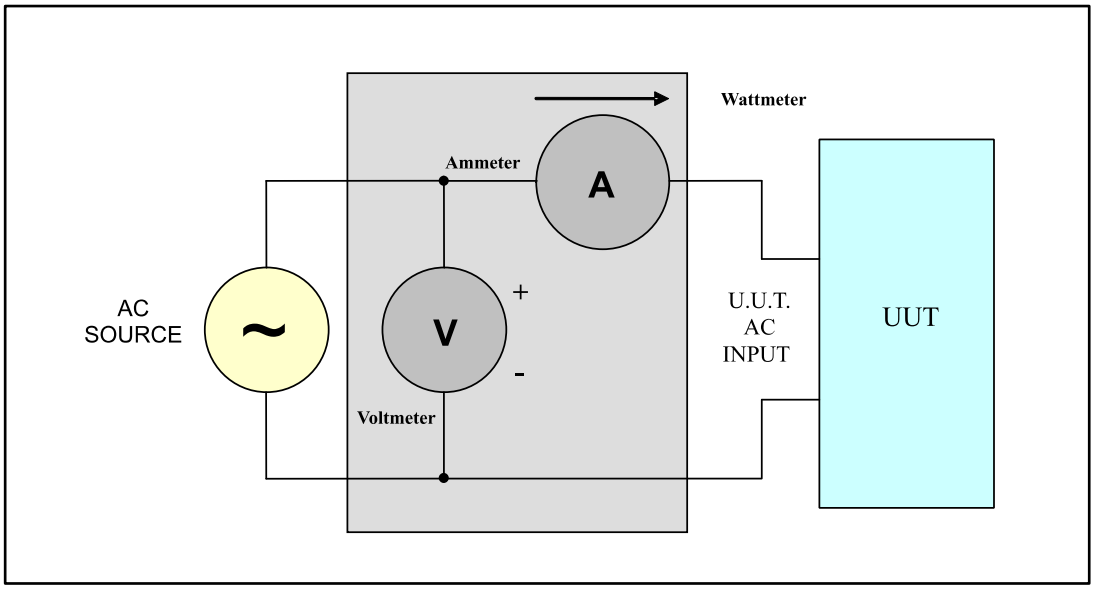
Considerations when measuring input power

With reference to *Figure 37: "Connections of the UUT to the wattmeter for power measurements"*, the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal as it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

If the switch in *Figure 37: "Connections of the UUT to the wattmeter for power measurements"* is in position 1 (see the simplified schematic below) this voltage drop causes an input measured voltage higher than the input voltage at the UUT input, which of

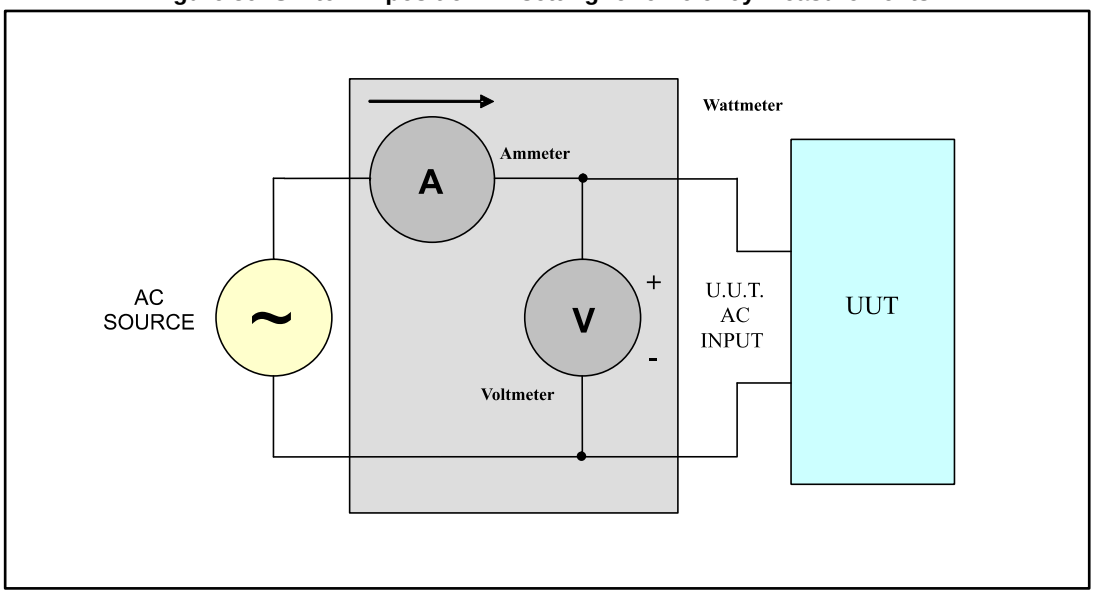
course distorts the measured power. The voltage drop is generally negligible if the UUT input current is low (e.g., the input power of UUT under low load condition).

Figure 38: Switch in position 1 - setting for standby measurements



For high UUT input currents (e.g., heavy load conditions), the voltage drop compared to the UUT real input voltage can become significant. In this case, the switch in *Figure 37: "Connections of the UUT to the wattmeter for power measurements"* should be set to position 2 (see the simplified schematic below), where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 39: Switch in position 2 - setting for efficiency measurements



On the other hand, the arrangement in *Figure 39: "Switch in position 2 - setting for efficiency measurements"* may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (not having infinite input resistance) is not negligible. This is why it is better to use the *Figure*

38: "Switch in position 1 - setting for standby measurements" arrangement for light load measurements and *Figure 39: "Switch in position 2 - setting for efficiency measurements"* for heavy loads.

If you are not certain which arrangement distorts the result less, try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT shall be operated at 100% of nameplate output current output for at least 30 minutes (warm up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power shall be monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5 minute period. If AC input power is not stable over a 5 minute period, the average power or accumulated energy shall be measured over time for both AC input and DC output.

Some wattmeter models allow integrating the measured input power over a time range and measuring the energy absorbed by the UUT during the integration time. Dividing by the integration time itself gives the average input power.

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