# AN4932
# Application note

# HVLED001A - enhanced QR high power factor flyback controller for LED drivers

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## Introduction

The flexibility of the LED chips and their improving performances are more and more exploited in many fields of applications. Besides the residential and bulb replacement applications, whose input power spreads between 3 W and 15 W, a very wide range of higher power applications are available for very different environment such office or store lighting, professional or colored lighting and outdoor lighting. Those applications are characterized by output powers up to 100 W.

Key factors of such applications are good efficiency, power controllability (e.g.: dimming) and a small component count. In such condition, the single stage high power factor flyback topology combines the advantages of the single stage (higher efficiency and low BOM count) with the flexibility of the control algorithm (higher controllability).

The HVLED001A controller has been designed to optimize the control of a high power factor flyback or buck-boost to be used in a LED driver. Nevertheless it is also able to efficiently control the same topology to provide a constant output voltage exploiting a proprietary primary side controlled algorithm. When driven by a PFC pre-regulator the HVLED001A device can be used as a DC/DC QR flyback converter.

This application note is intended to describe the HVLED001A features and to provide the design guidelines to implement a single stage LED driver.

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## 1.1 Pin function summary

**Table 1. Pin function**

| Symbol | Pin | Function name | Section |
|---|---|---|---|
| HVSU | 1 | High voltage start-up | *Section 1.3: Device supply management on page 8*. |
| | | Input voltage detection | *Section 1.4: Peak current mode definition on page 10*. |
| | | Input overvoltage detection | *Section 1.9.1: Input overvoltage and surge protection (IOVP) on page 26*. |
| N.C. | 2 | Not connected pin | |
| TOFF | 3 | ZCD blanking time setting | *Section 1.5.3: Frequency foldback on page 17*. |
| FB | 4 | Input for optocoupler connection | *Section 1.6.2: Secondary side regulation on page 24*. |
| | | PSR E/A output connection | *Section 1.6.1: Primary side regulation on page 22*. |
| | | Opto failure protection | *Section 1.9.2: Overload and optocoupler failure management (OFP) on page 27*. |
| | | Overload protection | *Section 1.9.2*. |
| | | Burst mode | *Section 1.6.3: Burst mode on page 24*. |
| CTRL | 5 | Inrush limit / soft-start | *Section 1.4.3 on page 14*. |
| | | Disable input (active low) | *Section 1.8.1: Instant disable on page 25*. |
| | | Timed disable (active high) | *Section 1.8.2: Timed disable by CTRL on page 26*. |
| ZCD | 6 | ZCD detection | *Section 1.5.2: SMART ZCD detection on page 17*. |
| | | Vout sampling input for PSR | *Section 1.6.1: Primary side regulation on page 22*. |
| | | Brownout protection | *Section 1.9.4: Brownout on page 28*. |
| CS | 7 | Current sense comparator input | *Section 1.4.2 on page 12*. |
| | | Overcurrent protection (OCP) input | *Section 1.9.5: Magnetic saturation or rectifier short-circuit on page 29*. |
| GND | 8 | Reference pin | - |
| GD | 9 | Gate driver output | *Section 1.7: Gate driving on page 25*. |
| VCC | 10 | Supply energy to the IC | *Section 1.3: Device supply management on page 8*. |
| | | Internal UVLO logic | *Section 1.3*. |

## 1.2 Operating modes

The HVLED001A device has four main operating modes: the start-up mode, active mode, stop mode and low consumption mode.

### 1.2.1 Start-up mode

This state is entered to begin the switching activity after the application's turn-on or leaving the low consumption state. The HVSU is involved into the mechanism of VCC charging; all other peripherals, except from the UVLO and logic supply, are turned off to minimize the start-up time.

During this state the CTLR pin is internally pulled to ground.

### 1.2.2 Active mode

It is the normal operational mode. During this state the external MOSFET is driven accordingly to signals coming from the application in order to regulate the desired output parameter in the closed loop (peak current control method).

The active mode is exit when abnormal conditions are present. The HVSU is inactive during the active mode.

### 1.2.3 Stop mode

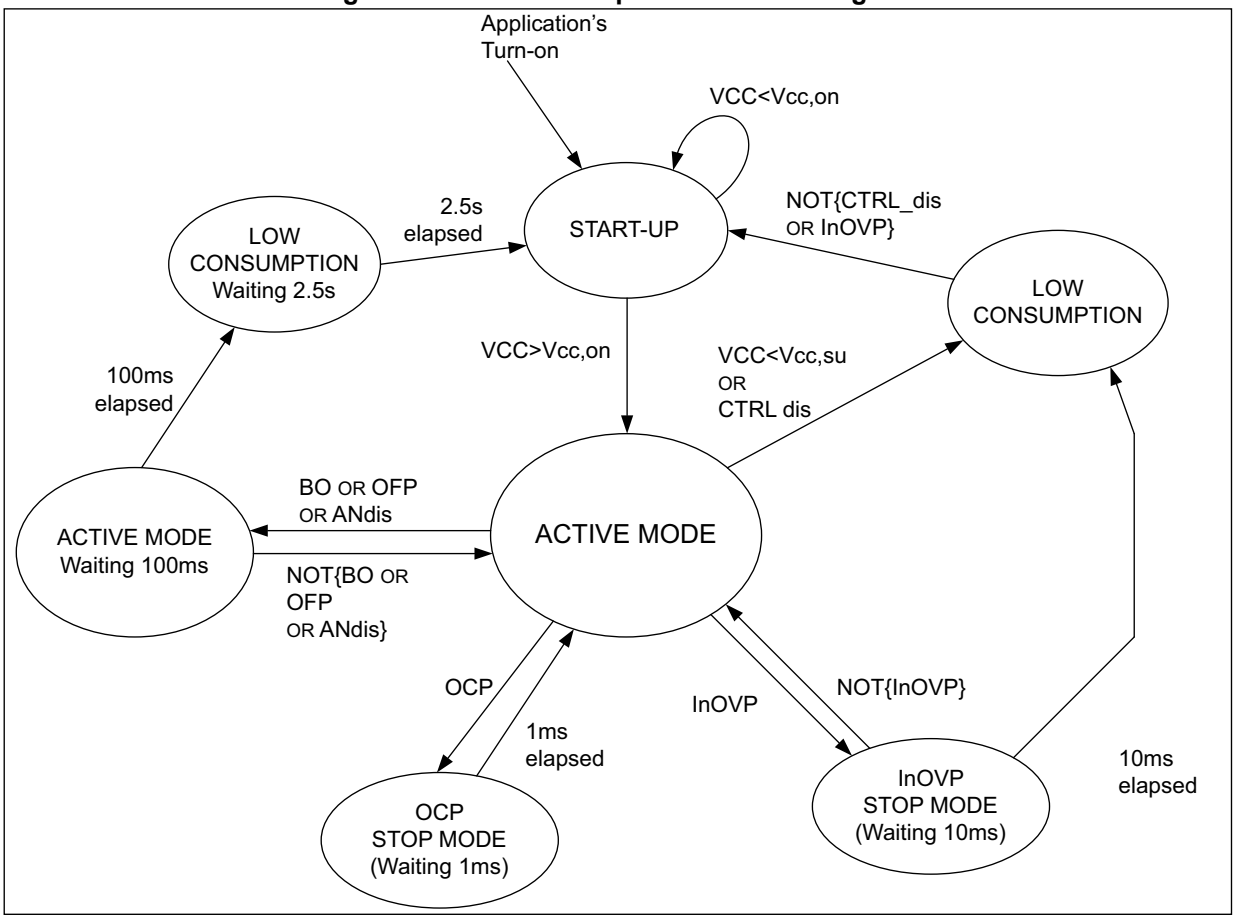
This state is intended to stop the switching activity without turning off the entire function set, to quickly restart when abnormal or disabling conditions end. During this state the power consumption is not minimized and the soft-start procedure is not enabled.

### 1.2.4 Low consumption mode

This state is intended to stop the switching activity reducing the power consumption to a minimum level. During this state the VCC is kept between VCC,su and VCC,on by the HVSU.

A simplified state diagram is reported in *Figure 1*.

**Figure 1. HVLED001A operation states diagram**



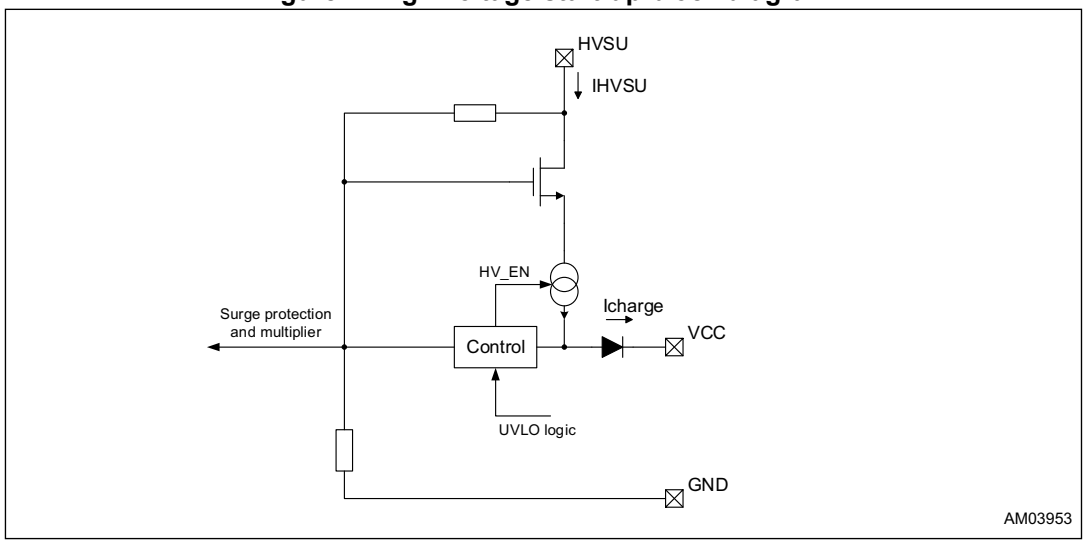
## 1.3 Device supply management

*[Involved pins 1: HVSU, 10: VCC]*

The HVLED001A device embeds smart supply voltage management able to both prevent the application from driving the MOSFET with insufficient energy and to maintain the precision of the internal references.

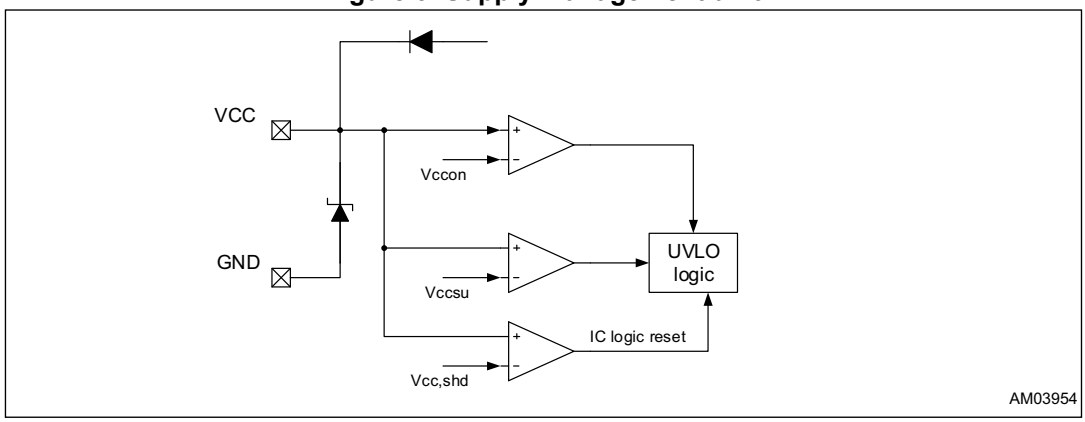
A high voltage start-up unit, connected to the HVSU pin, provides the start-up current to initiate the IC operations and maintain the IC on during low consumption modes (*Figure 2*).

**Figure 2. High voltage start-up block diagram**




The HVSU starts its operation when the applied voltage is higher than 45 V (typ.). The charging current ensures a quick start-up independent from the voltage applied to the HVSU pin. Two different currents are generated depending on VCC voltage and the lower value is generated when VCC is below the Vcc,su threshold. At the first start-up the VCC,su threshold assumes its lower value (around 2 V).

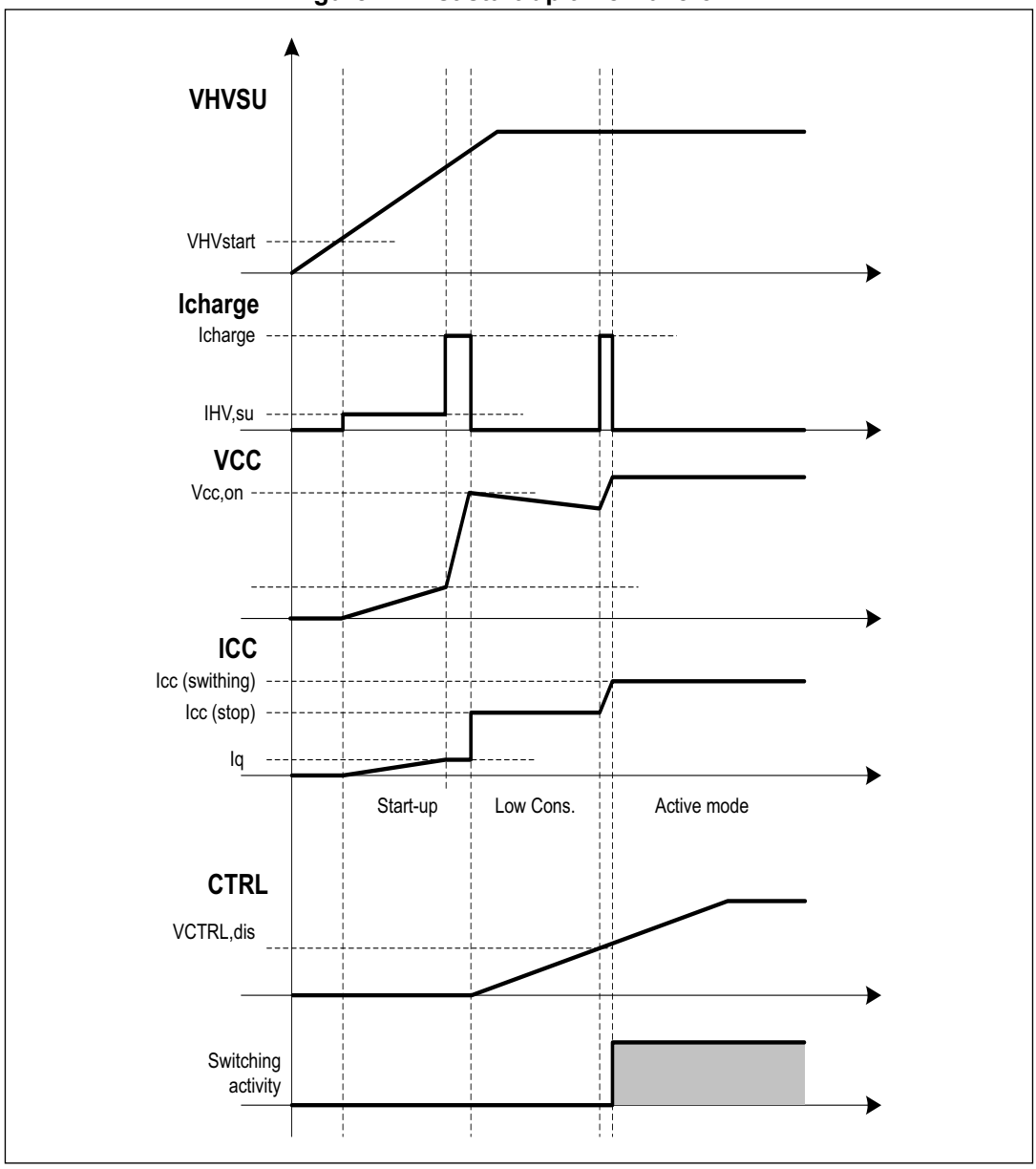
**Figure 3. Supply management unit**




The VCC management unit consists of three comparators (*Figure 3*). The lower threshold is the Vcc,shd: this comparator is responsible to reset all timing and protection information when VCC is lower than this voltage.

As soon as the VCC voltage reaches the turn-on threshold (Vcc,on), the HVSU is turned off and pull-up sources of the pins TOFF and CTRL are turned on. If the above mentioned pins are not externally pulled down, the switching activity will start as soon as both the operative conditions are reached (CTRL above relevant disable thresholds) and $V_{CC}$ is pulled up again to the Vcc,on threshold.

**Figure 4. First start-up time waveform**




During the switching activity the HVSU is kept off, in fact the IC is expected to be supplied by the energy kept from either an auxiliary winding of the main magnetic component (transformer or inductor) or an auxiliary converter. To be noted that any kind of supplying mean (including auxiliary winding) must be decoupled from the VCC pin using a general purpose diode having the proper reverse voltage rating: this good practice is necessary to preserve the mutual functionality of HVSU and VCC.

If the supplying energy is insufficient the VCC voltage may drop below the Vcc,su threshold; at this occurrence the switching activity is stopped and the device enters the low consumption mode. Contemporarily the CTRL pin is internally pulled down: the CTRL voltage could then be used to signal this state to external supervisors or to disable external circuits.

During the low consumption mode the HVSU is active to maintain the VCC voltage between VCC,on and VCC,su.

An internal clamping device is connected to the VCC pin to prevent spurious VCC fluctuation from damaging internal structures.

## 1.4 Peak current mode definition

*[Involved pins 1: HVSU, 4: FB, 5: CTRL, 7: CS]*

### 1.4.1 Multiplier

The core of the HVLED001A device is a peak current mode controller that provides the turn-off command to the gate driver when the MOSFET's source current reaches a threshold (VCS) provided by a multiplier block as per the following equation.

**Equation 1**

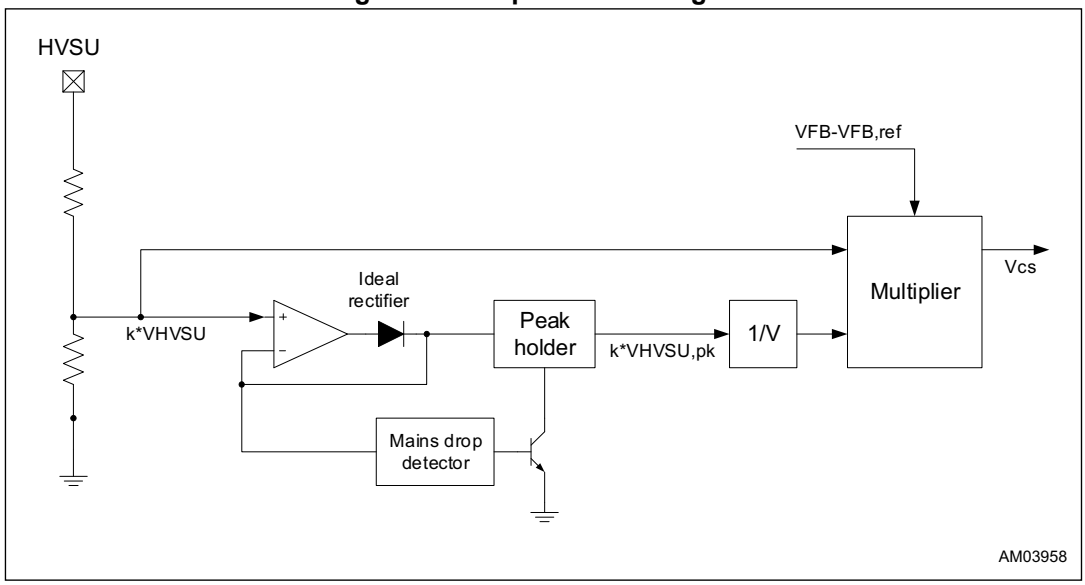
$$V_{CS} = k_p \cdot \frac{V_{HVSU}}{V_{HVSU,pk}} \cdot \left(V_{FB} - V_{FB,ref}\right)$$

At first the input voltage, connected to the HVSU pin, is scaled by an internal equivalent voltage divider. Then it is normalized dividing the input voltage by its maximum value (VFF); as a result the term VHVSU / VHVSU,pk is either a half sinusoid having amplitude of 1 V or a unity DC voltage if the HVSU pin is connected respectively to a rectified mains (any value between typ. 32 VAC to 305 VAC) or to a DC voltage (e.g.: PFC output).

The peak of the input voltage is obtained by a peak detector able to quickly react to an abrupt mains change thanks to a proprietary internal structure able to operate without any external storing element (capacitors). A positive going variation of the input voltage is immediately processed by the peak holder block, while a negative going variation is detected within typically 3 half sine waves and results into a limited variation (in time and amplitude) of the application's output (current or voltage).

A detail of the blocks involved in this feature is shown in *Figure 5*.

**Figure 5. Multiplier block diagram**




The voltage present on the FB pin, representative of the energy required by the load, is firstly purged by the term VFB,ref and then applied to another input of the multiplier.

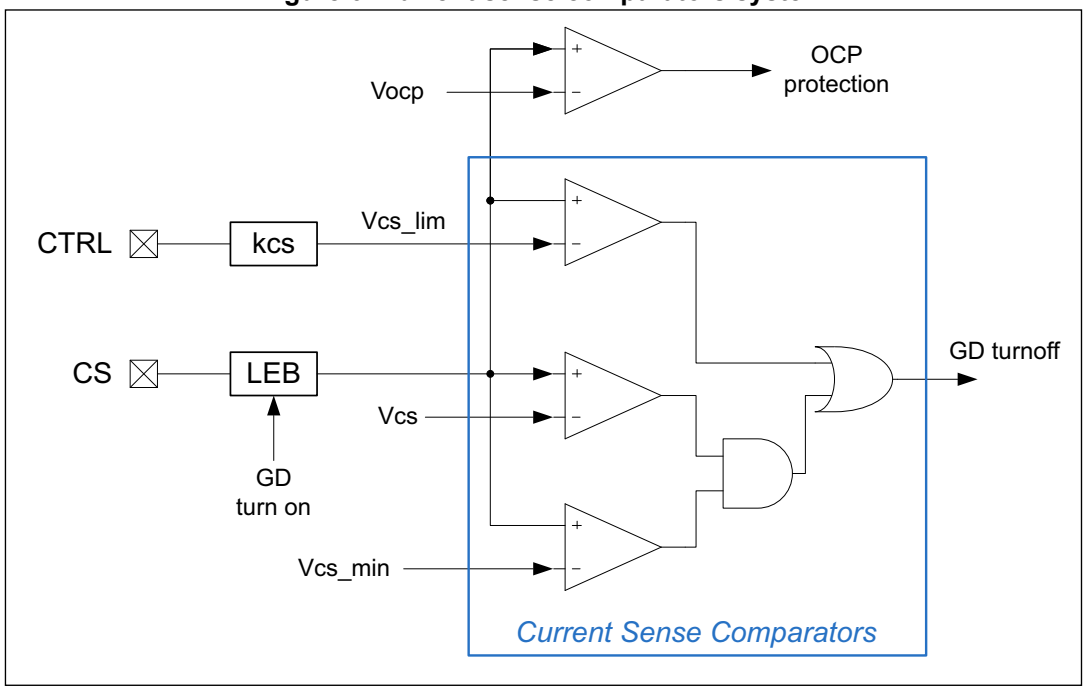
Finally the multiplier block adapts the result of the product between the voltages representative of input voltage and load energy to a maximum level for current sense input equal to VCS,lim (around 0.75 V). The overall scaling factor of the multiplier is equal to $k_p$ and is reported in the product datasheet. The linearity of the multiplier block is guaranteed over a range of input voltages between 0 V and 480 Vdc. Higher input voltages may result into a clipping of the multiplier results, but without affecting the safe operation of the device.

### 1.4.2 Current sense comparator system

The internal current sense comparator compares the output of the multiplier with the voltage present at the CS pin. In a typical application the CS pin is connected to a shunt resistor (RCS) placed between the source of the MOSFET and common ground.

A summary of the structures involved into peak current detection is shown in *Figure 6*.

**Figure 6. Current sense comparators system**

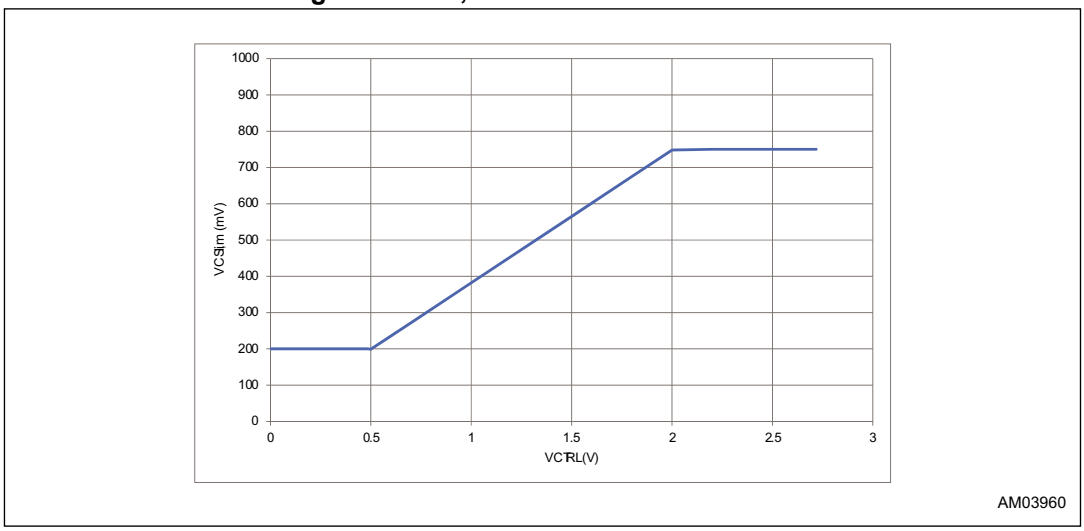



The maximum value of VCS is also related to the voltage present at the CTRL pin as per following equation:

**Equation 2**

$$\begin{cases} V_{CS,lim} = 0.366 \cdot V_{CTRL} + 0.016 \\ V_{CTRL} \in (V_{CTRL,dis}, Veoss) \end{cases}$$

**Figure 7. VCS,lim vs. Vctrl characteristic**




The value of RCS has to be selected in order to obtain VC,lim at a full load, i.e.: at a maximum MOSFET's peak current Ipkp,max. The value of the Ipkp,max can be obtained according to the implemented topology.

**Equation 3**

$$R_{CS} = \frac{V_{CS,lim}}{I_{pkp,max}}$$

An internal LEB structure prevents the loop from reacting to gate driver's turn-on spikes; when a proper design of the PCB layout is made, no further filter structure should be necessary.

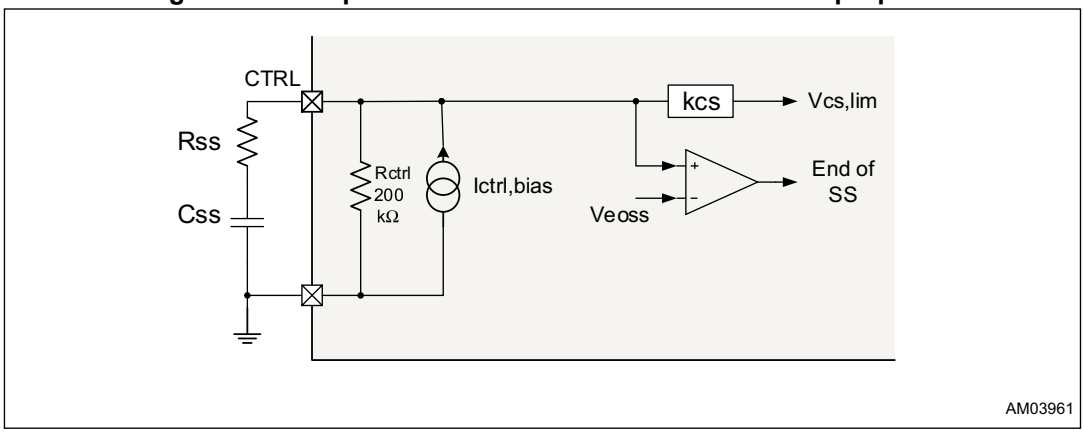
A minimum level of VCS is also present to guarantee a minimum value for the MOSFET drain's current: this minimum current helps to reduce the THD and to guarantee a minimum value for the demagnetization time.

### 1.4.3 Soft-start

The dependence of VCS,lim on CTRL pin's voltage can be exploited either at the start-up or when low consumption ends: in fact it limits the peak of the current transferred to the load (inrush limit). The duration of this limitation is determined by the time the CTRL takes to reach its steady value, i.e.: by the size of the capacitance (Css) placed between CTRL and GND.

*Figure 8* illustrates the equivalent model of the internal structures connected to the CTRL pin that are involved in soft-start function and the suggested circuitry to activate this feature.

**Figure 8. CTRL pin structures to be used for soft-start purpose**




Until the CTRL voltage is below VCTRL,dis the HVLED001A device is disabled. After the device's start and until CTRL pin's voltage is lower than Veoss many features are disabled: namely the THD optimization and the timed protections. In fact, during the first operation instants the control loop is providing the maximum power to the output in order to reach the set value of the output variables, but this condition, without a proper masking, may trigger said protections.

During the normal operation, after CTRL voltage rises above Veoss, all protections and features are active and the CTRL voltage can be optionally reduced by external circuitry to limit the maximum level of VCS,lim.

A proper choice of the optional resistor Rss allows to obtain a CTRL pin's voltage higher than the disabling threshold immediately after the IC turn-on.

## 1.5 Smart zero current detection

*[Involved pins 3: TOFF, 6: ZCD]*

The ZCD pin of the HVLED001A device features the following functionalities:

- Detection of the resonant's valleys associated with the transformer's demagnetization instant to set the boundary mode conduction of the desired topology.
- Measurement of the voltage present at the pin at the demagnetization instant, for the primary side control purpose (described in *Section 1.6.1 on page 22*).
- Measurement of the current sunk during the on time of the controlled MOSFET, for the brownout protection purpose (described in *Section 1.9.4 on page 28*).

### 1.5.1 Demagnetization detection

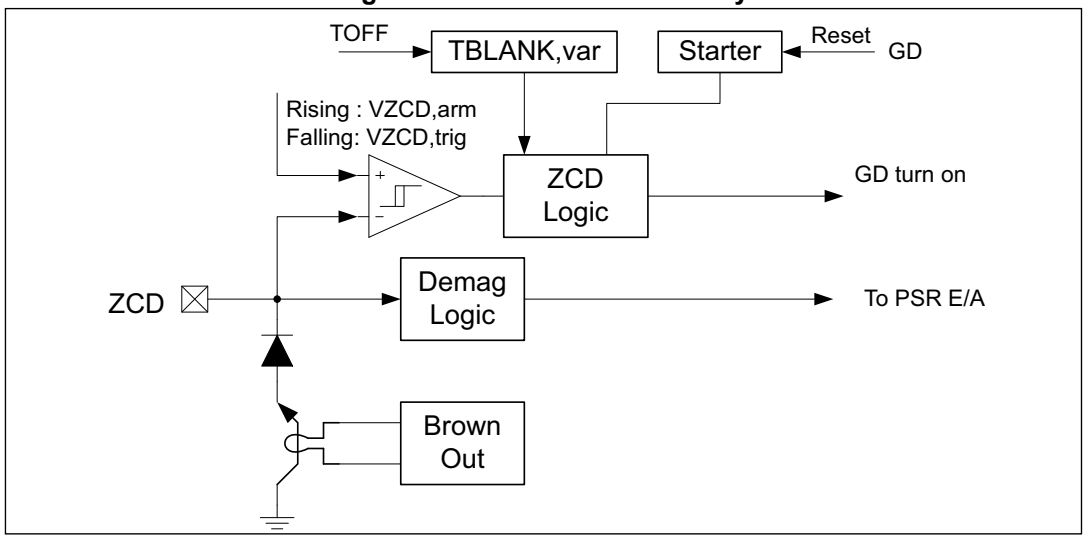
The detection of the resonant valley is designed to implement the quasi resonant (QR) mode of flyback or buck-boost topology. The QR mode consists on turning on the MOSFET when the current into the primary side of the flyback transformer (or alternatively into the inductor of the buck-boost) becomes zero. At this occurrence, the drain of the MOSFET starts oscillating at a frequency set by the value of the inductance and the overall drain capacitance.

**Equation 4**

$$f_{Resonance} = \frac{1}{2\pi\sqrt{C_{Drain} \cdot L_{PRI}}}$$

The amplitude of the oscillation is given by the output voltage scaled by the primary-to-secondary turn ratio (or output voltage in case of buck-boost topology) and is superimposed to input voltage. This oscillation (without DC component) is also present on the output of any winding coupled with the primary inductance and then it can be fed to the ZCD pin, whose internal block structure is illustrated in *Figure 9*.

**Figure 9. ZCD detection circuitry**

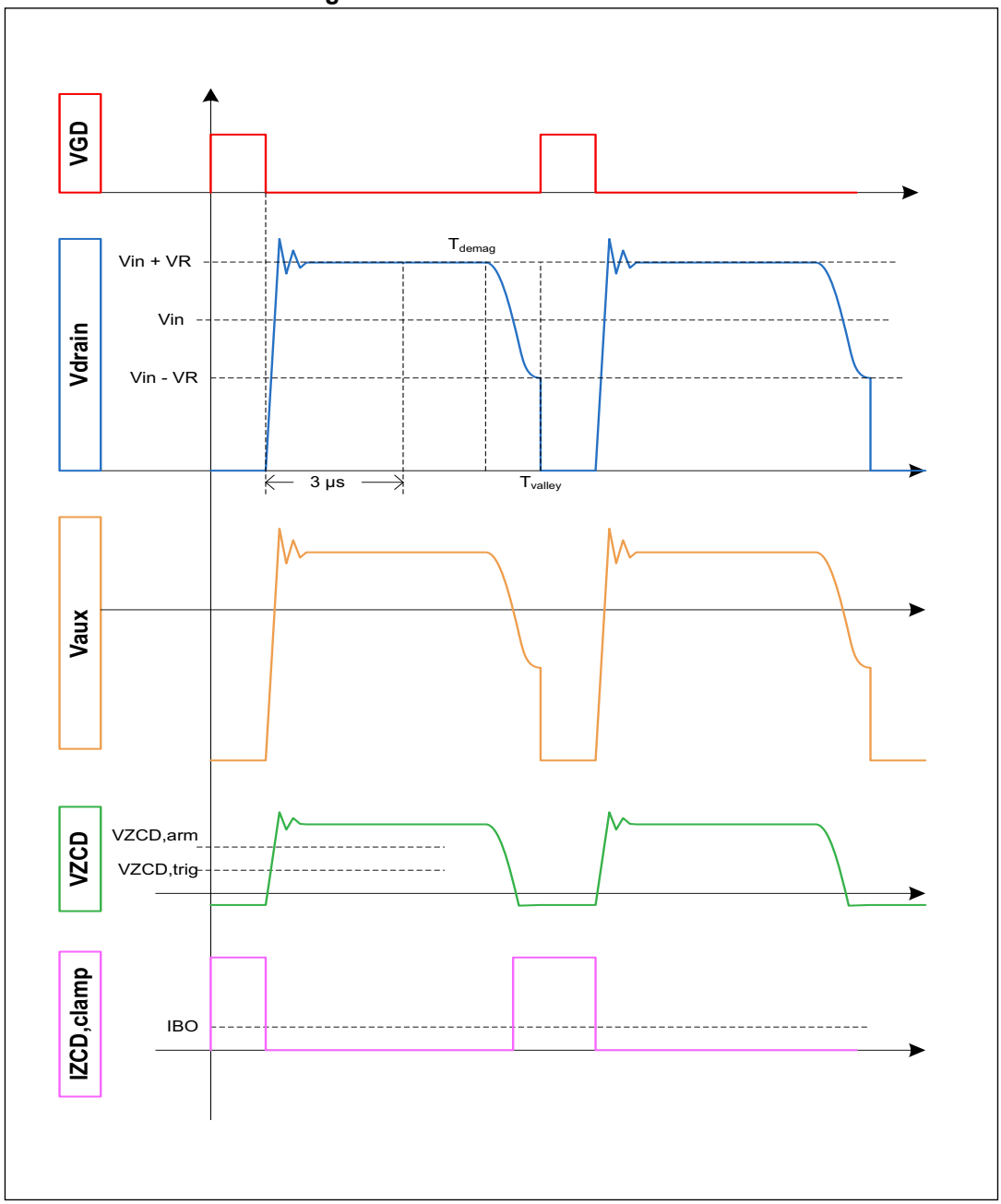



The signals related to the zero current detection are illustrated in *Figure 10*.

Although the boundary mode operation is achieved when the MOSFET is turned on when the demagnetization occurs, it is most convenient, in order to minimize the switching losses, to turn-on the MOSFET to the minimum of the oscillation (valley switching).

The demagnetization instant (Tdemag) is captured by the DEMAG LOGIC block when the derivative of the voltage becomes suddenly negative, while the valley switching (Tvalley) is managed by the ZCD comparator waiting for the falling edge of the oscillation across zero (VZCD,trig).

Figure 10. ZCD related waveforms



### 1.5.2 SMART ZCD detection

The HVLED001A device is able to distinguish an effective demagnetization from abnormal signals.

The HVLED001A considers an energy transfer phase correctly ongoing if the ZCD signal is higher than an arming threshold (VZCD,arm) 3 µs (TBLANK,min) after the MOSFET turn-off. This strategy helps rejecting the high frequency oscillations associated with the leakage inductance that normally ends in a couple of microseconds after the MOSFET turn-off.

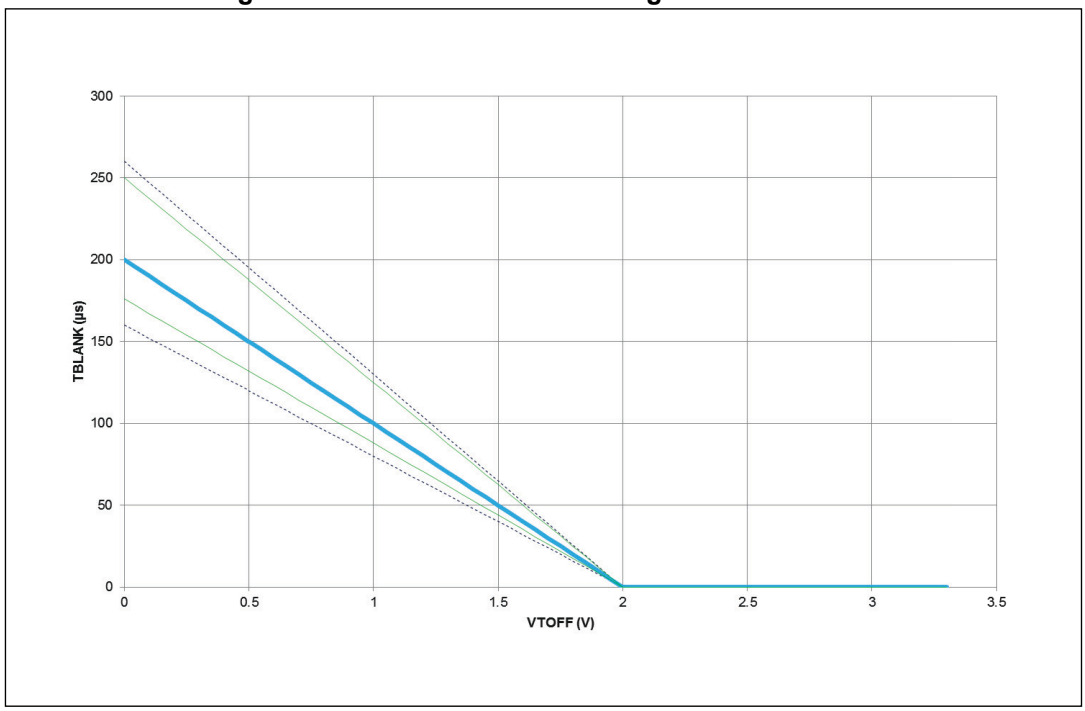
This check is performed when the value of the Vcs threshold (or the output of the multiplier) is higher than 650 mV (typ.). If a correct energy transfer occurs, the first falling edge (VZCD,trig) subsequent the blanking time (defined by the voltage at the pin TOFF) is used to trigger the MOSFET's turn-on instant.

At the start-up, when no ZCD signal is present, a 500 µs timer (starter) provides a triggering signal for GD turn-on. The same unit provides a restarting attempt in case of absence of a valid ZCD signal (e.g.: during short-circuit).

### 1.5.3 Frequency foldback

When the output power demand diminishes, the duty cycle of the MOSFET's activity is reduced. This duty cycle reduction can be obtained either reducing the MOSFET's on time interval or increasing the off time interval entering into the discontinuous conduction mode. The valley skipping technique is an efficient approach to obtain both a longer off time and to turn-on the MOSFET with a lower drain voltage. The resulting operating frequency is folded back to a lower value. The HVLED001A performs this “valley skipping” technique adding a further blanking time after the detection of the first resonance valley. The increase of the blanking time is adjustable up to 200 µs varying the voltage applied to the TOFF pin as described in the characteristic illustrated in *Figure 11* (typical values). The MOSFET is turned on in correspondence of the first valley occurring after the end of the additional blanking time, while a proprietary structure ensures a correct turn-on of the MOSFET's also after the oscillation amplitude is fully decayed.

**Figure 11. TBLANK vs. TOFF voltage characteristics**




The behavior of the HVLED001A in correspondence of the different TBLANK,var setting is also illustrated from *Figure 12* to *Figure 14 on page 21*.

*Figure 12* is the case when TOFF voltage is higher than 2 V: the TBLANK,var is zero and the first valley is used as a trigger signal to turn-on the MOSFET gate driver.

**Figure 12. Example: TOFF voltage higher than 2 V**

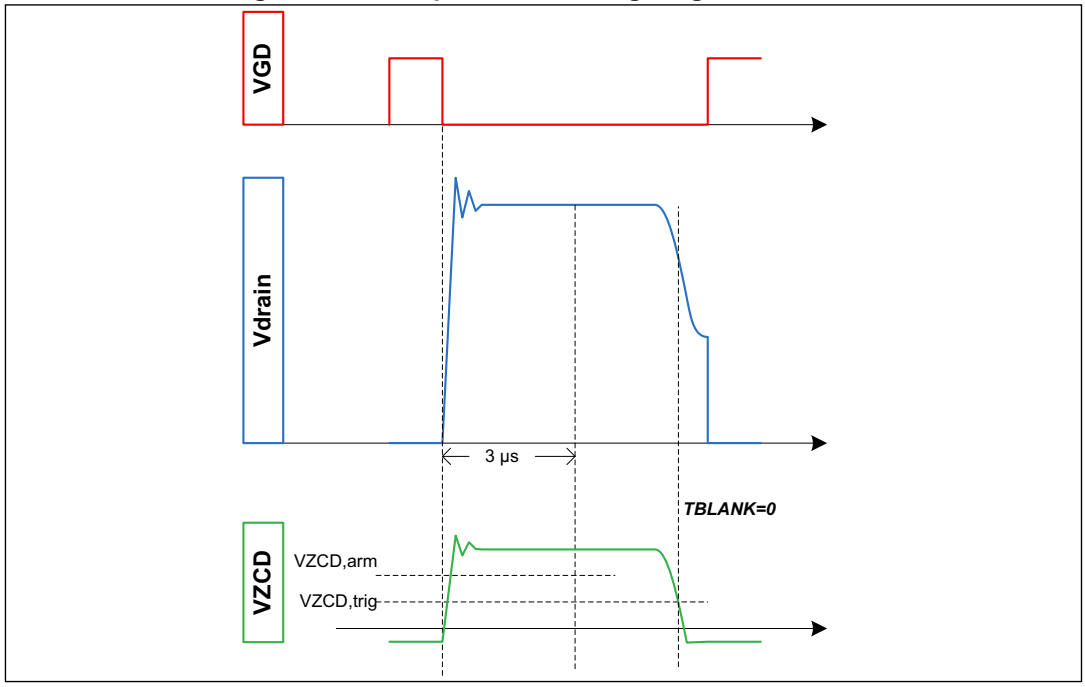


*Figure 13* is the case when TOFF voltage is lower than 2 V, the first valley subsequent to TBLANK,var is used as a trigger signal to turn-on the MOSFET gate driver resulting in valley skipping.

**Figure 13. Example: TOFF voltage lower than 2 V and resulting in valley skipping**

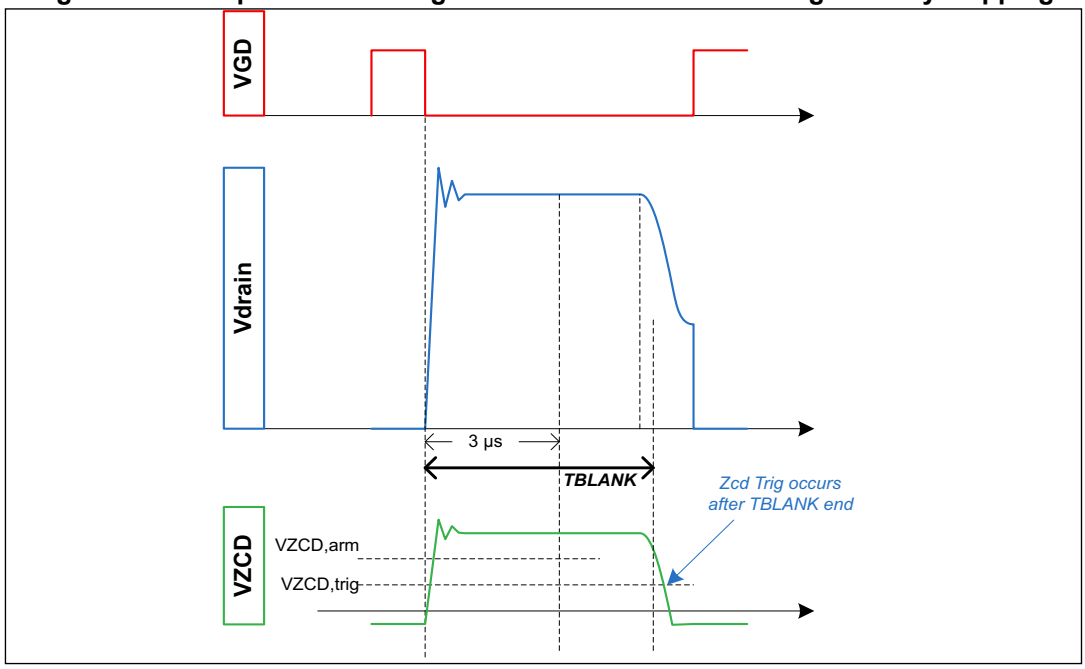
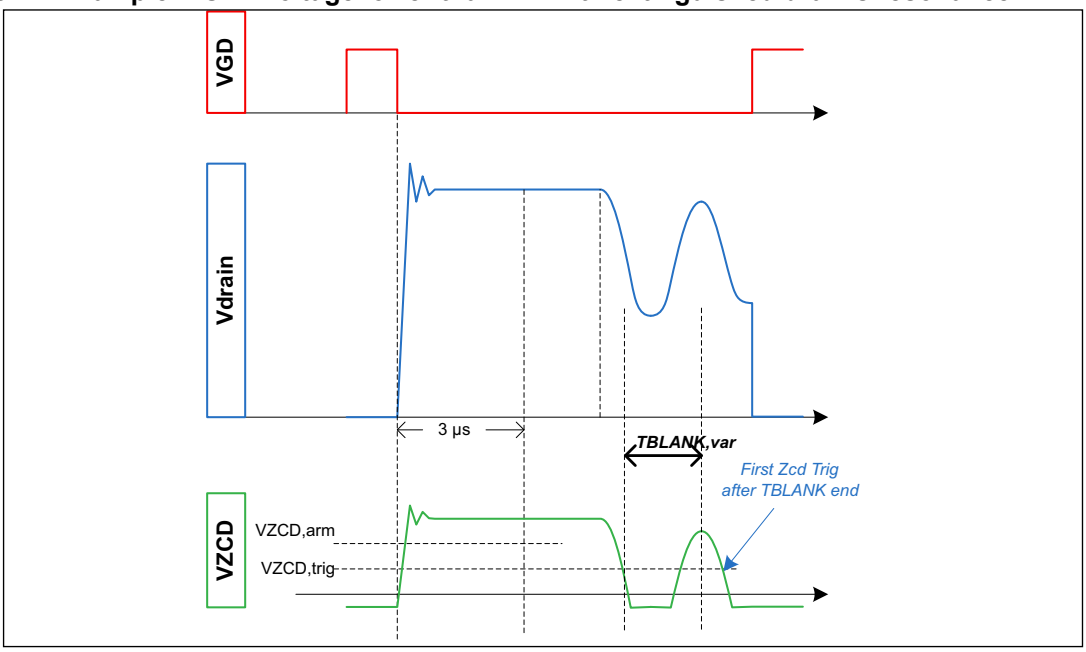


*Figure 14* is the case when TOFF voltage is lower than 2 V, and the selected TBLANK,var ends after the drain oscillation almost extinguished its amplitude: being the ZCD level above the arming threshold after the very first 3 µs (Tblank,min), the HVLED001A waits for a triggering signal, during the following 3 µs (min.) timeout. When the timeout elapses the internal starter forces the gate driver turn-on.

**Figure 14. Example: TOFF voltage lower than 2 V with extinguished drain's resonance**



## 1.6 Control loop

*[Involved pins 4: FB, 6: ZCD]*

The HVLED001A is able to operate either with an optocoupler based control loop or a primary side regulated control loop (constant output voltage only).

The FB pin can be used respectively as a pull-up current generator for optocoupler output and as output of the primary side regulator operational amplifier. In both cases a part of (or whole) the compensation network is connected between the FB and GND pin.

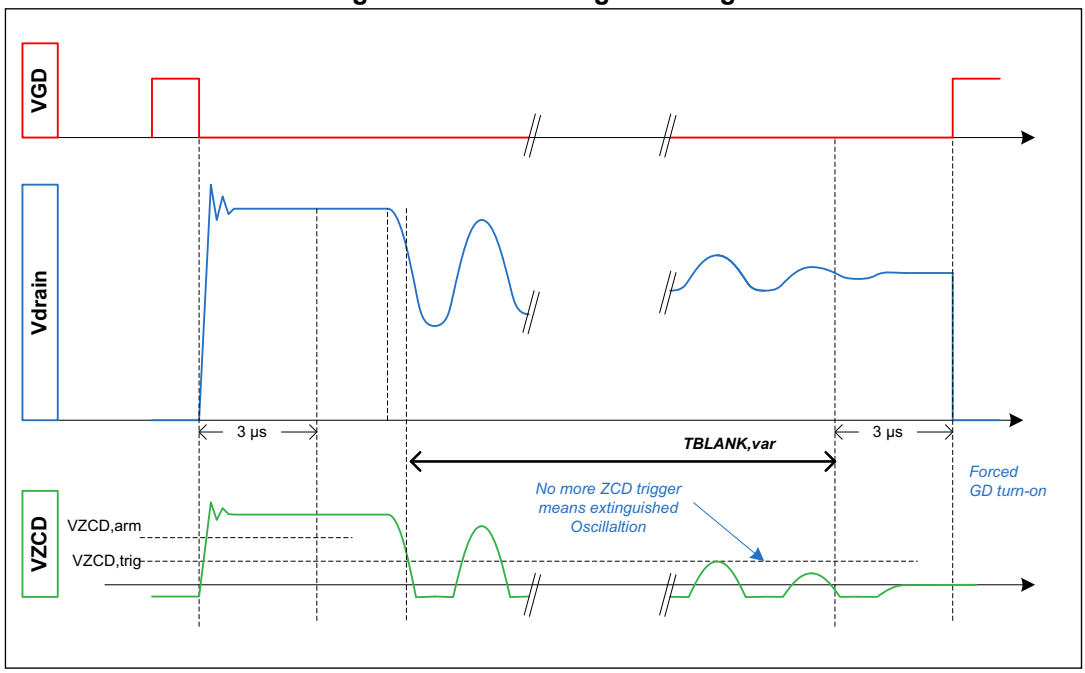
### 1.6.1 Primary side regulation

A block diagram of the blocks involved in closing the control loop is depicted in *Figure 15*.

When the entire energy stored in the transformer is transferred to the load, the rectifier current reaches zero as well as the voltage drop across the said diode.

As a consequence, the voltage across the secondary side at the demagnetization instant is exactly equal to output voltage; the same voltage is also present across all other windings, scaled by the relevant transfer ratio, in particular the auxiliary winding on the primary side is monitored by the ZCD pin.

**Figure 15. PSR management logic**




The ZCD pin DEMAG LOGIC acquires this value and feeds it to the inverting pin of the internal error amplifier (E/A) to close the control loop.

The E/A is an operational transconductance amplifier (OTA) designed to operate either with narrow or wide bandwidth so that the HVLED001A is able to control equally a high power factor topology or a DC/DC topology (e.g.: flybacks fed by PFC pre-regulators).

The non-inverting pin of the E/A is connected to a high precision reference voltage (2.6 V).

The output of the E/A is connected to the FB pin, where the suitable compensation network can be placed, referred to the common potential (GND); an equivalent small signal model of

this component, useful for a compensation network definition, is illustrated in *Figure 16*, while the OTA characteristic curve is illustrated in *Figure 17*.

In case the sampled voltage is higher than (typ.) 3 V, an overshooting is occurring. In this case an additional current is sunk from the FB pin to quickly discharge the compensation network and to limit the overshooting.

**Figure 16. OTA output equivalent model**

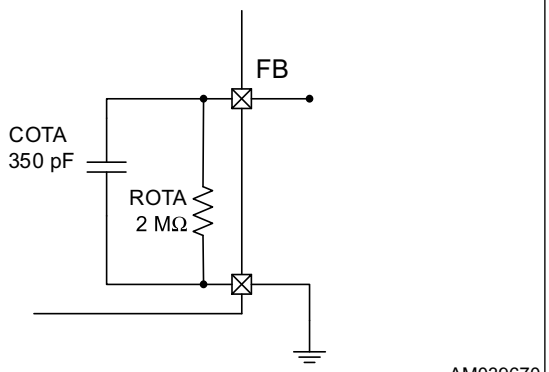
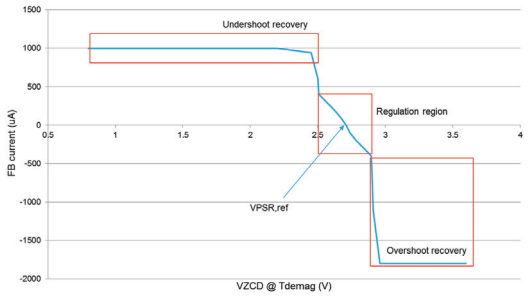


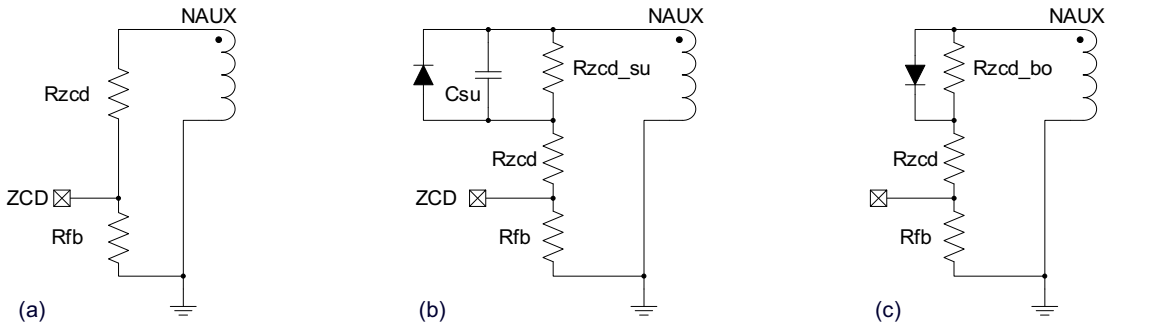

**Figure 17. OTA output characteristic**




Three different ways to implement the ZCD voltage divider are illustrated in *Figure 18*. *Figure 18* (a) shows the basic voltage divider structure, that can be replaced with a more effective structure, illustrated in *Figure 18* (b), that contains a reset diode which introduces a derivative action independent from the auxiliary voltage value during on time. This derivative action helps reducing THD.

Finally, the voltage divider with reduced equivalent resistance is illustrated in *Figure 18* (c). The brownout protection prevents the use of low values of the upper resistor during on time, so a bypass diode must be placed to differentiate between on time upper resistance (Rzcd_bo + Rzcd) and off time upper resistance (Rzcd only). In this arrangement is highly suggested to select a value for the lower resistance approximately equal to 2.7 kΩ.

**Figure 18. ZCD voltage divider settings**



### 1.6.2 Secondary side regulation

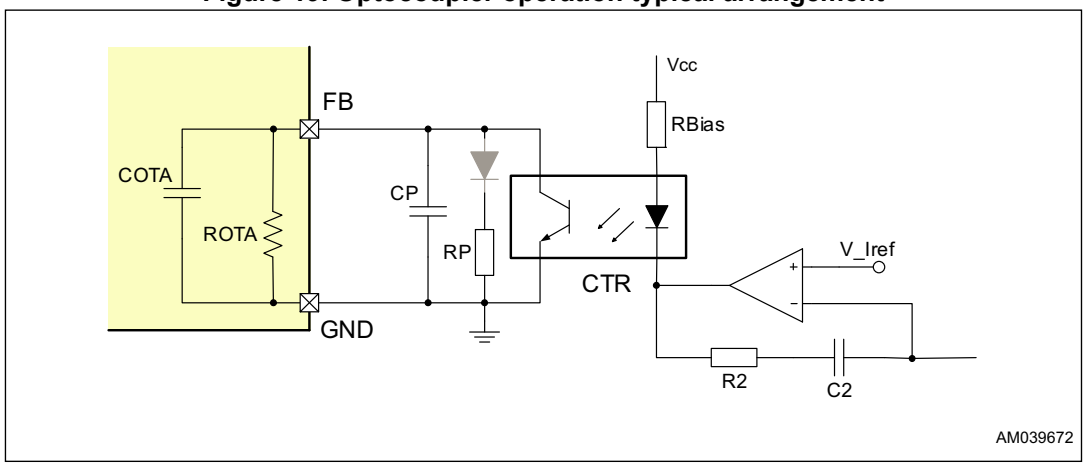
When an optocoupler is used to transfer the error information from the error amplifier placed on the secondary side, the FB pin can be used as a pull-up for the photo transistor of an optocoupler connected between FB and GND.

The pull-up current (around 1 mA) is active when the PSR error amplifier saturates high (see *Figure 17* illustrating the E/A output characteristics). To enter this mode of operation it is sufficient to set the PSR regulated voltage to a value that is higher than the maximum operating one (approximately 15% more).

Both the internal pull-up and the optocoupler output are ideal current sources; therefore they cannot drive the same node without any compensation impedance. For this reason, besides a noise canceling capacitor (CP, normally in the range 1 to 10 nF), a degeneration resistor (RP) has to be connected between the FB pin and GND. Depending on the desired bandwidth this resistor's value can be selected in a typical range between 4.7 kΩ up to 47 kΩ.

To speed up the load transients from the light to heavy load a general purpose diode may be placed in series with the resistor (with an anode connected to the FB pin).

**Figure 19. Optocoupler operation typical arrangement**




### 1.6.3 Burst mode

During the normal control operation the FB pin voltage is set (by the loop balance) between VFB,bm (lighter load) and VOFP (heavier load).

When FB voltage drops below VFB,bm, i.e.: the load is very light, the burst mode operation is entered: until the FB voltage stays in this condition, the controller generates a series of 4 GD pulses every 1 ms. The MOSFET's turn on instants between each CD pulses is determined by the detection of the ZCD as during the normal operation.

In this phase the minimum power delivered to the transformer's outputs equals:

**Equation 5**

$$P_{BM} = \frac{1}{2} \cdot L_{PRI} \cdot I_{pkp}^2 \cdot \frac{4}{1ms} = \frac{1}{2} \cdot L_{PRI} \cdot \left( \frac{V_{CS,min}}{R_{CS}} \right)^2 \cdot \frac{4}{1ms}$$

A corresponding minimum load has to be guaranteed on the transformer's outputs to dissipate this minimum energy during no-load application and to prevent the output voltage to increase without limitation.

## 1.7 Gate driving

*[Involved pins 9: GD]*

The gate driver consists on a push-pull stage whose output is able to drive an external MOSFET with the 300 mA source and 600 mA sink capability.

To avoid undesired switch-on of the external MOSFET an internal pull-down circuit holds the pin low. This circuit guarantees 2 V maximum on the pin (at Isink = 2 mA) when $V_{CC}$ is below the Vcc,shd threshold. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET used for this purpose.

## 1.8 Disabling features

*[Involved pin 5:CTRL]*

The CTRL pin embeds a set of inputs able to externally control the device activity.

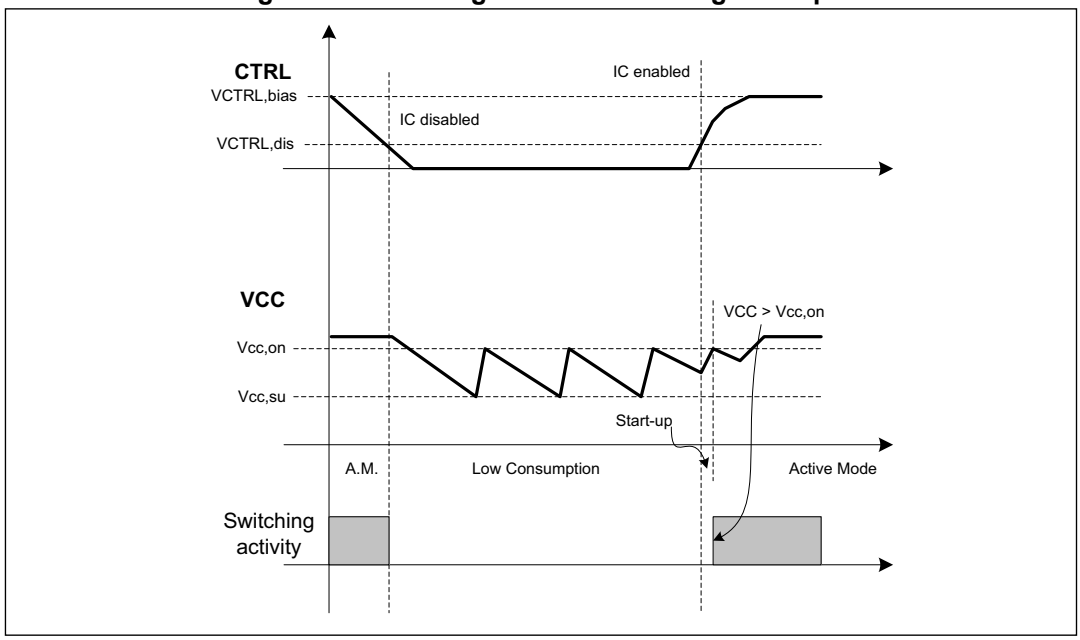
### 1.8.1 Instant disable

The device can be disabled entering into the low consumption mode since the CTRL pin is pulled below the VCTRL,dis threshold. At this occurrence the device becomes immediately inactive and the internal structures are put in the low consumption mode.

The response time of the internal comparator is very fast acting on the device status in less than 200 ns. An internal debouncing structure is also present to improve the noise immunity of this comparator. During the inactive state, the HVSU block guarantees that the VCC remains within the range VCC,su … $V_{CC}$ on. The power demand in this condition is approximately equal to 120 mW at Vin = 480 Vdc.

When the disabling signal is released, the HVSU charges the VCC pin and then the switching activity starts from the start-up state (*Figure 20*).

Figure 20. Disabling HVLED001A using CTRL pin



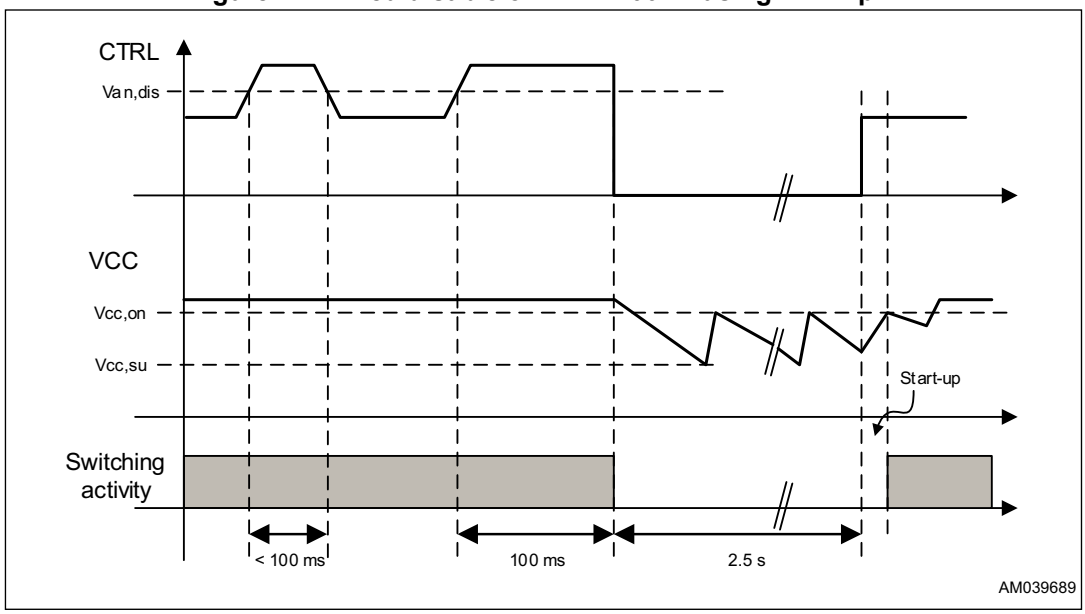

## 1.8.2 Timed disable by CTRL

The device can be also disabled when the CTRL pin is constantly kept above the threshold named Vadis for a time longer than 100 ms.

After this time the IC enters the low consumption mode activating the HVSU and the CTRL pull down resistor. It is then restarted, from the start-up state, after 2.5 s (typ.).

If the CTRL pin drops below Vadis before the 100 ms the counting timer is reset to zero (*Figure 21*).

Figure 21. Timed disable of HVLED001A using CTRL pin



## 1.9 Protections

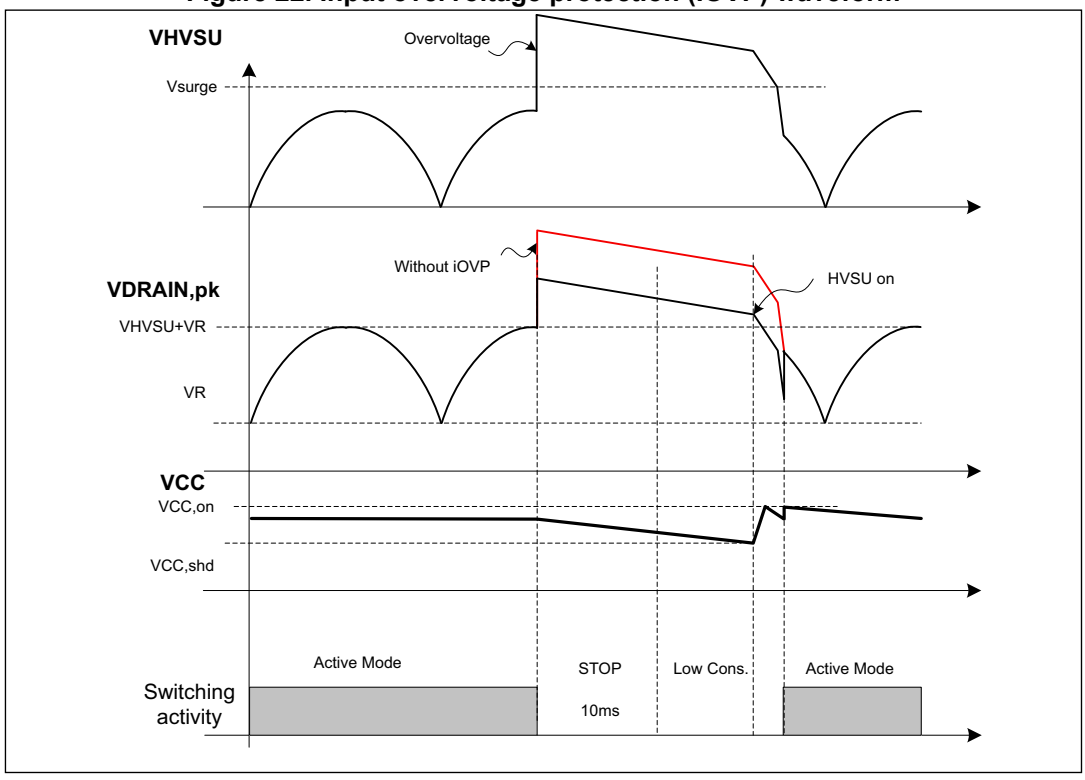
### 1.9.1 Input overvoltage and surge protection (IOVP)

*[Involved pins 1: HVSU]*

During the normal operation as the offline converter, the HVLED001A can be subjected to voltage variations, bursts and surges whose amplitude can be easily greater than 600 V. During the off time, the voltage of the MOSFET' s drain is the sum of the input voltage and the reflected voltage: the input overvoltage protection (IOVP) immediately (200 ns typ.) interrupts the switching activity of the HVLED001A device when the input voltage is higher than Vsurge. As a result, the rating of both - the MOSFET and the secondary side diode is less critical than in standard controllers.

When the protection is triggered the HVLED001A device enters the stop mode. If the HVSU voltage falls below the threshold within 10 ms, the switching activity is immediately restored, otherwise the controller enters the low consumption mode until the HVSU voltage is reduced. In the last mode of operation the internal high voltage start-up unit maintains the HVSU supplied and, contemporarily, slightly loads the input capacitor (*Figure 22*).

**Figure 22. Input overvoltage protection (IOVP) waveform**



### 1.9.2 Overload and optocoupler failure management (OFP)

*[Involved pins 4: FB]*

There are some abnormal conditions that make the FB pin voltage to rise until the output of the internal E/A saturates. Such conditions are namely:

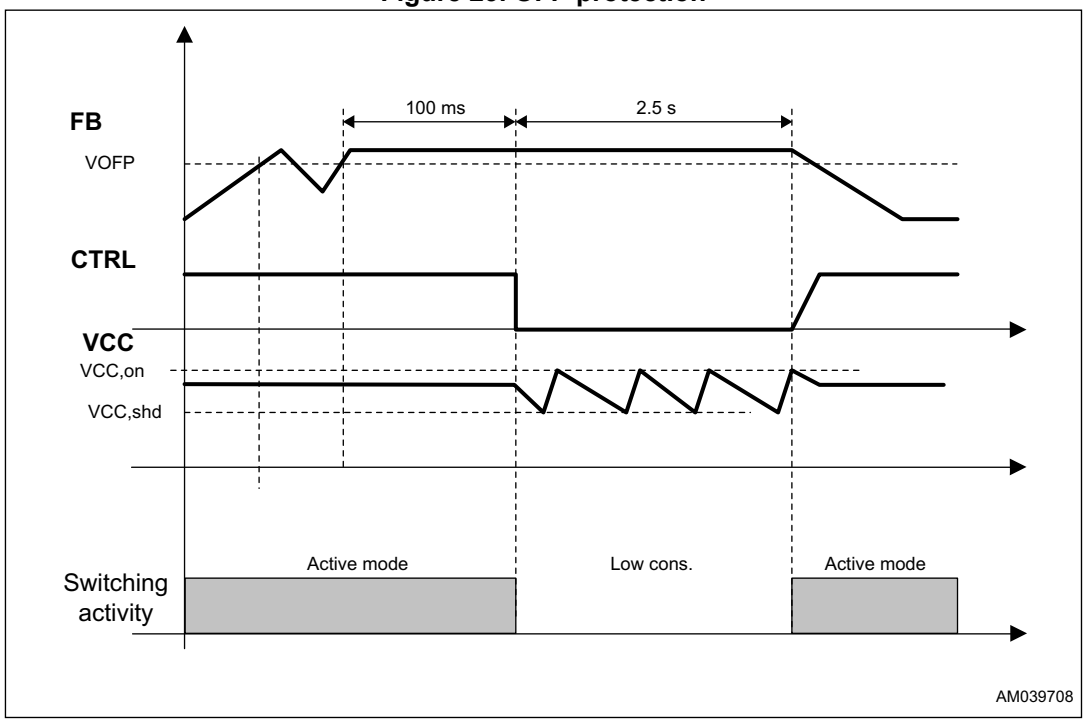
- Overload
- Short-circuit
- Optocoupler failure

While in the first two cases the E/A reacts to deliver more power to the output in order to recover a loss of output voltage, in the third case is more critical, especially when the LED string is directly connected to the application's output.

The LED load behaves as a voltage limiter so that an optocoupler failure results into an increase of the output current without an increase of the output voltage: without a dedicated protection the LED string would be destroyed.

The optocoupler failure protection (*Figure 23*) embedded into the HVLED001A stops the switching activity and enters the low consumption mode if FB pin's voltage remains above the OFP threshold for a time longer than 100 ms. The switching activity is auto restored after 2.5 s, during which the IC is supplied by the high voltage start-up unit.

**Figure 23. OFP protection**




### 1.9.3 Short-circuit detection

*[Involved pins 6: ZCD]*

In case of short-circuit on the output connector of the application, theoretically, the amplitude of the ZCD signal is insufficient to arm and trigger the ZCD comparator. Unfortunately the primary side's peak current, quite high due to the reaction of the control

loop, magnetizes the leakage inductance that, oscillating with drain's capacitance, generates a signal whose amplitude is higher than the arming threshold.

To prevent a false triggering of the ZCD comparator by those spurious oscillations, the arming threshold is checked after TBLANK,min. If the ZCD signal is lower than the arming threshold, then the starter (500 µs) is invoked. This approach minimizes the stress of the secondary side rectifier reducing the risk of hard switching.

A constant short-circuit condition either triggers the OFP protection or results in an insufficient VCC power supply.

### 1.9.4 Brownout

*[Involved pins 6: ZCD]*

Brownout protection is intended to stop the switching activity if the input voltage is constantly lower than a desired level. The input voltage is monitored by the ZCD pin using the current sunk from its internal negative clamp during the on time.

During the on time the auxiliary winding is expected to provide a negative voltage whose amplitude is proportional to the input voltage, scaled by the turn ratio between primary and auxiliary winding (NAUX/NPRI).

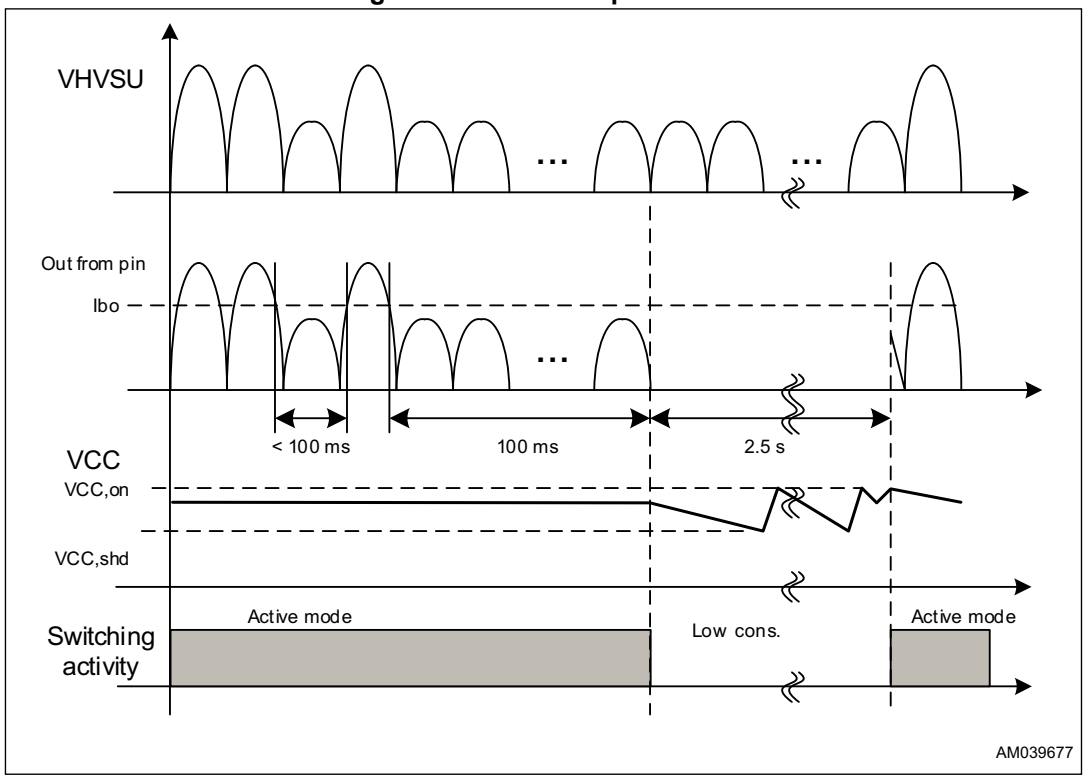
In this condition, the upper resistance of the voltage divider that is connected to the ZCD pin generates a current that is compared with a typical threshold value (100 µA):

**Equation 6**

$$I_{ZCD} = \frac{Vin \cdot \frac{NAUX}{NPRI}}{R_{zcd}}$$

A free running timer is reset anytime the current is higher than the threshold: when the count reaches 100 ms (i.e.: the current has never been sufficient to reset it) the brownout condition is met and the IC is stopped in the low consumption mode. After 2.5 s an internal auto-restart mechanism restores the switching activity (*Figure 24*).

Figure 24. Brownout protection




### 1.9.5 Magnetic saturation or rectifier short-circuit

*[Involved pins 7: CS]*

In case of either saturation of the primary side, secondary side rectifier short-circuit or the continuous mode operation the voltage across the current sense pin quickly rises above the threshold set by the multiplier. At this occurrence a second level comparator interrupts the switching activity for 1 ms before restarting the switching activity. The inactive mode associated with this protection is a special case of the stop mode.

### 1.9.6 VCC short-circuit protection

*[Involved pins 1: HVSU, 10: VCC]*

The overload or short-circuit on the VCC pin prevents the internal high voltage start-up unit to rise the VCC voltage from 0 V. On the other hand a continuous operation of the charging unit at the maximum current may result into permanent damage of the device.

For this reason, if the VCC is lower than 2 V, then the charging current of the high voltage start-up unit is reduced to a safe value.

# 2 Designing a high power factor flyback LED driver

This section describes how to design an LED driver based on the single stage flyback controlled by the HVLED001A. Guidelines on how to correctly design the transformer to obtain robust performances is presented as well as the control loop analysis of both - CC and CV (PSR) loops are illustrated.

## 2.1 Selecting the design input specifications

At first the target specification of the application needs to be defined. A list of this specification is reported in *Table 2*.

**Table 2. Typical design specification list**

| Design specs. | Parameter | Unit | Description |
|---|---|---|---|
| Mains voltage | Vmains | VAC | The range of this value can be defined in terms of the single range (e.g.: 198 ...265), wide range (100 ... 264) or universal range (90 ... 305). Within each range is very common to distinguish a narrower range of values where the optimal performances are guaranteed.<br>The class of the components of the input filter is mainly affected by this parameter. |
| Mains frequency | Fmains | Hz | The mains frequency is nominally 50 Hz or 60 Hz and is normally very precise. |
| Output LED current | ILED | mA | The average current to supply the LED. |
| Output current ripple | ΔILED% | % | Amplitude of the ripple superimposed to the LED current ILED expressed as a percentage.<br>In such kind of application it is quite large (± 30% or more). |
| LED forward voltage | VLED | V | LED total forward voltage. The range of this parameter has normally a ratio between maximum and minimum value around 3 or 4. |
| LED dynamic resistance | Rd_LED | Ω | LED dynamical resistance. It is the inverse of the slope of the LED's current/voltage curve and plays an important role in both compensation and output capacitor selection. |
| Output voltage | Vout | V | Maximum regulated output voltage during the open circuit. |
| Expected efficiency | η | % | The efficiency of the application: its main contributors are the transformer and the power semiconductors (input rectifier bridge, MOSFET and secondary side rectifier). |
| Ambient temperature | Tamb | °C | This information is important to select the class of the electrolytic capacitor and the size of the heat sinks (where needed). |

Some additional parameters can be defined starting from the specifications.

In particular the first important step is to select the value for the reflected voltage:

**Equation 7**

$$VR = (Vout + Vf) \cdot \frac{NPRI}{NSEC}$$

This term is the voltage present at the primary side of the transformer when the MOSFET is off. Its value affects the MOSFET's breakdown voltage, the MOSFET switching losses and the input current distortion (THD, see *Appendix A: Theory of QR flyback topology fed by an AC line on page 53*).

In order to obtain both - good efficiency (> 90%) and low THD (typ < 10% at Vmains max.), a reflected voltage equal to VR = 240 V is suggested.

Higher reflected voltage leads to better efficiency and THD, but the MOSFET's breakdown voltage increases and the PSR regulation is less accurate and vice-versa.

Given the reflected voltage is convenient to solve some preliminary equations to obtain both auxiliary parameters and operating voltages and currents.

**Table 3. Preliminary equations**

| Eq. no. | Description | Note |
|---|---|---|
| **Equation 8** | $K_V = \frac{Vinpk}{VR}$ | Auxiliary parameter |
| **Equation 9** | $F1(K_V) = \frac{\overline{\sin(\theta)}}{1+K_V\sin(\theta)} = \frac{1}{\pi}\int_0^{\pi} \frac{\sin(\theta)}{1+K_V\sin(\theta)} d\theta \approx \frac{0.637 + 4.6\times10^{-3}\cdot K_V}{1+0.729\cdot K_V}$ | Refer to AN1059 (on *www.st.com*) for detailed description |
| **Equation 10** | $F2(K_V) = \frac{\overline{\sin^2(\theta)}}{1+K_V\sin(\theta)} = \frac{1}{\pi}\int_0^{\pi} \frac{\sin^2(\theta)}{1+K_V\sin(\theta)} d\theta \approx \frac{0.5+1.4\times10^{-3}\cdot K_V}{1+0.815\cdot K_V}$ | Refer to AN1059 for detailed description |
| **Equation 11** | $F3(K_V) = \frac{\overline{\sin^3(\theta)}}{1+K_V\sin(\theta)} = \frac{1}{\pi}\int_0^{\pi} \frac{\sin^3(\theta)}{1+K_V\sin(\theta)} d\theta \approx \frac{0.424 + 5.7\times10^{-4}\cdot K_V}{1+0.862\cdot K_V}$ | Refer to AN1059 for detailed description |
| **Equation 12** | $N = \frac{NPRI}{NSEC} = \frac{VR}{(Vout + Vf)}$ | Transformer turn ratio |
| **Equation 13** | $Pin = \frac{Vout\cdot ILED}{\eta}$ | Maximum input power |
| **Equation 14** | $Ipkp = \frac{2\cdot Pin}{Vinpk\cdot F2(K_V)}$ | Peak value of the primary side current |
| **Equation 15** | $IDCp = \frac{1}{2} Ipkp\cdot F1(K_V)$ | DC value of the primary side current |
| **Equation 16** | $IRMSp = Ipkp\cdot\sqrt{\frac{F2(K_V)}{3}}$ | RMS value of the primary side current |

**Table 3. Preliminary equations (continued)**

| Eq. no. | Description | Note |
|---|---|---|
| **Equation 17** | $Ipks = \frac{2 \cdot ILED}{K_V \cdot F2(K_V)}$ | Peak value of the secondary side current |
| **Equation 18** | $IDCs = \frac{1}{2} Ipkp \cdot F1(K_V)$ | DC value of the secondary side current |
| **Equation 19** | $IRMSs = Ipks \cdot \sqrt{K_V \cdot \frac{F3(K_V)}{3}}$ | RMS value of the secondary side current |
| **Equation 20** | $IACi = \sqrt{IRMS_i^2 - IDC_i^2} \quad i = p, s$ | AC value of primary / secondary side current |

## 2.2 Transformer design guide lines

Given the preliminary calculation of operating parameters, the proper design of the flyback transformer can be accomplished.

### 2.2.1 Primary inductance selection

Usually the transformer's primary inductance is selected to set the minimum switching frequency to a suitable value.

Using the HVLED001A device a further constraint has to be considered at first to properly operate the smart ZCD detection (see *Section 1.5.2: SMART ZCD detection on page 17*).

It must be guaranteed that the demagnetization time is longer than 3 µs when the output of the multiplier is higher than 0.7 V, otherwise a false missed magnetization condition is detected and an abnormal operation is obtained (500 µs of the inactive state is observed).

The following equations find the relation between the demagnetization time, output of multiplier and primary inductance:

**Equation 21**

$$Tdemag = \frac{L_{SEC} \cdot Ipks}{Vout + Vf}$$

Rewritten the previous equation using the turn ratio a primary side rated version can be obtained:

**Equation 22**

$$Tdemag = \frac{1}{N} \frac{L_{PRI} \cdot Ipkp}{(Vout + Vf)} = \frac{L_{PRI} \cdot Ipkp}{VR}$$

The peak of the primary current can be easily related to the CS pin voltage using the value of the current sense resistor.

**Equation 23**

$$Tdemag = \frac{L_{PRI} \cdot VCS}{VR \cdot R_{CS}}$$

The value of RCS is selected to exploit the entire VCS dynamic: therefore its value can be expressed as the ratio between the maximum value of VCS (VCS,lim = 750 mV) and the maximum value of the primary current (at maximum load and minimum input voltage) Ipkp,max.

**Equation 24**

$$R_{CS} = \frac{VCS,lim}{Ipkp,max}$$

Substituting *Equation 24* into *Equation 23*, the demagnetization time can be written using known parameters.

**Equation 25**

$$Tdemag = \frac{L_{PRI} \cdot VCS \cdot Ipkp,max}{VR \cdot VCS,lim}$$

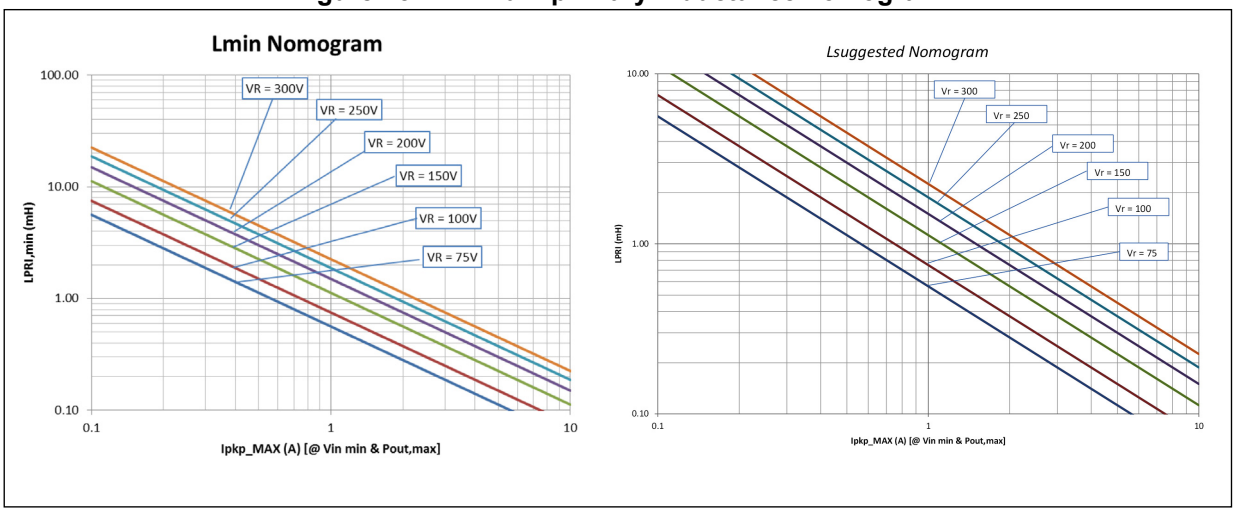
Re-arranging the terms and considering that 0.7 V / VCS,lim = 0.95, the minimum primary inductance, given a desired reflected voltage and the maximum primary current, can be written as:

**Equation 26**

$$L_{PRI,min} \geq \frac{4.3\,\mu \cdot VR}{Ipkp,max \cdot 0.93}$$

The equation is also expressed as nomogram as illustrated in *Figure 25*, together with the nomogram related to the primary side inductance's suggested value to obtain the best performance.

**Figure 25. Minimum primary inductance nomogram**




The value of the Ipkp,max can be obtained using *Equation 14* with maximum input power and minimum input voltage.

### 2.2.2 Core size selection

The size of the flyback transformer can be differently approached to optimize different parameters. Besides the different techniques, a valid starting point to select core's size is the use of the area product calculation.

Two expressions for determining the minimum required core area-product (winding window area times effective magnetic cross section in $cm^4$) will be provided:

**Equation 27**

$$AP_{min} = \left[\frac{460 \cdot Pin,max}{fsw,min \cdot (1+K_V) \cdot \sqrt{F2(K_V)}}\right]^{1.316}$$

**Equation 28**

$$AP_{min} = \left[\frac{480 \cdot Pin,max}{fsw,min \cdot (1+K_V) \cdot \sqrt{F2(K_V)}}\right]^{1.585} \cdot [J_H(K_V) \cdot fsw,min + J_E(K_V) \cdot fsw,min^2]^{0.66}$$

where $J_H$ ($K_V$) and $J_E$ ($K_V$) are functions related to hysteresis and eddy current losses, whose best fit approximation are respectively:

**Equation 29**

$$J_H(K_V) = \frac{1.87 + 1.26 \cdot K_V}{1 + 0.55 \cdot K_V} \cdot 10^{-5}$$

**Equation 30**

$$J_E(K_V) = \frac{1.88 + 1.06 \cdot K_V}{1 + 0.34 \cdot K_V} \cdot 10^{-10}$$

*Equation 27* assumes that the maximum peak flux density inside the core is limited by core saturation and that all transformer losses are located in the windings; *Equation 28* assumes that core losses limit the flux swing and the total dissipation are half due to core losses and half to windings losses.

Common to both formulas are the following assumptions:

1. the material is a typical power ferrite with a saturation flux density above 0.3 Tesla;
2. the windings occupy 40% of the total window area to leave space for isolation layers, creepage and clearance distances;
3. primary and secondary winding wires are proportioned for equal RMS current density;
4. core and/or copper losses result in 30 °C hot spot temperature rise (no forced cooling);
5. skin and proximity effects are neglected, considering the frequency range involved.

For a given fsw,min, one should try both formulas (considering $K_V$ at minimum line voltage) and use the higher resulting value.

### 2.2.3 Turn selection

The number of primary side turn can be written considering the maximum allowable magnetic flux (Bmax) and the core's effective area (listed into magnetic core datasheet).

**Equation 31**

$$NPRI = \frac{L_{PRI} \cdot Ipkp,max}{Bmax \cdot Ae}$$

The primary-to-secondary side turn ratio is defined by reflected voltage selection (*Equation 12 on page 32*), while the primary-to-auxiliary side turn ratio is selected based on both power supply and ZCD triggering considerations.

Auxiliary winding can be coupled accordingly to primary side (flyback configuration) or to primary side (forward configuration).

The first arrangement can be adopted when the output voltage range is small and the PSR operation is needed to control Vout:

**Equation 32**

$$\frac{VLED,min}{Vout} < \frac{VZCD,arm}{Vref,PSR}$$

In this case the auxiliary turn number has to be set in order to obtain a Vaux higher than Vcc,shd when the LED voltage is minimum. Often a simple linear regulator is beneficial to set the VCC voltage within the pin's voltage allowed range.

**Equation 33**

$$\frac{NPRI}{NAUX} = \frac{VLED,min}{Vaux} \cdot \frac{NPRI}{NSEC}$$

When the output voltage range is wider than calculated in *Equation 32* the ZCD signal must be obtained using an alternate structure and/or the VCC has to be obtained connecting the auxiliary winding in forward configuration.

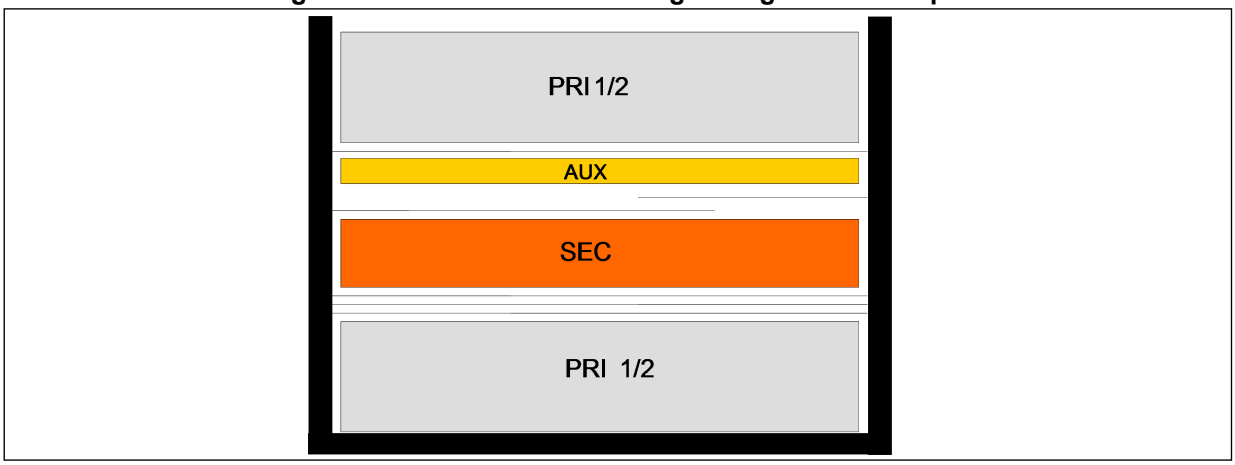
In case of forward configuration auxiliary voltage variation has the same variation of the input voltage and a linear regulator can be used, even in universal mains application, to limit the VCC excursion. Being the rectified mains a half sinusoid, is preferable to consider, as minimum input voltage for the turn ratio selection, the RMS value of the input mains rather than its peak value. Doing so, some margin is automatically taken into account.

**Equation 34**

$$\frac{NPRI}{NAUX} = \frac{Vinmin_{(RMS)}}{Vaux}$$

Different winding arrangement can be done: one arrangement example that reduces the primary side leakage inductance and gives good regulation facts is illustrated in *Figure 26*.

**Figure 26. Transformer's winding arrangement example**




### 2.2.4 Transformer design equation summary

*Table 4* summarizes the equations to be used designing the transformer.

**Table 4. Transformer design equations**

| Parameter | Equation | |
|---|---|---|
| Primary inductance | *Equation 26* $L_{PRI,min} \geq \frac{4.3\,\mu \cdot VR}{Ipkp,max \cdot 0.93}$ | |
| Area product (must be higher than the maximum between the two) | *Equation 27* $AP_{min} = \left[\frac{460 \cdot Pin,max}{fsw,min \cdot (1+K_V) \cdot \sqrt{F2(K_V)}}\right]^{1.316}$ | |
| | *Equation 28* $AP_{min} = \left[\frac{480 \cdot Pin,max}{fsw,min \cdot (1+K_V) \cdot \sqrt{F2(K_V)}}\right]^{1.585} \cdot [J_H(K_V) \cdot fsw,min + J_E(K_V) \cdot fsw,min^2]^{0.66}$ | |
| Primary side turn number | *Equation 31* $NPRI = \frac{L_{PRI} \cdot Ipkp,max}{Bmax \cdot Ae}$ | |
| "Pri to sec" turn ratio | *Equation 12 on page 32* $N = \frac{NPRI}{NSEC} = \frac{VR}{(Vout + Vf)}$ | |
| "Pri to aux" turn ratio | Flyback configuration | *Equation 33* $\frac{NPRI}{NAUX} = \frac{VLED,min}{Vaux} \cdot \frac{NPRI}{NSEC}$ |
| | Forward configuration | *Equation 34* $\frac{NPRI}{NAUX} = \frac{Vinmin_{(RMS)}}{Vaux}$ |

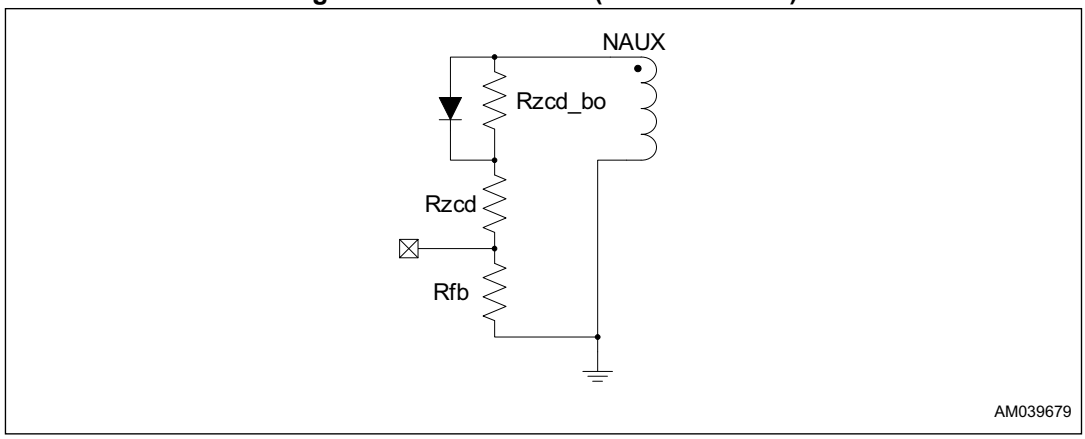
## 2.3 ZCD network definition

The ZCD network's functions are listed in *Table 1 on page 5*.

### 2.3.1 ZCD network to implement PSR (simple resistive network)

The ZCD network suitable to regulate output voltage with PSR function using resistors only is illustrated in *Figure 27*.

**Figure 27. ZCD network (PSR - resistive)**




**Equation 35**

$$Rfb = 2.7k\Omega$$

(suggested value)

**Equation 36**

$$Rzcd = Rfb \cdot \left( \frac{Vout - Vfzcd}{VREF,PSR} \cdot \frac{NAUX}{NSEC} - 1 \right)$$

*Vfzcd* is the voltage drop of the diode in parallel with Rzcd_bo.

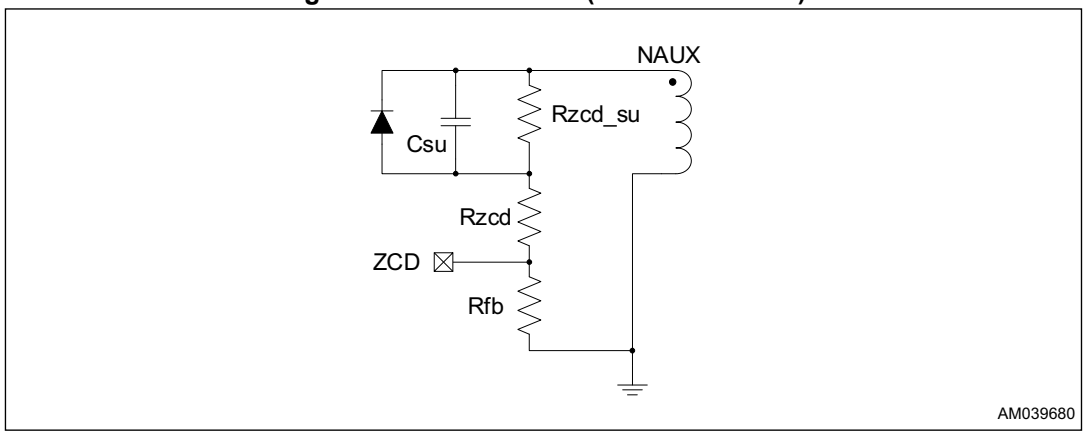
**Equation 37**

$$Rzcd\_bo = \frac{Vin \cdot \frac{NAUX}{NPRI}}{I_{BO}} - Rzcd$$

### 2.3.2 ZCD network to implement PSR (network with derivative components)

The ZCD network suitable to regulate output voltage with PSR function including the derivative contribution to compensate the sample and hold capacitive behavior is illustrated in *Figure 28*.

**Figure 28. ZCD network (PSR - derivative)**




This network needs some fine tuning, but can work with higher resistance values.

**Equation 38**

$$Rzcd = \frac{Vin \cdot \frac{NAUX}{NPRI}}{I_{BO}}$$

**Equation 39**

$$Rzcd\_su = Rzcd$$

**Equation 40**

$$Csu \cong \frac{0.5\mu s}{Rzcd}$$

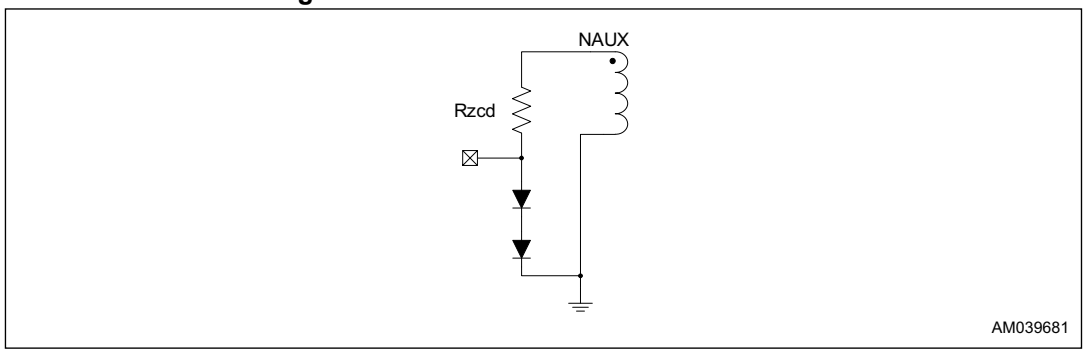
**Equation 41**

$$Rfb = \frac{Rzcd}{\left(\frac{Vout}{VREF,PSR} \cdot \frac{NAUX}{NSEC} - 1\right)}$$

### 2.3.3 ZCD network to operate without PSR

The ZCD network suitable to disable the PSR function is illustrated in *Figure 29*: the diodes (standard type, like 1N4148) allows to generate a ZCD signal having amplitude that is higher than VZCD,arm and lower than VREF,PSR. This configuration sets the FB pin to operate as a constant current source to bias the optocoupler output.

**Figure 29. ZCD network to disable the PSR**



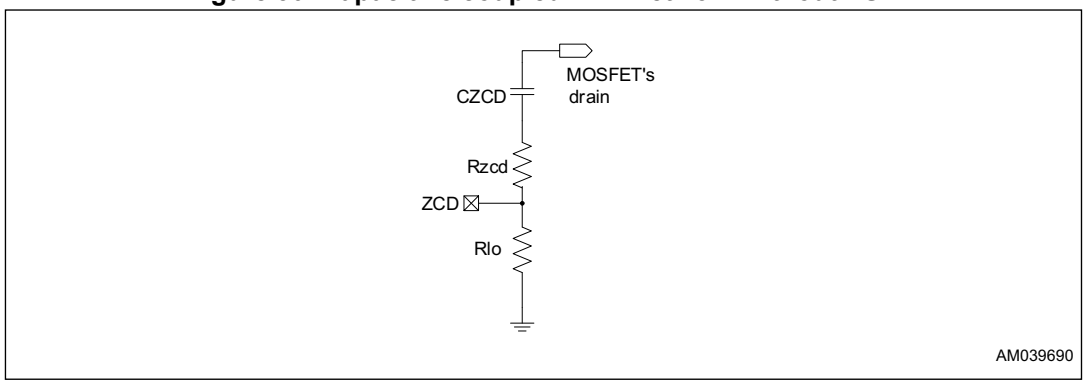

**Equation 42**

$$Rzcd = \frac{Vin \cdot \frac{NAUX}{NPRI}}{I_{BO}}$$

### 2.3.4 ZCD network driven by MOSFET's drain

An alternate connection of the ZCD network consists on connecting it to the MOSFET's drain through an RC network as illustrated in *Figure 30*.

**Figure 30. Capacitive coupled ZCD network without PSR**




This network is useful when, due to the auxiliary winding forward connection, the auxiliary signal is not available to detect the demagnetization's oscillations.

The CZCD is charged at Vin: in fact the network is supplied by an almost square wave whose amplitude is equal to:

$$Vin + (Vout + Vf_{sec}) \cdot \frac{NPRI}{NSEC} = Vin + VR$$

and whose duty cycle is equal to (1 - D), where *D* is the MOSFET's duty cycle and equates:

**Equation 43**

$$D = \frac{VR}{(Vin + VR)}$$

Therefore the average capacitor's voltage can be derived averaging this square wave:

**Equation 44**

$$V_{CZCD} = (Vin + VR) \cdot \left(1 - \frac{VR}{Vin + VR}\right) = Vin$$

The resistor can therefore be selected to satisfy the following relation:

**Equation 45**

$$Rzcd = \frac{Vin,max}{I_{BO}}$$

In order to guarantee correct valley detection, the time constant of this structure must be longer that the maximum expected damping time of the drain node oscillations. In practical flyback circuitries this time is normally around 40 µs.

**Equation 46**

$$CZCD = \frac{40\mu}{Rzcd}$$

This network is normally used with or without PSR and the value of Rlo can be found considering that VR is present across voltage divider:

**Equation 47**

$$\begin{cases} Rlo = Rzcd \cdot \left(\frac{VPSR,REF}{N \cdot Vout - VPSR,REF}\right) & \text{PSR is active} \\ Rlo = 2 \times \text{Standard diode} & \text{PSR disabled} \end{cases}$$

## 2.4 Active components definition

### 2.4.1 Input rectifier bridge

The input rectifier bridge should be able to withstand a reverse voltage greater than the input voltage peak's value.

**Equation 48**

$$Vbr\_rev > 2 \cdot Vinpk,max$$

An integrated or non-integrated bridge can be used depending on thermal and manufacturing considerations.

The maximum value of the RMS current flowing into the bridge is equal to:

**Equation 49**

$$Ibr\_f = \frac{Pin}{Vmains,min}$$

The power losses associated with the bridge can be estimated (with margin) as:

**Equation 50**

$$Pbr = Ibr\_f \cdot 2 \cdot Vf\_br$$

Where *Vf_br* is the forward voltage drop of a single diode of the bridge.

### 2.4.2 Secondary side rectifier

The output rectifier bridge should be able to withstand a reverse voltage greater than:

**Equation 51**

$$Vbr > Vout + Vinpk,max \cdot \frac{NSEC}{NPRI}$$

The maximum current that flows in the diode is Ipks (*Equation 17 on page 33*).

The diode's power losses are:

**Equation 52**

$$Pdsec = Vth \cdot IDCs + Rdsec \cdot IRMSs$$

The terms Vth and Rdsec can be found in the diode's datasheet.

### 2.4.3 MOSFET selection

The MOSFET must have a breakdown voltage greater than:

**Equation 53**

$$Vbrdss = Vinpk,max + VR + Vspike$$

Vspike in *Equation 53* is the allowed amplitude of the oscillations occurring between the transformer's leakage inductance and drain capacitance.

The Rds,on of the MOSFET can be selected as the best trade-off between cost and power losses performances.

The losses associated with the MOSFET are mainly dominated by conduction losses (Pcond) when the input voltage is low, while they are dominated by capacitive losses (Pcap) when the input voltage is high.

**Equation 54**

$$Pcond = Rds,on \cdot IRMSp^2$$

The capacitive losses are associated with the discharge of the capacitance present at the MOSFET drain. Therefore it is proportional to overall drain capacitance (Cdrain) and switching frequency. The last parameter varies over the half sinusoid: the average value of said frequency can be used to evaluate the switching losses.

**Equation 55**

$$fsw,avg = \frac{1}{\Pi}\int_0^{\Pi} \frac{Vinpk}{L_{PRI} \cdot Ipkp} \cdot \frac{1}{1 + K_V \cdot \sin\theta} d\theta$$

**Equation 56**

$$Pcap = fsw,avg \cdot \left\{ 3.3 \cdot Coss \cdot \left[ \frac{2 \cdot (Vinpk - VR)}{\pi} \right]^{\frac{3}{2}} + \frac{1}{2} \cdot C_{Drain} \cdot \left[ \frac{2 \cdot (Vinpk - VR)}{\pi} \right]^2 \right\}$$

The sum the of power losses contribution has to be considered to refine the MOSFET's selection and the size of the eventual heat sink.

### 2.4.4 Clamping device selection

Two different clamping structures can be applied in parallel with the transformer's primary side to limit the overvoltage spikes due to the leakage inductance of the transformer (Vspike): the RCD clamp (*Figure 31*) and Transil™ based clamp (*Figure 32*).

**Figure 31. RCD clamp**

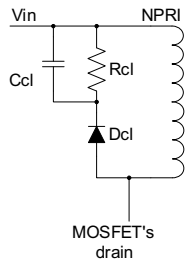
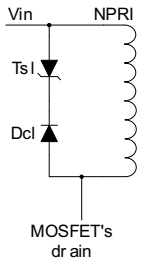



**Figure 32. Transil clamp**




Considering the RCD clamp, the capacitor is selected so as to have Vspike (as a rule of the thumb, half the reflected voltage) at turn-off such that the voltage rating of the MOSFET is never exceeded.

From energetic balance, it is possible to write:

**Equation 57**

$$Ccl = \frac{Llk \cdot Ipkp,max^2}{Vspike \cdot (Vspike + 2 \cdot VR)}$$

The term *Llk* in *Equation 57* is the leakage inductance of the transformer. Normally, it can be minimized between approximately 1% and 3% of LPRI. The capacitor undergoes large current spikes and therefore it should be a very low ESR type with a polypropylene or polystyrene dielectric film.

The minimum resistor value can be found by imposing that the voltage on the capacitor at the beginning of each switching cycle never falls below the reflected voltage:

**Equation 58**

$$Rcl \geq \frac{1}{fsw,min \cdot Ccl \cdot ln\left(1 + \frac{Vspike}{VR}\right)}$$

The term *fsw,min* in *Equation 58* can be derived by *Equation 55* calculated when the minimum input voltage is applied. The power rating of this resistor can be estimated by considering the DC dissipation due to the reflected voltage and the leakage inductance energy:

**Equation 59**

$$P(Rcl) = \frac{fsw,min}{2} \cdot Llk \cdot Ipkp,max^2 \cdot (1 + K_{Vmin}) \cdot F2(K_{Vmin}) + \frac{VR^2}{Rcl}$$

The diode will be rated for repetitive peak currents equal to Ipkp,max, and with a breakdown voltage greater than Vpk,max + VR.

Considering the Transil based clamp, its clamping voltage can be approximated with its breakdown voltage. In fact, the peak current is quite small and it is possible to neglect the contribution due to the dynamic resistance. The breakdown voltage, which should account for the drift due to the temperature rise, will then be:

**Equation 60**

$$Vbr\_tsl = VR + Vspike$$

The steady-state power dissipation capability must be at least:

**Equation 61**

$$P(Tsl) = \frac{fsw,min}{2} \cdot Llk \cdot Ipkp,max^2 \cdot (1 + K_{Vmin}) \cdot F2(K_{Vmin}) \cdot \frac{Vbr\_tsl}{Vbr\_tsl - VR}$$

The rating of the diode follows the same rules of the RCD-based Transil structure.

## 2.5 Input and output filter definition

### 2.5.1 Output capacitor

The output capacitor undergoes the AC component of the secondary current. The current ripple (similarly to voltage ripple) has two components: a high frequency ripple due to finite ESR of the capacitor and the low frequency ripple due to the twice line frequency envelope.

The high frequency ripple can be expressed as (it has been supposed that ESR << Rd_LED that is the LED dynamical resistance):

**Equation 62**

$$\Delta Io_{HF} = Ipks \cdot \frac{ESR}{Rd\_LED}$$

To calculate the low frequency ripple an auxiliary variable needs to be defined (see AN1059 for further details):

**Equation 63**

$$H2(K_V) = \frac{1}{\pi} \cdot \left| \int_0^{\pi} \frac{\sin^2(\theta) \cdot \cos(2\theta)}{1 + K_V \cdot \sin(\theta)} d\theta \right| \cong \frac{0.25 - 1.5 \cdot 10^{-3} \cdot K_V}{1 + 1.074 \cdot K_V}$$

The low frequency ripple can be expressed as:

**Equation 64**

$$\Delta Io_{LF} = \frac{1}{\pi} \cdot \frac{H2(K_V)}{F2(K_V)} \cdot \frac{ILED}{Fmains \cdot Cout}$$

The Cout voltage rating must be higher than Vout plus some additional margin.

### 2.5.2 Input capacitor

The input capacitor undergoes the high frequency component of the input (line) current. The goal is to prevent this high frequency from its transferring back to the line.

Once defined the maximum allowed percentage ripple (f_HF), the capacitor value can be found as:

**Equation 65**

$$\Delta Iin_{HF} = \frac{1}{2\pi} \cdot \frac{1}{r\_HF \cdot Pin \cdot fsw,min}$$

The rating of the capacitor must be at least higher than Vinpk,max.

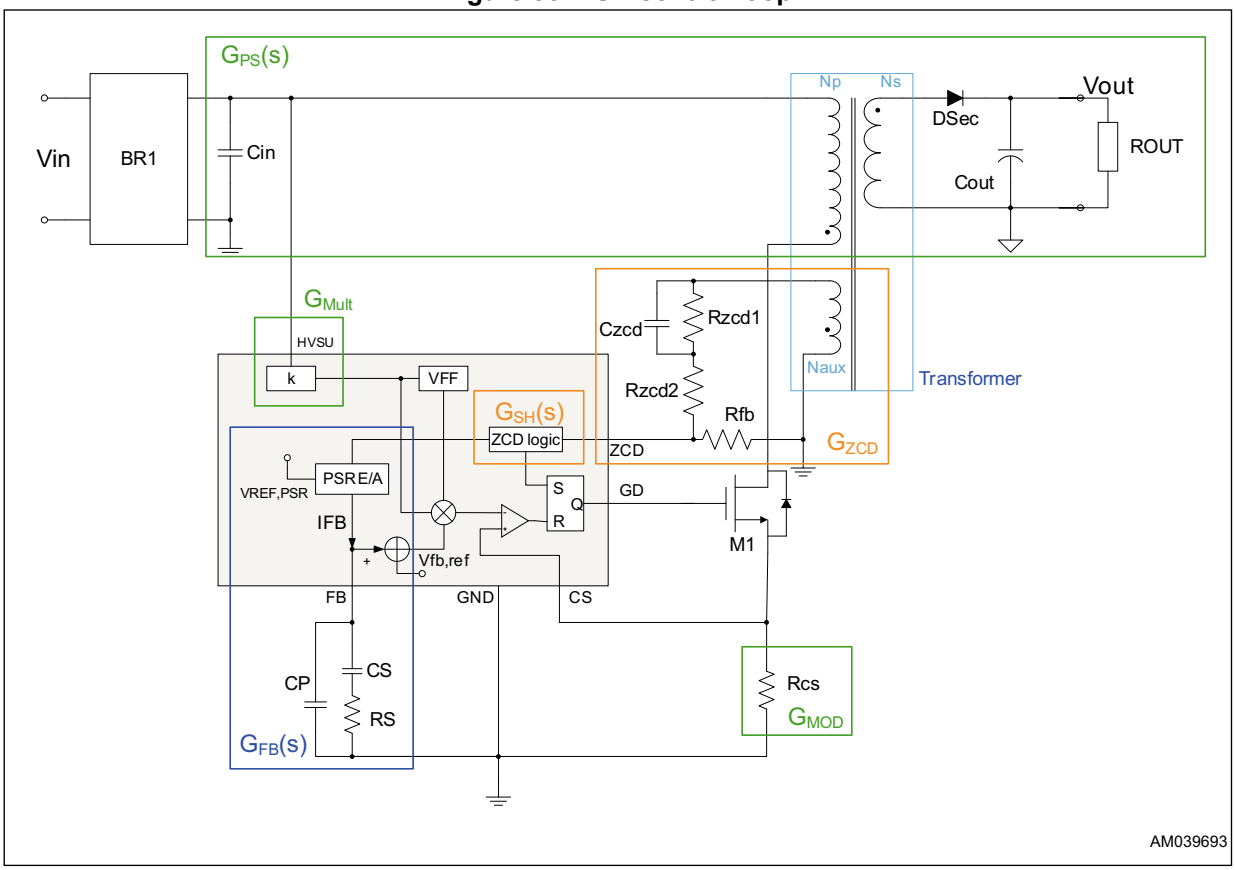
An X2 type film capacitor is suggested.

## 2.6 Control loops definition

### 2.6.1 PSR control loop

In order to compensate the PSR loop, the open loop transfer function has to be derived starting from its elementary components (see *Section 1.6.1: Primary side regulation on page 22*). The compensation network will be placed between the FB pin and GND.

**Figure 33. PSR control loop**



At first the plant transfer function can be written as:

**Equation 66**

$$Ap(s) = G_{PS}(s) \cdot G_{Mult} \cdot G_{MOD} = \left[ \frac{K_V \cdot F2(K_V)}{1+\Gamma(K_V)} \cdot \frac{N}{2} \cdot ROUT \cdot \frac{1+s \cdot ESR \cdot Cout}{1+s \cdot \frac{ROUT \cdot Cout}{1+\Gamma(K_V)}} \right] \cdot km \cdot \frac{1}{R_{CS}}$$

The term $\Gamma(K_V)$ in *Equation 66* is equal to:

**Equation 67**

$$\Gamma(K_V) \cong \frac{1+1 \cdot 10^{-3} \cdot K_V}{1+0.8 \cdot K_V}$$

The plant transfer function has a low frequency pole and high frequency zero: the zero could be neglected, being the narrow bandwidth a requirement to obtain a good PF and THD.

The effect of ZCD input circuitry can be written as:

**Equation 68**

$$G_{EA\_in}(s) = G_{ZCD} \cdot G_{SH}(s) = \left[ \frac{NAUX}{NSEC} \cdot \frac{Rfb}{Rfb + Rzcd} \right] \cdot \left[ \frac{1}{1+s\frac{4\pi}{fsw}} \right]$$

Depending on the ZCD voltage divider, the Rzcd term assumes different means - please refer to *Section 2.3: ZCD network definition on page 38* for a complete description of the possibilities.

The internal sample and hold introduces a pole whose frequency depends on the operating frequency.

Finally the compensation network connected between the FB and GND allows obtaining the desired bandwidth tuning the singularities position. Its transfer function is:

**Equation 69**

$$G_{FB}(s) = gm \cdot ROTA \cdot \frac{1+s \cdot RS \cdot CS}{(1+s \cdot ROTA \cdot CS) \cdot (1 + s \cdot RS \cdot (CP+COTA))}$$

ROTA and COTA have been introduced in *Figure 16 on page 23* and are respectively equal to 2 MΩ and 350 pF.

*HINTS:*

It can be convenient to set the zero's frequency equal to the low frequency pole of the plant transfer function and act on the poles of the compensation network to obtain the desired bandwidth.

In case the PSR loop is used as an output voltage limit of a constant output current application, the bandwidth is wider than in a HPF application. This aspect has to be taken into account when setting the zero/pole position.

### 2.6.2 Optocoupler based control loop (constant current)

In order to compensate the loop based on the optocoupler (constant output current), the open loop transfer function has to be derived.

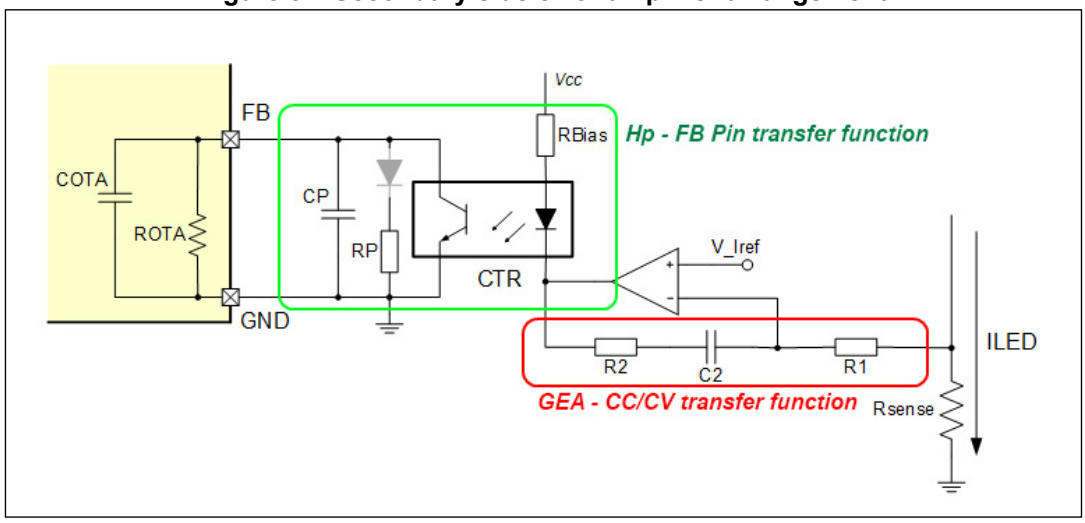
The plant transfer function can be written as:

**Equation 70**

$$Ap(s) = G_{PS}(s) \cdot G_{Mult} \cdot G_{MOD} = \left[ \frac{K_V \cdot F2(K_V)}{1 + \Gamma(K_V)} \cdot \frac{N}{2} \cdot \frac{1 + s \cdot ESR \cdot Cout}{1 + s \cdot \frac{Rd\_LED \cdot Cout}{1 + \Gamma(K_V)}} \right] \cdot km \cdot \frac{1}{R_{CS}}$$

The error amplifier section is on the secondary side and includes the relevant compensation network [GEA(s)] the optocoupler and relevant biasing means [Hp(s)] as illustrated in *Figure 34*.

**Figure 34. Secondary side error amplifier arrangement**




**Equation 71**

$$Hp(s) = \frac{Rsense}{RBias} \cdot CTR \cdot \frac{RP \cdot ROTA}{RP + ROTA} \cdot \left[ \frac{1}{1 + s \cdot \frac{RP \cdot ROTA}{RP + ROTA} \cdot (CP + COTA)} \right]$$

The pole of *Equation 71* is normally set on relatively high frequency, but the DC gain of said frequency represents an important tuning factor to set the bandwidth to a low value.

The RP can eventually be placed in series with a diode if its value is lower than VFB,dis / IFBpu = 15 kΩ.

The compensation network is finally designed according to its transfer function:

**Equation 72**

$$G_{EA}(s) = \frac{1 + s \cdot (R1 + R2) \cdot C2}{s \cdot C2 \cdot R2}$$

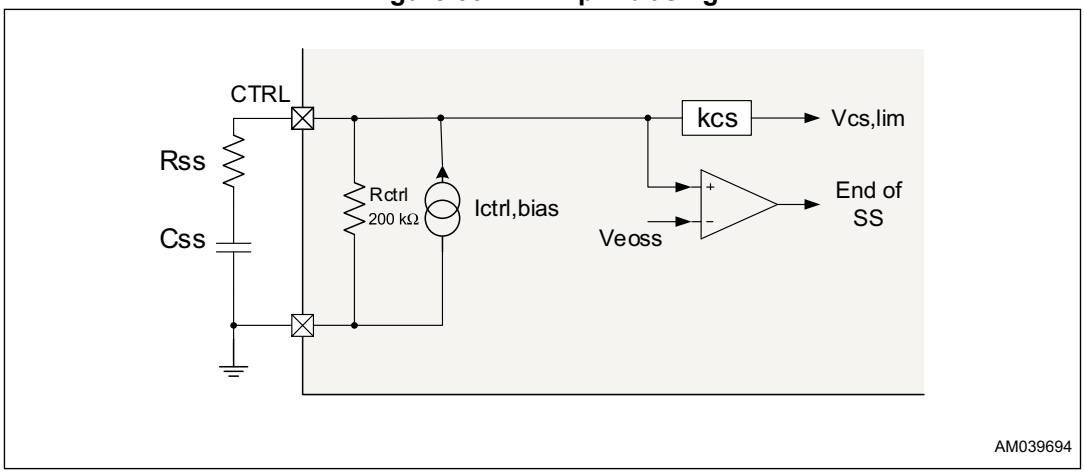
The zero of $G_{EA}$ can be used to cancel the plant transfer function's low frequency pole.

## 2.7 Soft-starting the application

When the application is turned on, the output capacitor needs to be charged to reach the operating voltage. During this phase the control loop is saturated high to transfer the maximum energy to the secondary side resulting into two main effects: the initial rectifier current is very high (inrush current) and an overshoot appears due to the narrow loop's bandwidth.

The capacitor connected to the CTRL pin can be used to limit the inrush current and, eventually, to reduce the overshooting by means of the reduction of the maximum primary side current. It is convenient to add a resistor in series with the capacitor as illustrated in *Figure 8 on page 14* and *Figure 35* to bypass the CTRL disable feature (*Section 1.8.1: Instant disable on page 25*).

**Figure 35. CTRL pin biasing**




Said RC network can be designed as follows:

**Equation 73**

$$Rss \cong \frac{VCTRL,dis}{Ictrl,bias}$$

The soft-start phase is accomplished when CTRL voltage reaches Veoss. The size of Css can be selected to obtain the desired soft-start time (Tss):

**Equation 74**

$$Css \cong \frac{Tss}{(Rctrl + Rss)} \cdot \frac{1}{-\ln\left[\left(1+\frac{Rss}{Rctrl}\right)\cdot\left(1+\frac{Veoss}{Vctrl,bias}\right)\right]}$$

## 2.8 Supplying the application

The device has to be supplied by a generator having an average current capability higher than operating ICC: normally the auxiliary winding of the transformer is sufficient (self-supplied applications), but different requirements may need the implementation of separate controllers (separate supplied applications - e.g.: when the application belongs to a complex subsystem). Whatever the supplying method is adopted, a decoupling diode between the supplying source and the VCC pin is required for a proper functionality of the HVSU.

The present section is focused on self-supplied applications only. The different load characteristics lead to different constraints or an external circuitry approach.

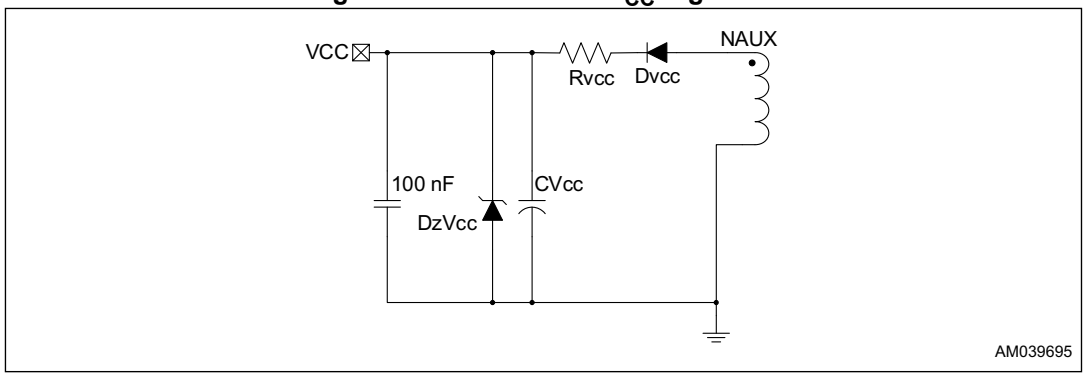
### 2.8.1 Simple Zener regulator

A constant output voltage application, normally, can be supplied directly by the auxiliary winding as illustrated in *Figure 36*: this structure has to be designed to limit the maximum VCC voltage during overshooting thanks to the Zener diode DzVcc. The Zener clamping voltage must be lower than the VCC pin's absolute maximum rating and its current has to be limited by Rvcc; said resistor represents an additional voltage drop between Vaux and $V_{CC}$.

**Equation 75**

$$Vcc,min \cong Vaux - Vf,Dvcc - ICC,max \cdot Rvcc$$

**Figure 36. Zener based $V_{CC}$ regulator**




The size of the capacitor $CV_{CC}$ can be estimated considering a trade-off between the required hold-up time (Thold-up, at least 10 ms to sustain the VCC during the stop mode occurring at the beginning of an input overvoltage event) and the start-up time.

**Equation 76**

$$CVcc > \frac{Thold - up \cdot ICC,max}{Vcc,min - Vcc,su_{max}}$$

The resulting start-up time can be estimated as:

**Equation 77**

$$Tstart-up = CVcc \cdot \left( \frac{Vcc,su_{start-up}}{Icharge,su} + \frac{Vcc,on - Vcc,su_{start-up}}{Icharge} \right) + 2 \cdot Arcsin\left( \frac{1}{2\pi \cdot Fmains} \cdot \frac{VHVstart}{Vinpk,min} \right)$$

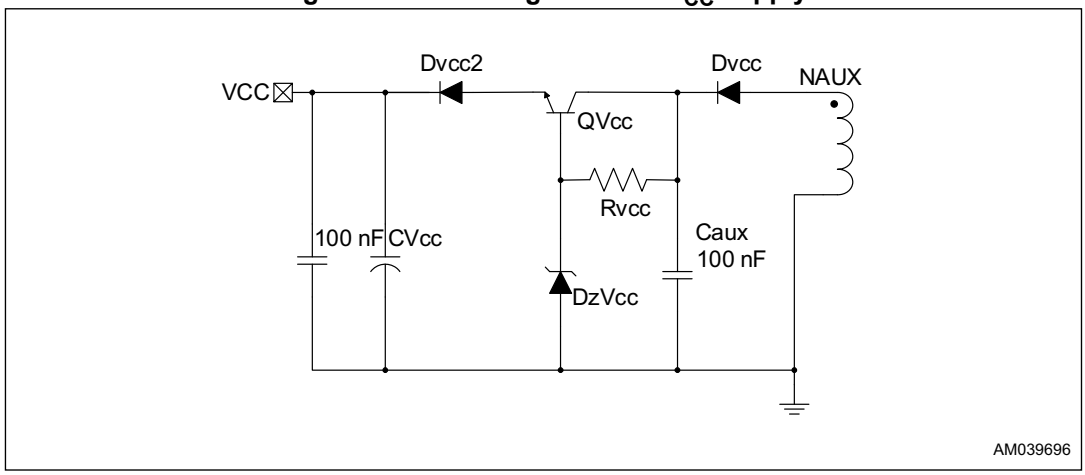
The second term in *Equation 77* represents the additional delay time that can be present when the application is turned when Vin is lower than VHV,start.

## 2.8.2 Linear voltage regulator

There are several situations when the simple Zener regulator is inappropriate. As an example, when the aux. voltage varies over a wide range of values (LED drivers) the Zener diode must dissipate any extra voltage exceeding its rating. As a result both very huge dissipation and regulated voltage increasing could occur when aux. voltage is at maximum value.

Linear regulator (*Figure 37*) helps reducing the Zener dissipation.

**Figure 37. Linear regulator for $V_{CC}$ supply**




The Vbe rating of $QV_{CC}$ must be higher than maximum aux. voltage, while its package depends on the associated thermal resistance that allows to keep the $QV_{CC}$ junction temperature below the desired value.

The diode $D_{VCC}2$ prevents the base to emitter the junction of $QV_{CC}$ from being reverse biased by the start-up network (a high voltage start-up unit of the HVLED001A).

$DzV_{CC}$ value can be set as the sum of the operating $V_{CC}$ value and twice standard diode's forward voltage drop (2 x 0.7 V).

Finally the value for $R_{VCC}$ has to be set in order to bias both - the base current and Zener diode:

**Equation 78**

$$Rvcc = \frac{Vaux,min - Vf_{Dvcc} - V_{DzVcc}}{hfe \cdot ICC,max + I_{DzVcc}}$$

The Zener biasing current ($I_{DzVcc}$) is usually in the range of few tenths of µA, while *hfe* is reported in the NPN transistor datasheet.

The $CV_{CC}$ value is set using *Equation 76* and *Equation 77*. In case the resulting start-up time is too long a trick can be adopted: selecting a lower $CV_{CC}$ value and increasing the value of the Caux capacitor to a suitable level. This arrangement ensures contemporarily a quick start-up (the HVSU charges $CV_{CC}$ only) and a longer hold-up time (the energy is stored into Caux).

# Appendix A Theory of QR flyback topology fed by an AC line

It can be demonstrated that the flyback topology operating in the discontinuous conduction mode is intrinsically able to operate with a high power factor. A particular case of DCM is the quasi resonant (QR) flyback that, in respect of the standard DCM, optimizes the efficiency and reduces the high frequency output current ripple. A unity power factor is obtained when the input current is sinusoidal and in phase with the input voltage.

To obtain almost sinusoidal input current absorption, the HVLED001A device modulates sinusoidally the peak of the primary side current, but, at the same time, also the duty cycle (D) is modulated. As a result: the PF and the THD of the input current cannot be respectively 1 and 0, but their theoretical limit can be calculated. At first, some preliminary conditions need to be assumed:

- The multiplier is perfectly linear so that Ipkp(ɵ) = Ipkp · sin(ɵ)
- The feedback signal (FB voltage) is perfectly constant over a mains cycle
- The transformer is ideal so that perfect winding coupling can be assumed
- The MOSFET is turned on immediately after demagnetization (Tdemag)

The current absorbed by a flyback converter can be written as:

**Equation 79**

$$Iin(t) = \frac{1}{2} Ipkp(t) \cdot D$$

It is convenient to express the currents and voltages in terms of the angular phase to extend the equations to any input frequency:

The expression for the duty cycle can be obtained writing the expressions for Ton and Toff periods.

**Equation 80**

$$T_{ON} = \frac{L_{PRI} \cdot Ipkp(\theta)}{Vin(\theta)} = \frac{L_{PRI} \cdot I_{pkp}}{Vinpk}$$

**Equation 81**

$$T_{OFF} = \frac{L_{SEC} \cdot Ipks(\theta)}{Vout + Vf} = \frac{\frac{L_{PRI}}{N^2} \cdot N \cdot Ipkp(\theta)}{Vout + Vf} = \frac{L_{PRI} \cdot Ipkp(\theta)}{N(Vout + Vf)} = \frac{L_{PRI} \cdot Ipkp(\theta)}{VR}$$

Combining *Equation 79* and *Equation 82* it is possible to write the expression of the input current.

**Equation 82**

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{1}{1 + \frac{Vinpk}{VR} \cdot |\sin(\theta)|} = \frac{1}{1 + K_V \cdot |\sin(\theta)|}$$

**Equation 83**

$$Iin(\theta) = \frac{1}{2} Ipkp \cdot \frac{|\sin(\theta)|}{1 + K_V |\sin(\theta)|}$$

*Equation 83* contains a distortion term (the denominator of the fractional term) that is equal to one only if $K_V$ equals zero. Practically the ratio between the peak and reflected voltage cannot be zero.

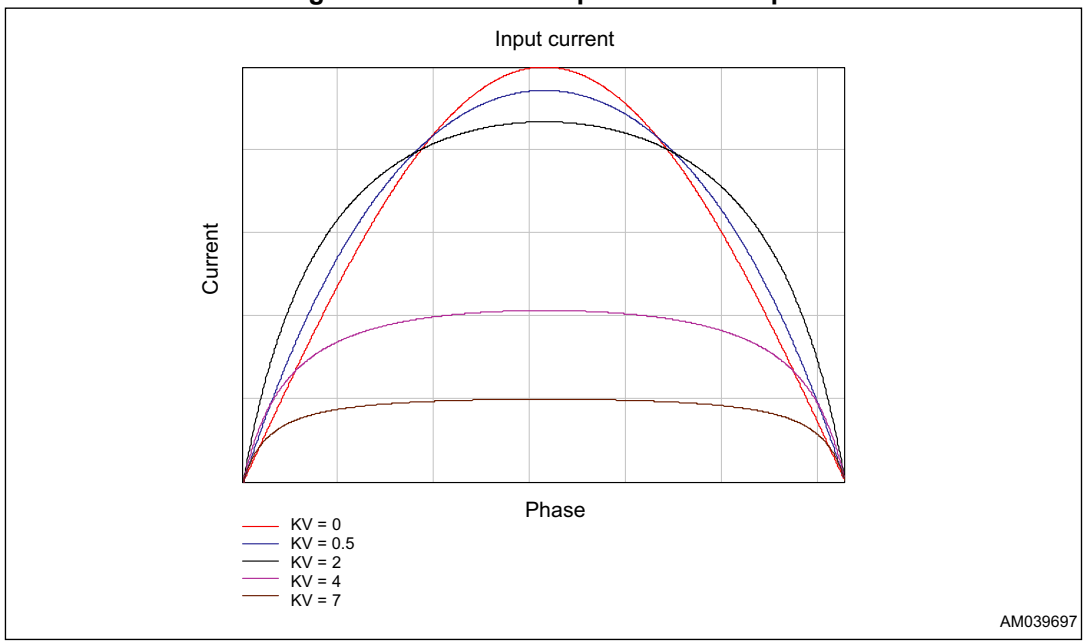
Considering that the reflected voltage is typically fixed between 150 V and 250 V and the output voltage could also be variable over a range from 4 to 1, the minimum value of the parameter $K_V$ can be around 0.5 in a wide range applications at minimum line voltage.

The maximum value of this parameter is reached at maximum input voltage and minimum output voltage: in a wide range applications $K_V > 7$ can be easily reached.

*Figure 38* illustrates, in the same graph, the normalized input line voltage (red line) and the input line currents at different condition. The worst case is a wide range application having an input voltage range from 90 Vac ($K_V = 0.5$) to 305 Vac. Output voltage can vary by a factor 4 obtaining, at maximum output voltage a $K_V$ varying between around 2 and 7.

The input current amplitudes are normalized to the same RMS values if output condition is constant, and are adjusted if output voltage decreases.

**Figure 38. Estimated input current shape**




The expression for THD and PF associated with the input current can be explicitly obtained.

**Equation 84**

$$PF = \frac{Iin_{RMS,1st\_harmonic}}{Iin_{RMS}}$$

**Equation 85**

$$Iin_{RMS,1st\_harmonic} = \frac{Pin}{Vin} = \frac{\sqrt{2}\cdot Pin}{Vinpk}$$

**Equation 86**

$$Pin = \frac{1}{2}Vinpk \cdot Ipkp \frac{\overline{\sin^2(\theta)}}{1+K_V \sin(\theta)} = \frac{1}{2}Vinpk \cdot Ipkp \cdot F2(K_V)$$

**Equation 87**

$$Iin_{RMS} = \frac{1}{2}\cdot Ipkp \cdot \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{\sin(\theta)}{1+K_V \sin(\theta)}\right]^2 d\theta}$$

Using *Equation 85*, *Equation 86* and *Equation 87* into *Equation 84* and exploiting numerical analysis an approximate expression for PF, depending on $K_V$ can be found:

**Equation 88**

$$PF(K_V) = 1 - 8.1\times10^{-3}K_V + 3.4\times10^{-4}K_V^2$$

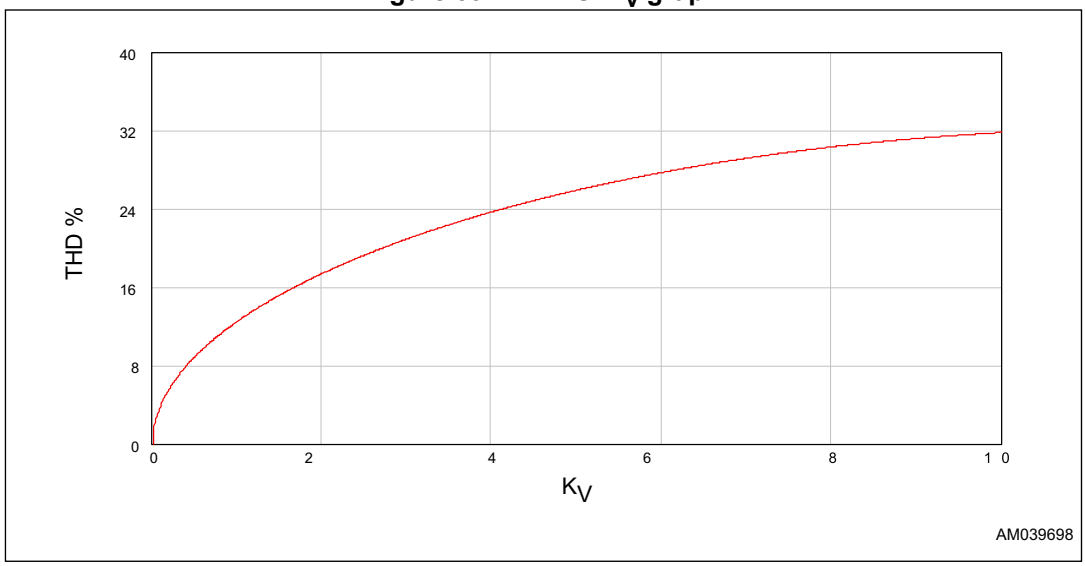
Neglecting the distortion related with input capacitance, the THD can be related to PF using the following expression:

**Equation 89**

$$THD(K_V) = \sqrt{\frac{1}{[PF(K_V)]^2} - 1}$$

*Equation 89* gives a measurement of the distortion already noticed looking at *Figure 39*.

**Figure 39. THD vs. $K_V$ graph**



# Appendix B List of abbreviations

The list of the abbreviations adopted in this application note is reported in this appendix. The symbols corresponding to HVLED001A electrical characteristics can be found in the relevant datasheet.

**Table 5. List of abbreviations**

| Symbol | Description |
|---|---|
| C2 | Capacitor of secondary side compensation network belonging to feedback network (CC mode) |
| Ccl | Primary side clamp capacitor |
| $C_{drain}$ | Total capacitance of the drain's node |
| Cin | Input capacitor connected after the rectifier bridge |
| Coss | MOSFET's drain to source capacitance |
| Cout | Output capacitor |
| CP | Capacitor of primary side compensation network directly placed between FB and GND |
| CS | Capacitor of the R/C of the primary side compensation network |
| Css | Capacitor of the typical R/C network connected to CTRL pin |
| Csu | Speed up capacitor of the ZCD network |
| $C_{VCC}$ | VCC bulk capacitor |
| D | Duty cycle of MOSFET |
| Dcl | Primary side clamp rectifier |
| DSec | Secondary side rectifier |
| $D_{VCC}$ | VCC rectifier diode |
| DZ_clamp | Primary side clamp Zener |
| DzVcc | VCC limiting Zener |
| Fmains | Mains frequency |
| $f_{Resonance}$ | Frequency of the main resonance of the flyback topology |
| fsw | Switching frequency (avg., min. or max.) |
| Iin | Input current |
| ILED | Average value of LED current |
| Ipkp,max | Peak of primary current - max. value |
| Ipkp,min | Peak of primary current - min. value |
| IZCD,on | ZCD pin |
| $K_V$ | Ratio between input peak and reflected voltage |
| Llk | Transformer's leakage inductance |
| $L_{PRI}$ | Primary inductance of flyback transformer |
| $L_{SEC}$ | Secondary side inductance of flyback transformer |
| N | Primary-to-secondary turn ratio |

**Table 5. List of abbreviations (continued)**

| Symbol | Description |
|---|---|
| NAUX | Number of turns of transformer's auxiliary (primary side) winding |
| NPRI | Number of turns of transformer's primary side winding |
| NSEC | Number of turns of transformer's secondary side winding |
| $P_{BM}$ | Minimum deliverable power during burst mode |
| Pin | Input power |
| Pout | Output power |
| R1 | Resistor of secondary side compensation network connecting E/A with shunt (CC mode) |
| R2 | Resistor of secondary side compensation network belonging to feedback network (CC mode) |
| Rbias | Optocoupler input biasing resistor |
| Rcl | Primary side clamp resistor |
| $R_{CS}$ | Primary side shunt resistor connected in series with the source of the MOSFET |
| Rds,on | MOSFET's Rds,on |
| Rd_LED | LED dynamical resistance |
| Rfb | Lower resistor of the ZCD network |
| Rhvsu | Resistor in series with high voltage start-up pin |
| Rmin | Secondary side bleeder resistor |
| ROUT | Equivalent output capacitor |
| RP | Resistor of primary side compensation network directly placed between FB and GND |
| RS | Resistor of the R/C of the primary side compensation network |
| Rshunt | Secondary side shunt resistor |
| Rss | Resistor of the typical R/C network connected to CTRL pin |
| Rzcd | Upper resistor of the ZCD network |
| Rzcd_bo | Upper resistor of the ZCD network bypassed by diode when low impedance voltage divider is implemented |
| Rzcd_su | Upper resistor of the ZCD network bypassed by speed - up capacitor and/or diode |
| Tamb | Ambient temperature |
| Tcase | Case temperature |
| Tdemag | Demagnetization time of the transformer |
| $T_j$ | Junction case |
| $T_{ON}$ | MOSFET's on time |
| $T_{OFF}$ | MOSFET's off time |
| Tvalley | Time interval between MOSFET's turn-off and minimum of the first resonance oscillation |
| Tvalley_n | Time interval between MOSFET's turn-off and minimum of the n-th resonance oscillation |
| Vf | Secondary side diode forward voltage |
| VCS | Voltage of CS pin |

**Table 5. List of abbreviations (continued)**

| Symbol | Description |
|---|---|
| Vin | Input voltage |
| Vinpk | Peak value of input voltage |
| VLED | LED forward voltage |
| Vmains | Mains (AC) voltage applied to the application |
| Vout | Output voltage |
| VR | Reflected voltage |
| Vref_CC | Reference voltage for SSR - CC loop |
| Vref_CV | Reference voltage for SSR - CV loop |
| Vspike | Primary side overvoltage due to leakage inductance |
| ΔILED | Amplitude of the LED current ripple (absolute) |
| ΔILED% | Amplitude of the LED current ripple (%) |
| ΔILEDpp | Amplitude of the LED current ripple (peak to peak) |
| η | Efficiency (%) |
| ɵ | Angular phase of the mains voltage |

# Revision history

Table 6. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 08-Nov-2016 | 1 | Initial release. |
| 19-Dec-2018 | 2 | Updated *Equation 16* and *Equation 69*. Updated *Figure 20* & *Figure 22*.. |