STM32WB Series microcontrollers ultra-low-power features overview

Introduction

The STM32WB Series microcontrollers are built using an innovative architecture to reach best-in-class, ultra-low-power consumption with their high flexibility, powerful radio and advanced set of peripherals. They can operate up to 64 MHz and achieve 80 DMIPS performances at 64 MHz, thanks to the integration of the ART Accelerator with the lowest possible dynamic power consumption.

The STM32WB Series microcontrollers include a proprietary low-power RF subsystem, with its own dedicated Arm® Cortex®-M0+ to offload all the real-time RF communication tasks from the Cortex®-M4, resulting in best power efficiency distribution between the user and the communication tasks.

The STM32WB Series microcontrollers feature the FlexPowerControl, which increases flexibility in the power modes management while at the same time reducing the overall application consumption.

The STM32WB Series microcontrollers embed a large number of smart and high performance peripherals, a large set of advanced and low-power analog features, and several peripherals tuned for Low-power modes. By using the batch acquisition sub-mode (BAM), they optimize the power consumption when data is transferred using the communication peripherals, while the rest of the device is kept in Low-power mode.

Based on the solid foundations of the STM32L4 Series, already embedding several power efficient innovations minimizing the power consumption in the different modes while maintaining most of the existing peripherals, the STM32WB Series microcontrollers enable an easy migration from a dual chip solution (STM32L4 + Bluetooth Low Energy / 802.15.4) to that of a single chip, with almost the same power budget.

The STM32WB Series microcontrollers (except the STM32WBx0) include an embedded SMPS that further improves the power consumption figures in applications where the supply voltage is high, as well as the overall consumption.

Thanks to their built-in internal voltage regulator and voltage scaling (except the STM32WBx0), device consumption in active modes is kept at a minimum, whatever the external supply voltage. This makes these devices particularly suited for handheld battery-powered products, down to 1.71 V (2 V for the STM32WBx0). In addition, their multi-voltage domains (except the STM32WBx0) supply the product at low voltage (further reducing consumption) while the analog-to-digital converters operate with a higher supply and reference voltage, up to 3.6 V.

STM32WB Series microcontrollers support a battery backup domain to keep the RTC running, and a set of 20 32-bit wide, registers, that can be retained in case of power loss. This optional backup battery can be charged when the main supply is present.

The STM32WB Series microcontrollers support many Low-power modes, each of them with several sub-mode options. This allows the designer to achieve the best compromise between low-power consumption figures, shorter start-up time, available set of peripherals and maximum number of wake-up sources.

1 General information

This application note applies to the STM32WB Series microcontrollers that are Arm® Cortex® core-based devices.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Energy-efficient processing

The high Run mode processing performance (expressed in DMIPS/MHz) is achieved thanks to the use of a Cortex®-M4 core together with its associated memory interfaces. To ensure full operating performance up to 64 MHz, STM32WB Series microcontrollers embed the ART Accelerator, which masks the Flash memory access wait state, and makes it possible to achieve 1.25 DMIPS/MHz, whatever the system clock frequency.

The high energy efficiency, expressed in mA/DMIPS, is achieved by dynamically adapting the internal supply voltage to the operating frequency. This method is called “undervolting”.

STM32WB Series microcontrollers offer two dynamically selectable voltage and frequency ranges:

- Range 1 for a system frequency up to 64 MHz
- Range 2 for a system frequency up to 16 MHz with improved efficiency (up to 15% higher than Range 1).

Note: Range 2 is not supported by the STM32WBx0.

When the RF is not used, a dedicated Low-power run mode (LPRun) allows the core to operate at frequencies of 2 MHz and lower, with up to 20% improved efficiency compared to Range 2.

Note: In this case, the RF cannot be used as it requires an operating frequency of at least 32 MHz to operate.

Figure 1 shows the typical current consumption of the STM32WB35 and STM32WB55, as a function of system frequency, for different run modes.

Figure 1. Current consumption versus Cortex®-M4 system frequency (25 °C)

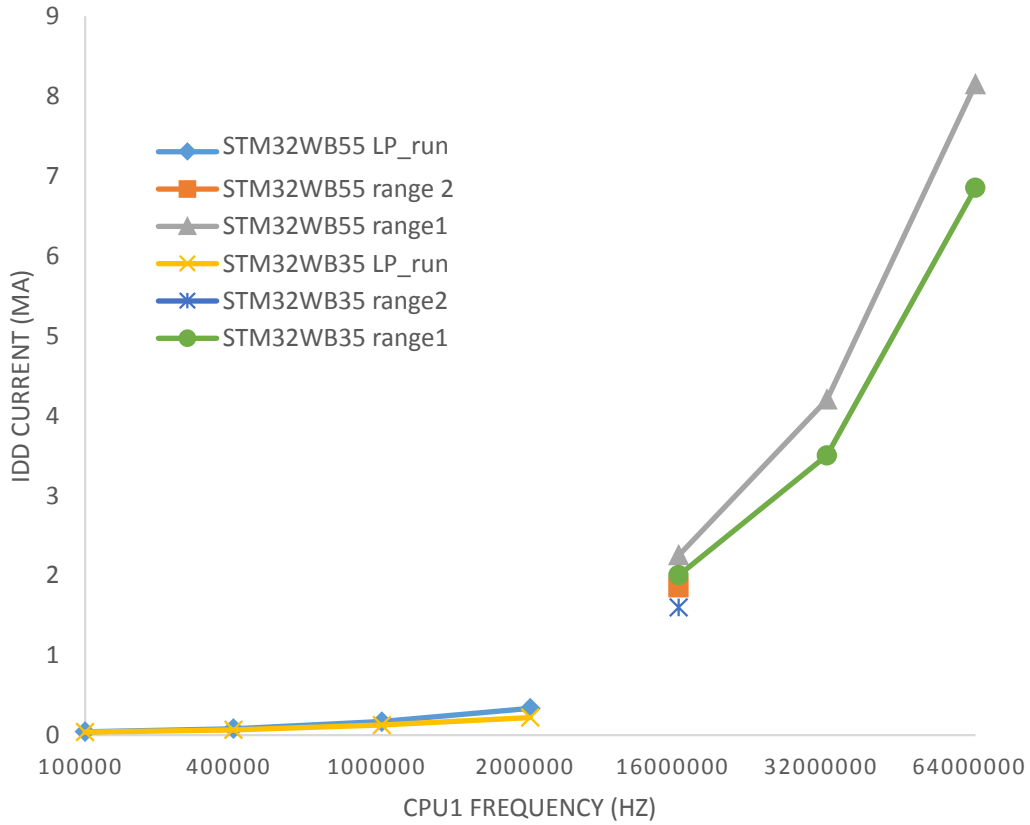
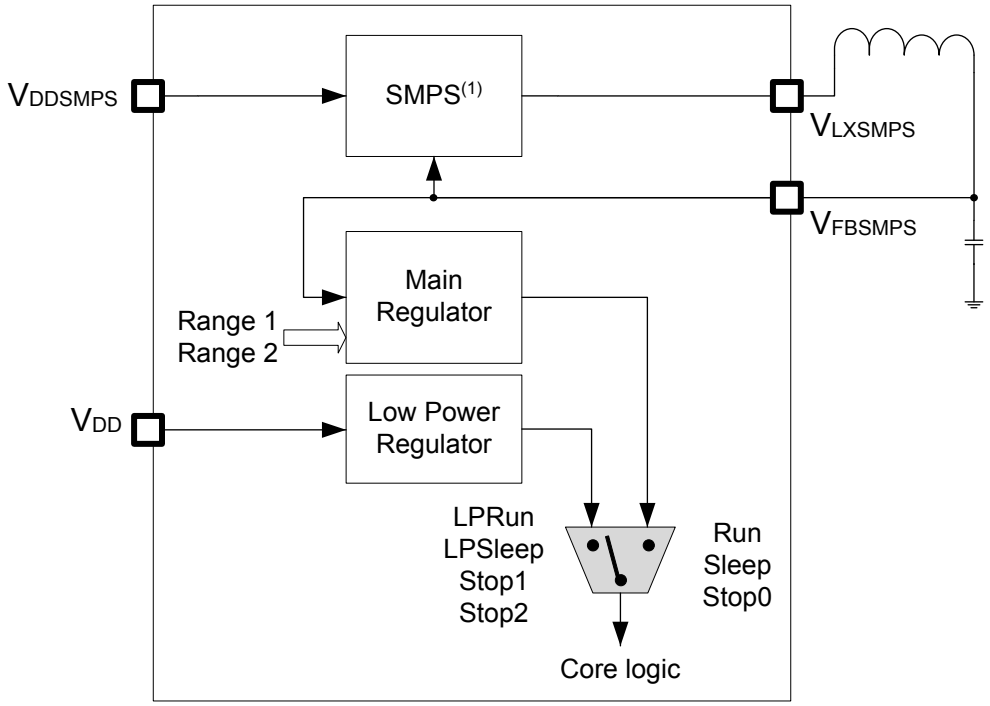


Figure 2 shows the power distribution from the internal LDO regulator in the different Run modes.

Figure 2. Power distribution architecture



Note:
(1) No SMPS on STM32WBx0

STM32WB Series microcontrollers allow the CPU1 Cortex®-M4 to execute code either from the internal Flash memory, the SRAM1 and SRAM2, or from the external Quad-SPI (only for STM32WB55 and STM32WB35).

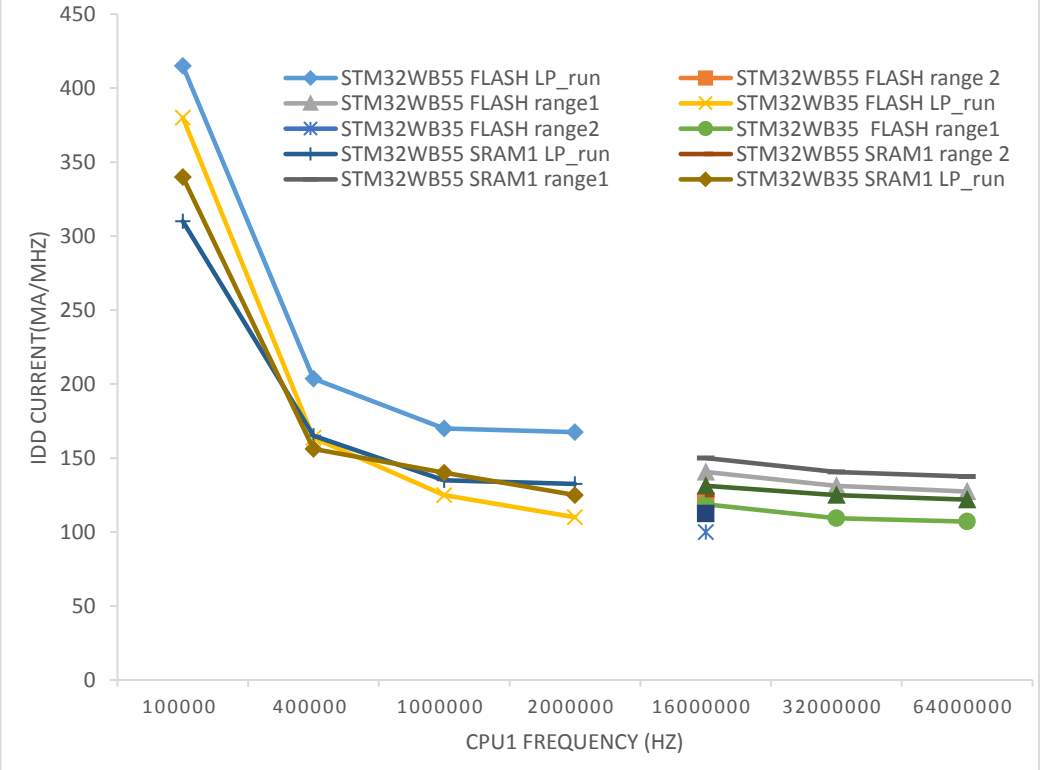
The lowest power consumption is achieved by running from internal SRAM. When running from the internal Flash memory, the ART Accelerator reduces the number of memory accesses thus reducing the overall current consumption.

Note: The ART Accelerator cannot be disabled when the RF subsystem is in use, as the Cortex®-M0+ and the Cortex®-M4 share the same Flash memory.

Figure 3 shows the consumption of the STM32WB55 for two main memory configurations:

- Execution from the internal Flash memory, ART Accelerator enabled
- Execution from the internal SRAM1, Flash memory disabled.

Figure 3. STM32WB55 - current consumption for different memory configurations



The location of the executable code and data within the memory system impacts not only the current consumption but also the overall computation performance. As an example, Table 1 details the overall performances measured on a STM32WB55 with the system clock running at 64 MHz, excuting a complex algorithm, such as CoreMark® from EEMBC® organization.

Table 1. STM32WB55 performance with system clock at 64 MHz

Configuration	mA/MHz	CoreMark® per MHz	CoreMark® per mA	Comments
FLASH ART On	0.125	3.37	27	Cache On, Prefetch buffer Off
SRAM1	0.117	2.42	20	Code and Data in SRAM1

The ART Accelerator allows the Cortex®-M4 core to run almost at the maximum efficiency as defined in the figures published by Arm®. Table 2 gives the impact of the SMPS on the same figures.

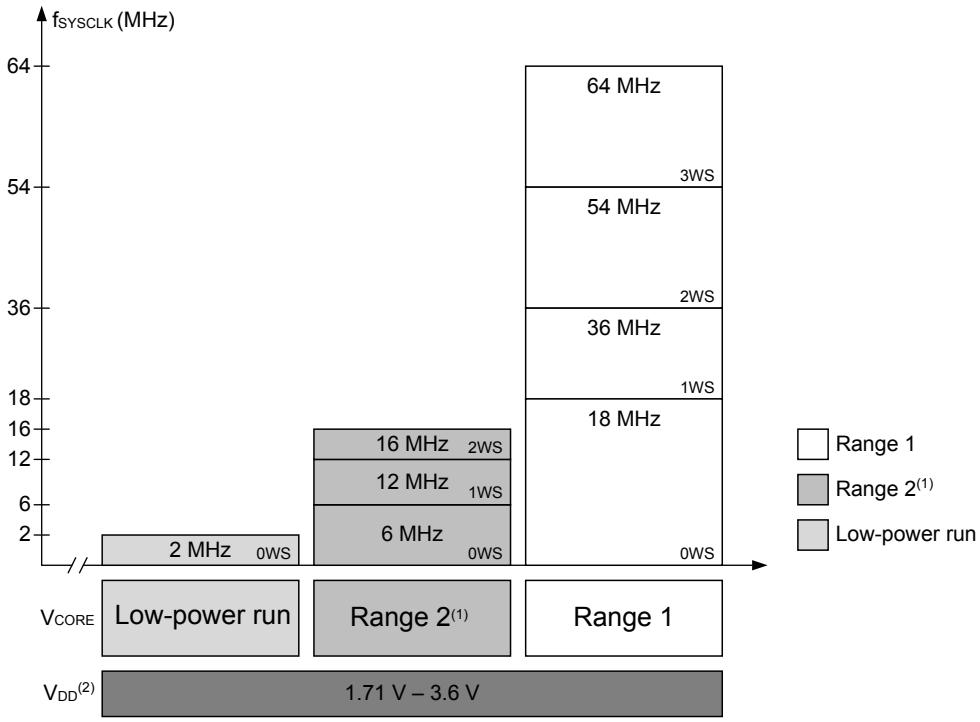
Table 2. STM32WB55 performance with SMPS

Configuration	mA/MHz	CoreMark® per MHz	CoreMark® per mA	Comments
FLASH ART On	0.077	3.37	43	-
SRAM1	0.073	2.42	33	-

The selection of the SMPS, when possible, improves the efficiency (CoreMark® per mA) by almost 40%.

Figure 4 shows the STM32WB Series microcontroller Flash memory latency (number of wait states to be programmed in the Flash memory access control register), depending on regulator voltage scaling range and system clock frequency.

Figure 4. STM32WB Series microcontrollers Flash memory latency versus V_{CORE} range



Note:
(1) Range 2 is not supported by the STM32WBx0
(2) VDD between 2 V and 3.6 V for STM32WBx0

3 FlexPowerControl description

FlexPowerControl reduces the application power consumption thanks to high flexibility in the power management, smart peripherals and architecture.

The STM32WB Series microcontrollers feature an independent power management state by the RF sub-system and the Cortex®-M4 application CPU. A dedicated hardware mechanism selects the lowest possible power consumption state.

3.1 Available low-power modes

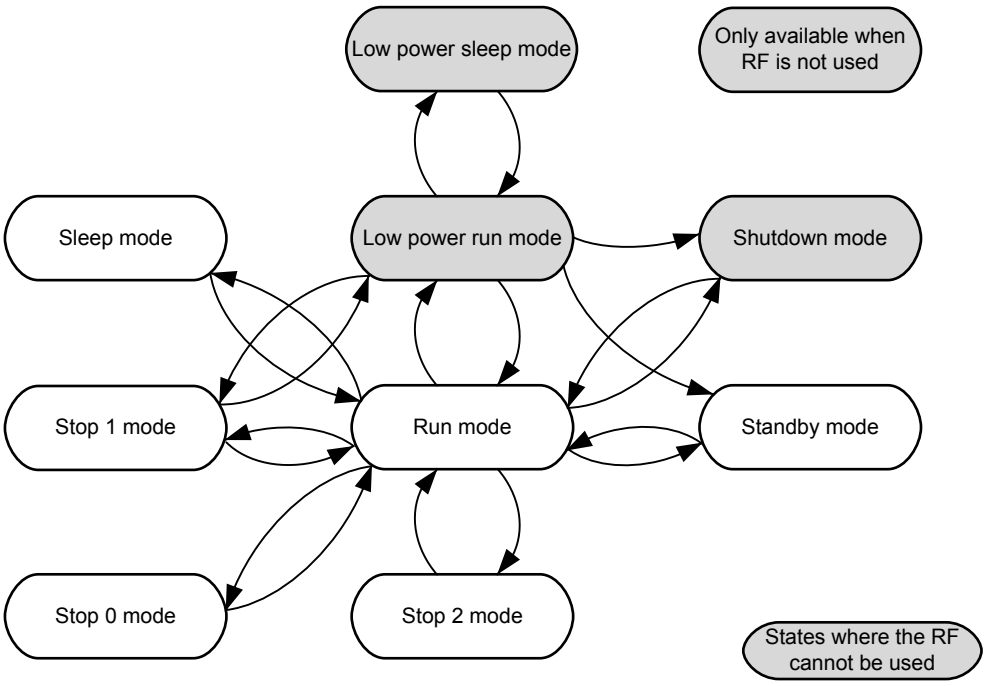
The STM32WB Series microcontrollers implement many different Power modes, of which seven of them are Low-power.

On top of these modes, the power consumption can be modulated by selecting different clock sources and frequencies, as well as clocking off unused peripherals.

In all these modes, except Shutdown, the safe power monitoring brown out reset (BOR) and the IWDG can stay active to guarantee safe execution.

The following sections outline the features available for each mode and are further described in product datasheet. Figure 5 shows the possible transitions between Low-power modes.

Figure 5. Possible Low-power modes transitions



3.1.1 Low-power run and Low-power sleep modes

When the RF sub-system is not in use and the application CPU is running below 2 MHz, the Low-power run mode and Low-power sleep mode result in the best power performance.

They offer Run and Sleep mode functionality for applications with extremely low current consumption where some peripherals cannot be switched off, or where the CPU is continuously processing at low speed to minimize current variations.

Several features are implemented to reduce the current consumption:

- The core logic is supplied by the low-power voltage regulator to reduce the quiescent current.
- The Flash memory can be switched off (Power-down mode and clock gating) in Low-power sleep mode. It can also be switched off in Low-power run mode when the application processor is executing from SRAM1.
- The system clock is limited to 2 MHz. The MSI internal RC oscillator can be selected as it supports several frequency ranges, with a small MCU total consumption as low as 48 µA in Low-power sleep Flash memory off at 100 kHz.

Batch acquisition sub-mode (BAM)

The STM32WB Series microcontrollers support the power efficient batch acquisition sub-mode (BAM), in which data is transferred using communication peripherals, while the rest of the device is in Low-power mode.

This is achieved by entering Sleep or Low-power sleep mode with this configuration:

- Only the DMA, the communication peripheral(s) and the SRAM1 or SRAM2 clocks enabled in Sleep (or Low-power sleep) mode.
- If the RF sub-system is not in use, the system clock can be limited to 2 MHz and the main regulator is switched off (to enter Low-power sleep). In this case the Flash memory can be powered off.

In Low-power sleep mode, the I2C and USART/LPUART peripherals can still be clocked with HSI at 16 MHz, making it possible to support BAM with I2C or USART at speeds up to 1 Mbps.

3.1.2 Stop mode

The STM32WB Series microcontrollers implement three Stop modes with full SRAM and peripheral retention capability and a wakeup capacity.

In these Stop modes all the high speed oscillators (HSE, MSI, HSI) are stopped, while the active low speed oscillators (LSE and / or LSI) are kept active. The peripherals are set to active using the HSI clock when needed, to wake the device up on a specific events (such as UART character reception or I^2C address recognition).

3.1.3 Standby mode

In Standby mode, the BOR is always enabled, ensuring that the devices is reset if the supply voltage drops below the selected functional threshold.

Individual pull-ups and pull-downs can be applied on each I/O during the Standby mode, preserving any external device configuration.

Wakeup from this mode is done by using one of the five wakeup pins, the reset pin or the independent watchdog. The RTC clocked by the low-speed oscillators (LSE or LSI) is also functional in this mode, with wakeup capability. Wakeup from this mode can also be performed by the Radio sub-system.

3.1.4 Shutdown mode

The Shutdown mode is implemented in the STM32WB Series microcontrollers to further lengthen the battery autonomy of battery-powered applications.

This mode provides the lowest power consumption, by switching off the internal voltage regulators and by disabling the voltage power monitoring. Wakeup from this mode is done with one of the wakeup pins or the reset pin. The RTC clocked by the low-speed external oscillator (LSE) is also functional in this mode, with wakeup capability. Wakeup from shutdown is equivalent to a POR.

Note: In this mode the RF sub-system cannot be used as all the BLE and 802.15.4 link parameters are lost.

3.2 Multi-supply and battery backup domain

The STM32WB Series microcontrollers require a V_{DD} operating voltage supply between 1.71 V (2 V for STM32WBx0) to 3.6 V. VDDSMPS, VDD USB, VDD LCD and VREF+ are not available for the STM32WBx0.

Independent supplies (V_{DDA}, V_{DDUSB}), can be provided for specific peripherals, thus removing the need to supply the whole system with high voltage when analog or USB functions are used. Supplying the MCU with low V_{DD} voltage reduces the power consumption in the low-power modes. When the peripherals supplied by the independent power supplies are not used in the application, those supplies should be connected to V_{DD}.

- V_{DD} and V_{DDSMPS} must be between 1.71 to 3.6 V (2 V to 3.6 V for the STM32WBx0).

  V_{DD} is the external power supply for the I/Os, the RF sub-system, the internal regulator and the system analog functions such as reset, power management and internal clocks. It is provided externally through VDD pins.

- V_{DDRF} must be between 1.71 to 3.6 V (2 V to 3.6 V for the STM32WBx0).

  Supplies the RF reference voltage.

- V_{DDA} minimum voltage (except STM32WBx0):
  - 1.62 V if ADC or COMPs are used;
  - 2.4 V if the built-in Reference source needs to be used for V_{REF}.
  - VDDA must be between 2 V to 3.6 V: external analog power supply for ADC (STM32WBx0).

  V_{DDA} is the external analog power supply for A/D converters and comparators.

- V_{DDUSB} must be between 3.0 to 3.6 V (if USB is used).

  V_{DDUSB} is the independent external power supply for USB transceivers.

In addition, the STM32WB Series microcontrollers support two voltage reference supplies:

- V_{LCD} must be between 2.5 to 3.6 V.

  The voltage reference for the LCD (V_{LCD}) is used to control the contrast of the glass LCD. It is provided either by an external supply voltage or by the embedded voltage step-up converter, independently of the V_{DD} voltage (up to 3.6 V if V_{DD} > 2.0 V). VLCD is multiplexed with PC3 or with PB2, which can be used as GPIO when the LCD is not used.

- V_{REF+} is the input reference voltage for the ADC.

  It is also the output of the internal reference voltage buffer when enabled. VREF+ pin, and thus internal reference voltage, is not available on all packages. When the VREF+ is double-bonded with VDDA in a package, the internal reference voltage buffer is not available and must be kept disabled (refer to datasheet for packages pinout description).

To retain both the content of the Backup registers and supply the RTC function when V_{DD} is turned off, the VBAT pin must be connected to an optional backup voltage supplied by a battery or by another source: V_{BAT} must be between 1.55 to 3.6 V

V_{BAT} is the power supply for the RTC, the external clock 32 kHz LSE oscillator and the backup registers (through power switch) when V_{DD} is not present. When V_{DD} is present these peripherals (RTC, LSE) are automatically supplied by V_{DD}, and it is then possible to charge the external battery on VBAT through an internal resistance.

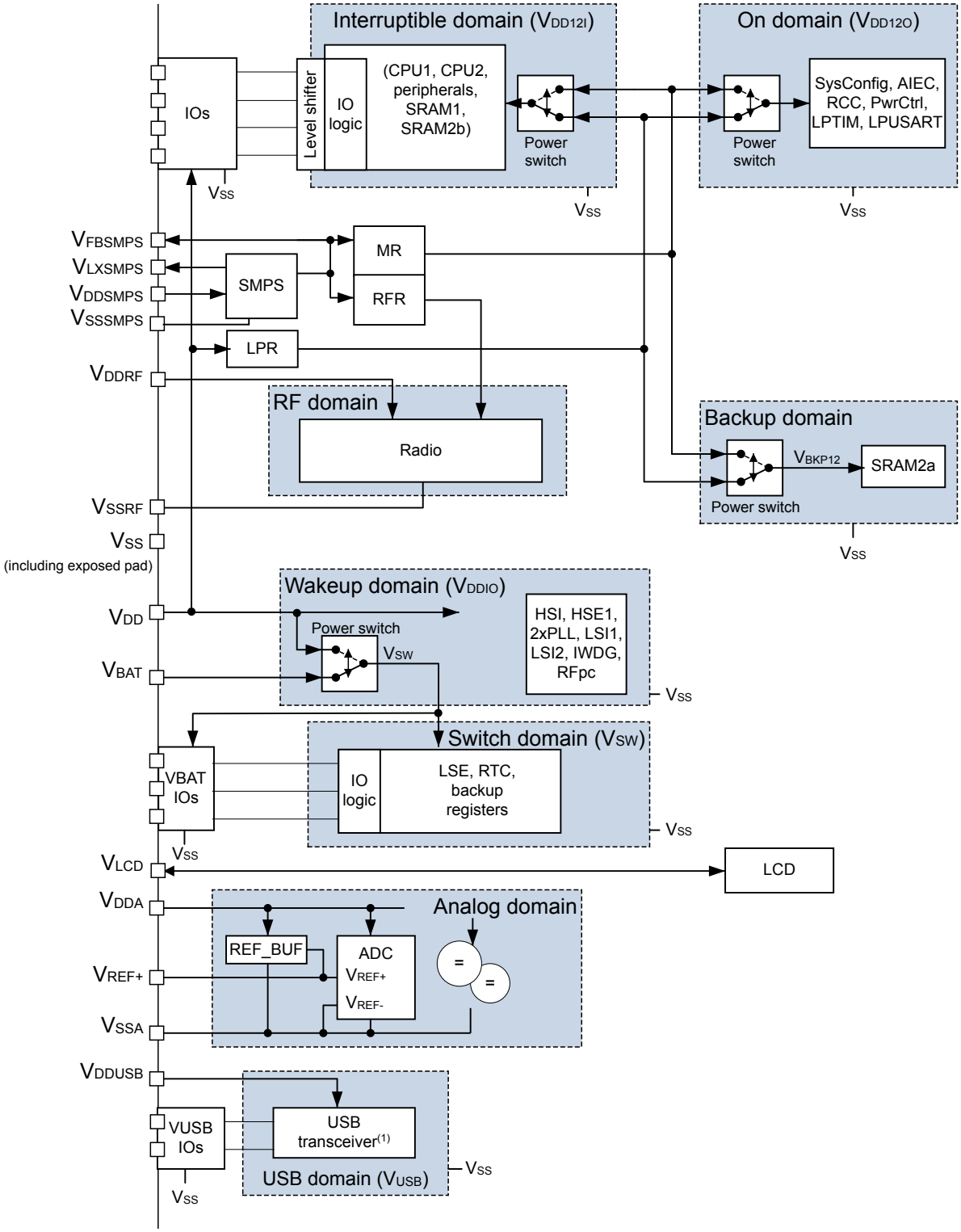
The STM32WB Series microcontrollers (except STM32WBx0) include a built-in SMPS to convert V_{DD} to the lowest voltage used by both the RF transceiver and the digital logic. This SMPS voltage (V_{FBSMPS}) is programmable, to adapt to the desired performance of both the RF Transmitter and the digital logic requirements.

An embedded linear voltage regulator is used to supply the internal digital power V_{CORE}, the power supply for digital peripherals and memories. Thanks to the internal voltage regulator and voltage scaling, the power consumption in active modes is kept at a minimum, whatever the supply voltage.

Note: Not all supply pins are present on all packages, refer to the datasheet for details.

Note: When using independent voltage sources for V_{DDA}, V_{DDUSB}, V_{DDLCD} and V_{DDRF}, the power-on and power-off supply sequence must be compliant with the constraints specified in each device datasheet.

Figure 6. STM32WB55 power supply overview



3.2.1 SMPS

The STM32WB Series microcontrollers feature a switched mode power supply (SMPS) to improve power performance at the high voltage (not included in STM32WBx0). This SMPS supplies all the logic and RF power stages. The SMPS is designed so that the RF sensitivity performance is not degraded by using the same clock as the RF.

In order not to waste energy when commuting from Run to Low-power states, the SMPS implements an Open mode that maintains the load on its output capacitance in Stop1/2 and Standby. This also results in an improved wakeup time.

The STM32WB Series microcontrollers also features an automatic mechanism to disable the SMPS if the V_{DD} voltage drops below a given level, programmable using the BORH detector. In that case, the application needs to restart the SMPS when the V_{DD} voltage increases again.

This SMPS can be switched on/off on the fly, for examples if an analog task (such as an ADC acquisition) requires a very clean and stable supply.

The SMPS output voltage V_{FBSMPS} is monitored and a reset is automatically generated if the voltage drops below a level that does not allow the digital section to operate correctly over the whole voltage and temperature range. (except in the STM32WBx0)

3.3 Ultra-safe supply monitoring

The STM32WB Series microcontrollers include a sophisticated supply supervisor module with several programmable options. This module is active during both power-on/down and

run-time phases.

The power-up is a critical phase where the various parts of the internal circuitry must be sequentially started and critical parameters (such as factory trimming values or options) are retrieved from the non-volatile memory to perform MCU initialization, even before the user reset phase. It is also during this period that V_{DD} can be impacted by glitches coming from the battery insertion or due to a weak power source.

The ultra-safe BOR circuitry guarantees that the reset is released only if the V_{DD} is above the selected threshold, whatever the slope of the V_{DD} ramp-up phase, so that the circuit is within its guaranteed operating conditions when the program execution starts. A reset is generated when V_{DD} falls below the selected threshold. Five thresholds can be selected depending on the value stored in Flash memory option byte. The BOR minimum threshold is 1.71 V, guaranteeing that the device exits reset above 1.71 V, supplying 1.8 V ± 5% to the MCU.

The BOR is enabled in all modes except Shutdown mode. In Shutdown mode, the power monitoring is disabled, as a consequence the switch to V_{BAT} domain when V_{DD} is not present (and vice-versa) is not supported.

The SMPS output voltage is monitored (except in the STM32WBx0), to guarantee that the device has a proper voltage to sustain operation. If the V_{FBSMPS} falls below 1.2 V, in operating mode (other than Shutdown, Standby and Stop2) a hardware reset is generated.

In addition, a 7-level programmable voltage detector (PVD) is available to generate an early interrupt in case of a voltage drop.

Finally, the independent power supplies (V_{DDA} and V_{DDUSB}) can be monitored by comparing them with a fixed voltage threshold. An interrupt is generated when the voltage falls below the threshold (except STM32WBx0).

The PVD and PVM can wakeup from Stop modes.

3.4 A set of peripherals tailored for low-power

Some peripherals require special attention, either because of their intrinsic high consumption, or because they are always powered up.

- The STM32WB Series microcontrollers include an RF subsystem that automatically interfaces with the Power mode selection. At predefined times, driven by the LSE low-power oscillator, the RF-sub-system wakes the device up to perform an RF link operation. Once completed it automatically goes back to the previous Low-power mode.
- The STM32WB Series microcontrollers embed a multiple 12-bit / 4.26 Msps (2.13 Msps for STM32WBx0) ADC. This very fast and accurate converter can jeopardize the battery lifetime if left powered-up. As the ADC consumption is roughly proportional to the acquisition frequency (around 200 µA / Msps), from a consumption standpoint the application can choose between two solutions, either performing the acquisition at low speed to limit maximum current, or doing it at maximum speed to switch back to Ultra-low-power mode quickly.

  When the acquisition is performed slowly, the ADC consumption itself can go down to few tens of a µA, drastically limiting the maximum current. This is be mandatory when the power source provides a limited current. The drawback, if the CPU has no other task to perform during that time, it increases the time the system spends in Run or Sleep mode (or Low-power run or Low-power sleep modes) versus the time spent in Ultra-low-power mode (Stop or Standby).

Several peripherals have been developed to operate even in Stop mode, when the system clock is stopped, with the main oscillator and memory powered down.

- A pair of ultra-low-power comparators are available (except in the STM32WBx0) to monitor analog voltages. These comparators can wake the STM32WB Series microcontrollers up as soon as the external voltage reaches the selected threshold and they can be combined together to provide a window comparator. One of these comparators has a rail-to-rail input capability and its output can be redirected to a timer for a general purpose use.
- An RTC peripheral provides a clock / calendar with two alarms, includes a periodic wake-up unit and several application specific functions (such as time-stamp and tamper detection). It can remain enabled in the lowest power mode (shutdown), when most of the chip is powered down, and wake up the full MCU circuitry in case of an event such as an alarm or tamper detection, for instance. It also contains up to 80 bytes of register backup to store contextual information when exiting from Standby mode, or to store sensitive information as they are protected by tamper detection mechanism, and readout memory protection. This peripheral has been designed using asynchronous design techniques to minimize its consumption.

  The RTC can be clocked by two low-power low-speed clocks:

  – LSE: the external 32.768 kHz quartz oscillator supports four power consumption modes, combined with drive capability;

  – LSI1: when high accuracy is not required, the RTC can be clocked by an internal 32 kHz oscillator, with extremely low consumption.
- The glass LCD is one of the most common displays in low-power applications, because of its inherently low current consumption, low price and simple customization. The STM32WB Series microcontrollers (except for the STM32WBx0 and the STM32WB35) include a versatile LCD controller, which can drive displays with up to 8 common lines and 40 segments (or 4 lines, 44 segments), with the capability of individually selecting the I/O ports assigned to the LCD for an optimal use of the chip alternate functions. It also controls an optional internal step-up converter to maintain the LCD contrast on a wide range of V_{DD} values with a current as low as 5 µA (LCD consumption not included).
- The low-power timer (LPTIM) is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. With its clock source diversity, the LPTIM is able to keep running whatever the selected power mode. Given its capability to run even with no internal clock source, the LPTIM can be used as “pulse counter” which can be useful in some applications. Also, the LPTIM capability to wake up the system from Low-power modes, makes it suitable with extremely low-power consumption “time-out functions”. The LPTIM introduces a flexible clock scheme that provides the required functionality and performance, while minimizing the power consumption.

- The low-power universal asynchronous receiver transmitter (LPUART) available in the STM32WB Series microcontrollers (except in the STM32WBx0) is a UART which allows bidirectional UART communications with a limited power consumption. Only 32.768 kHz LSE clock is required to allow UART communications up to 9600 bauds. Higher baud rates can be reached when the LPUART is clocked by sources other than from the LSE clock. Even when the MCU is in Stop mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption.

  Several sources of wakeup from Stop mode can be selected:

  – wakeup on address match
  – wakeup on Start bit detection
  – wakeup on received byte.
- The I^2C is able to wakeup the MCU from Stop modes (APB clock is off), when it is addressed. All addressing modes are supported. The HSI oscillator must be selected as the clock source for I2CCLK in order to allow wakeup from Stop. During Stop mode, the HSI is switched off. When a START is detected, the I^2C interface switches the HSI on, and stretches SCL low until HSI is woken up. HSI is then used for the address reception. In case of an address match, the I^2C stretches SCL low during MCU wakeup time. The stretch is released when ADDR flag is cleared by software, and the transfer goes on normally. If the address does not match, the HSI is switched off again and the MCU is not woken up.
- The USART is able to wakeup the MCU from Stop0/1 mode when USART clock is HSI or LSE. Several sources of wakeup from Stop0/1 mode can be selected:
  – wakeup on address match
  – wakeup on Start bit detection
  – wakeup on received byte.
- The USB can wakeup from Stop0/1 mode with these events (not available in the STM32WBx0):
  – resume from Suspend
  – attach detection protocol event.

All the available peripheral feature modes and wakeup capability are detailed in the product datasheet.

3.5 A versatile clock management

A reset and clock controller (RCC) peripheral manages the STM32WB Series microcontrollers seven clock sources.

Two external oscillators can be used for applications requiring high precision:

- The HSE clock (32 MHz high speed external clock), mandatory for RF operation, typically used to feed the PLL and to generate a CPU clock frequency of up to 64 MHz, and independent frequencies required for the USB controller and the audio clocks.
- The LSE (typically 32.768 kHz low speed external clock) normally used to provide a low-power clock source to the real time clock (RTC) and the RF sub-system, can also be used as LCD clock.

Five internal oscillators can be selected for various tasks:

- The LSI1 clock (32 kHz low speed internal clock) is a ultra-low-power source that can feed the real time clock (with a limited accuracy), the LCD controller and the independent watchdog
- The LSI2 in low constraint applications
- The HSI clock (16 MHz high speed internal clock) is a high speed voltage-compensated oscillator.
- The MSI clock (100 kHz to 48 MHz multi speed internal clock) is an oscillator with an adjustable frequency and low current consumption. It is designed to operate with a current proportional to the frequency, so as to minimize the internal oscillator consumption overhead for the low CPU frequencies. This oscillator can provide a high-accuracy signal when configured in PLL-mode, where it is auto-calibrated using the LSE.
- The RC48, when available, with clock recovery system (HSI48) is the internal 48 MHz clock source can be used to drive the USB (except for the STM32WBx0) or the True RNG peripheral. This clock can be output on the MCO.

Table 3 summarizes the characteristics and uses of the various oscillators.

Table 3. STM32WB Series microcontrollers clock source characteristics

Clock source	Use	Frequency	Consumption (typical)	Accuracy	Trimming	
					Factory	User
HSE	Master clock for RF, CPUs, LCD and RTC	32.000 MHz	260 µA	Crystal dependent, down to few ppm	NA	Yes (option)
LSE	RTC and LCD USART, LPUART, LPTIM independent clock	32.768 kHz(typical)	250 nA	Crystal dependent, down to a few ppm	Not applicable	
HSI	Master clock Peripheral independent clock	16 MHz	150 µA	± 0.8 % typical over -10 to +85 °C +0.1 / -0.2 % typical over 1.62 to 3.6 V	Yes	Yes
MSI	Master clock	100 kHz 200 kHz 400 kHz 800 kHz 1 MHz 2 MHz 4 MHz 8 MHz 16 MHz 24 MHz 32 MHz(1) 48 MHz	0.6 µA 0.8 µA 1.2 µA 1.9 µA 4.7 µA 6.5 µA 11 µA 18.5 µA 62 µA 85 µA 110 µA 155 µA	Default mode: +1.5/-1 % typical over -10 to +85 °C +1.5/-5.5 % typical for 16 to 48 MHz over 1.62 to 3.6 V PLL-mode: less than 0.25 %	Yes	Yes
LSI1	RTC, LCD and IWDG	32 kHz	110 nA	±1.5 % typical over -40 to +125 °C +0.5/-1.5 % typical over 1.62 to 3.6 V	Yes	No
LSI2	RF	~32 kHz	200 nA	Low jitter	Yes	No
HSI48	USB, RNG	48 MHz	380 nA	±3 % max over 15 to 85 °C V_{dd} 3.0 to 3.6 V ±4.5 % max over -40 to +125 °C V_{dd} 1.65 to 3.6 V	Yes	USB PLL

1. *Only possible in Range 1.*

In addition, the STM32WB Series microcontrollers embed two PLLs (one PLL is available for the STM32WBx0), each of them provides up to three independent outputs and can be fed by the HSI, the HSE or the MSI. The six outputs can be configured independently for:

- The system clock
- The ADC interface clock
- The USB, true RNG clock
- The serial audio interface SAI1 clock (not available in STM32WB35)

This removes the peripheral constraints on the system clock. Many other peripherals can be clocked independently from the system clock: USART, LPUART, I2Cx (x=1, 3) and LPTIMx (x=1, 2) receive an independent clock. This makes it possible, for instance, to reduce the system and APB bus frequencies and keep the communication peripheral baud rate constant, independently of the system clock frequency.

All peripheral clocks can be individually enabled or disabled in Run and Low-power run modes.

The peripheral clocks can also be individually enabled or disabled in Sleep and Low-power sleep modes.

Although the HSI and the MSI are factory trimmed, they can be further trimmed in 0.5% steps during run time to compensate for frequency deviations due to temperature and voltage changes.

When LSE is present in the application, the MSI can be automatically calibrated using the LSE (PLL-mode configuration), making it possible to reach long-term LSE accuracy. This mode can provide the USB clock with the accuracy required to operate in device mode.

Moreover when the MCU exits from Stop modes, the system clock can be configured to be either HSI or MSI at any frequency range. This enables the exit from Stop mode directly at 48 MHz, without waiting for a PLL starting time.

4 Conclusion

The main features of the STM32WB Series microcontrollers presented in this application note demonstrate the benefits offered by this microcontroller family in reducing the current consumption in embedded communication systems.

Besides having the same characteristics of the STM32L4 ultra-low-power Series, the STM32WB Series microcontrollers offer high processing performance without compromising the power consumption. They complement the STM32 portfolio, maintaining compatibility with other STM32 devices.

The STM32WB Series microcontrollers rich set of peripherals, associated with the proprietary low-power RF subsystem enable the user to cover a wide range of applications, while the available low-power modes give full flexibility to adjust the consumption for any task on-the-fly.

This results in an extended operating lifetime for today and tomorrow’s constantly greener applications.

Revision history

Table 4. Document revision history

Date	Revision	Changes
14-Sep-2018	1	Initial release.
21-Feb-2019	2	Changed document classification, from ST restricted to Public.
17-Oct-2019	3	Added: Throughout the document: the exception for the STM32WBx0 in: • Section Introduction: include the 2V support on STM32WBx0. • Section 2 Energy-efficient processing: the STM32WBx0 support exclusion. • Section 3.2 Multi-supply and battery backup domain: the supported voltages and exceptions for the STM32WBx0. • Section 3.2.1 SMPS: the exception for the STM32WBx0. • Section 3.4 A set of peripherals tailored for low-power: 2.13Msps support for the STM32WBx0, added the support restriction for the LCD display USB wake up. • Section 3.5 A versatile clock management: USB support restriction and the available PLLs for the STM32WBx0. Updated: • Section 3.1.4 : corrected consumption and wakeup time figures. • Figure 6. STM32WB55 power supply overview: Specified the illustrated device reference. • Section 3.4 : Specified the device reference.
22-Jan-2020	4	Updated: • Section 2 Energy-efficient processing – Figure 1. Current consumption versus Cortex®-M4 system frequency (25 °C) – Figure 2. Power distribution architecture – Figure 3. STM32WB55 - current consumption for different memory configurations – Table 1. STM32WB55 performance with system clock at 64 MHz – Table 2. STM32WB55 performance with SMPS • Section 3.1 Available low-power modes • Section 3.1.2 Stop mode • Section 3.1.3 Standby mode • Section 3.1.4 Shutdown mode • Move Figure 5. Possible Low-power modes transitions to Section 3.1 Available low-power modes • Figure 6. STM32WB55 power supply overview • Section 3.4 A set of peripherals tailored for low-power • Section 3.5 A versatile clock management Removed: • Table: STM32WB55 modes overview • Table: STM32WB55 features over all modes

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