How to improve EMI behavior in switching applications

Introduction

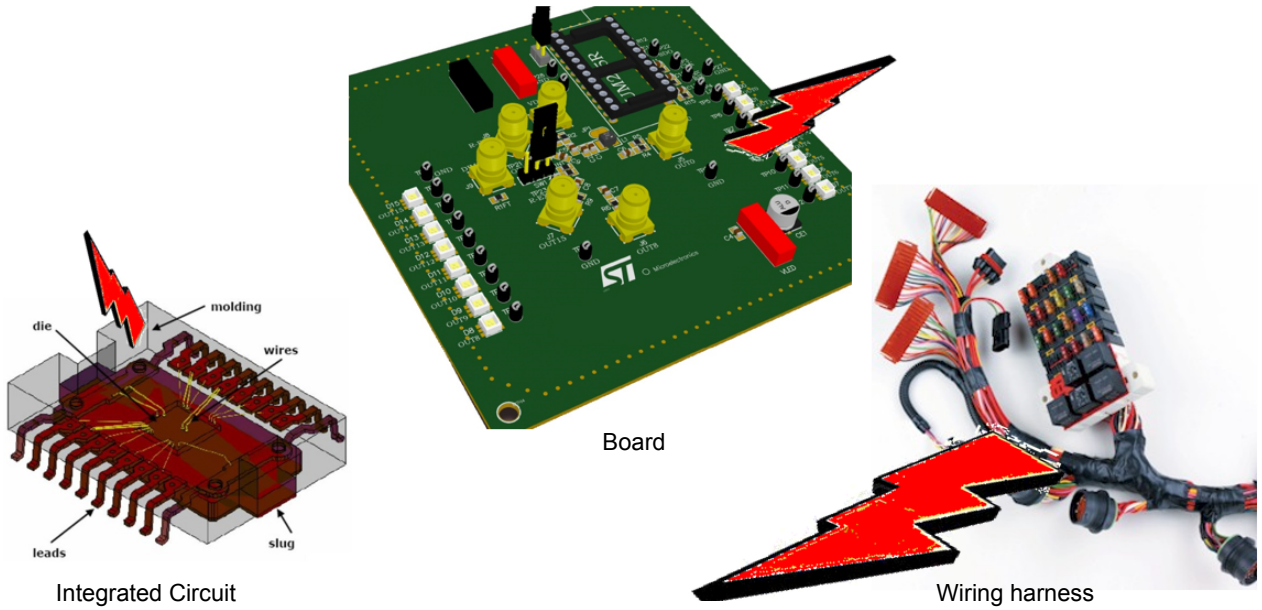
The aim of this application note is to provide the criteria to improve EMI behavior in automotive switching applications.

The present analysis helps understanding why EMI is critical in switching applications and how to reduce it in a practical example. The analysis is mainly focused on board design and load driving strategies, rather than IC design and wiring harness.

Peak & Hold injection, electro-valve control and H-Bridge driving can be listed among the most stressing applications in terms of timings and switching frequency.

Independently on the application, this document aims at providing a set of information, equations and criteria useful to choose the correct external transistors and components, along with the switching frequency. The analysis is focused on the charging and discharging of a transistor gate, and on the impact that such operation has on EMI. The ST L9945, an 8-channel configurable HS/LS pre-driver, is considered as the reference device to be used in several applications (P&H, H-Bridge, HS/LS). The ST STD105N10F7AG NMOS transistor is taken as an example of driver used in power applications.

Figure 1. Source of EMI in an automotive system



1 EMI contributions

In order to understand why a circuit generates electromagnetic disturbance, three main phenomena must be analysed:

- Heat dispersion
- Electric field generation
- Magnetic field generation

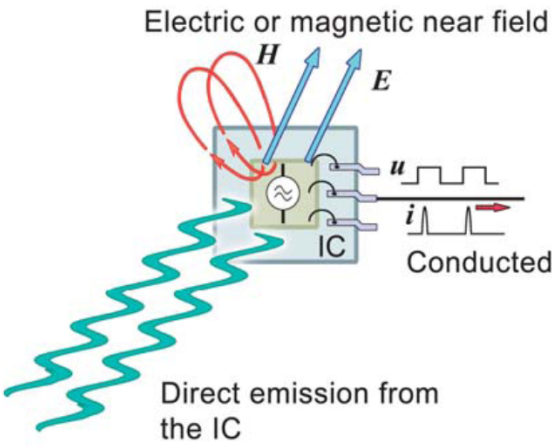
All these contributions depend on many factors, such as:

- Amount of current switched into loads
- Control signal switching frequency
- Clock tree distribution
- IC design (internal charge pump, big digital blocks, etc.)
- …many others

All these aspects can be considered as sources of electromagnetic disturbance, resulting in system generating both static and dynamic fields. The main issues to be faced when designing a complex system are:

- **Near fields:** quasi-static fields, mainly associated to the storage of electromagnetic energy in electronic components (e.g. capacitors and inductors). These fields don't propagate but can generate unwanted coupling between adjacent components
- **Conducted emissions:** disturbances associated to the switching of a huge amount of power into loads. This often results in spikes on the related power lines that may couple with adjacent wires
- **Radiated emissions:** disturbances associated to both power and signal switching. These fields propagate into free space and may be "captured" by other electronic components acting as good antennas for the whole emitted spectrum or a part of it

Figure 2. Electromagnetic disturbances



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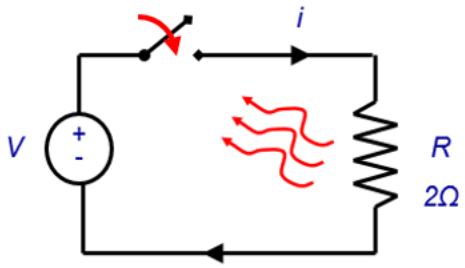
1.1 Heat dispersion

Every electronic component gets warmer when operating. From an electrical point of view, this is the effect of the current flowing through its resistance (nominal or parasitic).

Figure 3. Resistor radiating heat when current flows through it



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The amount of power dissipated as heat can be evaluated according to the well-known Joule law:

Eq: Joule law

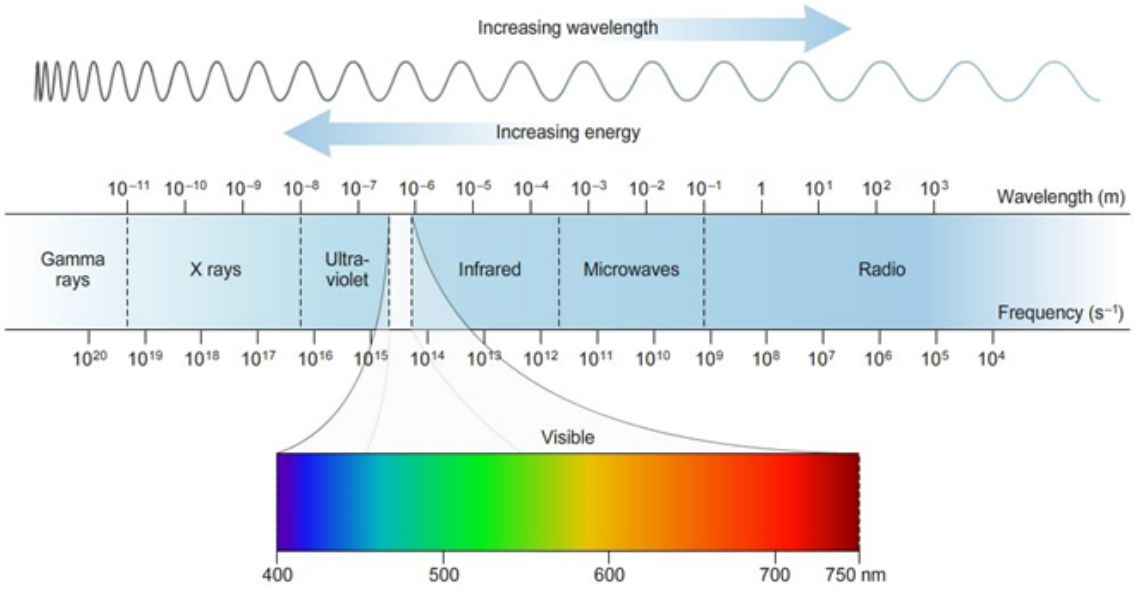
$$P_Q = R^* I^2 = \frac{V^2}{R} \quad (1)$$

The heat can be transferred in three ways:

- **Conduction:** heat transferred by means of energized electrons that start moving inside solid matter
  - The amount of heat transferred by conduction depends on the component package and the board thermal resistance. Power components have exposed pads to improve thermal resistance, lowering it, thus facilitating conduction.
- **Convection:** heat transferred to a fluid or a gas
  - The amount of heat transferred by convection depends on the presence of passive/active heatsink. A fan is rarely used in automotive systems because of cost and reliability issues. Therefore, unlike microprocessors boards, convection isn't the main source of dissipation.
- **Radiation:** energy transferred as electromagnetic waves
  - Because convection doesn't play a dominating role, a non-negligible amount of heat power is transferred via electromagnetic waves

Since this paper is mainly focused on EMI behavior, the radiated aliquot of the total heat represents our main interest. As known, heat is radiated with infrared waves, whose frequency lies in the THz range (from 10^{12} to 10^{14} Hz, as shown in the figure below). Since these frequencies are very high in respect to the signals used in automotive applications, they're not considered as a real issue for electromagnetic compatibility of these kind of circuits. The heat dispersion represents a problem in terms of thermal resistance and product reliability, rather than an EMI related matter.

Figure 4. **EM spectrum**



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1.2 Electric field generation

Both static and dynamic electric fields are present in an electronic circuit.

1.2.1 Electrostatic field

The electrostatic field is associated to the storage of electrical energy. In a circuit, components like capacitors are used to store such form of energy. A charged capacitor has an internal electrical field, whose intensity is related to the voltage applied by the following relations (calculated for a parallel plate capacitor):

Eq: Relation between electric energy stored into a capacitor and electrical field intensity

$$\begin{cases} U_E = \frac{1}{2}CV^2 \\ \vec{E} = -\nabla V \\ C = C''A \end{cases} ==> \begin{cases} U_E = \frac{1}{2}C''AV^2 \\ \left|\vec{E}\right| = \frac{dV}{dx} \\ C = \frac{\varepsilon}{d}*A \end{cases} ==> \begin{cases} \boldsymbol{U_E} = \frac{1}{2}C\boldsymbol{V}^2 = \frac{1}{2}\varepsilon A\left|\vec{\boldsymbol{E}}\right|^2 d \\ V = \left|\vec{E}\right| d \\ C = \frac{\varepsilon}{d}*A \end{cases} \quad (2)$$

Where:

- *C″* is the capacitance per area unit
- *ε* is the permittivity of the dielectric material between the plates
- *d* is the distance between the plates

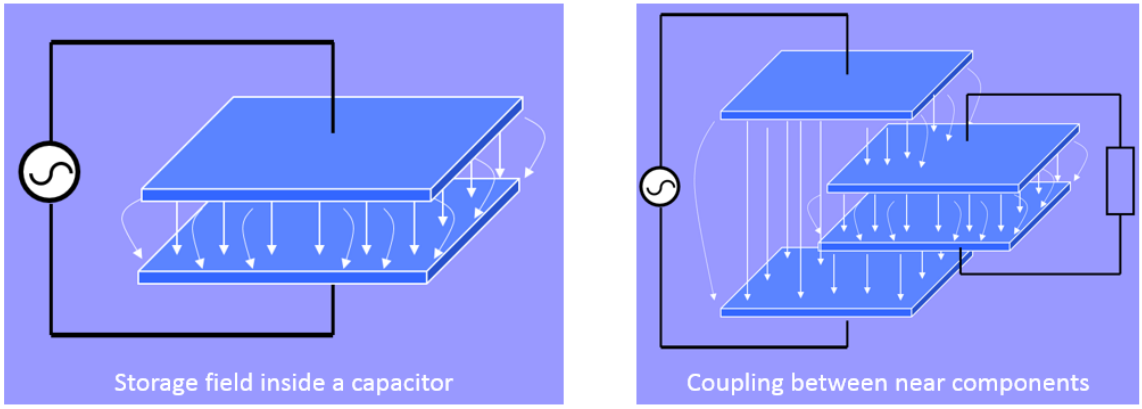
To give an example, a tank capacitor for a charge pump with the following characteristics:

- C = 470 nF
- V = 12 V
- ε = 2.66 * 10^{-10} F/m
- A = 1.28 * 10^{-6} m^2
- d = 3.2 mm

Has an internal constant electrical field with an amplitude of E = 7.88 MV/m.

Ideally, the intensity of the electrical field outside the plates area should be zero, thus allowing to place capacitors real close one to another, without having undesired coupling.

Figure 5. Electric field inside a capacitor and coupling between near components



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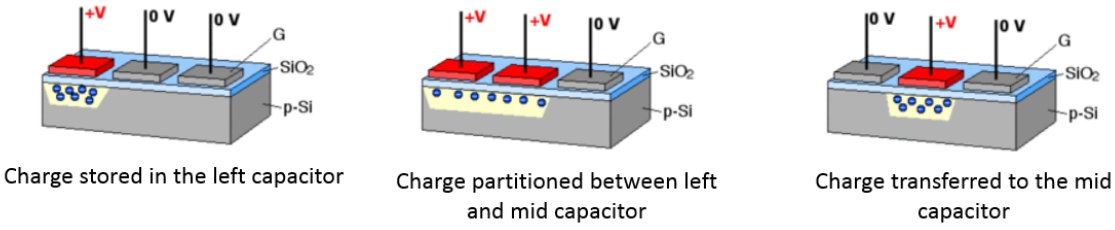
In a real capacitor, the electrical field shows some border effects. This doesn't represent an issue, unless different components are placed too close on the board, causing unwanted coupling effect, as shown in the Figure 5. Every PCB design tool has a set of rules (DRC/DFM) meant to avoid these issues, also known as **near field** effects. Modern SMD devices are realized with packages that drastically reduce proximity effects, thus allowing to use small spacing between components on a PCB layer.

In some other applications, like CCD sensors for imaging purposes, the coupling between adjacent capacitors is exploited to transfer charge between them, as shown in the following picture

Figure 6. Transfer of charge between adjacent capacitors in CCD sensors



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However, as discussed, this is an undesired effect for the majority of automotive applications. Hence, it must be avoided through both robust board design and proper switching control, as discussed in Section 3 Key for a robust configuration.

1.2.2 Radiated Electric field

In switching circuits, charges are continuously redistributed among various nodes, thus travelling from a point to another. Figure 7 and Figure 8 describe what happens to them during a switching cycle:

- When the circuit is in **idle** state, charges are still and they're stored in the different nodes of the circuit, thus generating an Electrostatic field
- During the **positive phase** of the switching control signal, charges are accelerated in a given direction. The acceleration has its peak at the beginning of the transient. The electrical field is travelling along with the charge, but with a small delay due to the time needed for the polarization of the surrounding matter
- During the **negative phase** of the switching control signal, charges are accelerated in the opposite direction. Once again, the acceleration has its peak at the beginning of the transient and the electrical field is travelling along with the charge, but with a small delay due to the time needed for the polarization of the surrounding matter
- If the switching frequency is much higher than the system response time, the effects of the positive and negative phase are combined, generating a disturbed electrical field which propagates from the source. This happens because control signal switches far before transients are over. Actually, in many applications where

currents in the loads must be controlled with a high precision, the control signal is switched at the very beginning of the transient, making the scenario depicted in Figure 8 even truer.

The Figure 8 is an example of switching application where the gate node is a source of electric field emissions.

Figure 7. How the radiated electric field is generated in a switching circuit

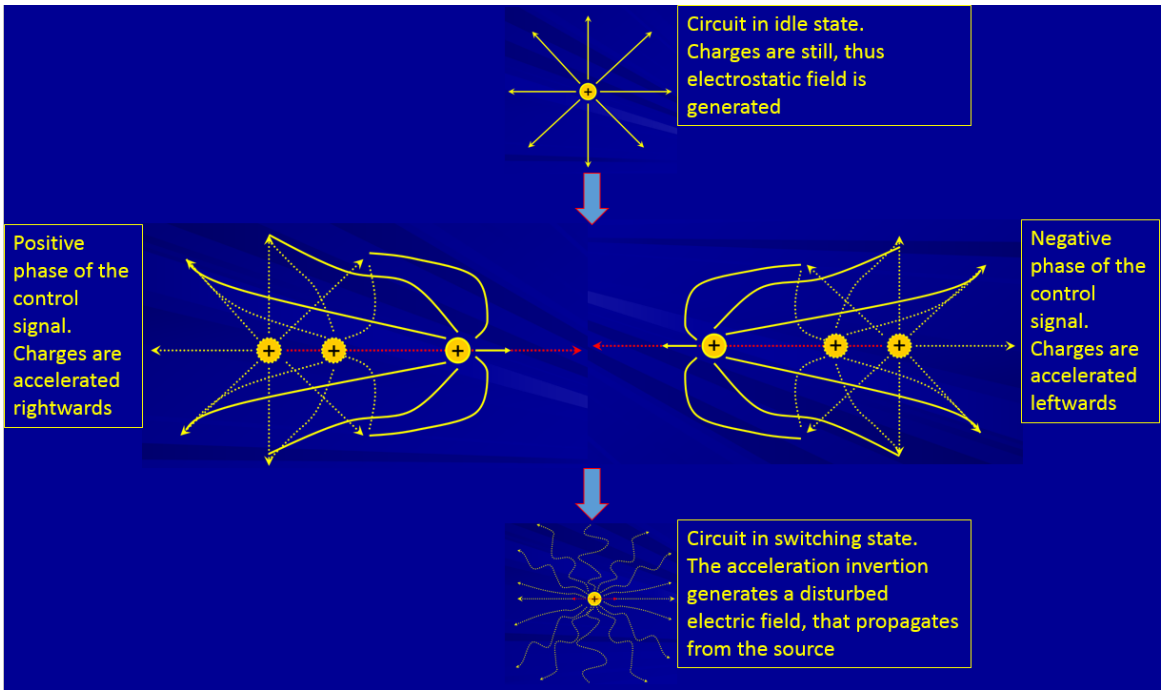

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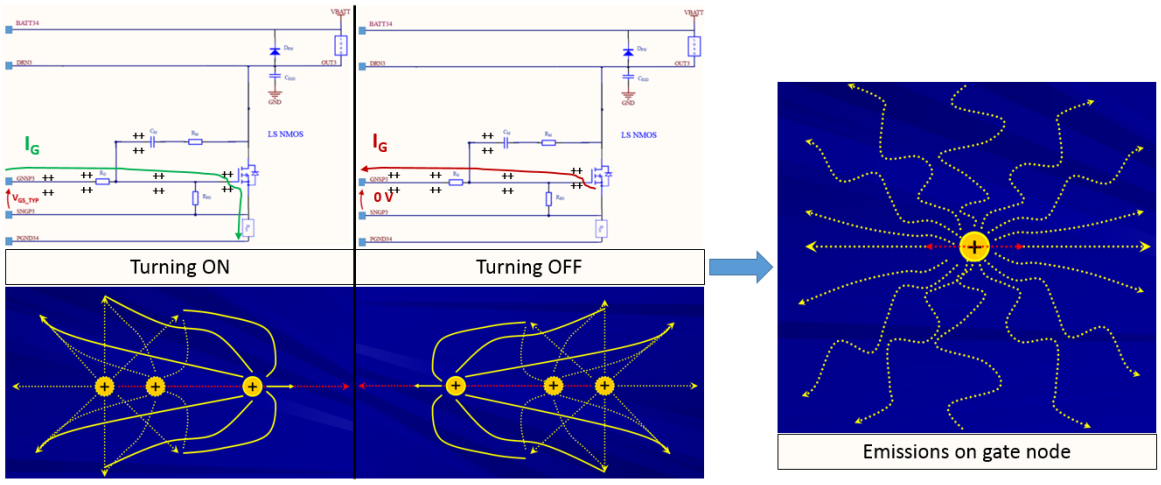
Figure 8. Focus on electric field emissions in a switching application



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1.3 Magnetic field generation

Both static and dynamic magnetic fields are present in an electronic circuit.

1.3.1 Magnetostatic field

The magnetostatic field is associated to the storage of magnetic energy. In a circuit, components like inductors are used to store such form of energy. A charged inductor has an internal magnetic field, whose intensity is related to the current applied by the following relations (calculated for a solenoid):

Eq: Relation between magnetic energy stored in a solenoid and magnetic field intensity

$$\begin{cases} U_M = \frac{1}{2}LI^2 \\ \left|\vec{B}\right| = \mu\frac{N}{l}I \\ L = L''A \end{cases} = = > \begin{cases} U_M = \frac{1}{2}L''A\frac{l^2\left|\vec{B}\right|^2}{\mu^2N^2} \\ I = \frac{l\left|\vec{B}\right|}{\mu N} \\ L = \frac{\mu N^2}{l}*A \end{cases} = = > \begin{cases} \boldsymbol{U_M = \frac{1}{2}LI^2 = \frac{1}{2}\frac{A\left|\vec{B}\right|^2 l}{\mu}} \\ I = \frac{l\left|\vec{B}\right|}{\mu N} \\ L = \frac{\mu N^2}{l}*A \end{cases} \quad (3)$$

Where:

- L'' is the inductance per area unit
- μ is the permeability of the ferromagnetic material in the solenoid core
- l is is the solenoid length

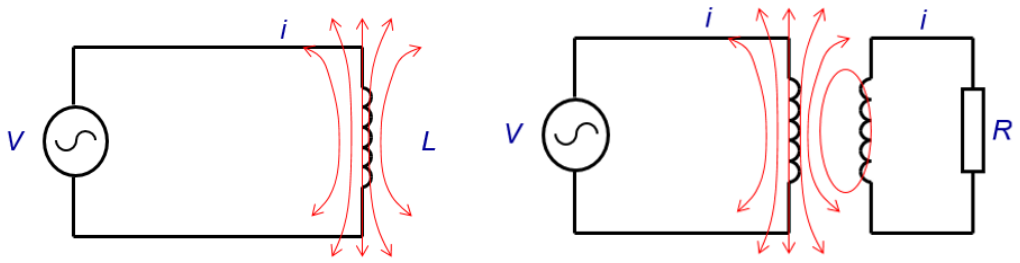
To give an example, a PFI injector with the following characteristics:

- L = 2 mH
- I = 6 A
- μ = 2.5 * 10^{-1} H/m
- A = 1 * 10^{-4} m^2
- l = 3 cm

Has an internal magnetic field with an amplitude of B = 78.2 T.

Ideally, the intensity of the magnetic field outside the core area should be zero, thus allowing to place inductors real close one to another, without having undesired coupling.

Figure 9. Storage field inside an inductor and coupling between near components



In a real inductor, the magnetic field shows some border effects. This doesn't represent an issue, unless different components are placed too close on the board, causing unwanted coupling effect, as shown in Figure 5. Every board design tool has a set of rules (DRC/DFM) meant to avoid these issues, also known as **near field** effects.

In some other applications, like transformers, the coupling between adjacent inductors is exploited to transfer power between them with galvanic isolation.

However, as discussed, this is an undesired effect for the majority of automotive applications. Hence, it must be avoided through both robust board design and proper switching control, as discussed in Section 3 Key for a robust configuration.

Also wires carrying a constant current generate a constant magnetic field according to the **Biot-Savart** law:

Eq: Biot-Savart law

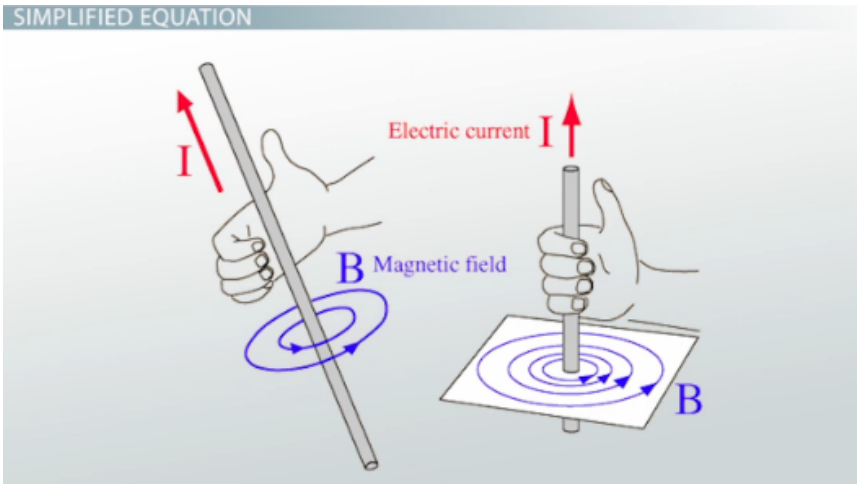
$$B = \frac{\mu_0 I}{2\pi r} \quad (4)$$

Where

- μ_0 is the vacuum permeability
- I is the constant current flowing through the wire
- r is the distance between the point under analysis and the wire axis

To give an example, a power wire carrying constant 10 A is generating a magnetic field B = 2*10-4 T at a distance of 1 cm.

Figure 10. Magnetic field generated by a wire carrying a constant current



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In switching applications, current is almost never constant and therefore this can be considered as a minor contribution to the EMI issues.

1.3.2 Radiated Magnetic field

In switching circuits, charges are continuously redistributed among various nodes, thus travelling from a point to another. Figure 11 describes what happens to them during a switching cycle. To simplify the analysis, consider the Biot-Savart law applied in a dynamic context (refer to Eq. (4)):

- When the circuit is in **idle** state, charges are still and they're stored in the different nodes of the circuit, thus generating no magnetic field
- During the **positive phase** of the switching control signal, charges are accelerated in a given direction. The acceleration has its peak at the beginning of the transient. The magnetic field is travelling along with the charge, but with a small delay due to the time needed for the polarization of the surrounding matter. Field intensity is decreasing in time because current has a typical exponential decay during a transient.
- During the **negative phase** of the switching control signal, charges are accelerated in the opposite direction. The acceleration has its peak at the beginning of the transient. The magnetic field is travelling along with the charge, but with a small delay due to the time needed for the polarization of the surrounding matter. Field intensity is decreasing in time because current has a typical exponential decay during a transient.
- If the switching frequency is much higher than the system response time, the effects of the positive and negative phase are combined, generating a disturbed magnetic field which propagates from the source. This happens because control signal switches far before transients are over. Actually, in many applications where currents in the loads must be controlled with a high precision, the control signal is switched at the very beginning of the transient, making the scenario depicted in the Figure 11 even truer.

Figure 11. **How the radiated magnetic field is generated in a switching circuit**

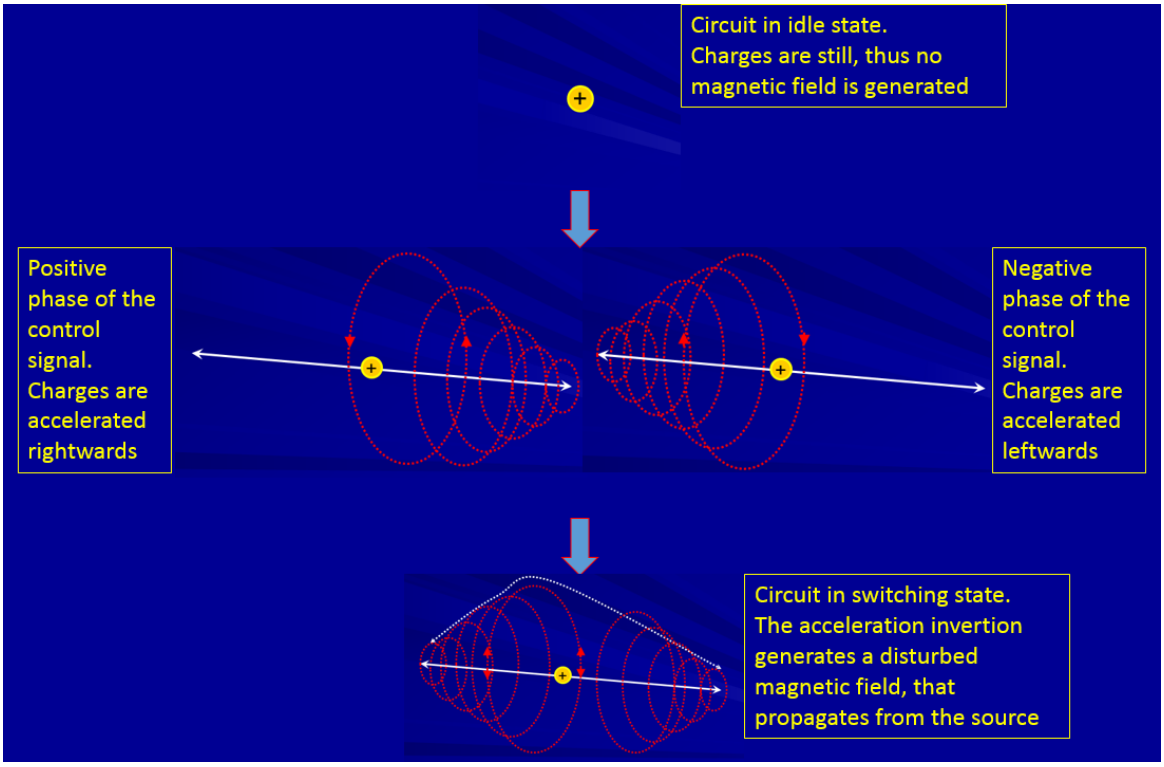

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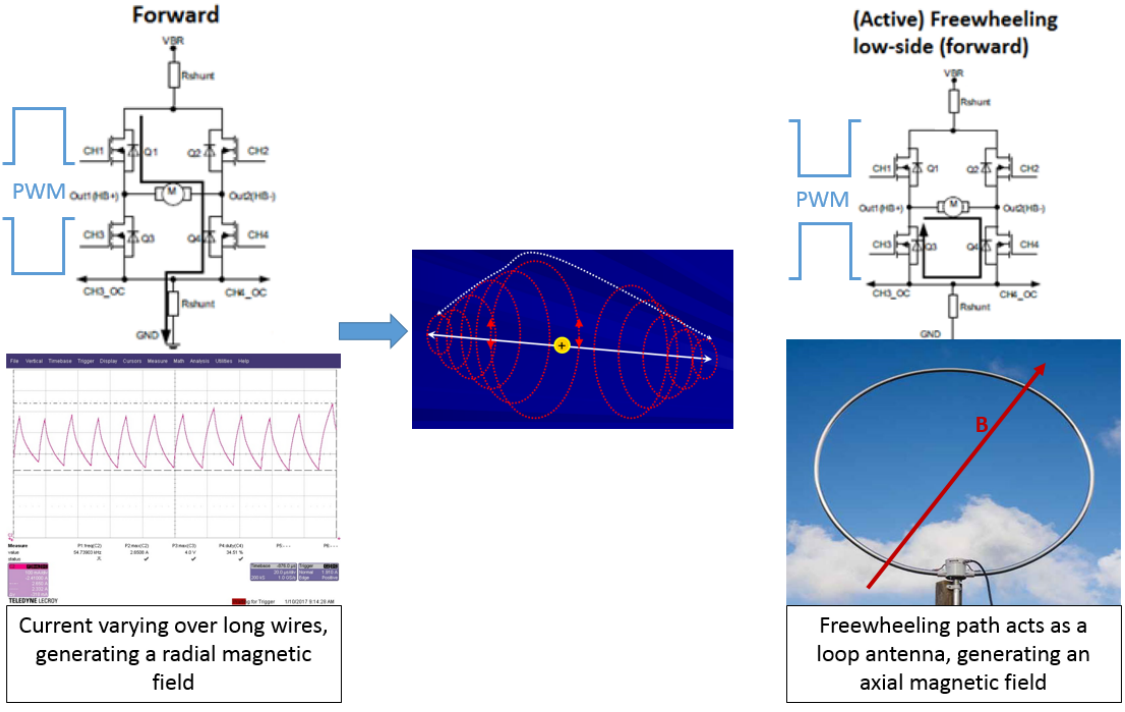
Figure 12. **Focus on magnetic field emissions in a switching application**



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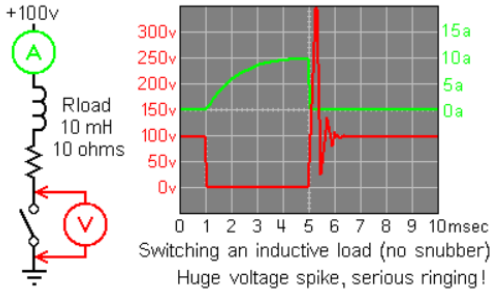
1.4 Conducted emissions

Conducted emissions are disturbances associated to the switching of a huge amount of power into loads. This often results in spikes on the related power lines that may couple with adjacent wires.

A typical example of application prone to generate conducted emissions is represented by the switching of inductive loads (pumps, injectors, motors, etc.).

The figure below shows the worst case for conducted emissions where no recirculation diode (also known as snubber) is mounted. Huge voltage spikes occur on both internal nodes and battery line. Such disturbances may also couple with other near wires, leading to bad performance and possibly also failures.

Figure 13. Worst case for conducted emissions: switching an inductive load without a snubber for recirculation



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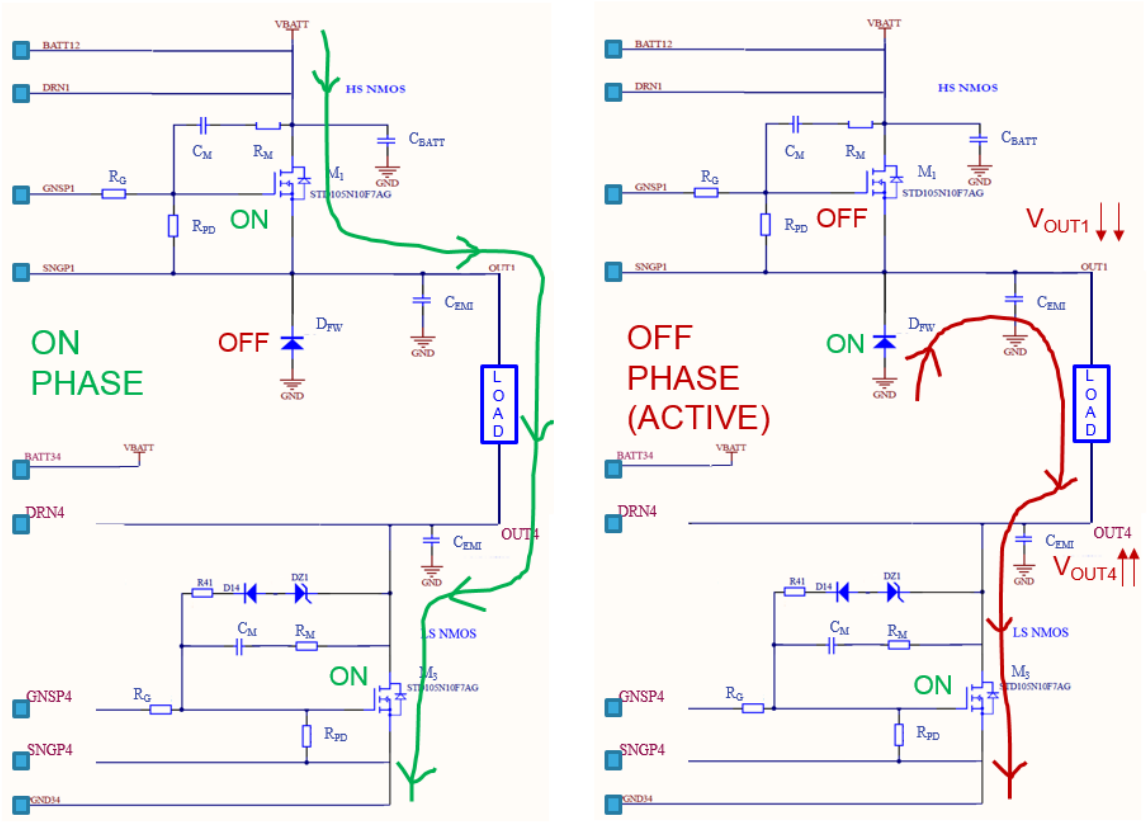
2 Example of Peak and Hold application

To give a concrete example where EMI behavior must be accounted for, in a peak & hold application, the current flowing through an electrovalve has to be controlled very precisely in order to avoid valve flickering and to determine the exact opening time.

A typical circuit used to control such current is shown in the figure below, along with the ON and recirculation phases.

Figure 14. Peak and Hold control circuit



ON phase

active recirculation phase

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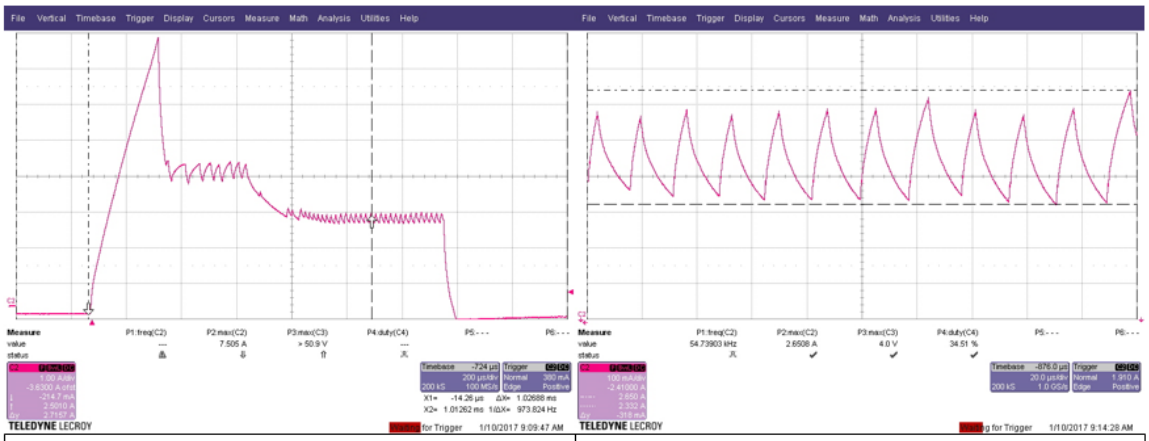
The next figure shows a typical peak and hold waveform:

Figure 15. Example of peak and hold waveform for GDI injection



The following considerations apply:

- The switching control signal applied on the gate of the transistors must have a high frequency (typically around 20 kHz) in order to allow small ripple during the hold phase. The duty-cycle varies according to the control parameters (I_{peak}, I_{hold1} and I_{hold2}). If long wires connect the external FET mounted on the PCB to the corresponding pin of the control IC, the parasitic inductance of such wires will radiate a field whose spectrum varies according to the main switching frequency (20 kHz) and the duty-cycle.

  Eq: Spectrum of a square wave with amplitude A, pulsation ω_0 and varying duty cycle

$$\begin{cases} x(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) \\ a_0 = A\frac{T_{ON}}{T} \\ a_n = 2\frac{A}{n\pi} sin\left(n\pi\frac{T_{ON}}{T}\right) \end{cases} \quad (5)$$

- Figure 15 shows how current is switched with a period much smaller than the circuit time constant. In fact, transients are almost linear since the very first path of the exponential rise/decay is covered before another switching event occurs. This will contribute to the generation of EM disturbances as described in Section 1.2.2 Radiated Electric field and Section 1.3.2 Radiated Magnetic field
- The recirculation of current through the freewheeling diode during the OFF phase can generate a conducted emission on the GND

All these phenomena must be taken into account and a robust PCB design must be ensured in order to guarantee that system won't fail EMC trials.

3 Key for a robust configuration

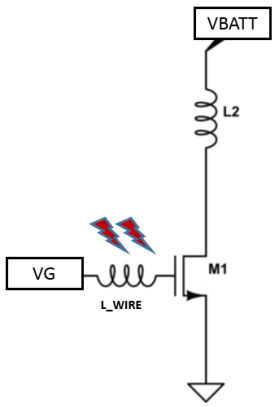
Our analysis led to formulate several criteria for building a configuration robust against EMI issues in power switching applications. These criteria are mainly focused on PCB design and IC configuration. Problems like IC design are not covered by this paper.

3.1 PCB design techniques to improve EMI robustness

3.1.1 External FET placement on PCB

Place the external FETs used as power drivers close to their gate control pin. This avoids unwanted radiations to be propagated due to the parasitic inductance of the control signal wires.

Figure 16. Parasitic inductance of gate control wire



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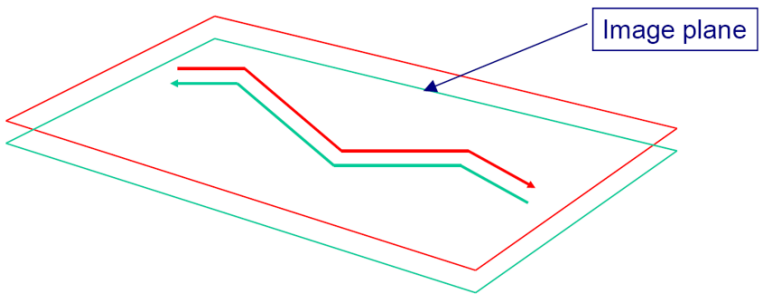
3.1.2 Image plane

An image plane is a copper layer internal to a PCB, which is physically adjacent to a signal plane. On such plane, the return path of high-frequency signals can be traced mirroring the forward path. In this way the area of the loop is minimized, and so the emissions.

Figure 17. Image plane



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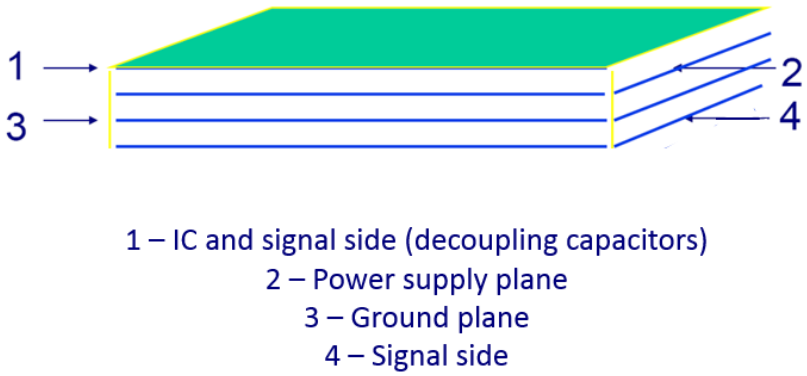
3.1.3 Supply planes and 20H rule

Power and Ground planes must be always adjacent to minimize parasitic resistance on supply lines. For instance, on a 4-layered board, the arrangement would be:

Figure 18. Planes stacking on a 4-layered board

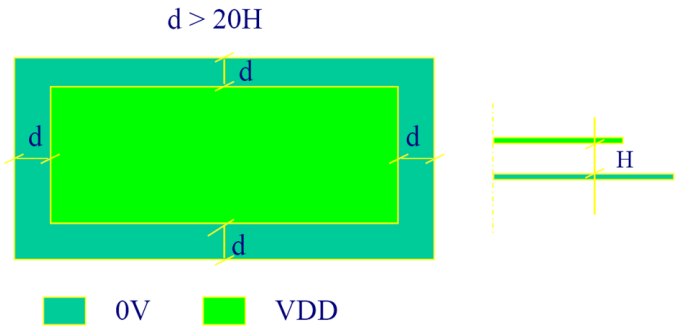


However, it is known that a two faced metal structure represents a resonant cavity. If the power supply has oscillations falling in the resonance range, energy will be trapped inside the cavity and spread all over the board, causing huge disturbances. In order to prevent such failure, the resonance frequency of the cavity must be brought far away from the operating range. Since resonance frequency is strictly dependent on the geometrical characteristics of a cavity, the issue must be solved acting on PCB layout. The **20H rule** is a PCB design empirical rule that applies to supply planes in order to avoid resonance.

As shown in the figure below, the GND and VDD planes haven't got the same area: the latter is smaller.

The enclosure "d" must be at least 20 times bigger than the vertical spacing "H" between planes.

Figure 19. 20H rule



A typical stackup of a 0.062" 4-layered PCB is shown in the below table:

Table 1. Typical stackup of a 0.062" 4-layered PCB

Layer index	Material	Function	Dielectric Constant	Thickness [um]	Copper Weight [oz]
1	Copper	Signal		35	1
	2116 and 3313	Prepreg	4.2	300	
2	Copper	Plane		17	½
	Core	Core	4.2	1000	

Layer index	Material	Function	Dielectric Constant	Thickness [um]	Copper Weight [oz]
3	Copper	Plane		17	½
	2116 and 3313	Prepreg	4.2	300	
4	Copper	Plane		35	1

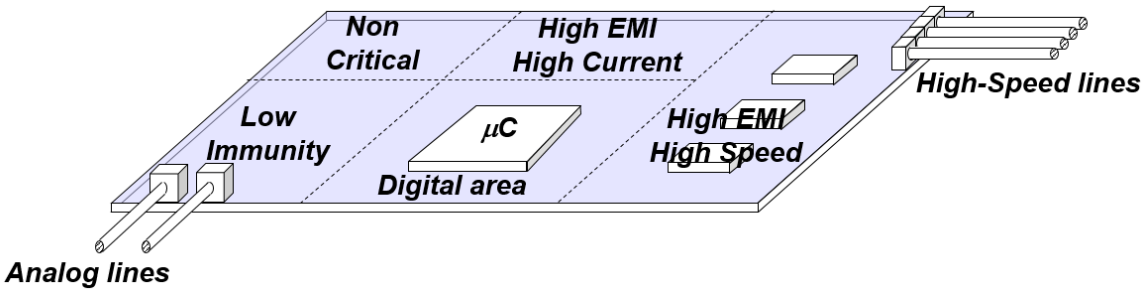
In this case, using layer 3 as ground plane, the corresponding enclosure **d** for layer 2 (power supply) should be at least 20 mm according to the 20H rule.

3.1.4 PCB partitioning

The PCB area can be partitioned according to component EMC characteristics. The following criteria can be applied:

- Divide the PCB on different areas where elements sharing the same EMC characteristics can be put together
- Trace analog and high-speed lines perpendicular to each other to minimize the interaction between parallel wires

Figure 20. PCB partitioning technique



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3.1.5 Routing techniques for crosstalk and EMI reduction

Routing wires in the correct way helps reducing parasitic elements, thus mitigating emissions and crosstalk events. Follow these criteria:

- Avoid trace loops and serpentines: they act as antennas

Figure 21. GSM antennas

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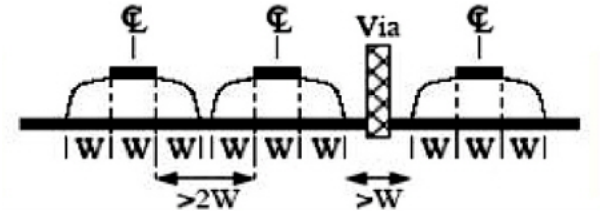
- For power traces, avoid crossings from a plane to another. Try to limit the eventual disturbances to a single plane
- The distance of separation between traces must be 3 times the width of the traces, measured center-line to center-line. This will help reducing crosstalk flux by 70%. For a 98% reduction, use a spacing equal to 10 times the width of the traces. Do not route wires too close to the plane edge. Use at least one width spacing: this will reduce border effects.

Figure 22. **Spacing between adjacent lines**



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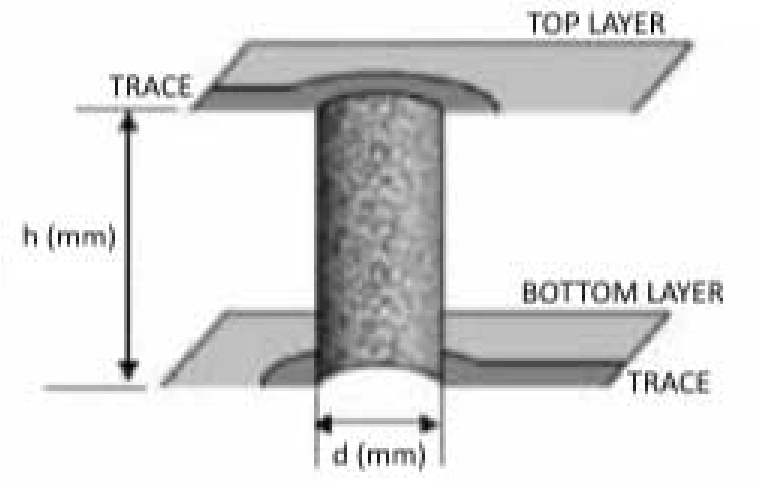
- Each via introduces about 1 pF of parasitic capacitance and a parasitic inductance that can be estimated using Eq. (6) Avoiding concentration of vias means avoiding high concentration of parasitics in a region of the PCB

Figure 23. **Geometrical characteristics of a PCB via**



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Eq: Estimation of parasitic inductance introduced by a PCB via. Measure in nH

$$L = \frac{h}{5}\left[1 + \ln\left(\frac{4h}{d}\right)\right] \quad (6)$$

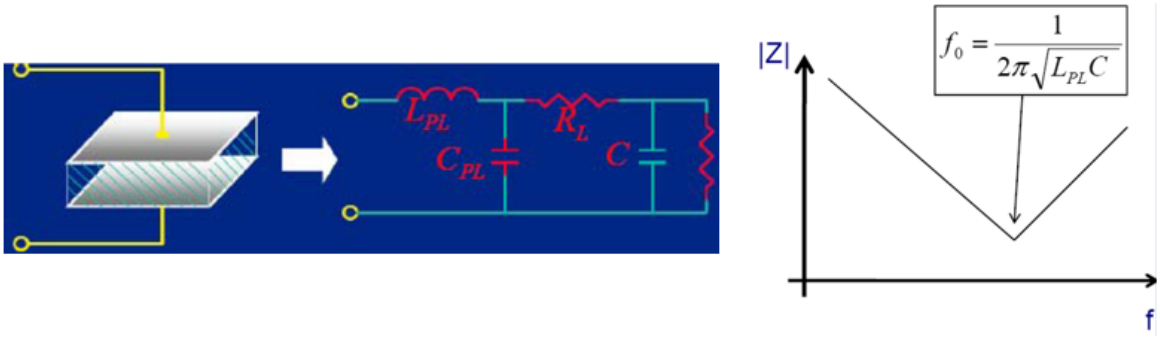
3.2 Components for reducing EMI issues

A PCB mounted in a complex system generates and receives electromagnetic emissions at the same time. In addition to the components normally mounted to grant system functionality, it is important using components for decoupling signal and supply lines. This confers robustness to the PCB against both self-generated and external disturbances.

3.2.1 Decoupling capacitors

A single decoupling capacitor is not enough to sufficiently protect a line against disturbances along the whole EM spectrum. This occurs because a real capacitor has got parasitics elements leading to a non-ideal impedance. In particular, for frequencies higher than the self-resonance $\mathbf{f_0}$ threshold, the capacitor starts behaving as an inductor, since its impedance is increasing with frequency, as shown in the figure below.

Figure 24. **Equivalent model for a capacitor and real impedance**



Therefore, capacitors can be considered as good decoupling elements for frequencies below f_0. Not all capacitors have the same f_0:

- Electrolytic and tantalum capacitors can be used for filtering signals up to 1 MHz
- Ceramic capacitors are good filters in the [1 MHz – 100 MHz] range

Hence, using different types of capacitors is mandatory to ensure full robustness against EMI disturbances.

However, the equation in Figure 24 shows that self-resonance frequency depends also on capacitance value: the higher the capacitance, the lower f_0.

Therefore, the criterion for a good decoupling is using capacitors of different types and different values:

- Bigger electrolytic capacitors with higher capacitance are used to filter disturbances at low frequency
- Smaller ceramic capacitors with lower capacitance are used to filter disturbances at high frequency

The following table lists the self-resonance value for different types of capacitors and can be used as a guideline:

Table 2. **Guideline for capacitor self-resonance frequency estimation**

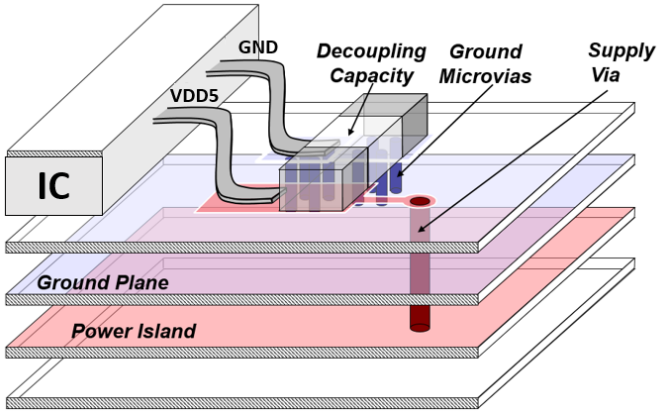
Capacitance value	f_0 of a through hole component	f_0 of an SMD component
1 µF	2.5 MHz	5 MHz
100 nF	8 MHz	16 MHz
10 nF	25 MHz	50 MHz
1 nF	80 MHz	160 MHz
100 pF	250 MHz	500 MHz
10 pF	800 MHz	1.6 GHz

In general, an SMD component has a self-resonance frequency twice the one of a leaded device.

Fixing EMC issues does not imply choosing a higher value for existing capacitors. On the contrary, it must be achieved by using smaller components with lower capacitance in parallel. In fact, such components have higher self-resonance frequency and might be capable of suppressing high frequency disturbances.

Also make sure that decoupling capacitors are distributed over the entire path of the sensitive line, in order to filter disturbances that might be injected in different points of the circuit. In particular, always put a small decoupling capacitor very close to the device pin of the sensitive line in order to act as last filtering stage, as shown in the figure below.

Figure 25. Decoupling capacitors close to device pins



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Advices on decoupling capacitors apply to all kind of power supply lines. For instance, regarding L9945, decoupling capacitors must be mounted between the following lines:

- **VPS** and **GND** (battery supply line): more than one decoupling element spanning from the PCB power connector to the VPS pin.
- **VDD5** and **GND** (5 V supply line): more than one decoupling element spanning from the PCB power connector (or the 5 V regulator output) to the VDD5 pin.
- **VPS** and **VGBHI** (tank capacitor for charge pump): very close to the IC pins, as shown in Figure 25
- **CH1** and **CH2** (flying capacitor for charge pump): very close to the IC pins, as shown in Figure 25
- **CH3** and **CH4** (flying capacitor for charge pump): very close to the IC pins, as shown in Figure 25
- **VIO** and **GND** (SDO supply line): very close to the IC pins, as shown in Figure 25
- **BATT12** and **PGND12** (sense lines for channels 1 and 2): very close to the IC pins, as shown in Figure 25
- **BATT34** and **PGND34** (sense lines for channels 3 and 4): very close to the IC pins, as shown in Figure 25
- **BATT56** and **PGND56** (sense lines for channels 5 and 6): very close to the IC pins, as shown in Figure 25
- **BATT78** and **PGND78** (sense lines for channels 7 and 8): very close to the IC pins, as shown in Figure 25

3.2.2 Miller capacitor for power drivers

In addition to supply and high-frequency lines, power lines are also a major source of EMI. In fact, these stages are where the switching of huge currents takes place, thus leading to high electromagnetic emissions as discussed in Section 1.2.2 Radiated Electric field and Section 1.3 Magnetic field generation.

In order to improve EMI performances, an external Miller capacitor C_M is usually mounted between gate and drain of the external FET, as shown in Figure 26. Note that Miller capacitance is always present as a parasitic element: the internal capacitance between transistor gate and drain is usually reported in the transistor datasheet as "C_{rss}" or "Reverse Transfer Capacitance" (see Figure 27). However, C_{rss} is usually small: consider 30-40 pF as a typical value. When interested in improving EMI performances by slowing down the drain transitions, an external C_M with a higher value (hundreds of pF) must be mounted in parallel to C_{rss}.

Figure 26. Example of HS and LS NMOS power switches

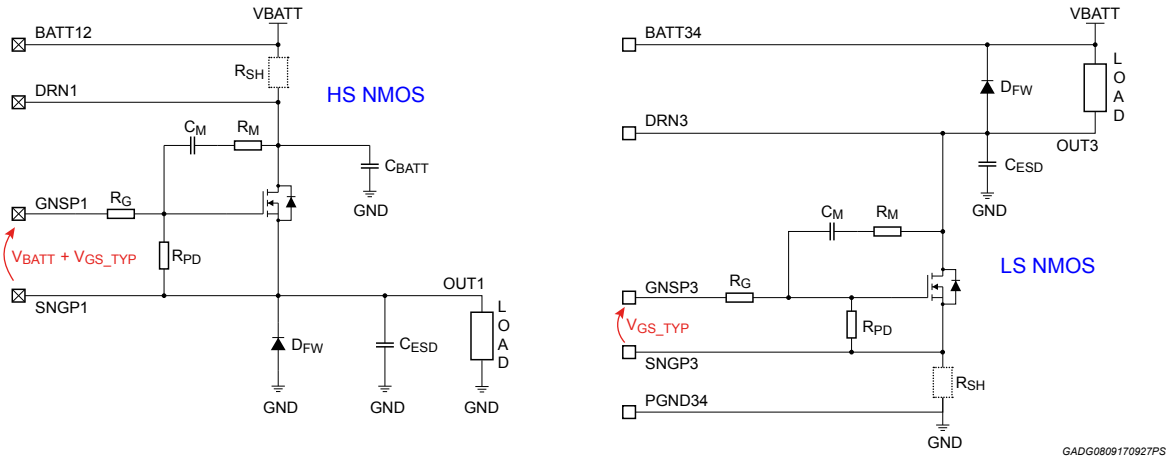
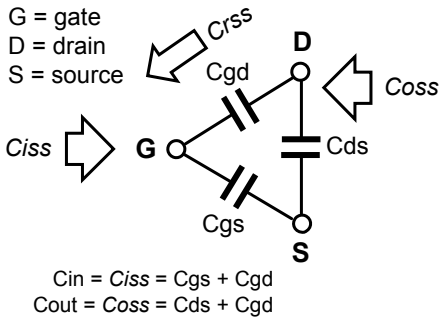


Figure 27. MOSFET internal capacitors



The presence of C_M helps smoothing the ON/OFF transitions, thus reducing the electromagnetic emissions. Consider the LS NMOS in Figure 26 and refer to the VGS turn ON profile in Figure 28:

- At the beginning of the transient, the pre-driver injects charge into the NMOS gate, until the transistor turns ON ($V_{GS} > V_{TH}$). In this phase, the CM was holding a charge equal to (see Figure 29):

  Eq: Charge stored in the Miller capacitor during transistor OFF state.

$$Q_{MOFF} = C_M{}^*V_M = C_M{}^*V_{BATT} \quad (7)$$

- As soon as the transistor turns ON, the C_M needs to be discharged following drain potential. Now the charge needs to be removed and the polarity inverted to V_{GS_TYP} (see Figure 29):

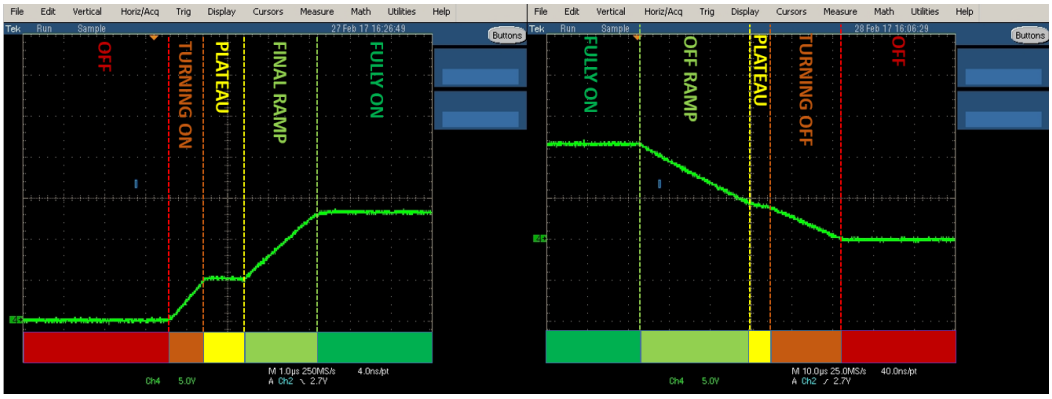
  Eq: Charge stored in the Miller capacitor during transistor ON state.

$$Q_{MON} = C_M{}^*V_M = C_M{}^*V_{GStyp} \quad (8)$$

Charge removal and polarity inversion implies current primarily flowing only through the Miller capacitor, while almost no current flows through the gate-source capacitance (CGS). Hence, the VGS is temporarily constant (see Figure 28).

- When the transistor is fully ON, its drain-to-source resistance R_{DSon} becomes very low, thus allowing huge drain current to flow without heavy losses on the transistor.

Figure 28. VGS profile for a LS configuration



Turn ON phase Turn OFF phase

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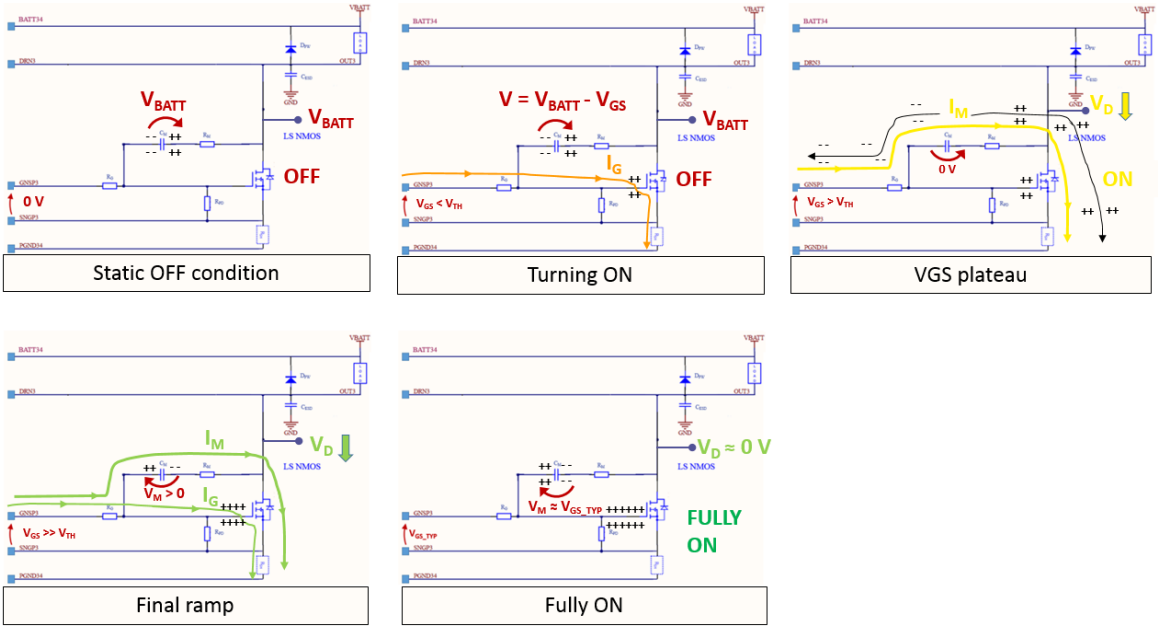
The turn OFF sequence shows a dual behavior in respect to the turn ON one. The effect of Miller capacitor during such phase is visible looking at the VGS plateau in the middle of the transition. Turn OFF phase can be described as follows:

- Initially, Ciss (C_{GD} + C_{GS}) and C_M can be considered in parallel, because they're both connected between gate and ground. In fact, since R_{DSon} is very small, the drain node is very close to 0 V, as shown in the last picture of Figure 29. Observing Figure 28, the discharge profile shows a falling ramp until V_{GS} reaches the ON threshold.
- Once V_{GS} has fallen below the ON threshold, the transistor turns OFF and the drain voltage starts raising, with a slope controlled by the pull-up network (can be either a transistor mounted on the high-side or simply a resistor). During this phase, the C_{GS} and C_{GD}+C_M are not in parallel anymore.

Figure 29. VGS turning ON sequence step by step



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Hence, the turn ON phase is always the most-relevant in terms of EMI because it determines how fast the power output switches the current into the load. In fact, in a Low Side configuration:

- The LS turn ON phase determines how fast the load current falls

- During the LS turn OFF phase, the load current slope is determined by the HS turn ON phase

The concept is exactly the same (with inverted roles) for a High Side configuration.

If the turn ON sequence is performed too fast, a huge amount of current will be switched on the drain node in a very small time, causing a high peak and generating high EMI. Hence, the Miller capacitor acts decoupling the gate and drain nodes, smoothing the transitions and lowering current and voltage peaks.

On the other hand, the presence of such capacitor implies an additional amount of charge Q_M to be supplied by the charge pump when switching ON the transistor. The main criterion for the selection of C_M is the following:

- Limit the stress induced on the charge pump
- Guarantee the turn on time needed by the application

Note: The assumption is made that the charge pump supplies both HS and LS transistors. Some pre-drivers, such as L9945, implement this feature in order to guarantee gate driver functionality also during deep battery crank.

The additional charge to be supplied by the charge pump depends on FET side, Miller capacitance value and battery supply voltage:

- For HS FETs the gate node voltage swing is $V_{GS\_TYP} + V_{PS}$

  The amount of charge to be stored in C_M is:

  Eq: Amount of charge to be stored in the external Miller capacitor for HS NMOS

$$Q_{M_{HS}} = C_M{}^* \Delta V = C_M{}^* \left(V_{GS_{typ}} + V_{PS} \right) \tag{9}$$

- For LS FETs the gate node voltage swing is V_{GS_TYP}

  The amount of charge to be stored in CM is:

  Eq: Amount of charge to be stored in the external Miller capacitor for LS NMOS

$$Q_{M_{LS}} = C_M{}^* \Delta V = C_M{}^* V_{GS_{typ}} \tag{10}$$

The dependency on battery supply voltage applies only to HS FETs and varies between Passenger Vehicle (PV) and Commercial Vehicle (CV) applications:

- For PV, the battery voltage is nominally 12 V, but V_{PS} = 14 V should be considered as the typical battery voltage
- For CV, the battery voltage is nominally 24 V, but V_{PS} = 28 V should be considered as the typical battery voltage

For instance, if CM = 1.5 nF and V_{GStyp} = 12 V:

- For HS FETs
  - PV: Q_{M_HS} = 39 nC
  - CV: Q_{M_HS} = 60 nC
- For LS FETs, Q_{M_HS} = 18 nC, independently on V_{PS}

These contributions must be converted into mean current absorption aliquots. The Q_M is an impulsive charge that must be supplied every time the external MOS is switched on. Therefore, the equivalent DC current can be evaluated dividing the charge injected on the switching period T_{SW}, as shown in the equation below:

Eq: Mean current absorption for charging the external Miller capacitor

$$I_{M_{mean}} = \frac{\Delta Q}{\Delta T} = \frac{Q_M}{T_{SW}} = Q_M{}^* f_{SW} = \begin{cases} C_M{}^* \left(V_{GS_{typ}} + V_{PS} \right)^* f_{SW} & for\ HSFETs \\ C_M{}^* V_{GS_{typ}}{}^* f_{SW} & for\ LSFETs \end{cases} \tag{11}$$

For instance, if C_M = 1.5 nF and f_{SW} = 20 kHz:

- For HS FETs
  - PV: I_{M_MEAN} = 780 µA
  - CV: I_{M_MEAN} = 1.2 mA
- For LS FETs, I_{M_MEAN} = 360 µA

3.3 IC configuration (example on L9945)

Many power applications make use of pre-driver ICs to drive external power MOS. It is essential to configure these devices in a proper way to limit EMI.

Don't use high frequency control signals when not needed:

- A peak & hold application requires high switching frequency (e.g. 20 kHz)
- Controlling a lambda probe heater doesn't (e.g. 100 Hz)

This will have the dual benefit of reducing EMI and limiting charge pump stress.

Some advanced pre-drivers like L9945 allow programming values for charge/discharge gate currents. Selecting the right value for the given application helps guaranteeing functionality while limiting emissions.

Table 3. Programmable gate charge/discharge currents for L9945

GCC_config_xx	I_{PU} / I_{PD} [mA]
00	Limited by external resistor (R_G) Internally clamped to 100 mA
01	20
10	5
11	1

Observing Figure 28, the V_{GS} charging profile is made of three phases:

- A first ramp to bring V_{GS} above threshold
- A plateau, where the NMOS is ON with a constant V_{GS}
- A final ramp that guarantees the V_{GS} overdrive necessary to obtain a small R_{DSon}

The charging phase ends when V_{GS} reaches V_{GStyp} (12 V typical). Then, the pre-driver output is controlled to keep a constant gate to source voltage, until a switch OFF command is received.

3.3.1 IC operation in constant current mode

The effect of the currents programmed in the **GCC_config_xx** bit is visible during V_{GS} plateau. In fact, during such interval, the drain voltage starts falling and controlling its slope is critical for reducing emissions. When V_{GS} shows its plateau, the Miller capacitor C_M is connected between a constant voltage node (gate) and the drain node, which is being discharged through the LS NMOS. In order to guarantee a smooth transition on the output node, the V_D slope can be controlled having a constant current flow through the Miller capacitor: the current programmed in the **GCC_config_xx** bit. In fact, the capacitor characteristics is:

Eq: Charging current for Miller capacitor during the V_{GS} plateau

$$i_{C_M} = C_M \frac{dv_{C_M}}{dt} = C_M \frac{d(v_G - v_D)}{dt}\bigg|_{v_G = cost} = -C_M \frac{dv_D}{dt} \quad (12)$$

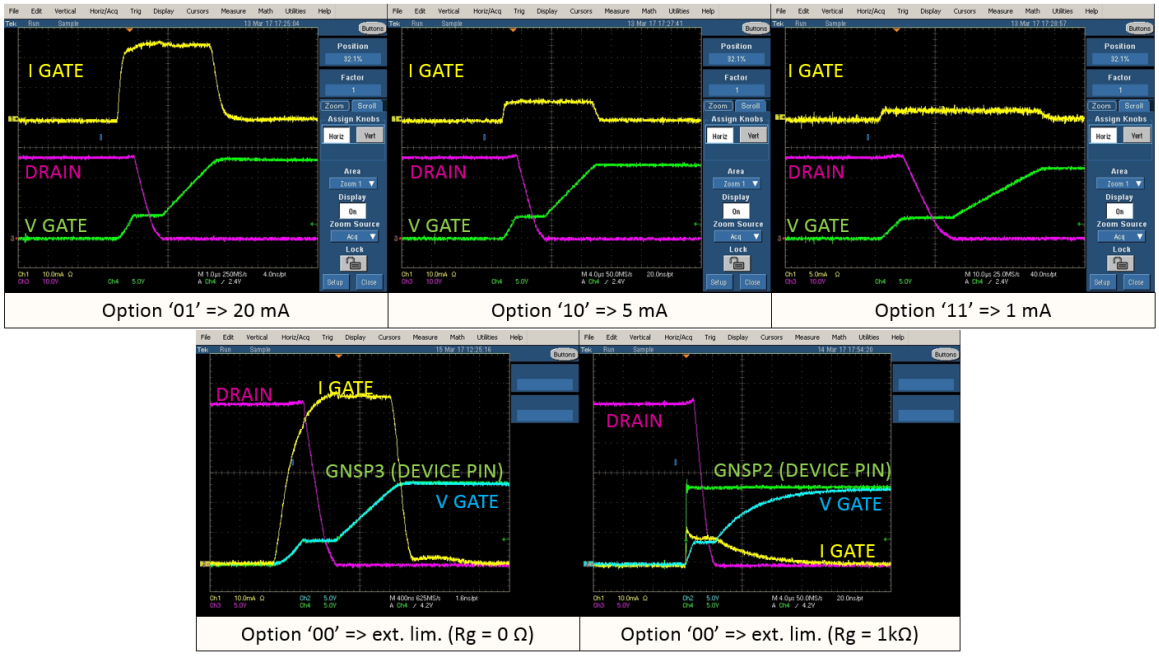
The effect of the currents programmed in the **GCC_config_xx** bit is also visible during V_{GS} turn OFF phase, in the first interval where C_{iss} (C_{GD} + C_{GS}) and C_M can be considered in parallel, as described in Miller capacitor for power drivers. During such phase, gate current can be estimated as follows:

Eq: Discharge current for Miller capacitor during the initial phase of the VGS turn OFF profile

$$i_G = (C_M + C_{iss}) \frac{dv_G}{dt} \quad (13)$$

Because the turn ON phase is the most relevant in terms of EMI, a study has been conducted on L9945 using a LS NMOS mounted on channel 1. The following pictures show the signal evolution when four different options for the **GCC_config_xx** are programmed:

Figure 30. Turn ON transient for different values of gate charge current



As can be noticed, when one of the three constant current options is selected:

- Gate current is rapidly increasing during the turn on ramp in order to bring V_{GS} above threshold
  - This represents a critical part for emissions on the gate wires: the energy to be stored in the gate and miller capacitors is released in a very short interval, meaning high power radiated. This effect can be mitigated by shortening the wires from the external FET to the L9945 pins, as described in Section 3.1.1 External FET placement on PCB
- Gate current is almost constant during the VGS plateau
  - This represents a critical part for emissions on the drain power line. Keeping the gate current constant during this phase helps having a linear transition on the drain. By choosing different values for the gate current, the transition speed can be selected according to the Eq. (13). The higher the gate current, the faster the transition, the higher the emissions
- Gate current is kept constant during the final turn ON ramp to obtain the lowest R_{DSon} possible
  - This represents a critical part for emissions on the gate wires. Because the transistor is already ON, there is no need to be as fast as in the first turn ON phase. Hence, current is kept constant in order to reduce emissions

In general, choosing a low value for the gate charge current helps reducing the emissions. However, this is not always possible: applications where timing is critical and current must be controlled with a very small ripple (as in Section 2 Example of Peak and Hold application) require fast switching, thus posing a severe constraint on gate current values.

The following table lists the data acquired for the transitions shown in Figure 30, where a C_M = 470 pF has been used:

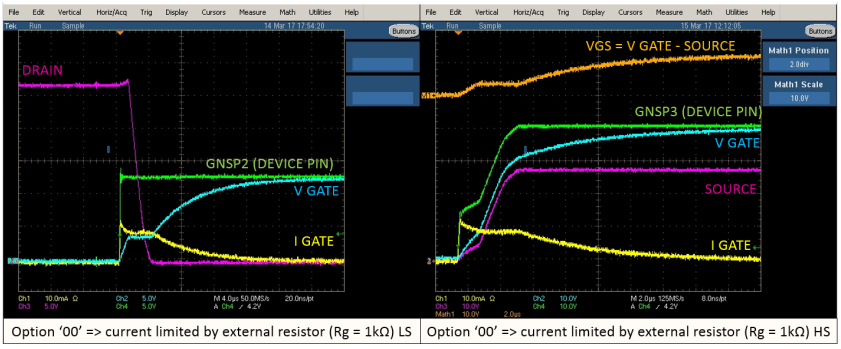
Table 4. Data acquired during the turn ON transitions using different values for gate charge current

Gate Charge Current [mA]	Measured drain voltage slope [V/µs]	Gate charge current estimation obtained using Eq. (12) [mA]	Measured gate charge current [mA]	Full transient duration [µs]
20	50	23.5	25	3
5	12.5	5.9	7.5	12
1	2.5	1.2	2	46

3.3.2 IC operation when current is limited by external resistor

L9945 offers also the possibility to limit charge/discharge current by using an external series resistor R_G on the gate line (refer to Figure 27. MOSFET internal capacitors). This option can be selected programming **GCC_config_xx = "00"**. In all other cases, the R_G resistor is not needed because current is internally regulated to one of the three programmable values.

Figure 31. Turn on transient using option "00" and mounting a 1 kΩ series resistor on gate line



LS NMOS on channel 2 HS NMOS on channel 3

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The figure above shows the turn on transient on both LS and HS NMOS configurations, using option "00" and mounting RG = 1 kΩ. Focusing on LS case, the transient steps are the following:

- When the turn on command is received, L9945 provides as much current as possible, draining it from the charge pump tank capacitor. Since the C_{GS} is discharged, it can be considered as a short-circuit at the beginning of the transient. Hence, an initial gate current peak is observed
- As soon as the voltage between GNSP2 and SNGP2 pins reaches V_{GS_TYP} (12 V typical), the internal pull-up current generator enters triode region, thus reducing the gate charge current. In a LS configuration, SNGP2 is grounded. Hence, only GNSP2 has been monitored. Because this part of the transient is very fast, the C_{GS} capacitance can still be considered as a short-circuit, and the peak current can be estimated as shown in the next equation:

Eq: Gate current peak at the beginning of the turn on transient, when the "00" option is selected

$$I_{G_{peak}} = \frac{V_{GStyp}}{R_G} \tag{14}$$

Observing Figure 31, gate current is clamped around 12 mA by circuit design, in accordance with Eq. (14).

- The gate to source voltage starts rising as C_{GS} is being charged. Voltage on the external FET gate V_{GATE} is growing until it reaches the plateau. In the meantime, V_{GNSP2} is kept constant to V_{GS_TYP}. During such phase, current is decreasing according to the following equation:

Eq: Gate current evolution before the VGS plateau (option "00" selected)

$$I_G(t) = \frac{V_{GNSP2}(t) - V_{GATE}(t)}{R_G} = \frac{V_{GS_{typ}} - V_{GATE}\left(t\right)}{R_G} \tag{15}$$

$$= I_{G_{peak}} - \frac{V_{GATE}(t)}{R_G}$$

- When the VGS reaches its plateau (ON threshold reached), voltage on the R_G resistor is constant, and so current:

Eq: Gate current during VGS plateau (option "00" selected)

$$I_{G_{plateau}} = \frac{V_{GS_{typ}} - V_{GS_{plateau}}}{R_G} \tag{16}$$

Observing Figure 31, the VGS plateau occurs around 3.5 V, which is the typical ON threshold for STD105N10F7AG transistor. Current is kept constant to 8.5 mA in accordance with Eq. (16).

- When the plateau ends, all nodes evolution continues exponentially, as typical for an RC circuit. L9945 is only keeping $V_{GNSP2} - V_{SNGP2}$ constant, but no current regulation is being performed.

The same steps apply to the ON transient analysis for an HS configuration, except that:

- Current peak described by Eq. (14) occurs when differential voltage between GNSP3 and SOURCE (SNGP3 pin) nodes reaches V_{GS_TYP}
- V_{GS} plateau occurs when both gate (blue curve) and source (pink curve) voltage are rising with the same slope, looking like parallel lines (see the orange curve).

Note how mounting R_G = 1 kΩ determines transient duration equal to:

- 24 µs for the LS configuration
- 20 µs the HS configuration

In many cases, faster transients and better EMI performances can be achieved using the IC in constant current mode. For instance, choosing the “10” (5 mA) option and considering a LS configuration, the following advantages are verified in respect to the “00” option with R_G = 1 kΩ (refer to Figure 30 and Figure 31 for comparison)

Table 5. Advantages of the “10” (5 mA) configuration in respect to the “00” option with RG = 1 kΩ

Parameter	Option “00” (limited by ext. resistor)	Option “10” (5 mA constant)	Advantage with Option “10”
Transient duration	24 µs	12 µs	50% reduction
Gate current	8.5 mA constant only during plateau	7.5 mA constant during whole transient	Lower consumption and better EMI performance
Drain voltage slope	-12.5 V/µs	-12.5 V/µs	Same load current control capability

In high demanding applications where extremely fast switches on times are required, the “01” option (20 mA) may not be sufficient to grant such speeds. In cases like Section 2 Example of Peak and Hold application, the “00” configuration might be an option in order to reduce the control loop delay. However, its effectiveness is verified only in case R_G is chosen in a useful range, to be determined as follows:

- The upper bound for R_G is represented by the performances achieved with the 20 mA configuration. The device under analysis provides a 25 mA constant current during the transient when the option “01” is selected. The same current would have been obtained in “00” configuration, only during the VGS plateau, if a resistor R_{G_MAX} had been mounted. Value for R_{G_MAX} can be obtained inverting Eq. (16):

Eq: Maximum useful RG value to match performances between “00” and “01” configurations (typical case)

$$R_{Gmax}|_{typical} = \frac{V_{GS_{typ}} - V_{GS_{plateau}}}{I_{G_{plateau}}} = \frac{12 - 3.5}{0.025} \quad (17)$$

$$= 340\Omega$$

However, to fit every case, considering process spread for both L9945 and STD105N10F7AG, the following corner case must be evaluated:

Eq: Maximum useful RG value to match performances between “00” and “01” configurations (corner case)

$$R_{Gmax}|_{min} = \frac{V_{GS_{min}} - V_{GS_{plateau}}|_{max}}{I_{G_{plateau}}|_{max}} \quad (18)$$

- The lower bound for RG is represented by the internal current limitation, preventing excessive current peaks from stressing the charge pump. The device under analysis clamps the gate charge current to a maximum value of 55 mA, measured mounting R_G = 0 Ω, as shown in Figure 32. Therefore, R_{G_MIN} can be evaluated as follows:

Eq: Minimum useful RG value to trigger internal gate current limitation (typical case)

$$R_{Gmin}|_{typical} = \frac{V_{GS_{typ}} - V_{GS_{plateau}}}{I_{G_{plateau}}} = \frac{12 - 3.5}{0.055} \quad (19)$$

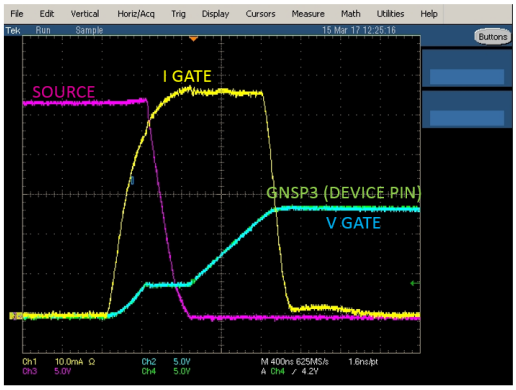
$$= 155\Omega$$

However, to fit every case, considering process spread for both L9945 and STD105N10F7AG, the following corner case must be evaluated:

Eq: Minimum useful RG value to trigger internal gate current limitation (corner case)

$$R_{Gmin}|_{max} = \frac{V_{GS_{max}} - V_{GS_{plateau}}|_{min}}{I_{G_{plateau}}|_{min}} \quad (20)$$

Figure 32. Gate charge current clamped to 55 mA when RG = 0 Ω is mounted and "00" option is selected



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The R_G useful range is strongly dependent on process spread (20 mA current precision and internal limiter spread affect the range) and external FET. To be sure of obtaining better performances in terms of turn on time, fitting every case of the process spread, ST recommends to choose option "00" with a very small resistor: 50 mΩ guarantees current limitation to be always triggered, as in figure above.

3.3.3 Case study: L9945 in a switching application

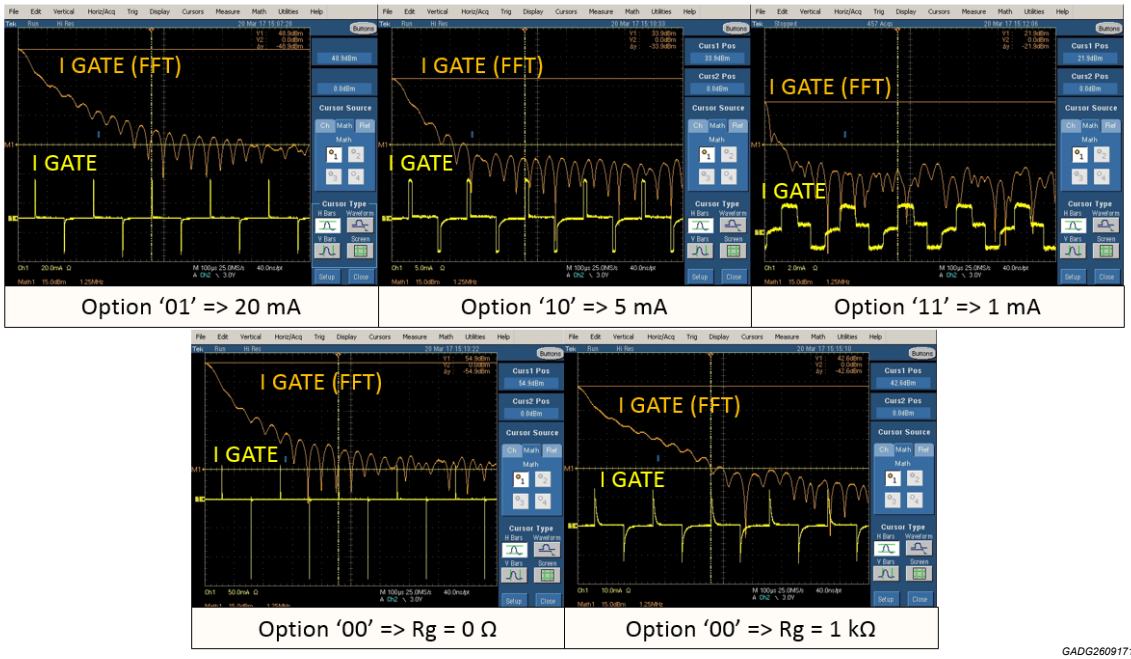
The following case study summarizes all the key points analyzed in Section 3.3 IC configuration (example on L9945), showing how IC configuration affects EMI performances in a real switching context.

In order to compare all the different configurations, the following common test bench has been adopted:

- FET type: NMOS (STD105N10F7AG)
- FET side: LS
- Channel monitored: CH1
  - Current in series to gate pin (GNSP1) monitored with current probe
  - Conversion ratio: 1 A/V
  - Acquisition mode: Hi-Res
  - Sample rate: 25 MSamples/s
- Channel control input (NON1) switching frequency: 5 kHz
- Analysis type
  - FFT with Hamming window
  - Span: 0 – 12.5 MHz
  - Resolution: 12.5 kHz
  - Floor noise: below -68 dBm

The figure below shows the analysis results for the five different configuration options explored in this paper.

Figure 33. FFT on gate current signal for different IC configurations



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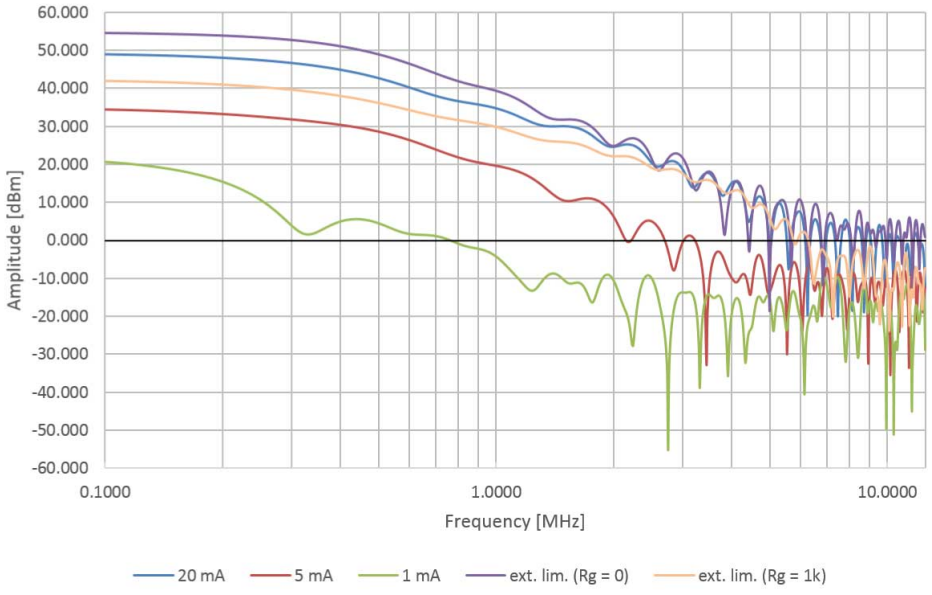
The main spectral contribution is concentrated at low frequencies, with a spectral decay strongly dependent on the selected option. It is also worth noticing that the option "00" with R_G = 0 Ω is the only one with an asymmetric current pattern. In fact, I_{GATE} is clamped only during the turn ON phase, when the charge is taken from the tank capacitor. On the contrary, no clamping occurs when switching OFF the external FET, because charge pump is not involved in the transient. As a consequence, while being the most performant in terms of switching times, the "00" option with R_G = 0 Ω is the one featuring the highest emissions.

In order to easily compare the EMI performances of the different options, FFT spectra have been overimposed in the figure below.

Figure 34. Comparison between the FFT spectra of the gate current signals obtained with different configurations



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As expected comparing the constant current options, there is a high correlation between the value of the programmed current and the EMI behavior. The 1 mA option (“11”) guarantees the best EMI performances, while the 20 mA one (“01”) features the worst EMI profile.

As already discussed in Section 3.3.2 IC operation when current is limited by external resistor (with a special reference to Table 5), the “00” option with R_G = 1 kΩ brings no advantage in terms of switching times compared to the “10” option (5 mA). The figure above confirms that also EMI profile is worsened choosing the former option, thus making this choice pointless.

On the other hand, choosing the “00” option with R_G = 0 Ω brings real advantages in terms of switching times, even if degrading the EMI performance.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
13-Mar-2019	1	Initial release.

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