Cycling endurance and data retention of EEPROMs in products of the ST25DV-I2C series, based on the CMOS F8H process

## Introduction

Electronic applications, based on integrated circuits (ICs), need a high level of reliability and robustness, each electronic component must therefore offer a very high level of quality.

To fulfill these requirements STMicroelectronics has developed a new family of Dynamic NFC Tags embedding EEPROMs, based on a new, improved architecture, and produced with the CMOS F8H process.

This application note details the improved cycling and data retention performance of the EEPROMs embedded in the products of the ST25DV-I2C series Dynamic NFC Tags, for the industrial range 6 (temperature range -40 °C to +85 °C) and range 8 (temperature range -40 °C to +105 °C or +125 °C, depending upon the package).

# Contents

# List of tables

# List of figures

# 1    NFC/RFID dynamic tags and memory technology

This document applies only to the products of the ST25DV-I2C series, namely ST25DV04K/16K/64K and ST25DV04KC/16KC/64KC, manufactured using the CMOS F8H process.

Refer to the product datasheet to know which part of the dynamic tag memory is based on CMOS F8H EEPROM (e.g. user memory and configuration registers), and which part is not (e.g. Fast transfer mode buffers and dynamic registers). The latter are not subject to cycling endurance and data retention as described in this document.

# 2 Cycling endurance

This section intends to detail the cycling capabilities of the ST25DV-I2C EEPROMs based on CMOS F8H process, industrial ranges 6 and 8 (respectively temperature range -40 °C to +85 °C and -40 °C to +105 °C or +125 °C, depending upon the package).

## 2.1 Cycling values specified in datasheets

**Table 1. ST25DV-I2C products - CMOS F8H process - Cycling values**

| Industrial range | Number of cycles for each cell |
|---|---|
| Range 6: -40 °C to +85 °C | 1 million cycles (at 25 °C) or 600k cycles (at 85 °C) |
| Range 8:<br>– -40 °C to +125 °C for SO8N and TSSOP8 packages<br>– -40 °C to +105 °C for UFDFPN8 and UFDFPN12 packages | 1 million cycles (at 25 °C) or 600k cycles (at 85 °C) or 500k cycles (at 105 °C) or 400k cycles (at 125 °C) |

## 2.2 CMOS F8H process Dynamic NFC Tags cycling performance

### 2.2.1 Cycling and temperature dependence

In this section Cycle and Cycling indicate, respectively, an internal write cycle executed by the EEPROM and the cumulated number of write cycles.

As specified in the related datasheets, the cycling endurance depends upon the operating temperature (and is independent from the value of the supply voltage): the higher the temperature, the lower the cycling performance.

This safe cycling operating area can be represented by the following equation and/or by *Figure 1*

$$\text{Number of cycles} = 1 \text{ Million} * e^{(-k*(t° - 25))}$$

where k = 0.00851 and $t^o$ is defined in Celsius degrees, and is higher than 25 °C.

**Figure 1. ST25DV-I2C products - CMOSF8H
Safe cycling operating conditions (per byte) vs. temperature[1]**
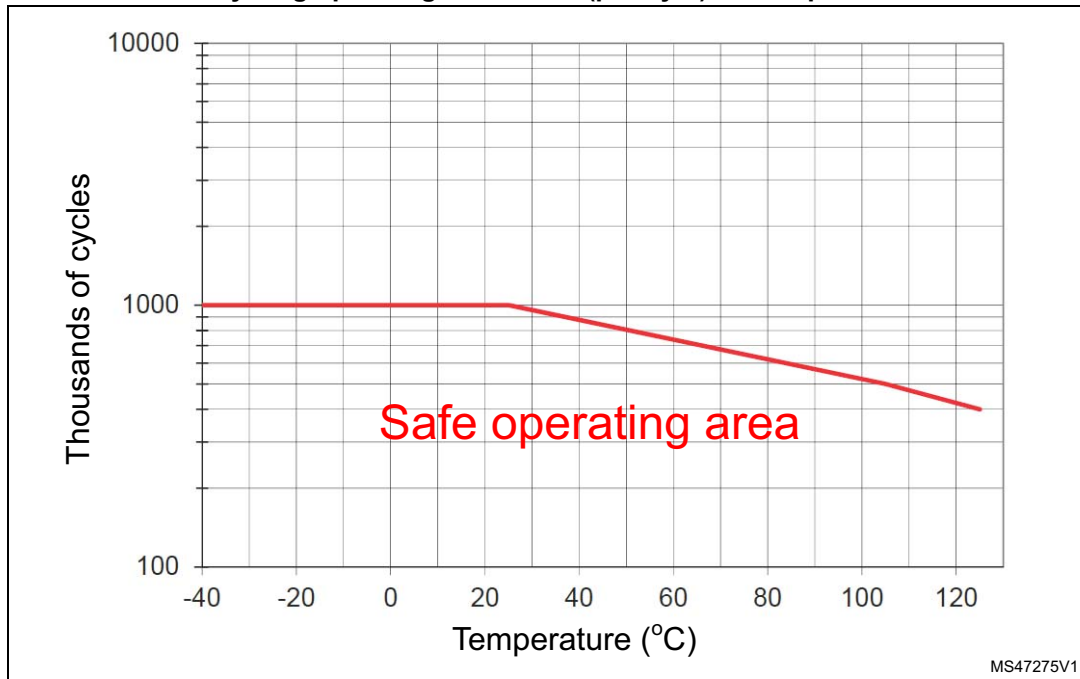


1. For temperatures lower than 25°C, the safe operating conditions are considered as 1 million cycles (the real limit is actually higher).

For a robust application design, the safe cycling operating area shown in *Figure 1* has to be considered as a maximum cycling value for each byte of the memory, going above this safe operating area is not recommended.

*Note:*       *The cycling limits measured on the CMOS F8H process devices are well above the safe area shown in Figure 1.*

## 2.2.2   Cycling qualification method

The qualification procedure of devices produced with the CMOS F8H process identifies the cell cycling intrinsic[a] performance over the full temperature range. During the qualification phase, the parts are cycled and then read in order to locate the failing bits (if any).

In STMicroelectronics, the CMOS F8H process EEPROM intrinsic failure criterion is defined as 1 failing cell (or less) over 10 million cells.

---

a. Intrinsic = belonging to the essential nature or constitution of the EEPROM die (extrinsic = originating from random events).

### 2.2.3 Overall number of write cycles

When evaluating the cycling performance of an application, the number of cycles can be defined either for each memory cell or for the overall number of cycles decoded by the whole memory:

– the maximum cycling value defined in datasheets is the maximum number of cycles for each byte

– the overall number of cycles is the number of cycles correctly decoded and executed by the device, spread over all addressed locations in the memory.

The characterization trials performed on ST25DV-I2C products manufactured with the CMOS F8H process have demonstrated that the overall number of write cycles at 125 °C can reach 512 millions without failures (test performed on ST25DV64K range 8 device).

## 2.3 Cycling strategy

### 2.3.1 Cycling strategy and application temperature profile

To ensure the safest EEPROM cycling conditions, it is recommended to evaluate the number of write cycles and the relative temperature profile of the cycling performed by the EEPROM during the life of the application, that is:

• define the main temperature ranges at which the device is operating in the end application,

• for each temperature range, estimate the number of write cycles executed for each data block,

• for each data block (with different cycling profiles), calculate the cumulated cycling effect using the following equation or *Table 2*.

$$\sum_{i=1}^{n} \frac{\text{Number of cycles at temp(i)}}{\text{Max Number of cycles specified at temp(i)}} \leq 1$$

**Table 2. Application cycling profile evaluation[1]**

| Temperature | Number of cycles[2] | % of the maximum cycling value specified in *Table 1* |
|---|---|---|
| 25 °C | w | (w / 1M) x 100 = a (%) |
| 85 °C | x | (x / 600k) x 100 = b (%) |
| 105 °C | y | (y / 500k) x 100 = c (%) |
| 125 °C[3] | z | (z / 400k) x 100 = d (%) |
| Total | w + x + y + z | a + b + c + d (%) |

1. The table can be adapted according to the temperature profile by inserting the maximum cycling for each temperature.

2. w, x, y and z are the anticipated number of cycles for a specific data block.

3. SO8N and TSSOP8 packages only.

If the total percentage of cumulated cycles (last row in *Table 2*) is lower than 100%, data stored in the EEPROM are safely cycled.

If the total percentage of cumulated cycles is above 100%, the intrinsic safe margin for cycling is exceeded and a data relocation strategy must be defined. This can be done by distributing the number of cycles over several memory locations as follows:

• define a cycling limit for each data block according to the application needs and product performance (as shown in *Table 2*)

• count the numbers of cycles executed on each data block (counter value can be stored in the EEPROM)

• when the counter exceeds the defined limit, the cycled data block must be relocated to another physically independent memory address. The software developer should define this new data block to be duplicated in a location inside a different page and, when possible, not with the same byte address inside the new page. The counter itself must also be stored in a new location.

In addition, to optimize the number of cycles in the EEPROM and keep the other data blocks safe in the memory array:

• define data classes (located in the same page) where data with similar update rates are gathered together (this optimizes the use of the Page mode instead of the byte mode)

• the areas containing the read-only parameters and the cycled items must be separated and made as much as possible independent from each other. Two types of data should not share the same pages and, where possible, the same locations inside the related page.

# 3 Data retention

This section intends to offer all details concerning the data retention capabilities of the ST25DV-I2C products based on CMOS F8H process, industrial ranges 6 and 8.

*Data retention definition:*

– *At $t_0$, bytes are written, and then no Write is executed on these bytes. The data retention time is the time, after $t_0$, during which the bytes can still be correctly read (the EEPROM devices being DC supplied or not).*

## 3.1 CMOS F8H process data retention performance

### 3.1.1 Data retention and temperature dependence

The CMOS F8H process EEPROM data retention is temperature dependent and is independent from the value of the supply voltage ($V_{CC}$): the higher the temperature, the lower the data retention time.

Device mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard. Extended mission profiles can be assessed on demand.

The data retention safe values are defined in *Table 3*.

**Table 3. ST25DV-I2C products - CMOS F8H process - Data retention values**

| Industrial range | Data retention safe values |
|---|---|
| Range 6: -40 °C to +85 °C | More than 40 years at 55 °C or more than 20 years at 85 °C |
| Range 8:<br>– -40 °C to +125 °C for SO8N and TSSOP8 packages<br>– -40 °C to +105 °C for UFDFPN8 and UFDFPN12 packages | More than 40 years at 55 °C or more than 20 years at 85 °C or more than 10 years at 105 °C or more than 5 years at 125 °C |

### 3.1.2 Data retention qualification method

The data retention qualification procedure for the ST25DV-I2C products manufactured with the CMOS F8H process checks that the data written into the EEPROM remain readable with a safe programming level. The ST qualification method is:

– the part is stored in an oven at 200 °C for 4000 hours (or for an equivalent time / temperature combination), with no DC voltage on pin $V_{CC}$
– the part content is then checked.

The data retention follows an Arrhenius law, so it is possible to extrapolate, from the different qualification tests performed at different temperatures, the CMOS F8H process data retention limits. These limits are above the safe value defined in datasheets.

## 3.2 Data retention strategy in the end application

The data retention time is defined in the datasheets with specific temperatures. In order to ensure the safest EEPROM data retention, it is advisable to evaluate the amount of time during which the end application remains within a temperature range to evaluate the data retention profile, that is:

- define the time (in years) during which the EEPROM remains inside each temperature range (that is, the typical temperature profile of the end application)

- for each temperature range, estimate the data retention value, in percentage, as defined in the following equation or in *Table 4*.

$$\sum_{i=1}^{n} \frac{\text{Number of years at temp}(i)}{\text{Max Number of years specified for temp}(i)} \leq 1$$

**Table 4. Data retention profile evaluation example[1]**

| Temperature | Data retention (max) | Application ambient temperature in years[2] | Data retention capability percentage |
|---|---|---|---|
| 55°C | V = 40 years | v | (v / V) x 100 = a |
| 85°C | W = 20 years | w | (w / W) x 100 = b |
| 105°C | X = 10 years | x | (x / X) x 100 = c |
| 125°C[3] | Y = 5 years | y | (y / Y) x 100 = d |
| Total | | v + w + x + y | (a + b + c + d) |

1. The table can be adapted according to the temperature profile by inserting the appropriate data retention capability for each temperature.

2. v, w, x and y are the anticipated number of years for a given temperature.

3. SO8N and TSSOP8 packages only.

**Example**

An EEPROM is used in an application with a temperature profile defined as:

- 5 years at 85 °C (i.e. 25% of the maximum data retention time at this temperature)

- 20 years at 55 °C (i.e. 50% of the maximum data retention time at this temperature)

The data will be safe for 25 years, with only 75% of the data retention capability being used (5 years + 20 years is 25 years, with 25% + 50% = 75% of data retention capability).

# 4 Revision history

**Table 5. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 06-Oct-2017 | 1 | Initial release. |
| 08-Feb-2018 | 2 | Updated *Section 2.2.3: Overall number of write cycles*. |
| 03-May-2021 | 3 | Document scope extended to ST25DV-I2C series.<br>Updated document title, *Introduction* and *Section 1: NFC/RFID dynamic tags and memory technology*.<br>Removed former *Table 1: Applicable products*.<br>Minor text edits across the whole document. |