12 V – 150 W power supply based on STNRG011 digital combo and SRK2001 adaptive synchronous rectifier controller

Introduction

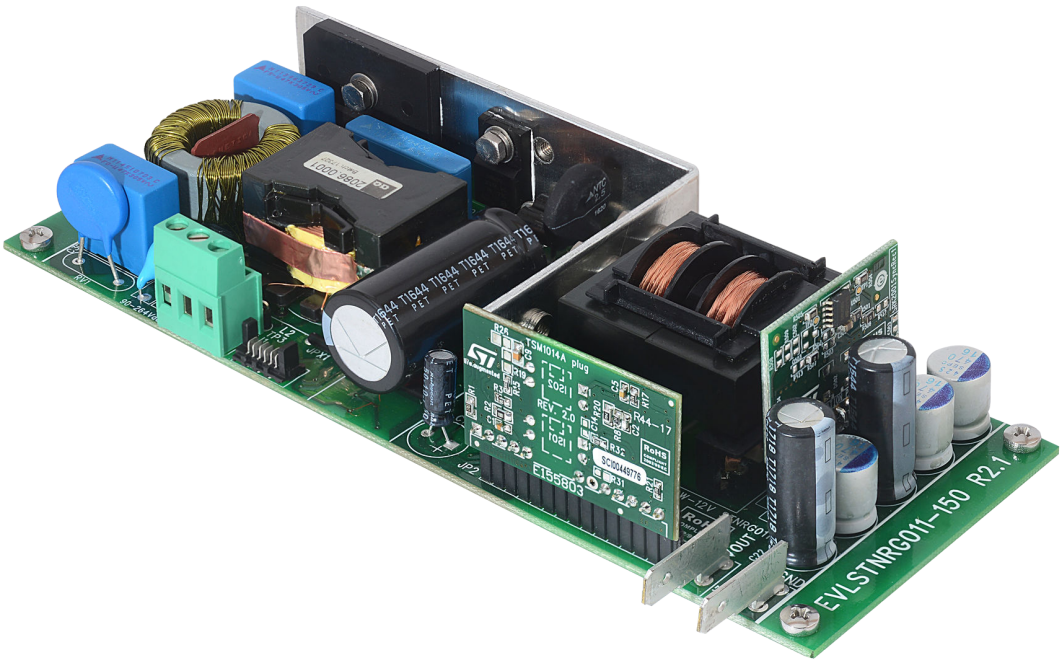
The AN5118 application note describes the EVLSTNRG011-150, a 12 V, 150 W power supply demonstration board for 90 Vac to 264 Vac mains, which is representative of an AC/DC converter for an all in one (AIO) computer or a general purpose high power adapter.

The design is based on the STNRG011 IC, a digital combo that controls a two stages AC/DC SMPS. The front-end is a transition mode PFC pre-regulator and the second stage is an LLC HB resonant converter. The SRK2001 implements the synchronous rectification in order to obtain higher efficiency.

No auxiliary supply is needed due to the very low consumption at the no-load.

A full set of auxiliary functions and protections is also provided, this allows to reduce the overall BOM while maintaining a rugged design.

Figure 1. EVLSTNRG011-150 demonstration board



1 STNRG011 the digital controller approach

The STNRG011 digital combo is a PFC + LLC digital controller that allows design of a high efficiency SMPS with the minimum component count.

Even though architecture of this demonstration board is somehow conventional and already seen with analog controllers, the full advantage of a digital implementation using the STNRG011 IC can be obtained without writing a single line of code. In fact, all the firmware and software are embedded in the controller, while the required flexibility can be achieved through a complete set of parameters, stored in its non-volatile memory (NVM), which allows the configuration and fine tuning of the application.

Moreover, if special, custom, functions are required, they can be coded and written in an external EEPROM: at the start-up the controller will read this code and integrate it in the original SW.

The same memory is also used by the STNRG011 to store all the housekeeping data.

A two wires serial bus is used for all the communications between the STNRG011, EEPROM and an (optional) external device. A programmable asynchronous serial protocol is used for data exchange between the controller and the external unit, while the I2C allows to access the EEPROM.

A PC, with a dedicated HW interface which guarantees the galvanic isolation, can be connected to the serial bus of the board, and a windows-based application with a graphical user interface (GUI) is available for the complete configuration and monitoring of the application.

Related documents

Additional information and details about parameters setting and the GUI and related hardware can be found in the following documents:

- UM2340 - STNRG011 NVM parameters description
- UM2342 - Getting started with the STEVAL-PCC020V1: USB to I²C UART interface board and associated GUI for STNRG products
- AN5119 - How to design an application from draft with STNRG011

This evaluation board has been developed starting from the existing STEVAL-ISA170V1 demonstration board, based on full analog control. Its application note (AN4677) can be used to have as a comparison between a fully analogue design and the digital one.

The NVM parameters stored into the STNRG011 are showed in: Section 6: Appendix A - NVM parameters configuration.

1.1 Target specifications

Table 1. Target specifications

Table 1 summarizes the main specifications that were taken into account for the board design.

Parameter	Value	Note
Input mains range	90 ÷ 264 Vac - frequency 45 ÷ 65 Hz	-
Output power	0W - 150 W continuous operation, 200 W peak	(1)
Nominal output voltage	12 V	-
Output voltage regulation	± 5%	(2)
Ripple / noise	< 120 mVp-p	(3)
Full load efficiency	>90% at 115/230 Vac	-
Avg. efficiency (at 25, 50, 75, 100% of full load)	>90% at 115/230 Vac	-
Efficiency (at 250 mW)	>60% at 115/230 Vac	-
No-load mains consumption	<75 mW	-
Hold-up time	>10 ms	-
Mains harmonics according to	EN61000-3-2 Class-D and JEITA-MITI, Class-D	-
EMI	According to EN55022 Class-B	-
Safety	According to EN60950	-
Dimensions	175 x 65 x 35 mm	-
PCB	Double side, 70 mm, CEM-1, mixed PTH/SMT	-

1. *Peak powerloading for 100 ms minimum.*
2. *Steady state and dynamic load (0.5 A/ms), no-load to full load.*
3. *Measured over band width of 20 MHz with a 10 µF electrolytic capacitor in parallel with a 100 nF ceramic capacitor placed at the point of measurement.*

1.2 Electrical diagrams

Figure 2. **Mother board electrical diagram**

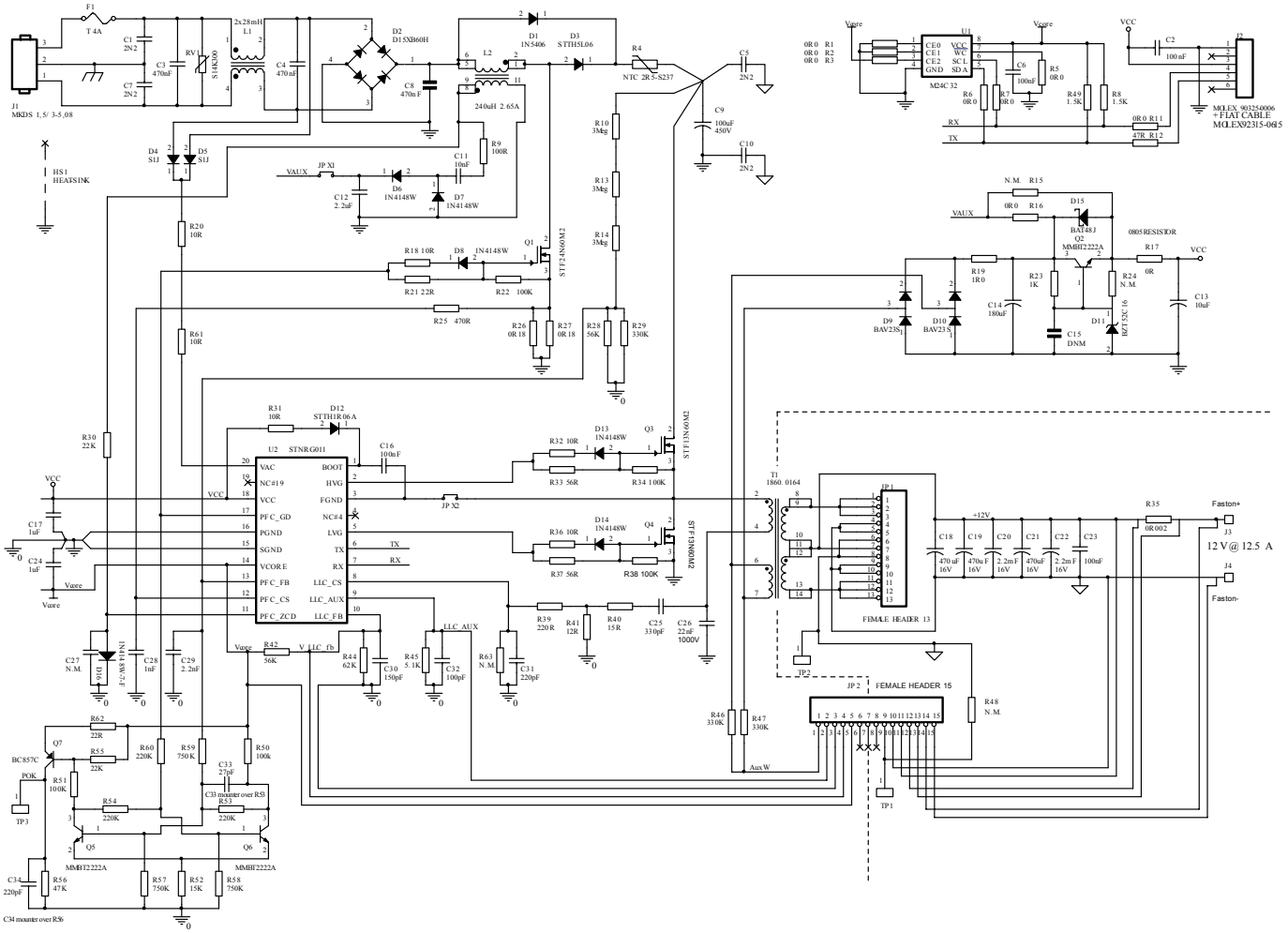


Figure 3. **Synchronous rectification (SRK) board electrical diagram**

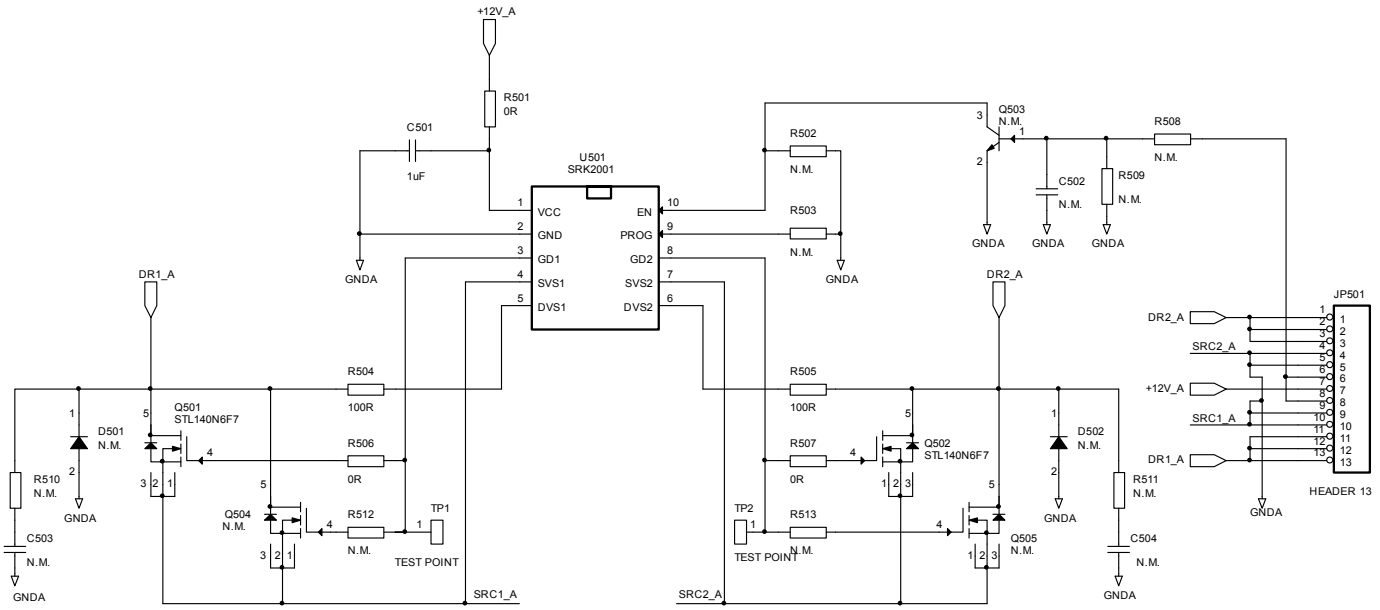


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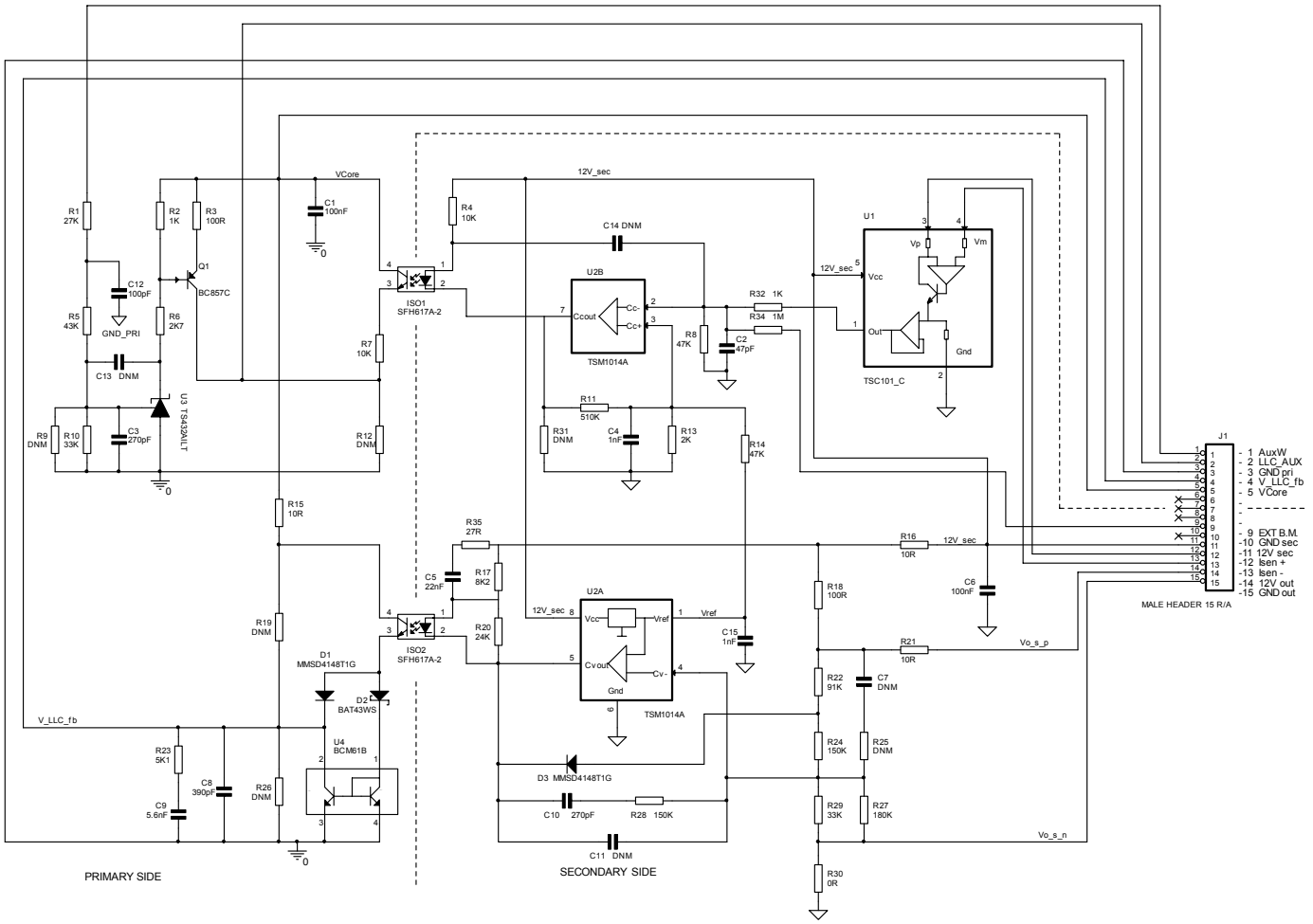
Figure 4. **Feedback (control) board electrical diagram**



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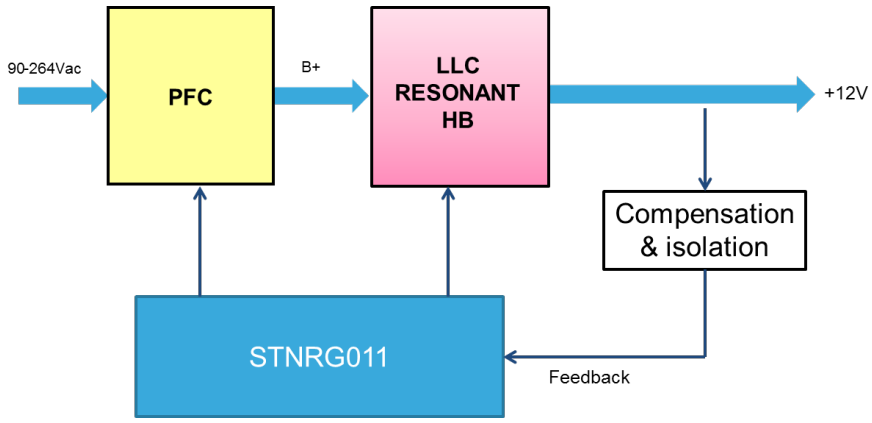
1.3 Board architecture

The block diagram of the demonstration board is showed in Figure 5: the architecture is a standard transition mode PFC pre-regulator that generates the 400 V bulk voltage and an LLC half bridge resonant downstream converter that generates the isolated 12 V output.

The feedback signal comes from the secondary side with an optocoupler that guarantees galvanic isolation from the primary to secondary side. All the compensation related network for the LLC converter is analog and located on the secondary side of the converter. The SRK2001 synchronous rectification is used on the secondary side to increase the overall efficiency of the board.

Figure 5. Block diagram of the demonstration board



The design of the demonstration board reflects the analog implementation described on the AN4677. For this reason only the major differences will be analyzed.

1.3.1 PFC power boost

The PFC power section, is a standard PFC TM design. The ST proprietary ramp enhanced constant on-time (ReCOT) algorithm of the STNRG011 allows the user to reach high PF and low THD even with high input capacitance at the mains input. The board and a complete sets of protection allows the design of the PFC with very low components count.

1.3.2 LLC half bridge DC / DC converter

The LLC half bridge resonant converter is designed to have a resonance frequency of about 100 kHz. The ST proprietary “Time Shift Control” algorithm of the STNRG011 allows high input voltage ripple rejection, even with single pole compensation. Due to the tight requirement imposed, the LLC control loop has a more complex configuration than usual.

The IC's protections for the LLC stage will always ensure the correct mode of the operation, and avoid entering into the capacitive region. The new burst mode functionality guarantees the minimum power consumption at low loads.

1.3.3 Synchronous rectification

The synchronous rectification is the standard SRK2001 demonstration board with the PowerFLAT 5 x 6 package STEVAL-ISA168V. The SR-MOSFETs have been changed with the new STripFET F7 power MOSFET STL140N6F7, which guarantees higher performance and lower switching losses compared with the STL140N4LLF5 mounted on the standard demonstration board. Also, the disabled circuit has been removed as the feature is not used in this application.

1.3.4 LLC control loop

It is worth noting that the tight requirements imposed, lead to a configuration more complex than usual, while for relaxed specs, conventional solutions can be used.

Table 2 indicates for each requirement the consequent main constraint and its implication.

Table 2. Design constraints vs. implications

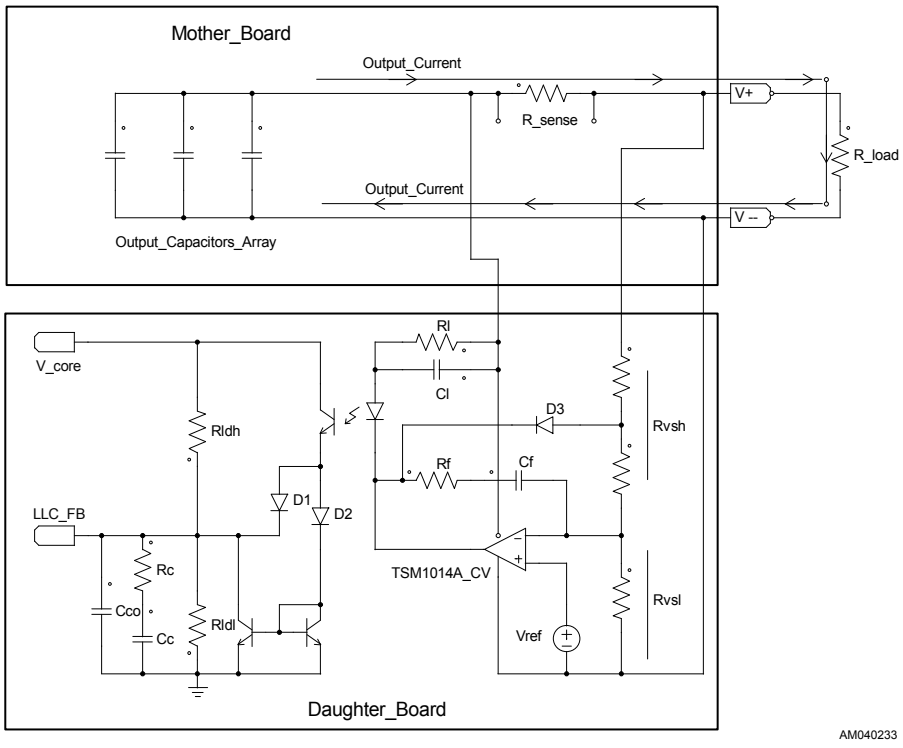
Constraints	Implications
DC accuracy	High DC loop gain, remote sense
Load transient response	Controlled large signal behavior, avoid saturation
Stability	Small signal transfer function with adequate phase margin
Output ripple	High bulk voltage rejection ratio: high gain attwice the line frequency
Power consumption at no-load	Reduced currents, also for the optocoupler

An analog solution has been chosen to control the output voltage of the SMPS, in order to minimize the delay between an output voltage change and the correction of the time shift value that compensates it, assuring in this way a fast response to load transients and good dynamic behavior.

The output voltage of the resonant converter is set by means of an analog feedback loop: a TSM1014A, at the secondary side, provides a voltage reference and an error amplifier that compares the resistor divided output voltage to its internal reference. The diode cathode of the optocoupler is driven by the error amplifier output, while its anode is connected to the output capacitors array through an R-C parallel network. On the primary side, the phototransistor of the optocoupler is configured as an emitter follower and drives the “diode section” of an integrated current mirror (BCM61B). Two diodes, D1 and D2 are introduced to clamp the current mirror's output in case of overdrive, whilst also avoiding saturation. The current mirror feeds a complex load and the central node of a voltage divider; this node is also connected to the LLC_FB pin of the STNRG011 IC, which voltage is sampled and converted into a digital number that is used by the SMEDs as the time-shift value for LLC power stage control.

Figure 6 shows the reference circuit diagram of the LLC control loop, used hereafter to describe its behavior.

Figure 6. Control loop reference circuit diagram



1.3.4.1 V_{out} remote sense

Due to the high load current (12.5 A and greater during peak power) and as the TSM1014A controller is mounted on a daughter board, it has been decided to connect the output voltage sense resistors (Rvsh, Rvsl) to the output Faston connectors through dedicated PCB traces, as indicated in the circuit diagram in Figure 6.

In this way the sense circuit is separated from the output current path and a more accurate measurement of the voltage at the output terminals can be obtained.

1.3.4.2 Secondary side error amplifier

The CV section of the TSM1014A compares the output voltage divided by Rvsh and Rvsl, to its internal reference voltage and drives the cathode of an SFH617A photodiode, while its anode is connected to the output capacitors through the Rl and Cl.

With this configuration the current through the photodiode is controlled by two paths

- A “slow” one implemented by the TSM1014A and its compensation network
- A “fast” one composed by the parallel Rl and Cl

In static conditions the TSM1014A fixes the operating point and then the output voltage with good accuracy, while in case of fast load transients the photodiode current is also modulated by the output voltage variations through the Rl and Cl, speeding up the response.

1.3.4.3 *Primary side optocoupler load*

The standard primary side optocoupler's transistor configuration is the common emitter with a resistor of several kΩ placed between its collector and the supply.

The main drawback of this solution is that the high output capacitance of the phototransistor (approximately 3 nF to 8 nF) with the relatively high resistive load introduces a pole at low frequency in the response of the circuit, with a consequent slow transient response.

To avoid this, the load resistor could be reduced, but this would increase the power consumption.

Instead, a better solution is implemented by connecting the phototransistor as the emitter follower that drives a current mirror. In this way the phototransistor sees low impedance, and the pole is pushed at higher frequencies, while maintaining the required resistive load.

Figure 7 shows the basic circuit diagram used for a simple simulation of the two configurations, while Figure 8 shows the resulting waveforms.

Figure 7. Optocoupler configurations

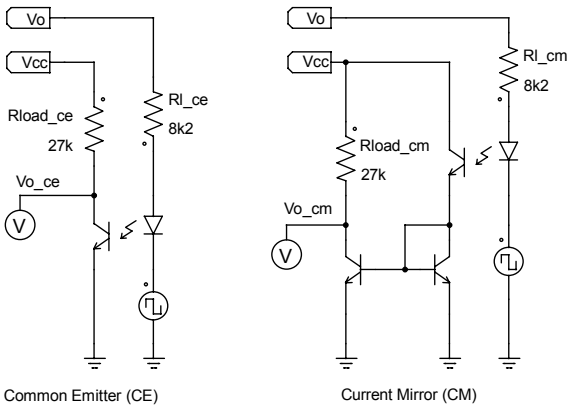
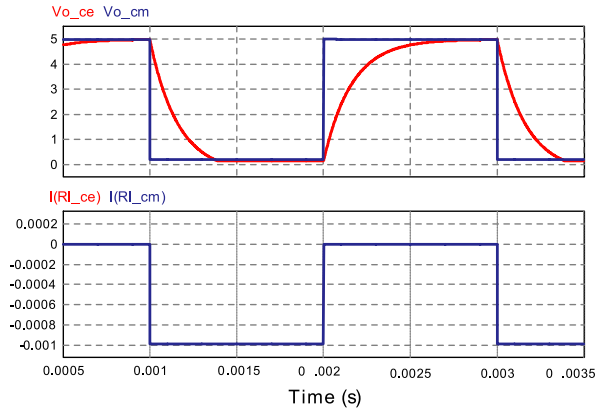


Figure 8. Transient responses



Upper plot: Vo_ce in red and Vo_cm in blue
Lower plot: Rl and photodiode current

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As can be seen the current mirror configuration is much faster, and in case of overdrive (due to heavy load transients) it avoids the phototransistor saturation and the consequent delay in response.

In order to analyze this point also in the frequency domain (small signal), a simple circuit that is representative of the actual configuration has been implemented with an SFH617A optocoupler

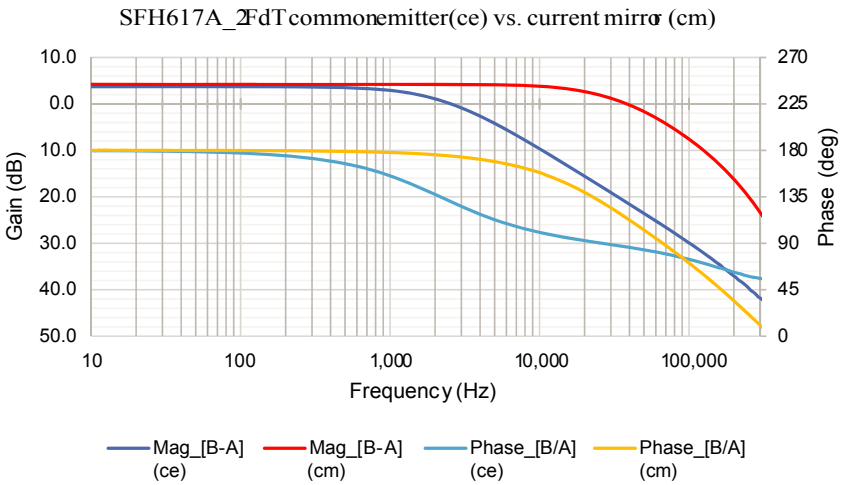
- The photodiode was polarized with a dc source with a series resistor, in order to fix the static current at 400 µA
- The phototransistor was configured either as a common emitter or with the current mirror circuit

In both cases the same resistive load has been used and it has been connected to a fixed voltage source to set up the bias voltage at 1.5 V.

A network analyzer has been connected for both configurations to measure the transfer function, defined as the ratio between the output voltage on the resistive load and the photodiode current, in the gain and phase.

Figure 9 compares the two structures: the current mirror configuration has bandwidth about an order of magnitude wider than the common emitter.

Figure 9. CE and CM optocouplers configurations frequency response



1.3.4.4 *Voltage clamps*

During heavy load transients, the nodes of the feedback path can be driven well out of the linear region and then the recovery time to the steady state may be long. For this reason a clamp mechanism has been introduced, both on the primary and on the secondary side.

On the primary side two diodes the D1 and D2 are placed between the emitter of the phototransistor and the collectors of the two transistors of the current mirror. In this way, in case of an overdrive, when an excess current flows in the optocoupler, D1 conducts and avoids the transistor saturation.

The second diode D2 has been introduced to raise the clamp level of the LLC_FB voltage to about 360 mV, thus accelerating the response when exiting burst mode.

Moreover the current mirror load is composed of two resistors, one towards Vcore (equal to 56 kΩ) and the other towards ground (equal to 62 kΩ), such that when no current flows through the optocoupler, the LLC_FB voltage is limited to 2.627 V, about 100 mV above the A/D converter full scale of 2.5 V.

The clamp circuit on the secondary side has been introduced to avoid TSM1014A saturation and to limit the maximum current in the photodiode. This has been done by splitting the resistor between Vout and the inverting input of the error amplifier and placing a diode between these two resistors and the TSM1014A output. In steady state condition the CVinput equals the CV+ (1.25 V of the reference voltage), and then the converter output voltage is at the nominal value of 12 V while the node between the two resistors is at 7.97 V.

If the output voltage goes above the regulation point, the TSM1014A output is forced low, but it is clamped to 7.97 V - 0.7 V = 7.27 V because the diode starts conducting.

Taking into account a voltage drop on the phototransistor of 1.1 V, the maximum voltage excursion on the photodiode series resistor (equal to 8.2 kΩ) is: 12 V - 7.27 V - 1.1 V = 3.63 V, that leads to a maximum current in the photodiode equal to 3.63 V / 8.2 kΩ = 443 µA.

With this current the circuit must guarantee that the LLC_FB pin voltage goes towards zero (actually below the clamp voltage on the primary side), so the phototransistor has to sink the entire current that is equal to Vcore / 56 kΩ = 89 µA.

In other words, when the maximum current of 443 µA flows in the photodiode, the phototransistor must sink 89 µA, and then the minimum CTR required for the optocoupler is 89 µA / 443 µA = 0.2 at a bias current of about 400µA.

1.3.4.5 *Control loop stability*

A good starting point for the definition of the compensator is the evaluation of the transfer function of the power section (plant). In order to do this, the TSM1014A CV operational amplifier can be overcompensated increasing the Cf value between 0.1 µF and 1 µF and reducing Rf to a few hundred Ω: in this way the system would behave as having a single pole at low frequency: the plant transfer function can be measured with the network analyzer with this configuration, starting from low output current, and then increasing the output power while observing the output and feedback voltages, immediately stopping in case of signs of instability.

With this approach it was noted that the most critical condition from the stability point of view was at the full load, when the plant first pole was at the highest frequency and the gain loop has the highest bandwidth. For this reason the analysis and the fine-tune was performed at this condition.

In the performance verification section can be found the final plots of the transfer functions of the power section, the compensation network, and the complete gain loop.

2 Functional verification

2.1 Startup

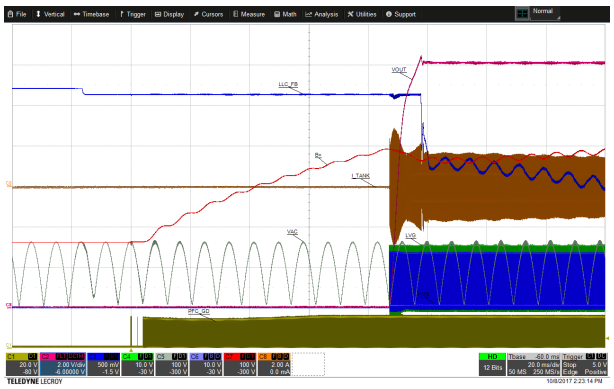
As soon as the mains is applied, the STNRG011 starts sinking current from the VAC pin, charging the VCC capacitor. The total VCC capacitor charging time is strictly related to the total capacitance connected to the VCC pin. When the VCC voltage reaches the 17 V threshold (Vcc_{On} threshold) the device turns on. It requires at least 1 complete mains cycle to perform the MCC synchronization. After that, the device turns on at the estimated peak of the mains voltage and at the falling edge of the internal MCC line comparator (i.e. at about 135° of the sinusoidal voltage), in order to estimate the resonance period of the PFC boost section for the TM and valleys skipping operation. The PFC soft-start begins at the next mains estimated zero crossing, with a fixed power set by the “PFC pss” parameter.

The PFC soft-start ends when the PFC reaches the value set by the NVM with the parameter “PFC Vout SS end (delta)”. The NVM of the device installed into the demonstration board is set in the order to end the PFC soft-start when the bulk voltage reaches approximatively 396 V. The LLC soft-start begins only at the next mains estimated zero crossing, until the output voltage reaches the regulation. The LLC soft-starts ends when the LLC feedback reaches the steady state condition.

Figure 10 and Figure 11 show the full load startup from the PFC soft-start to the end of the LLC soft-start, when the mains voltage is 115 Vac / 60 Hz and 230 Vac / 50 Hz respectively.

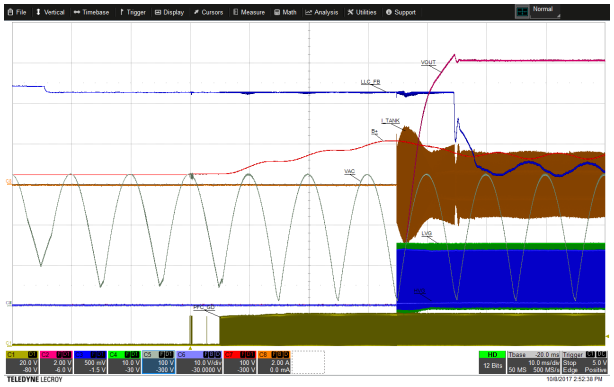
Figure 12 shows the PFC synchronization and startup, while the Figure 13 shows the LLC startup with the safe start procedure that avoids hard switching during the firsts turn-on.

Figure 10. Full load startup at 115 Vac / 60 Hz



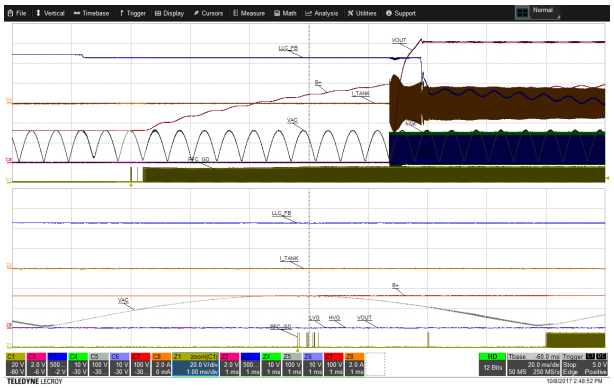
CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = VAC; CH6 = HVG; CH7 = B+; CH8 = I_TANK

Figure 11. **Full load startup at 230 Vac / 50 Hz**



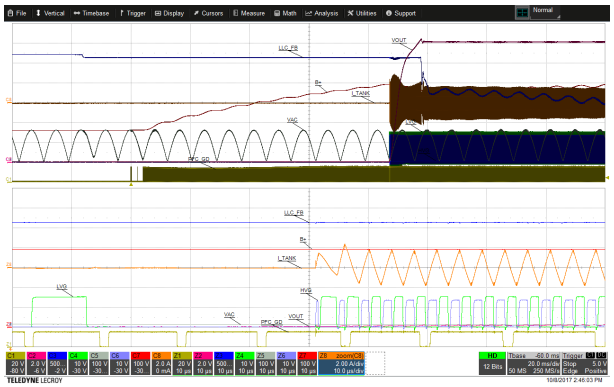
CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = VAC; CH6 = HVG; CH7 = B+; CH8 = I_TANK

Figure 12. **Full load startup at 115 Vac / 60 Hz, PFC turn-on**



CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = VAC; CH6 = HVG; CH7 = B+; CH8 = I_TANK

Figure 13. **Full load startup at 115 Vac / 60 Hz, LLC turn-on**



CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = VAC; CH6 = HVG; CH7 = B+; CH8 = I_TANK

2.2 Early warning feature

The STNRG011 has integrated the early warning feature to generate an early warning signal in case the system is shutting down. This feature is important in the PC power application where all the supplied devices must be informed that the power supply is shutting down. The early warning signal is generated on the PFC_FB pin, putting it up to 5 V and the information is latched with the Q5 and Q6 latch circuitry. The latch is reset as soon as the PFC gate drive restarts switching. Even though the demonstration board application is an adapter power supply and the early warning feature is not necessary, it is still enabled in order to clarify how a practical application could be. For more information regarding the Power OK circuitry, please refer to Section 9.3.

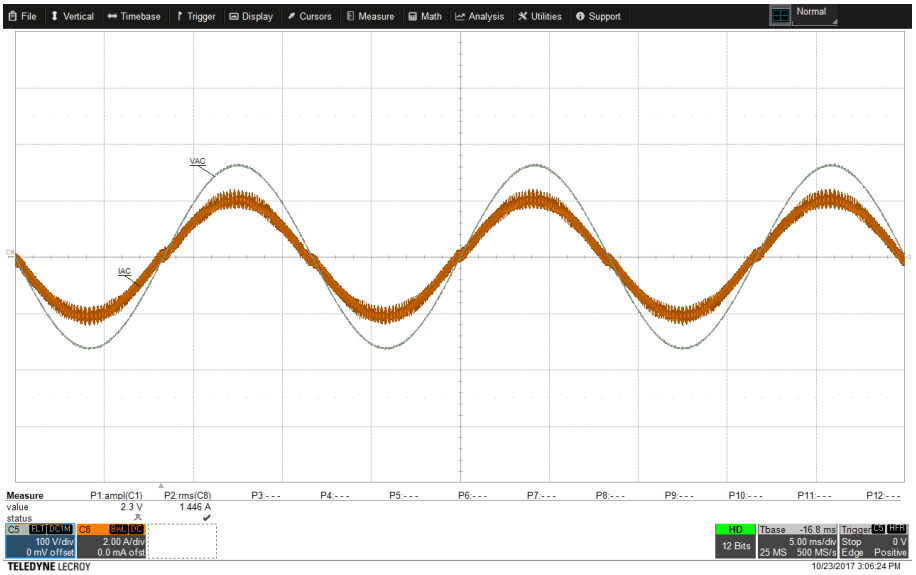
2.3 PFC operation

2.3.1 ReCOT functionality

The STNRG011 controls the PFC MOSFET turn-on time with the proprietary ramp enhanced constant on-time algorithm. It compensates the input EMI filter capacity, to increase the PF and consequently to reduce the THD, keeping it low not only at the full load.

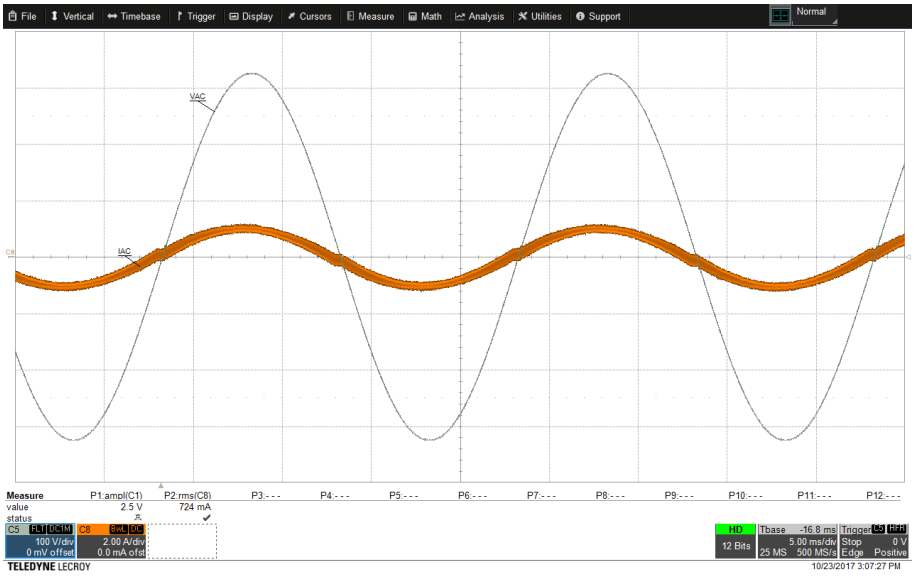
Figure 14 and Figure 15 show the input voltage and current at 115 Vac / 60 Hz and 230 Vac/50 Hz respectively.

Figure 14. Input voltage and current at 115 Vac / 60 Hz, full load



CH5 = VAC; CH8 = IAC

Figure 15. **Input voltage and current at 230 Vac / 50 Hz, full load**

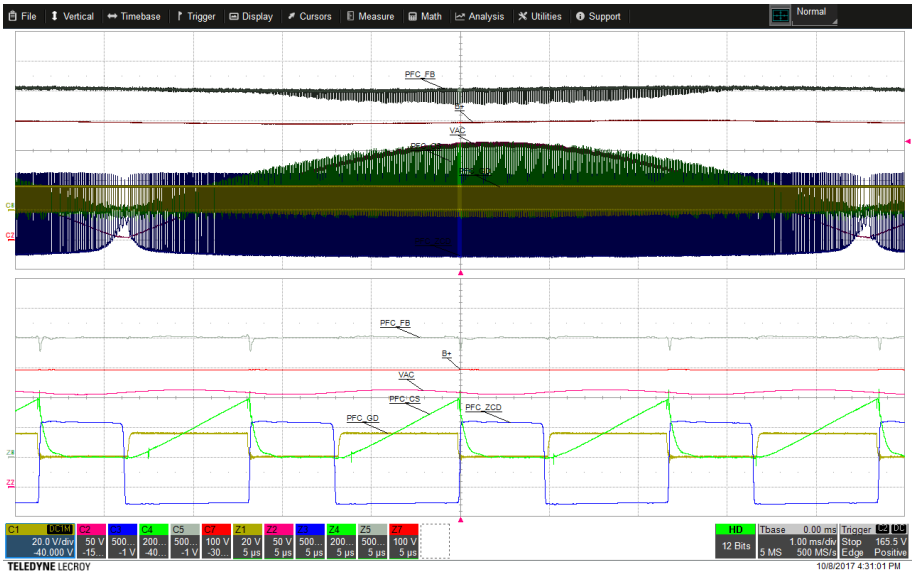


CH5 = VAC; CH8 = IAC

2.3.2 Operating modes: transition mode, valleys skipping and DCM

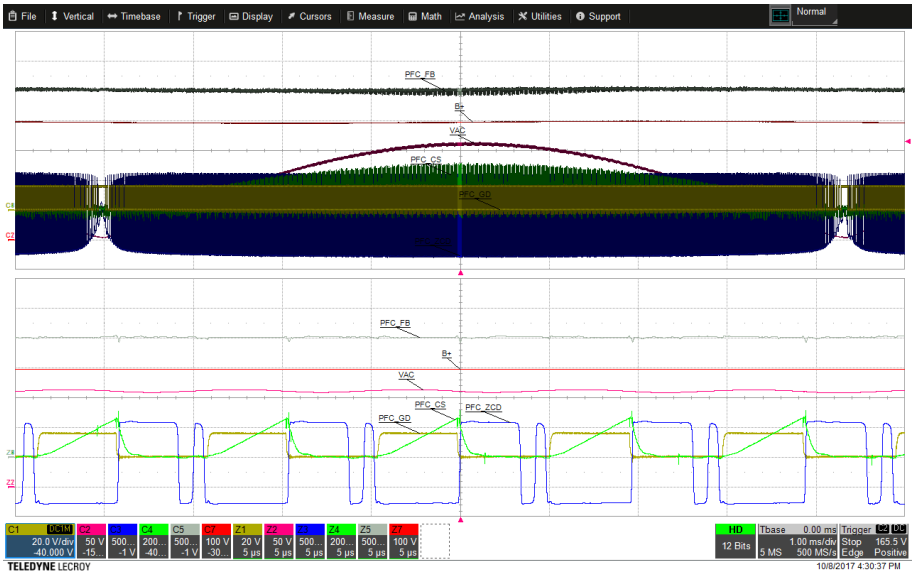
The PFC manager changes the operating mode dynamically, obtaining optimal performance in terms of both efficiency and THD, from the transition mode to DCM, passing through one, two or three valleys skipping. This is possible thanks to the NVM configurability that allows to match the IC to the application. Figure 16 to Figure 20 show the different operating modes of the PFC.

Figure 16. **Multi-mode PFC in TM**



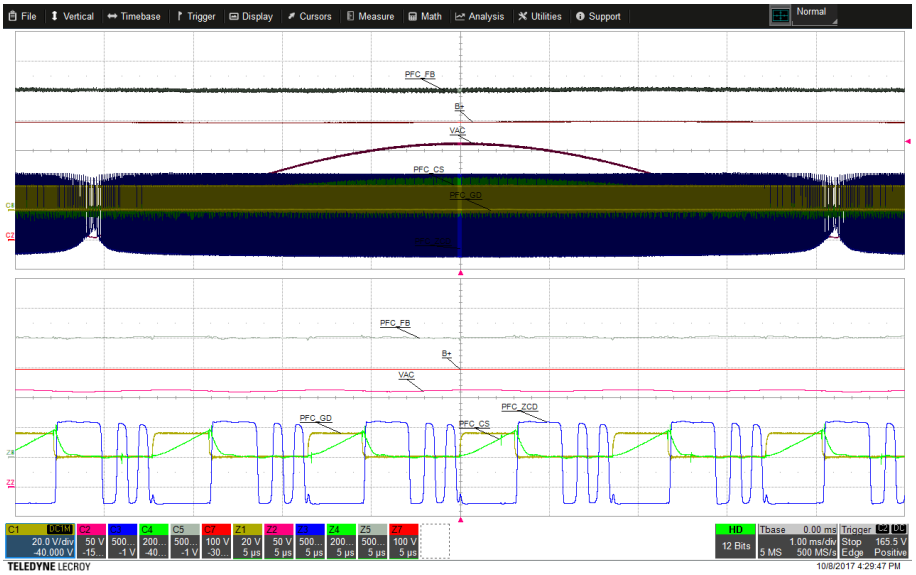
CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 17. **Multi-mode PFC skipping 1 valley**



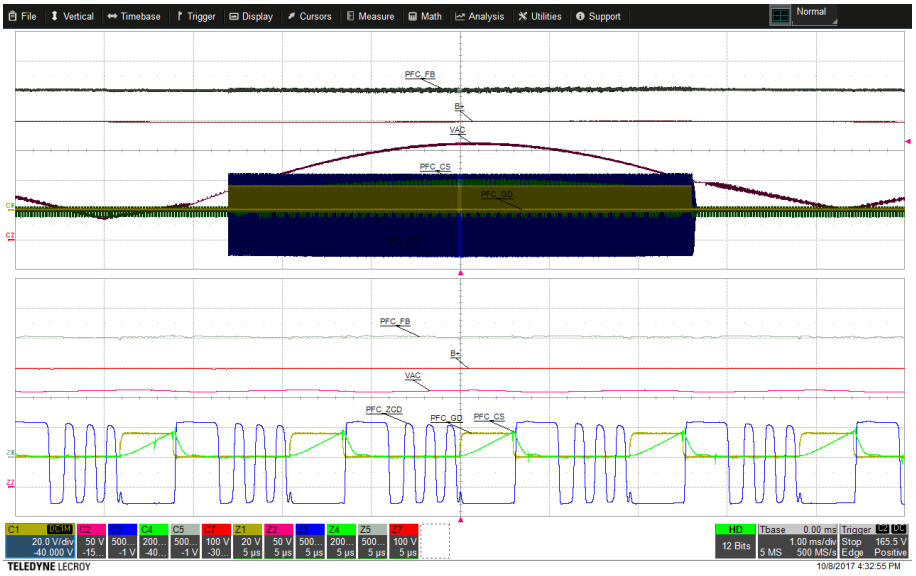
CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 18. **Multi-mode PFC skipping 2 valleys**



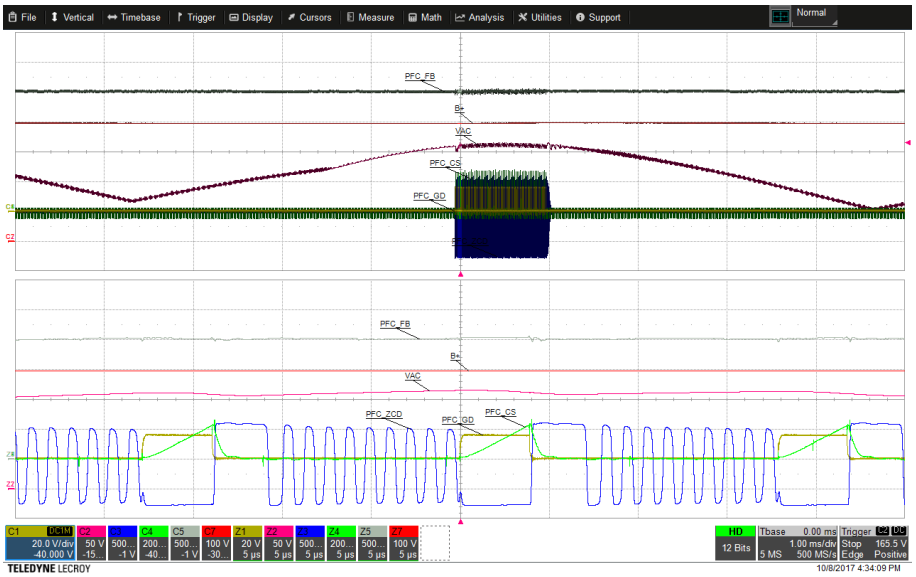
CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 19. **Multi-mode PFC skipping 3 valleys and narrow skipping area**



CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 20. **Multi-mode PFC in DCM and deep skipping area**



CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

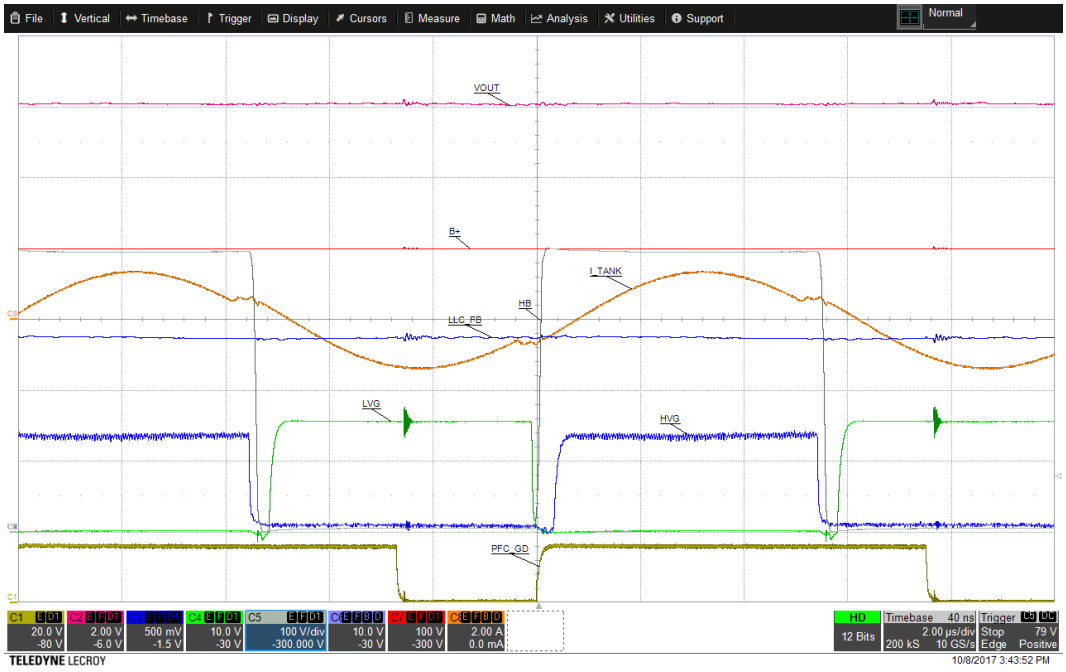
2.3.3 Skipping area functionality (below 75 W)

The skipping area feature allows toreduce the PFC dissipated power, turning-on the PFC MOSFET only during the peak of the line voltage, either by reducing the lost power (reducing the number of switching cycles) and by increasing the performance of the PFC where the transferred power is more efficient. The skipped area increases when the load decreases and the entering threshold has been set in order to be out of the skipping area feature when the input power is 75 W and above, in order to be compliant with the mains harmonic reduction standards at that power threshold. When the system is working in the skipping area power region, the operating mode and the MOSFET on-time are not fixed but modulated depending on the requested power, as can be seen in previously Figure 19 and Figure 20.

2.4 LLC operation: symmetric time shift control

The “Symmetric time shift control” is the evolution of the time shift control that always guarantees 50% of the duty cycle for the half bridge resonant converter. The algorithm changes the time between the zero current detection and the MOSFET turn-off of the low side MOSFET and the cycle-by-cycle copies the total on time to the high side MOSFET. The time shift applied is directly converted from the LLC_FB pin, while the dead time between half bridge gate drivers is set by the “LLC dead time” NVM parameter. Figure 21 shows the resonant stage key waveforms at the full load.

Figure 21. **LLC resonant converter key waveforms**



CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = HB; CH6 = HVG; CH7 = B+; CH8 = I_TANK

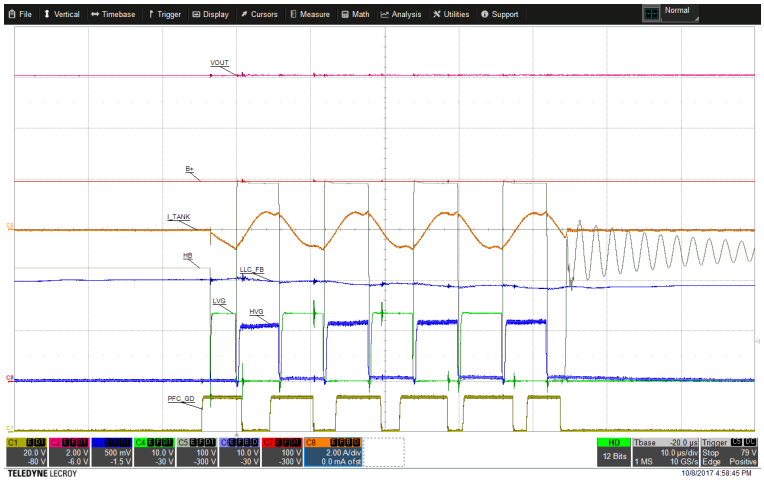
2.5 Burst mode

The STNRG011 has three kinds of the burst mode: the LLC_FB controlled burst mode, the pure external burst mode and the hybrid external burst mode.

The EVLSTNRG011-150 and the NVM of the installed STNRG011 is configured to use the LLC_FB controlled burst mode, but the demonstration board is ready for the pure external burst mode, by changing two NVM parameters.

During the burst mode, the PFC is always synchronized with the LLC and the PFC MOSFET on-time is modulated in order to reduce acoustic noise. Figure 22 shows a burst mode sequence at the no-load.

Figure 22. **Burst sequence details at no-load**



CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

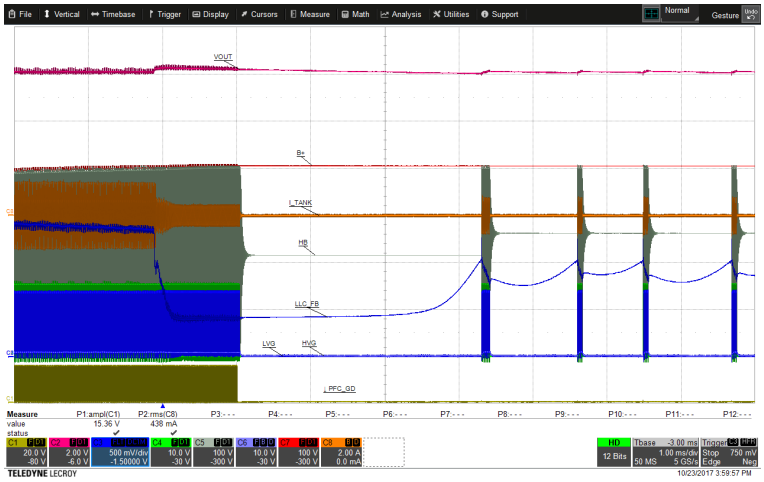
2.5.1 Feedback controlled

Figure 23 shows the behavior of the demonstration board when the LLC_FB voltage goes below the threshold sets by the “LLC_FB burst entering threshold” parameter. After the digital filtering set by the “Burst entering digital filtering” parameter, the system enters the burst mode.

Each burst sequence is performed when the LLC_FB value triggers the wake-up comparator, whose threshold is set by the “LLC_FB burst wake-up thr” parameter. The number of burst pulses is modulated depending on the load. Figure 22 shows a burst sequence at the no-load, where the number of burst pulses is the minimum and set by the “Min number of burst pulses” parameter. Figure 24 shows a burst sequence before exiting the burst mode, where the number of burst pulses is the maximum and set by the “Max number of burst pulses (delta)” parameter If the load increases, as soon as the period of consecutive burst sequences is lower than the “Minimum period to exit burst” parameter, the system exits the burst. This is shown in Figure 25.

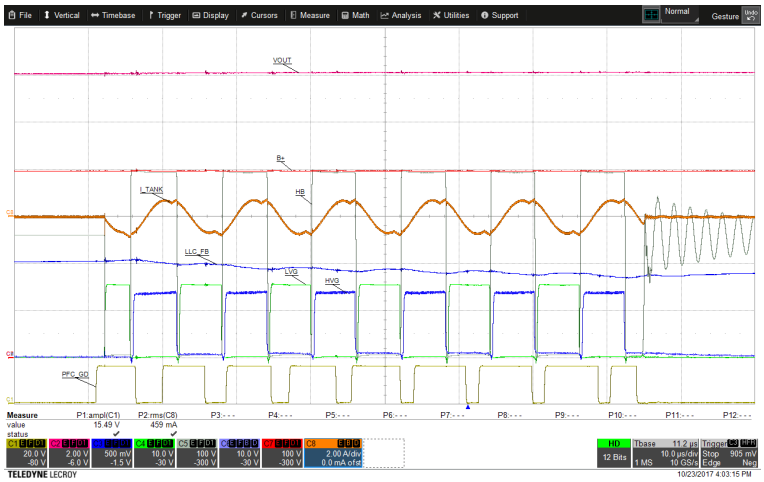
In order to respond to a heavy load transient, the system exits the burst mode also in case the LLC_FB voltage after the burst sequence is sensed higher than the “LLC_FB burst wake-up thr” parameter minus the hysteresis set by the “LLC_FB burst wake-up hyst” parameter. This is shown in Figure 26.

Figure 23. Burst mode entering with a full load to 0.3 A transient



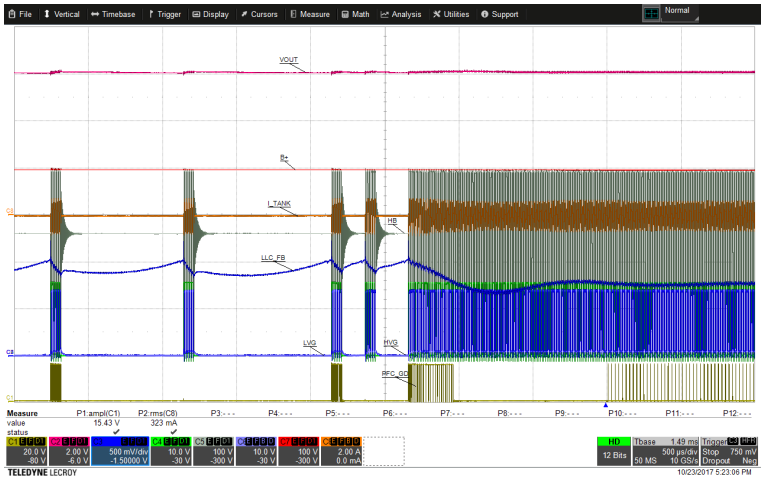
CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 24. Burst sequence detail with the maximum number of burst pulses set



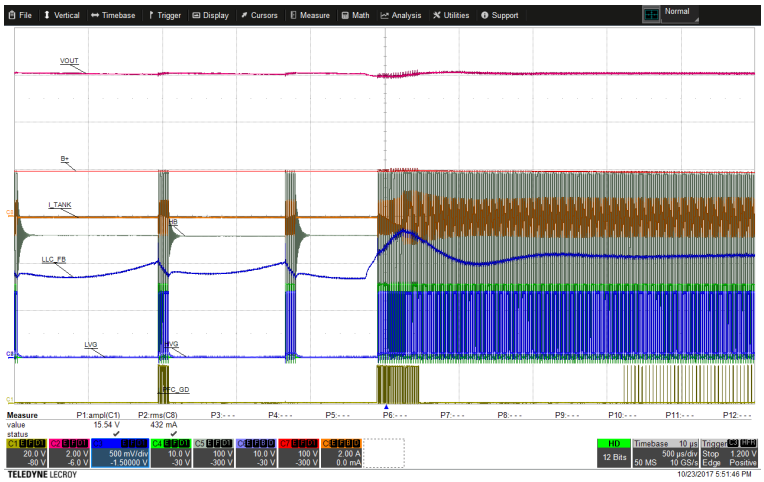
CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 25. Burst mode exiting with 0.3 A to 1 A load transient



CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 26. Burst mode exiting with 0.3 A to 5 A load transient



CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

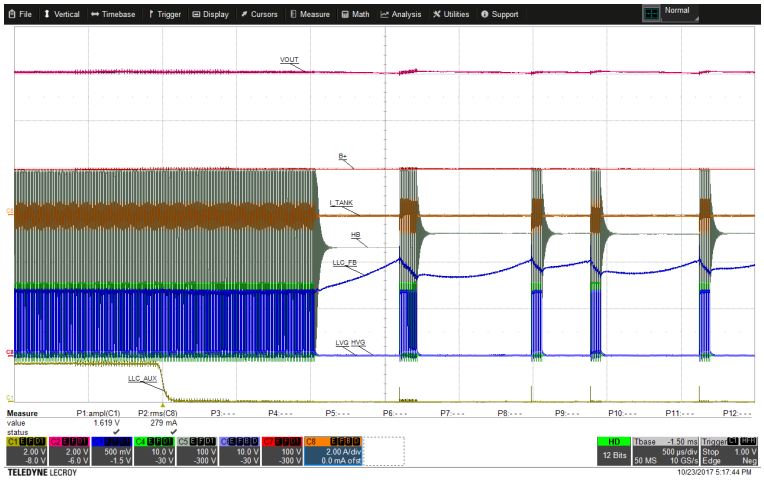
2.5.2 Load current controlled

In order to enable the load current controlled burst mode, it is necessary to change two NVM parameters. In particular, the “External burst mode” parameter must be set to “enabled” and the “LLC_FB burst entering threshold” parameter must be set to the minimum, otherwise the hybrid external burst mode will be enabled, but it is not effective for this demonstration board.

When the secondary side burst mode comparator senses the output current below its threshold, the LLC_AUX pin is pulled below 0.8 V and, after the digital filtering is set by the “Burst entering digital filtering” parameter, the system enters the burst mode, as shown in Figure 27. The burst mode function is still managed by the LLC_FB voltage and a burst sequence is started when it triggers the wake-up comparator, whose threshold is set by the “LLC_FB burst wake-up thr” parameter.

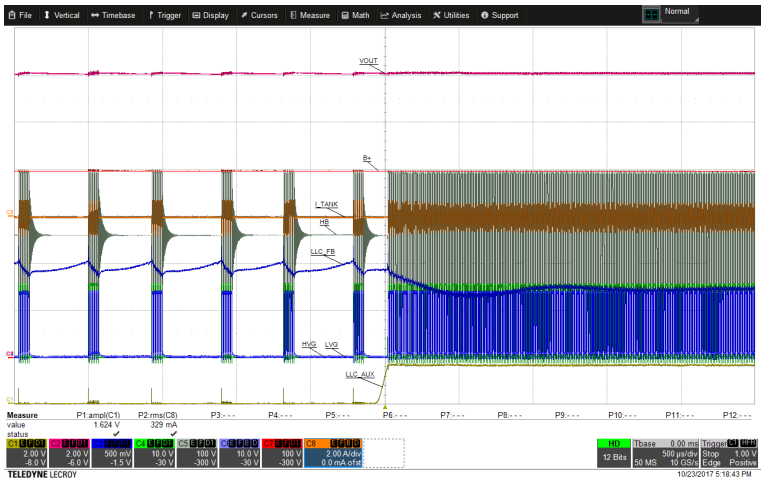
The system exits the burst mode when the secondary side current level exceeds the comparator threshold and the LLC_AUX pin goes above 0.9 V. This is shown in Figure 28.

Figure 27. External burst mode entering



CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 28. External burst mode exiting

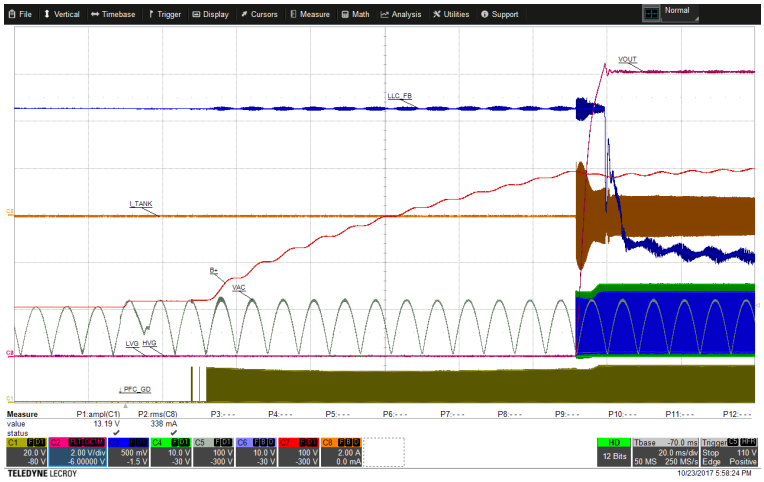


CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

2.6 Brown-in / brown-out

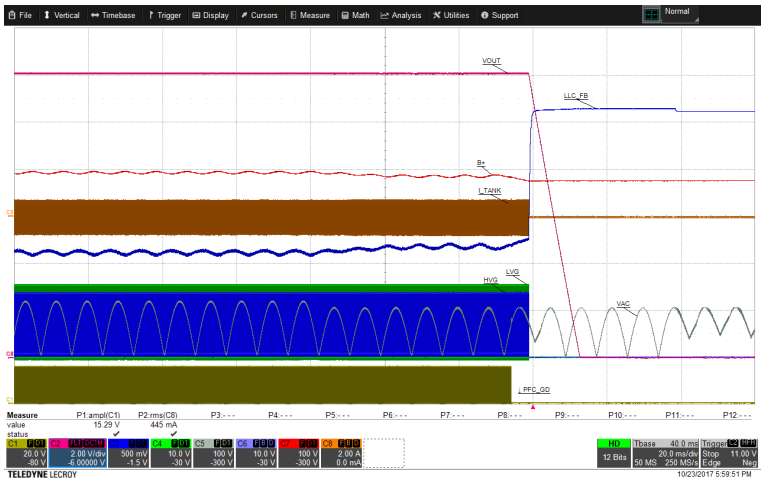
The STNRG011 has integrated the mains brown-in / brown-out function. Figure 29 and Figure 30 show both functions, when mains voltage changes from 75 Vac to 85 Vac and vice versa.

Figure 29. **Brown-in during line transient from 75 Vac to 85 Vac**



CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

Figure 30. **Brown-out during line transient from 85 Vac to 75 Vac**

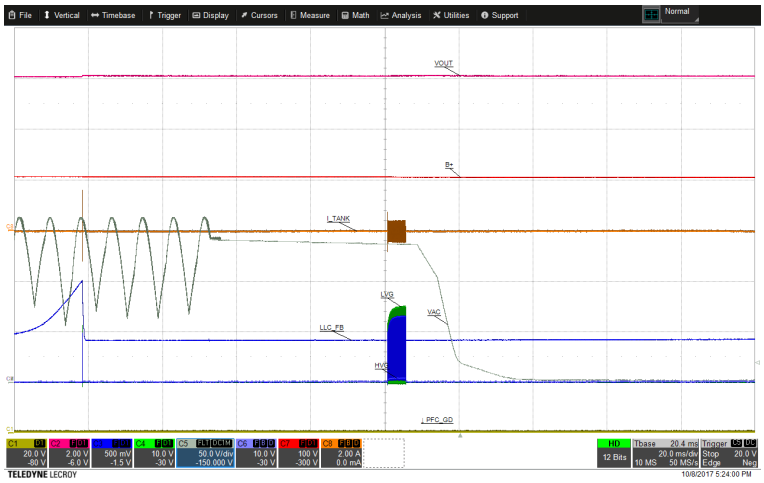


CH1 = PFC_GD; CH2 = VAC; CH3 = PFC_ZCD; CH4 = PFC_CS; CH5 = PFC_FB; CH7 = B+

2.7 X-cap discharge

The integrated X-cap discharge (XCD) function compliant with the IEC 62368-1 is activated any time there is no activity sensed on the line, for about 50 ms. Figure 31 shows the activation of the XCD function at no-load, simulating the cable unplugging on the mains connector. As soon as the STNRG011 detects the inactivity, it restarts LLC switching for 5 ms in order to generate the early warning signal and to keep the output regulated. This feature could be disabled in case the application is not designed to keep the output voltage regulated at the no-load, by changing the “EW signal in burst mode” NVM parameter from “normal” to “quick”. This will apply for any early warning managed fault in the burst mode.

Figure 31. **X-cap discharge function activation and normal early warning pulse at no-load**



CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = VAC; CH6 = HVG; CH7 = B+; CH8 = I_TANK

2.8 Mains dip

The system was designed to keep the output voltage regulated if a half-cycle mains dip occurs. Figure 32 shows the behavior of the demonstration board at 230 Vac / 50 Hz: the output voltage stays within the regulation bandwidth during the mains dip.

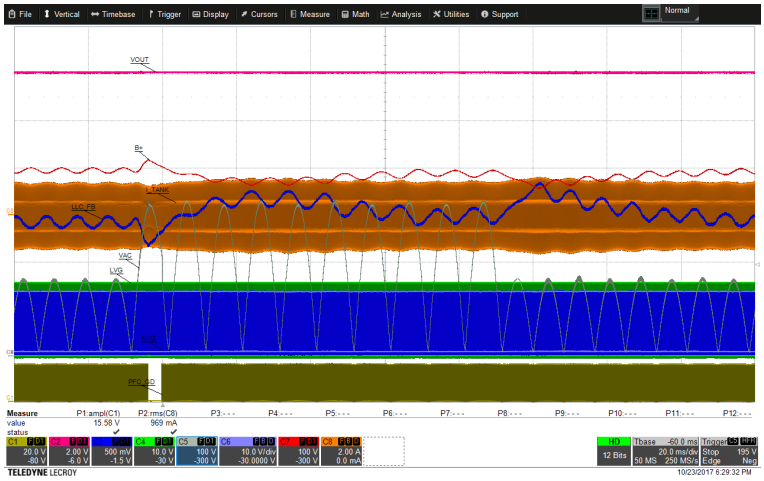
Figure 32. Waveforms during 10 ms mains dip

CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = VAC; CH6 = HVG; CH7 = B+; CH8 = I_TANK

2.9 Line transient

In case a line voltage transient is detected, the STNRG011 will immediately adapt the PFC MOSFET turn-on time. Figure 33 shows a line voltage transient from 115 Vac to 230 Vac and vice versa.

Figure 33. **Line transient from 115 Vac to 230 Vac and vice versa**



CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = VAC; CH6 = HVG; CH7 = B+; CH8 = I_TANK

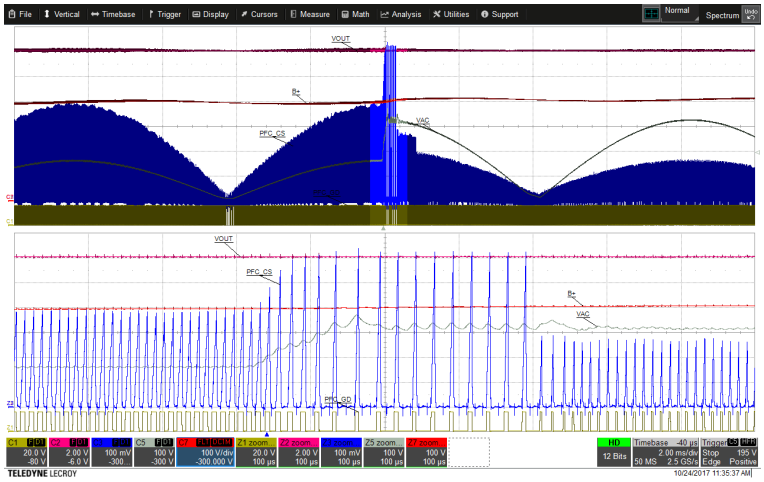
2.10 Faults managing

2.10.1 PFC OCP1

The PFC OCP1 sets the limit for the maximum allowed peak current into the PFC MOSFET.

The protection works cycle-by-cycle. If the PFC OC1 comparator threshold is hit, the PFC state machine turns-off the PFC gate drive for this cycle and the entire system continues to run. Figure 34 shows the behavior of the PFC during full load line transient from 90 Vac to 265 Vac at the peak of the line.

Figure 34. **PFC_CS hit PFC OC1 comparator**



CH1 = PFC_GD; CH2 = VOUT; CH3 = PFC_CS; CH5 = VAC; CH7 = B+

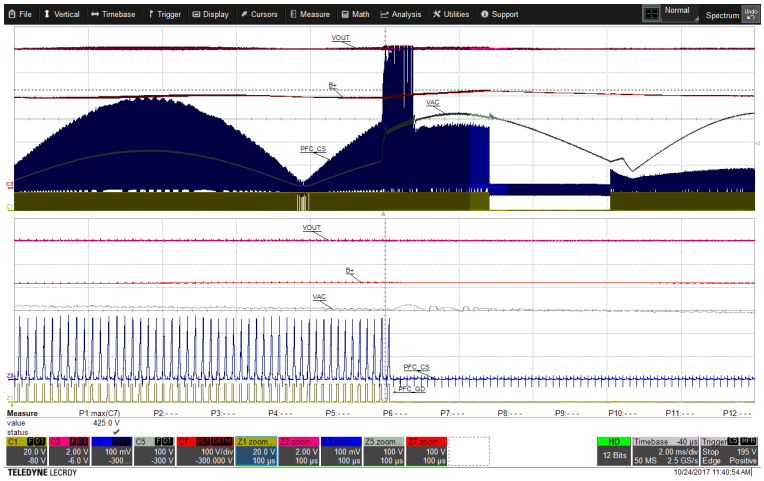
2.10.2 PFC OCP2

The PFC OCP2 fault is generated when the PFC OC2 comparator is triggered. The protection turns off the PFC MOSFET until the next mains half cycle for a maximum number of times defined by the “Max number of PFC OC2” parameter, beyond which the system shuts down. The counter is decreased every new line half cycle when the PFC OC2 comparator does not trigger any overcurrent for at least one line half cycle. The protection is usually triggered if the PFC coil saturates and the current is no longer controlled.

2.10.3 PFC SW OVP

The PFC SW OVP fault turns off the PFC MOSFET until the next mains half cycle if the bulk voltage exceeds the value defined by the “PFC SW OVP threshold (delta)” parameter. The fault never shuts down the system. Figure 35 shows the behavior of the converter when the PFC SW OVP is triggered during a line transient.

Figure 35. PFC_FB hit the software overvoltage protection



CH1 = PFC_GD; CH2 = VOUT; CH3 = PFC_CS; CH5 = VAC; CH7 = B+

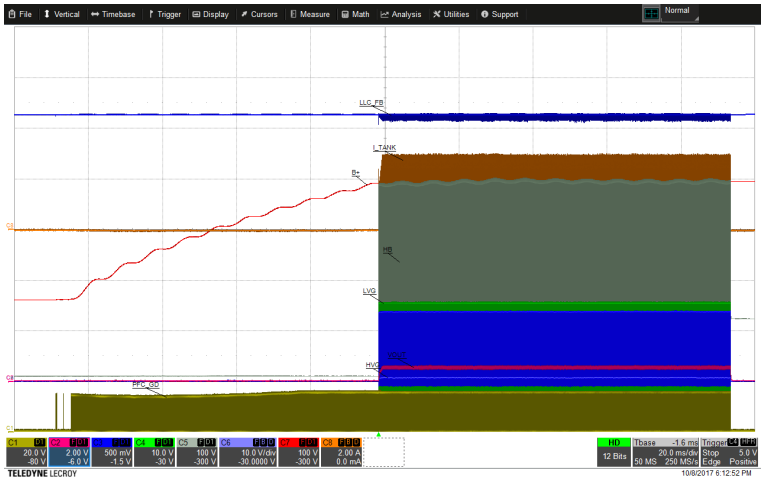
2.10.4 PFC HW OVP

The PFC HW OVP fault immediately shuts down the system as soon as the HW OVP threshold is reached. The PFC SW OVP is usually able to avoid the PFC HW OVP comparator shutting down the system.

2.10.5 LLC SS timeout

The LLC SS timeout fault is declared if the LLC is stuck in the soft-start state for at least 100 ms. This usually happens when the system starts with the output short-circuited and cannot reach the regulation, as shown in Figure 36.

Figure 36. **LLC SS timeout protection**

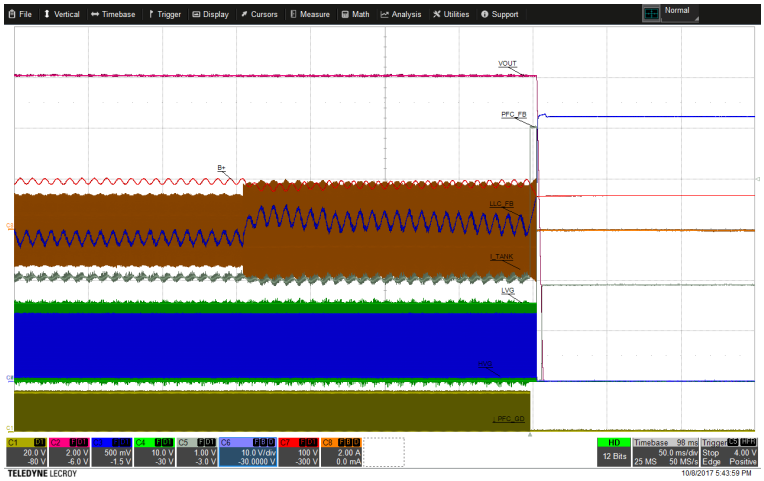


CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = HB; CH6 = HVG; CH7 = B+; CH8 = I_TANK

2.10.6 LLC OLP

The LLC OLP allows the system to source an output current higher than the nominal one, for a maximum allowed time defined by the “LLC OLP timeout” parameter. Figure 37 shows the behavior of the converter in case of a load transition from 12.5 A to 16 A.

Figure 37. **LLC overload protection**

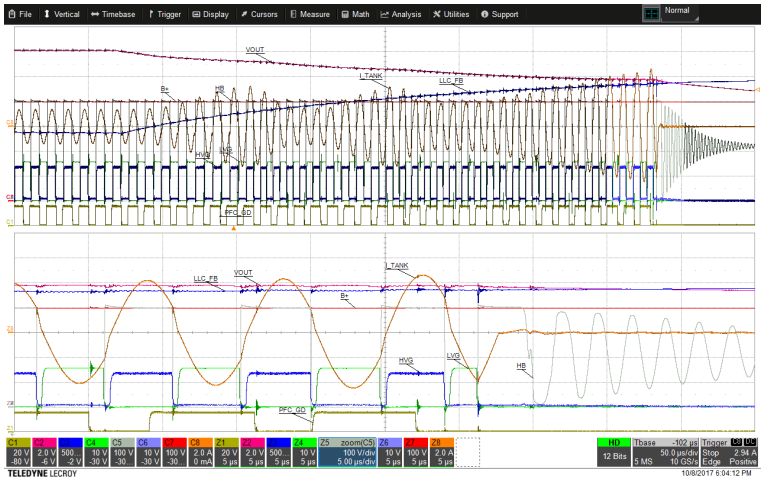


CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = HB; CH6 = HVG; CH7 = B+; CH8 = I_TANK

2.10.7 LLC OCP2

The LLC OCP2 fault is generated when the LLC OC2 comparator is triggered for a maximum number of time defined by the “Max number of LLC OC2” parameter. This could happen in case of a sudden output short-circuit, as shown in Figure 38. The soft ACP functionality also prevents the system from entering the capacitive region.

Figure 38. LLC_CS hit the LLC OC2 comparator during output short at full load



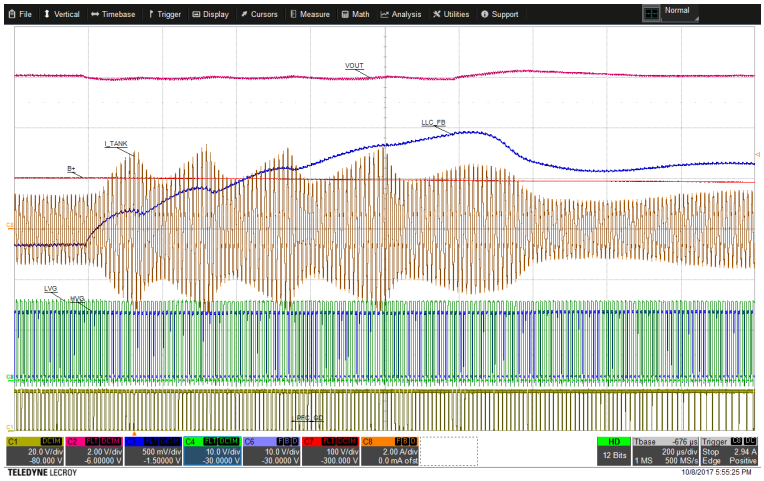
CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = HB; CH6 = HVG; CH7 = B+; CH8 = I_TANK

2.10.8 LLC ACP

The LLC ACP feature prevents the resonant converter from functioning in the capacitive region, losing the soft switching capability. The soft ACP feature intervenes in case the resonant tank is approaching the capacitive region, as shown in Figure 39 in case of a heavy load transient from 12.5 A to 22 A for 1 ms. The feature is immediately decrease the time shift value, in order to move aside the capacitive region.

The hard ACP feature intervenes in case the system reaches the capacitive mode, where the resonant tank current changes its sign during dead-time or during the half-bridge MOSFET turn-on instant. Usually the soft ACP feature avoids entering the capacitive region and loosing the ZVS operation, triggering the hard ACP.

Figure 39. LLC soft ACP intervention during heavy load transient

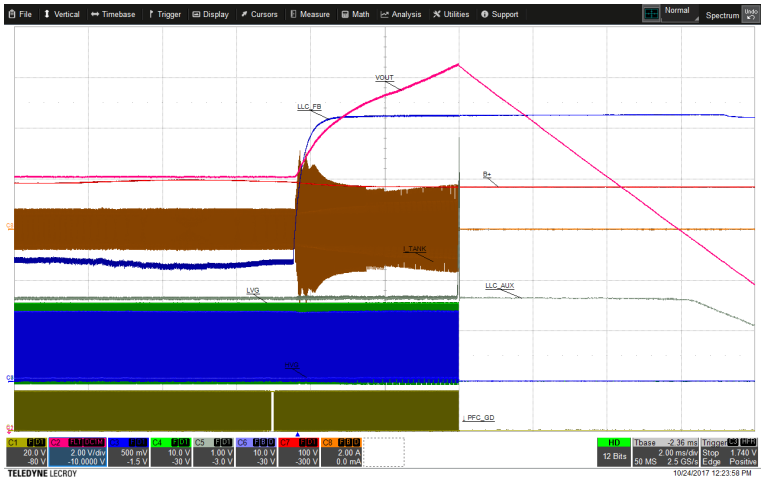


CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = HB; CH6 = HVG; CH7 = B+; CH8 = I_TANK

2.10.9 LLC OVP

The LLC OVP function is active on the LLC_AUX pin: if the voltage on the auxiliary winding of the LLC resonant transformer is sensed higher than the OVP threshold, the LLC_AUX pin is brought up to Vcore voltage and the LLC OVP fault is declared, as shown in Figure 40.

Figure 40. **LLC OVP simulation, shorting the diode section of the optocoupler**



CH1 = PFC_GD; CH2 = VOUT; CH3 = LLC_FB; CH4 = LVG; CH5 = HB; CH6 = HVG; CH7 = B+; CH8 = I_TANK

3 Performance verification

3.1 Efficiency

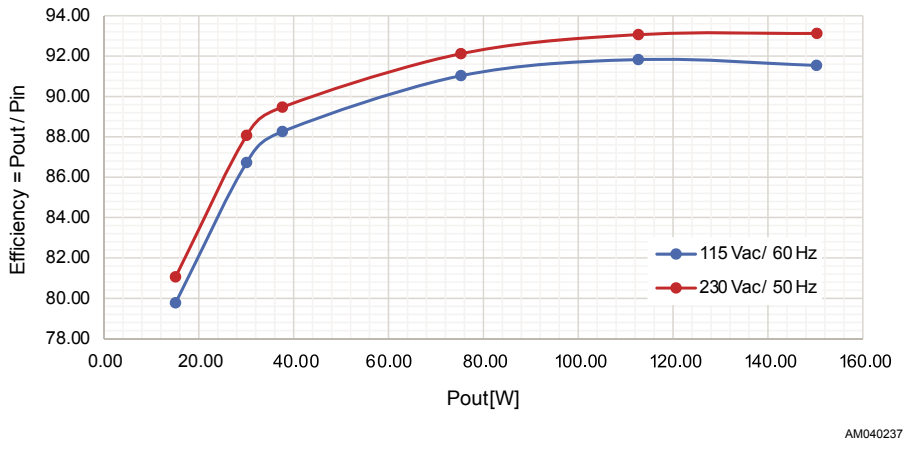
3.1.1 Overall

Table 3 and the Figure 41 show the overall efficiency of the EVLSTNRG011-150 demonstration board, measured at the nominal mains voltages, after a warm up time of about 30 minutes at the full load after which each measurement point has been kept for about 15 minutes, starting from heavy loads down to light loads. The active load has been set in the constant current mode with output voltage sensing. The output voltage and current have been read on the active load display, while the output power has been computed as Vout * Iout. The input power has been measured through a power meter with the voltage probe at the ac inlet of the converter.

Table 3. Overall efficiency

Output load	115 Vac/ 60 Hz					230 Vac/ 50 Hz				
	Vout [V]	Iout [A]	Pout [W]	Pin [W]	Ƞ [%]	Vout [V]	Iout [A]	Pout [W]	Pin [W]	Ƞ [%]
10%	12.042	1.254	15.10	18.93	**79.77**	12.042	1.254	15.10	18.63	**81.06**
20%	12.04	2.498	30.08	34.68	**86.72**	12.04	2.498	30.08	34.15	**88.07**
25%	12.039	3.126	37.63	42.64	**88.26**	12.038	3.126	37.63	42.06	**89.47**
50%	12.035	6.255	75.28	82.70	**91.03**	12.035	6.255	75.28	81.72	**92.12**
75%	12.027	9.369	112.68	122.71	**91.83**	12.031	9.369	112.72	121.12	**93.06**
100%	12.022	12.498	150.25	164.14	**91.54**	12.028	12.498	150.33	161.43	**93.12**
-	Average (100, 75, 50, 25 %) =				**90.66**	Average (100, 75, 50, 25 %) =				**91.94**

Figure 41. Overall efficiency vs. output load



3.1.2 Light load

The light load measurement procedure is described hereafter, while results are shown in Table 4 and Figure 42.

The board under test is supplied by the ac source and it is loaded by the active load set in the constant current mode with output voltage sensing. Input power and voltage are measured by a power meter while the output current and voltage are read through multimeters. Output power has been computed as Vout * Iout. At light loads, the current drawn by the board under test from the ac source is irregular and its measurement is typically unstable. To overcome this issue, the active energy consumption is measured by integration in mWh, and the corresponding input power is computed as energy divided by time. For the very light loads, i.e. from the open load to 500 mW, integration time has been 6 minutes, while for loads between 1 W and 10 W, the integration time has been 36 s.

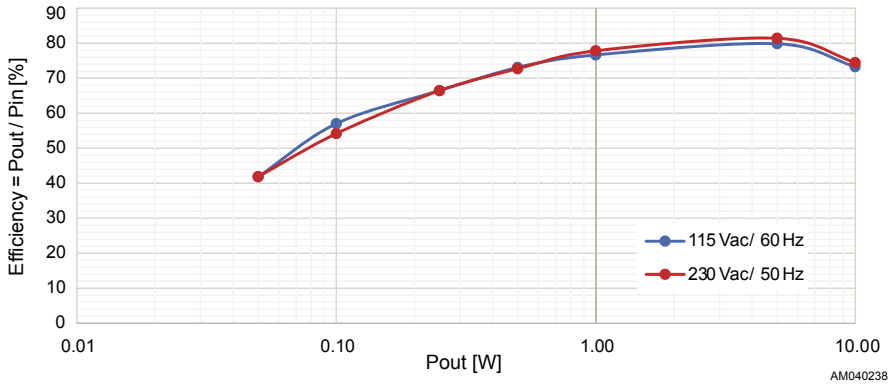
Each measurement point is kept for about 5 minutes, after which the values are taken.

Loads have been applied increasing the output power from minimum to maximum. For the no-load input power measurements, the only connection to the board was the input ac source.

Table 4. Light load efficiency

Output load	115 Vac / 60 Hz					230 V ac / 50 Hz				
	Vout [V]	Iout [mA]	Pout [W]	Pin [W]	η [%]	Vout [V]	Iout [mA]	Pout [W]	Pin [W]	η [%]
0 mW	12.042	-	-	0.051	-		-	-	0.063	-
50 mW	12.042	4.17	0.05	0.12	41.85	12.042	4.52	0.05	0.13	41.87
100 mW	12.039	9	0.11	0.19	57.03	12.04	9	0.11	0.20	54.18
250 mW	12.042	20.97	0.25	0.38	66.45	12.042	20.97	0.25	0.38	66.45
500 mW	12.037	41.89	0.50	0.69	73.08	12.037	41.67	0.50	0.69	72.69
1 W	12.036	83.43	1.00	1.31	76.65	12.035	83.43	1.00	1.29	77.84
5 W	12.035	416.7	5.01	6.28	79.86	12.035	416.7	5.01	6.16	81.41
10 W	12.044	833.6	10.04	13.70	73.28	12.044	833.6	10.04	13.48	74.48

Figure 42. Light load efficiency vs. output load



3.2 Eco design requirement

The most important eco design requirements are summarized in Table 5, Table 6, and Table 7.

Table 5. Energy star® requirements for computers ver. 6.1

ENERGY STAR ® for computers ver. 6.1	Test results		Limits	Status
	115 Vac / 60 Hz	230 Vac / 50 Hz		
Efficiency at 20% load	86.72%	88.07%	> 82%	PASS
Efficiency at 50% load	91.03%	92.12%	> 85%	
Efficiency at 100% load	91.54%	93.12%	> 82%	
Power factor at 100% load	0.995	0.982	> 0.9	

Table 6. EuP Lot 6 Tier 2 requirements for household and office equipment

EuP Lot 6 Tier 2	Test results		Limits	Status
	115 Vac / 60 Hz	230 Vac / 50 Hz		
Avg. efficiency measured at 25, 50, 75, 100%	90.66%	91.94%	> 87%	PASS
Efficiency at 250 mW load	66.45%	66.45%	> 50%	
Efficiency at 100 mW load	57.03%	54.18%	> 33%	

Table 7. European CoC ver. 5 Tier 2 requirements for external power supplies

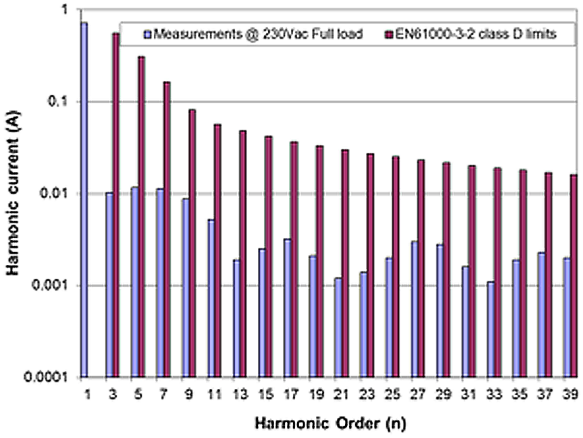
European CoC ver. 5 Tier-2 for ext. pow. sup.	Test results		Limits	Status
	115 Vac / 60 Hz	230 Vac / 50 Hz		
Avg. efficiency measured at 25, 50, 75, 100%	90.66%	91.94%	> 89%	PASS
Efficiency at 10% load	79.77%	81.06%	> 79%	
No-load input power [W]	0.051 W	0.063 W	< 0.15 W	

3.3 PFC

3.3.1 Harmonics contents measurements

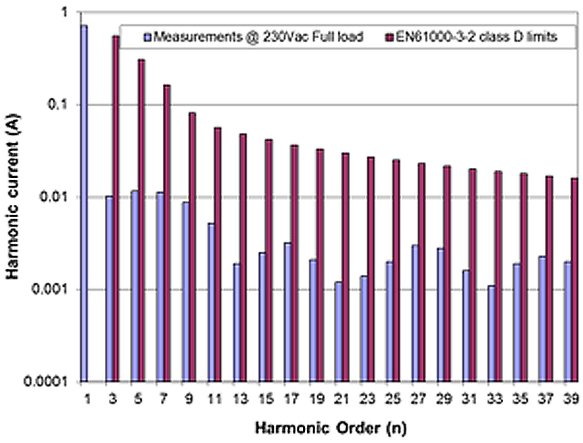
The board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI Class-D, at 230 Vac and 100 Vac / 50 Hz, both at the full load and at 75 W of input power. As reported from Figure 43 to Figure 46, the circuit is able to reduce the harmonics well below the limits of both regulations. The total harmonic distortion and power factor measurements are included below the charts. The values clearly indicate the correct functionality of the PFC in all conditions.

Figure 43. Compliance to EN61000-3-2 at 230 Vac / 50 Hz - full load



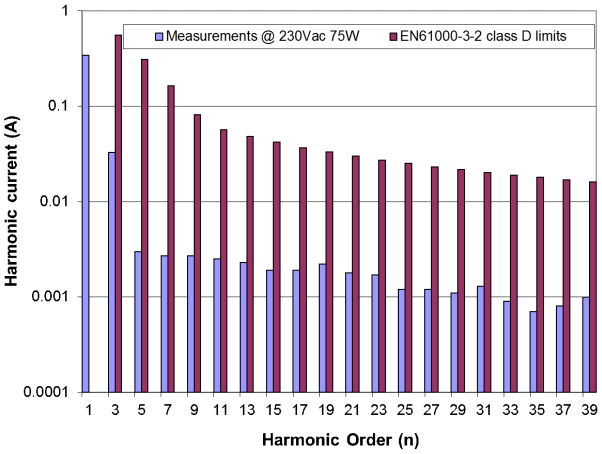
THD = 3.1% - PF = 0.9823

Figure 44. Compliance to JEITA-MITI at 100 Vac / 50 Hz - full load



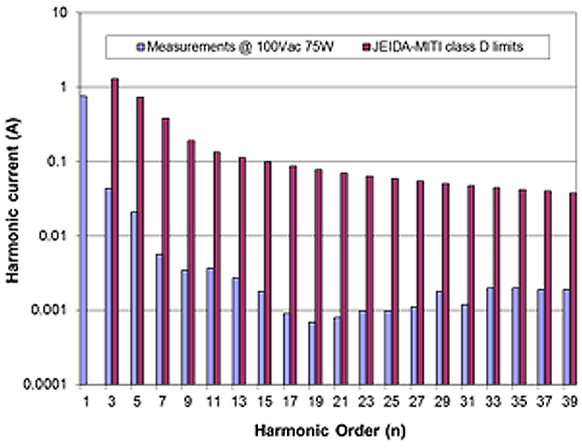
THD = 3.2% - PF = 0.9948

Figure 45. Compliance to EN61000-3-2 at 230 Vac / 50 Hz - input power 75 W



THD = 10.9% - PF = 0.9323

Figure 46. Compliance to JEITA-MITI at 100 Vac / 50 Hz - input power 75 W

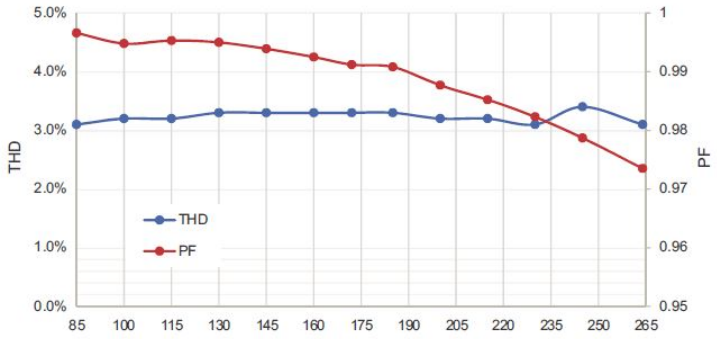


THD = 5% - PF = 0.9857

3.3.2 Total harmonic distortion and power factor

The THD and the PF have been measured at full load varying the input voltage from 90 Vac to 264 Vac. The line frequency has been set to 50 Hz. Figure 47 shows the performance of the converter.

Figure 47. **THD and PF at full load, varying input voltage**



The THD and the PF have been measured also varying the output power from half to full load, with a fixed input voltage. These are shown in Figure 48 and Figure 49 respectively.

Figure 48. **THD vs. output power**

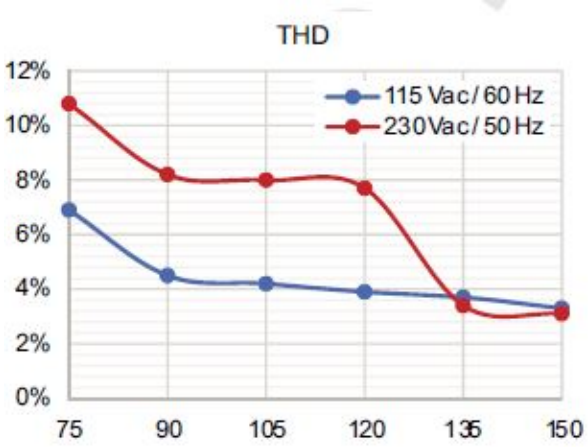
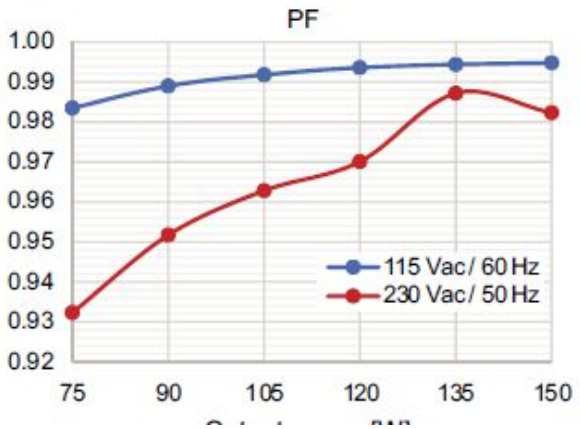


Figure 49. **PF v.s output power**



3.4 LLC

3.4.1 Output voltage regulation

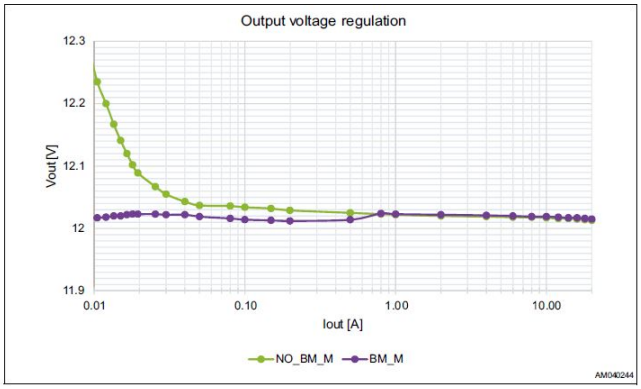
Figure 50 shows the output voltage as a function of the output current in case the burst mode is enabled (standard configuration) or in case it is disabled up to the no-load.

When the burst mode is disabled, at very low output current, (less than 30 mA), the output voltage is slightly above the set point (12 V nominal), and it increases up to 13.6 V when the load is disconnected.

On the other hand, when the burst mode is enabled, the regulation is maintained down to the no-load.

This behavior is due to the fact that the LLC resonant tank is not designed to work at the noload, and thus, even with the minimum time shift, there is still enough energy transfer to drive the output voltage above 12 V. Enabling the burst mode, instead, forces the system to stop and wait before restarting, until the output voltage goes below the regulation point. In this way the output voltage is always in range and the efficiency is increased. The only drawback is a higher output ripple. This strictly depends on two NVM parameters “LLC_FB burst entering thr” and “Minimum period to exit burst”, that allows the setting of the output current thresholds to enter / exit the burst mode, and thus also the output voltage ripple.

Figure 50. **Output voltage vs. output current**



3.4.2 Transient response

The transient response is shown from Figure 51 to Figure 58. Test results are not affected by the input voltage and then the ac input voltage information is not present. Also, the output current variation (dI/dt slope) is always in the order of 2.5 A/µs as indicated on the active

load menu.

Figure 51 and Figure 52 represent the most demanding situation of a load variation with the 20 ms period (10 ms / 10 ms), and the no-load to full load swing.

Figure 53 and Figure 54 show the same load variation, but with longer periods, 200 ms and 800 ms.

Figure 55 is representative of standby condition, where the load transition is between 0 A and 2.2 A.

Figure 56 shows a transition 0 A - 8.2 A with the 20 ms period (10 ms / 10 ms).

Figure 57 and Figure 58 are a representative of the active mode (0.2 A - 12.5 A).

Figure 51. **Iout = 0.0 A - 12.5 A, 10 ms / 10 ms**

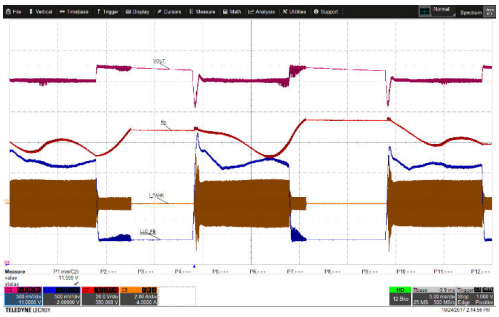


Figure 52. **Iout = 0.0 A - 12.5 A, 10 ms / 10 ms (zoom)**

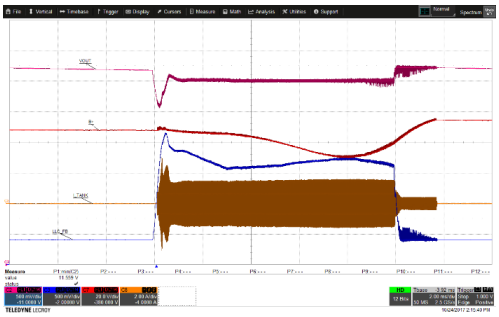


Figure 53. **Iout = 0.0 A - 12.5 A, 100 ms / 100 ms**

Figure 54. **Iout = 0.0 A - 12.5 A, 400 ms / 400 ms**

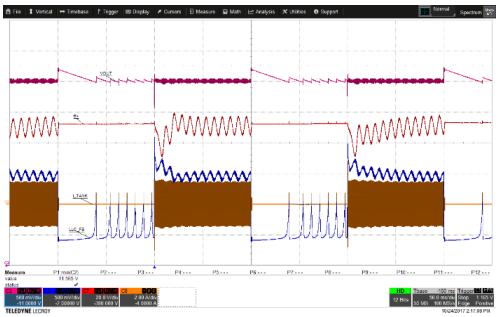


Figure 55. Iout = 0.0 A - 2.2 A, 10 ms / 10 ms

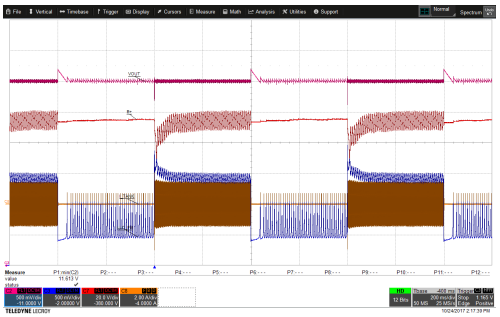


Figure 56. Iout = 0.2 A - 8.2 A, 10 ms / 10 ms

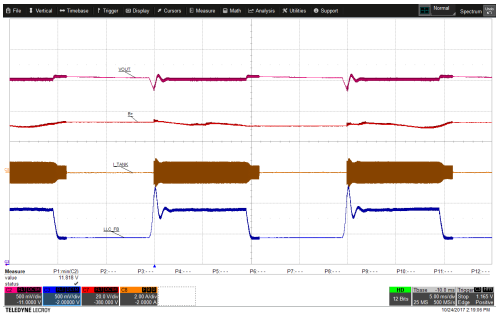


Figure 57. Iout = 0.2 A - 12.5 A, 10 ms / 10 ms

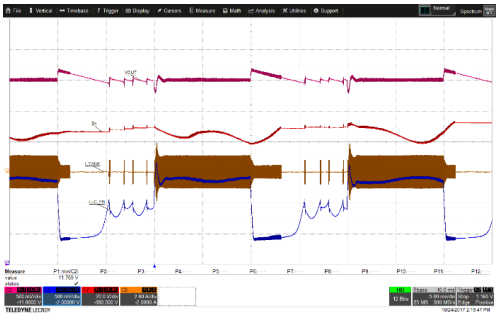
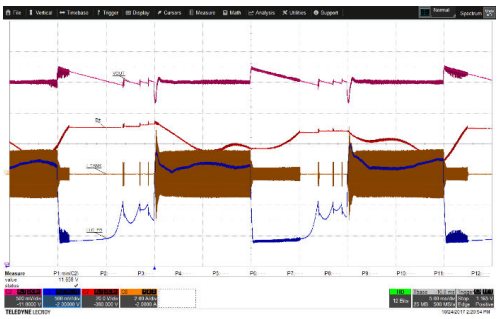
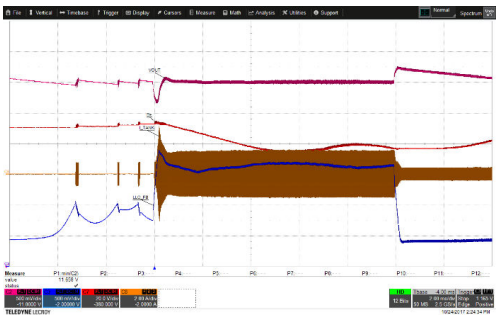


Figure 58. Iout = 0.2 A - 12.5 A, 10 ms / 10 ms (zoom)





3.4.3 Transfer functions

A network analyzer has been used to evaluate the stability of the SMPS and its design margins.

To simplify the measurement, the resistor R18 (100 Ω) on the feedback control board has been shorted, and the injected signal was applied between this point and the output connector.

The plant transfer function was measured with a probe connected to the LLC_FB pin (J1 pin 4) and the other to the output connector J3. It is shown in Figure 59.

The controller transfer function was measured with a probe connected to the R18 (shorted) and the other at the LLC_FB pin. It is shown in Figure 60.

The overall gain loop (Gloop) transfer function was measured with the probes connected at the injection points. The result is shown in Figure 61.

As can be seen, the phase margin is more than 60 degrees, and the loop gain at 100 Hz is about 36 dB, assuring good stability as well as the enough loop gain to reject the bulk voltage ripple.

Figure 59. **Plant transfer function at Iout = 12.5 A**

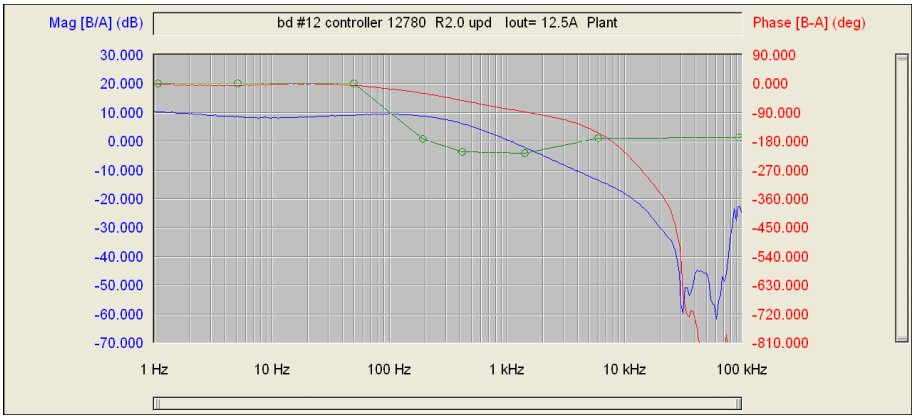


Figure 60. **Controller transfer function at Iout = 12.5 A**

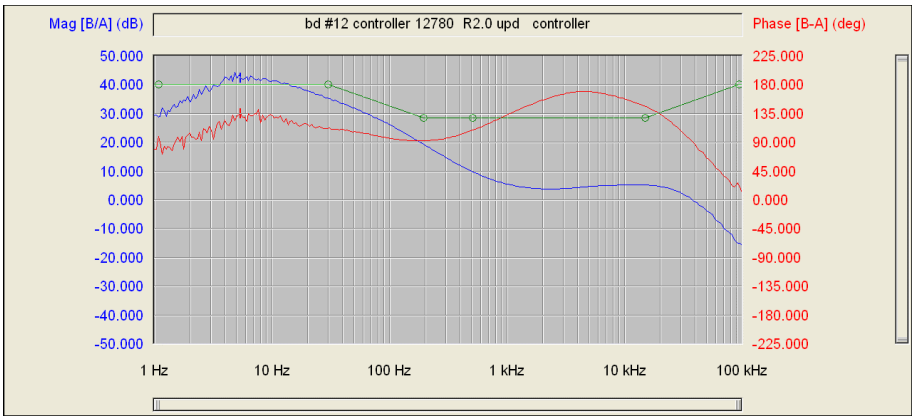
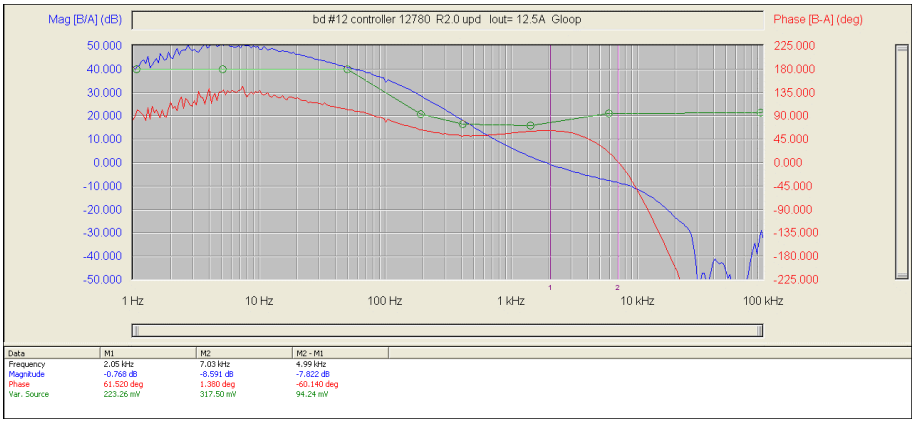


Figure 61. **Gloop transfer function at Iout = 12.5 A**



3.4.4 Output voltage ripple and noise

In order to measure the output ripple and noise, an oscilloscope has been used with the vertical channel setup with a dc offset of about 12 V and the bandwidth of 20 MHz. A 10X probe was connected directly to the output connector of the board, with two capacitors of 10 µF and 0.1 µF in parallel, placed just at the probe tip.

The line voltage was set to 115 Vac / 60 Hz, then the tests were repeated at 230 Vac / 50 Hz.

As no relevant differences appeared during the tests, only the first measurements are reported hereafter.

Table 8 summarizes the result of the measures of the output voltage corresponding to a load current of 12.5 A, 1.0 A, 0.4 A (out of burst mode), 0.4 A (in burst mode), 25 mA, and the noload.

The corresponding figures from Figure 62 to Figure 67 are also annexed. As can be seen, the ripple and noise values are well below the 120 mV peak-to-peak of the requirement.

Moreover two averaged acquisitions have been taken to evaluate only the output ripple at 2 * (F-line), while measuring the corresponding bulk voltage variations. These are shown in Figure 68 and Figure 69. In this way the CMRR of the resonant converter at 2 * (F-line) at a rated output current can be evaluated.

$$\mathrm{CMRR}|_{\mathrm{IOUT}} = 20 \cdot \mathrm{Log}\left(\frac{\Delta \mathrm{Vout}}{\Delta \mathrm{Vbulk}}\right)\Big|_{\mathrm{iout}} \quad (1)$$

$$\mathrm{CMRR}|_{12.5\,\mathrm{A}} = 20 \cdot \mathrm{Log}\left(\frac{10.42 \cdot 10^{-3}}{11.91}\right)\Big|_{12.5\,\mathrm{A}} = -61.2dB \quad (2)$$

$$\mathrm{CMRR}|_{1\,\mathrm{A}} = 20 \cdot \mathrm{Log}\left(\frac{1.716 \cdot 10^{-3}}{2.997}\right)\Big|_{1\mathrm{A}} = -64.8dB \quad (3)$$

Table 8. Vout ripple and noise

Iout	Vout (peak-to-peak)
12.5 A	53mV
1.0 A	25mV
0.4 A (not in BM)	23 mV
0.4 A (in BM)	80mV
0.025 A	76mV
0.0 A	45mV

Figure 62. Vout at Iout = 12.5 A

Figure 63. Vout at Iout = 1.0 A

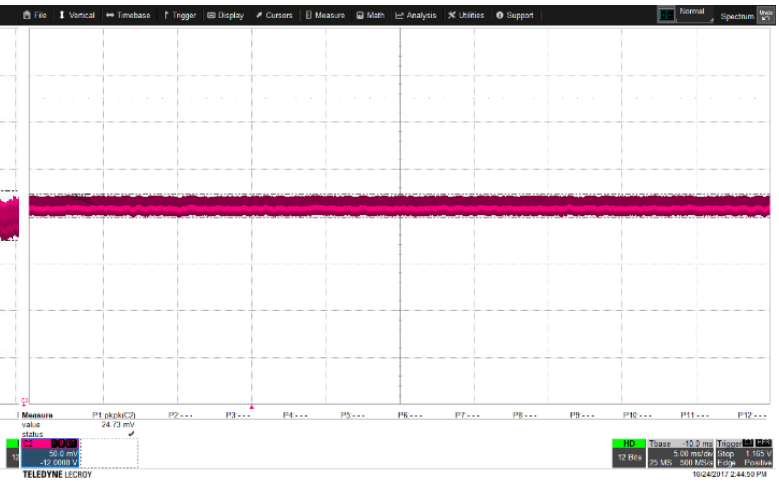


Figure 64. Vout at Iout = 0.4 A, not in burst mode

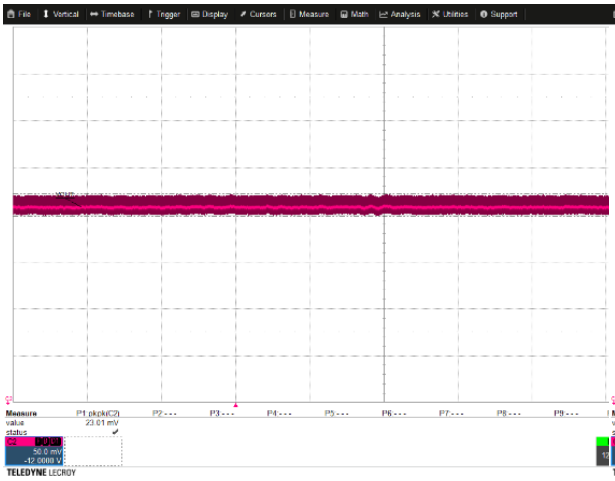


Figure 65. Vout at Iout = 0.4 A, in burst mode

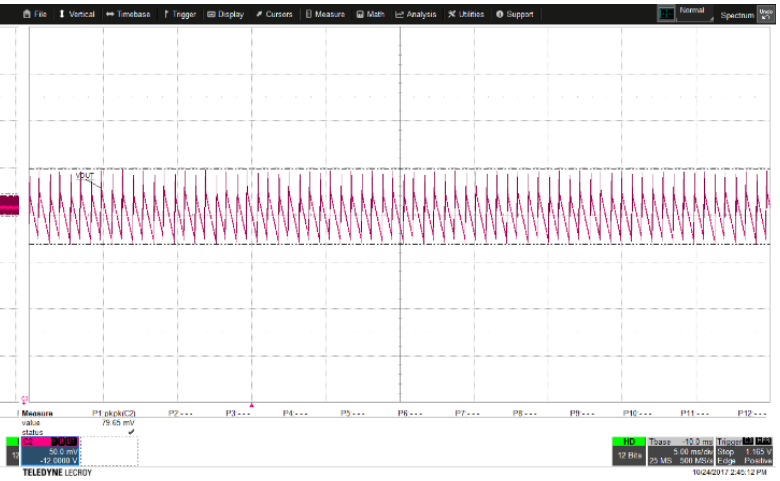


Figure 66. Vout at Iout = 0.025 A

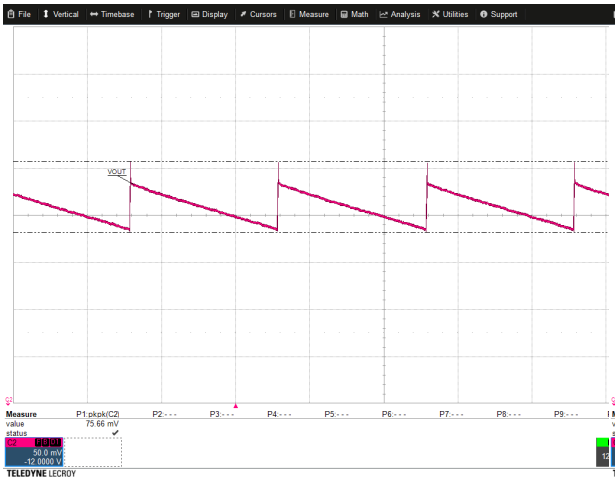


Figure 67. Vout at Iout = 0.0 A, no-load

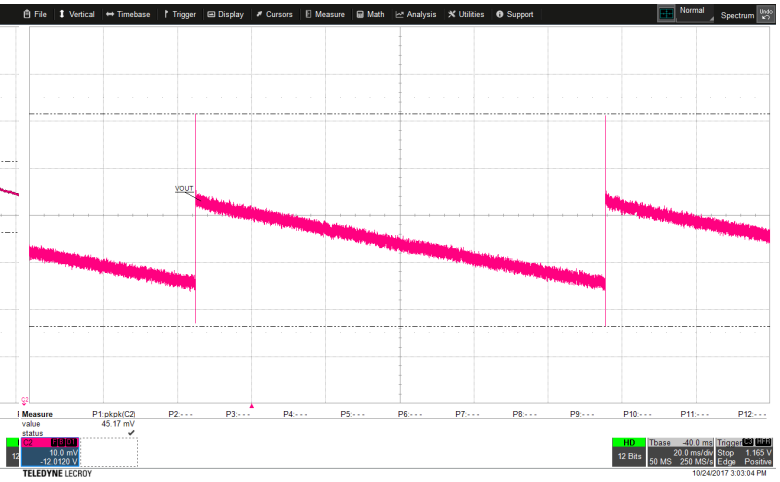


Figure 68. Vout at Iout = 12.5 A (averaged)

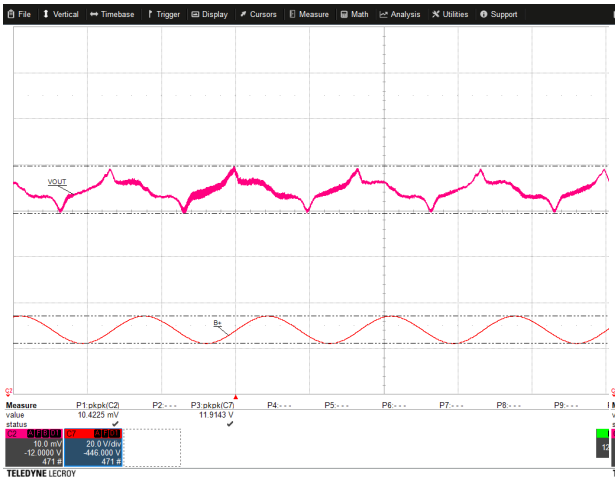


Figure 69. Vout at Iout = 1.0 A (averaged)

4 Thermal map

Thermal mapping with an IR camera was performed to verify the design reliability. Figure 70 and Figure 71 show the thermal measurements of the component side of the board at nominal input voltages. Key components or components showing higher temperatures are highlighted. The ambient temperature during measurement is 26 °C. Table 9 summarizes all the values.

Figure 70. Thermal map at 115 Vac / 60 Hz - full load

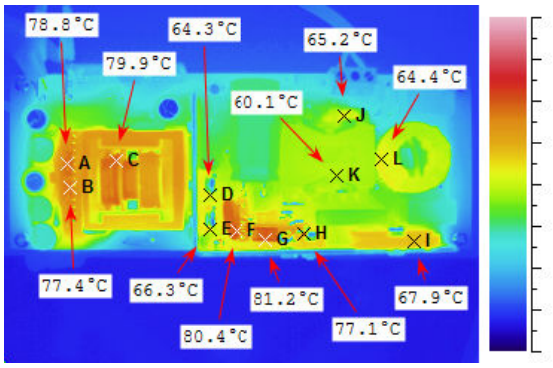


Figure 71. Thermal map at 230 Vac / 50 Hz - full load

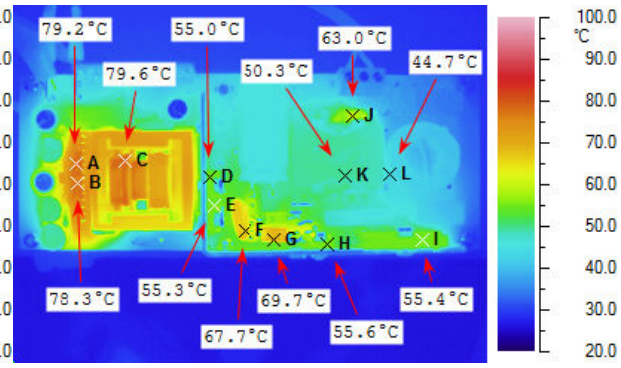


Table 9. Thermal maps reference points

Point	Reference	Description	Temp. at 115Vac / 60 Hz	Temp. at 230 Vac / 50 Hz
A	Q502	SR MOSFET	78.8 °C	79.2 °C
B	Q501	SR MOSFET	77.4 °C	78.3 °C
C	T1	Resonant power transformer	79.9 °C	79.6 °C
D	Q4	Resonant low side MOSFET	64.3 °C	55 °C
E	Q3	Resonant high side MOSFET	66.3 °C	55.3 °C
F	R4	Inrush limiting NTC resistor	80.4 °C	67.7 °C
G	D3	PFC output diode	81.2 °C	69.7 °C
H	Q1	PFC MOSFET	77.1 °C	55.6 °C
I	D2	Bridge rectifier	67.9 °C	55.4 °C
J	R9	Charge pump limiting resistor	65.2 °C	63 °C
K	L2	PFC inductor	60.1 °C	50.3 °C
L	L1	EMI filtering inductor	64.4 °C	44.7 °C

5 Conducted emission pre-compliance test

Figure 72 and Figure 73 are the average measurements of the conducted emission noise at full load and nominal mains voltages. The limits shown in the diagrams are the EN55022 Class-B, which is the most popular standard for domestic equipment and has more severe limits compared to the Class-A, dedicated to IT technology equipment. The EN55022 Class- B limit relevant to average measurements is indicated in red on the diagrams. In all test conditions the measurements are significantly below the limits.

Figure 72. CE average measurement at 115 V - 60 Hz and full load - phase wire

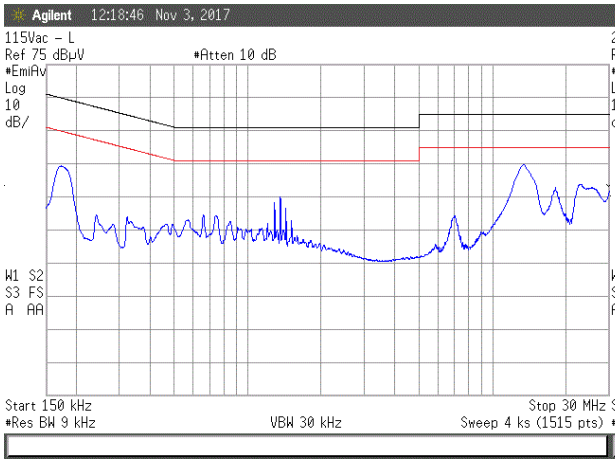
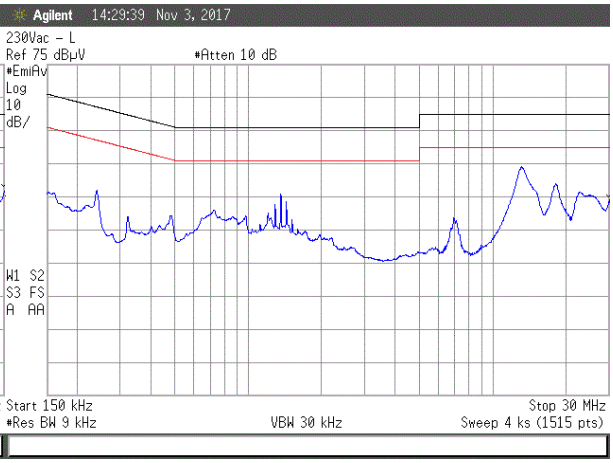


Figure 73. CE average measurement at 230 V - 50 Hz and full load - phase wire



6 Appendix A - NVM parameters configuration

Table 10. NVM parameters configuration

Item	Name	Value
0	Shutdown feature	0 = disabled
1	Patch upload from EEPROM	1 = enabled
2	ATE mode	0 = enabled
3	System monitoring	0 = enabled
4	VAC reading improvement	1 = enabled
5	Early warning feature	0 = enabled
6	EW signal in burst mode	1 = normal
7	Non latched faults timer	3 = 4.37 s
8	Surge detection	1 = enabled
9	PFC OC2 detection	1 = enabled
10	Max. number ofPFC OC2	4
11	PFC HW OVP detection	1 = enabled
12	LLC OC2 detection	1 = enabled
13	Max. number of LLC OC2	4
14	LLC OVP detection	1 = enabled
15	Disconnection faults detection	1 = enabled
16	PFC OC2 behavior	1 = latched
17	PFC HW OVP behavior	1 = latched
18	PFC UVP behavior	1 = adaptive
19	LLC SS timeout behavior	1 = latched
20	LLC ACP behavior	0 = not latched
21	LLC OC2 behavior	1 = latched
22	LLC OLP behavior	0 = not latched
23	LLC OVP behavior	1 = latched
24	PFC Ki	8
25	PFC Kp	32
26	PFC boost exiting burst	1 = enabled
27	PFC MOSFET LEB	16 = 267 ns
28	PFC THD improver base	5 = 10 mV
29	PFC THD improver gain	0 = gain disabled
30	PFC maximum power	9216
31	PFC pss	2560
32	PFC pcc	10238
33	PFC min. pin Vskip	2176
34	PFC max. pin Vskip (delta)	2560
35	PFC Delta pin Vskip	352
36	PFC maximum DCM power	3072
37	PFC min .Tsw Vskip	448 = 134 kHz

Item	Name	Value
38	PFC max. Tsw Vskip	608 = 87 kHz
39	Skipping area threshold	1536
40	PFC Vout target	80 = 2.063 V - 400 V
41	PFC Vout SS end (delta)	8 = 19.5 mV - 3.8 V
42	PFC UVP threshold (delta)	32 = 0.234 V - 45 V
43	PFC SW OVP threshold (delta)	2= 105 mV - 20 V
44	LLC low frequency range	1 = disabled
45	LLC HVG first Ton	24 = 400 ns
46	LLC LVG first TS	30 = 400 ns (566.7 ns)
47	LLC dead time	24 = 400 ns
48	LLC soft-start speed	2 = 16.7ns(33.3ns)
49	Minimum time shift	60 = 625 ns (1250 ns)
50	Maximum time shift	480 = 7.96 µs (15.92 µs)
51	LLC OLP threshold	19 = 309.55 mV
52	LLC OLP timeout	1 = 200 ms
53	ACP sensitivity	1 = high
54	Hard ACP detection	1 = enabled
55	Soft ACP feature	0 = enabled
56	Soft ACP entering threshold	14 = 233 ns (467 ns)
57	Soft ACP TS decrement	5 = 400ns (800 ns)
58	Maximum soft ACP occurrences	1 = 16
59	External burst mode	0 = disabled
60	BM enter for minimum TS	1 = enabled
61	Burst entering digital filtering	24 = 990 µs
62	LLC_FB burst entering thr (1)	294 = 717.8 mV - 1883 ns (3767 ns)
63	LLC_FB burst wake-up thr	1 = 1.0 V - 2.85 µs (5.7 µs)
64	LLC_FB burst wake-up hyst	1 = 10 mV
65	Min TS in burst mode	19 = 3.53 µs (6.73 µs)
66	Min. number ofburst pulses	4
67	Max. number ofburst pulses (delta)	2
68	Min. time between burst seq	128 = 10.2 ms
69	Max. time between burst seq (delta)	64 = 4.97 ms
70	Minimum period to exit burst (1)	9 = 367 µs
71	No-burst window width	1 = 7.5 ms
72	Surge comp digital filtering	30 = 500 ns
73	PFC CS comp digital filtering	3 = 50 ns
74	PFC CS comp hysteresis	0 = 5 mV
75	PFC OC2 comp digital filtering	24 = 400 ns
76	PFC OC1 comp digital filtering (delta)	2 = 33.3 ns
77	PFC ZCD comp digital filtering	2 = 33.3 ns
78	PFC ZCD comp falling thr	0 = 0 mV

Item	Name	Value
79	PFC ZCD comp rising thr	1 = 110 mV (N/Awith TH_F[3] = 200mV)
80	PFC HW OVP comp digital filtering	255 = 4.25 µs
81	LLC OLP comp digital filtering	1= 16.7ns
82	LLC OC2 comp digital filtering	14 = 233.3 ns
83	LLC ZCD comp digital filtering	15 = 250 ns
84	LLC ZCD comp hysteresis	1 = 10 mV
85	LLC OVP comp digital filtering	255 = 4.25 µs

1. *Both parameters for input and exit burst could be different board by board in order to allow the designer to compensate the component tolerance respecting the burst requirements*

7 Appendix B - Bill of materials

Table 11. **EVLSTNRG011-150 mother board bill of materials**

Reference	Part number /part value	Description	Supplier	Case
C1, C5, C7, C10	2.2 NF	Ceramic Y1 capacitor - 250 Vac	Murata	p. 10 mm
C2, C6, C23	100 nF	SMD ceramic capacitor X7R	AVX	0805
C3, C4	470 nF	Polypropylene X2 capacitor -275 Vac	EPCOS	9.0 x18.0, p. 15 mm
C8	470 nF	Polypropylene film cap. -630 Vdc	EPCOS	Plastic radial
C9	100 µF	Electrolytic capacitor TXW -450 V	Rubycon	Dia. 18 x 32 mm
C11	10 nF	SMD ceramic capacitor X7R - 100 V	AVX	1206
C12	2.2 µF	SMD ceramic capacitor X7R	AVX	1206
C13	10 µF	Electrolytic capacitor YXF	Rubycon	Dia. 5.0 x11 mm, p. 2mm
C14	180 µF	Electrolytic capacitor ZLH -63 V	Rubycon	Dia.10 x20 mm, p. 5mm
C15	N. M.	SMD ceramic capacitor		1206
C16	100 nF	SMD ceramic capacitor X7R	AVX	1206
C17	1 µF	SMD ceramic capacitor X7R	AVX	1206
C18, C19, C21	470 µF	Aluminium polymer capacitor	Panasonic	Dia. 10x 13 mm, p. 5mm
C20, C22	2.2 mF	Elect. cap.	RUBYCON	Radial
C24	1 µF	SMD ceramic capacitor X7R	AVX	0805
C25	330 pF	Ceramic capacitor - 1 kV	MURATA	1206
C26	22 nF	Film capacitor -1 kV	EPCOS /TDK	CKR05
C27	N. M.	SMD ceramic capacitor X7R	AVX	0805
C28	1nF	SMD ceramic capacitor X7R	AVX	0805
C29	2.2 nF	SMD ceramic capacitor X7R	AVX	0805
C30	150 pF	SMD ceramic capacitor X7R	AVX	0805
C31	220 pF	SMD ceramic capacitor X7R	AVX	0805
C32	100 pF	SMD ceramic capacitor X7R	AVX	0805
C33 on R53	27 pF	SMD ceramic capacitor X7R	AVX	0805
C34 on R56	220 pF	SMD ceramic capacitor X7R	AVX	0805
D1	1N5406	General purpose rectifier	Vishay	DO201
D2	D15XB60H	Bridge rectifier	Shindengen	5S
D3	STTH5L06	Ultrafast diode	STMicroelectronics	DO201
D4, D5	S1J	Diode	Vishay	DO214AC-SMA
D6, D7, D8, D13, D14	1N4148W	SMD diode	Vishay	SOD123
D9, D10	BAV23S	Switching rectifier	Diodes Inc.	SOT23
D11	BZT52C16	SMD Zener diode	Diodes Inc.	SOD123
D12	STTH1R06A	Ultrafast rectifier	STMicroelectronics	DO214AC-SMA

Reference	Part number /part value	Description	Supplier	Case
D15	BAT48J	SMD Schottky diode SOD-323	STMicroelectronics	SOD323
D16	1N4148W-7-F	Fast switching rectifier	Diodes Inc.	SOD123
F1	T 4A	PCB fuse 4A time lag	Littelfuse	TE5
HS1	Heatsink	Heatsink FOR D2, Q1, Q3, Q4	-	DWG
JPX1, JPX2	Shorted	Wire jumper	-	DWG
JP1	STRIP1X36PF	Female header 13-pin	-	p. 2.54 mm
JP2	STRIP1X36PF	Female header 15-pin -pin 6, 7, 8 removed	-	p. 2.54 mm
J1	MKDS 1,5/ 3- 5,08	AC socket	Phoenix contact	3P - p. 5 mm
J2	MOLEX 90325-0006	Molex PicoFlex connector 6P1,27 mm pitch	MOLEX	1.27 mm pitch
J3	FASTBFH/A1/ 6,3	Faston .250 TAB PCB	KEYSTONE	DWG
J4	FASTBFH/A1/ 6,3	Faston .250 TAB PCB	KEYSTONE	DWG
L1	2 x 28 mH	Input EMI filter	Magnetica	DWG
L2	240 µH, 2.65 A	PFC inductor -add Kapton to isolate inductor from PCB	Magnetica	DWG
Q1	STF24N60M2	Power MOSFET	STMicroelectronics	TO220-FP
Q2,Q5, Q6	MMBT2222A	SMD NPN transistor		SOT23
Q3, Q4	STF13N60M2	Power MOSFET	STMicroelectronics	TO220-FP
Q7	BC857C	Trans. PNP general purpose	NXP	SOT23
RV1	S14K300	Metal oxide varistor	EPCOS	Dia.15 x 5 mm, p.7.5mm
R1, R2, R3, R5, R6, R7, R11, R16	0R0	SMD resistor	Vishay	0805
R4	NTC 2R5- S237	NTC resistor S237	EPCOS	DWG
R8, R49	1.5 KΩ	SMD resistor	Vishay	0805
R9	100 Ω	SMD resistor 1/2 W	Vishay	1206
R10, R13, R14	3 MΩ	SMD resistor	Vishay	1206
R12	47 Ω	SMD resistor	Vishay	0805
R15, R24	N.M.	SMD resistor	Vishay	0805
R17	0 Ω	SMD resistor	TTI	0805
R18, R32, R36	10 Ω	SMD resistor	Vishay	0805
R19	1Ω	SMD resistor	Vishay	1206
R20, R31, R61	10 Ω	SMD resistor	Vishay	1206
R21, R62	22 V	SMD resistor	Vishay	0805
R22, R34, R38, R50, R51	100 KΩ	SMD resistor	MultiComp	0805
R23	1 KΩ	SMD resistor	Vishay	0805
R25	470 Ω	SMD resistor	Vishay	0805
R26, R27	0.18 Ω	SMD resistor	YAGEO (PHYCOMP)	2512
R28, R42	56 KΩ	SMD resistor	MultiComp	0805
R29	330 KΩ	SMD resistor	MultiComp	0805
R30, R55	22 KΩ	SMD resistor	Vishay	0805
R33, R37	56 Ω	SMD resistor	Vishay	0805

Reference	Part number /part value	Description	Supplier	Case
R35	0.002 Ω	SMD resistor	YAGEO	2512
R39	220 Ω	SMD resistor	Vishay	1206
R40	15 Ω	SMD resistor	Vishay	0805
R41	12 Ω	SMD resistor	MultiComp	0805
R44	62 KΩ	SMD resistor	MultiComp	0805
R45	5.1 KΩ	SMD resistor	MultiComp	0805
R46, R47	330 KΩ	SMD resistor	-	1206
R48	N. M.	SMD resistor	Vishay	0805
R52	15 KΩ	SMD resistor	MultiComp	0805
R53, R54, R60	220 KΩ	SMD resistor	Multicomp	0805
R56	47 KΩ	SMD resistor	MultiComp	0805
R57, R58, R59	750 KΩ	SMD resistor	MultiComp	0805
TP1, TP2, TP3	Test point	Testpoint	-	-
T1	1860.0164	LLC transformer	Magnetica	ETD34
U1	M24C32	32-Kbit I²C 1MHz EEPROM	STMicroelectronics	SO8
U2	STNRG011	Digital combo controller	STMicroelectronics	SO20

Table 12. EVLSTNRG011-150 feedback (control) board bill of materials

Reference	Part number /part value	Description	Supplier	Case
C1, C6	100 nF	SMD ceramic capacitor X7R	SCI	0603
C2	47 pF	SMD ceramic capacitor C0G/NP0	SCI	0603
C3, C10	270 pF	SMD ceramic capacitor X7R	SCI	0603
C4, C15	1nF	SMD ceramic capacitor X7R	SCI	0603
C5	22 nF	SMD ceramic capacitor X7R	SCI	0603
C7, C11, C13	N. M.	SMD ceramic capacitor	-	0805
C8	390 pF	SMD ceramic capacitor C0G/NP0	SCI	0603
C9	5.6 nF	SMD ceramic capacitor C0G/NP0	SCI	0805
C12	100 pF	SMD ceramic capacitor C0G/NP0	SCI	0603
C14	N. M.	SMD ceramic capacitor	SCI	0603
D1, D3	MMSD4148T1G	Switching rectifier	SCI	SOD123
D2	BAT43WS	Schottkyrectifier	SCI	SOD323
ISO1, ISO2	SFH617A-2	Optocoupler	Vishay	DIP4
J1	Male header 15 R/A	Strip male 15-pin, 90° -pin 6, 7, 8, 9, 10 removed	SCI	p. 2.54 mm
Q1	BC857C	Trans. PNP general purpose	SCI	SOT23
R1	27 KΩ	SMD resistor	SCI	0805
R2	1 KΩ	SMD resistor	SCI	0805
R3, R18	100 Ω	SMD resistor	SCI	0603
R4, R7	10 KΩ	SMD resistor	SCI	0603
R5	43 KΩ	SMD resistor	-	0603
R6	2.7 KΩ	SMD resistor	SCI	0805

Reference	Part number /part value	Description	Supplier	Case
R8, R14	47 KΩ	SMD resistor	SCI	0603
R9, R19, R25, R26	N. M.	SMD resistor	-	0805
R10	33 KΩ	SMD resistor	SCI	0805
R11	510 KΩ	SMD resistor	SCI	0805
R12	N. M.	SMD resistor	-	0603
R13	2 KΩ	SMD resistor	SCI	0603
R15, R16, R21	10 Ω	SMD resistor	SCI	0603
R17	8.2 KΩ	SMD resistor	SCI	0603
R20	24 KΩ	SMD resistor	SCI	0805
R22	91 KΩ	SMD resistor	SCI	0603
R23	5.1 KΩ	SMD resistor	SCI	0603
R24, R28	150 KΩ	SMD resistor	SCI	0603
R27	180 KΩ	SMD resistor	SCI	0805
R29	33 KΩ	SMD resistor	SCI	0603
R30	0 Ω	SMD resistor	SCI	0603
R31	N. M.	SMD resistor	-	0603
R32	1 KΩ	SMD resistor	SCI	0603
R34	1 MΩ	SMD resistor	SCI	0603
R35	27 Ω	SMD resistor	SCI	0603
U1	TSC101_C	High side current sense amplifier	STMicroelectronics	SOT23-5
U2	TSM1014A	Voltage and current controller	STMicroelectronics	SO8
U3	TS432AILT	Vol. reg.	STMicroelectronics	SOT23
U4	BCM61B	Bipolar rectifier	SCI	SOT143-B

Table 13. EVLSTNRG011-150 synchronous rectifier (SRK) board bill of materials

Reference	Part number /part value	Description	Supplier	Case
C501	1 µF	SMD ceramic capacitor X7R	SCI	0805
C502	N. M.	SMD ceramic capacitor X7R	-	0805
C503, C504	N. M.	SMD ceramic capacitor X7R	-	0805
D501, D502	N. M.	SMD Transilä	-	0805
JP501	STRIP36PMDD90	Strip male 13-pin, 90°	SCI	p. 2.54 mm
Q501, Q502	STL140N6F7	Power MOSFET	STMicroelectronics	PoweFLAT 5 x6
Q503	N. M.	SMD NPN transistor	-	SOT-23
Q504, Q505	N. M.	Power MOSFET	-	PoweFLAT 5 x6
R501, R506, R507	0 Ω	SMD resistor	SCI	0805
R504, R505	100 Ω	SMD resistor	SCI	0805
R508, R509	N. M.	SMD resistor	-	0805
R502	N. M.	SMD resistor	-	0805
R503	N. M.	SMD resistor	-	0805
R510, R511, R512, R513	N. M.	SMD resistor	-	0805
U501	SRK2001	SR controller	STMicroelectronics	SSOP10

8 Appendix C - Magnetics specifications

8.1 PFC coil specifications

General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Coil former: vertical type, 6 + 6 pins
- Max. temp. rise: 45 ºC
- Max. operating ambient temperature: 60 ºC
- Mains insulation: N. A.
- Unit finishing: varnished

Electrical characteristics

- Converter topology: boost, transition mode
- Core type: PQ32/20-PC44 or equivalent
- Min. operating frequency: 30 kHz
- Typical operating frequency: 120 kHz
- Primary inductance: 240 µH ± 15% at 1 kHz - 0.25 V

Electrical diagram and winding characteristics

Figure 74. **Electrical diagram and winding characteristics**

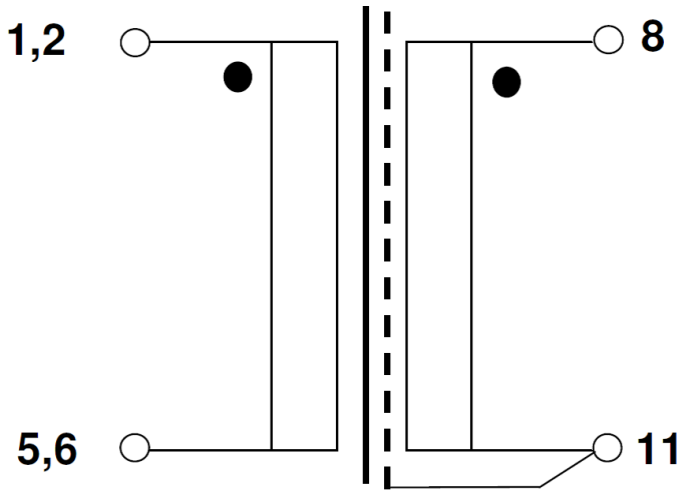


Table 14. **PFC coil winding data**

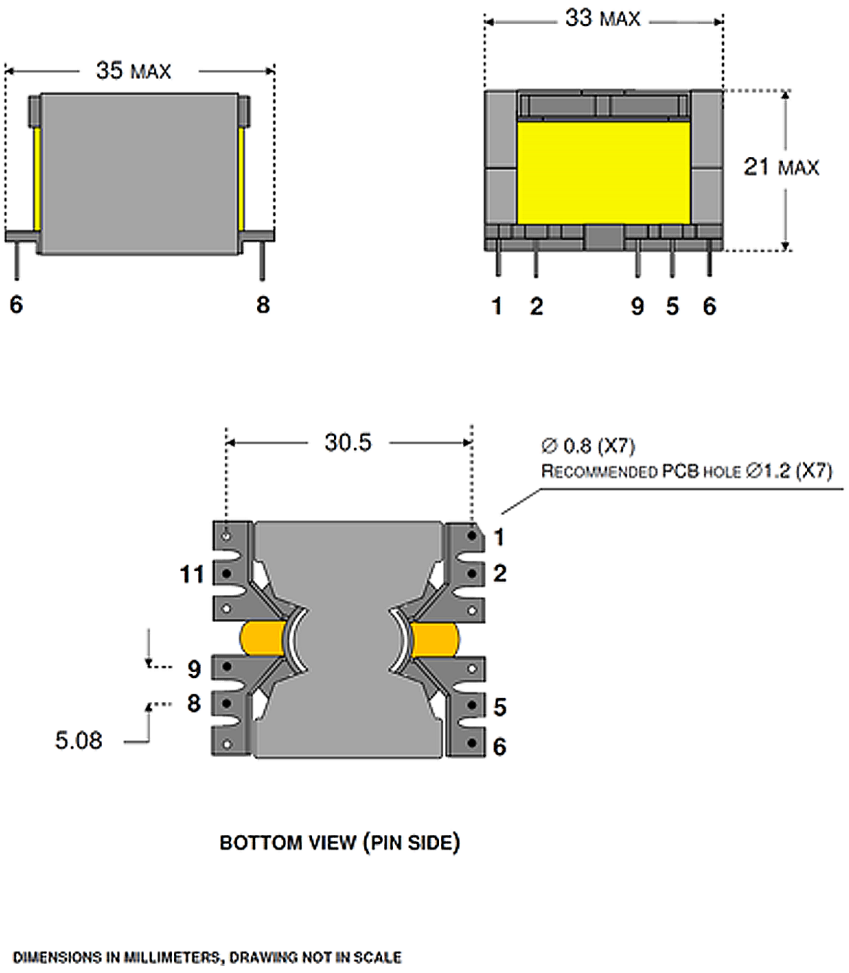
Pins	Windings	RMS current	Number of turns	Wire type
8 - 11	AUX	0.05 A_{RMS}	3 spaced	0.3 mm - G2
1, 2 - 5, 6	PRIMARY	2.65 A_{RMS}	28	2 x 40 x 0.1 mm - G2

Mechanical aspect and pin numbering

- Maximum height from PCB: 22 mm
- Coil former type: vertical, 6 + 6 pins (pins #3, 4, 7, 12 are removed)

- Pin distance: 5.08 mm
- Row distance: 30.5 mm
- External copper shield: not insulated, wound around the ferrite core and including the coil former. The height is 8 mm. Connected to the pin #11 by a soldered solid wire.

Figure 75. PFC coil mechanical aspect



Manufacturer

- AQ Magnetica - Italy
- Inductor P/N: 2086.0001

8.2 Resonant power transformer specification

General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Coil former: horizontal type, 7 + 7 pins, two slots
- Max. temp. rise: 45 ºC
- Max. operating ambient temperature: 60 ºC
- Mains insulation: acc. to EN60065

Electrical characteristics

- Converter topology: half bridge, resonant

- Core type: ETD34-PC44 or equivalent
- Min. operating frequency: 60 kHz
- Typical operating frequency: 100 kHz
- Primary inductance: 910 □H ± 10% at 1 kHz - 0.25 V
- (Measured between pins 2 - 4)
- Leakage inductance: 110 µH ± 10% at 100 kHz - 0.25 V
- (Measured between pins 2 - 4 with only half secondary winding shorted at a time)

Electrical diagram and winding characteristics

Figure 76. Transformer electrical diagram

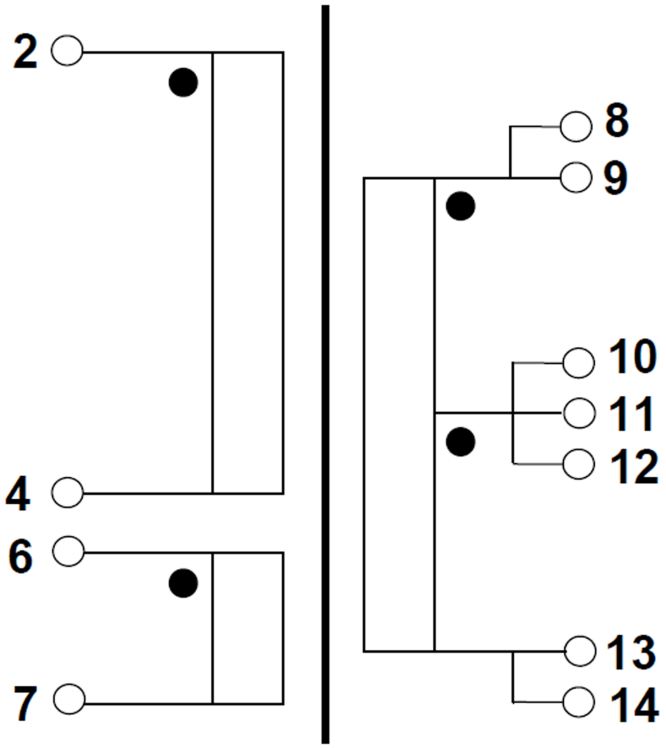


Table 15. Transformer winding data

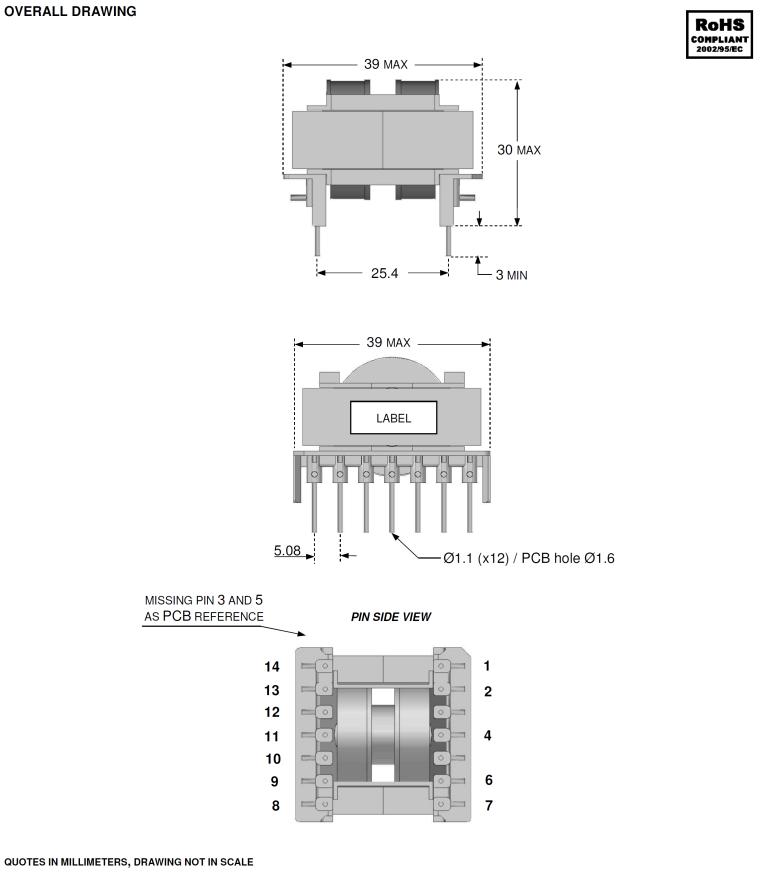
Pins	Windings	RMS current	Number of turns	Wire type
2 - 4	Primary	1 A_{RMS}	36	30 x Φ 0.1 mm - G1
8 - 11	SEC-1A (1)	8.5 A_{RMS}	2	90 x Φ 0.1 mm - G1
9 - 10	SEC-1B (1)	8.5 A_{RMS}	2	90 x Φ 0.1 mm -G1
10 - 13	SEC-2A (1)	8.5 A_{RMS}	2	90 x Φ 0.1 mm -G1
12 - 14	SEC-2B (1)	8.5 A_{RMS}	2	90 x Φ 0.1 mm -G1
6 - 7	AUX (2)	0.05 A_{RMS}	3	Φ 0.28 mm - G2

1. *Secondary windings A and B are in parallel.*
2. *AUX winding is wound on the top of secondary windings.*

Mechanical aspect and pin numbering

- Maximum height from PCB: 30 mm
- Coil former type: horizontal, 7 + 7 pins (pins #1, #3 and #5 are removed)
- Pin distance: 5.08 mm
- Row distance: 25.4 mm

Figure 77. Transformer overall drawing



Manufacturer

- AQ Magnetica - Italy
- Transformer P/N: 1860.0164

9 Appendix D Biasing circuitry and HW connections

9.1 VAC pin connection

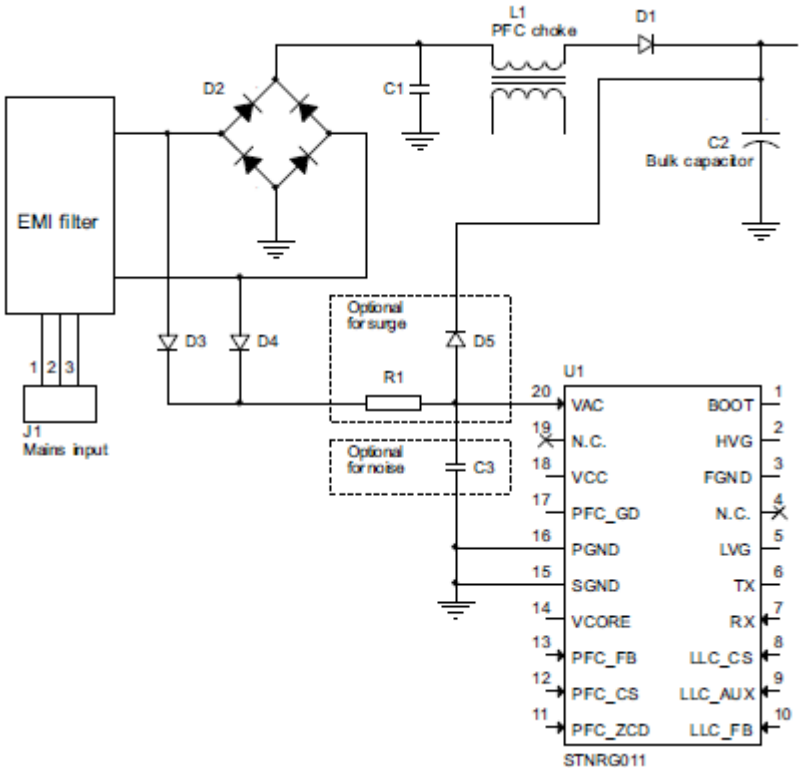
The VAC pin is used to perform several different functions related to the mains voltage.

The pin requires sensing the AC voltage and this can be done by using two diodes connected before the bridge diode like the D3 and D4 in Figure 78. Please note that the device is sensing a low frequency signal (100 Hz ÷ 120 Hz) therefore an economical standard diode should be used (like 1N4007 or similar).

Using an ultrafast rectifier will not add any benefit; depending on the board, it could even have the drawback to inject noise on the VAC pin.

The R1 and D5 can be used to protect the device in case of surge: the D5 acts as a voltage clamp, while the R1 limits the current through diodes.

Figure 78. VAC pin connection

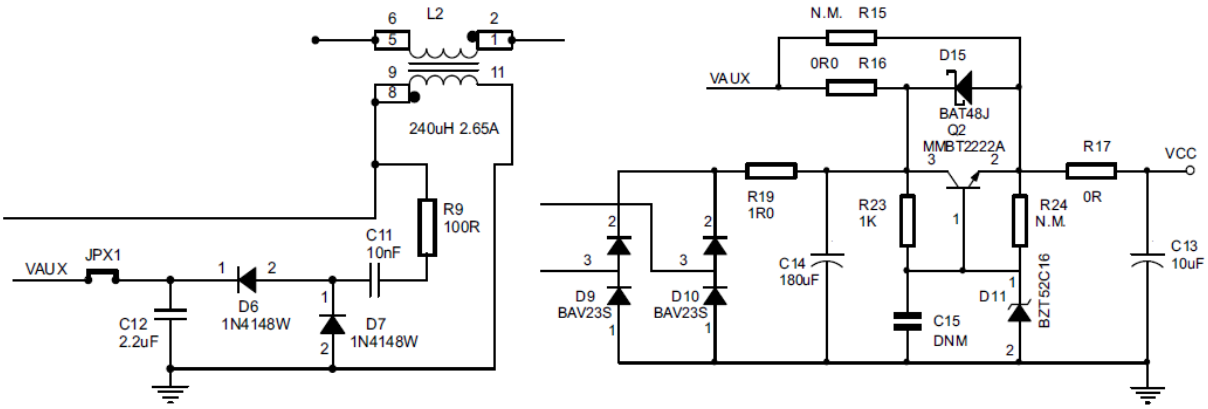


9.2 IC supply circuitry

Figure 79 shows the IC supply circuity, obtained from the original EVLSTNRG011-150 circuit diagram. When the mains voltage is applied, the IC sink the current from the VAC pin, charging the capacitor connected to the VCC pin. During this phase, both capacitors C13 and C14 are charged by the VCC pin, because the diode D15 conducts as soon as the voltage on the C13 is higher than the C14 plus the voltage of the diode forward drop. The diode also avoids the breakdown of the BTJ regulator Q2. A low voltage N-channel MOSFET can be used instead of the couple BJT-diode.

As soon as the IC starts driving the PFC MOSFET, the charge pump R9-C11-D6-D7 connected to the auxiliary winding of the PFC inductor, recharges the C14. The linear regulator Q2-R23-D11 will ensure that the maximum V_{CC} voltage during running is kept below of 16 V. The C14 is also recharged by the auxiliary winding of the LLC transformer through the full bridge rectification made with the D9 and D10, in order to keep the V_{CC} high also when the system works at low loads and the PFC charge pump is not able to sustain it.

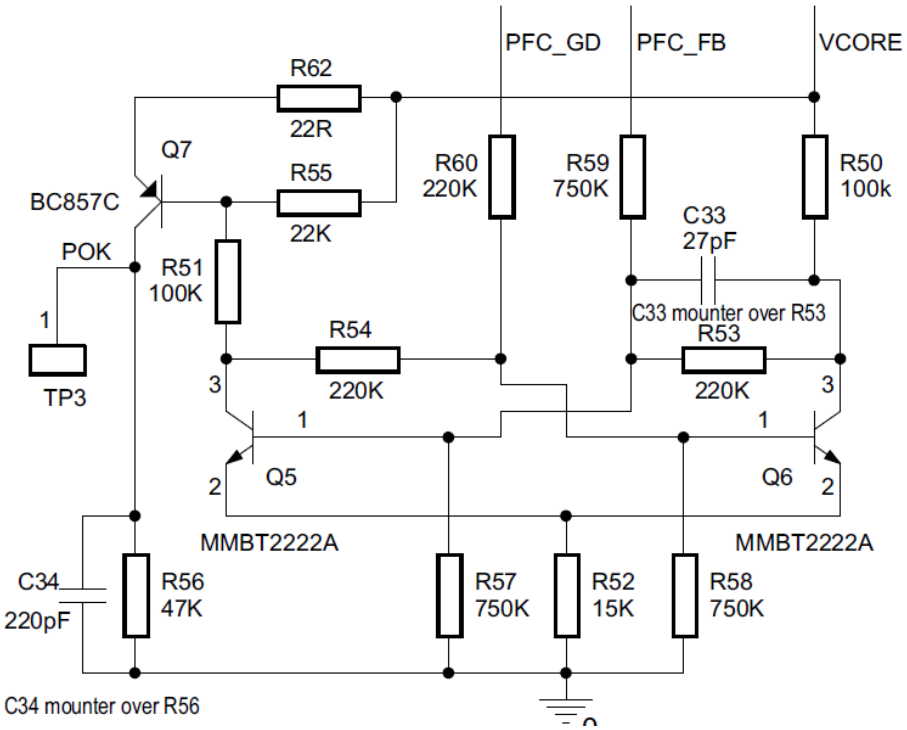
Figure 79. **IC supply circuitry**



9.3 Power OK (POK) signal generation circuitry

The Power OK signal is generated by the circuitry composed by the transistors latch Q5-Q6 and the common emitter transistor Q7, as shown in Figure 80. The latch is set (i.e. the Q5 is turned-on) during the early warning signal generation when the PFC_FB pin voltage is put higher than 4 V, while it is reset when the PFC_GD is tuned-on. When the latch is set, also the transistor Q7 is on and the POK signal is put high (negative logic).

Figure 80. **POK circuitry**



Revision history

Table 16. **Document revision history**

Date	Version	Changes
02-Feb-2018	1	Initial release.
17-May-2022	2	Footnote inserted in Table 10, Table 1.
16-Sep-2024	3	Updated figures descriptions in Section 1.2.

Contents

List of tables

List of figures