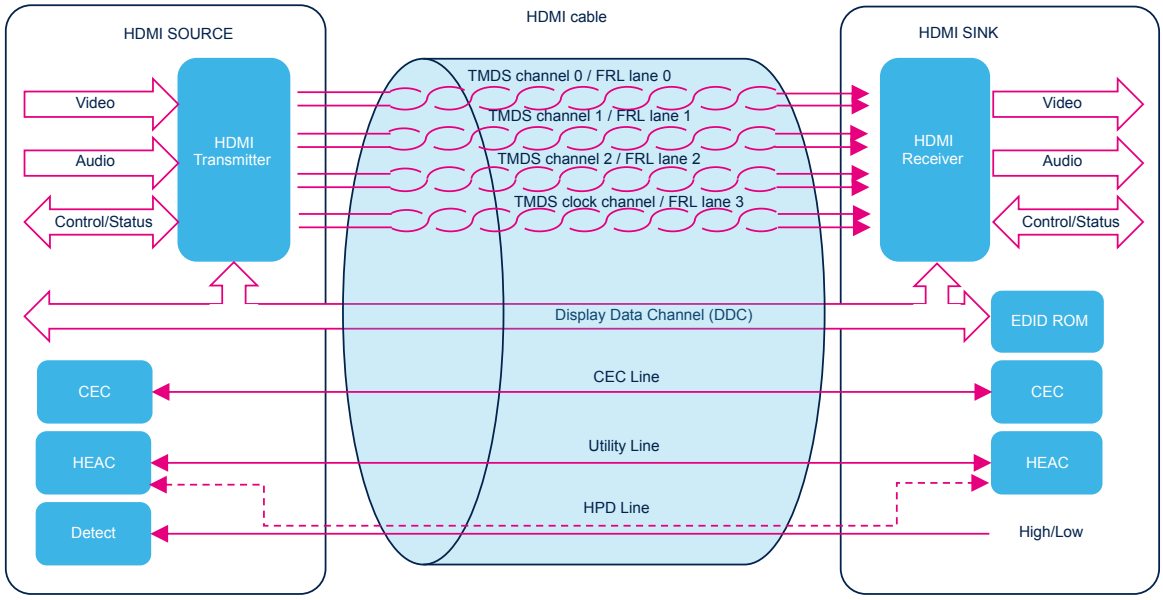
HDMI ESD protection, filtering and signal conditioning products

Introduction

HDMI (high-definition multimedia interface) is a proprietary audio/video digital interface for transferring uncompressed video data and compressed or uncompressed audio data.

An HDMI link is composed of one HDMI source and one HDMI sink linked together through an HDMI cable. As shown in Figure 1, HDMI link is composed of four physically separate communication channels, which are TMDS/FRL, DDC, CEC (optional) and HEAC (optional).

Figure 1. HDMI block diagram



The TMDS channel is composed of four differential pairs, used to carry video, audio, and auxiliary data with a maximum throughput of 48Gbps for HDMI 2.1b using FRL coding, from the HDMI source to the HDMI sink.

The VESA DDC channel is composed of two lines and based on the I²C protocol. It is used for configuration and status exchange between a single source and a single sink. HDMI requires a maximum data rate of 100 kbps corresponding to I²C standard mode speed operation.

The optional CEC channel provides control functions between up to 10 HDMI devices. It is a one-wire bidirectional communication bus, based on the CENELEC AV-link protocol.

The HEAC channel, composed of HEC and/or ARC channel, use the utility pin and the HPD pin to provide bidirectional 100 Mbps Ethernet link (HDMI Ethernet channel) and an audio channel (audio return channel) from the sink to the source.

This application note presents the HDMI port's electrical characteristics for each channel and the constraints induced on ESD protection or filtering devices choice.

Finally, ST offers in ESD protection and filtering for HDMI port and signal conditioning for DDC/CEC lines is presented.

1 EMI/EMC for STB: ESD test system

All equipment that shall comply with CISPR20/EN55020 or CISPR24/EN55024 standards must be able to withstand up to ±8 kV air discharge or ±4 kV contact discharge according to IEC61000-4-2 standard. The surge current waveform is given on Figure 2, the voltage level on Table 1.

Figure 2. IEC61000-4-2 typical current waveform, contact discharge

Table 1. IEC61000-4-2 ESD level, contact discharge

Level	Indicated voltage	First peak current of discharge ±15 %	Rise time t_r (±25 %)	Current (± 30 %) at 30 ns	Current (± 30 %) at 60 ns
	kV	A	ns	A	A
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

The equipment shall continue to operate as intended after the test. No loss of function is allowed after the test when the apparatus is used as intended, but failures which are recovered automatically but which cause temporary delay in processing, are permissible. No change of actual operating state, for example change of channel or stored data and settings, is allowed as a result of the test application. During the test, degradation of performance is allowed.

For further information, you can look at application notes:

- AN3353 “IEC61000-4-2 standard testing”
- AN5241 “Fundamentals of ESD protection at system level”

2 TMDS lines requirements

2.1 Data rate

2.1.1 TMDS coding

HDMI link is composed of four high-speed TMDS lines: 3 dedicated to data, 1 dedicated to clock synchronization. The clock lane speed is 1/10th of data lanes speed for a data rate lower than 3.4Gbps, and 1/40th of data lanes speed for a data rate between 3.4Gbps and 6Gbps. The maximum data rate for TMDS coding is 5.94Gbps.

The data rate on HDMI TMDS lanes depends on video resolution, frame rate, and color depth. The pixel clock rate versus video resolution is given in EIA/CEA 861 standard (table 2 in EIA/CEA 861-D).

2.1.2 FRL coding

When operating in fixed rate link (FRL) mode, the TMDS clock signal pair carries a fourth data lane. In this mode, the clock information is embedded in 16b18b coded data. The data rates per lane allowed are 3Gbps and 6Gbps in 3-lanes configuration, and 6Gbps, 8Gbps, 10Gbps and 12Gbps in 4-lanes configuration.

2.2 Eye diagram

The signal quality transmission is evaluated through eye diagram measurement. HDMI standard defines the eye diagram mask function of TMDS or FRL data rate. Eye diagrams are measured at HDMI connector output (TP1) for data rate lower than 3.4Gbps, and at the end of reference cable (TP2_EQ) for data rate higher than 3.4Gbps.

Figure 3. HDMI source test point for Eye diagram

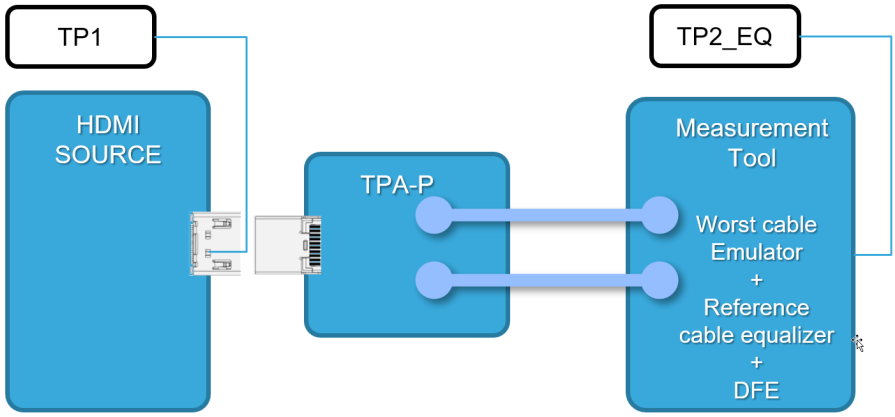
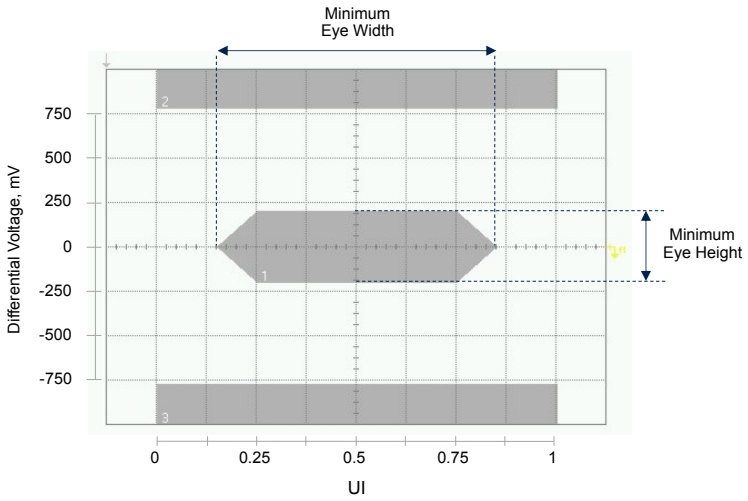
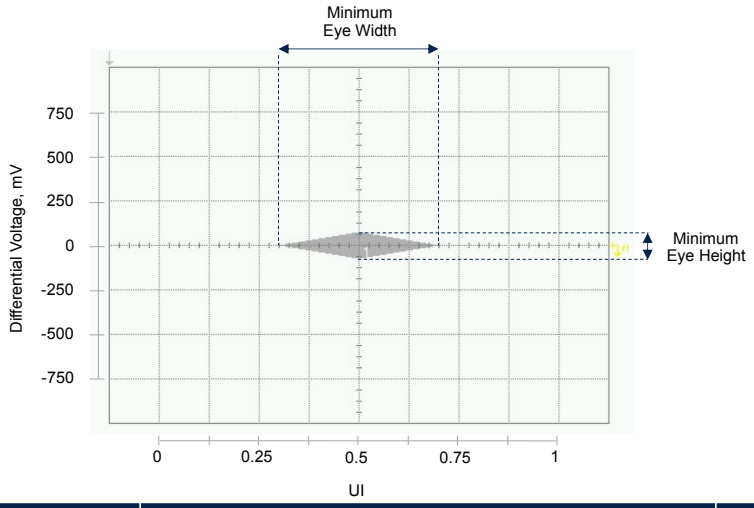


Figure 4. HDMI source Eye diagram mask at TP1, R_{bit} ≤ 3.4Gbps



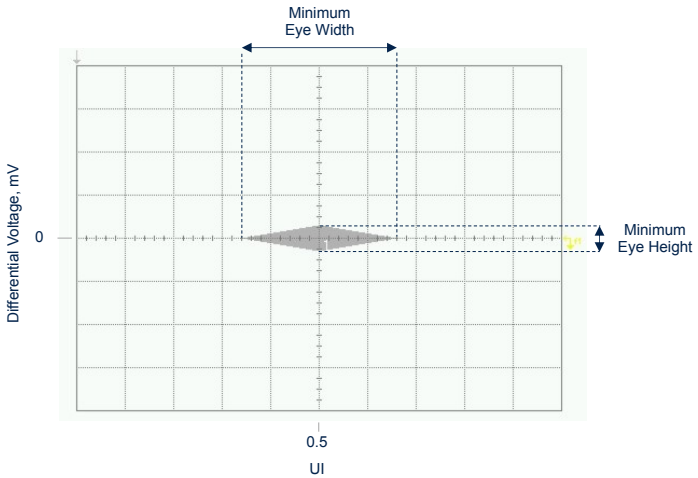
Signal Characteristics	Minimal	Nominal	Maximum	Units
Eye Height	400		1560	mV
Eye Width	0.700			UI

Figure 5. HDMI source Eye diagram mask at TP2_EQ, 3.4Gbps < R_{bit} ≤ 6.0Gbps



Signal characteristics	TMDS bit rate (Gbps)			Unit
	3.4 < R_{bit} < 3.712	3.712 < R_{bit} < 5.94	5.94 < R_{bit} < 6.0	
Eye Height	335	$-19.66R_{bit}^2 + 106.74R_{bit} + 209.58$	150	mV
Eye Width	0.6	$-0.0332R_{bit}^2 + 0.2312R_{bit} + 0.1998$	0.4	UI

Figure 6. HDMI source Eye diagram mask at TP2_EQ for FRL coding



FRL bit rate (Gbps)	Eye Height (mV)	Eye width (UI)
3	150	0.5
6	150	0.4
8	135	0.385
10	120	0.37
12	100	0.35

2.3 Differential impedance

To ensure a good signal propagation minimizing signal distortion, the entire transmission channel must be impedance matched.

The impedance is checked through TDR measurements for HDMI sink and cable. It is also checked on source side since HDMI 2.0 specification.

The TDR rise time must be set to 200 ps defined between 10 % and 90 %.

Table 2. HDMI source and Sink TMDS\FRL lane characteristic impedance

Coding	Data rate	Source		Sink	
		Through connector	Termination impedence	Through connector	Termination impedence
TMDS	R_{bit} ≤ 3.4Gbps	N/A	N/A	100 Ω ±15 %(1)	100 Ω ±10 %
	3.4Gbps < R_{bit} ≤ 6.0Gbps	100 Ω ±15 %(3)	75 Ω min., 150 Ω max.	100 Ω ±15 %(1)	100 Ω ±10 %
FRL	3Gbps, 6Gbps, 8Gbps, 10Gbps, 12Gbps	100 Ω ±10 %(2)(3)(4)	100 Ω ±10 %(4)	100 Ω ±10 %(1)	100 Ω ±10 %

1. *Impedance from TP2 to sink termiation.*
2. *A single excursion is permitted out to a max./min. 100 Ω ±25 Ω and of a duration less than 250 ps.*
3. *Impedance from TP1 to source termiation.*
4. *Informative specification. Eye diagram at TP2_EQ is normative for the source output signal.*

2.4 PCB layout design

To ensure a good signal propagation minimizing signal distortion, the TMDS channel must be impedance matched. The PCB layout must be carefully designed with a differential impedance without ESD protection device as close as possible to 100 Ω unless specific requirements.

The ESD protection/EMI filter must be placed as close as possible to the connector for ESD safety reasons.

The tracks between the ESD protection device and the line to be protected and between the protection device and the ground plane must also be as short as possible to minimize the inductor effect on clamping voltage value. Indeed, the tracks parasitic inductor adds an extra voltage to the clamping voltage of the ESD protection device.

Figure 7. Unoptimized ESD protection layout

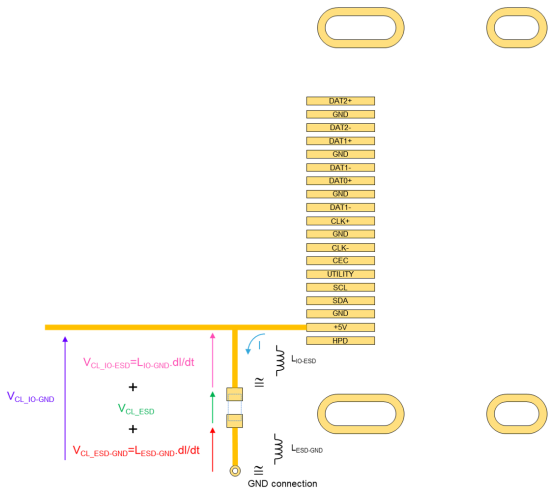
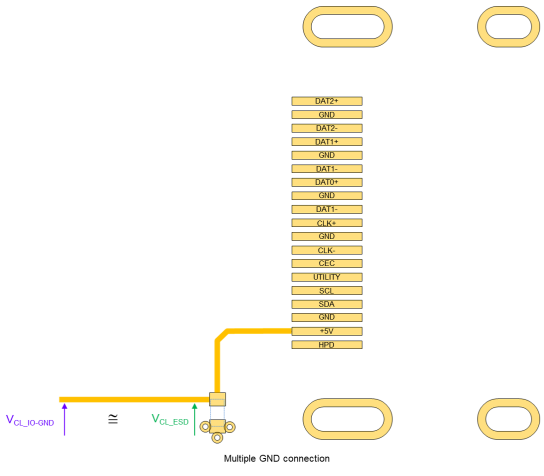


Figure 8. Optimized ESD protection layout



For further information, you can look at the application notes AN5686 “PCB layout tips to maximize ESD protection efficiency.”

3 Control lines

3.1 DDC bus

3.1.1 HDMI standard requirements

The HDMI DDC bus is a point-to-point bidirectional communication link based on the I²C bus specification. DDC bus shall meet the I²C specification in standard mode, meaning a maximum data rate of 100 kbit/s. The I²C standard mode's timing specifications are shown in Table 3.

Table 3. I²C timing requirements in standard mode (I²C specification, UM10204 rev. 7)

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	100	kHz
t_r	Rise time		1000	ns
t_f	Fall time		300	ns

HDMI devices shall have DDC electrical characteristics complying with the values shown in Table 4, Table 5, and Table 6. That means a maximum total DDC bus capacitance of 1.5 nF in automotive application (HDMI source + automotive cable + CE relay cable + automotive relay cable + HDMI sink), with SDA/SCL pull-up resistor between 1.5 kΩ and 2.0 kΩ on source side, and with SCL pull-up resistor of 47 kΩ ±10 % on sink side.

Although the HDMI standard specifies a maximum capacitance of 700 pF on DDC bus for cable, some on the market can have a higher capacitance value. Per example, the capacitance of SDA to ground or SCL to ground have been measured at 1.7 nF on one 15 m cable.

Table 4. Maximum capacitance of DDC lines (HDMI 1.4, table 4-35)

Item	HDMI source	Cable assembly	HDMI sink
SDA-DDC/CEC GROUND	50 pF	700 pF	50 pF
SDL-DDC/CEC GROUND	50 pF	700 pF	50 pF

Table 5. Maximum capacitance of DDC lines for automotive (HDMI 1.4, table 4-36)

Item	HDMI source	Cable assembly			HDMI sink
		Automotive cable	CE relay cable	Automotive relay cable	
SDA-DDC/CEC GROUND	50 pF	700 pF	210 pF	490 pF	50 pF
SDL-DDC/CEC GROUND	50 pF	700 pF	210 pF	490 pF	50 pF

Table 6. HDMI 1.4 pull-up resistors on DDC lines (HDMI 1.4, table 4-37)

Item	Min.	Typ.	Max.
SDA and SCL source pull-up resistors	1.5 kΩ		2.0 kΩ
SCL sinks pull-up resistor	42.3 kΩ	47 kΩ	51.7 kΩ

The failure to respect I²C timing and electrical requirements can generate interoperability issues at end customer side.

3.1.2 Benefits of switched pull-up on DDC bus

It is difficult to fulfill I²C timing specification according to HDMI requirements in worse DDC bus capacitance condition.

The Eq. (1), rise time function of pull-up resistor value and bus capacitance, gives the relation between rise time, pull-up resistor, and bus capacitance for a rise time defined between 0.3 V_{DD} and 0.7 V_{DD}.

$$t_r = 0.85 \times R_{PU} \times c_{DDC\_BUS} \quad (1)$$

Assuming a pull-up resistor of 2.0 kΩ with a bus capacitance of 800 pF, the rise time is 1.36µs, higher than the 1µs maximum value specified in HDMI standard.

Assuming a 1.5 kΩ pull-up resistor with the same 800 pF bus capacitance, the rise time is 1.02 µs, higher than the maximum value allowed.

HDMI standard allows the use of switched pull-up circuit to manage high capacitance buses as describe in the I²C standard. A switched pull-up circuit helps to fulfill HDMI and I²C timing requirements on the DDC bus by temporarily decreasing the pull-up resistor value.

Figure 9. 30 %-70 % rise time measurement with and without dynamic pull-up resistor, C_{LOAD} = 450 pF

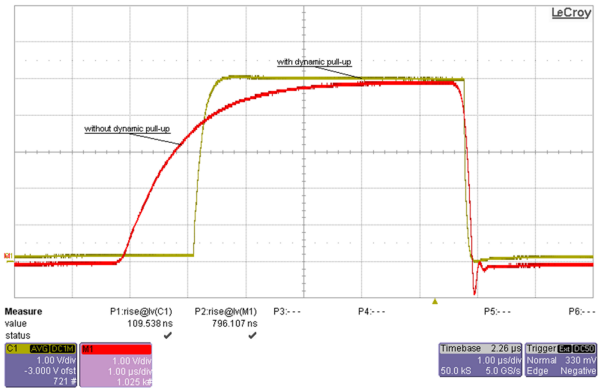
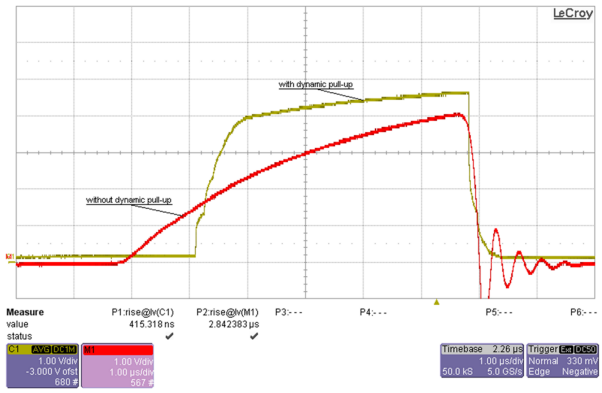


Figure 10. 30 %-70 % rise time measurement with and without dynamic pull-up resistor, C_{LOAD} = 1.5 nF



Switched pull-up circuit helps to fulfill I²C timing requirements and reduces the risk of interoperability issue.

3.2 +5 V power pin

The HDMI connector provides a pin allowing the source to supply +5 V to the cable and Sink. All HDMI sources shall be able to supply a minimum of 55 mA to the +5 V power pin, with an overcurrent protection of no more than 0.5 A. The voltage at the source output must be between 4.8 V and 5.3 V.

An HDMI sink shall draw no more than 50 mA when powered off from a +5 V power pin, and no more than 10 mA when powered on. The voltage at the sink input must be between 4.7 V and 5.3 V.

Figure 11. HDMI test points

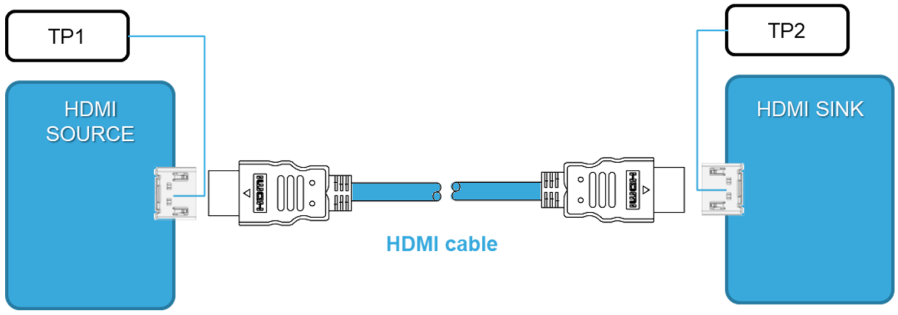


Table 7. +5V power pin voltage

Item	Min.	Max.
Source output (TP1)	4.8 V	5.3 V
Sink input (TP2)	4.7 V	5.3 V

The +5 V power pin is used to provide power supply to the sink's E-EDID EEPROM even if the sink is powered off or in standby mode.

3.3 HPD line

An HDMI source device uses an HPD line to detect if a sink device is connected at the end of the HDMI cable. The HPD line is set to high level by the sink, sometimes through a 1kΩ resistor connected to +5 V power pin.

On the sink side, the HDP high level must be between 2.4 V and 5.3 V, on the source side between 2.0 V and 5.3 V.

HEAC (HDMI Ethernet and audio return channel) optional feature uses HPD line.

4 ST offer for ESD protection of TMDS or FRL lanes:

4.1 HSP051-4M10

HSP051-4M10 is a 4 lines diode array ESD protection, suitable to protect TMDS lanes of HDMI connector. Its ultra-low I/O/GND parasitic capacitance help to minimize the impact of ESD protection device on TDR response as shown in Figure 13. The very high frequency bandwidth (Figure 12) ensures a non-noticeable impact on eye diagram up to 3.4Gbps (Figure 14), and a small impact up to 12Gbps.

Figure 12. HSP051-4M10 attenuation

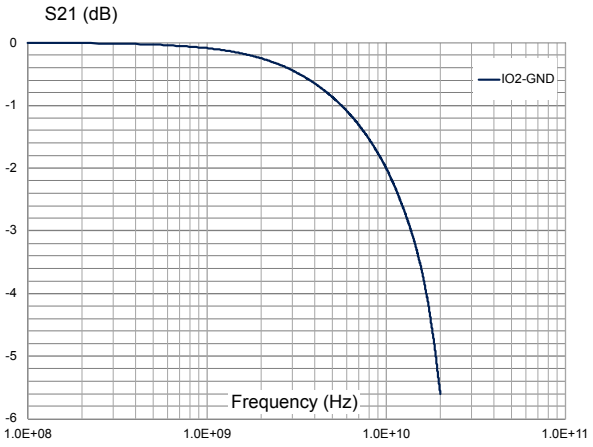


Figure 13. HSP051-4M10 TDR measurements, $t_{r\ 10\ \%-90\ \%}$ = 200 ps typical value

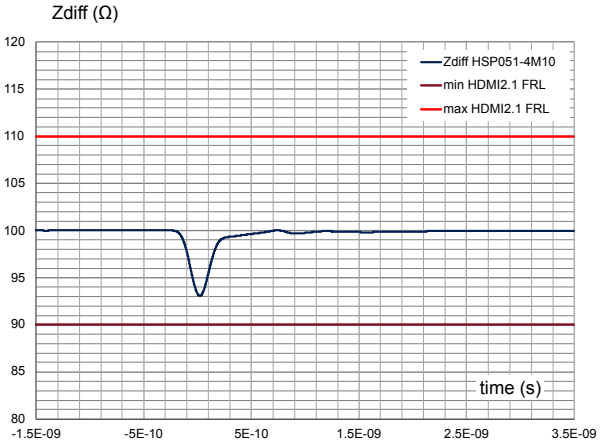


Figure 14. Eye diagram without the HSP051-4M10, 3.4Gbps

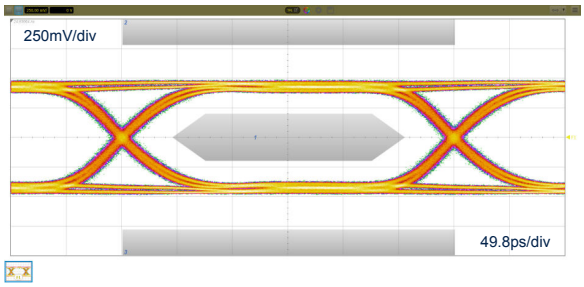


Figure 15. Eye diagram with the HSP051-4M10, 3.4Gbps

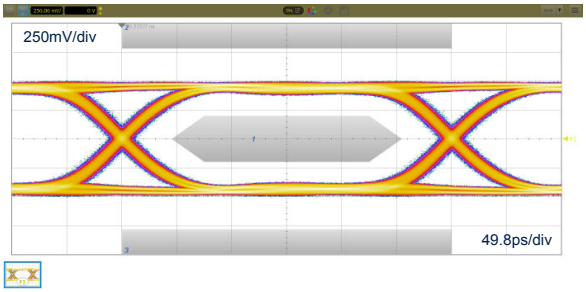


Figure 16. Eye diagram without the HSP051-4M10, HDMI1.4 5.94Gbps

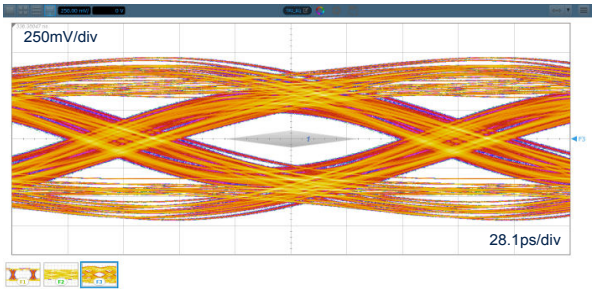


Figure 17. Eye diagram with the HSP051-4M10, HDMI1.4 5.94Gbps

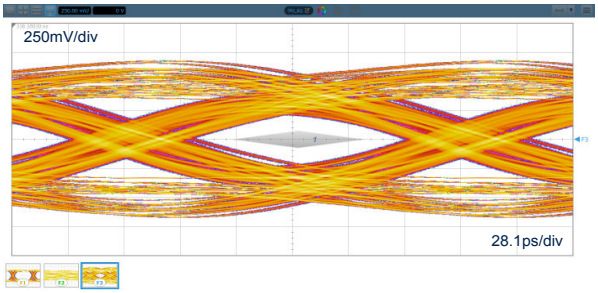


Figure 18. Eye diagram without the HSP051-4M10, HDMI2.1 6Gbps

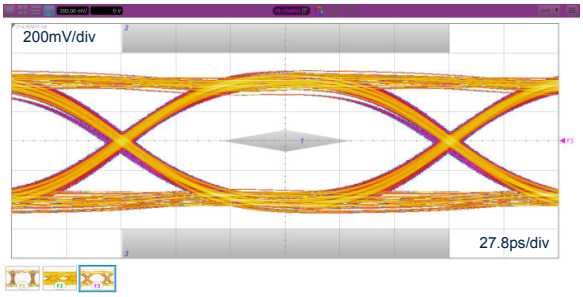


Figure 19. Eye diagram with the HSP051-4M10, HDMI 2.1 6Gbps

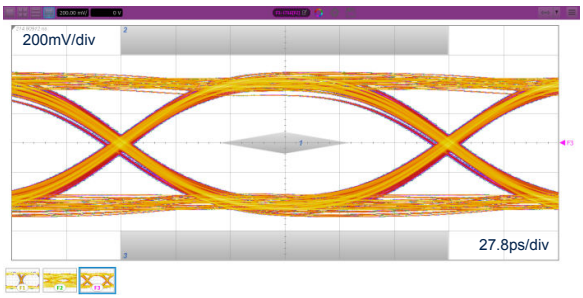


Figure 20. Eye diagram without the HSP051-4M10, HDMI2.1 12Gbps worst cable

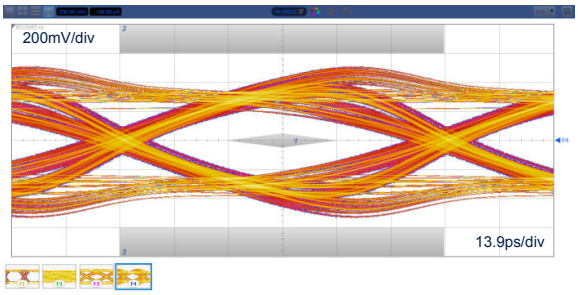
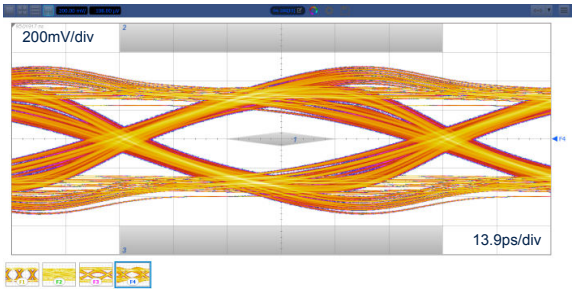


Figure 21. Eye diagram with the HSP051-4M10, HDMI 2.1 12Gbps worst cable



HDMI TMDS lanes require two HSP051-4M10 for ESD protection. The typical electrical schematic is given in Figure 22, an example of layout in Figure 23.

Figure 22. HSP051-4M10 electrical schematic

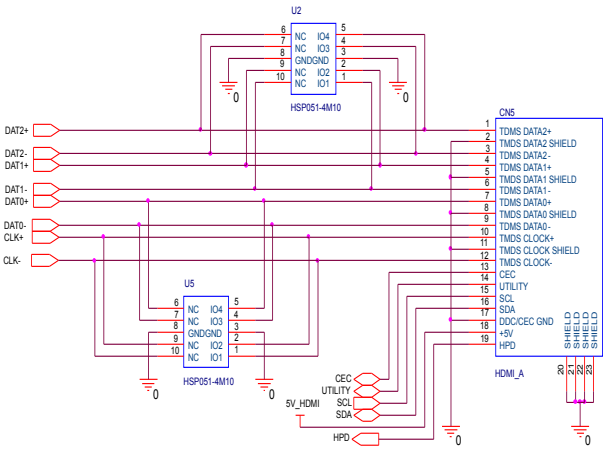
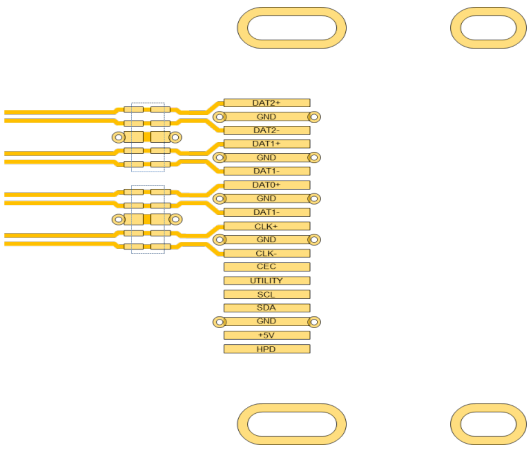


Figure 23. Layout example with 2xHSP051-4M10



4.2 HSP051-4N10

The HSP051-4N10 is a 4 lines diode array ESD protection, suitable to protect TMDS lanes of HDMI connector. Its ultra-low I/O/GND parasitic capacitance help to minimize impact of ESD protection device on TDR response as shown Figure 24. The very high frequency bandwidth ensures a non-noticeable impact or small impact on eye diagram according to HDMI 1.4b (Figure 26 to Figure 29) and HDMI 2.1b (Figure 30 to Figure 33).

Figure 24. HSP051-4N10 attenuation

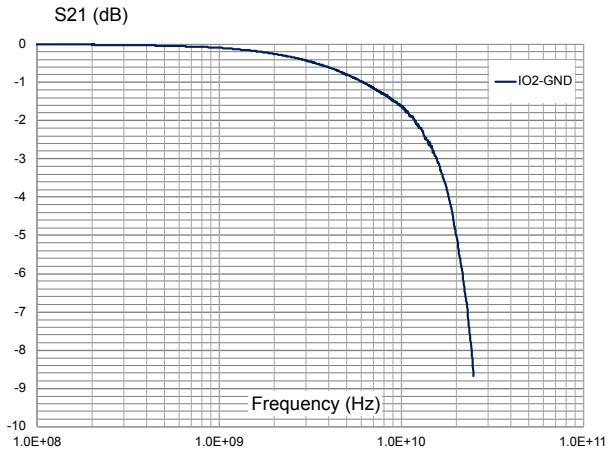


Figure 25. HSP051-4N10 TDR measurements $t_{r\ 10\ \%-90\ \%}$ = 200 ps typical value

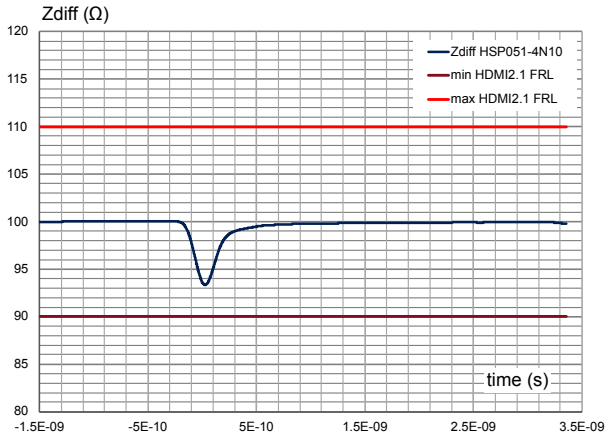


Figure 26. Eye diagram without the HSP051-4N10, 3.4Gbps

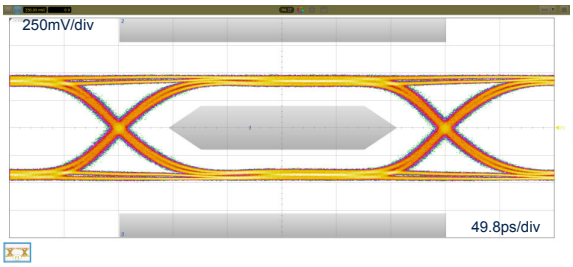


Figure 27. Eye diagram with the HSP051-4N10, 3.4Gbps

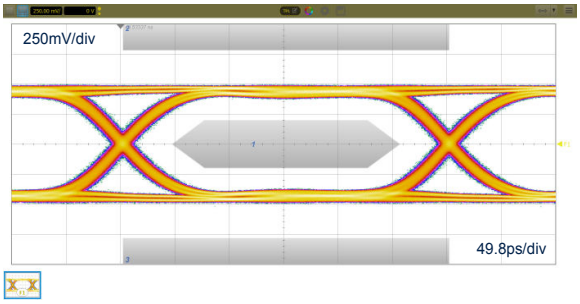


Figure 28. Eye diagram without the HSP051-4N10, HDMI1.4 5.94Gbps

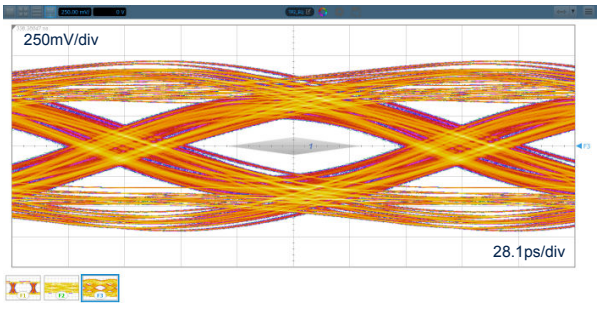


Figure 29. Eye diagram with the HSP051-4N10, HDMI1.4 5.94Gbps

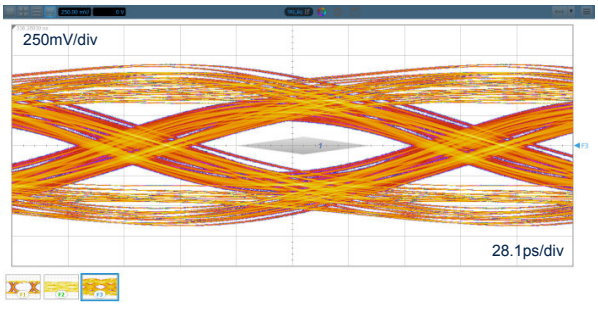


Figure 30. Eye diagram without the HSP051-4N10, HDMI2.1 6Gbps, worst cable model

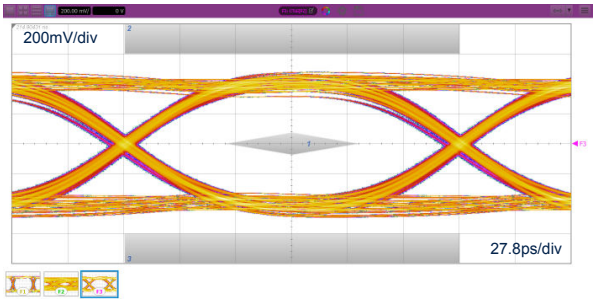


Figure 31. Eye diagram with the HSP051-4N10, HDMI 2.1 6Gbps, worst cable model

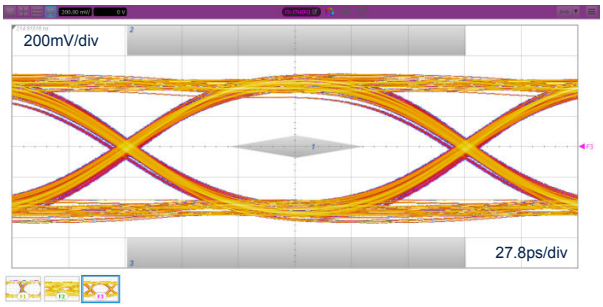


Figure 32. Eye diagram without the HSP051-4N10, HDMI2.1 12Gbps worst cable

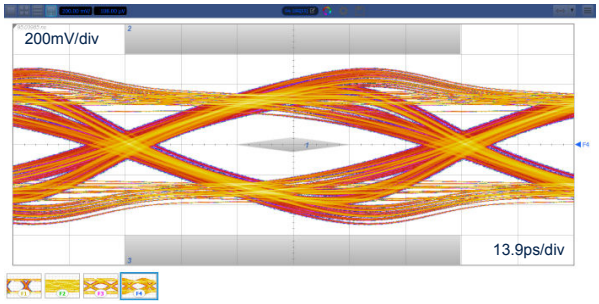
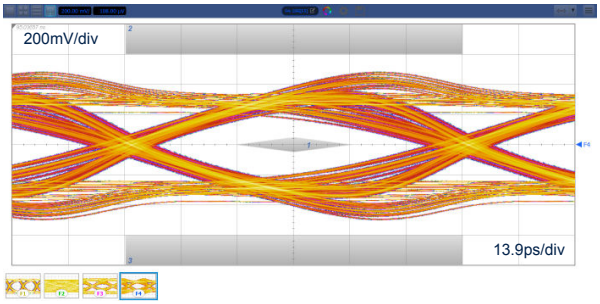


Figure 33. Eye diagram with the HSP051-4N10, HDMI 2.1 12Gbps worst cable



HDM TMDS/FRL lanes require two HSP051-4N10 for ESD protection. The typical electrical schematic is given in Figure 34, an example of layout in Figure 35.

Figure 34. HSP051-4N10 electrical schematic

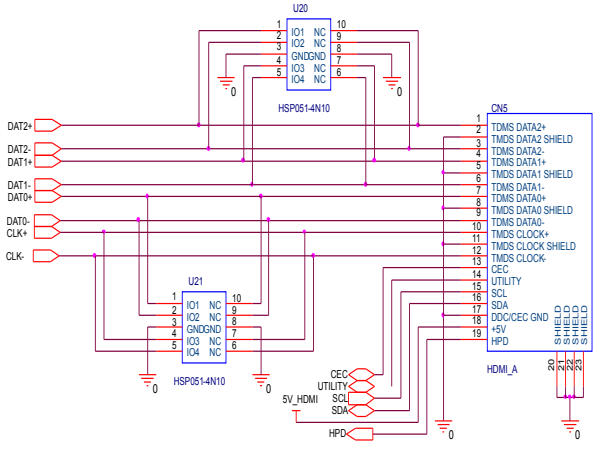
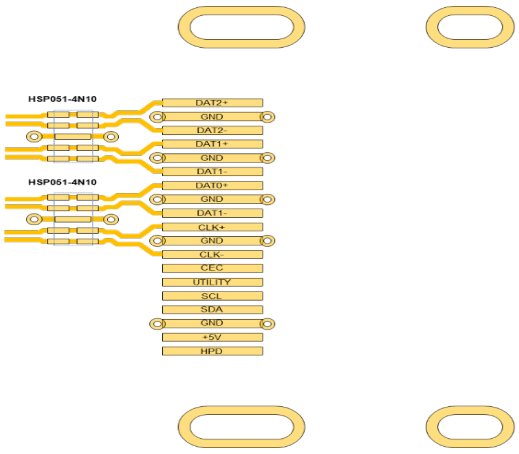


Figure 35. Layout example with 2xHSP051-4N10



4.3 HSP053-4M5

The HSP053-4M5 is a 4-line diode array ESD protection, suitable to protect TMDS lanes of HDMI connector. Its ultra-low IO/GND parasitic capacitance helps to minimize the impact of ESD protection device on TDR response as shown in Figure 37. The very high frequency bandwidth ensures a non-noticeable impact on eye diagram up to 3.4 Gbps (Figure 39), and a small impact up to 12 Gbps (Figure 45).

Figure 36. HSP053-4M5 attenuation

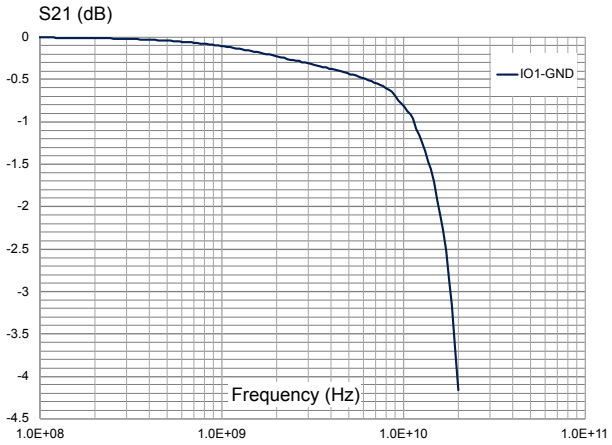


Figure 37. HSP053-4M5 TDR measurements, $t_{r\ 10\ \%-90\ \%}$ = 200 ps typical value

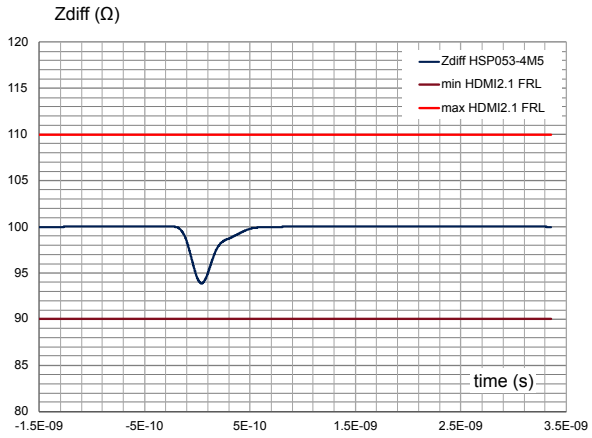


Figure 38. Eye diagram without HSP053-4M5, 3.4Gbps

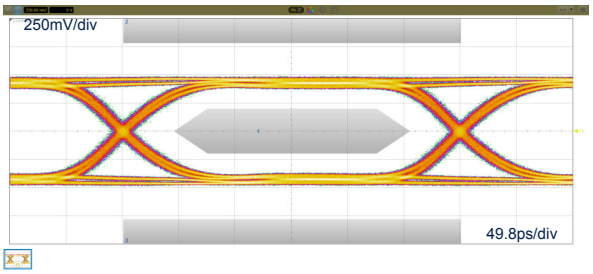


Figure 39. Eye diagram with HSP053-4M5, 3.4Gbps

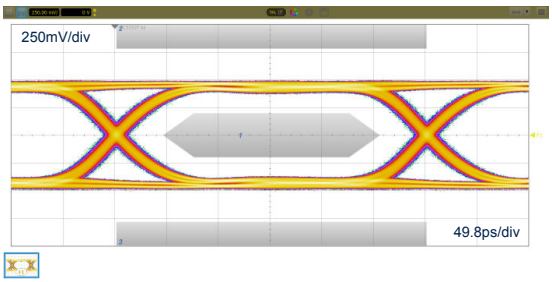


Figure 40. Eye diagram without HSP053-4M5, HDMI1.4 5.94Gbps

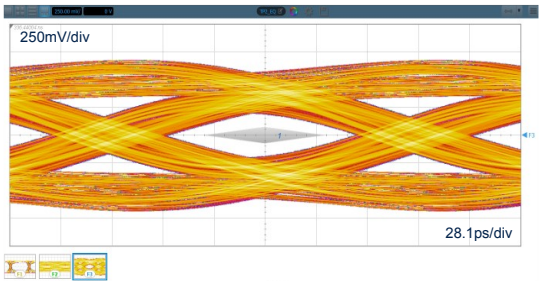


Figure 41. Eye diagram with HSP053-4M5, HDMI1.4 5.94Gbps

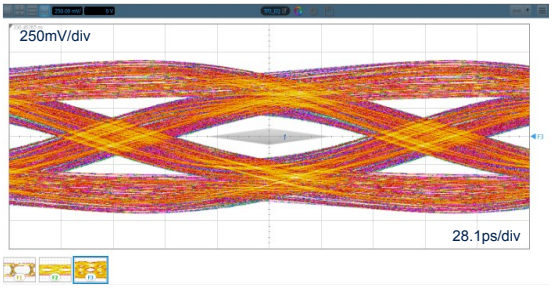


Figure 42. Eye diagram without HSP053-4M5, HDMI2.1 6Gbps

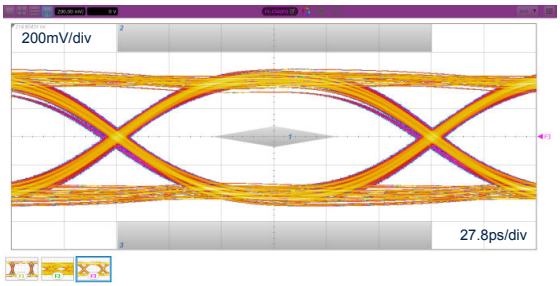


Figure 43. Eye diagram with HSP053-4M5, HDMI 2.1 6Gbps

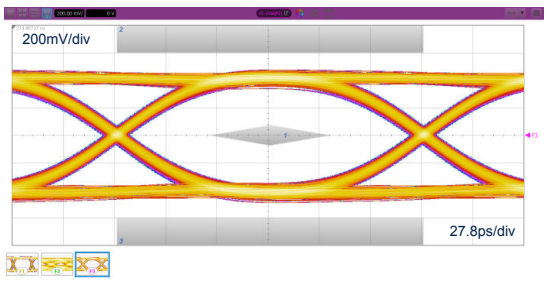


Figure 44. Eye diagram without HSP053-4M5, HDMI2.1 12Gbps worst cable

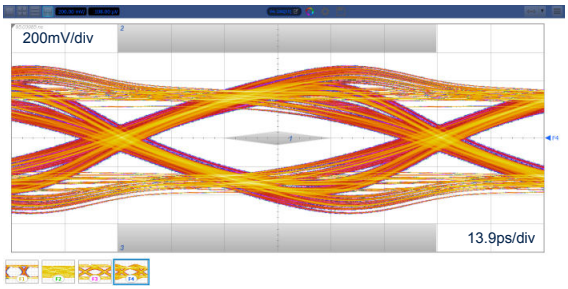
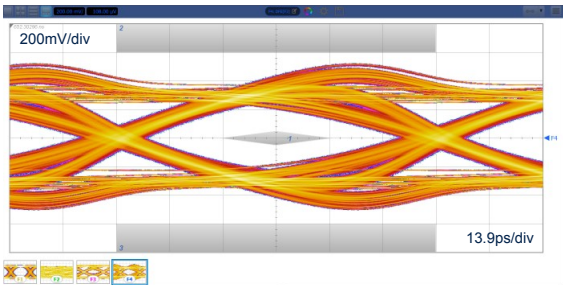


Figure 45. Eye diagram with HSP053-4M5, HDMI 2.1 12Gbps worst cable



HDMI TMDS lanes require two HSP053-4M5 for ESD protection. The typical electrical schematic is given in Figure 46, an example of layout in Figure 47.

Figure 46. HSP053-4M5 electrical schematic

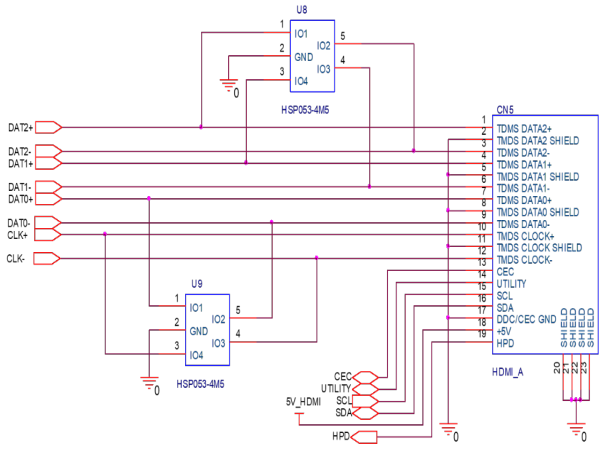
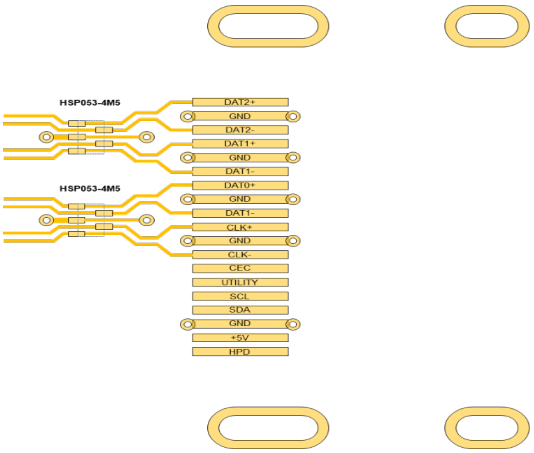


Figure 47. Layout example with 2xHSP053-4M5



5 Common-mode filtering with ESD protection for TMDS lanes

Intrapair skew on TMDS can induce a common-mode signal that can be an important source of radiated noise and can have an impact on other signals in the application by coupling.

Common-mode filters can be used to minimize this radiated noise.

You can refer to “EMI/EMC and co-existence simulation methodology for high performance digital, mixed signal and RF wireless products” technical article.

The STMicroelectronics ECMF family integrates common-mode filter and ESD protection in the same package.

You can refer to application note AN4511 “common-mode filters” and AN4356 “How to solve antenna desence issue with ECMF” for more information.

5.1 ECMF4-40A100N10 / ECMF2-40A100N6

ECMF4-40A100N10 and ECMF2-40A100N6 integrates ESD protection and common mode filter in the same plastic package. Its large differential bandwidth > 10 GHz and its high common mode attenuation on WLAN frequencies make it suitable for HDMI application.

Figure 48. ECMF4-40A100N10 differential mode attenuation

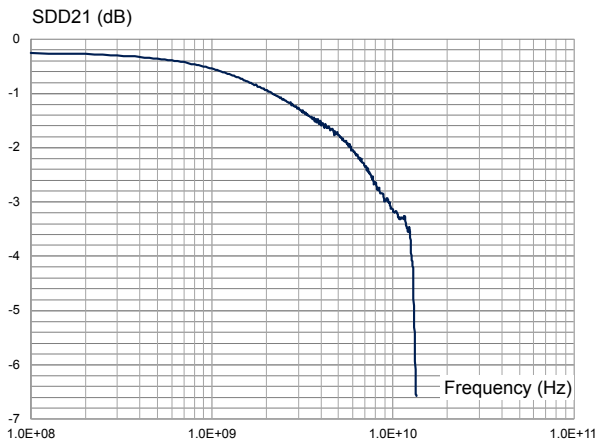


Figure 49. ECMF4-40A100N10 common mode attenuation

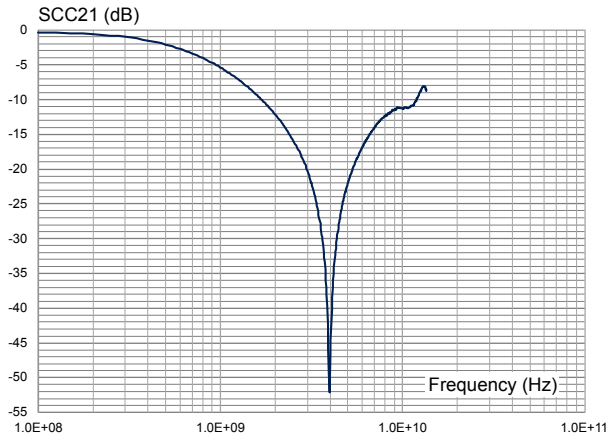


Figure 50. ECMF4-40A100N10 TDR measurements, $t_{r\ 10\ \%-90\ \%}$ = 200 ps typical value

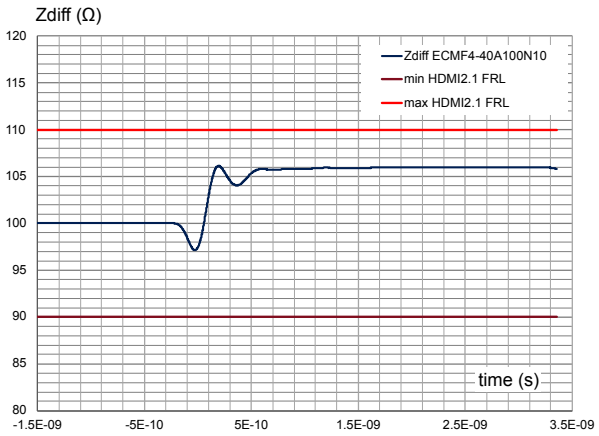


Figure 51. Eye diagram without ECMF4-40A100N10, 3.4Gbps

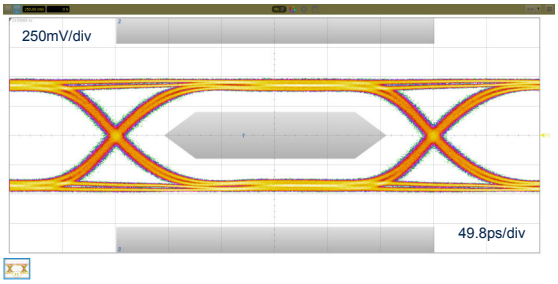


Figure 52. Eye diagram with ECMF4-40A100N10, 3.4Gbps

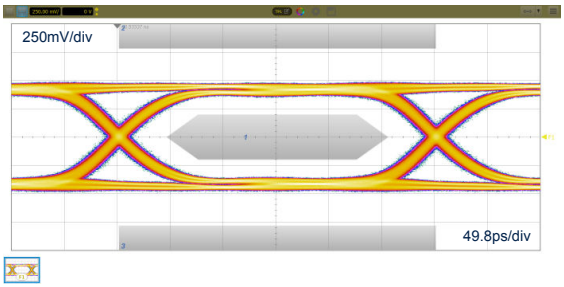


Figure 53. Eye diagram without ECMF4-40A100N10, HDMI1.4 5.94Gbps

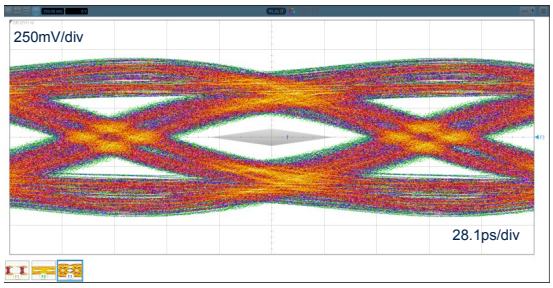


Figure 54. Eye diagram with ECMF4-40A100N10, HDMI1.4 5.94Gbps

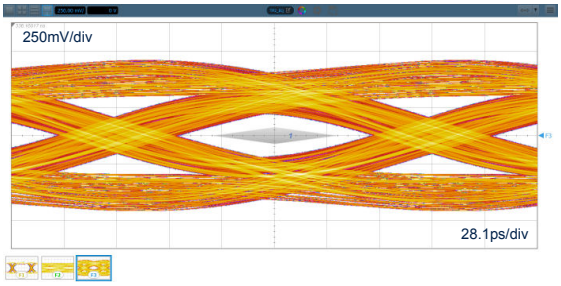


Figure 55. Eye diagram without ECMF4-40A100N10, HDMI2.1 6Gbps

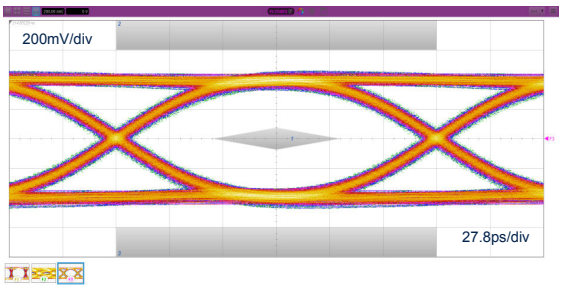


Figure 56. Eye diagram with ECMF4-40A100N10, HDMI 2.1 6Gbps

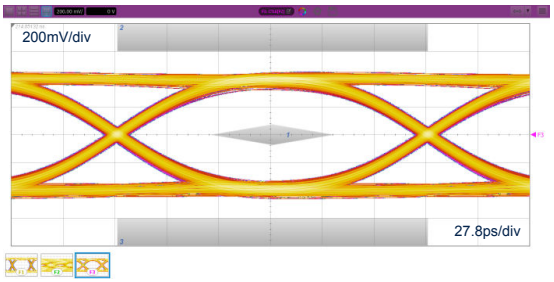


Figure 57. Eye diagram without ECMF4-40A100N10, HDMI2.1 12Gbps worst cable

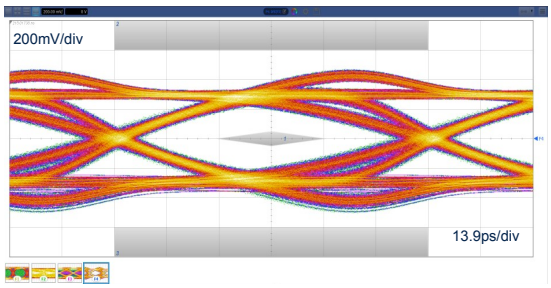


Figure 58. Eye diagram with ECMF4-40A100N10, HDMI 2.1 12Gbps worst cable

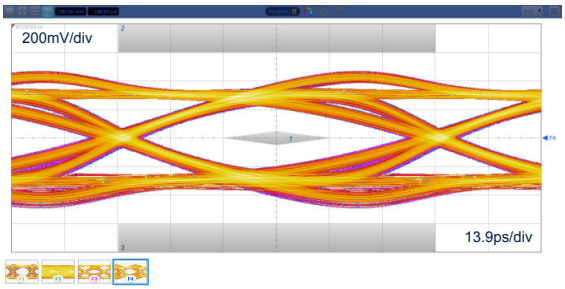


Figure 59. ECMF4-40A100N10 electrical schematic

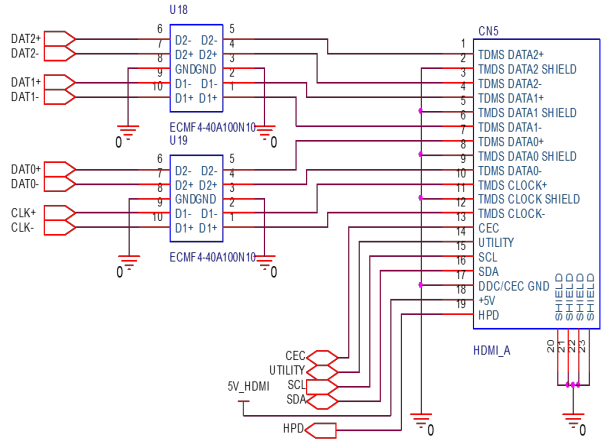


Figure 60. Layout example with 2xECMF4-40A100N10

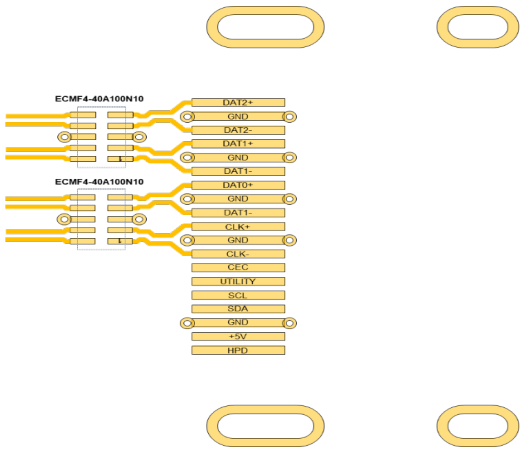


Figure 61. ECMF2-40A100N6 electrical schematic

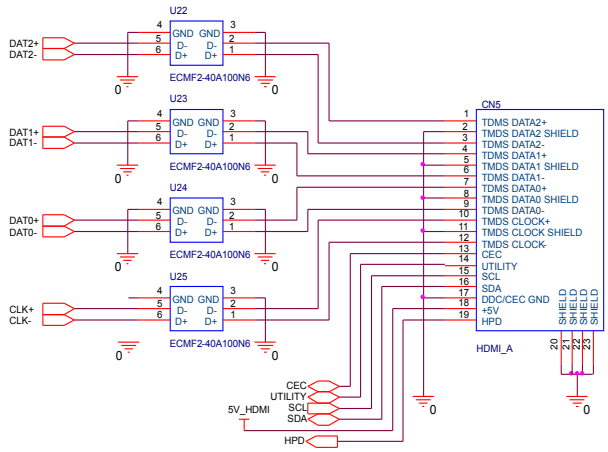
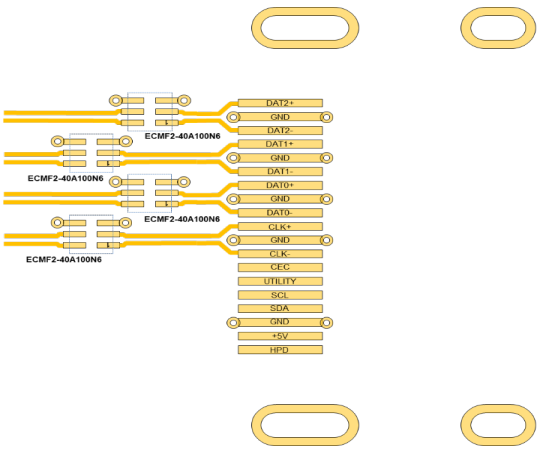


Figure 62. Layout example with 4xECMF2-40A100N6



5.2 ECMF4-2450A60N10

ECMF4-2450A60N10 is a 4-lines – 2-lanes common mode filter with ESD protection for high-speed serial interfaces. It is designed to suppress EMI/RFI common mode noise and present a very large differential bandwidth to comply with HDMI up to 12Gbps and a high common mode attenuation on WLAN frequency.

Figure 63. ECMF4-2450A60N10 differential mode attenuation

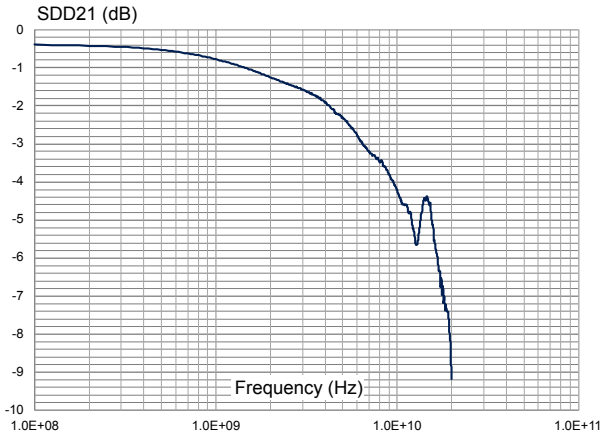


Figure 64. ECMF4-2450A60N10 common mode attenuation

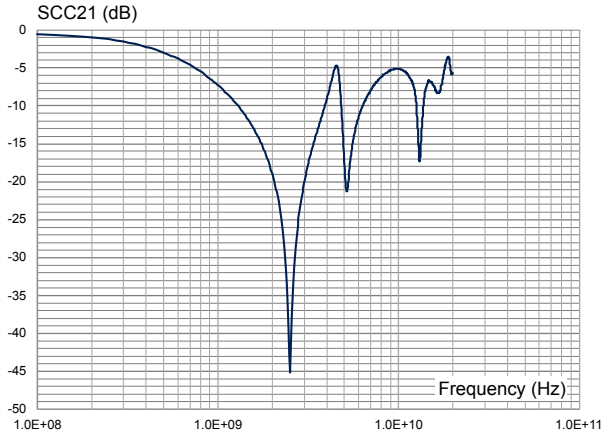


Figure 65. ECMF4-2450A60N10 TDR measurements, $t_{r\ 10\ \%-90\ \%}$ = 200 ps typical value

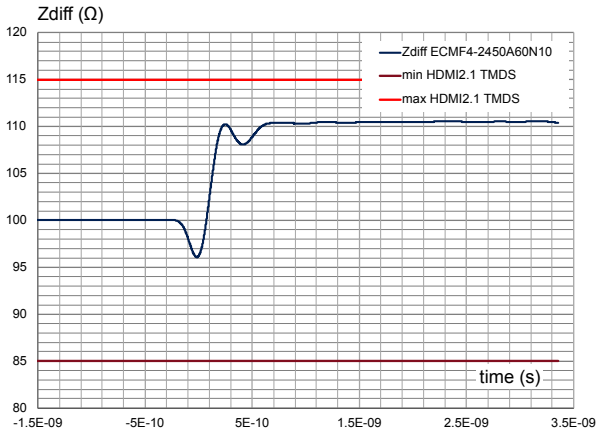


Figure 66. Eye diagram without ECMF4-2450A60N10, 3.4Gbps

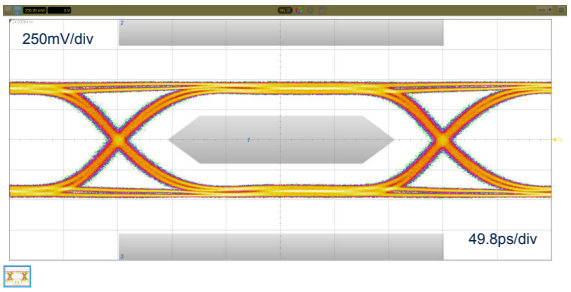


Figure 67. Eye diagram with ECMF4-2450A60N10, 3.4Gbps

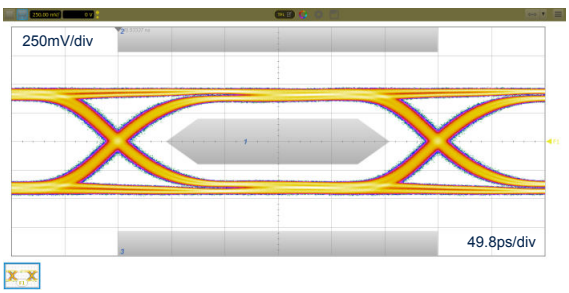


Figure 68. Eye diagram without ECMF4-2450A60N10, HDMI1.4 5.94Gbps

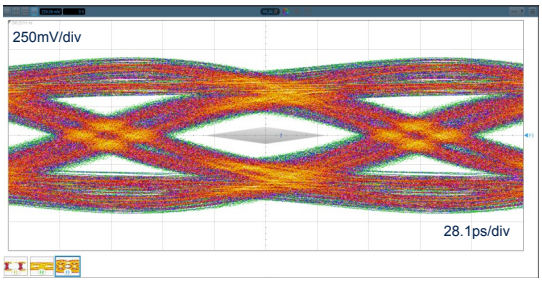


Figure 69. Eye diagram with ECMF4-2450A60N10, HDMI1.4 5.94Gbps

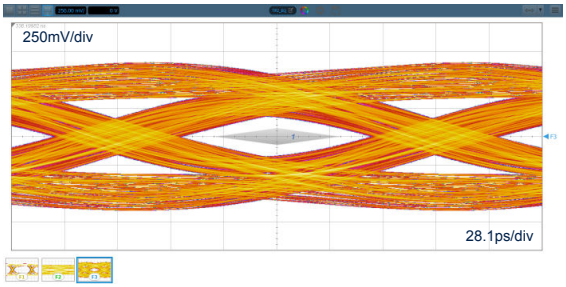


Figure 70. Eye diagram without ECMF4-2450A60N10, HDMI2.1 6Gbps

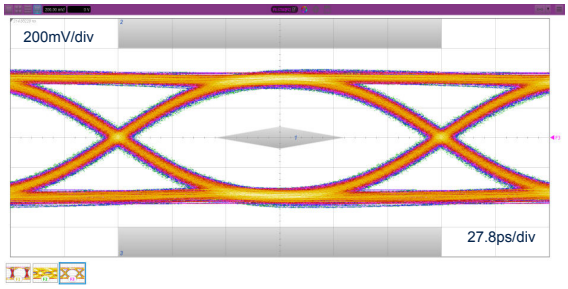


Figure 71. Eye diagram with ECMF4-2450A60N10, HDMI 2.1 6Gbps

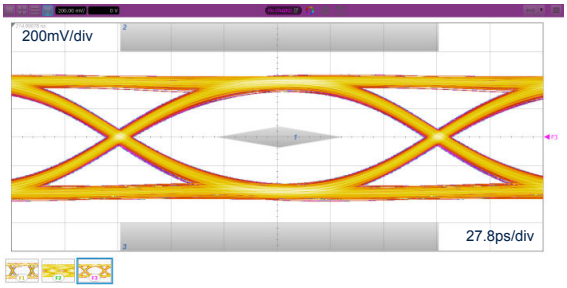


Figure 72. Eye diagram without ECMF4-2450A60N10, HDMI2.1 12Gbps worst cable

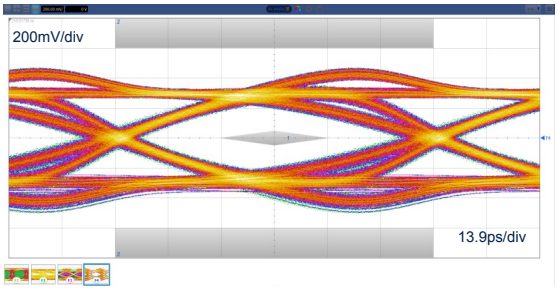
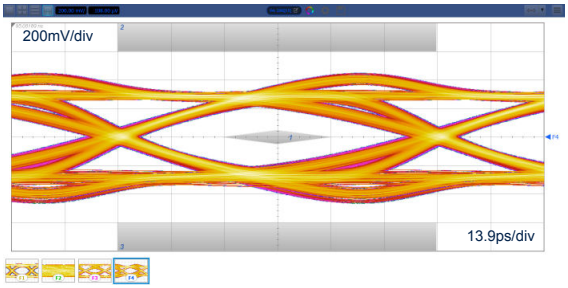


Figure 73. Eye diagram with ECMF4-2450A60N10, HDMI 2.1 12Gbps worst cable



HDMI TMDS lanes require two ECMF4-2450A60N10 for ESD protection and common mode filtering. The typical electrical schematic is given in Figure 74, an example of layout in Figure 75.

Figure 74. ECMF4-2450A60N10 electrical schematic

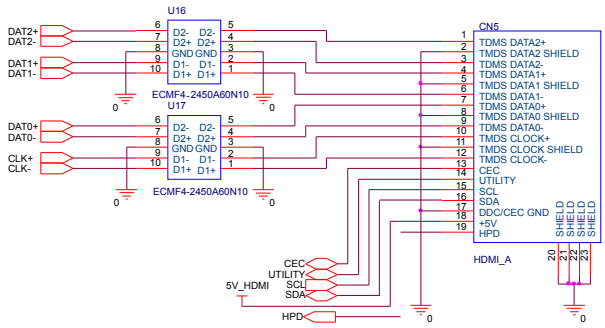
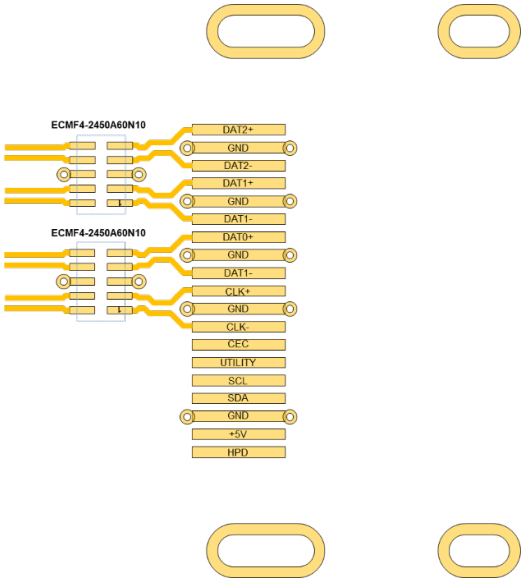


Figure 75. Layout example with 2xECMF4-2450A60N10



6 ST offer for Control lines

6.1 HDMI2Cx family features

- ESD protection

The HDMI2Cx product family is able to withstand ±8 kV contact discharge according to IEC61000-4-2 standard on connector pins and ±2 kV HBM on other pins.

- DDC bus

The HDMI2Cx product family integrates a level shifter on the DDC bus, allowing translating high-level voltage from 5 V on the cable side down to V_{DD_IC} on the system side.

It integrates dynamic pull-up resistors on DDC bus, allowing managing high capacitive cables exceeding HDMI standard specifications. Those dynamic pull-ups on cable side help to improve interoperability by ensuring a rise time on SDA and SCL lines compliant with HDMI and I²C specification even with a capacitive load twice higher than HDMI requirements.

The buffers on DDC bus ensure signal reshaping to improve signal quality transmission and ensure the compliancy with capacitance measurement.

- HPD

Unless specified, HDMI2Cx product integrate a level shifter on HPD line, ensuring signal reshaping and voltage translation from 5 V on cable side to V_{DD_IC} on system side. The HPD line is pulled down through an integrated current source.

- +5 V power pin

All HDMI2Cx products dedicated to source devices integrate on the +5 V power line a current limiter and a thermal protection to manage short circuit event on the +5 V HDMI connector pin.

6.2 HDMI2Cx for HDMI source devices

6.2.1 Control lines only

6.2.1.1 HDMI2C1-6C1

The HDMI2C1-6C1 is an integrated ESD protection and signal-conditioning device for control lines of HDMI source. It provides current limitation and short circuit protection on 5 V power pin. HDMI2C1-6C1 is available in QFN 18 leads, 500 µm pitch package.

Figure 76. HDMI2C1-6C1 package

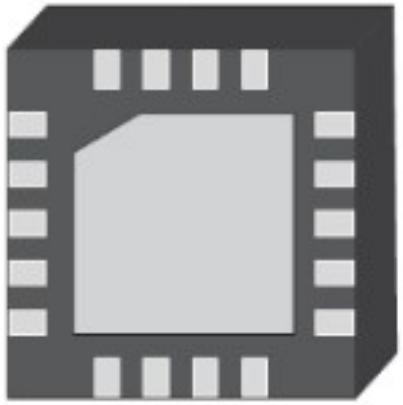
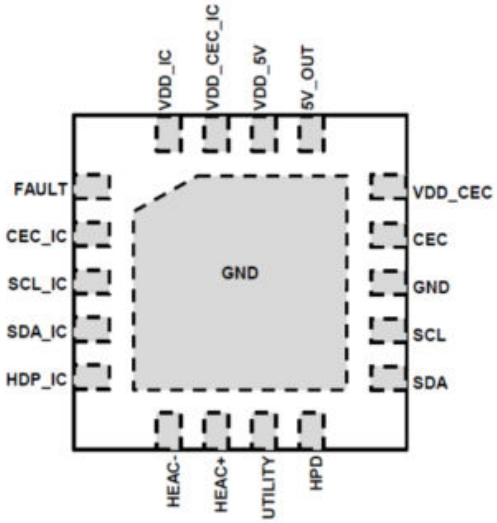


Figure 77. HDMI2C1-6C1 pin-out, top view



The active-low fault pin is used to indicate short circuit or over temperature protection activation on 5V_OUT pin.

The HDMI2C1-6C1 (Figure 77) pin-out provides an easy routing. The typical electrical schematic is given in Figure 78, a layout example in Figure 79.

Figure 78. HDMI2C1-6C1 electrical schematic

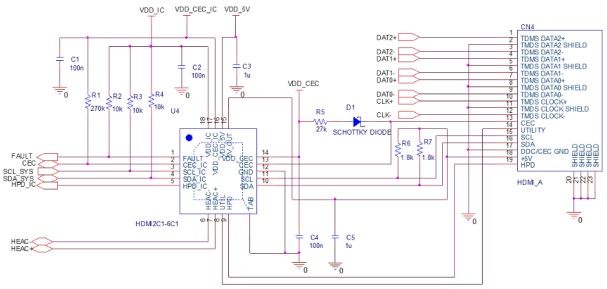
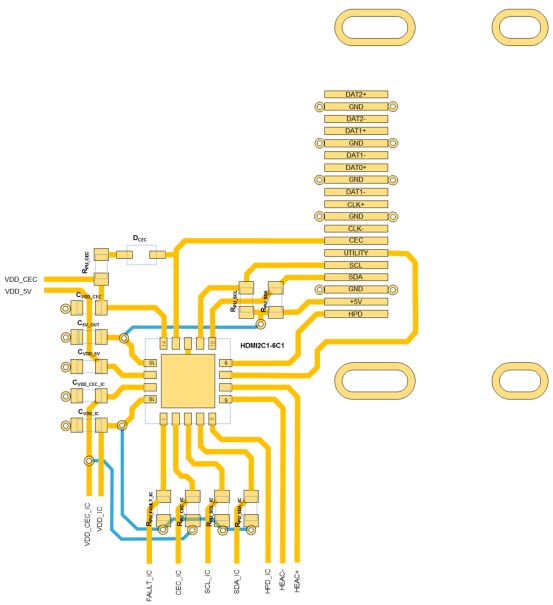


Figure 79. HDMI2C1-6C1 layout example



The HDMI2C1-6C1 is fully compliant with HDMI 1.4b standard requirements.

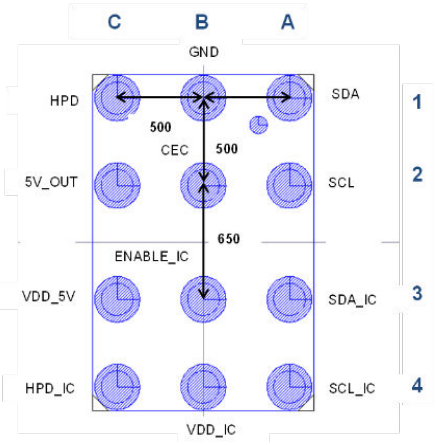
6.2.1.2 *HDMI2C4-5F2*

HDMI2C4-5F2 provides ESD protection on all HDMI connector control pins, and integrates level shifter, signal conditioning, and dynamic pull-up on DDC pin in flip-chip package. It also integrates current limiter and short circuit protection on +5 V power pin.

HDMI2C4-5F2 is dedicated to HDMI source device.

Figure 80. HDMI2C4-5F2 package

Figure 81. HDMI2C4-5F2 pinout, bump side view



The ENABLE_IC pin is used to enable or disable level-shifters on DDC bus and on HPD line to reduce power consumption in standby mode. To set the ENABLE_IC pin to low level, disable all integrated level shifter and disconnect the 5V_OUT pin from VDD_5V.

HDMI2C4-5F2 provides ESD protection on CEC line without level shifting.

The typical electrical layout and an example of the layout are shown on Figure 82 and Figure 83.

Figure 82. HDMI2C4-5F2 electrical schematic

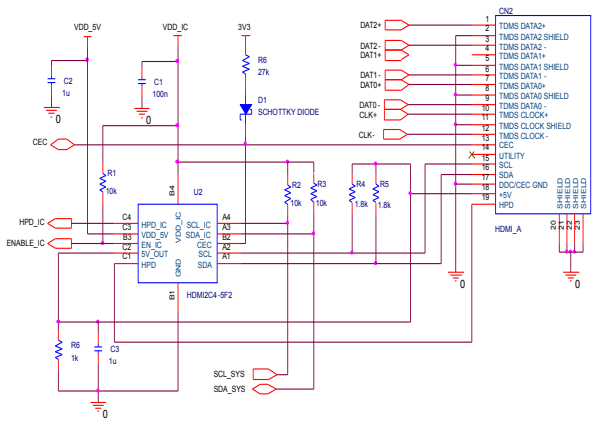
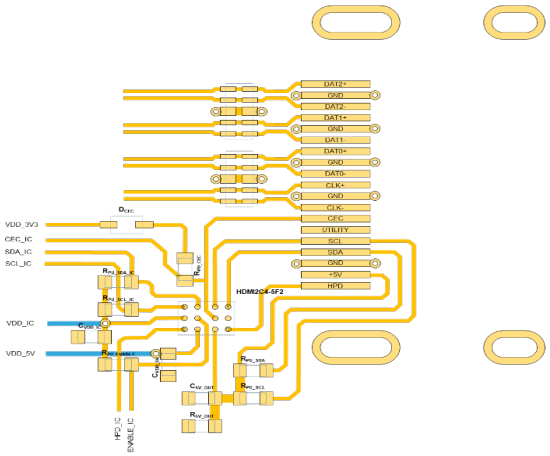


Figure 83. HDMI2C4-5F2 layout example



The HDMI2C4-5F2 is fully compliant with HDMI 2.1b standard requirements.

6.2.2 Full port protection

6.2.2.1 *HDMI2C1-14HDS*

HDMI2C1-14HDS provides ESD protection for all HDMI connector's pin and provides signal conditioning for control link of HDMI source in a single QFN 24 leads package with 500 µm pitch. It integrates current limiter and short circuit protection on the +5 V power pin.

HDMI2C1-14HDS is dedicated to HDMI source devices.

Figure 84. HDMI2C1-14HDS package

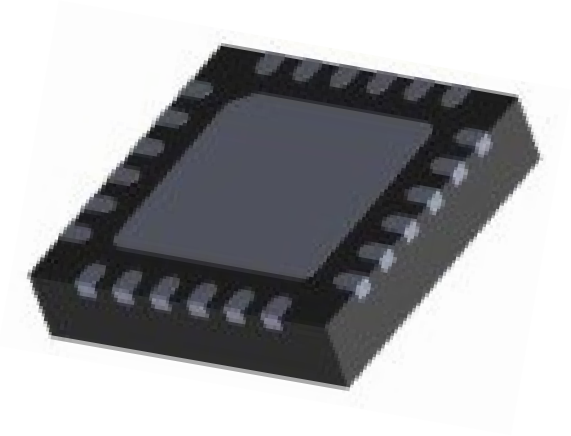


Figure 85. HDMI2C1-14HDS pin-out, top view

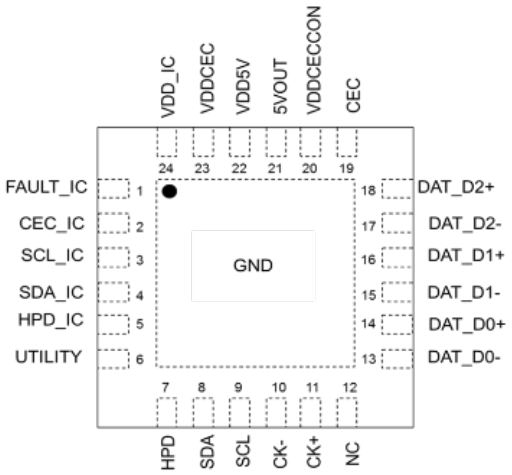
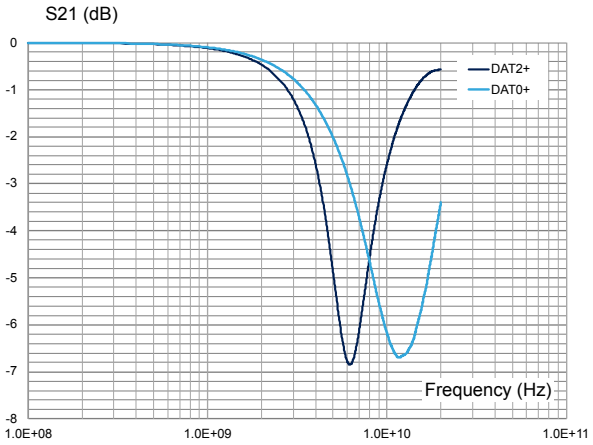


Figure 86. HDMI2C1-14HDS attenuation S21 typical value



Its high frequency bandwidth and low clamping voltage on TMDS lines ensure compatibility with the higher resolution of HDMI standard.

The eye diagrams shown on Figure 87 to Figure 90 highlight a very low impact on signal transmission ensuring a good signal integrity.

Figure 87. Eye diagram at 3.4Gbps, without HDMI2C1-14HDS

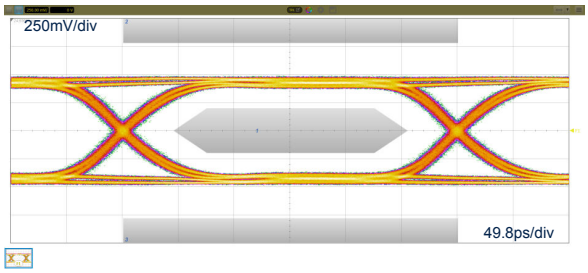


Figure 88. Eye diagram at 3.4Gbps, with HDMI2C1-14HDS

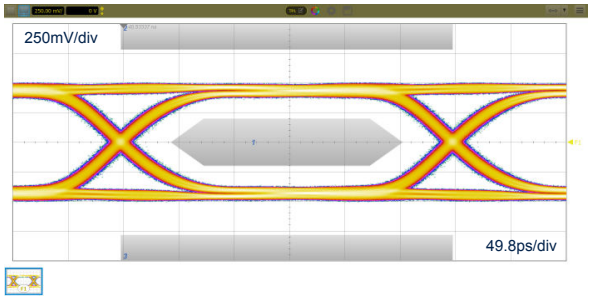


Figure 89. Eye diagram at 5.94Gbps, without HDMI2C1-14HDS

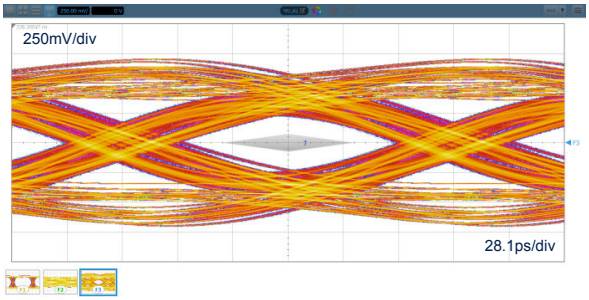
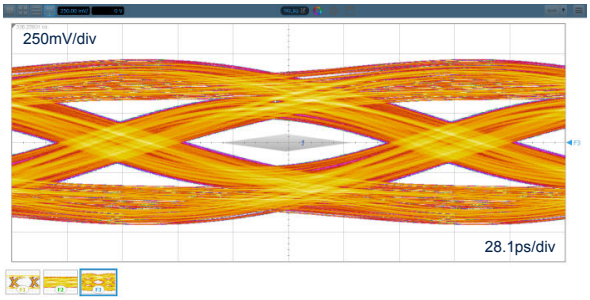


Figure 90. Eye diagram at 5.94Gbps, with HDMI2C1-14HDS



The active-low fault pin is used to indicate short circuit or over temperature protection activation on 5V_OUT pin. The typical electrical schematic is given in Figure 91.

Figure 91. HDMI2C1-14HDS electrical schematic

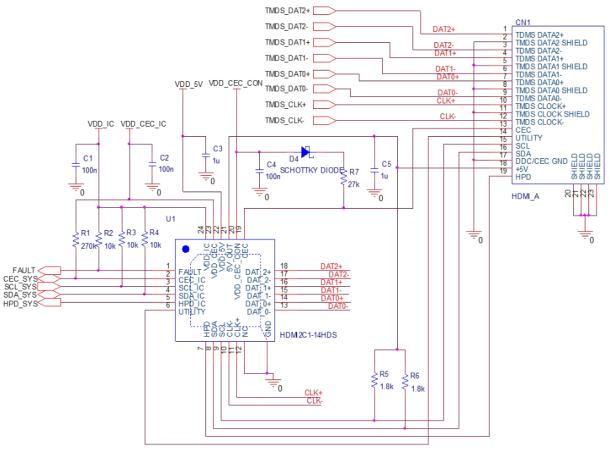
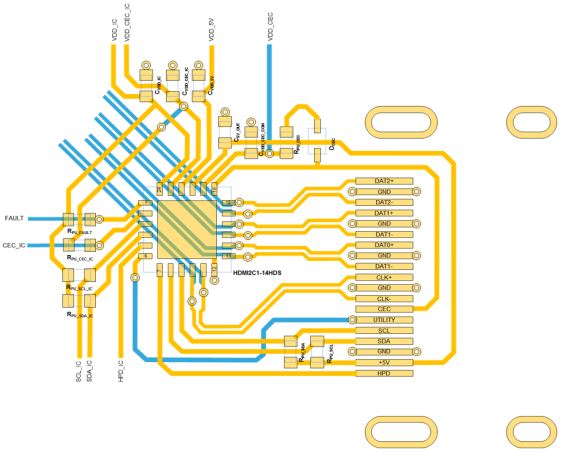


Figure 92. HDMI2C1-14HDS layout example



The HDMI2C1-14HDS is compliant with HDMI 1.4b standard requirements.

6.3 HDMI2Cx for HDMI sink device

6.3.1 Control lines: HDMI2C2-5F2

HDMI2C2-5F2 provides ESD protection on all HDMI connector control pin, and integrates level shifter, signal conditioning and dynamic pull-up on DDC pin in flip-chip package.

HDMI2C2-5F2 is dedicated to HDMI sink device.

Figure 93. HDMI2C2-5F2 package

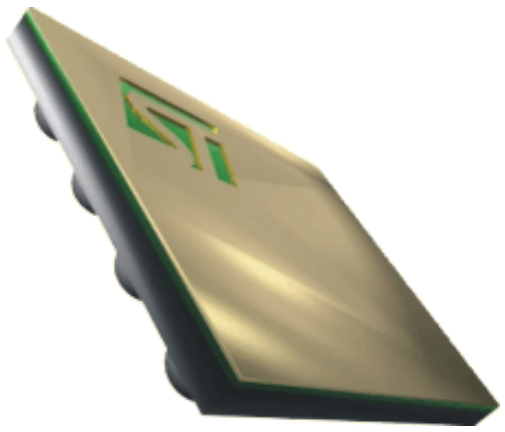
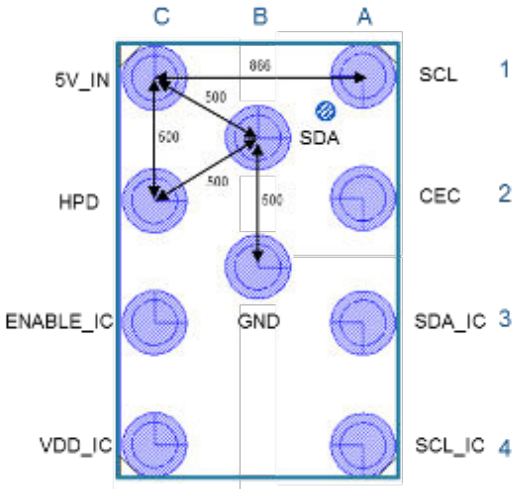


Figure 94. HDMI2C2-5F2 pinout, bump side



The ENABLE pin allows to sense the +5 V power pin and/or to disable HDMI2C2-5F2 to reduce power consumption in standby mode. Setting the ENABLE_IC pin to low level disable all integrated level shifter and disconnect the 5V_OUT pin from VDD_5V.

The typical electrical schematic is given in Figure 95, a layout example in Figure 96.

Figure 95. HDMI2C2-5F2 electrical schematic

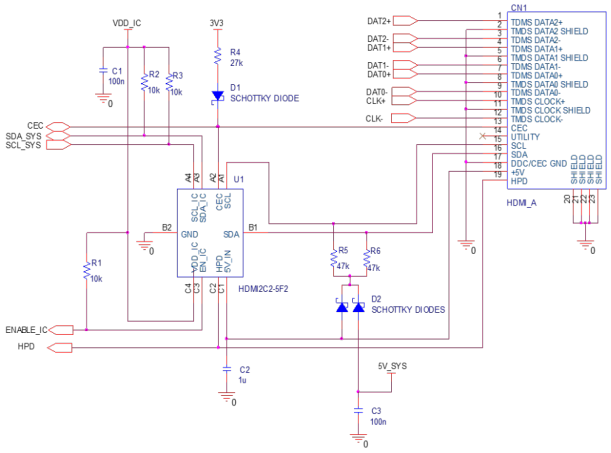
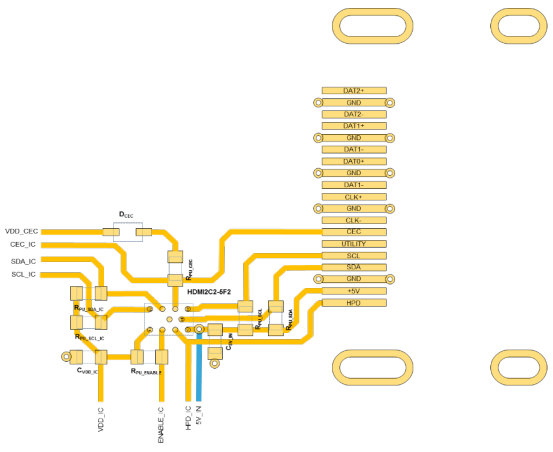


Figure 96. HDMI2C2-5F2 layout example



The HDMI2C2-5F2 is fully compliant with HDMI 2.1 standard requirements.

7 Conclusion

Consumer applications as Streaming boxes, Game console, Tablet, HDMI stick, Notebook and PC graphic cards shall fulfill EMC requirements as described in CISPR20/EN55020 or CISPR24/EN55024. In particular, an ESD robustness test performed on the HDMI port.

An HDMI port is composed of several links with different electrical characteristics introducing specific constraints on ESD protection devices.

This application note presents STMicroelectronics offer for HDMI port: Standalone ESD protection and common-mode filter with ESD protection for TMDS lines and ESD protection with signal conditioning for control lines or for the whole HDMI port. The high frequency bandwidth of ESD protection and common-mode filter with ESD protection for TMDS lines ensure a low impact of the protection device on signal integrity. The signal conditioning and the dynamic pull-up on the DDC bus help the system to drive high capacitive cable while respecting the standard requirements.

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
04-Dec-2017	1	Initial release.
19-Nov-2024	2	Document reworked to improve readability. No content changes.

Contents

List of tables

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