AN5128

Application note

STSPIN32F0/F0A/F0B and STSPIN32G0A1/A2/B1/B2 - Buck converter

Introduction

The STSPIN32F0 and STSPIN32G0 low voltage family devices are systems in package providing a complete solution for 3-phase brushless motor driving applications.

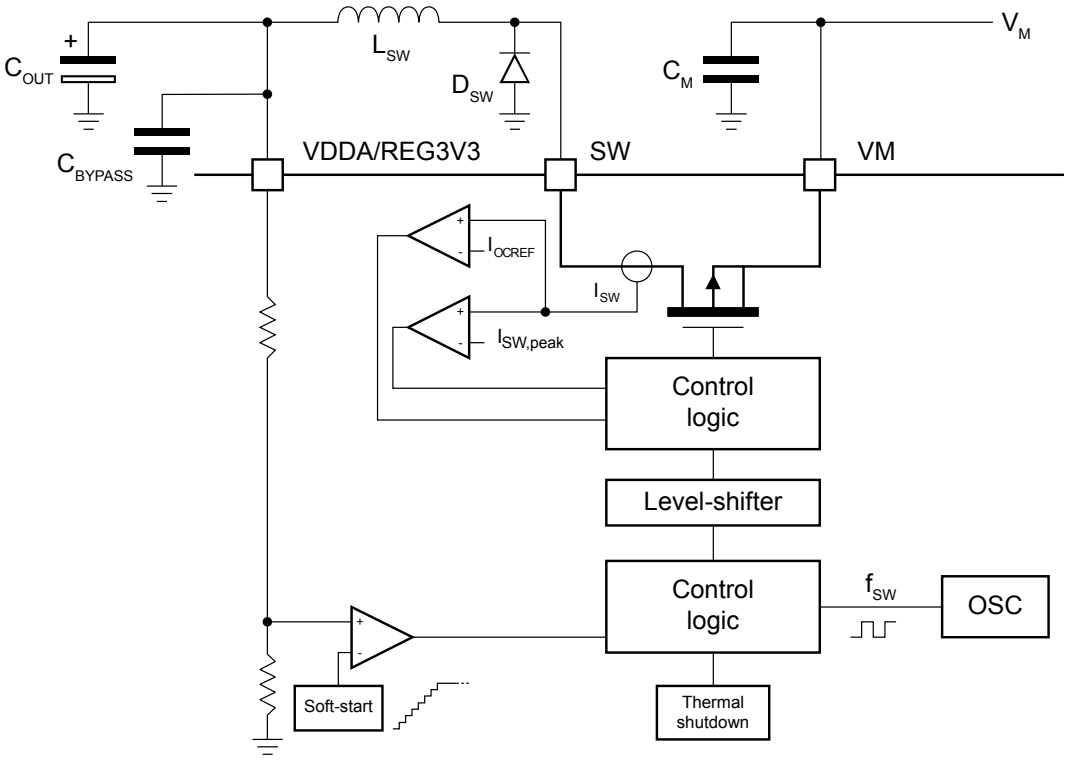
One of the blocks embedded into the devices is a DC/DC buck converter generating a 3.3 V voltage starting from the motor supply.

This document describes in details the operation of the DC/DC buck converter and provides recommendations about the layout and the selection of the discrete components.

1 Operating principle

The buck converter embedded into the STSPIN32F0 and STSPIN32G0 family devices is based on hysteretic control. When the feedback voltage of the DC/DC regulator — that is VDDA in the STSPIN3F0 family and REG3V3 in the STSPIN32G0 family — is below the target value, the integrated PMOS connects the SW pin to the VM supply charging the output inductor up to $I_{SW,peak}$ = 320 mA (typ.), then the PMOS is turned off and the inductor current recirculates through the external diode.

Figure 1. DC/DC converter block diagram

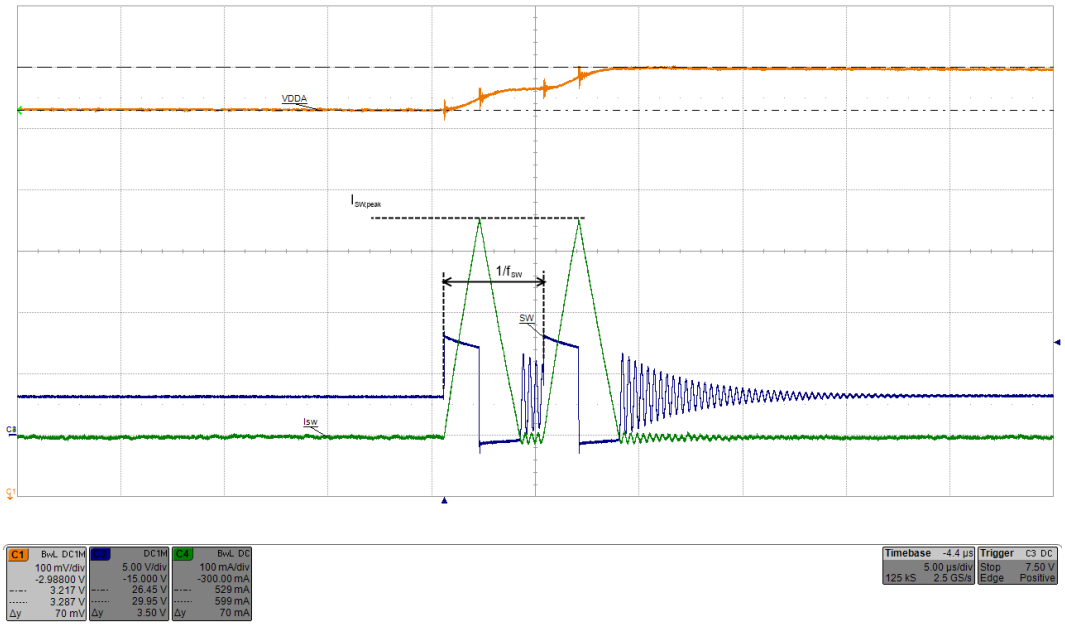


The controller generates a new SW pulse with a frequency of f_{SW} = 200 kHz (typ.) until the output voltage reaches the target value (3.3 V nominal).

When target has been reached, no more pulses are generated until the output voltage drops below the hysteresis of the feedback comparator.

The hysteretic control allows high stability to the variation of external components and input voltage, keeping the ripple on the output voltage constant and equal to the hysteresis of the feedback comparator.

Figure 2. DC/DC converter waveforms (V_M = 8 V - STSPIN32F0)



1.1 Overcurrent protection

The buck converter integrates protection against the overcurrent or short-circuit of the SW pin. The protection monitors the drop between VM and SW pins detecting anomalous load conditions of the integrated PMOS; when the drop exceeds a safety threshold, the DC/DC regulator is immediately disabled.

The device returns operative only applying a power-cycle on the VM pin, i.e. the supply must be removed and then applied again.

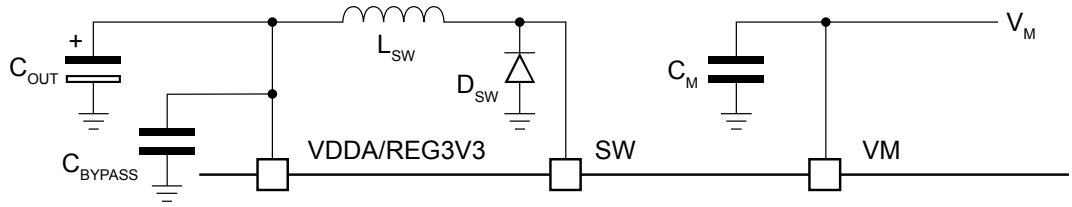
2 Selection of external components

The buck regulator requires some external components. Following the typical application description in Table 1 and Figure 3.

Table 1. Typical application BOM - DC/DC converter

Part	Value
C_M	10 µF
D_{SW}	STPS0560Z
L_{SW}	22 µH
C_{BYPASS}	100 nF
C_{OUT}	47 µF

Figure 3. Typical application schematic - DC/DC converter



2.1 Input capacitor (C_M)

The input capacitor should be a low ESR ceramic capacitor of at least 10 µF. It must be positioned as near as possible to the VM pin. A second 100 nF ceramic capacitor can be put in parallel in order to reduce the equivalent ESR.

Low ESR is an important requirement because this capacitor will filter the current spikes coming from the commutations of the DC/DC regulator MOSFET. A poor capacitor with poor ESR or a bad layout could cause ringing on the VM supply and cause the triggering of the OC protection (see Section 1.1: Overcurrent protection).

More details on the layout can be found in Section 3 of this document.

2.2 Diode (D_{SW})

The external diode is required to allow recirculation of the inductor current when the embedded PMOS is turned off.

Key characteristics of the diode are:

- Forward voltage drop (V_F)
- Maximum repetitive reverse voltage (V_{RRM})
- Maximum non-repetitive peak forward current (I_{FSM})
- Maximum average forward current ($I_{F(AV)}$)

A low forward drop voltage reduces the dissipation in the diode during recirculation and improves the efficiency, for this reason a low drop power Schottky diode is recommended.

The V_{RRM} must be greater than the V_M supply voltage. Usually a margin of 20% is considered when this component is selected:

Equation 1

(1)

$$V_{RRM} \times 80\% \geq V_M$$

The I_{FSM} is the maximum current the diode can sustain during forward bias condition and it must be greater than the $I_{SW,peak\ value}$. The minimum recommended value is 1 A.

The $I_{F(AV)}$ is the average current flowing into the diode (in forward direction) during the operation and its maximum value is limited by the power dissipation. For this reason, the $I_{F(AV)}$ decreases with ambient temperature.

The average current flowing into the diode during the operation of the buck converter can be estimated starting from the output current of buck regulator according to the following formula:

Equation 2

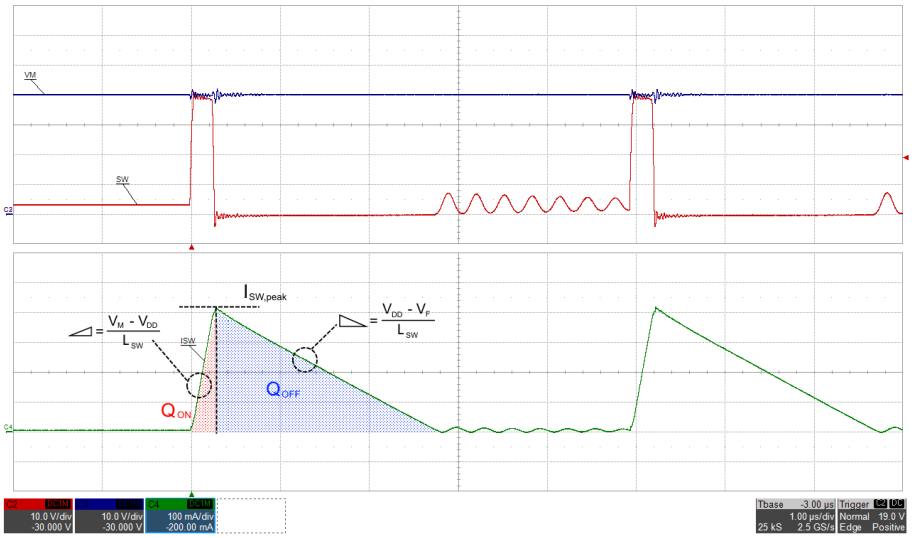
(2)

$$\frac{I_{F(VA)}}{I_{DD}} = 1/\left(1 + \frac{Q_{ON}}{Q_{OFF}}\right) = 1/\left(\frac{V_{DD} - V_F}{V_M - V_{DD}}\right) = \frac{V_M - V_{DD}}{V_M - V_F}$$

Where VDD is the output voltage of the regulator (3.3 V nominal).The formula is obtained considering that the output current is proportional to the total charge provided to the output capacitor through the inductor (Q_{TOT}) and the current flowing into the diode is proportional (in the same way) to the charge provided by the inductor during the discharging phase only (Q_{OFF}).

The total charge Q_{TOT} is represented by the area below the inductor current during a single DCM pulse as shown in Figure 4. It is the sum of the area during the charging phase (Q_{ON}) and discharging phase (Q_{OFF}).

Figure 4. Q_{ON} and Q_{OFF}



Equation 3 and Equation 4 approximate the Q_{ON} and Q_{OFF} values and are used to obtain the relation in Equation 2.

Equation 3

(3)

$$Q_{ON} = \frac{1}{2} \times I^2_{SW,peak} \times \frac{L_{SW}}{V_M - V_{DD}}$$

Equation 4

(4)

$$Q_{OFF} = \frac{1}{2} \times I^2_{SW,peak} \times \frac{L_{SW}}{V_{DD} - V_F}$$

2.3 Inductor (L_{SW})

The recommended value of the inductor is 22 µH and the saturation current must be greater than the regulator peak current $I_{SW,peak}$.

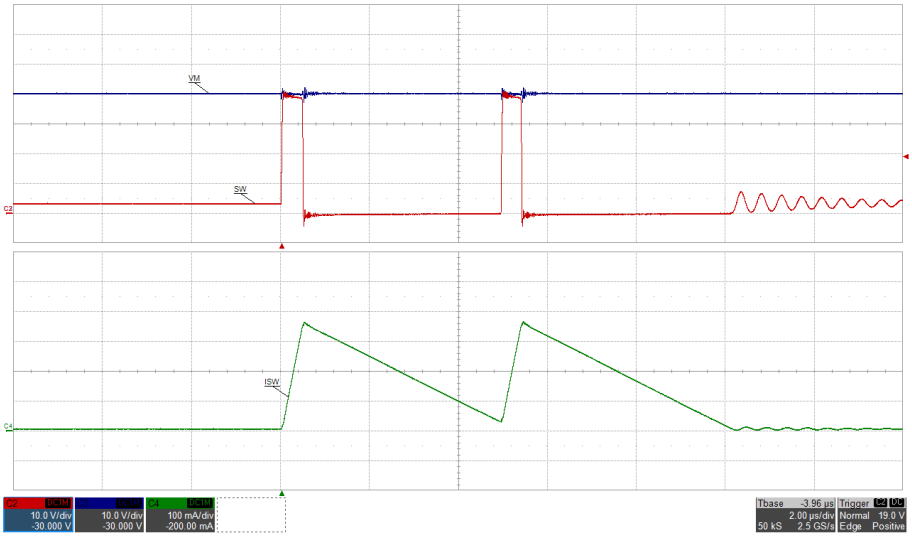
From the power dissipation point of view, the r.m.s. current flowing into the inductor is equal to the output current of the regulator.

When a higher inductor value is used (see Figure 5), the buck regulator could start operating in CCM mode. This operation mode increases the impact of the parasitic effects on the VM pin because

- The turn-on of the integrated PMOS is not performed at the 0 current, so a strong dI/dt is present on the VM-SW path.
- At the turn-on of the integrated PMOS the external diode is turned off and the recovery current pulse flows into the VM-SW path.

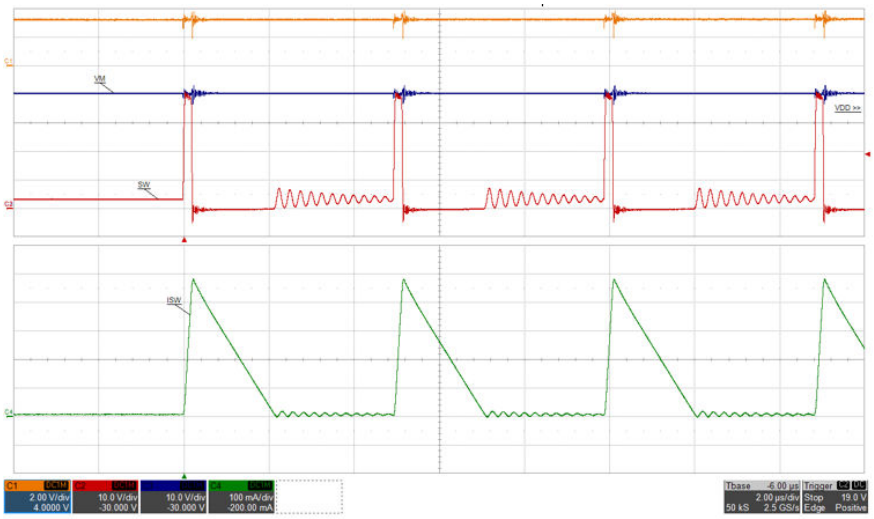
Both these events stimulate the parasitic inductor on the VM-SW path (PCB traces, internal bondings of the device, etc.) introducing a drop that could cause spurious OC detection.

Figure 5. **Operation with 47 µH**



When a lower inductor value is used (see Figure 6), the total charge provided by each DC/DC converter cycle is lower. This implies more pulses are required to obtain the same output current and a lower maximum output current limit.

Figure 6. **Operation with 15 µH**



2.4 Output capacitor (C_{OUT})

The DC/DC regulator has been designed to operate with an output capacitor of at least 47µF and an ESR lower than 200 mΩ.

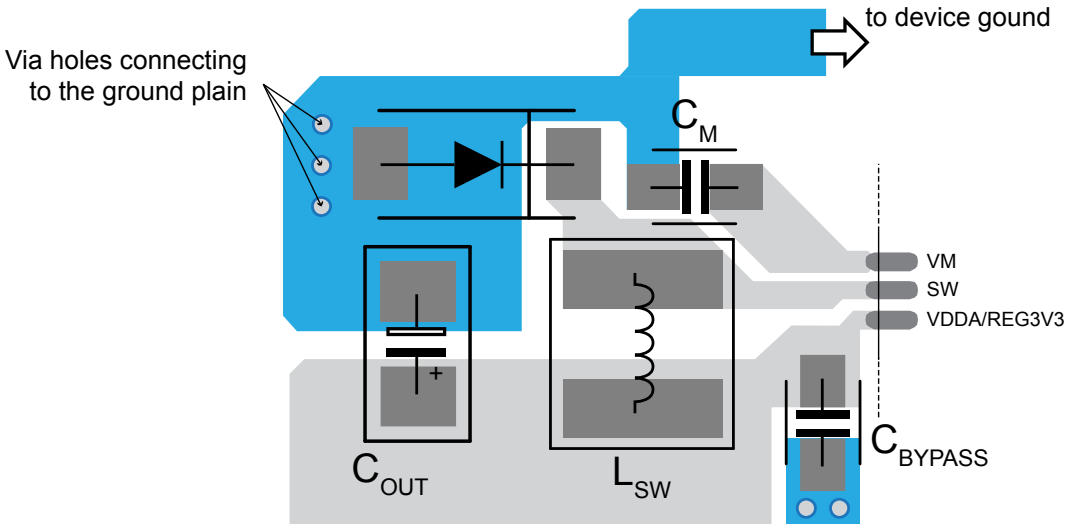
Considering the VDDA/REG3V3 pin is both the buck converter output and one of the device supply pins, it is recommended to place a 100 nF ceramic capacitor as near as possible to the pin (C_{BYPASS}).

3 Layout suggestions

For the layout of the DC/DC converter circuitry, the following recommendations should be considered

- Put the input capacitor C_M as near as possible to the VM pin.
- Directly connect the input capacitor C_M to the device ground avoiding long nets and via holes.
  If a short connection to the device ground is not possible using the top layer only, 2 or more via holes must be placed as near as possible to the capacitor to connect it to the ground plain. The ground plain must guarantee a direct connection to the device ground.
- Make the area of the ring composed by the recirculation diode, inductor (L_{SW}) and output capacitor (C_{OUT}) in order to reduce EMI emissions.

Figure 7. Recommended layout (top)



Revision history

Table 2. **Document revision history**

Date	Version	Changes
28-Feb-2018	1	Initial release.
27-Nov-2019	2	Added STSPIN32F0B RPN.
20-Jan-2025	3	Changed Figure 1, Figure 3 and Figure 7; changed title in cover page; changes to extend the AN to the STSPIN32G0 family.

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