AN5165
Application note

How to develop RF hardware using STM32WB microcontrollers

Introduction

STM32WB series microcontrollers integrate a high quality RF transceiver for Bluetooth® Low Energy and 802.15.4 radio solution.

Special care is required for the layout of an RF board, compared to a conventional circuit.

At high frequencies copper interconnections (traces) behave as functional circuit elements, introducing disturbances that can degrade RF performance. Parasitic components created by traces and pads contribute significantly to the overall circuit behavior. Layout rules must be carefully followed to mitigate these effects and achieve the requested performance.

This document describes the precautions to take to achieve the best performance from the MCU. These guidelines are generic, they need to be adapted to the specific application. The description is based on the QFN48 / QFN68 / UFBGA129 reference boards for 2-layer PCBs, and on the WLCSP100 reference board for the 4-layer PCB.

For some products of the STM32WB series only the QFN48 is available, check the product datasheet available on *www.st.com*.

Contents

List of tables

List of figures

1 RF basics

This section covers generic terms and definitions used in RF board design.

The following references can help the user.

1	Paul Horowitz and Winfield Hill	The art of electronics (3rd edition)	Cambridge University Press
2	Roger C. Palmer	An introduction to RF circuit design for communication systems (2nd edition)	Newnes
3	Christopher Bowick	RF circuit design (2nd edition)	Newnes
4	Joseph J. Carr and George W. Hippisley	Practical antenna handbook (5th edition)	McGraw-Hill Education
5	Smith chart (free SW)		http://www.fritz.dellsperger.net
6	Coplanar waveguide calculator (free SW)		http://wcalc.sourceforge.net

1.1 Terminology

1.1.1 Power

This unit, expressed in dBm, is the measure of the RF signal strength: **dBm = 10 Log P**, where P is the power in mW:

- 1 pW = -90 dBm
- 10 µW = -20 dBm
- 1 mW = 0 dBm
- 2 mW = 3 dBm
- 10 mW = 10 dBm

1.1.2 Gain

The gain (expressed in dB) is the ratio between the output and the input power of an RF device. Negative values correspond to attenuation.

1.1.3 Loss

If there is impedance mismatch, incorrect transmission line design or incorrect PCB material selection between two stages of a circuit, signal power losses appear and not all the power is transmitted from one stage to the following one. There are also inherent losses, such as , the dielectric loss, which depends upon the laminate and materials used to manufacture the board.

1.1.4 Reflection coefficient, voltage standing wave ratio and return loss

When a signal flows from a source to a load via a transmission line, a mismatch between the characteristic impedance of the transmission line and the load results in a portion of the signal being reflected back to the source. The polarity and the magnitude of the reflected signal depend on whether the load impedance is higher or lower than that of the line.

The reflection coefficient (Γ) is the measure of the amplitude of the reflected wave versus the amplitude of the incident wave, namely $\mathbf{\Gamma = (Z - Z_0) / (Z + Z_0) = (z - 1) / (z + 1)}$.

The voltage standing wave ratio (VSWR) is the measure of the accuracy of the impedance matching at the point of connection. It is a function of the reflection coefficient and is expressed as $\mathbf{VSWR = (1 + |\Gamma|) / (1 - |\Gamma|)}$. If VSWR is 1, there is no reflected power.

The return loss (RL) is a function of the reflection coefficient, but expressed in dB: $\mathbf{RL = 20 \log |\Gamma|}$.

1.1.5 Harmonics

The harmonics are the integer unwanted multiples of the input frequency (fundamental frequency).

1.1.6 Spurious

The spurious are the non-integer multiples of input frequency (unwanted frequencies).

1.1.7 Intermodulation

When two RF signals are mixed together, intermodulation products are the signals composed by an integer multiple of the sum and the difference between the two signals.

1.2 Impedance matching

To optimize the RF performance, it is imperative to adapt the impedance matching from the antenna to the input of the chip, as well as that from the chip output to the antenna.

A poor adaptation introduces losses in the RX/TX chain. These losses immediately translate in lower sensitivity and in lower signal amplitude of the transmitted signal. These disadatpations, if high enough, increase the level of TX harmonics.

As a consequence it is very important to spend efforts to adapt as best as possible the RF chain. In the Bluetooth® Low Energy bandwidth of the STM32WB, and more generally in RF frequencies, spurious elements (such as PCB track inductances and layer capacitors, trace length) have a significant impact on the impedance matching. To achieve the best TX/RX budget (optimum transfer of signal and energy) between the load and the STM32WB, a dedicated matching network is needed between the two blocks.

The maximum power is transferred when the internal resistance of the source equals the resistance of the load. When extended to a circuit with a frequency-dependent signal, to obtain maximum power transfer the load impedance must be the complex conjugate of the source impedance.

1.3 Smith chart

The Smith chart (*Figure 1*) is used to determine the matching network.

1.3.1 Normalized impedance

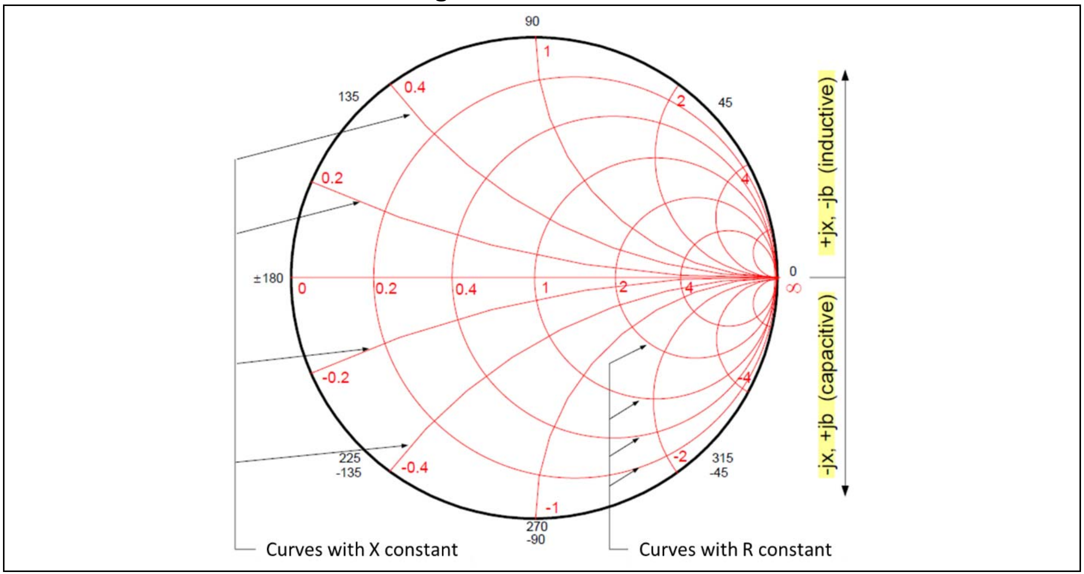
The normalized impedance z is a complex impedance (r is the real part and x the imaginary part): $\mathbf{z = r + jx = Z / Z_0}$ where Z_0 is the characteristic impedance and is often a constant (in our case Z_0 = 50 Ω).

For a capacitor z = - j / (2 π * f * C * Z_0), for an inductor z = j (2 π * f * L) / Z_0.

1.3.2 Reading a Smith chart

The Smith chart is represented with the normalized impedance scale z = Z / Z_0.

Figure 1. Smith chart



If Z_0 = 50 Ω, when there is matching (Z = Z_0) the normalized impedance at 50 Ω is 1 and it is the center of the Smith chart. The goal in the search of a matching network is to converge towards this point.

The horizontal axis of the Smith chart represents pure resistors: at the left side, z = 0 (short circuit) and at the right side, z = ∞.

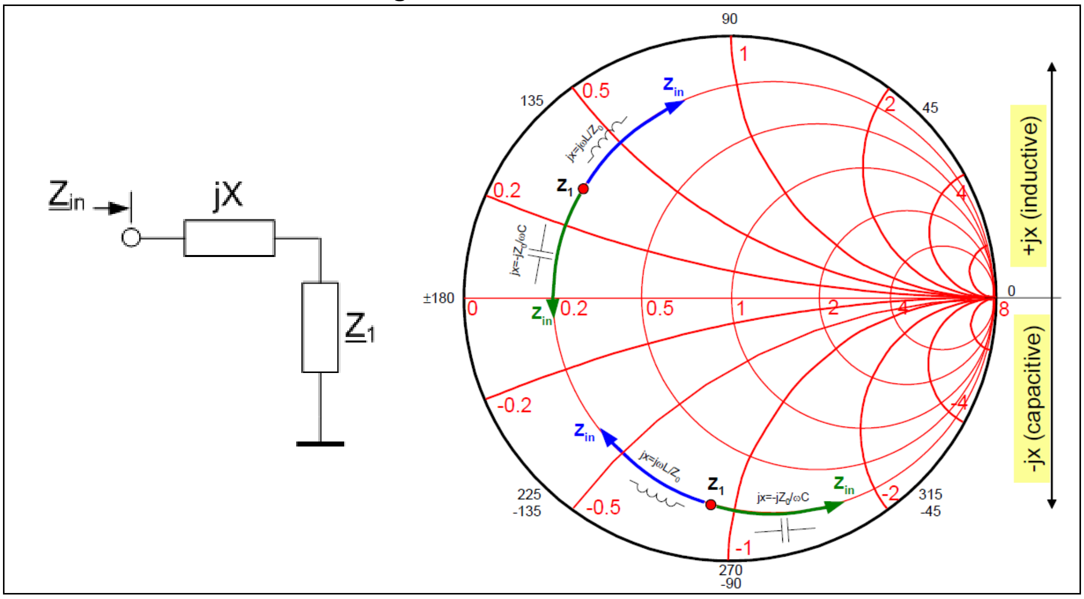
The region located above the X axis represents impedances with inductive reactance (positive imaginary part of the complex impedance) or capacitive susceptance (positive imaginary part of the complex admittance).

The region below the X axis represents impedances with capacitive reactance (negative imaginary part of the complex impedance) or inductive susceptance (negative imaginary part of the complex admittance).

Serial inductor or capacitor

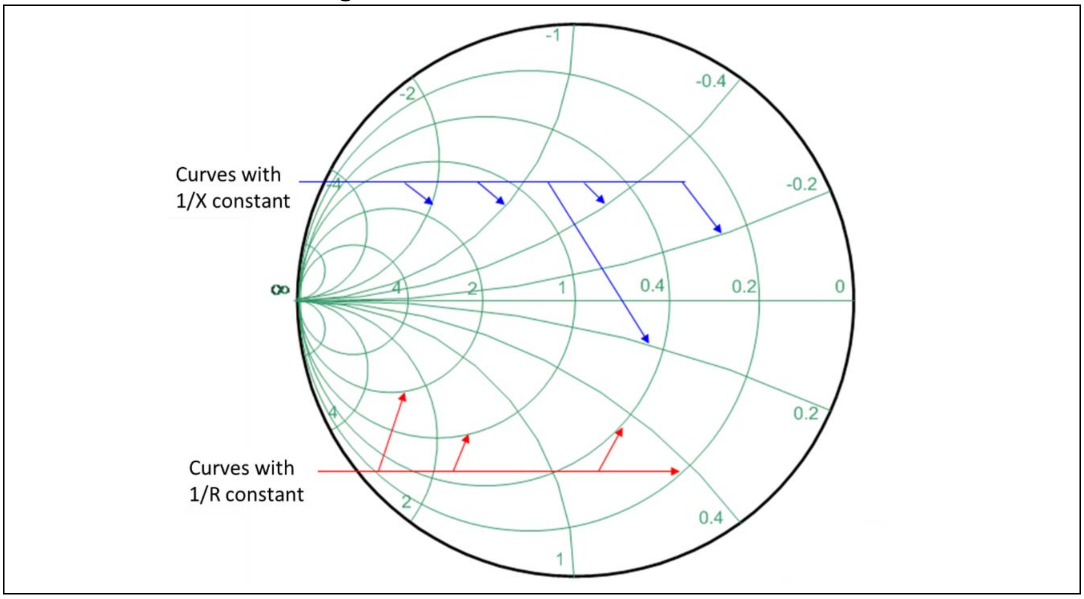
If an inductor or a capacitor is in series with the load impedance Z_1 the resulting impedance Z_{in} moves as shown in *Figure 2*.

Figure 2. Series connection



The Smith chart can be represented in normalized admittance (y = 1/z) scale, as shown in *Figure 3*.

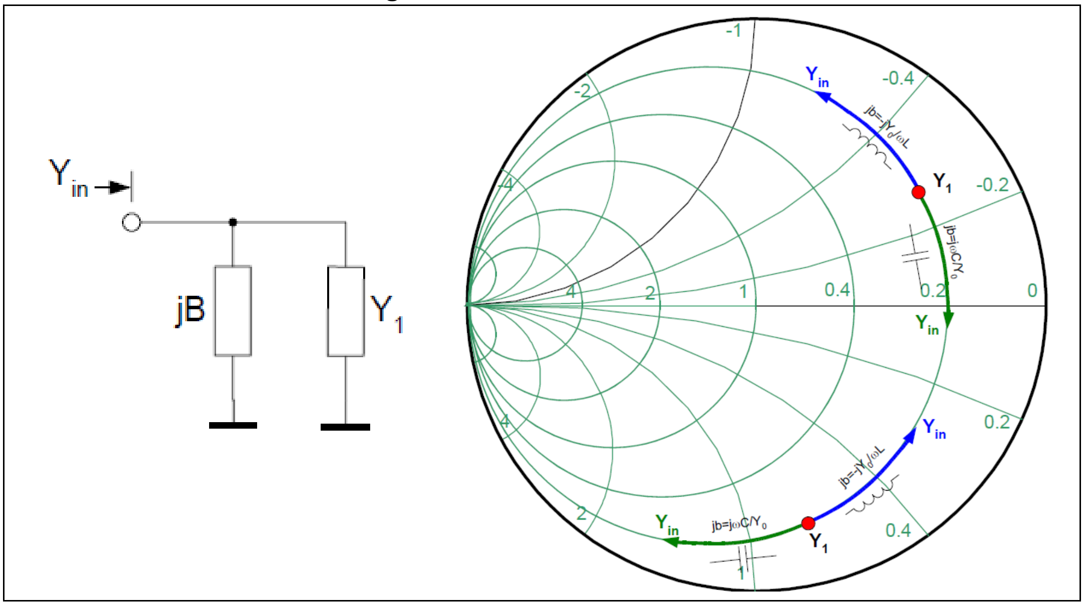
Figure 3. Smith chart for admittance



Parallel inductor or capacitor

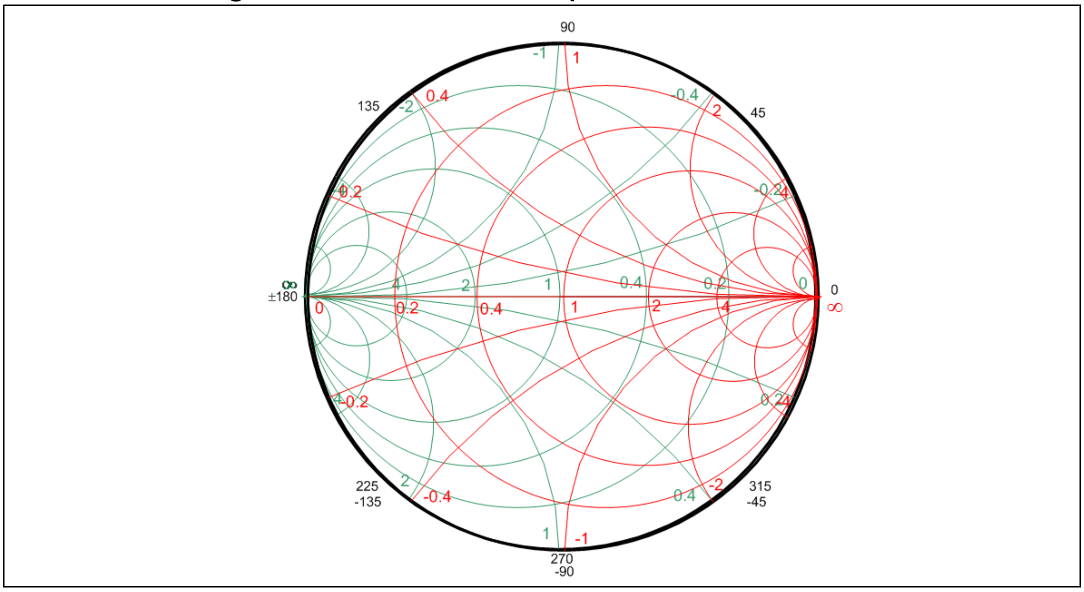
If an inductor or a capacitor is in parallel with the load admittance Y_1 the resulting impedance Y_{in} moves as shown in *Figure 4*.

Figure 4. Parallel connection



In *Figure 5* the Smith chart in impedance and admittance planes.

Figure 5. Smith chart with impedance and admittance



The circles with constant VSWR are additional information that can be retrieved from the Smith chart even when they are not represented. These circles have the same center, and as values the intersections between the circle and the right side of the horizontal axis from the center (see *Figure 6*).

Figure 6. Smith chart with VSWR circles

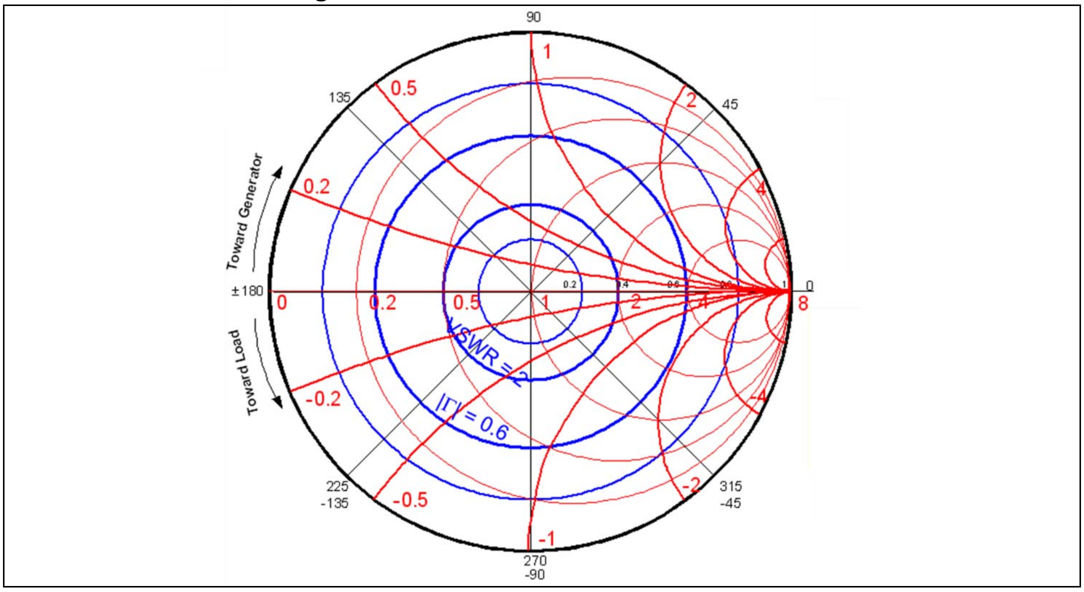
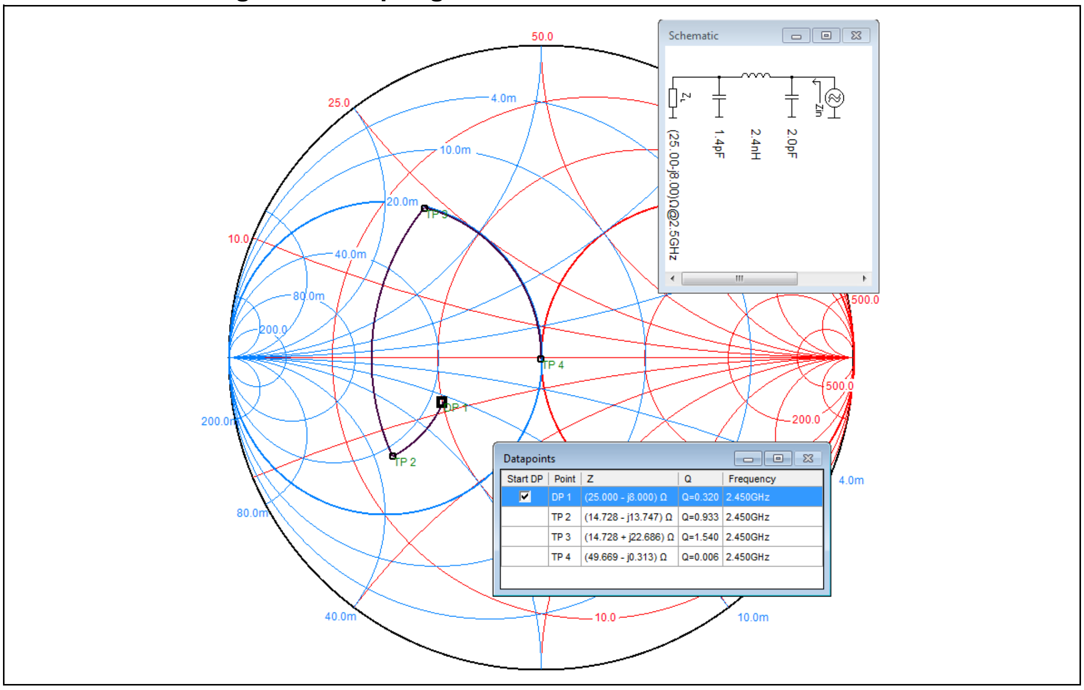


Figure 7 is an example of the free software “Smith”: starting from Z_L = (25.00 – j * 8.00) Ω represented on the Smith chart by DP1, the goal is to obtain Z_{in} = 50 Ω. By adding (in series or in parallel) inductors or capacitors, the impedance converges towards the center of the graph.

Figure 7. Adapting a network with the Smith free SW



2 Reference board schematics

The STM32WB series microcontrollers are based on Arm®[a] cores.

The schematics in *Figure 8*, *Figure 9* and *Figure 10* represent, respectively, the 2-layer reference boards for UFQFPN48, VFQFPN68, and UFBGA129 packages. *Figure 11* represents the 4-layer reference board for WLCSP100. The RF output is only from SMA. All the layout guidelines described in the next paragraphs for two-layer PCBs are based on these boards.

Table 1. External components

Component(s)	Description
C1, C2	Decoupling capacitors for V_{DDRF}
C3, C4	Matching capacitors
C5	Decoupling capacitor for NRST pin
C6, C7, C8, C9, C10	Decoupling capacitors for V_{DD}/V_{BAT}
C11, C12	Decoupling capacitors for SMPS
C13	DC-DC converter filtering capacitor
C15, C16	X2 capacitors
D1	Diode protection for NRST pin
FLT1	Integrated low-pass filter
L1	Matching inductor
L2, L3	DC-DC converter inductors
R1	Pull-up resistor for NRST
R2	Boot selector resistor
U1	STM32WBxx
X1	High frequency crystal
X2	Low frequency crystal

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Figure 8. UFQFPN48 reference board

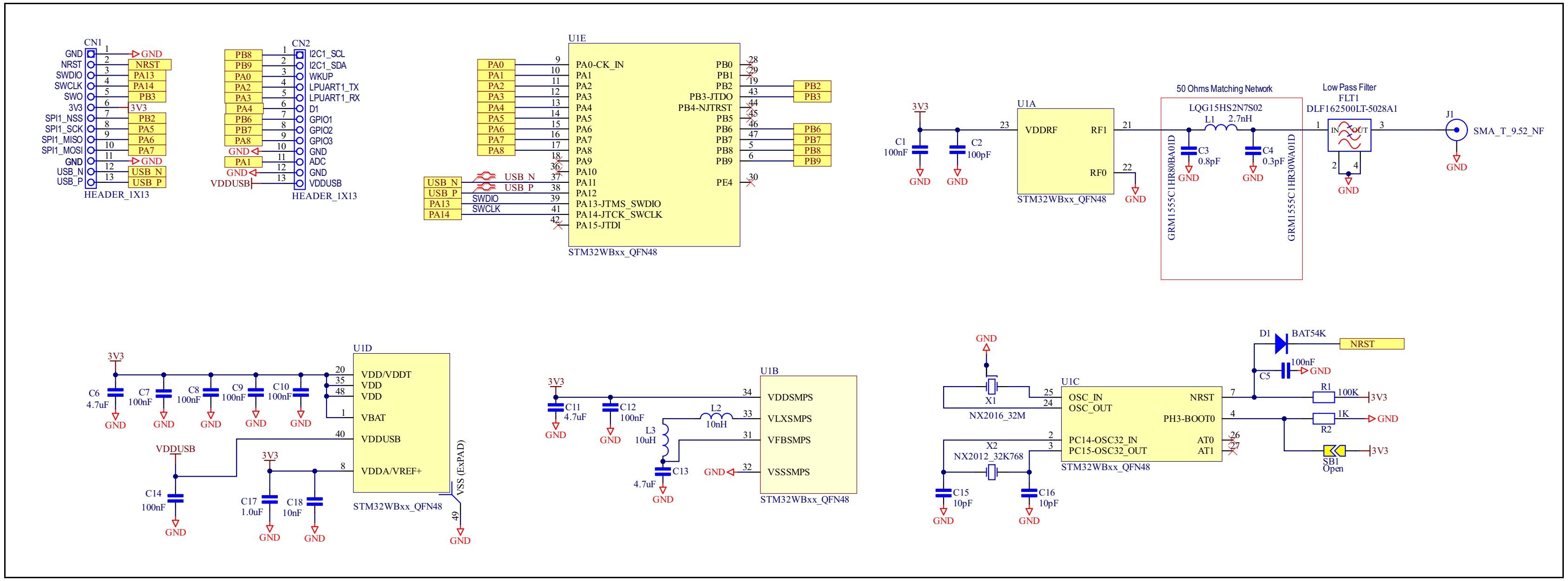


Figure 9. VFQFPN68 reference board

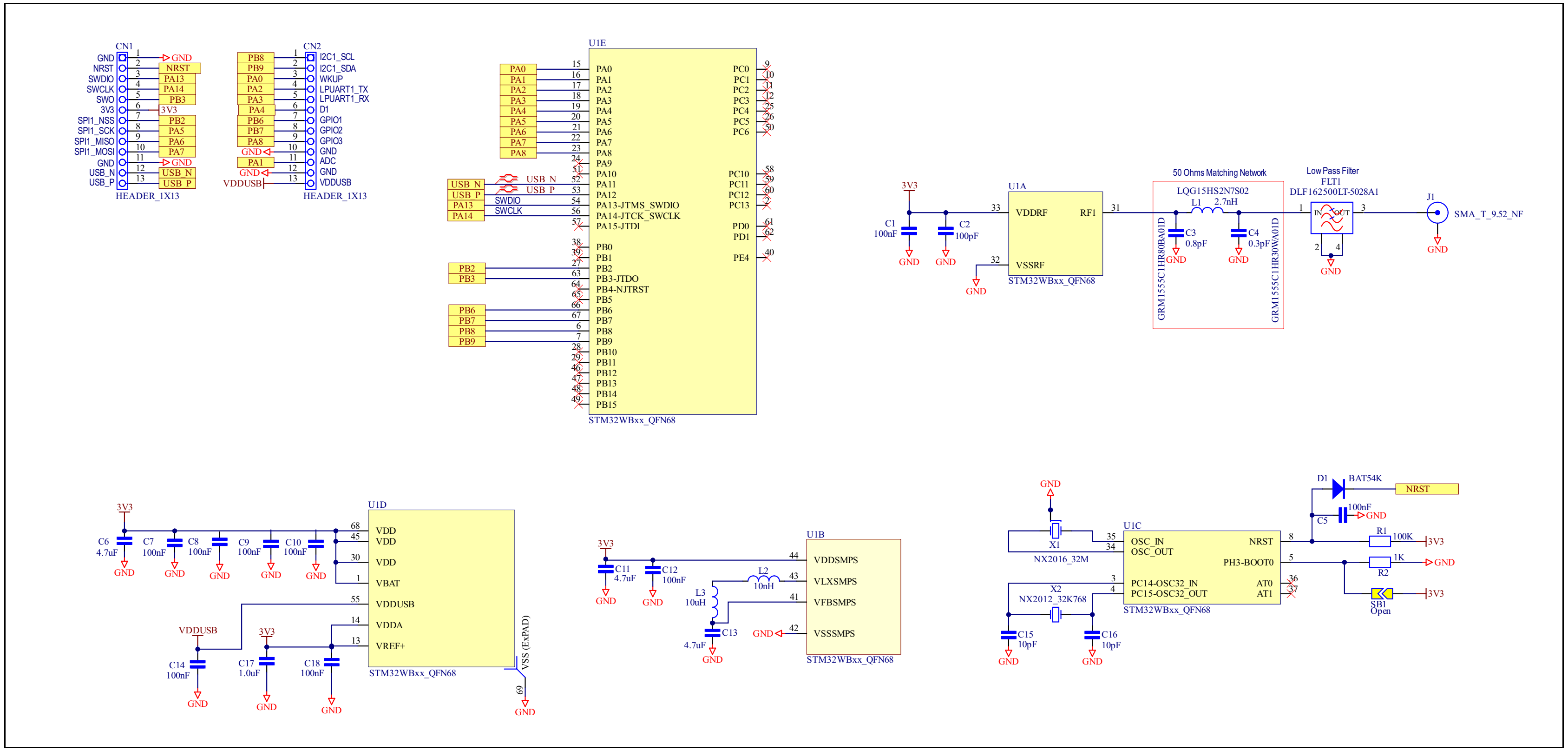


Figure 10. UFBGA129 reference board

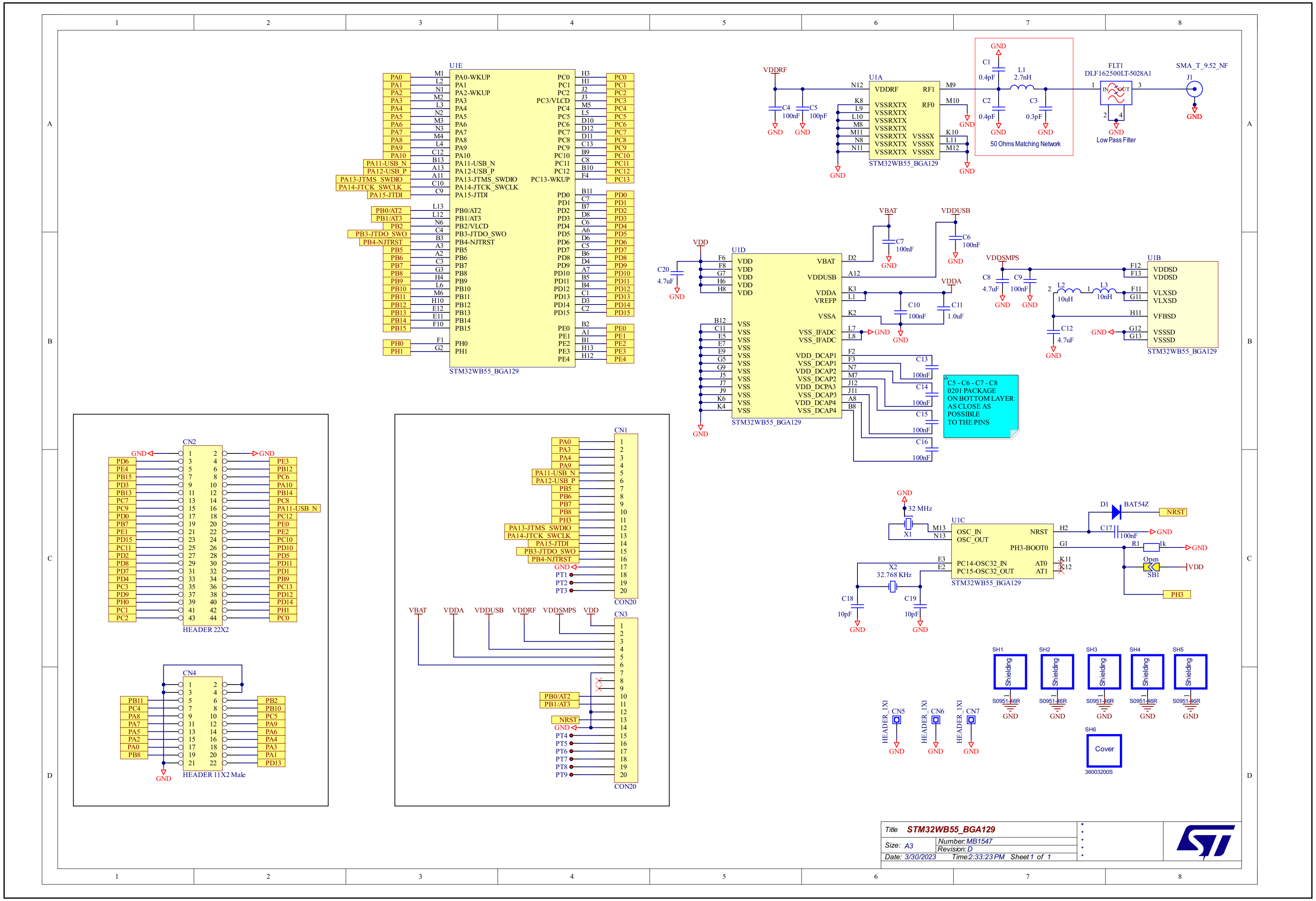
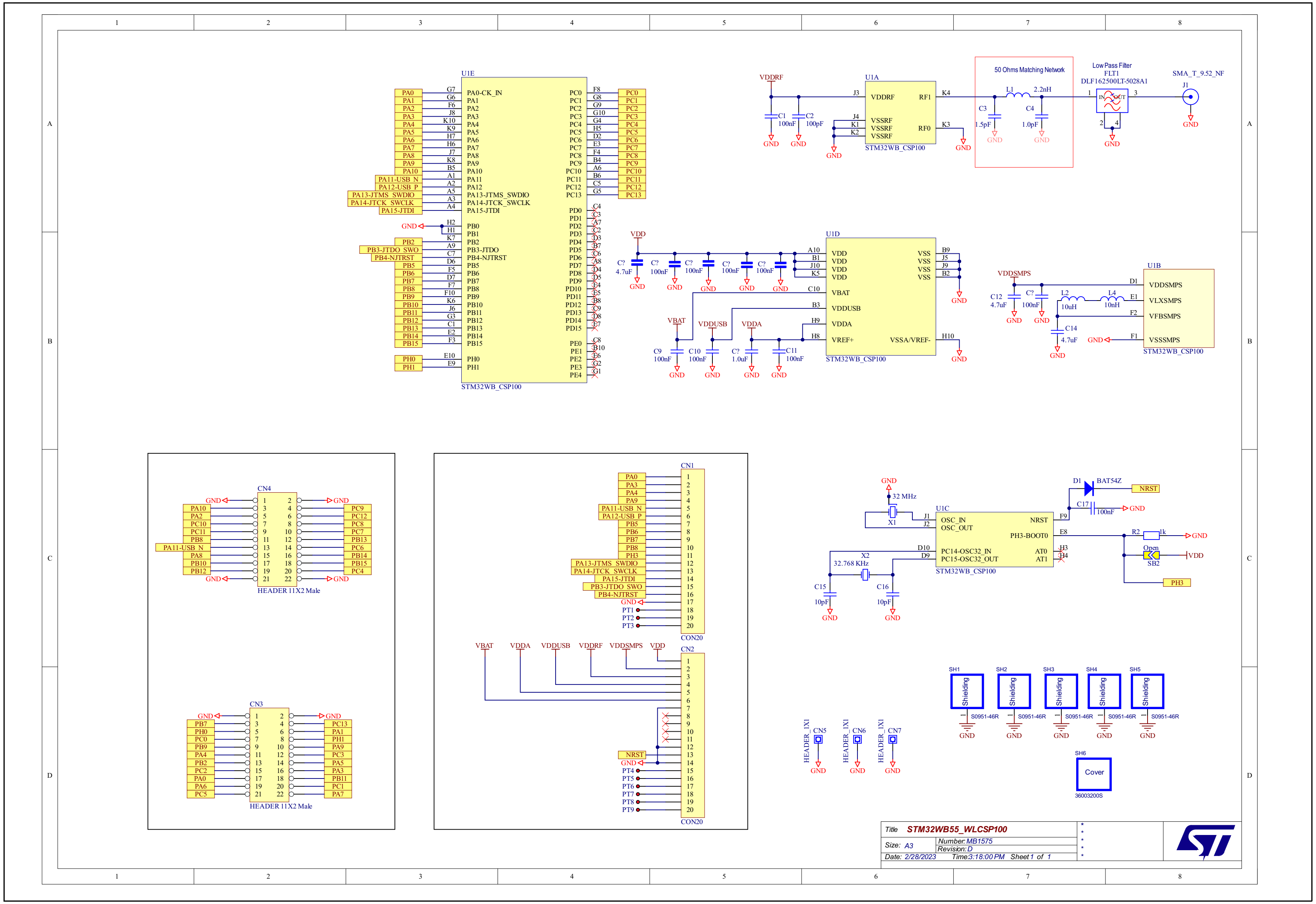


Figure 11. WLCSP100 reference board



3 Choosing the components

In the Bluetooth Low Energy bandwidth, and more generally at high frequencies, the choice of the external components is critical because they directly influence the performance of the application.

3.1 Capacitor

Capacitors are passive electrical components used to store energy in an electrical field. They are made with different construction techniques, materials (such as double-layer, polyester, polypropylene) and sizes. For RF design, it is recommended to use ceramic capacitors on surface mount version.

The equivalent circuit of a capacitor is represented in *Figure 12*. The resistor R_p represents its leakage current, while R_s is the equivalent serial resistor (ESR), representing all ohmic losses of the capacitor. The inductor L_s is the equivalent serial inductance (ESL), and its value is a function of the SRF (self-resonant frequency). From *Figure 13* it can be appreciated that the impedance of the capacitor is capacitive at low frequencies, at the SRF is resistive, and inductive at higher frequencies.

Figure 12. Capacitor equivalent circuit

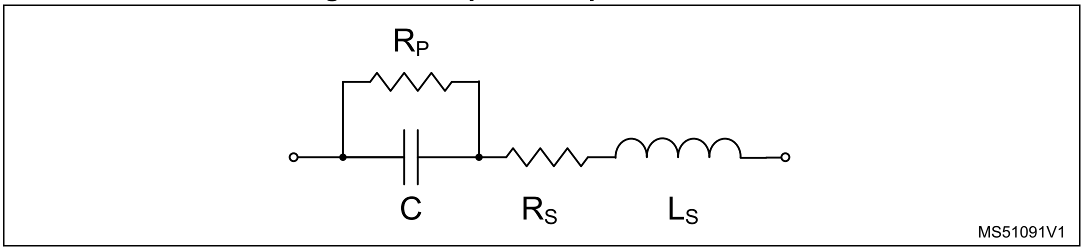
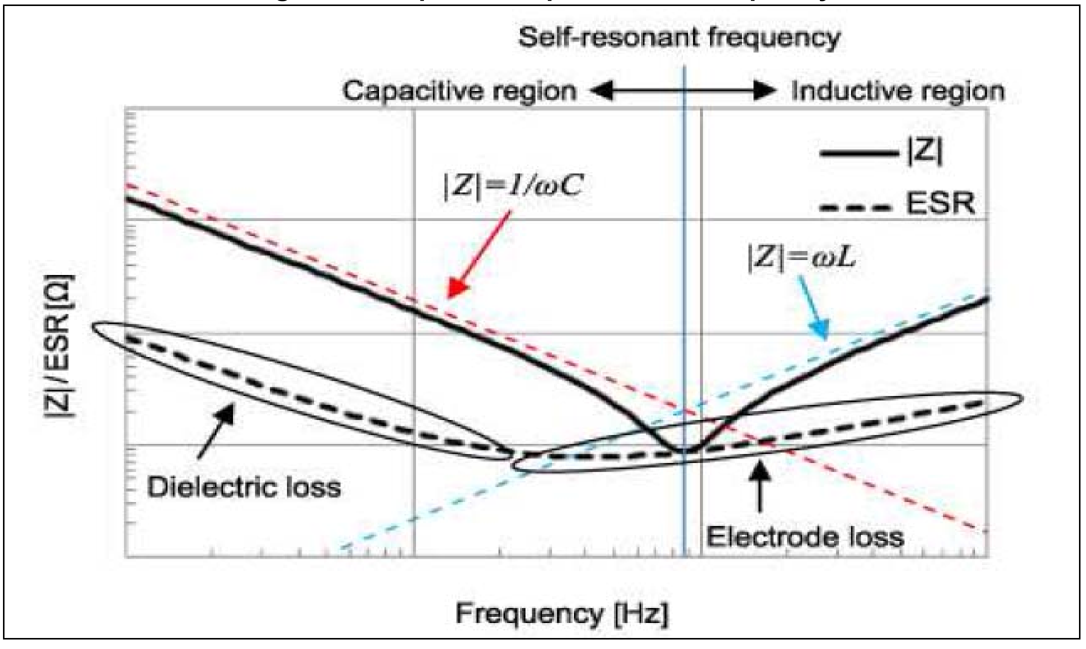


Figure 13. Capacitor impedance vs. frequency



For RF matching, multilayer ceramic capacitors offer linear temperature coefficients, low losses and stable electrical properties over time, voltage, and frequency. SMD (surface mount device) is used with a 0402 package, a good compromise between performance and handling.

For RF decoupling, the capacitance value must be chosen so that the frequency to be decoupled is close to or just above the self-resonant frequency of the capacitor.

For DC-DC converter, as the quality factor of a capacitor is inversely proportional to its ESR, a capacitor with low insertion loss and a good quality factor is recommended. The capacitor requires either an X7R or X5R dielectric.

Table 2. Capacitor temperature ranges

Minimum temperature		Maximum temperature		Variation over the temperature range	
Code	Temperature	Code	Temperature	Code	Variation (%)
X	-55 °C (-67 °F)	4	+65 °C (+149 °F)	P	±10
		5	+85 °C (+185 °F)	R	±15
Y	-30 °C (-22 °F)	6	+105 °C (+221 °F)	S	±22
		7	+125 °C (+257 °F)	T	+22 / -33
Z	+10 °C (+50 °F)	8	+150 °C (+302 °F)	U	+22 / -56
		9	+200 °C (+392 °F)	V	+22 / -82

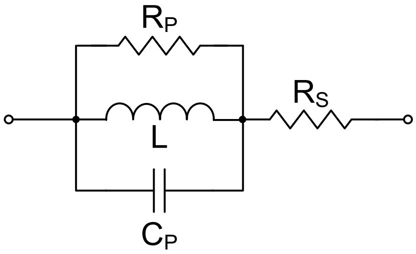
3.2 Inductor

An inductor is a passive electrical component used to store energy in its magnetic field. Inductors differ from each other for construction techniques and used materials.

For RF design, where a high Q (quality factor = Im[Z] / Re[Z]) is required to reduce insertion loss, it is generally recommended to use air core inductors. Those inductors do not use a magnetic core made of ferromagnetic material, but are wound on plastic, ceramic, or other nonmagnetic materials. SMD is also used with a 0402 package.

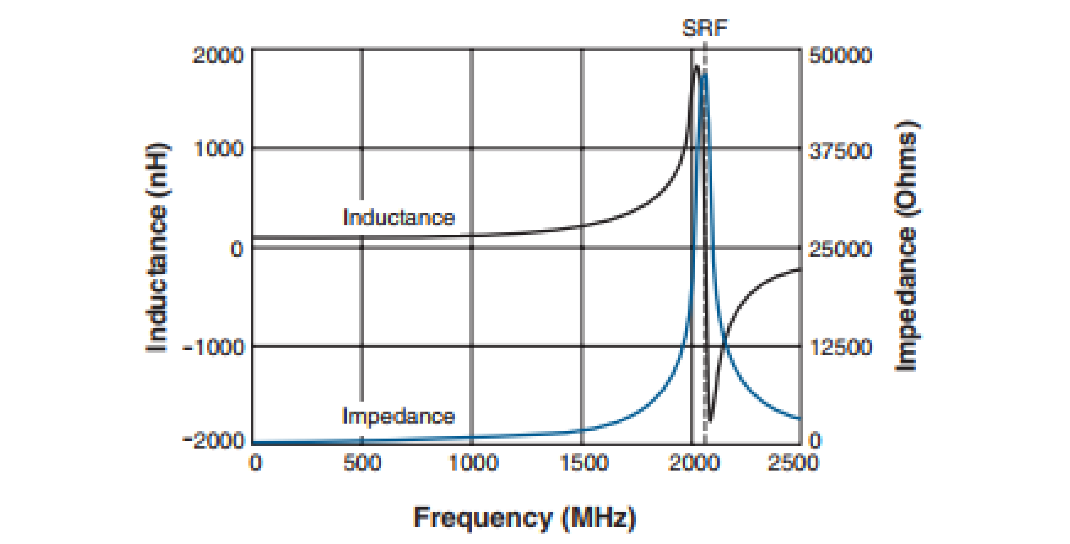
The equivalent circuit of an inductor is shown in *Figure 14*. The resistor R_s represents the losses due to the winding wire and terminations, its value increases with temperature. The resistor R_p represents the magnetic core losses, it varies with frequency, temperature and current. The capacitor C_p is associated with the windings.

Figure 14. Inductor equivalent circuit



As shown in *Figure 15*, at SRF the impedance and inductance are at their maximum. At lower/higher frequencies impedance and inductance increase/decrease with frequency.

Figure 15. Inductor impedance vs. frequency



For RF matching and decoupling, a good compromise between application cost and RF performance is to use an inductor with medium Q.

For DC-DC converter, the nominal value is 10 µH. The inductor value affects the peak-to-peak ripple current, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current.

It is important to use the components shown in the schematics to obtain the best RF performance with the given PCB layout of the reference boards.

3.3 SMPS

Some STM32WB microcontrollers (check the product datasheet available on *www.st.com*) embed an SMPS (switched-mode power supply) that can be used to improve power efficiency when V_{DD} is high enough.

In order not to disturb the RF performances, this SMPS has its switching frequency synchronous with the RF main clock source HSE. The allowed frequencies for the SMPS are 4 or 8 MHz. During RF startup phases from low power modes, the HSI is used, to allow a faster wake-up time compared to waiting from the HSE stabilization before starting the SMPS and the digital logic.

Two specific features have been added to this step down SMPS in association with all the low power modes supported by the STM32WB microcontrollers.

To operate properly the SMPS needs two inductors and two capacitors, whose values depend upon the targeted performance, and upon the PCB area and total height allowed in the mechanical design.

For best power performance, 4 MHz should be selected, leading to a 10 µH inductor associated with a 4.7 µF bulk capacitance. For smaller footprint, and especially to use very low profile inductor, the 8 MHz can be selected, making it possible to use a 2.2 µH inductor associated with a 4.7 µF bulk capacitance.

For all packages it is advised to add an extra 10 nH inductor in series with the 10 or 2.2 µH one, to filter the RF harmonic that can degrade the receiver performance.

Another 4.7 µF capacitor must be used to decouple the V_{DDSMPS} supply. All of these external components must have the lowest possible ESR values. Note that V_{DDSMPS} must be connected to V_{DD}, and that voltage rising and falling must satisfy the conditions described in the STM32WB datasheet.

3.4 External crystal

Two oscillators with external crystals are available on the STM32WB microcontrollers.

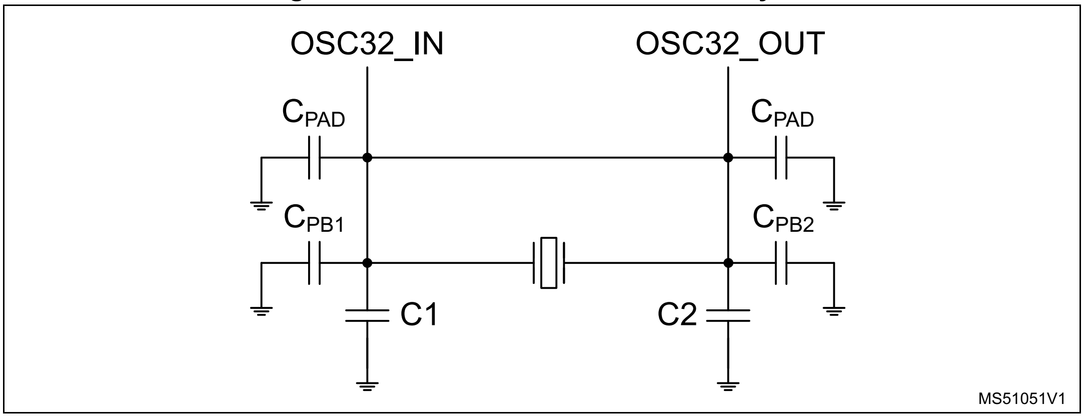
The HSE (high speed external) with 32 MHz frequency is used by the RF subsystem. The crystal X1 must be placed as close as po/ssible to pins OSC_IN and OSC_OUT, to minimize output distortion and startup stabilization time. The HSE with the frequency tolerance must be reached during the start time of the HSE, which is 1 ms. The load capacitances are integrated on chip and can be tuned according to the selected crystal via an internal register. By default, the load capacitances are 8 pF for the NX2016 from NDK used on the boards.

The LSE (low speed external) with 32.768 kHz frequency is used for the RTC subsystem. C_1 and C_2 must be tuned to meet to the recommended load capacitance C_0 of the selected crystal. Low power consumption and fast startup time are achieved with a low C_0 value. On the contrary, a higher C_0 leads to a better frequency stability.

With reference to *Figure 16*, the total load capacitance C_0 seen by the crystal is $C_0 = [(C1 + C_{PAD} + C_{PB1}) * (C2 + C_{PAD} + C_{PB2})] / (C1 + C_{PAD} + C_{PB1} + C2 + C_{PAD} + C_{PB2})$, where:

- C_{PAD} accounts for the parasitic capacitance of the STM32WB pads, of the SMD components C_1 and C_2, and of the crystal itself.
- C_{PB1} and C_{PB2} represent the PCB routing parasitic capacitances. They must be minimized by placing X2, C1, and C2 close to the chip, thus improving the robustness against noise injection.
- C1 and C2 must be connected to ground by a separate via.

Figure 16. Connection of an external crystal



4 PCB stack and technology

PCB traces at RF frequencies have to be designed carefully because their length is a fraction of the signal wavelength. Furthermore, the impedance of a PCB trace at RF frequencies depends upon the thickness of the trace, its height above the ground plane, and the dielectric constant and loss tangent of the PCB dielectric material. Another important parameter is the PCB stack.

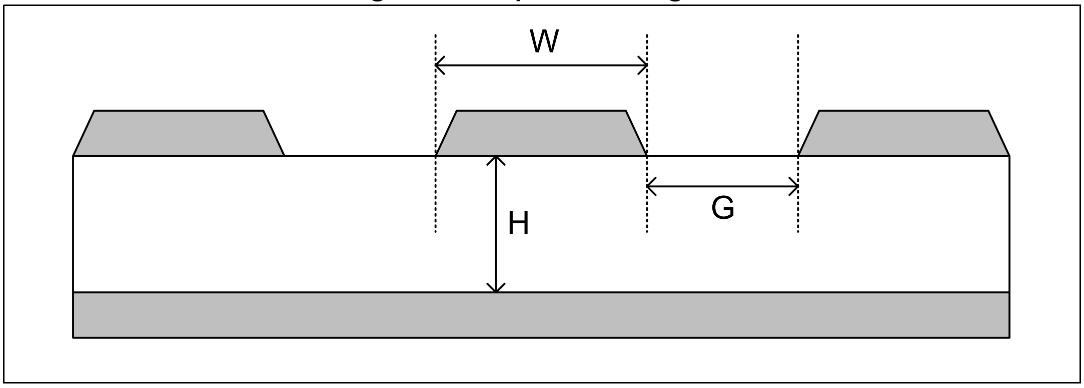
RF boards are designed with at least two or four layers to obtain the best performance.

4.1 RF transmission lines

The transmission lines on a PCB can be implemented on external layers (microstrips and coplanar waveguides), or buried in internal layers (striplines).

The coplanar waveguide (CPW) is composed of a central signal line of width W between two ground planes, separated from them by a gap G (see *Figure 17*). The central line and ground planes are on the surface of a dielectric substrate of thickness H.

Figure 17. Coplanar waveguide



A CPW version named GCPW or CPWG exists, with a ground plane opposite to the dielectric.

4.2 PCB substrate choice

There are different types of PCB substrate, even if built with the same basic material (glass), some of them have controlled parameters that are more suitable for RF product. The PCB substrate used in RF designs is FR-4 (flame resistant 4). This material is known to retain its high mechanical values and electrical insulating qualities in both dry and humid conditions, at the expenses of dielectric constant stability over frequency and loss.

4.3 Ground planes

It is recommended to use a continuous ground plane on INNER 1 layer, assuming TOP layer is used for the components and the RF transmission line. This plane must not be shared or assigned to signal or power nets but must be uniquely allocated to ground. Partial ground planes on a layer, sometimes required by design constraints, must underlie all RF components and transmission line. Ground planes must not be broken under transmission line routing.

Ground vias between layers should be added liberally throughout the RF portion of the PCB. This helps prevent accrual of parasitic ground inductance due to ground-current return paths. The vias also help to prevent cross-coupling from RF and other signal lines across the PCB.

Additionally, on the TOP component layer, it is usually a good idea to fill the unused area with ground plane and then connect this top fill with the INNER1 ground plane with several vias. It is recommended to have these vias space about 1/10th of the wavelength apart.

The layers assigned to power supplies and ground must be considered in terms of the return current for the components. It is recommended to have no signals routed on layers between the power supplies layer and the ground layer.

- 2 -layer PCB
  - limited to thicknesses between 0.8 and 1.0 mm to make a 50 Ω line with an acceptable width
  - TOP layer: components and signal routing
  - BOTTOM layer: predominantly ground
- 4 -layer PCB
  - thickness between 0.8 and 1.6 mm
  - TOP layer: components and critical signals (for example, RF, XTAL, SMPS)
  - INNER1 layer: ground plane
  - INNER2 layer: power plane and signal routing
  - BOTTOM layer: ground plane and signal routing

The 2-layer PCB provides a cheaper solution and can provide performance equivalent to those of the 4-layer PCB, but requires careful signal routing and component placement.

The 4-layer solution is more complicated and expensive. The laser-filled and the buried vias have to be used to connect the tracks to the internal balls.

For PCBs with more than four layers, keep the components and critical signals (RF, XTAL, SMPS) on the TOP layer, put the ground plane in INNER1 layer before routing the signals on the others layers (INNER2, INNER3), to isolate the GPIOs from the critical signals.

Table 3. 2-layer PCB

ID	Layer	Material	Type	Thickness	ε_r
-	Top overlay	-	Overlay	-	-
-	Top solder	Solder resist	Solder mask	0.03 mm	3.6
1	Top layer	-	Signal	0.042 mm	-
-	Dielectric 1	FR4	Core	0.89 mm	4.7
2	Bottom layer	-	Signal	0.042 mm	-
-	Bottom solder	Solder resist	Solder mask	0.03 mm	3.6
-	Bottom overlay	-	Overlay	-	-

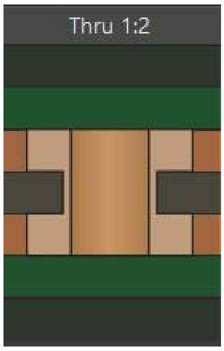


Table 4. 4-layer PCB

ID	Layer	Material	Type	Thickness	ε_r
-	Top overlay	-	Overlay	-	-
-	Top solder	Solder resist	Solder mask	0.01 mm	3.6
1	Top layer	-	Signal	0.017 mm	-
-	Dielectric 1	1 x 106	Prepreg	0.06 mm	4.2
2	Mid layer 1	-	Signal	0.017 mm	-
-	Dielectric 2	FR4	Core	1.4 mm	4.2
3	Mid layer 2	-	Signal	0.017 mm	-
-	Dielectric 3	1 x 106	Prepreg	0.06 mm	4.2
6	Bottom layer	-	Signal	0.017 mm	-
-	Bottom solder	Solder resist	Solder mask	0.01 mm	3.6
-	Bottom overlay	-	Overlay	-	-

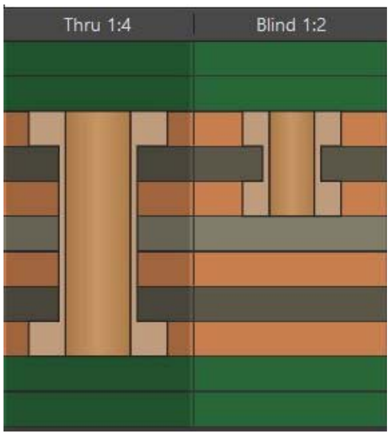
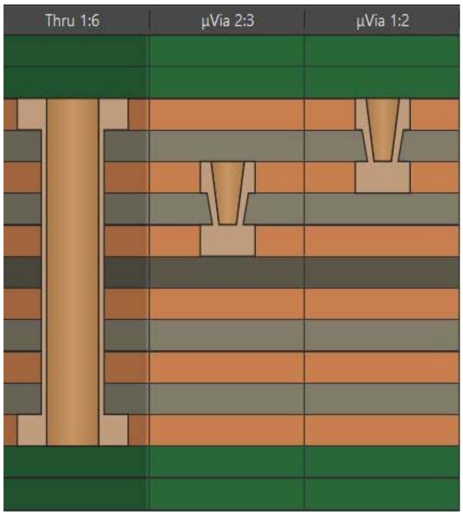


Table 5. 6-layer PCB

ID	Layer	Material	Type	Thickness	ε_r
-	Top overlay	-	Overlay	-	-
-	Top solder	Solder resist	Solder mask	0.03 mm	3.6
1	Top layer	-	Signal	0.037 mm	-
-	Dielectric 1	1 x 1080	Prepreg	0.065 mm	3.5
2	Mid layer 1	-	Signal	0.012 mm	-
-	Dielectric 2	1 x 1080	Prepreg	0.065 mm	3.5
3	Mid layer 2	-	Signal	0.017 mm	-
-	Dielectric 3	FR4	Core	1.08 mm	4.7
4	Mid layer 3	-	Signal	0.017 mm	-
-	Dielectric 4	1 x 1080	Prepreg	0.065 mm	3.5
5	Mid layer 1	-	Signal	0.012 mm	-
-	Dielectric 1	1 x 1080	Prepreg	0.065 mm	3.5
6	Bottom layer	-	Signal	0.037 mm	-
-	Bottom solder	Solder resist	Solder mask	0.03 mm	3.6
-	Bottom overlay	-	Overlay	-	-



5 Layout recommendations

5.1 2-layer PCB

Figure 18. PCB layout for UFQFPN48 (left to right: all, top and bottom layers)

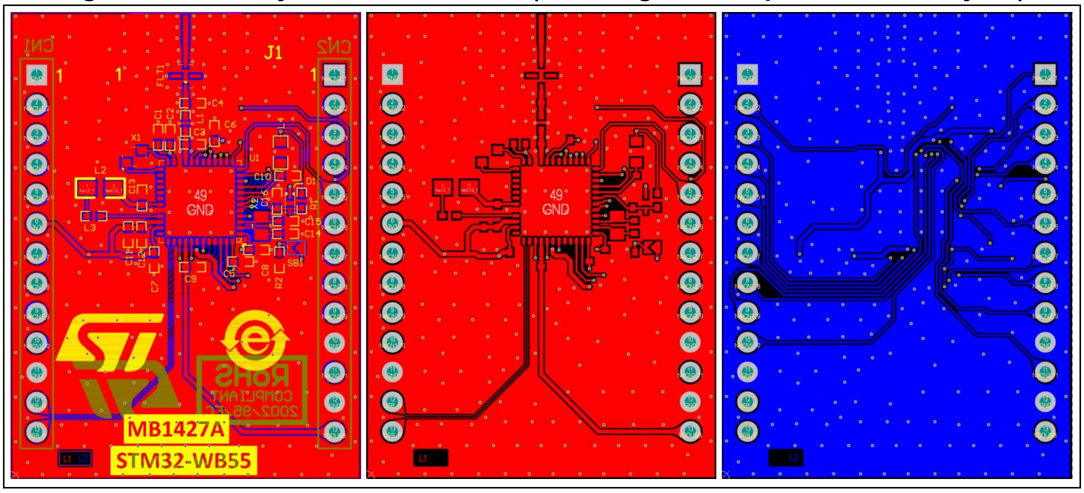


Figure 19. PCB layout for VFQFPN68 (left to right: all, top and bottom layers)

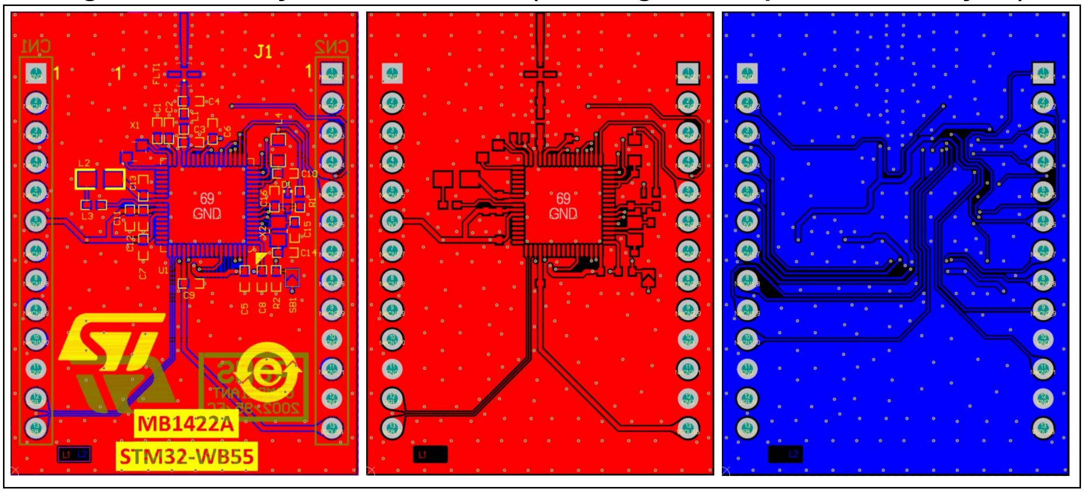
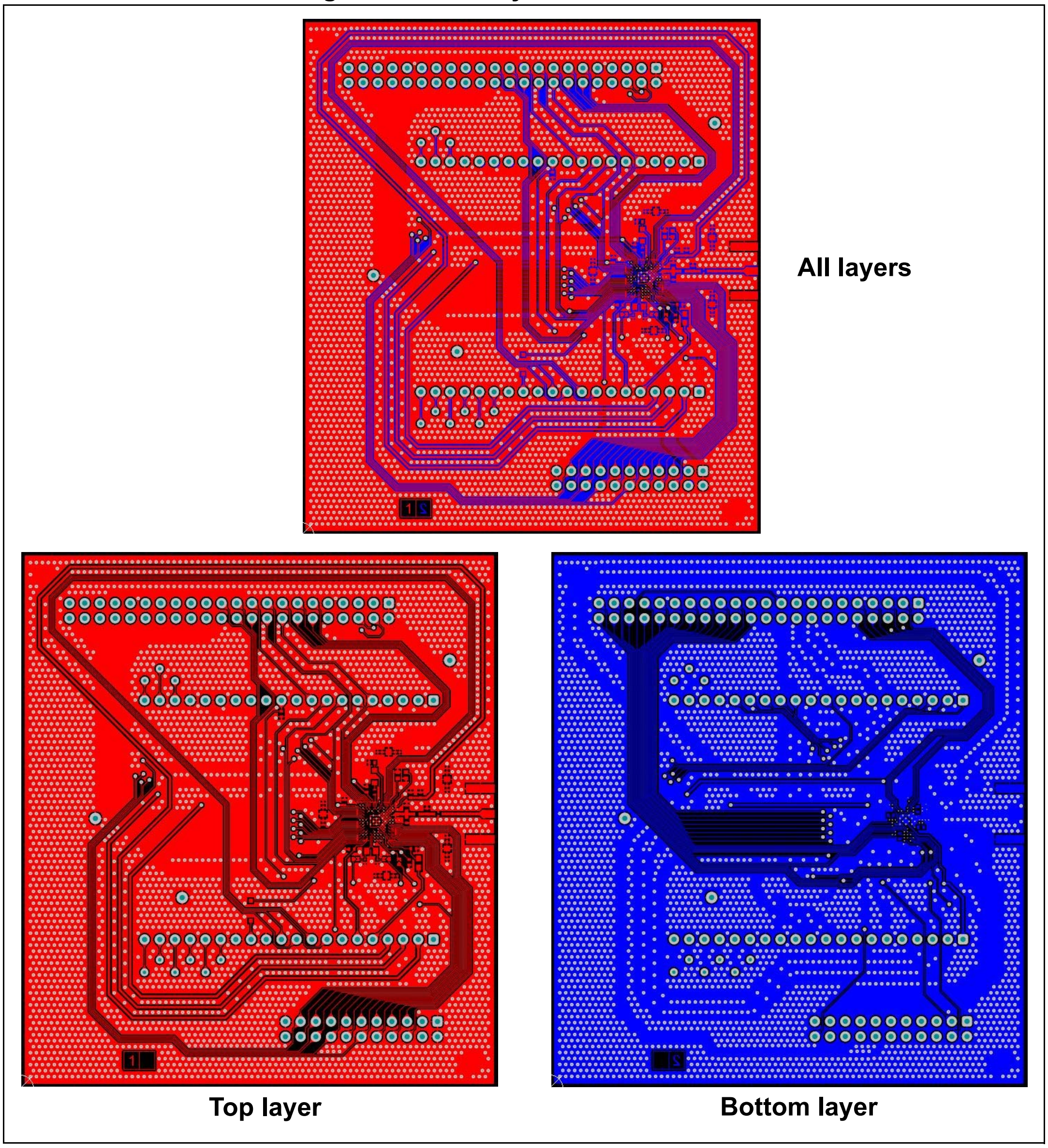


Figure 20. PCB layout for UFBGA129



5.2 6-layer PCB

Figure 21. PCB layout for WLCSP100 - All layers

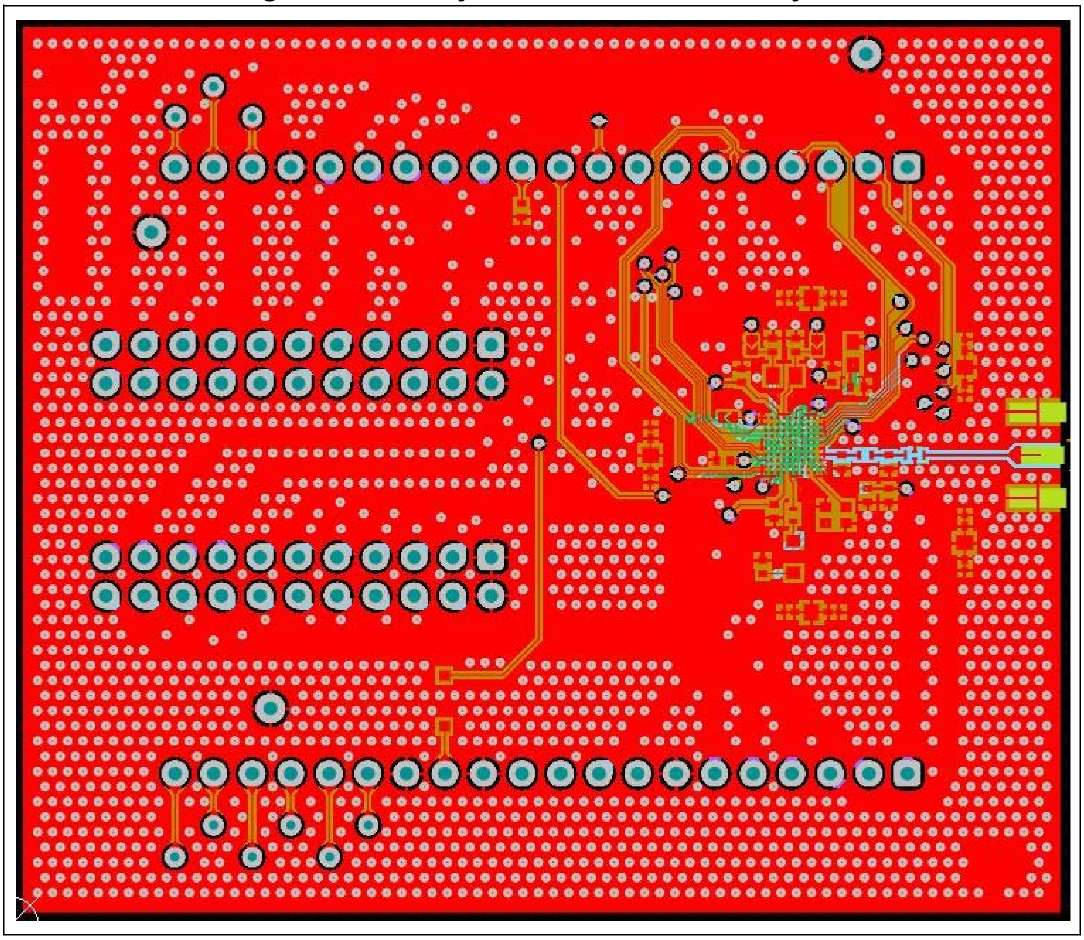
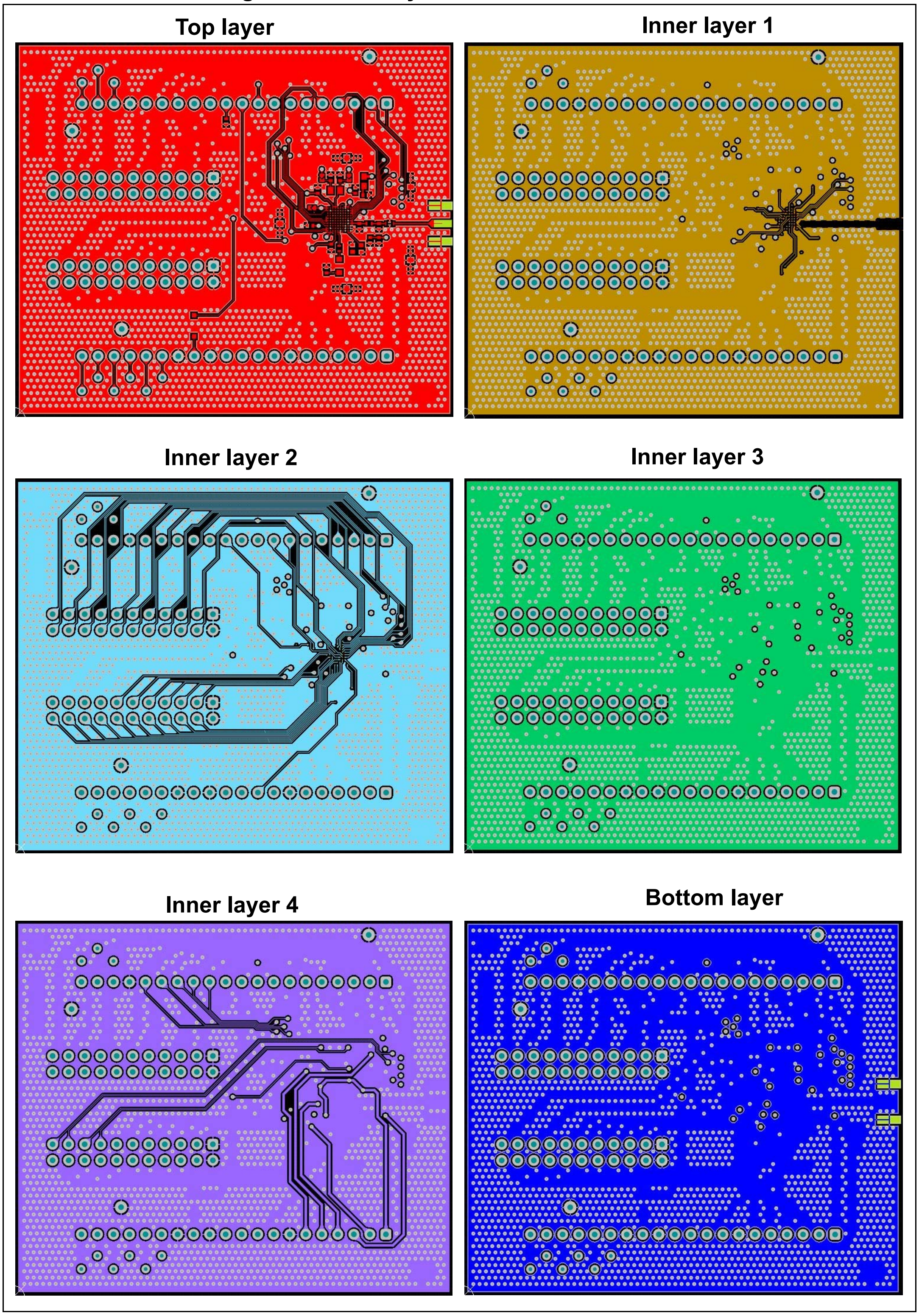


Figure 22. PCB layout for WLCSP100 - Detail



5.3 Critical parts

The three critical parts in the layout are the RF, the SMPS, and the LSE.

5.3.1 RF

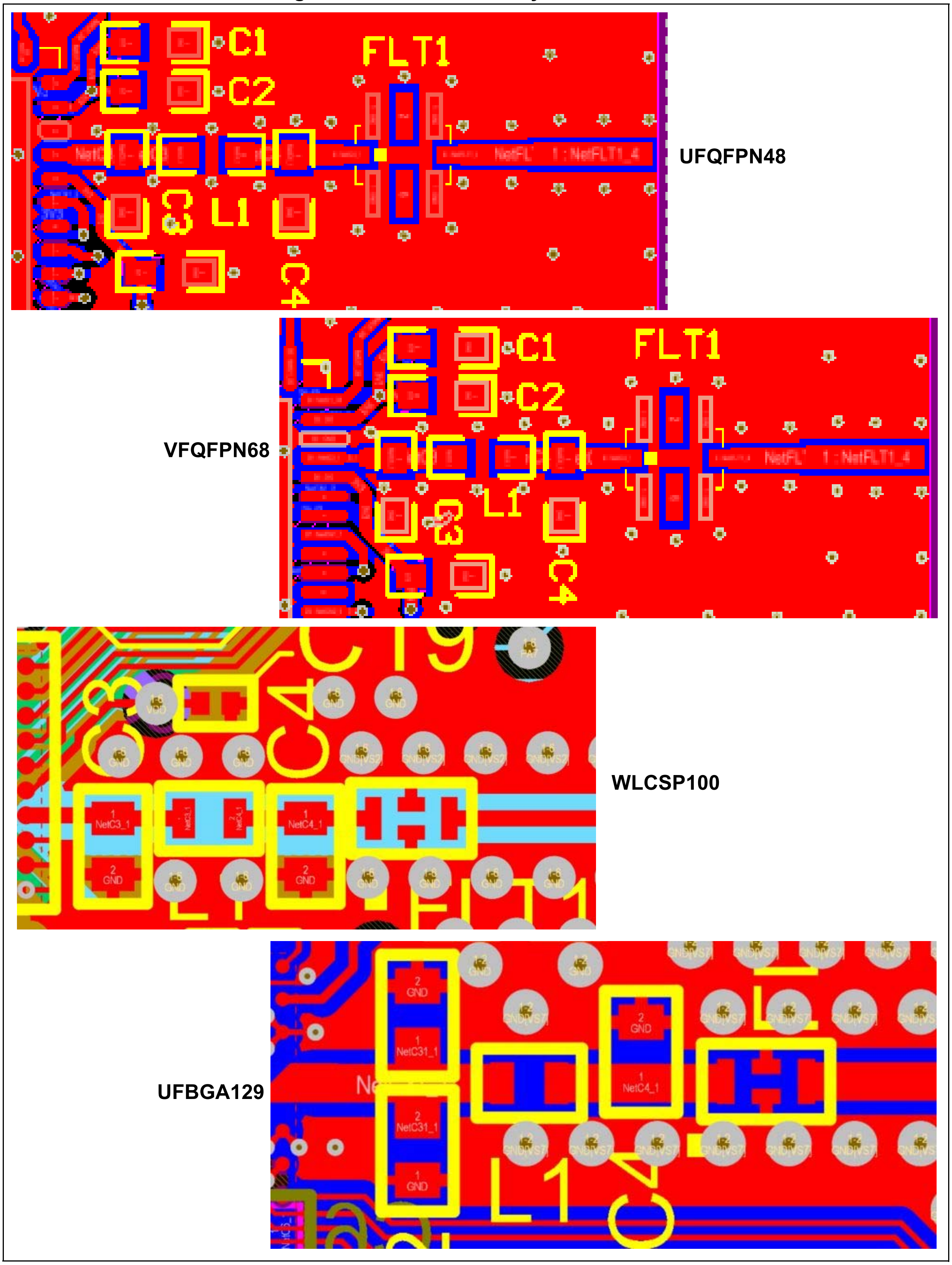
To obtain the best RF performance (in particular the maximum transmission power, the optimum reception sensitivity and a sufficient spurious and harmonic rejection), a matching network is required between the RF1 output pin and the RF low-pass filter.

This network is composed by a discrete LC PI filter followed by an integrated low-pass filter. C3 and L1 have the role of adapting the RF pin impedance of the STM32WB to 50 Ω, the impedance that must be seen by the SMA. C4 and the integrated low-pass filter FLT1 are used to reject the harmonic frequencies. The values of C3, C4, and L1 depend on the reference board PCB definition, detailed in *Section 2: Reference board schematics*.

The low-pass filter FLT1 used has a mark to distinguish the direction. Respect the direction indicated on the PCB (the filter structure is not perfectly symmetric, the properties change with the mounting direction).

It is also recommended to place the matching network as near as possible to the RF output and to avoid long track between each component of this matching network. The track between the output of the low-pass filter FLT1 and the SMA connector can have a variable length, depending upon the application, provided that its impedance is always 50 Ω.

Figure 23. Detail of PCB layout for the RF



5.3.2 SMPS

When the device goes from BYPASS mode (SMPS output voltage is tied to supply voltage) to ON mode (SMPS output voltage is lower than supply voltage, typically 1.4 V), the SMPS must discharge in the output capacitor and consequently, the coil current becomes negative. To avoid excessive currents (that can damage the device), some design rules must be considered for the layout of the V_{DDSMPS} tracks.

The following example is based on the reference board of the STM32WB55 in a BGA129 package, but the guidelines can be applied to all devices of the STM32WB series.

- Capacitor C12 (4.7 µF) is required between VDDSMPS pins (F12 and F13), see *Figure 24*.
- Ensure that a whole ground plane is just under the layer and covers the capacitor and the track between it and the VDDSMPS pins. The example (see *Figure 25*) uses a 2-layer board. The capacitor is on the top layer (in red) and the ground plane on the bottom layer (in blue).
- Measure the width and length of the track between the VDDSMPS pin and the capacitor.
- Check the thickness and the permittivity of the dielectric between the top and the bottom layer (highlighted in the list below), which is the distance between the capacitor and the ground plane reference. In the example.

Layer	Material	Type	Weight	Thickness	ε_r
Top solder	Solder resist	Solder mask	-	0.03 mm	3.6
Top surface finish	Nickel, gold	Surface finish		0.004 mm	-
Top layer	-	Signal	1/2 oz	0.042 mm	-
Dielectric 1	FR4	Core		**0.89 mm**	**4.7**
Bottom layer	-	Signal	1/2 oz	0.042 mm	-
Bottom surface finish	Nickel, gold	Surface finish		0.004 mm	-
Bottom solder	Solder resist	Solder mask		0.03 mm	3.6

- Download the freeware Saturn PCB (available at https://saturnpcb.com)
- Launch Saturn PCB, go to “Conductor Impedance” with “Microstrip” configuration, and enter the previously found parameters. Then, click on “Solve”, the result appears in the Lo window (*Figure 26*). In this example, Lo (inductor) = 6.5523 nH/cm. As the track length is 0.1663 cm, the ESL (equivalent series inductance) due to the track is 1.0896 nH.
- The ground pin of C12 must return to the ground plane through a via as close as possible (see *Figure 27*). This via has also an ESL.

  As the height of the via corresponds to the thickness of the dielectric between the top and the bottom layer (890 µm), it can be seen in *Figure 28* that the via inductance is around 0.23 nH, hence the board ESL between the VDDSMPS pin through the decoupling capacitor to the ground is 1.0896 + 0.23 = 1.3196 nH

  The board ESL between the decoupling capacitance and the VDDSMPS pin must be lower than the value listed below for the STM32WB series MCUs:
  - 2.0 nH for QFN packages
  - 3.0 nH for WLCSP packages

  – 2.5 nH for BGA package

  The ESL of the decoupling capacitor (estimated at 0.4 nH) has been considered in the values indicated above.

- It is also important to verify that the VSSSMPS pins of the chip, the negative pin of the capacitor and the exposed pad (for QFN packages) or the VSS pins (for WLCSP/BGA packages) are connected as close as possible.

Figure 24. VDDSMPS capacitor

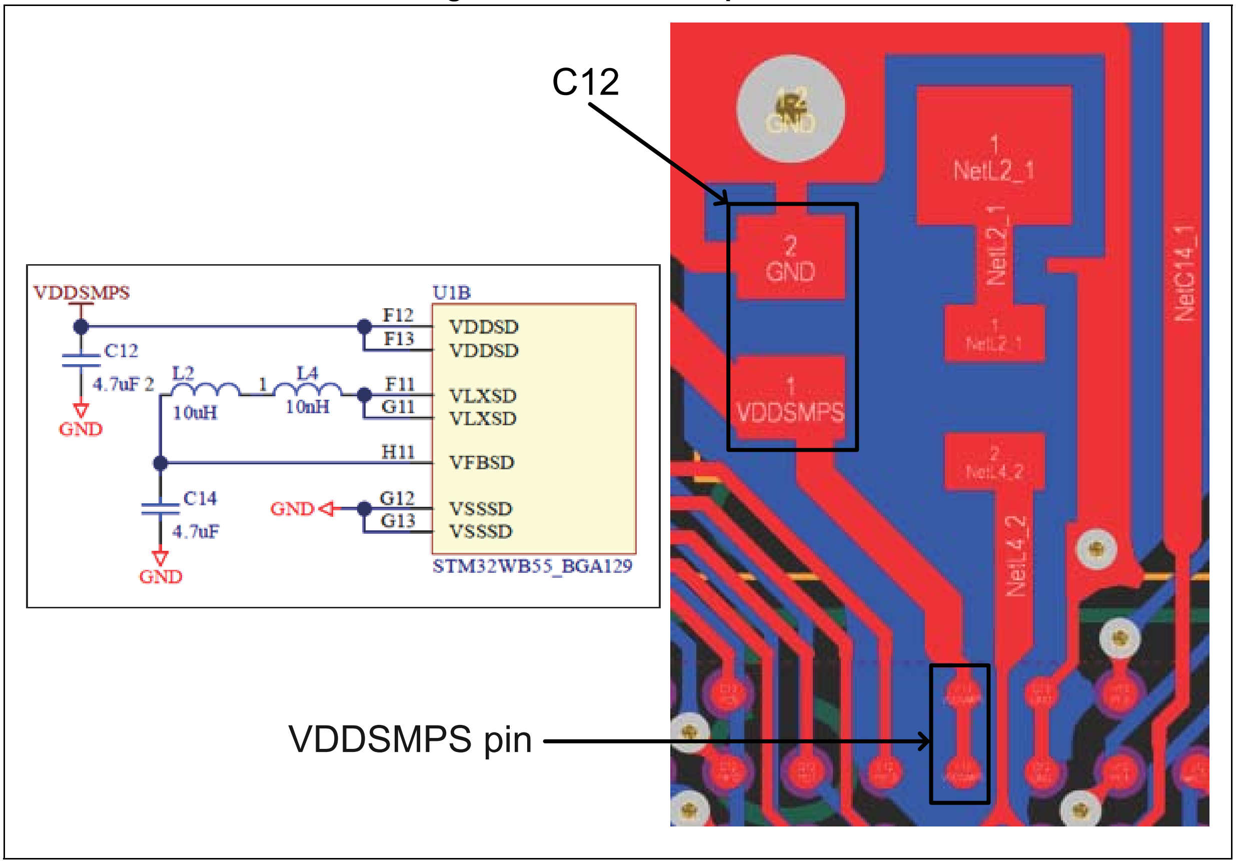


Figure 25. VDDSMPS capacitor connection

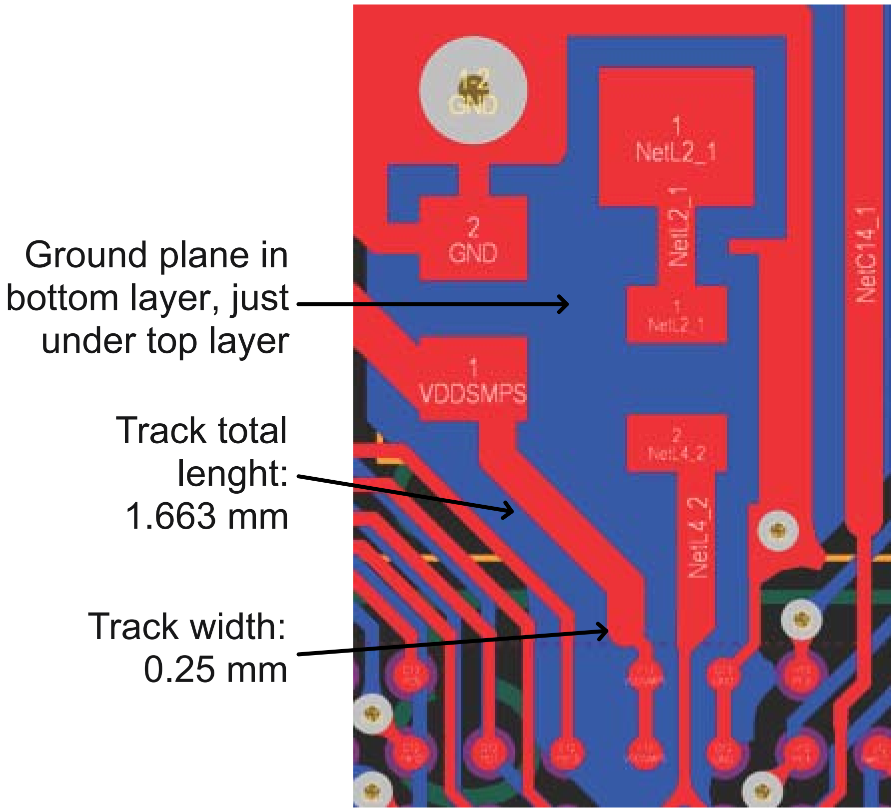


Figure 26. Saturn PCB Lo window

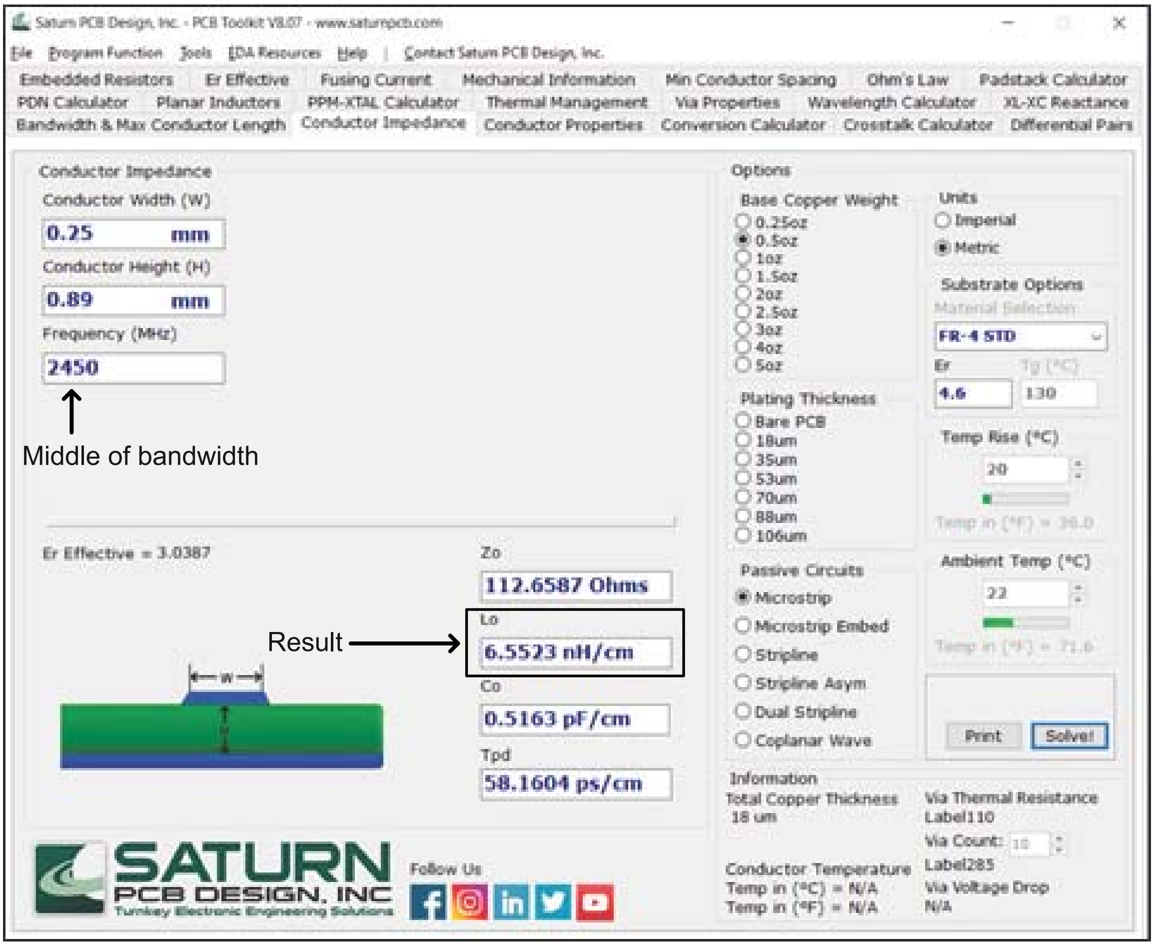


Figure 27. Via for ground pin of C12

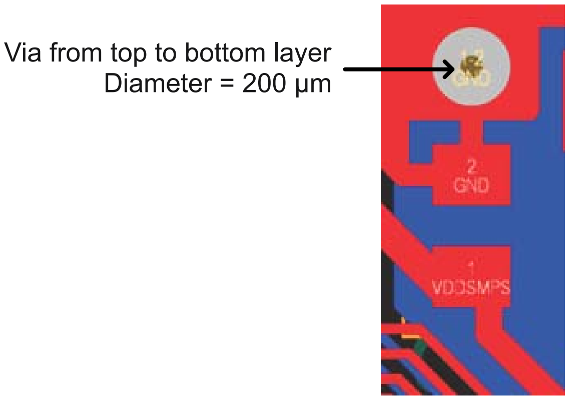
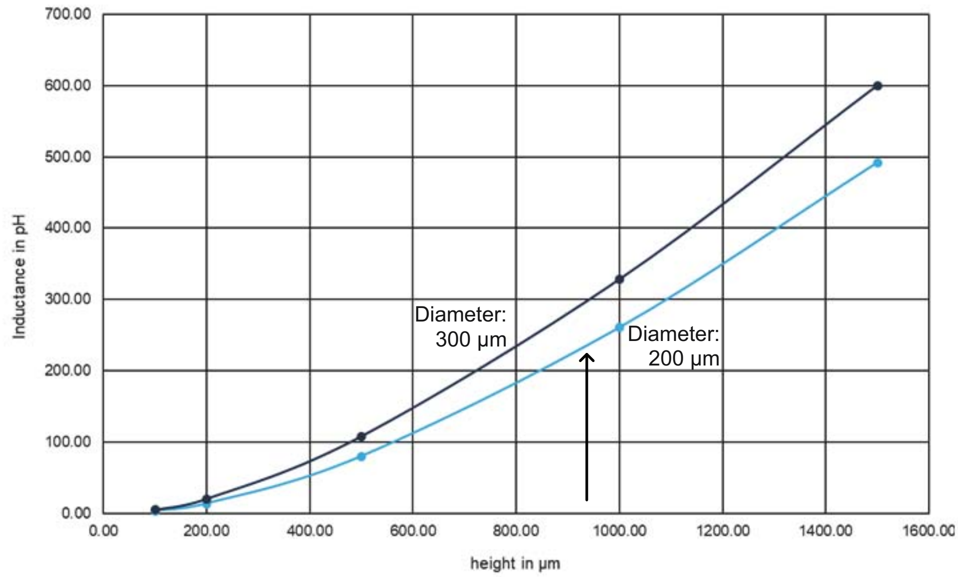


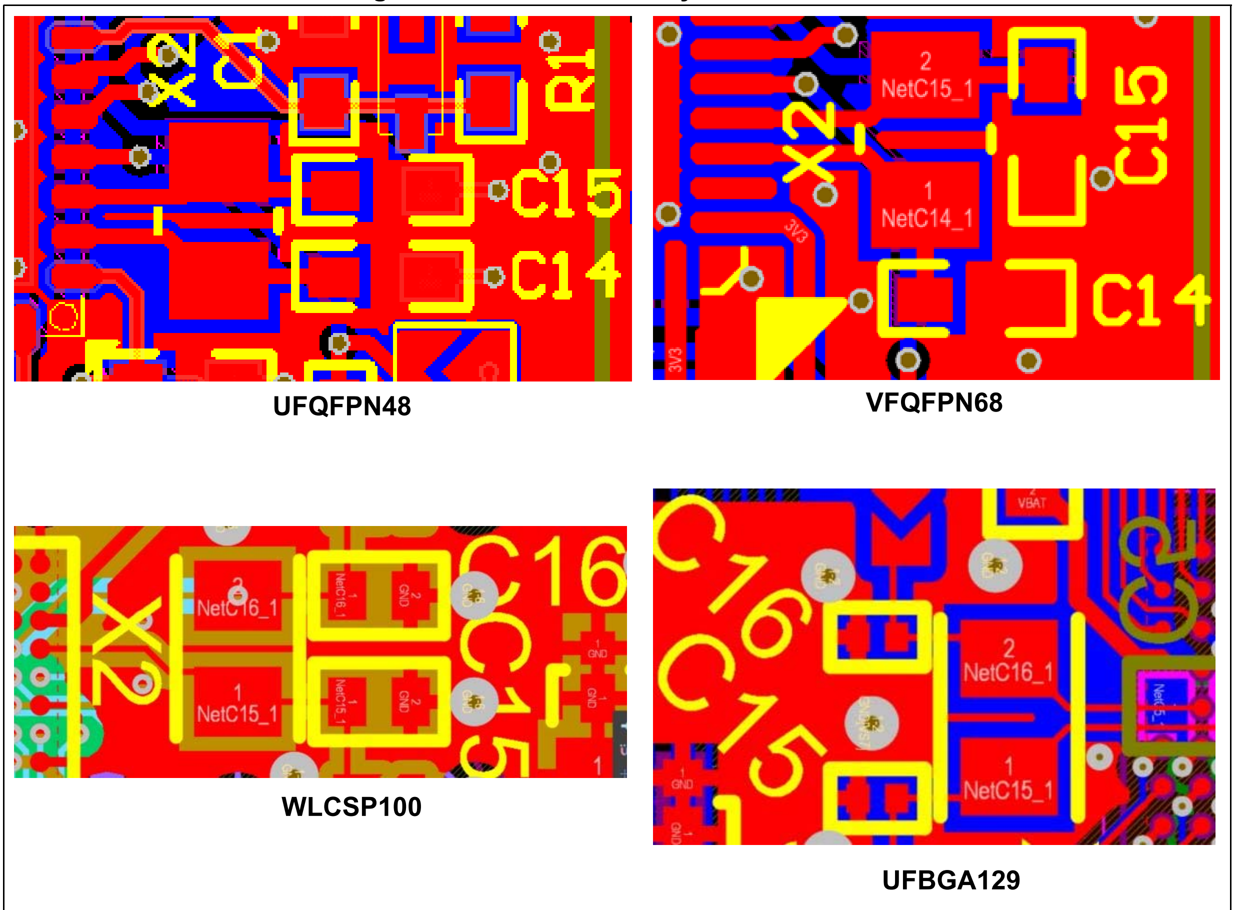
Figure 28. Via ESL



5.3.3 LSE

As indicated in *Section 3.4: External crystal*, place X2, C14 and C15 as close as possible to their respective pins.

Figure 29. Detail of PCB layout for the LSE



6 Layout recommendations for reference boards

6.1 Power supplies and decoupling

Power supply routing is important in RF design and, if not carefully made, can affect the system performance undesirably. Proper routing, bypassing and decoupling avoid noise coupling effects and affecting the performance of the system. A source of high frequency noise on a PCB can be the transient demand of current by active devices, casing high frequency harmonics to be generated. The generated noise can travel to the power supply pins of the devices, degrading performance, to prevent this it must be bypassed to the ground plane using a capacitor providing a low impedance path.

Also, the digital section switches rail to rail rapidly, generating high frequency harmonics, which can couple with the power supply lines if not routed and decoupled properly. Also, there may be undesired coupling between the power supply lines. The power supply and digital lines must be routed away from the RF section, and decoupling must be done to isolate the corresponding power supply pin from the high frequency noise on the other sections. Additionally, the bypass/decoupling capacitor must be selected considering the SRF (above this frequency the capacitor behaves as an inductor, hence a capacitor is effective only up to the SRF).

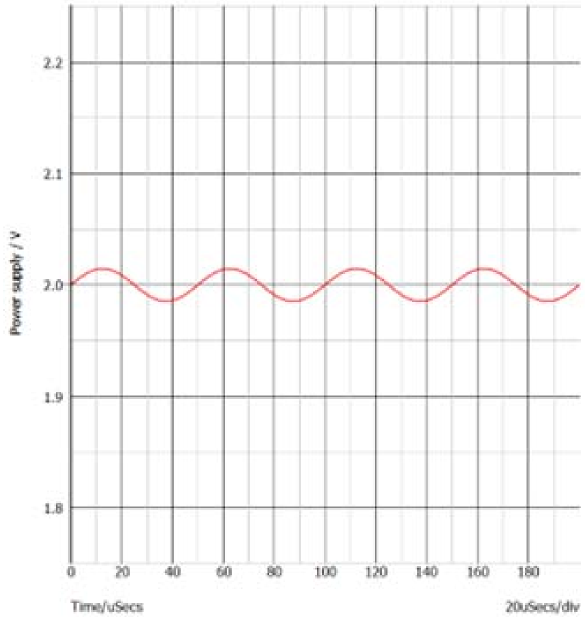
A common practice is to use a “star” configuration for the power supplies nets. A larger decoupling capacitor (4.7 to 10 uF) is mounted at the “root” of the star, and smaller capacitors (100 nF) at the end of each of the star branches near the power supply pins of the chip.

The star configuration avoids long ground return paths that would result if all the pins connected to the same power supply net are connected in series. A long ground return path causes a parasitic inductance that can lead to unintended feedback loops.

6.1.1 Behavior of the STM32WB according to the ripple on V_{DD}

Ripple is a variation on the power supply, it can be generated, for example, by an external DC-DC converter. In the example (*Figure 30*), the ripple is a sine wave with a peak-to-peak level of 15 mV and a frequency of 20 kHz. V_{DD} is 2 V in this case. The shape of the wave can have different aspects, for example sawtooth, or sinusoidal.

Figure 30. Ripple on V_{DD}



The RF performance and the RF link can be affected by the ripple, if present. It is recommended to reduce it if its level is above the limits indicated in *Table 6* for a frequency lower than the frequency limit. For example, 10 mV is the maximum level for a frequency between 50 and 150 kHz.

Table 6. Ripple limits[(1) (2)]

Level (mV_{PP})	Frequency (kHz)
15	50
10	150
5	> 150

1. These values have been set for a sine wave or a sawtooth wave on V_{DD}.
2. These values apply to all V_{DD} values

In the case of a 50 mV_{PP} ripple at 40 kHz generated by the external power supply, a low-pass filter (RC) can be implemented (see *Figure 31*). The goal is to reduce the ripple, for example from 50 to 10 mV_{PP}. A ratio of 5 is needed, equivalent to 14 dB for a first order filter.

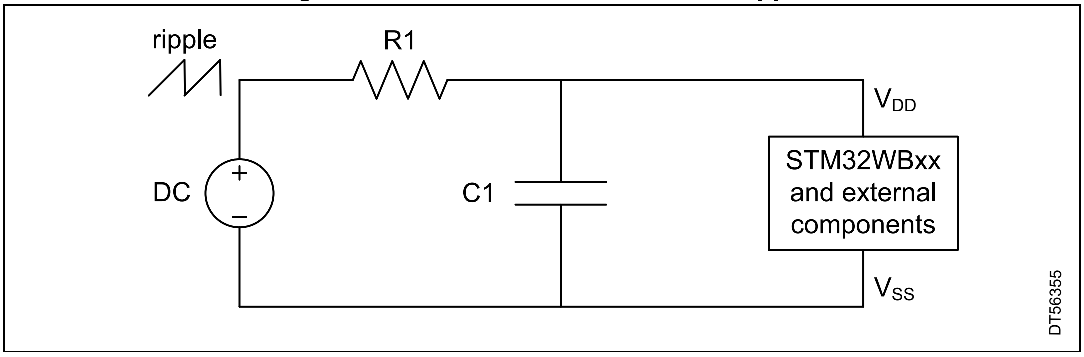
The consequence is that the cutoff frequency (Fc) must be 40 kHz / 5 = 8 kHz.

For an RC filter, Fc = 1 / 2 π R C.

To reduce the resistance loss, use a low value for R, for example 2.2 Ω. This produces a voltage drop proportional to the DC current consumption: for example, with 30 mA, V = R * I = 30 * 2.2 = 66 mV.

Then C = 1 / 2 π R Fc ~ 10 µF

Figure 31. RC solution to reduce the ripple

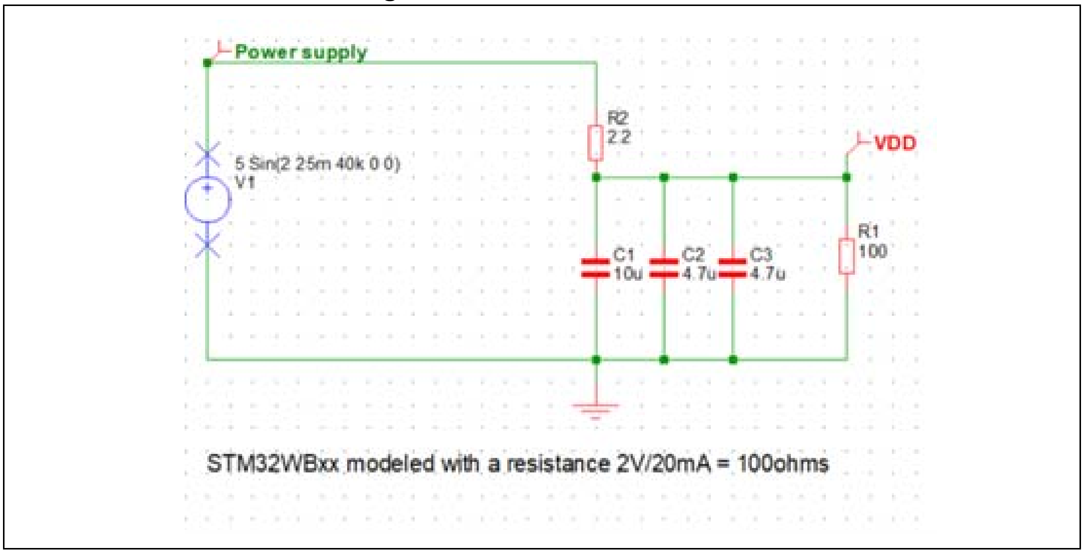


Filtering is more effective because the recommended decoupling capacitors (2 x 4.7 µF) add up and increase the performance of the RC filter.

Simulation tools are available, they make it possible to enter an equivalent scheme of the product and to check the attenuation.

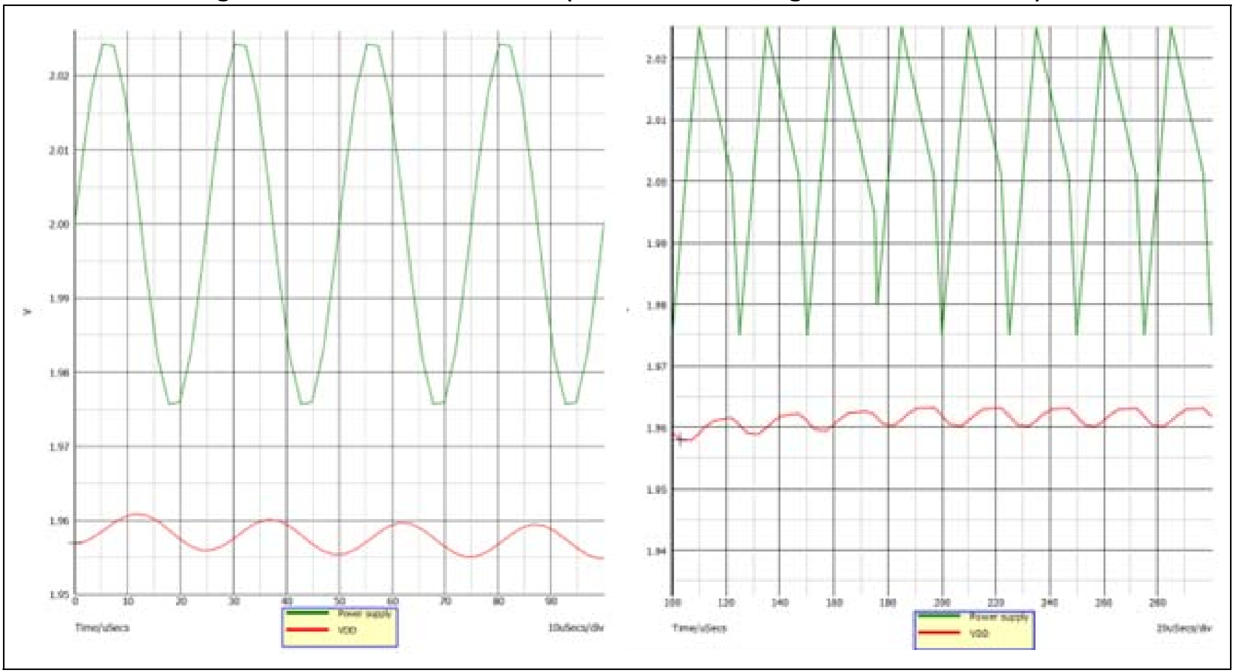
R1 is the equivalent resistance of the STM32WB when it is supplied with 2 V. It is assumed that the current consumption is 20 mA. C2 and C3 are the recommended capacitors for the power supply. R2 and C1 are the components of the RC filter.

Figure 32. Simulated scheme



The results are shown in *Figure 33*. The 50 mV_{PP} ripple is reduced to 5 or to 3 mV_{PP}, respectively, for a sine or sawtooth wave with a frequency of 40 kHz. These values are lower than the limits defined in *Table 6*.

Figure 33. Simulation results (left: sine wave, right: sawtooth wave)



6.2 Grounding shunt-connected components

For shunt-connected (grounded) components (such as power supply decoupling capacitors), the recommended practice is to use at least two grounding vias for each component. This reduces the effect of via parasitic inductance. Via ground 'islands' can be used for groups of shunt-connected components.

6.3 IC ground plane (exposed pad)

Most devices require a solid ground plane on the component layer (TOP or BOTTOM of PCB) directly underneath the component. This ground plane carries DC and RF return currents through the PCB to the assigned ground plane. The secondary function of the exposed pad is to provide a thermal heat-sink, so that the exposed pad should include the maximum number of vias allowed by the PCB design rules. These vias are ideally thru-vias (penetrating through all the PCB layers).

6.4 Isolation

Care must be taken to prevent unintended coupling between signal lines. Some examples of potential coupling and preventive measures:

- RF transmission lines: keep them as far apart as possible. The grounded coplanar waveguide provides excellent isolation between lines. It is impractical to achieve better than approximately -45 dB between RF lines on small PCBs.
- High-speed digital signal lines should be routed separately on a layer different from that of the RF signal line to prevent coupling. Digital noise (for example, clocks) can couple onto RF signal lines, and these can be modulated onto RF carriers.
- V_{DD} and power lines must be routed on a dedicated layer. Provide adequate decoupling/bypass capacitors at the main V_{DD} distribution nodes and at V_{DD} branches. The value of the bypass capacitances must be set based on the overall frequency response of the RF device, and the expected frequency distribution nature of any digital noise from clocks. These lines should also be separated from the RF lines.

6.5 Component orientation

Inductors on the PCB generate a magnetic field that can couple with other components and RF line. To obtain a good isolation between those components, place them orthogonally and, if not possible, space them as much as possible.

6.6 RF

To obtain the best RF performance (in particular maximum transmission power, optimum reception sensitivity and a sufficient spurious and harmonic rejection), a matching network is required between the RF output pin of the device following by the RF low-pass filter.

The discrete LC PI network have the role of adapting the RF pin impedance of the device to 50 Ω, the impedance that must be seen by the SMA. The integrated low-pass filter FLT1 is used to reject the harmonic frequencies. The values of the discrete LC PI network components depend upon the device package and the reference board PCB definition.

The low-pass filter used has a mark to distinguish the direction. Respect the direction indicated on the PCB (the filter structure is not perfectly symmetric, the properties change with the mounting direction).

Place the matching network as close as possible to the RF output and avoid long tracks between each component of this matching network to minimize the possible phase rotation with respect to harmonics and the risk of radiation by this line (radiation is proportional to the length). And obviously, minimize losses due to the track length.

It is also recommended not to cover the RF tracks with a metal mask.

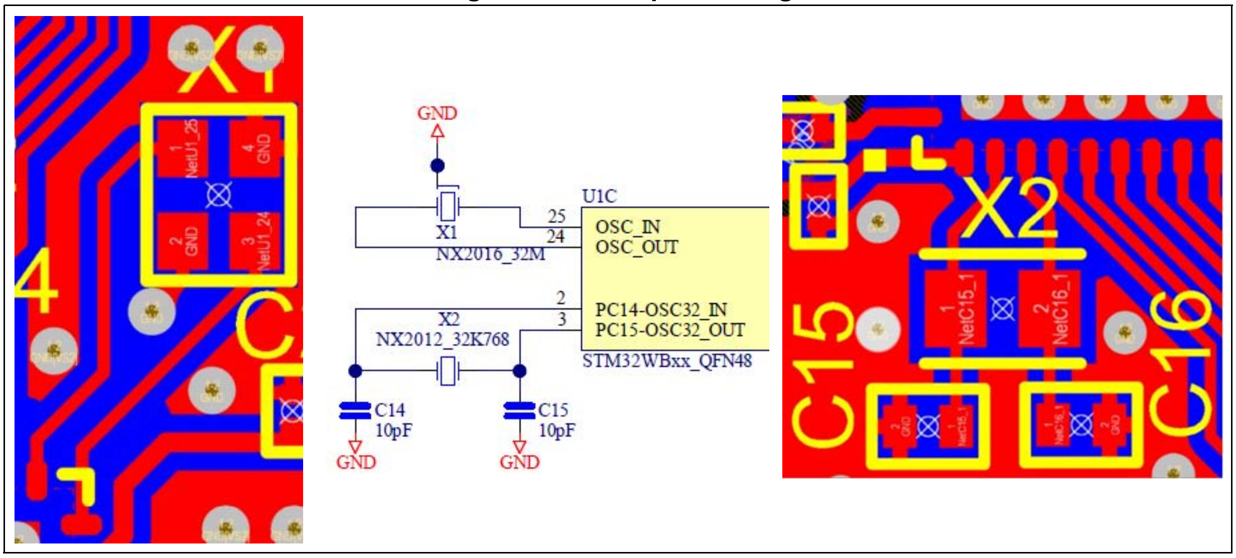
6.7 XTALs

It is recommended to place the XTALs on the top layer and to keep them as close as possible to the oscillator pins of the device. Long lines must be avoided.

No GPIO routing in the vicinity on the top layer and the layers below the XTAL as long as the ground layer is not inserted.

The XTAL must be kept far from SMPS and RF components (matching, filter, antenna).

Figure 34. XTAL positioning

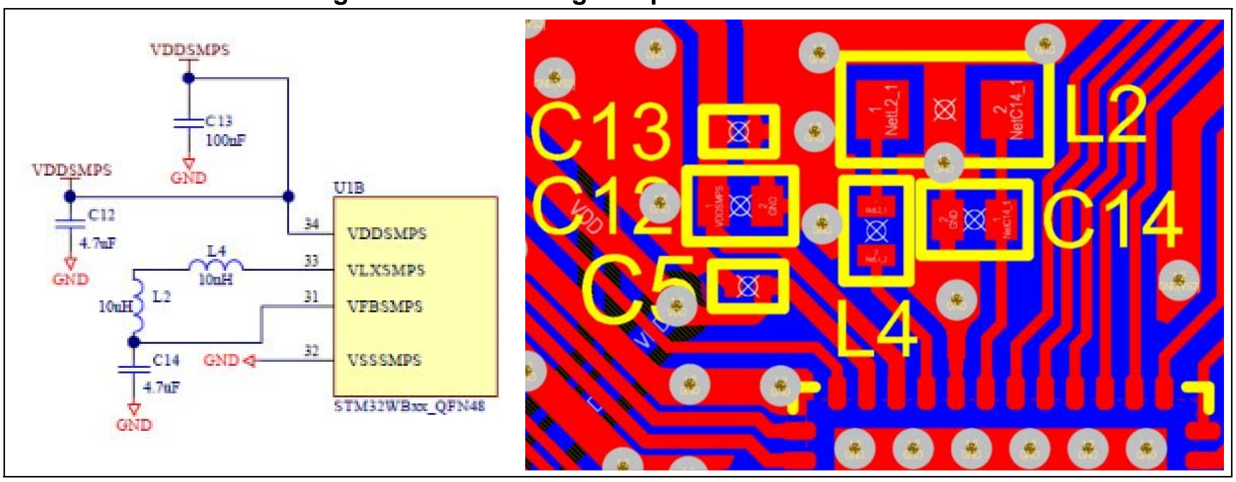


6.8 SMPS

V_{DDSMPS} and V_{SSSMPS} must be decoupled as close as possible to the device pin (refer to *Section 5.3.2*). Large currents flow from V_{DD} to the SMPS output and from here to V_{SS}.

Place and route the inductor (L1) as close as possible to the device with the area of the copper connection kept small (to let the coupling capacitance as small as possible). Be careful on the orientation of the inductances. Place and route the SMPS output capacitance C14 connected to the power ground terminal and place to minimize the distance between the inductance and the ground.

Figure 35. Positioning components for the SMPS



6.9 Check list

1. Verify that the bypass capacitors are as close as possible to the power supply pins that they are meant to bypass.
2. Ensure that each decoupling capacitor only decouples the specific pins recommended on the reference design and that the capacitor be of the correct value and type.
3. Check that the SMPS parasitic inductance is lower than the limit, and the ground position, as detailed in *Section 5.3.2*.
4. Verify that the stack-up matches the reference design. If the design is 4-layer or higher, verify that ground plane is INNER1 layer just below TOP/components layer.
5. Changing the spacing/stack-up affects the matching in the RF signal path and must be carefully accounted.
6. A solid ground plane must be placed below the device and the RF path. No ground plane must be placed below the antenna unless recommended by the manufacturer.
7. Verify that the RF signal path matches the reference design as close as possible (components should be arranged in a very similar way and oriented the same way).
8. The XTALs should be as close as possible to the oscillator pins of the device. Long lines to the oscillator must be avoided.
9. No GPIOs net nearby the XTAL area.
10. Verify that the ground pours on the TOP layer are stitched to the INNER ground plane and to the BOTTOM layer plane with many vias, especially around the RF path. Vias on the rest of the board should be no more than a tenth of wavelength apart.
11. If the device uses a battery, do not place it under the antenna, because it acts as a ground plane.
12. The board should specify impedance-controlled traces, meaning that the layer spacing and FR4 permittivity must be controlled and known.

Important considerations for the antennas:

1. Be sure to copy the reference design exactly with the same stack-up.
2. Changes to feed line length of the antenna change input impedance matching.
3. Metals in close proximity, plastic enclosures, and human body change the antenna input impedance and resonance frequency.
4. For multiple antennas on the same board use antenna polarization and directivity to isolate them.
5. For chip antennas, verify that the spacing from and the orientation respect to the ground plane is correct (as specified in the antenna datasheet).

6.10 Undesired effects

- Sensitivity/spurs (Receive mode; RF input):
  - GPIO coupling through RF lines, ground, power supply
  - XTAL coupling through RF lines, ground, power supply
  - SMPS coupling through RF lines, ground, power supply
  - Digital activities through ground, power supply
- Pulling:
  - VCO pulled by the PA, the XTAL or/and the GPIO
  - PA pulled by the VCO, the XTAL or/and the GPIO
  - XTAL pulled by the VCO, the PA or/and the GPIO

7 Reference boards with IPD

The goal of the IPD (integrated passive device) is to replace the discrete matching network plus the integrated low-pass filter keeping equivalent TX/RX performance. *Figure 36* shows the differences between the two approaches, using as example the QFN48 package.

Figure 36. Different matching networks (discrete components on the left, IPD on the right)

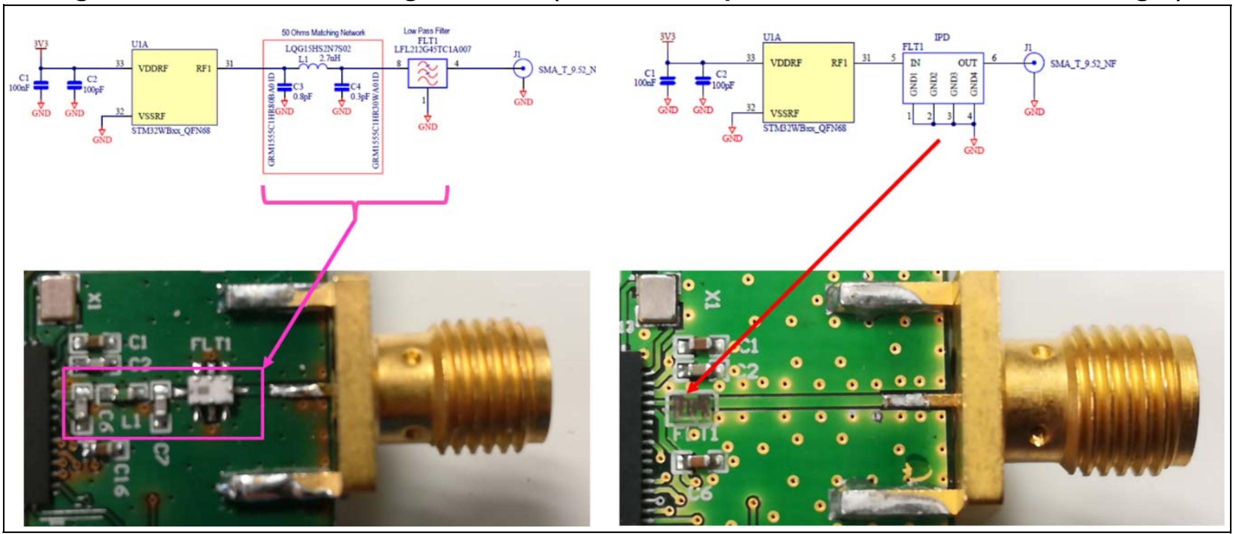


Table 7. References

Package	IPD reference	Document[(1)]
QFN48	MLPF-WB55-01E3 (bumpless package) MLPF-WB55-01D3 (CSP package)	DS12804, *2.4 GHz low pass filter matched to STM32WB55Cx/Rx*
QFN68		
UFBGA129		
WLCSP100	MLPF-WB55-02E3 (bumpless package) MLPF-WB55-02D3 (CSP package)	DS13176, *2.4 GHz low pass filter matched to STM32WB55Vx* DS14042, *2.4 GHz low pass filter matched to STM32WB5x and STM32WB1x in WLCSP and UFBGA packages*

1. Available on *www.st.com*.

Transmission and insertion loss performance are shown, respectively, on the left and on the right side of *Figure 37* (MLPF-WB55-01E3) and of *Figure 38* (MLPF-WB55-02E3).

Figure 37. RF performance of the MLPF-WB55-01E3

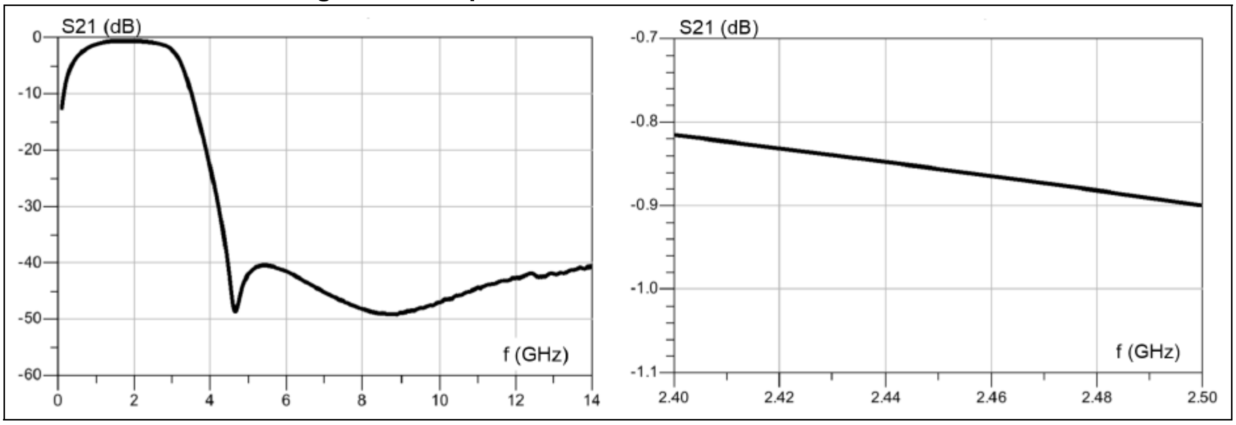
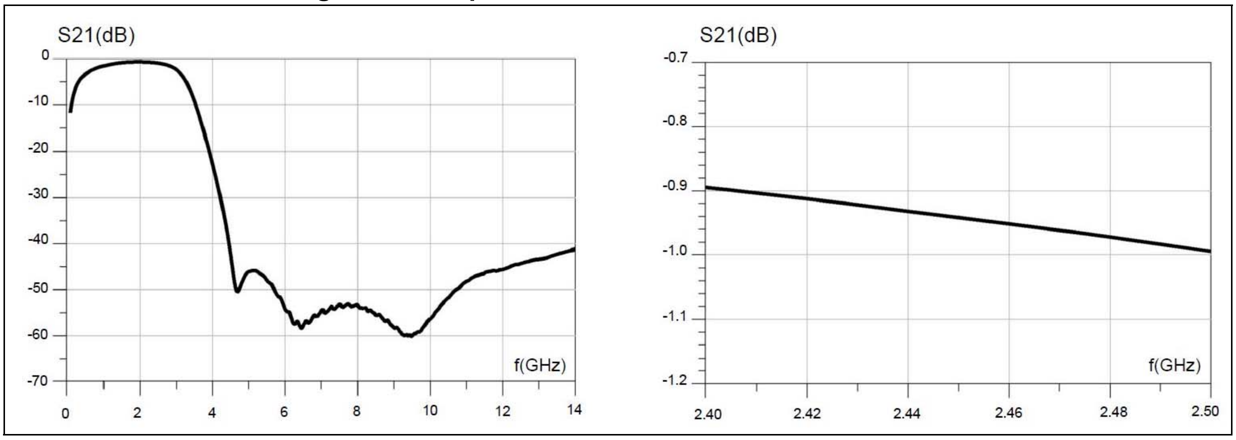
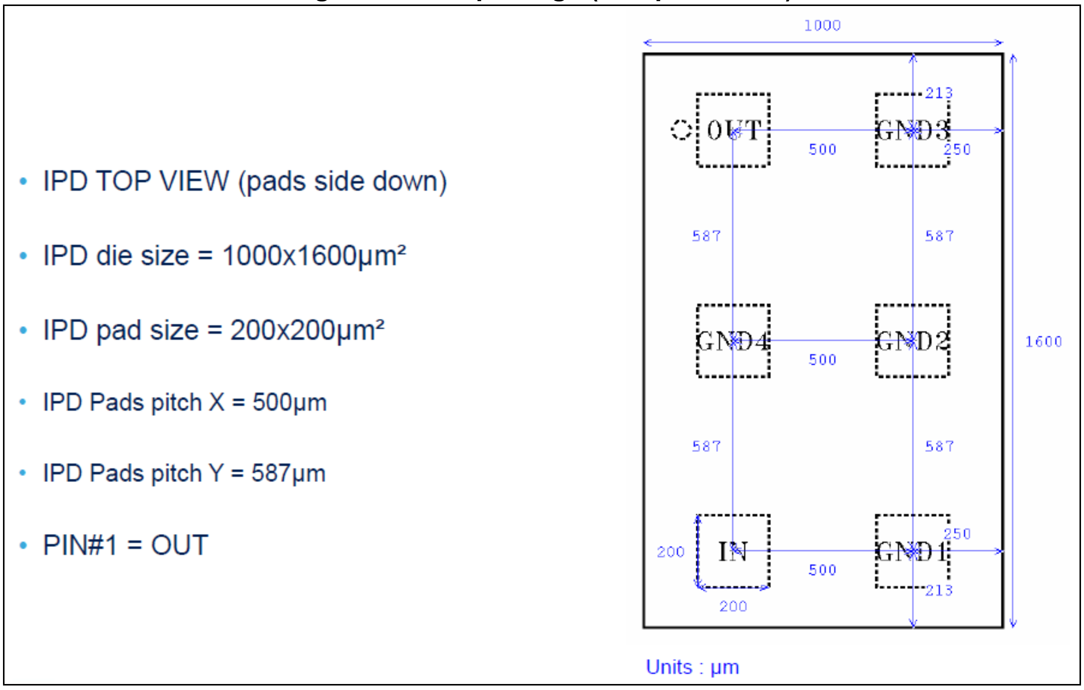


Figure 38. RF performance of the MLPF-WB55-02E3



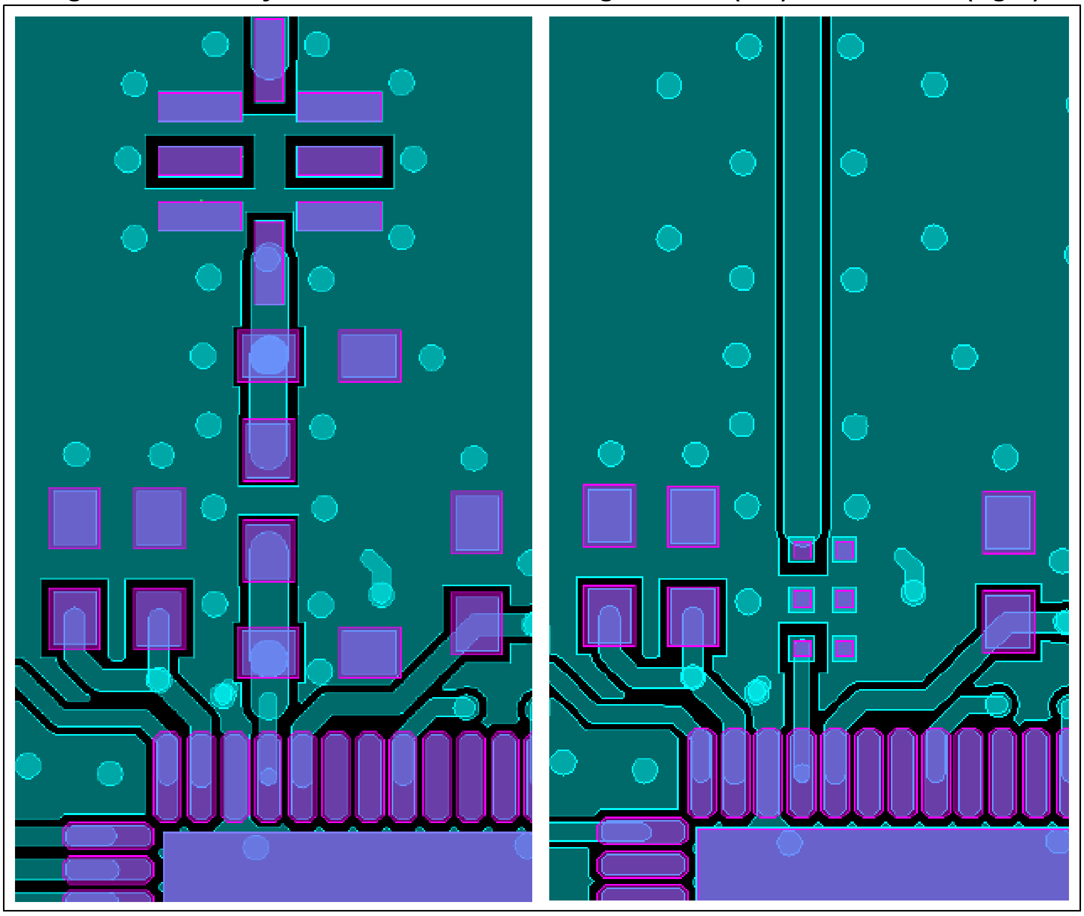
The bottom view of the IPD package is shown in *Figure 39*.

Figure 39. IPD package (bumpless CSP)



The PCB can be greatly simplified, as shown in *Figure 40*.

Figure 40. PCB layout with discrete matching network (left) and with IPD (right)



Note that the length of the track between the output of the IPD and the RF output can be further reduced to decrease the dimensions of the PCB. This improves RF performance by reducing losses due to the length of this track.

As a conclusion, the IPD reference MLPF-WB55-01E3 can replace the RF output network of the STM32WB for the QFN packages (an antenna filter is still needed) for a 2-layer PCB. The PCB size and the bill of materials are reduced, while guaranteeing equivalent RF performance compared with the discrete RF output network. Another advantage of the IPD solution is the performance stability on volume production (lower parameter dispersion compared with the discrete components).

8 Matching network determination

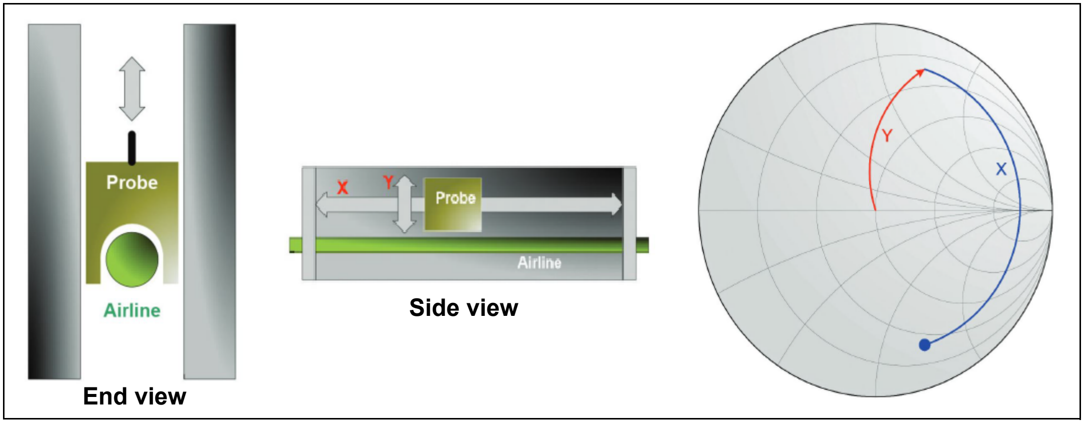
8.1 Load pull measurement

The load pull measurement is used to determine the network matching circuit, to obtain the maximum output power from an RF device. This measuring bench is mainly composed by an impedance tuner that makes it possible to present to the RF chip impedances different from 50 Ω. The software used to drive the impedance tuner is an example, others can be used.

The frequency chosen to determine the impedance is the middle of the Bluetooth Low Energy bandwidth (2450 MHz).

The most common impedance tuner is a slide screw. It consists of two parallel plates, a center line and a metal probe (see *Figure 41*). Moving the probe vertically modifies the reflection coefficient, moving it horizontally modifies the phase.

Figure 41. Load pull measurement



8.2 Procedure

The first step is to calibrate the RF2 tuner (each position correspond to an impedance), operating it empty (the part to test is not yet connected). The VNA measures the impedance at the entrance of the tuner (see *Figure 42*).

The tuner is calibrated at the end of an SMA cable, needed to bring the calibration plan to the end of the semirigid connector. A line delay is added to take into account the transition from welds to the semirigid connector.

The second step is to use the previously saved calibration file and to replay the positions of the motor, this time with the board connected to the RF tuner. Connect the semi rigid connector to the RF output pin of the chip without components on the RF path. The power is measured for each position (see *Figure 43*).

Figure 42. Calibration

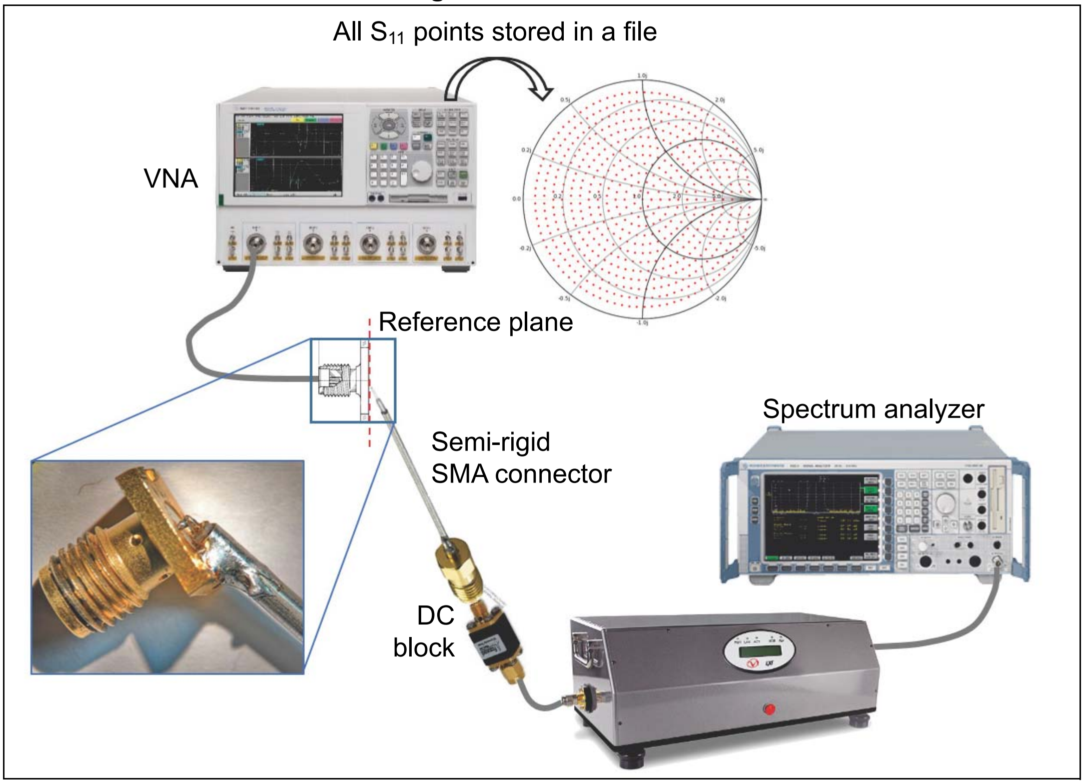
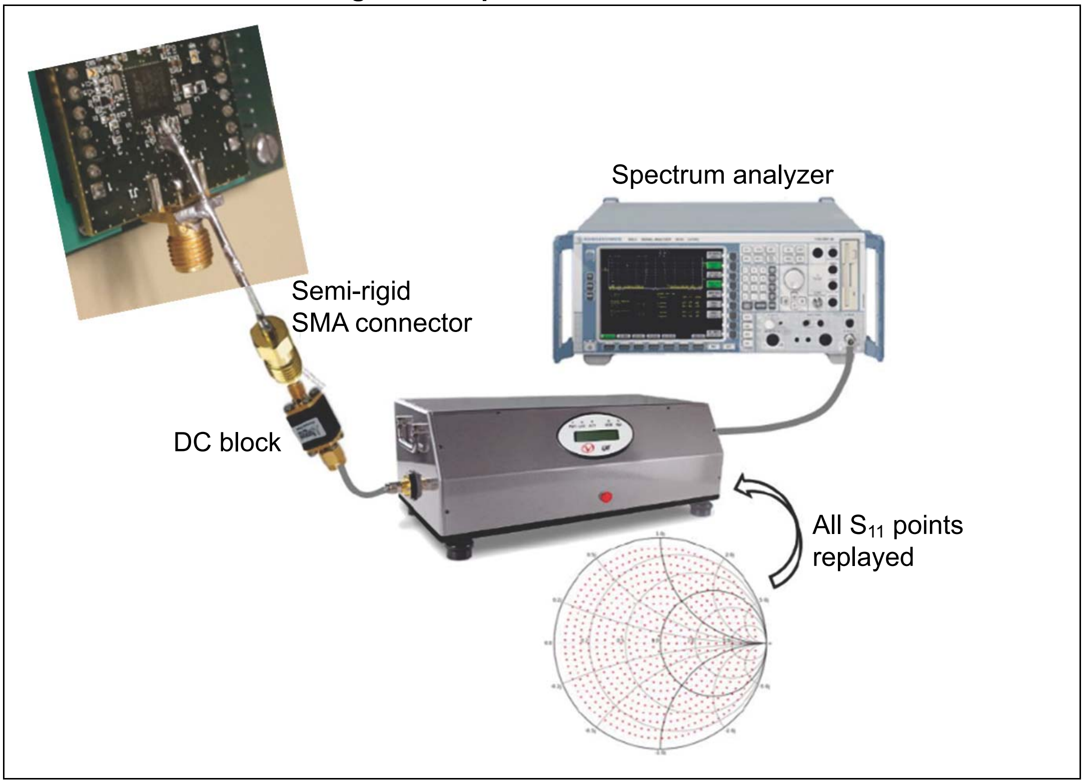
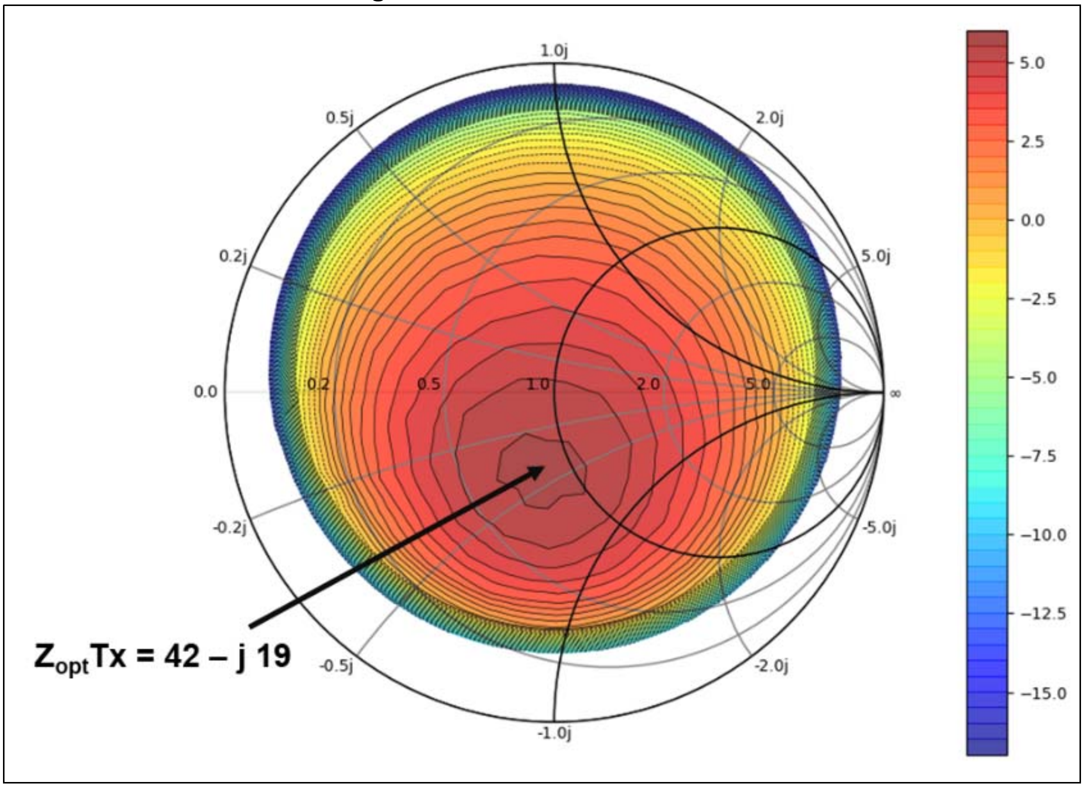


Figure 43. Optimum measurement



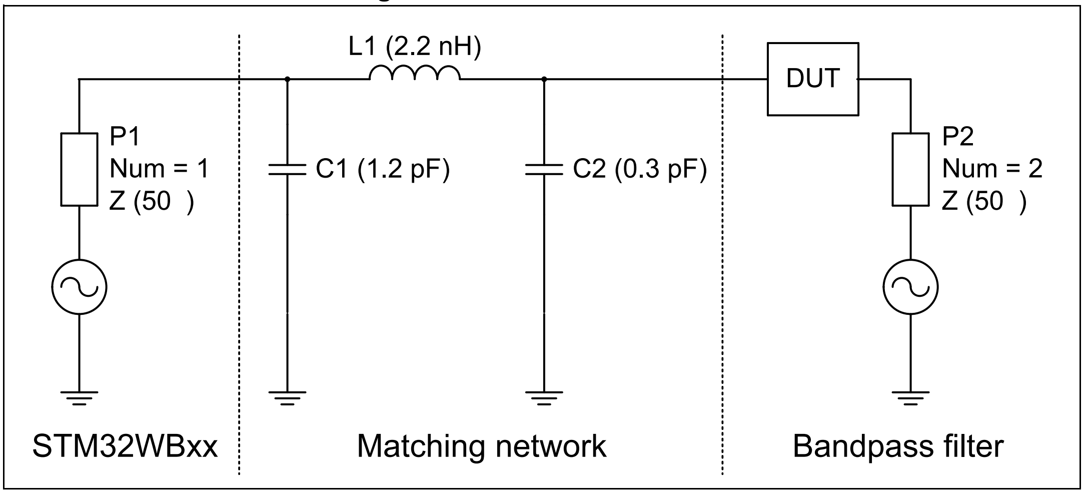
The last step is to analyze the measurement results. The maximum power measured in the Smith chart corresponds to the impedance to present to the RF chip (see *Figure 44*).

Figure 44. Extraction of results



Once the impedance to present to the RF device is known, a simulation tool is needed to determine the value of the components for the corresponding matching network (in this example the ADS simulation tool has been used).

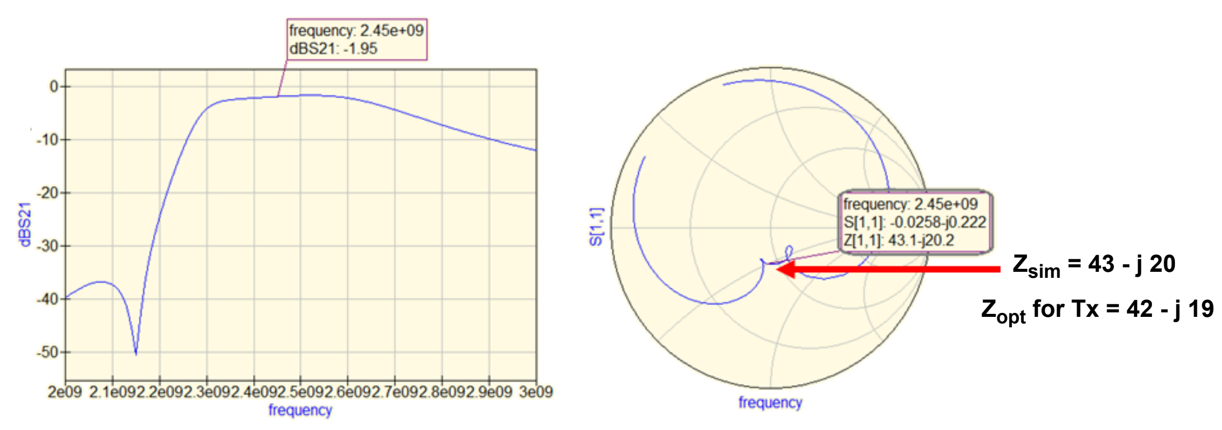
Figure 45. Network simulation



The goal is to find the values of the matching network components to obtain the same impedance at the same frequency as in the load pull measurement. It is recommended to use the complete model of the used components, as provided by the manufacturer (many of them provide S parameters that can be directly used in the simulation tool).

As shown in *Figure 46*, the matching network and the bandpass filter introduce a -1.95 dB insertion loss.

Figure 46. Simulation results



9 Adding an SMA connector to B-WB1M-WPAN1

B-WB1M-WPAN1 is the Connectivity Expansion Board based on the STM32WB1MMC module. It consists of a main board (MB1868) with the module, and an auxiliary board (MB1880) for power supply from USB.

It may be necessary to reconfigure the circuit when tests must be performed in conducted mode, or experiments are carried out with other antenna types. This section describes the needed steps, however it does not cover all possible cases and configurations.

Note: All radio certifications obtained for STM32WB1MMC and/or B-WB1M-WPAN1 are valid only for use with the embedded antenna, as described in the module datasheet (DS14096) and in the board user manual (UM3200), both available on www.st.com. Products based on other antennas require new certifications.

Figure 47. MB1868 top view (with SMA on CN2)

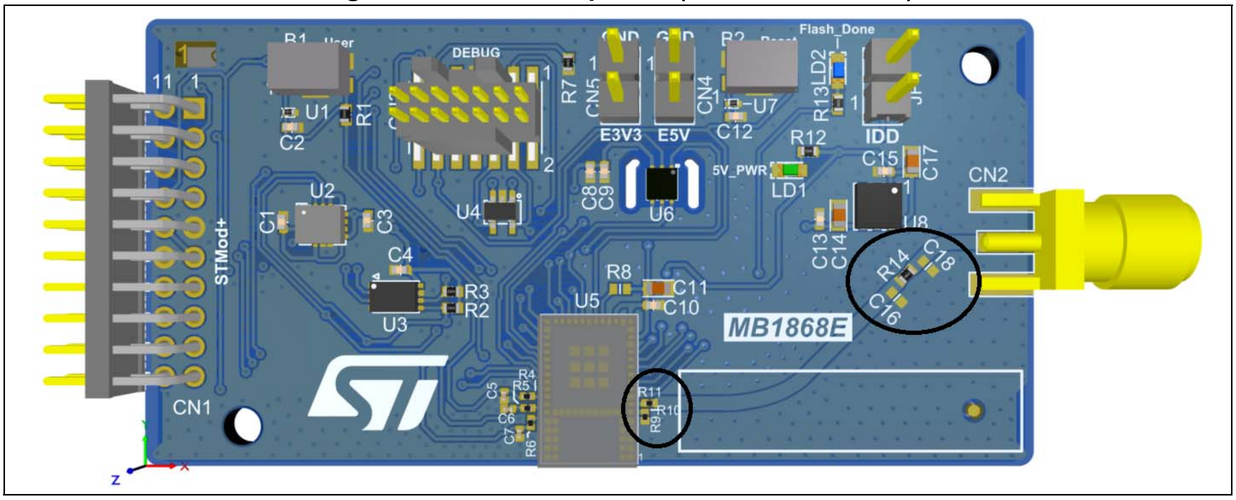


Figure 48. MB1868 block diagram

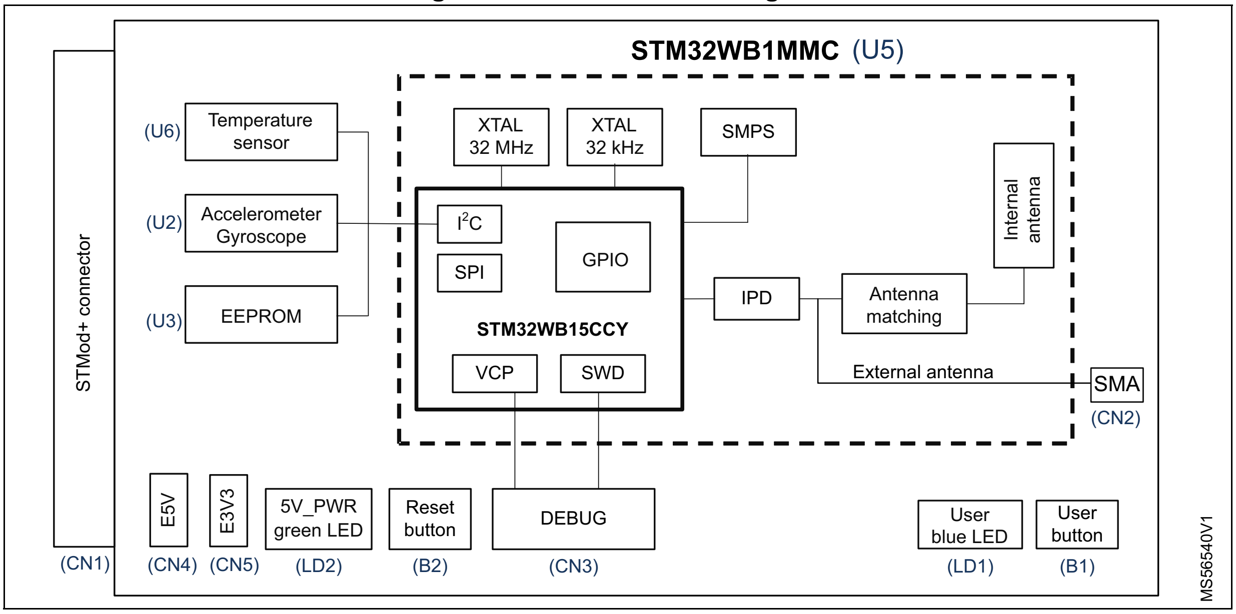
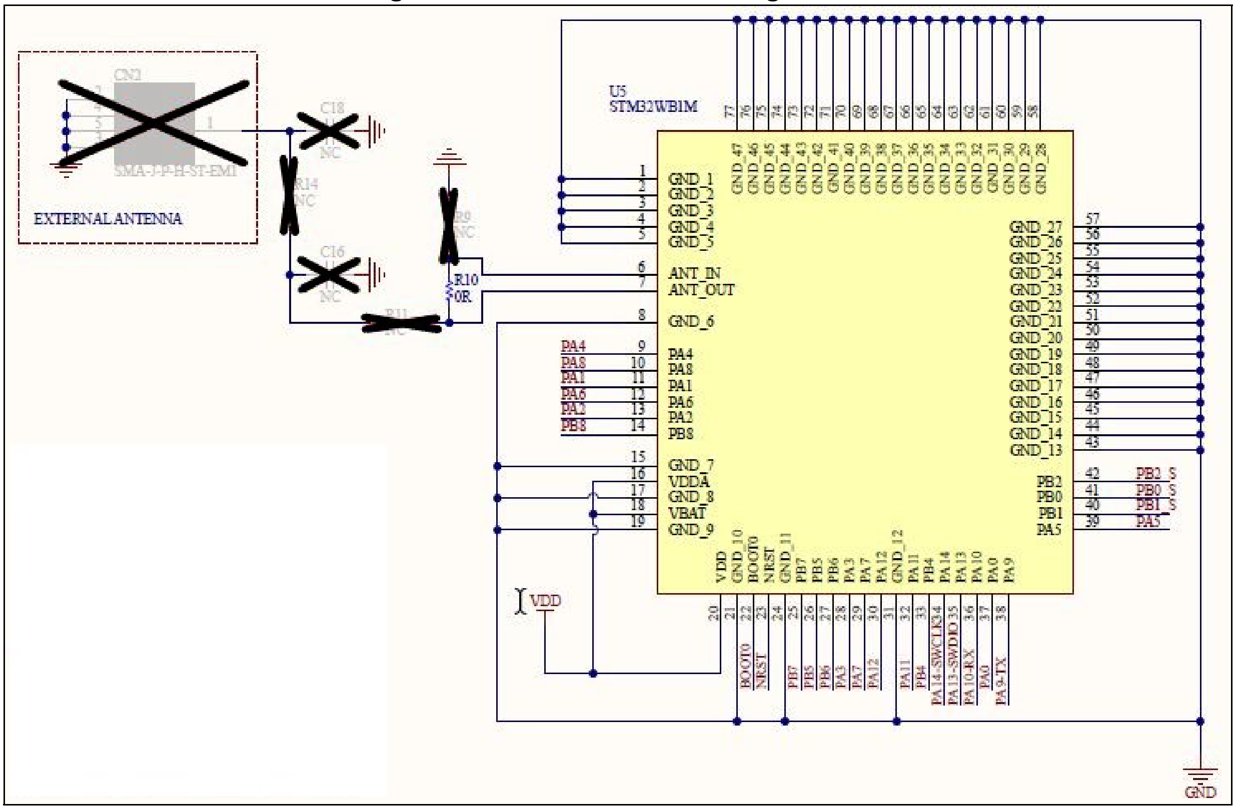


Figure 49 shows the default configuration of MB1868 and STM32WB1MMC for use with the internal antenna. ANT_IN and ANT_OUT are shorted with R10 (a 0 Ω resistor).

Figure 49. MB1868 default configuration



If the board is used to measure the RF output power in conducted mode, the loop from ANT_OUT to ANT_IN must be broken and a connection made to the connector CN2.

1. Remove R10
2. Place a 0 c resistor for R9, R11, and R14
3. Solder an SMA connector to CN2

The RF output power measured at the SMA connector is lower than the RF output power measured directly at ANT_OUT of the module STM32WB1MMC (due to the length of the track a 0.5 dBm loss is expected).

If the board is required to transmit using an external antenna, the loop from ANT_OUT to ANT_IN must be broken. Instead, a path must be created from ANT_OUT to the SMA connector and R14, C16 and C18 must be calculated depending on the impedance of the antenna

1. Remove R10
2. Place a 0 Ω resistors for R9 and R11
3. Place components with suitable values for R14, C16, and C18
4. Solder an SMA connector to CN2

Refer to *Figure 47* to identify resistors and capacitors. The names of these components may be different for other board revisions.

9.1 Practical experiment

As a proof of concept, an experiment has been carried out with the following configuration:

- R10 removed
- R9, R11, and R14 fitted with 0 Ω resistors
- C16 and C18 not fitted
- Antenova Titanis Swivel antenna (50 Ω impedance, average gain of 4.1 dBi) mounted on CN2

The board with antenna was placed in a test chamber in three different positions (see *Figure 50*), the results are detailed in *Figure 51*.

Figure 50. Positions of the board in the test chamber

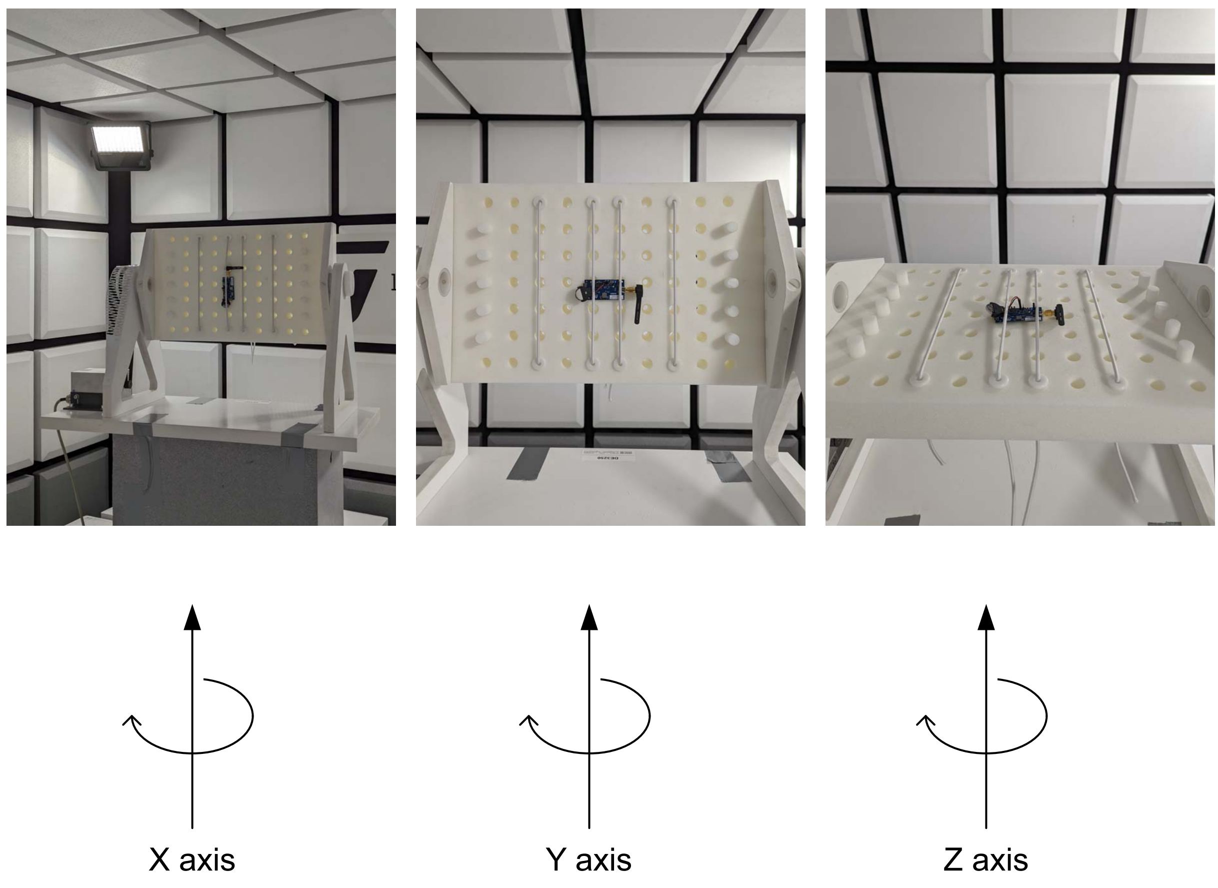
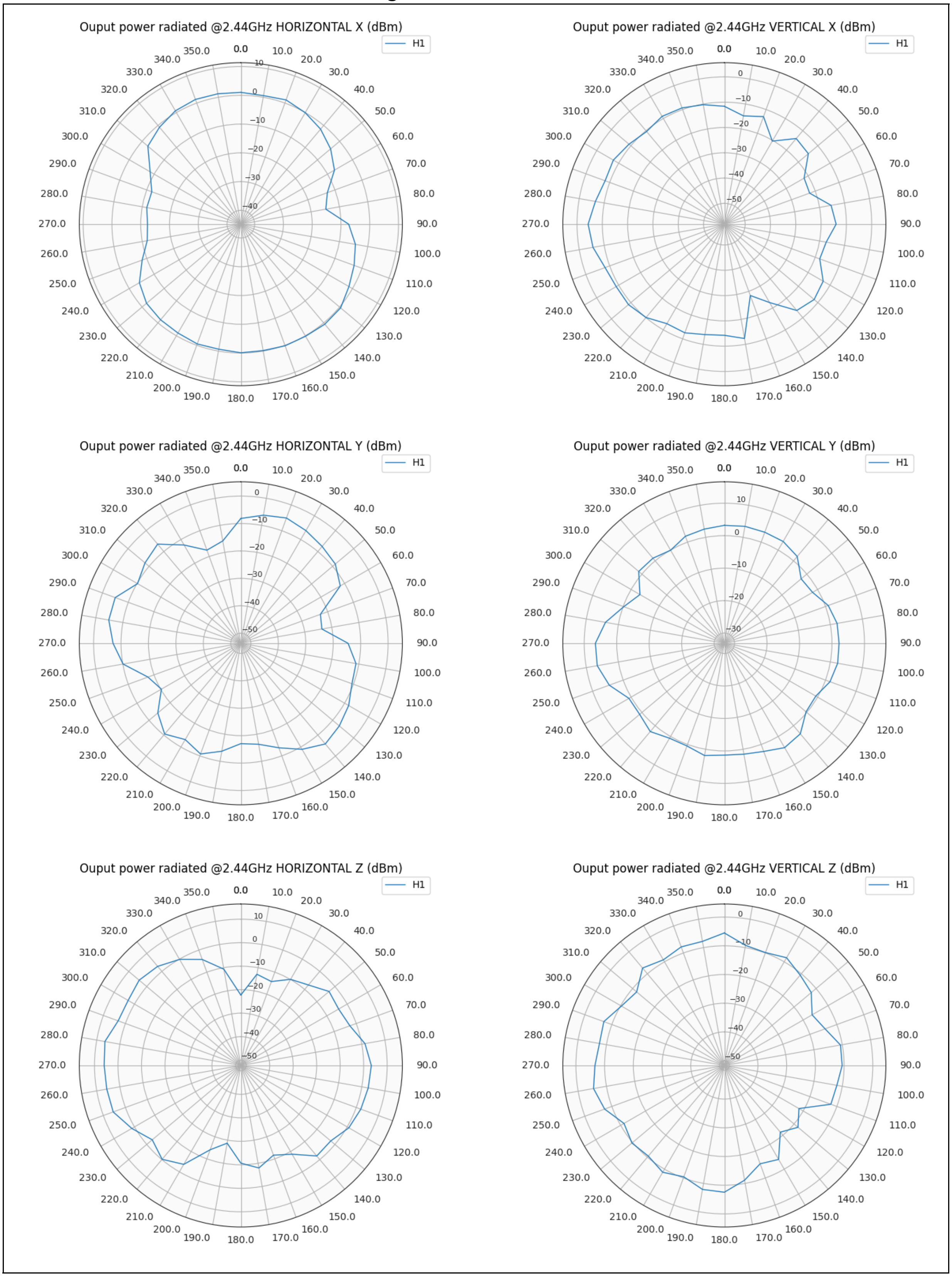


Figure 51. Test results



10 Conclusion

The STM32WB series microcontrollers integrate a high performance RF front-end.

To achieve the best TX and RX performance, several aspects must be addressed during the PCB design:

- choice of the PCB technology (number of layers, substrate technology)
- computation of the antenna matching and filtering network
- floor plan and critical RF component placement and routing
- placement of the SMPS and LSE components (if used)

This application note provides useful guidelines to help the user to reach the performance specified in the datasheets.

11 Revision history

Table 8. Document revision history

Date	Revision	Changes
14-Sep-2018	1	Initial release.
18-Jan-2019	2	Added *Section 7: Reference boards with IPD*.
28-Jan-2019	3	Changed document classification, from ST restricted to public.
24-Sep-2019	4	Updated *Introduction* and *Section 3.3: SMPS*.
25-Oct-2019	5	Introduced WLCSP100 package, hence updated *Introduction*, *Section 2: Reference board schematics* and *Section 3.3: SMPS*. Updated *Table 1: External components*. Updated *Figure 8: UFQFPN48 reference board*, *Figure 9: VFQFPN68 reference board*, *Figure 19: 2-layer PCB - Reference boards for UFQFPN48, VFQFPN68 and UFBGA129*, *Figure 21: 4-layer PCB - Reference board for WLCSP100*, *Figure 18: PCB layout for UFQFPN48 (left to right: all, top and bottom layers)*, *Figure 19: PCB layout for VFQFPN68 (left to right: all, top and bottom layers)*, *Figure 22: PCB layout for WLCSP100 - Detail*, *Figure 23: Detail of PCB layout for the RF*, *Figure 24: VDDSMPS capacitor*, and *Figure 29: Detail of PCB layout for the LSE*. Added *Section 5.1: 2-layer PCB* and *Section 5.2: 6-layer PCB*. Removed MB1355C board and related former *Section 3: Nucleo board (MB1355C) schematics* and *Section 6: 4-layer PCB Nucleo board MB1355C*.
25-Jan-2020	6	Introduced WLCSP100 package, hence updated *Introduction*, *Section 4.4: 2-layer PCB* and *Section 7: Reference boards with IPD*. Updated *Figure 8: UFQFPN48 reference board*, *Figure 9: VFQFPN68 reference board*, *Figure 11: WLCSP100 reference board*, *Figure 23: Detail of PCB layout for the RF*, *Figure 24: VDDSMPS capacitor*, *Figure 29: Detail of PCB layout for the LSE*, and *Figure 29: Detail of PCB layout for the LSE*. Updated caption of *Figure 19: 2-layer PCB - Reference boards for UFQFPN48, VFQFPN68 and UFBGA129* and of *Figure 21: 4-layer PCB - Reference board for WLCSP100*. Added *Figure 10: UFBGA129 reference board*, *Figure 20: PCB layout for UFBGA129*, *Figure 38: RF performance of the MLPF-WB55-02E3*, and *Table 7: References*.

Table 8. Document revision history

Date	Revision	Changes
24-Nov-2020	7	Added *Section 4.3: Ground planes*, *Section 6: Layout recommendations for reference boards*, *Section 8: Matching network determination* and their subsections. Removed former *Section 4.3: 2-layer PCB* and *Section 4.4: 4-layer PCB.* Updated *Section 5.2: 6-layer PCB*. Updated *Figure 10: UFBGA129 reference board*, *Figure 11: WLCSP100 reference board*, *Figure 20: PCB layout for UFBGA129*, *Figure 22: PCB layout for WLCSP100 - Detail*, *Figure 23: Detail of PCB layout for the RF*, *Figure 24: VDDSMPS capacitor*, and *Figure 29: Detail of PCB layout for the LSE*. Added *Figure 21: PCB layout for WLCSP100 - All layers*. Minor text edits across the whole document.
11-Apr-2022	8	Updated *Section 3.4: External crystal*. *Section 5.3.2: SMPS*, *Section 6.4: Isolation*, *Section 6.8: SMPS*, and *Section 6.9: Check list*. Updated *Figure 8: UFQFPN48 reference board*, *Figure 9: VFQFPN68 reference board*, *Figure 10: UFBGA129 reference board* and *Figure 11: WLCSP100 reference board*, and added notes to each of them. Updated *Figure 20: PCB layout for UFBGA129*, *Figure 21: PCB layout for WLCSP100 - All layers*, *Figure 22: PCB layout for WLCSP100 - Detail*, and *Figure 34: XTAL positioning*.
30-Mar-2023	9	Updated document title. Updated *Table 1: External components* and *Table 7: References*. Updated *Figure 8: UFQFPN48 reference board*, *Figure 9: VFQFPN68 reference board*, *Figure 10: UFBGA129 reference board*, and *Figure 11: WLCSP100 reference board*, and removed their notes. Added *Section 6.1.1: Behavior of the STM32WB according to the ripple on VDD*. Minor text edits across the whole document.
03-Apr-2024	10	Added *Section 9: Adding an SMA connector to B-WB1M-WPAN1* and its subsections. Minor text edits across the whole document.