Displaying variable voltage on a bar of LEDs using STM8 Nucleo-64 boards

Introduction

The NUCLEO-8S208RB (built around the STM8S208RBT6 device) and the NUCLEO-8L152R8 (built around the STM8L152R8T6 device) are boards that allow the evaluation of the main features of all the STM8S Series and STM8L Series microcontrollers.

This application note provides a short description on how to use the ADC, TIM and GPIO peripherals on the NUCLEO-8S208RB and on the NUCLEO-8L152R8.

Once the microcontroller (STM8S208RBT6 or STM8L152R8T6 in this example) has been powered-up through a USB cable connected to the host PC, the timer triggers the ADC according to a user-defined period to convert the analog voltage provided by variable resistor RV1 (10 KΩ variable resistor). The resulting average voltage measurement is represented on the LED bar.

Table 1. Applicable products

Type	Part number
Evaluation boards	NUCLEO-8S208RB
	NUCLEO-8L152R8

Reference documents

- *STM8 Nucleo-64 boards* data brief (DB3591)
- *STM8L152R8T6 Nucleo-64 board* user manual(UM2351)
- *STM8S208RBT6 Nucleo-64 board* user manual (UM2364)

1 Application description

This section describes the hardward requirements, the application's schematics and the application's principle to display a variable voltage on a bar of LEDs using the NUCLEO-8S208RB or the NUCLEO-8L152R8 boards.

1.1 Hardware requirements

No on-board resources are used.

External resources needed are:

- Four LEDs: LD2, LD3, LD4, LD5
- One 10-KΩ variable resistor: RV1
- Four 1-KΩ resistors: R1, R2, R3, R4
- One 100-nF capacitor: C1.

1.2 Application schematics

Capacitor C1 filters the voltage spike on the ADC input pin:

- ADC2_IN9 on PIN PE6 for NUCLEO-8S208RB
- ADC1_IN3 on PIN PC7 for NUCLEO-8L152R8

Resistors R1, R2, R3 and R4 limit the current going into LD2, LD3, LD4 and LD5 respectively.

Figure 1. STM8S Series application schematic

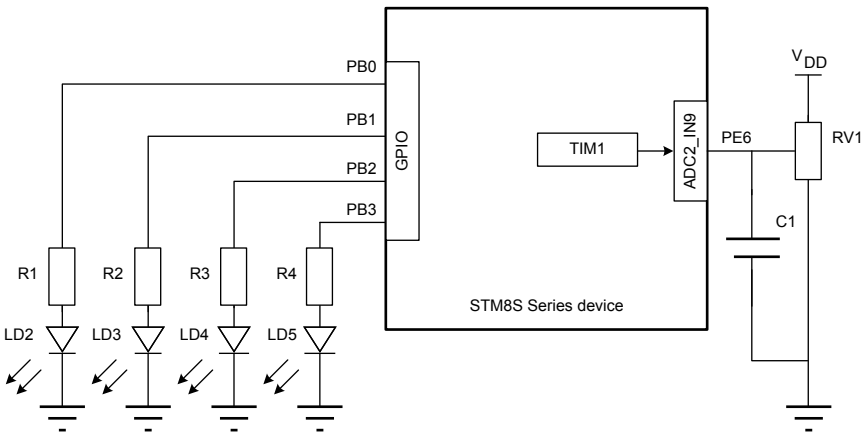
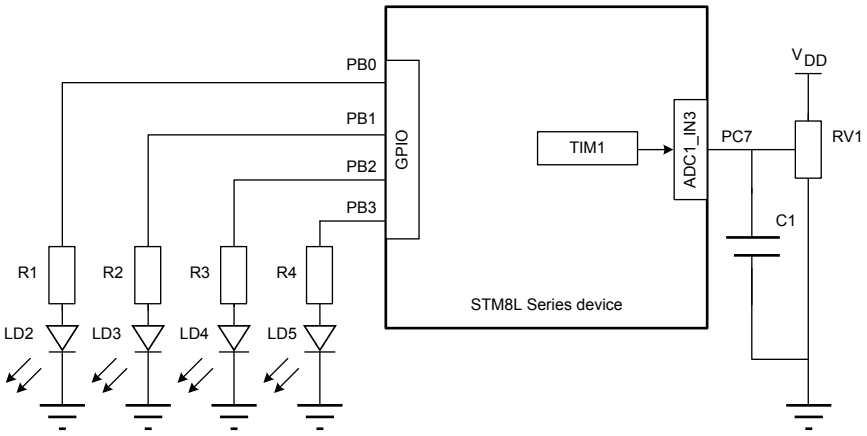


Figure 2. **STM8L Series application schematic**



1.3 Application principle

This application uses the ADC1 or ADC2, TIM1 and GPIO peripherals.

The input's voltage analog signal from variable resistor RV1 is different in each board:

- NUCLEO-8S208RB: sampled and filtered on channel 9 of the ADC2 system (PE6), internally triggered by TIM1
- NUCLEO-8L152R8: sampled and filtered on channel 3 of the ADC1 system (PC7), internally triggered by TIM1

The average value of this signal is represented on the LED bar (LD2-5).

Note: Even if by default the devices (STM8S208RBT6 or STM8L152R8T6) are powered with 3.3 V, on the STM8S board the user has the possibility to switch the MCU VDD power supply from 3.3 V to 5 V.

Table 2. **Voltage and LED correspondence**

Voltage (V)(1)	LEDs switched on
0.0 - 0.4	None
0.4 - 1.25	LD2
1.25 - 2.0	LD2 + LD3
2.0 - 2.8	LD2 + LD3 + LD4
2.8 - 3.3	LD2 + LD3 + LD4 + LD5

1. *This range values are true only with the default power supply configuration of 3.3 V.*

2 Software description

This application does not use neither the STM8S Series / STM8L Series standard libraries nor the STM8 touch sensing library. The peripherals used in this application are:

- **ADC:**voltage acquisition. Must be configured as:
  - Single conversion mode
  - External trigger by TIM1 TRGO
  - ADC_clock = Fmaster/2 for STM8L or Fmaster/8 for STM8S
  - Left alignment result (otherwise a software modification is required to calculate the average)
  - Disable Schmitt trigger on ADC input 9 for STM8S Series and on ADC input 3 for STM8L Series.
- **TIM1:** Timer TIM1 has two aims in this application:
  - To wake up the ADC for incoming conversion when the counter value reaches CCR1 (capture/compare interrupt). This action is very useful to allow ADC stabilization time before the conversion.
  - To send a conversion trigger signal to launch the ADC conversion when the counter value reaches TIM1_ARR.

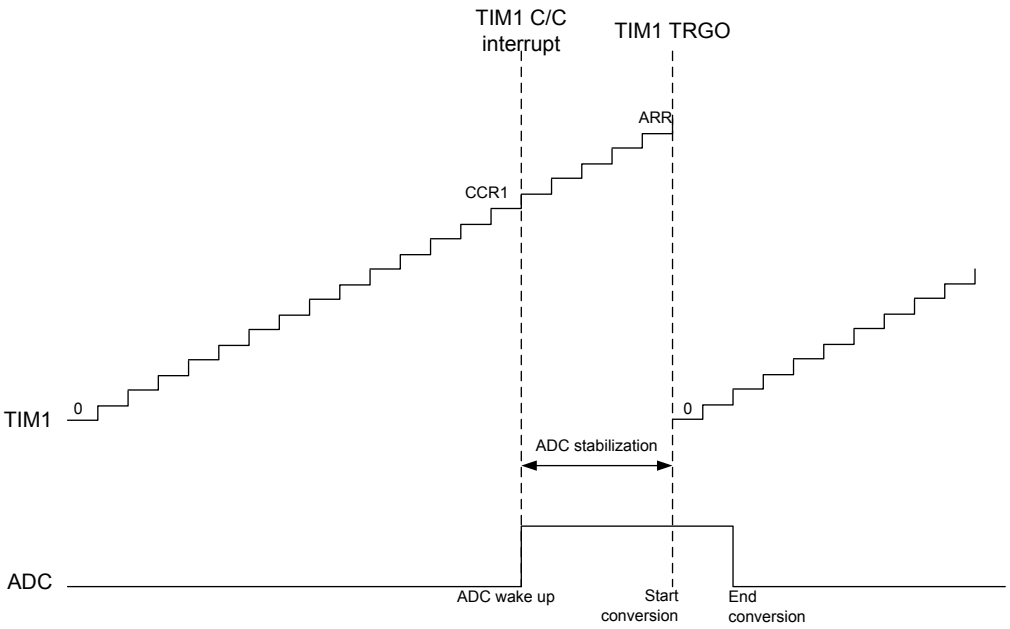
Note: With these two events the user can easily manage ADC wake-up and conversion timings. For this use, TIM1 must be configured with compare-OC1REF trigger output and PWM1 mode on PC1 (negative polarity): for testing purpose (to measure exactly the time allowed for stabilization)

- **GPIO:** configures PB0, PB1, PB2 and PB3 in output push/pull mode to control LEDs LD2, LD3, LD4 and LD5.

The ADC adquisition principle is described in the list below and illustrated in the figure just after.

1. TIM1 is configured as an upcounting counter.
2. When the compare/capture interrupt occurs, the ADC is woken up for the incoming conversion (the stabilization time of the ADC is respected before the ADC conversion).
3. On TIM1 TRGO, the ADC starts the conversion.
4. When the conversion is finished, the result is stored in RAM and the ADC is powered down until the next compare/capture interrupt.
5. When eight conversion results have been stored, the main routine calculates the average of these results and displays it on the LED bar.

Figure 3. **ADC acquisition principle**

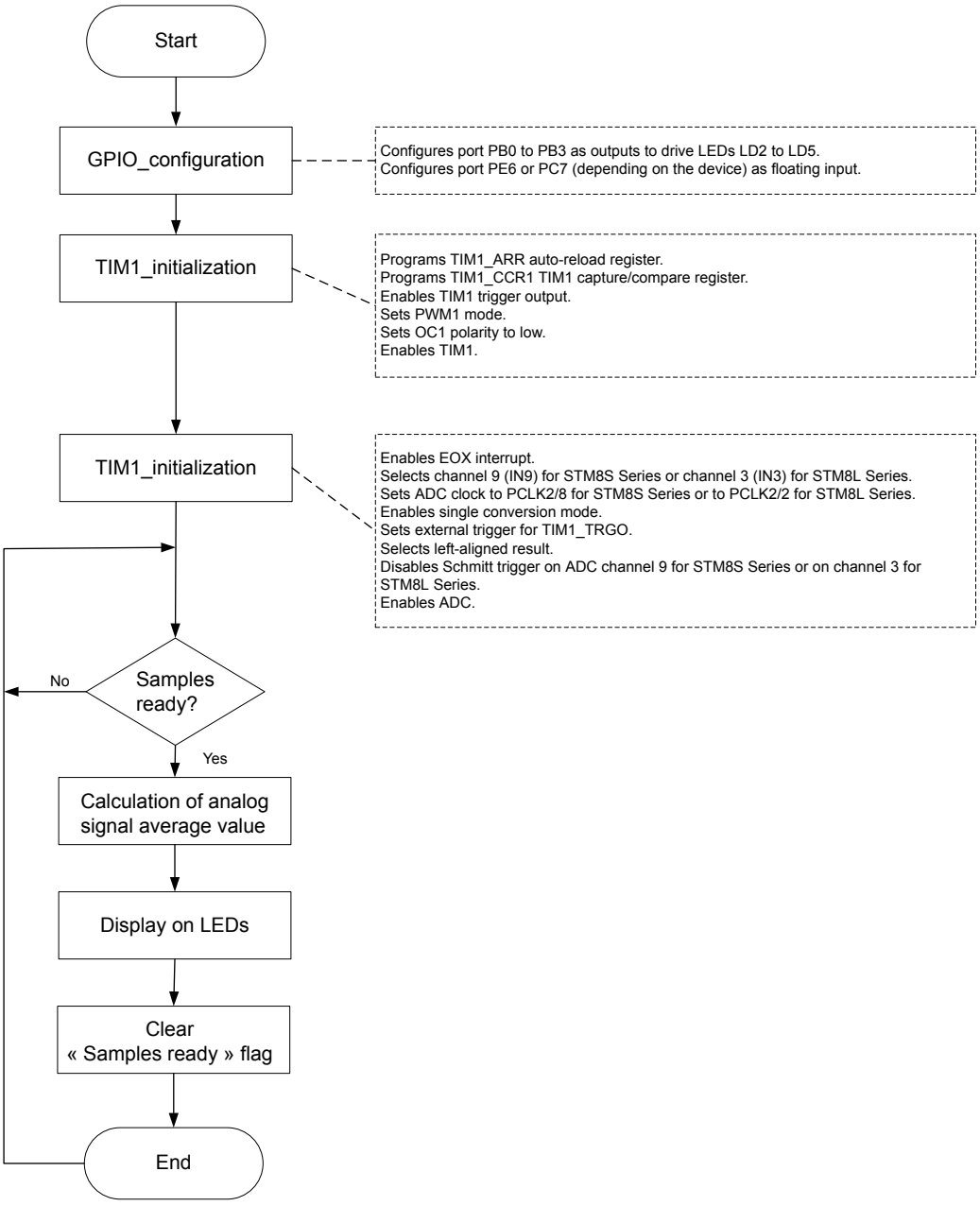


2.1 Application software flowcharts

This section contains the main loop flowchart, the ADC interrupt routine flowchart and the TIM1 capture/compare interrupt flowchart.

2.1.1 Main-loop flowchart

Figure 5. **Main-loop flowchart**

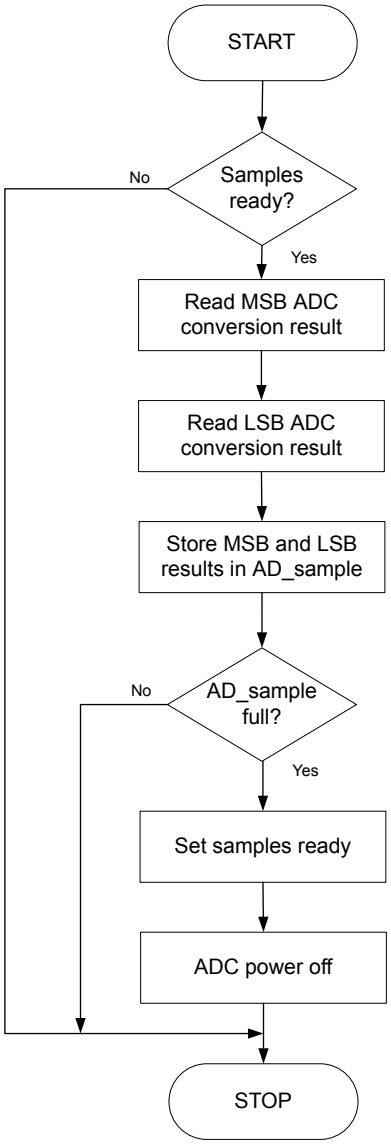


2.1.2 ADC interrupt routine

This interrupt occurs when the ADC1 has finished an analog to digital conversion. Every time it occurs the conversion result is stored in a table called AD. When this table is full, the variable *ADSampRdy* is set to 1 and the AD table is treated by the main routine (it calculates the average of the stored values). The ADC is switched off at the end of the interrupt routine.

Note: The result is stored only if the previous AD table has been treated by the main routine.

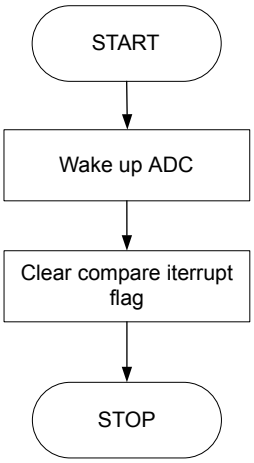
Figure 6. ADC EOC interrupt flowchart



2.1.3 TIM1 capture/compare interrupt

This interrupt occurs each time the TIM1 counter value is equal to the compare register value CCR1. During this interrupt process, conversion is triggered by setting the ADON bit of the CR1 register.

Figure 7. **TIM1 capture/compare flowchart**



Revision history

Table 3. **Document revision history**

Date	Version	Changes
29-Jun-2018	1	Initial release.

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