AN5246
Application note

How to use SMPS to improve power efficiency on STM32WB MCUs

Introduction

This document describes how the use the SMPS (switched mode power supply) integrated in microcontrollers of the STM32WB Series. It is intended to be used by system architects and by HW and board-level SW developers.

The patented implementation detailed in this document differs from the standard ones because it is able to maintain the RF transceiver full performance while, at the same time, providing the best power figure in burst application like those generally used by Bluetooth® Low Energy and IEEE 802.15.4 protocols.

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1 Description

STM32WB series microcontrollers are based on Arm®(a) cores. They embed a powerful SMPS that can be used to improve power efficiency when the supply voltage is high enough. The efficiency increases when the difference between V_{FBSMPS} and V_{DD} is high.

In order not to disturb the RF performance, the switching frequency of this SMPS is synchronous with the RF main clock source HSE. The allowed frequencies for the SMPS are 4 or 8 MHz. During the RF startup phases from low power modes, the HSI is used instead of HSE, resulting in a faster wake-up time (no need to wait for the HSE stabilization before starting the SMPS and the digital logic).

Two specifics features have been added to this step-down SMPS in association with all the low power modes supported by STM32WB microcontrollers:

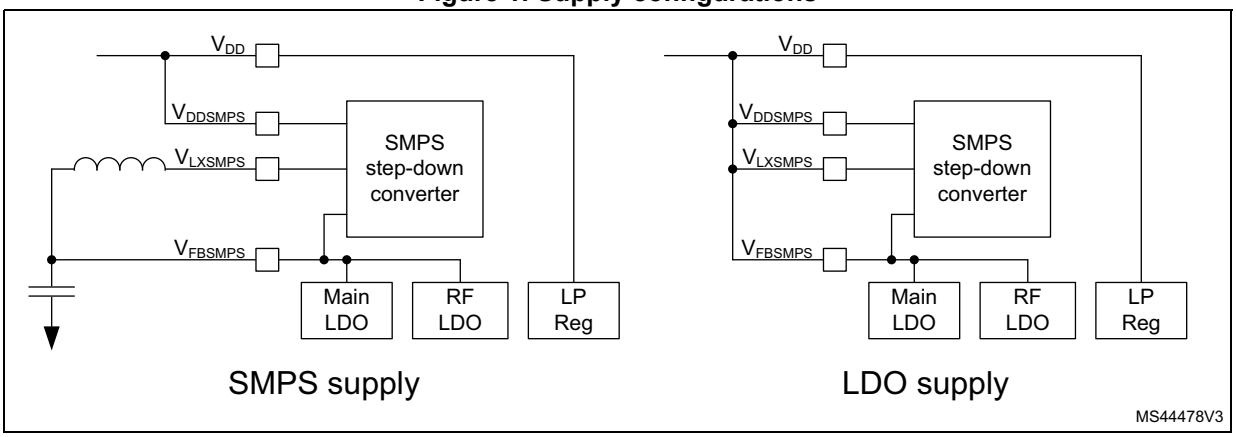
- BYPASS mode: capability for the SMPS to be bypassed (the current continues to flow through its coil), the V_{DDSMPS} voltage is directly connected to V_{LXSMPS}. An additional hardware mechanism allows the SMPS to automatically switch to the BYPASS mode if the V_{DD} voltage falls below a given level (V_{BORH}), ensuring smooth operation even at very low operating voltages.
- OPEN mode: the SMPS output (V_{LXSMPS}) is open from any circuitry, and the load of the SMPS bulk capacitance is kept. This makes it possible to speed up the wake-up time, by having the bulk capacitance precharged.

The internal state machine manages these states automatically when entering and exiting the low power modes.

1.1 Power distribution configurations

Two wiring configurations can be used, depending upon the global application, targeted power and cost.

Figure 1. Supply configurations



a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1.1 SMPS configuration

In this configuration, the SMPS can be used to provide the internal supply to the MCU.

It is not possible to use the SMPS output (V_{FBSMPS}) to supply any external circuitry, as its voltage and current capability are impacted by internal device states. For example, the SMPS nominal voltage depends upon the RF Tx level, and the current capability depends upon the MCU low power state (OPEN mode).

Note: This PCB configuration can be used also without the inductor, replacing it by a 0 Ω in BYPASS mode, similarly to the LDO configuration. In this case, the SMPS must be not enabled.

1.1.2 LDO configuration

In this configuration the SMPS is not used and V_{DDSMPS}, V_{LXSMPS}, and V_{FBSMPS} must be connected to V_{DD}.

This configuration is recommended when the V_{DD} is low (below 2.0 V), or if power consumption is not the major concern, but rather the size of the PCB and the number of external components are (gaining two inductors and one capacitor).

In this configuration, this section does not apply. All SMPS register must not be modified from their default reset value.

1.1.3 External components

To operate properly the SMPS needs two inductors and two capacitances, their values depend upon the targeted performance, the PCB area and the total height allowed in the mechanical design.

For best power performance 4 MHz should be selected, which leads to an inductor of 10 µH associated with a bulk capacitance of 4.7 µF.

For smaller footprint, and especially to enable the use of very low profile inductors, the 8 MHz can be selected, making it possible the use of a 2.2 µH inductor associated with a 4.7 µF bulk capacitance.

Another 4.7 µF capacitor must be used to decouple the V_{DDSMPS} supply.

All these components must have the lowest possible ESR values and good performance at high frequencies.

For all packages it is advised to add an extra 10 nH inductor in series with the 10 or 2.2 µH one. This is needed to filter the RF harmonic that can degrade the receiver performance.

Note: V_{DDSMPS} must be connected to V_{DD} and the voltage rising and falling must satisfy the conditions described in the data sheet.

1.2 SMPS calibration

The SMPS voltage is calibrated in production at 1.50 V reference voltage. Two flash memory locations contain the values to use when selecting the SMPS output voltage.

- *SMPS_coarse_engi_trim* (last four bits of the FLASH address 0x1FFF7559) contains a number (normally between 4 and 10) corresponding to the 1.5 V reference point. This

value is automatically applied to the SMPS by the hardware, but can be overridden by writing PWR_CR5.SMPSVOS bits.

- *SMP_fine_engi_trim* (byte at the FLASH address 0x1FFF7549) are automatically applied to the SMPS by the hardware.

1.3 SMPS programming

1.3.1 Programming registers

A set of registers allows the user to enable the SMPS, and to select its clock frequency (8 or 4 MHz), output voltage, and max current capability. It can also enable the automatic fall-back to BYPASS mode if the V_{DD} voltage drops below a given level (V_{BORH}).

PWR_CR5.SMPSEN (Read/Write)

Enables SMPS step-down converter. This bit must be set to enable the SMPS.

- 0: SMPS step-down converter SMPS mode disabled.
- 1: SMPS step-down converter SMPS mode enabled.

This bit is reset to 0 when the SMPS is automatically switched to Standby mode due to the V_{DD} voltage falling below the BORH threshold (assuming PWR_CR5.BORHC = 1).

Default value: 0 (this bit is not reset when existing from Standby mode).

V_{DDSMPS} must be higher than 1.95 V when the SMPS is enabled.

PWR_CR5.SMPSVOS[3..0] (Read/Write)

SMPS step-down converter voltage output setting. Refer to *Section 2.1* to select the appropriate SMPS output voltage.

SMPS step-down converter output voltage is given by the equation

$$V_{FBSMPS} = 1.5\ V + (SMPSVOS - SMPS\_coarse\_engi\_trim) \times 50\ mV$$

which gives

$$SMPSVOS = (V_{FBSMPS} - 1.5\ V) / 50\ mV + SMPS\_coarse\_engi\_trim$$

These bits are initialized at startup with the factory-programmed value corresponding to the trimming voltage (1.5 V[(a)]), and can be updated by overwriting them.

PWR_CR5.SMPSSC[2..0] (Read/Write)

SMPS step-down converter maximum output current selection. This value can be changed when the application supply is unable to deliver the default maximum current.

Maximum SMPS output current is limited to 80 mA + SMPSSC x 20 mA.

Default value: 7 (220 mA max): this bit is not reset when existing from Standby mode.

Note that the current limitation is approximate (±30%).

a. V_{DD} = 3 V, T = 25 °C, I_{load} between V_{FBSMPS} and ground = 10 mA.

The current limitation impacts the peak current when waking up from low power modes, and the SMPS efficiency. The SMPS efficiency degradation starts to be measurable at one half of the limitation value. The highest the current limitation, the best is the SMPS efficiency, but also the highest is the peak current when waking up.

The current limitation has also an effect on the wake-up time, as described in *Section 2.2*.

PWR_CR3.EBORHSMPSFB (Read/Write)

Enables CPU1 Interrupt when BORH forces the SMPS in BYPASS mode.

- 0: Interrupts BORHF and SMPSFBF to CPU1 disabled.
- 1: interrupts BORHF and SMPSFBF to CPU1 enabled.

Default value: 0 (this bit is not reset when existing from Standby mode).

CPU1 needs to manage the V_{DD} rising using the PVD or ADC to switch back from BYPASS to SMPS mode.

PWR_CR5.BORHC (Read/Write)

BORH configuration selection.

- 0: BORH generates a system reset.
- 1: BORH forces SMPS step-down converter in BYPASS mode. BORL generates a system reset if V_{DD} continues to fall.

Default value: 0 (this bit is not reset when existing from Standby mode).

Note: To operate properly, the BORH Level must have been programmed in the corresponding option byte (0x1FFF8000.BORLEV[2..0] > 000). If the BORH function is enabled, it adds an extra consumption of about 1.1 µA in all low power modes.

RCC_SMPSCR.SMPSSEL[1..0] (Read/Write)

SMPS step-down converter clock selection. Set by software to select SMPS step-down converter clock source (SMPSCLK).

- 00: HSI selected as SMPS step-down converter clock
- 01: MSI selected as SMPS step-down converter clock (the MSITRANGE must be set to a supported value, one among 16, 24, 32 or 48 MHz)
- 10: HSE selected as SMPS step-down converter clock
- 11: Reserved

Warning: Before entering low power modes (Stop1, Stop2, Standby, or Shutdown), set the SMPSSEL to select the same clock source selected for the system clock in SW in Clock configuration (RCC_CFGR) register.

Note: As the RF can force the SMPS to use the HSE clock, at any given time the real SMPS clock in use must be read in RCC_SMPSCR.SMPSSWS[1..0]. Recommended choices are HSI and HSE.

RCC_SMPSCR.SMPSDIV[1..0] (Read/Write)

SMPS step-down converter clock prescaler. Set by software to control the division factor of the SMPS step-down converter clock.

- 00: SMPS clock is 8 MHz, valid only for HSI, HSE, and MSI (16, 32 or 48 MHz)
- 01: SMPS clock is 4 MHz, valid only for HSI, HSE, and MSI (16, 24, 32 or 48 MHz)
- 1x: Reserved

PWR_SCR.CSMPSFBF (Write only)

Clears SMPS step-down converter forced in BYPASS interrupt flag for CPU1 (enabled with PWR_CR3.EBORHSMPSFB = 1). Setting this bit clears the SMPSFBF flag in the PWR_SR1. This bit is always read 0.

1.3.2 Status registers

PWR_SR2.SMPSF (Read only)

SMPS step-down converter SMPS mode Ready status. This bit indicates that the SMPS step-down converter is in SMPS regulation mode. This bit can be used to check that the SMPS has finished its transition from the BYPASS mode to the RUN mode and that its targeted output voltage, described in PWR_CR5.SMPSVOS[3..0] has been reached.

- 0: the SMPS step-down converter is not ready.
- 1: the SMPS step-down converter is ready.

PWR_SR1.SMPSFBF (Read only)

This bit is set when the SMPS step-down converter is enabled in SMPS mode and forced in BYPASS mode due to the BORH threshold. This bit can be used to detect that the interrupt event has occurred and this bit must be cleared with PWR_SRR.CSMPSFBF.

- 0: the SMPS step-down converter is not in BYPASS mode (either in OPEN or SMPS mode).
- 1: the SMPS step-down converter has been forced in BYPASS mode due to the automatic BYPASS mode selection and V_{DD} voltage has decreased below BORH value.

Default value: 0 (this bit is not reset when existing from Standby mode).

PWR_SR2.SMPSBF (Read only)

SMPS step-down converter bypass mode status. This bit indicates that the SMPS step-down converter is in BYPASS mode.

- 0: the SMPS step-down converter is not in BYPASS mode (either in OPEN or SMPS mode).
- 1: the SMPS step-down converter is in BYPASS mode.

RCC_SMPSCR.SMPSSWS[1..0] (Read only)

SMPS step-down converter clock switch status. Set and cleared by hardware to indicate which clock source is currently used as SMPS step-down converter clock when SMPS is enabled. Whenever the HSE is active it is used regardless of the settings in SMPSSEL.

Whenever the SMPS step-down converter is disabled in PWR_CR5.SMPSEN no clock is used.

- 00: HSI oscillator used as SMPS step-down converter clock
- 01: MSI oscillator used as SMPS step-down converter clock
- 10: HSE used as SMPS step-down converter clock
- 11: no clock used

Reset value: 3 (no clock).

1.4 Selecting SMPS clock on exit from low power modes

On a POR or NRST pin reset or when waking up from Shutdown the SMPSSEL is forced by hardware to select MSI (value b01). When waking up from Standby the SMPSSEL is forced by hardware to select HSI (value b00). When waking up from Stop modes the SMPSSEL is forced by hardware to select the MSI or HSI clock as defined in RCC_CFGR.STOPWUCK.

2 SMPS impact at system level

2.1 Selecting the output voltage

The application need to set the SMPS voltage according with different parameters:

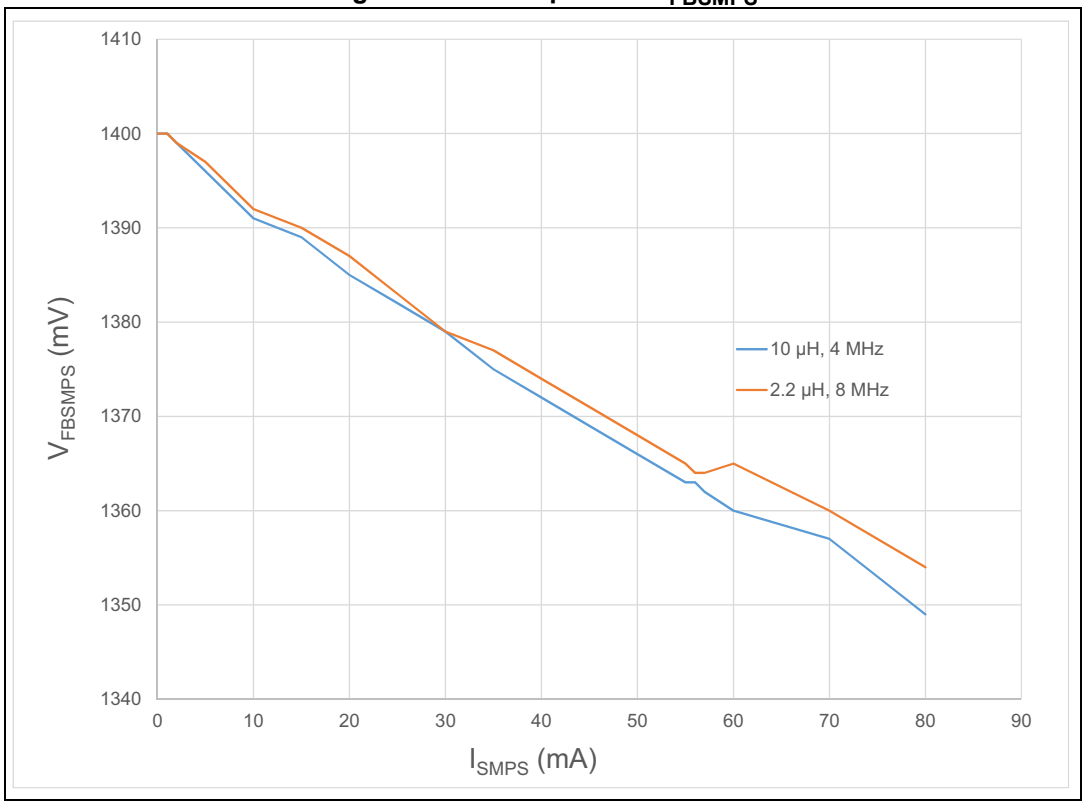
- minimum voltage requirement for the digital part to operate properly
- minimum voltage requirement to properly transmit, with no distortion, the wanted maximum RF transmit signal
- margin due to V_{FBSMPS} load current consumption
- margin due to accuracy of the SMPS production trimming.

To operate properly, the digital part of the microcontroller needs that the V_{FBSMPS} never drops below 1.4 V. For the RF part, the V_{FBSMPS} must be set to a voltage depending upon the wanted TX signal:

- ≥ 1.40 V for TX codes ≤ 29
- ≥ 1.55 V for TX code 30
- ≥ 1.70 V for TX code 31 (maximum power)

The SMPS has a load regulation, and V_{FBSMPS} depends upon the I_{SMPS} current consumed by the STM32WB. Note that the maximum SMPS output current capability is 80 mA overall. *Figure 2* illustrates a measurement of the load impact on the SMPS output voltage (independent from V_{DD}, and the impact of the 10 nH inductor on the V_{FBSMPS} is very low).

Figure 2. Load impact on V_{FBSMPS}



Note: The V_{FBSMPS} load impact depends on the selection of the coil and can be significantly worse at high (>85 °C) temperatures.

Finally, the SMPS trimming is performed with a ±10 mV accuracy.

2.1.1 Numerical examples

If we design a product with a maximum TX level of +0 dBm (Tx Code = 25) and a digital activity at 30 mA maximum, then we have to set the V_{FBSMPS} at a voltage higher than 1.4 V + 21 mV (see *Figure 2* to calculate the load impact independently from V_{FBSMPS}) + 10 mV (trimming accuracy), that is V_{FBSMPS} > 1.431 V, which gives 1.450 V (V_{FBSMPS} = 1.45 V to be used in the equation defined in *Section 1.3.1*).

If we design a product with a maximum TX level of +6 dBm (Tx Code = 31) and a digital activity at 50 mA maximum, then we have to set the V_{FBSMPS} at a voltage higher than 1.7 V + 34 mV (see *Figure 2* to calculate the load impact independently from V_{FBSMPS}, for the 10 µH case)+ 10 mV (trimming accuracy), that is V_{FBSMPS} > 1.744 V, which gives 1.750 V (V_{FBSMPS} = 1.75 V to be used in the equation defined in *Section 1.3.1*).

It is worth to remind that the SMPS efficiency increases when the difference between V_{FBSMPS} and V_{DD} is high.

2.2 Startup time when in Stop1 or Stop2 mode

The SMPS is automatically stopped when entering Stop1 or Stop2 modes.

To save power, its output capacitor is kept charged while in Stop1 / Stop2 modes. The capacitor charge evolves because of the various leakage currents (capacitor, PCB, STM32WB input), so its voltage is different when the system wakes up. Before restarting the CPU, it is important that the capacitor voltage has reached at least 1.4 V, to ensure proper operation of the digital part of the chip. A special mechanism ensures to release the CPU only if this voltage is high enough.

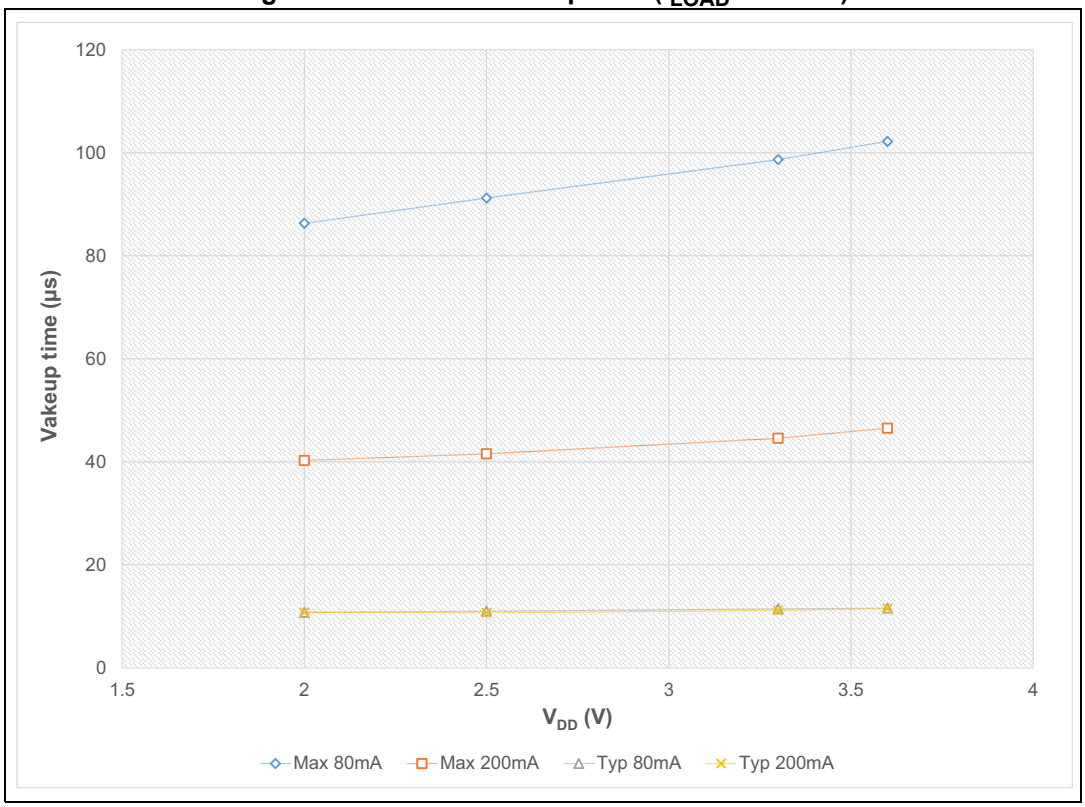
When restarting from Stop1 / Stop2, STM32WB MCUs start the SMPS (and its clock system) only when V_{FBSMPS} reaches 1.4 V (or above), and releases the CPU.

This mechanism can add a delay between the wake-up source and the real CPU startup.

The measurements show the extra delay to add to the normal Stop1 / Stop2 wake-up time, considering two extreme cases:

- Typical: the Stop1 / Stop2 duration is short enough (in this measurement the Stop2 duration is 10 µs at ambient temperature) to consider that the SMPS bulk capacitor voltage has not changed significantly.
- Max: the Stop1 / Stop2 duration is longer (in this measurement the Stop2 duration is 100 ms with a forcing discharge of the bulk capacitor through a resistor simulating the leakage down to 0 V).

Figure 3. Additional startup time (I_{LOAD} = 10 mA)



The measurements show the impact of the maximum output current selection (PWR_CR5.SMPSSC), the current limiting the reloading of the 4.7 µF bulk capacitor (80 and 200 mA).

2.3 STM32WB SMPS specificities

2.3.1 Rollback current when SMPS voltage decreases

When the SMPS operates and its output voltage decreases, instead of consuming the charge stored in the bulk capacitance, it rolls back the charge into V_{DDSMPS}. This charge is partially absorbed by the decoupling capacitances connected on V_{DDSMPS} and V_{DD}, and the impedance of the power supply.

This situation happens each time V_{FBSMPS} decreases, for example when:

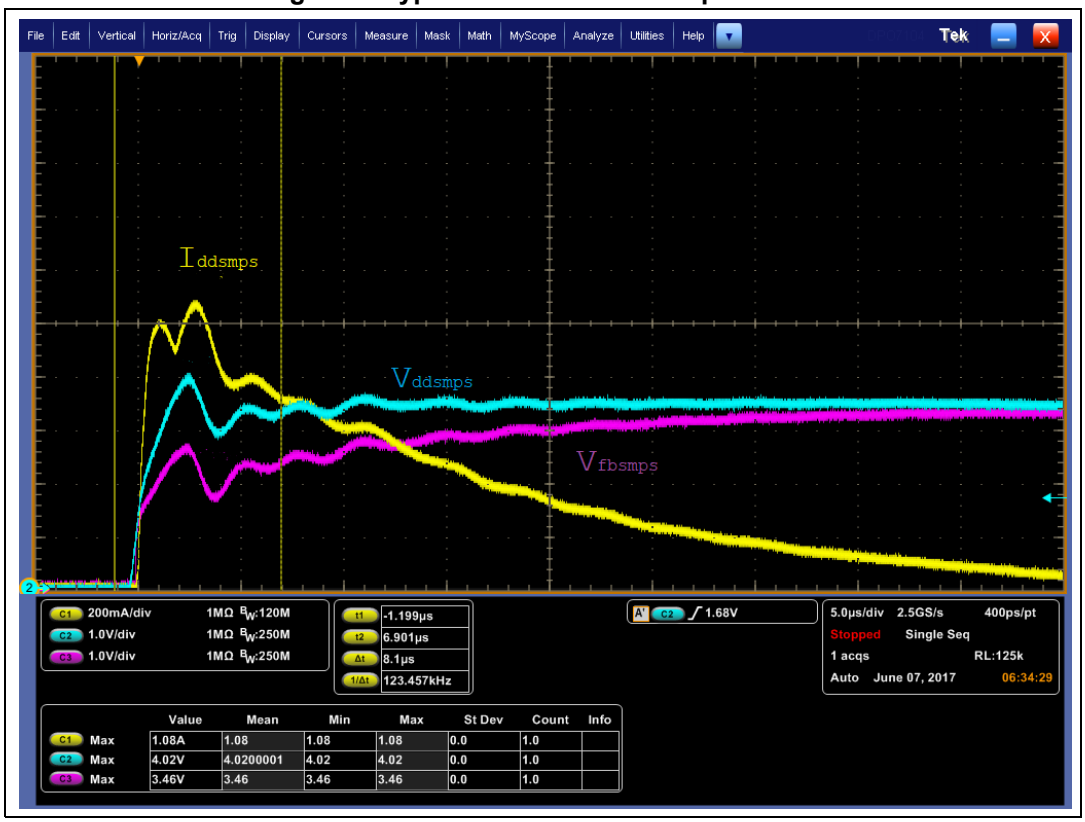
- moving from the BYPASS to SMPS mode (transition from V_{FBSMPS} = V_{DD} to 1.4 V)
- moving from Tx = +6 dBm (V_{FBSMPS} = 1.7 V) to Tx = 0 dBm (V_{FBSMPS} = 1.4 V)
- moving from OPEN to SMPS mode (bulk capacitance is sightly discharged)

On systems where the power supply (or the remaining part of the application) cannot sink this extra current, there is a V_{DD} increase, directly proportional to the ratio between the bulk and the decoupling capacitances. The simplest way to limit it is to increase the decoupling capacitance.

2.3.2 Inrush current at power-on

When the SMPS starts in BYPASS mode when powering up, the bulk capacitance must be powered when V_{DD} rises. At start-up, when the V_{DD} voltage enters the 0.7 to 1 V range, the SMPS PMOS starts to conduce, and $V_{FBDSMPS}$ follows V_{DDSMPS}. This leads to a temporary inrush current. which can be as high as 1.1 A if the power supply is strong enough.

Figure 4. Typical inrush current at power-on



2.3.3 Current peak when SMPS voltage increases

When the SMPS is operating and its output voltage increases, a short peak of current is present. This happens each time V_{FBSMPS} increases, for example when:

- moving from SMPS to Bypass mode (transition from V_{FBSMPS} 1.4 V or 1.7 V to V_{DD})
- moving from Open to SMPS mode (if V_{FBSMPS} decreases during Open mode)
- moving from SMPS to SMPS mode (1,4 V to 1.7 V)

This current peak depends upon the PWR_CR5.SMPSSC value and the ratio between V_{FBSMPS} and V_{FBSMPS} for SMPS mode. The simplest way to limit it is to increase the decoupling capacitance.

2.3.4 V_{LXSMPS} overrides absolute maximum ratings

In normal operation V_{LXSMPS} temporary exceeds V_{DD}, and can be lower than V_{SS}.

This happens at each SMPS cycle (8 or 4 MHz) when both the NMOS and PMOS switches are open, because the inductor current flows across the bulk diodes toward V_{DDSMPS} and V_{SSSMPS}.

This effect is considered by the ST qualification process, and does not affect product life time, quality. and reliability of the product.

3 Conclusion

The main functionalities and characteristics of the STM32WB series MCUs built-in switched mode power supply (SMPS) are described in this application note.

This circuit block optimizes the RF transceiver performance and the power consumption in applications based on Bluetooth® Low Energy and IEEE 802.15.4 protocols.

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
28-Nov-2018	1	Initial release.
18-Feb-2019	2	Changed document classification, from ST restricted to Public. Updated *Section 1.1.2: LDO configuration* and *Section 1.1.3: External components*.
20-Nov-2020	3	Updated *Section 1: Description*, *Section 1.1.2: LDO configuration*, *Section 1.3.1: Programming registers*, *Section 2.1: Selecting the output voltage* and *Section 2.1.1: Numerical examples*.
21-Apr-2023	4	Updated document title, *PWR_CR5.SMPSVOS[3..0] (Read/Write)*, *Section 2.1: Selecting the output voltage*, and *Section 2.3.1: Rollback current when SMPS voltage decreases*. Added *Section 2.3.3: Current peak when SMPS voltage increases*. Minor text edits across the whole document.