AN5256
Application note

STM32MP151, STM32MP153 and STM32MP157 discrete power supply hardware integration

Introduction

STM32MP151, STM32MP153, and STM32MP157 product lines (referred to as STM32MP15x in this document), are built on an Arm® Cortex®-A7 with single or dual-core combined with an Arm® Cortex®-M4. They are usually powered by the STPMIC1 power management IC companion chip, which is fully featured to supply complete applications.

This application note describes an alternative solution to supply power to STM32MP15x MPUs with discrete regulators. Only applications supporting the core chipset are covered (STM32MP15x + DDR + flash memory).

This application note is intended for hardware product designers and architects who require details about:

- Detailed schematic block diagrams
- Low power mode and reset management (crash recovery)
- Voltage regulator module (VRM) electrical specification for supplying the STM32MP15x power rail.

Contents

1 Overview 6

1.1 Reference documents 7

2 Glossary 8

3 Discrete power supply topologies 9

3.1 STM32MP15x with DDR3L and 3.3 V I/O voltage interface 9

3.1.1 Input voltage 11

3.1.2 Regulator topology recommendations for LDO or SMPS 11

3.2 STM32MP15x with DDR3L and 1.8 V I/O voltage interface 16

3.2.1 Input voltage 17

3.2.2 Regulator topology recommendations for LDO or SMPS 17

3.3 Low power modes and crash recovery management 19

3.3.1 Crash recovery management circuitry (optional) 20

4 Power sequence management 21

4.1 Power-up/power-down sequence and reset management 21

4.2 Low-power mode management 24

4.2.1 LP-Stop mode 24

4.2.2 Standby mode 26

4.3 Crash recovery management 28

5 STM32MP15xD and STM32MP15xF enhanced CPU frequency supply management 31

5.1 Crash recovery management and specific system operating modes 33

5.2 Power-up/power-down sequence and reset management 34

5.3 Low-power mode management 34

5.3.1 LP-Stop mode 34

5.3.2 Standby mode 36

6 Voltage regulator module (VRM) specification 37

6.1 VRM specification for VDD (VDD_ANA, VDD_PLL, VDD_DSI) power domain 37

6.2 VRM specification for VDDCORE power domain 38

6.2.1 VRM specification for VDDCORE power domain for STM32MP15xD and STM32MP15xF devices 38
6.3 VDDQ_DDR power domain VRM specification 39

7 Voltage regulator module examples 41
7.1 VRM example for 5 V DC to 3.3 V DC - 300 mA 41
7.2 VRM example for 5 V DC to 1.215 V DC - 1500 mA 41
7.3 VRM example for 5V DC to scalable 1.34 V / 1.2 V DC - 1500 mA 42
7.3.1 Vout (R1, R2, R3, R4) computation example 43
7.4 VRM example for 5V DC to 1.35 V DC - 1000 mA 43
7.5 VRM example for 5V DC to 3.3 V DC - 2000 mA 45

8 Revision history 46

List of tables

Table 1. Reference documents . . . 7
Table 2. Glossary . . . 8
Table 3. System operating modes . . . 19
Table 4. System operating modes . . . 33
Table 5. VRM specification for VDD power domain . . . 37
Table 6. VRM specification for VDDCORE power domain . . . 38
Table 7. VRM specification for VDDCORE power domain with voltage scaling for 800 MHz support . . . 39
Table 8. VRM specification for VDDQ_DDR and DDR3L IC power domain . . . 40
Table 9. VRM example for 5 V to 3.3 V - 300 mA . . . 41
Table 10. VRM example for 5 V to 1.215 V - 1500 mA . . . 41
Table 11. VRM example for 5 V to 1.34V / 1.2 V - 1500 mA . . . 42
Table 12. VRM 1.34V / 1.2 V truth table . . . 43
Table 13. VRM example for 5 V to 1.35 V - 1000 mA . . . 44
Table 14. VRM example for 5 V to 3.3V - 2000 mA . . . 45
Table 15. Document revision history . . . 46

List of figures

Figure 1. Discrete power supply topology example with IOs at 3.3 V and DDR3L . . . 10
Figure 2. Supply VDD3V3_USBHS/FS with integrated power switch . . . 14
Figure 3. VDD3V3_USBHS/FS supply with discrete power switch . . . 14
Figure 4. Discrete power supply topology example with IOs at 1.8 V and DDR3L . . . 16
Figure 5. Supply VDD3V3_USBHS/FS from VDD_PERIPH . . . 18
Figure 6. PWR_ONRST crash recovery management signal . . . 20
Figure 7. Power-up / power-down sequence and reset management diagram . . . 21
Figure 8. LP-Stop mode sequence . . . 24
Figure 9. Standby mode sequence . . . 26
Figure 10. Crash recovery sequence . . . 29
Figure 11. Discrete power supply topology example with IOs at 3.3 V, DDR3L and VDDCORE voltage scaling . . . 32
Figure 12. LP-Stop mode sequence . . . 35
Figure 13. Voltage regulator module perimeter example . . . 37
Figure 14. VRM 5 V to 3.3 V - 300 mA details . . . 41
Figure 15. VRM 5 V to 1.215 V / 1500 mA details . . . 41
Figure 16. VRM 5 V to scalable 1.34 V / 1.2 V - 1500 mA details . . . 42
Figure 17. VRM 5 V to 1.35 V - 1000 mA details . . . 43
Figure 18. VRM 5 V to 3.3 V - 2000 mA details . . . 45

1 Overview

This application note applies to all STM32MP15x devices, which have a large feature set and stringent power-supply requirements.

It focuses on the core chipset supplies (STM32MP15x + DDR + flash memory) with the following assumptions:

- 5 V DC input power source application
- DDR3L x32-bit bus width with bus termination resistors
- Generic flash memory powered from a 3.3 V power source.

The regulator electrical specifications provided in this document are only applicable when the STM32MP15x decoupling scheme (see AN5031 *[1]*) and layout recommendations are carefully followed.

Power consumption figures provided in this application note are illustrative examples only, and should not be used as a reference. For information regarding power consumption, refer to AN5284 *[7]* and the related product datasheet(s).

The STM32MP15x electrical and timing data provided in this application note is for illustration only, and should not be used as reference. Please refer to the relevant STM32MP15x product datasheet.

lpDDR2 and lpDDR3 memories are not within the scope of this application note. It is assumed that they are not powered by power discrete regulators for the following reasons:

- lpDDR2/3 memories have strict power-up and power-down sequence constraints (referring to JEDEC specification), which is complex to implement with discrete regulator circuitry
- Low-power management with discrete regulators is more complex than using a power management IC, such as the STPMIC1 (see DS12505 *[5]*).

STM32MP15x products are Arm®(a) Cortex®-based devices.

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a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Reference documents

Table 1. Reference documents(1)

Reference	Document ID	Title
[1]	AN5031	Getting started with STM32MP1 Series hardware development
[2]	AN5109	STM32MP1 Series using low-power modes
[3]	AN5089	STM32MP1 Series and STPMIC1 hardware and software integration
[4]	RM0436	STM32MP157 Reference manual (2)
[5]	DS12505	STM32MP157C Datasheet (3)
[6]	AN5122	STM32MP1 Series DDR memory routing guidelines
[7]	AN5284	STM32MP1 Series system power consumption
[8]	AN5438	STM32MP1 Series lifetime estimates

1. These documents are available on *www.st.com*.
2. This reference manual is used as a reference but this application note applies to all STM32MP15x devices.
3. This datasheet is used as a reference but this application note applies to all STM32MP15x devices.

2 Glossary

Table 2. Glossary

Term	Meaning
FSBL	First stage boot loader
HSI	High speed internal oscillator
LDO	Low drop out. a linear regulator in this document.
MPU	Micro-processor unit. Refers to STM32MP15x devices in this document
POR	Power-on reset
RC	Discrete resistor-capacitor network
RCC	STM32MP15x reset and clock control
RMS	Root mean square
SMPS	Switched-mode power supply
VRM	Voltage regulator module. in this document, a VRM is either a step-down SMPS or a LDO.

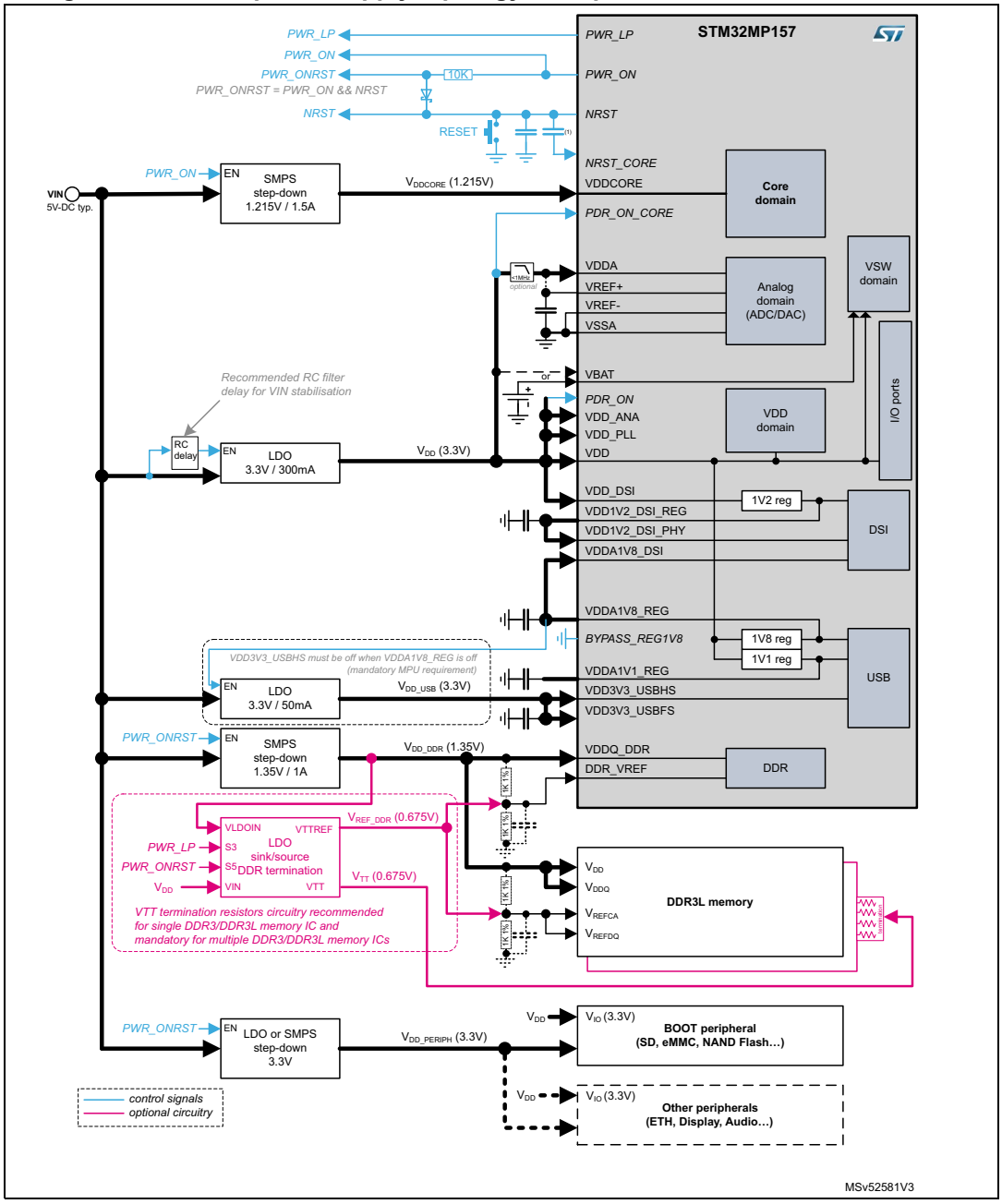
3 Discrete power supply topologies

3.1 STM32MP15x with DDR3L and 3.3 V I/O voltage interface

Figure 1 shows a basic application composed of an STM32MP15x, a DDR3L volatile memory, and a generic flash memory (boot peripheral). In this application, subsystem peripherals (Ethernet Phy, RGB LCD, audio, and so on) are not shown, but it is assumed that their I/O interface works at 3.3V (VDD). This application is powered by linear and switched-mode power supply step-down converters.

The following example is given for the STM32MP157 device. It is applicable for all STM32MP15x devices.

Figure 1. Discrete power supply topology example with IOs at 3.3 V and DDR3L



1. It is recommended to add a capacitor between NRST and NRST_CORE when V_{DD} = 3.3V. It is also possible to connect NRST_CORE directly to NRST.

Note: The MPU decoupling scheme is not shown (see AN5031 [1]).

SMPS and LDO regulator product part numbers and discrete components are not shown, but their electrical specifications are detailed in Section 3.1.2: Regulator topology recommendations for LDO or SMPS.

Additional protection on VIN, such as ESD, EMI filtering, and over-voltage, is not shown.

3.1.1 Input voltage

This application example is powered from a 5 V (typical) DC voltage source (VIN) with a range of 4.0 to 5.5 V. It uses only the following DC to DC step-down converters:

- linear regulators (LDOs)
- nonisolated buck SMPS

Alternatively, this application can be powered from a higher input voltage, such as 12 V. In this case, suitably rated discrete regulators of the correct input voltage are used. For input voltages higher than 12 V - typically industrial applications - use of preregulation topology is recommended. For example, use of a 24 V-to-5 V DC-DC buck SMPS for preregulation to generate VIN, followed by the topology defined in this example. Preregulation is recommended to avoid working the buck SMPS with very low duty cycle (with associated concerns).

The minimum VIN voltage should be higher than the highest voltage used in the application. In this application, 3.3 V is the highest voltage required by the application (to supply V_{DD} and V_{DD_PERIPH}). Considering an ideal regulator (no dropout) and an ideal power source, the minimum VIN could be 3.3 V. In real conditions, a reasonable 400 mV dropout for a 3.3 V regulator (working at full load) and a 300 mV drop on the VIN path (including DC and AC drop + margin), requires a minimum VIN voltage of about 4 V.

The maximum VIN voltage is limited by the regulator powered from VIN having the lowest maximum-rated input voltage. In this application, it is assumed to be 5.5 V.

3.1.2 Regulator topology recommendations for LDO or SMPS

The LDO or SMPS regulator topology selection is a trade-off between simplicity of integration versus power-efficiency performance:

- LDO: simplicity of integration, low noise, but poor power efficiency (thermal heating)
- SMPS: good power efficiency (lower thermal heating than LDO); complex to integrate, higher noise than LDO (switching activity).

For applications powered from DC source - typically powered from AC to DC wall adapter - power efficiency is less critical than in battery applications. Nevertheless, thermal heating remains an important criteria and should be minimized as much as possible. This is especially so when the application runs the most power-consuming use case, or when it is powered from a VIN power source at 12 V instead of 5 V.

Reciprocally, applications in Standby mode should have a low quiescent current for regulators kept ‘on’ and a low leakage current for regulators turned ‘off’.

Regulator topologies should be selected accordingly.

VDD power domain

For the VDD power domain, the LDO topology is a good compromise between power losses, voltage noise, and cost:

- The VDD / VIN voltage ratio is 0.66 (3.3 V / 5 V). The LDO power efficiency is approximately 66%, quasi constant.
- Average current consumption is low, even for complex use cases. It is typically below an average worst-case current of 100 mA (50 mA assumed) and never exceeds 200 mA (assuming 300 mA peak very worst case to allow some margin).
- Current consumption in Stop and Standby modes is very low; ~1 mA and ~10 µA respectively (see DS12505 *[5]* for details and conditions)

With the LDO topology, the power efficiency is ~66% (~VDD / VIN ratio), and ~90% with an SMPS buck converter. Power losses are 85 mW with an LDO and 18 mW with the SMPS converter respectively (assuming a 50 mA power consumption). For both, it is negligible in terms of thermal heating compared to other application power domains.

In Stop mode, power losses are equivalent between an LDO and a buck SMPS, because common buck converter power efficiency decreases under light load.

In Standby mode, power losses are higher with an SMPS compared to an LDO. An SMPS usually has a higher quiescent current than an LDO, and an LDO has no switching losses.

VDDA and VREF power domains

The VDDA pin supplies the ADC / DAC and the voltage reference buffer (VREFBUF) to generate the V_{REF+} reference voltage of the ADC / DAC.

The ADC and DAC performance is directly impacted by the noise level from the V_{REF+} source, but also by the VDDA source noise level (due to the VDDA power supply rejection ratio).

If VDDA is powered from VDD power source, a low pass filter with low DC impedance may be inserted in between VDD power source and VDDA depending on the required ADC / DAC performance.

V_{REF+} should only be connected to the VDD power source if limited ADC / DAC performance is expected.

VDDCORE power domain

For the VDDCORE power domain, buck SMPS topology is recommended for power efficiency as this is one of the highest power-consumption domains in the application.

For VDDCORE, LDO topology is not recommended due to the ratio between VDDCORE and VIN of about 0.24 (1.215 V / 5 V). With an LDO, power efficiency could be as low as 24%, meaning significantly more energy being consumed by the LDO converter than the energy consumed by the MPU itself.

VDD_DDR and VTT power domains

For V_{DD_DDR} power domain, buck SMPS topology is recommended for the same reason as for VDDCORE.

If the application requires termination resistors on the DDR3 / DDR3L address/command bus, a dedicated sink/source LDO should be used to supply VTT at V_{DD_DDR} / 2. Such a regulator usually integrates a VREF_DDR converter allowing the resistor divider (1 kΩ / 1 kΩ) to be removed from the design.

VDD_USB power domains

VDD3V3_USBHS and VDD3V3_USBFS are the USB PHY power supply pins of the MPU. They should be powered from 3.07 V to 3.6 V. Both VDD3V3_USBHS and VDD3V3_USBFS power consumptions are less than 30 mA (50 mA is assumed in order to allow some margin).

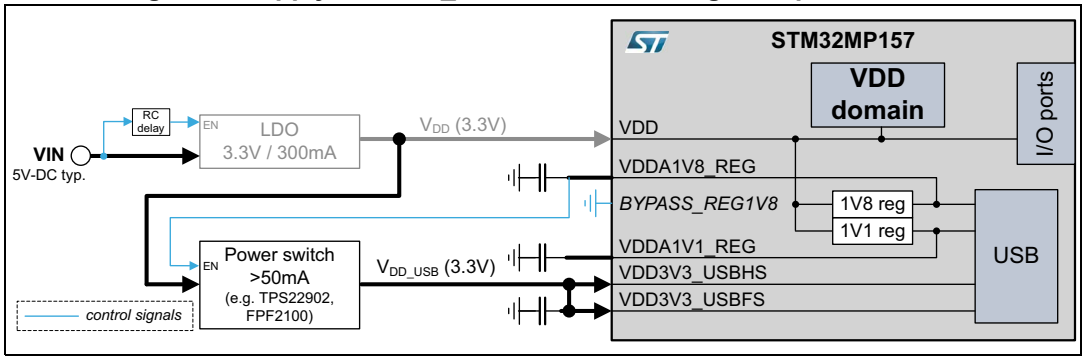
VDD3V3_USBHS must not be present when VDDA1V8_REG is absent, otherwise permanent MPU damage could occur (see DS12505 *[5]* for details). VDD3V3_USBHS cannot be connected directly to VDD as VDD is always present before VDDA1V8_REG.

To accommodate this constraint, VDD3V3_USBHS should be enabled by VDDA1V8_REG. VDD_USB is enabled when VDD1V8_REG is enabled, hence by default at power-on, and whenever DSI or USB are used. Different power supply options are possible:

- dedicated LDO (recommended), see *Figure 1*
- integrated power switch / load switch, see *Figure 2*
- discrete power switch, see *Figure 3*.

The following example is given for the STM32MP157 device. It is applicable for all STM32MP15x devices.

Figure 2. Supply VDD3V3_USBHS/FS with integrated power switch

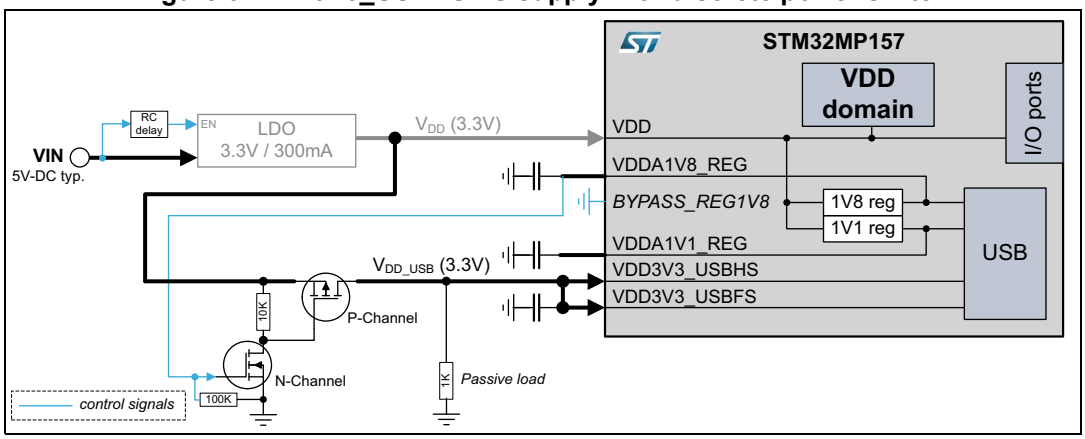


The power switch (load switch) main electrical criteria are:

- The ON-resistance should be low enough to guarantee that VDD_USB never drops below 3.07 V. Typically below 700 mΩ if VDD has +/-5% tolerance:
  R_{on} < ((3.3 V - 5%) – 3.07 V) / 50 mA = 0.7 Ω.
- The EN_V_{IH} min threshold (active high) should be below 1.7 V (VDDA1V8_REG min) to ensure that the power switch turns on in all conditions.
- An integrated output discharge resistor is recommended to discharge the VDD_USB decoupling capacitor when the power switch is disabled.

The following example is given for the STM32MP157 device. It is applicable for all STM32MP15x devices.

Figure 3. VDD3V3_USBHS/FS supply with discrete power switch



This discrete power switch is composed of one P-channel power MOSFET and one N-channel MOSFET. The P-channel MOSFET acts as a power switch to drain current from VDD to VDD_USB to supply VDD3V3_USBHS/FS. The P-channel gate is driven by the N-channel MOSFET, which acts as an open drain to reverse the P-channel polarity. The N-channel gate is driven by the VDDA1V8_REG voltage. The 1 kΩ passive load is added to discharge the decoupling capacitors on VDD3V3_USBHS/FS, continuously consuming 3.3 mA when VDD_USB is enabled.

Discrete power switch main electrical characteristics:

- P-channel MOSFET:
  - V_{DSS} and VGSS > -3.3 V
  - I_D min: -50 mA
  - I_D peak >> -50 mA (peak current when charging VDD3V3_USBHS/FS decoupling capacitor)
  - $R_{DS(ON)}$ < 0.7 Ω at V_{GS} = -3.3 V
- N-channel MOSFET:
  - V_{DSS} > 3.3 V
  - V_{GSS} > 1.8 V
  - I_D min: 10 mA
  - $R_{DS(ON)}$ < 100 Ω at V_{GS} = 1.8 V

VDD_PERIPH power domain

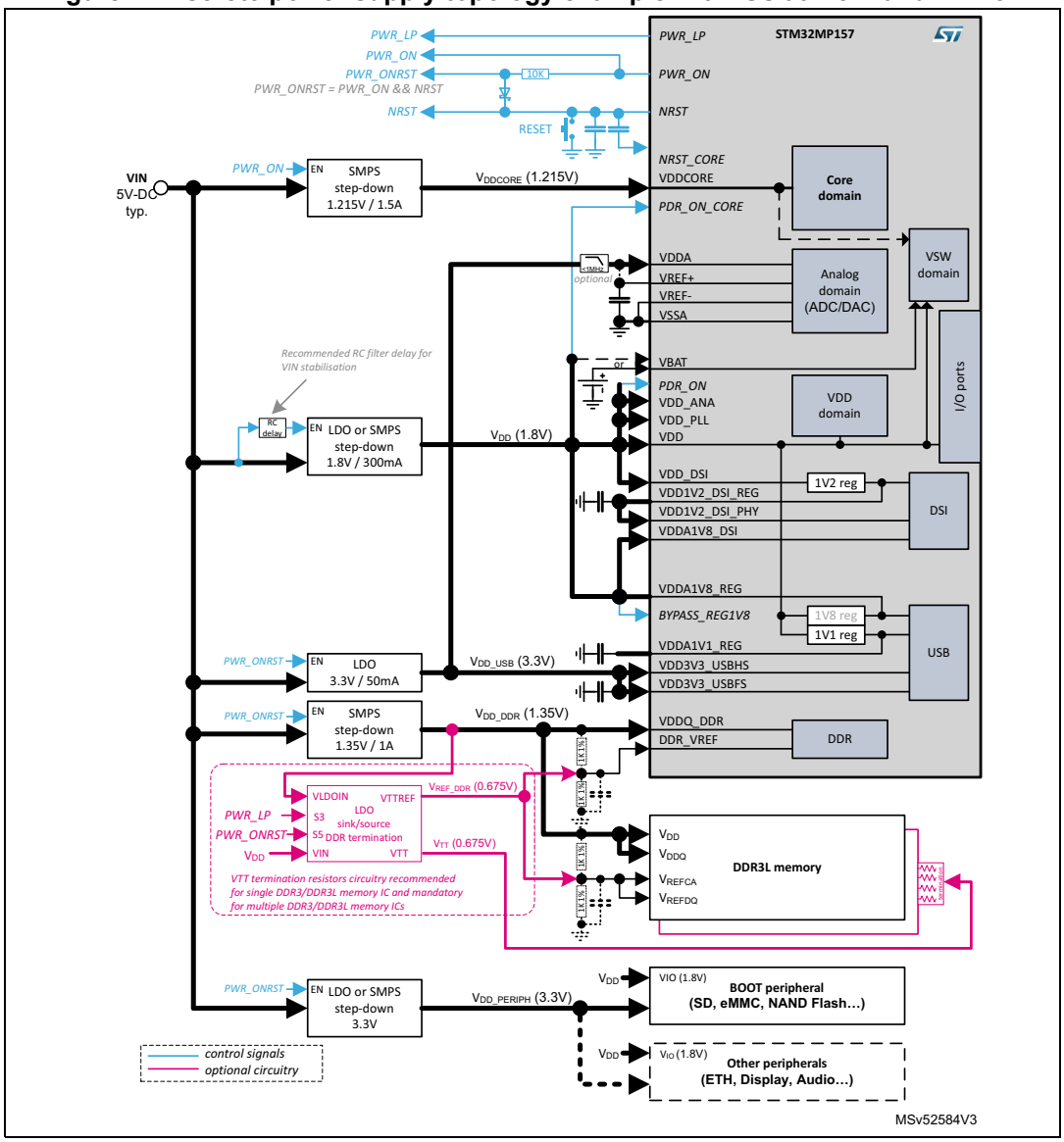
For VDD_PERIPH power domain, voltage and regulator topology depend on final application. In the application illustrated in *Figure 1*, it is assumed that all peripherals can be supplied from a 3.3 V voltage source.

3.2 STM32MP15x with DDR3L and 1.8 V I/O voltage interface

Figure 4 shows the same application as *Figure 1*, except that the I/O interface is changed from 3.3 V to 1.8 V. Subsystem peripherals (Ethernet, LCD, Audio, and so on) are not shown but it is assumed their I/O interface works at 1.8 V (V_{DD}), or they use level translators. It is powered by linear and switched-mode power supply step-down converters.

The following example is given for the STM32MP157 device. It is applicable for all STM32MP15x devices.

Figure 4. Discrete power supply topology example with IOs at 1.8 V and DDR3L



Note: The MPU decoupling scheme is not shown (see AN5031 [1]).

SMPS and LDO regulator part numbers and discrete components are not shown, but their electrical specifications are detailed in Section 3.2.2: Regulator topology recommendations for LDO or SMPS.

Additional protection on VIN, such as ESD, EMI filtering, and overvoltage, are not shown.

3.2.1 Input voltage

See *Section 3.1.1: Input voltage*.

3.2.2 Regulator topology recommendations for LDO or SMPS

This section is similar to *Section 3.1.2: Regulator topology recommendations for LDO or SMPS* with the following differences:

VDD power domain

For the VDD power domain, buck SMPS topology is recommended for power-efficiency reasons. Nevertheless, LDO topology may be acceptable due to the low power consumption on this supply domain.

- The VDD / VIN voltage ratio is 0.36 (1.8 V/5 V). LDO power efficiency is approximately 36%, quasi constant.
- The average current consumption average is low, even for complex use cases. The worst-case average is typically below 100 mA on (50 mA assumed), and never exceeds 200 mA (300 mA peak very worst case to allow some margin).
- The current consumption in Stop and Standby modes is very low; ~1 mA and ~10 µA respectively (see DS12505 for details and conditions.)

With the LDO topology, power efficiency is approximately 36% (~VDD / VIN ratio) and it is about 90% with an SMPS buck converter. Power losses are 160 mW with LDO and 18 mW with an SMPS converter respectively (assuming 50 mA power consumption). Depending on the application heat-dissipation capacity, if 60 mW in losses is acceptable, then an LDO can be used.

VDD_USB power domains

VDD3V3_USBHS and VDD3V3_USBFS are the USB PHY power supply pins of the MPU. They should be powered from 3.07 V to 3.6 V. Neither the VDD3V3_USBHS nor the VDD3V3_USBFS power consumption is more than 30 mA (50 mA is assumed to allow some margin).

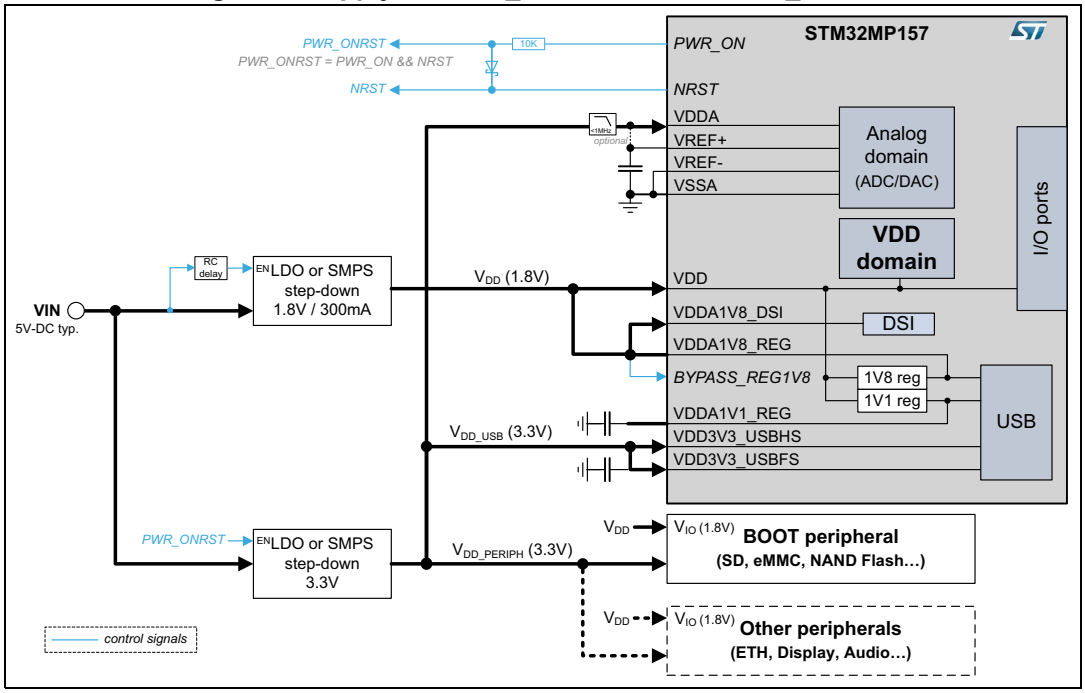
VDD3V3_USBHS must not be present when VDDA1V8_REG is absent, otherwise permanent MPU damage could occur (see DS12505 *[5]*).

To accommodate these constraints, VDD3V3_USBHS should be synchronized with the PWR_ON or PWR_ONRST signal, as VDD is connected to VDDA1V8_REG and VDD rises first in the application (see *Figure 4*). Two power supply options are possible:

- Dedicated LDO (recommended), see *Figure 4*
- Reuse of the regulator supplying the peripheral (V_{DD_PERIPH}), see *Figure 5*.

The following example is given for the STM32MP157 device. It is applicable for all STM32MP15x devices.

Figure 5. Supply VDD3V3_USBHS/FS from VDD_PERIPH



V_{DD_PERIPH} power source can be used to supply VDD3V3_USBHS and VDD3V3_USBLS if the following conditions are respected:

- the V_{DD_PERIPH} voltage should be in VDD3V3_USBHS/LS voltage tolerance (3.07 V to 3.6 V]
- the V_{DD_PERIPH} (VDD3V3_USBHS) must not be present unless VDD (VDDA1V8_REG) is present.

If the V_{DD_PERIPH} regulator has the same voltage and is controlled through PWR_ONRST, as in *Figure 5*, the two upon constraints are fulfilled.

VDDA and VREF power domains

The VDDA pin supplies the ADC / DAC and also the voltage reference buffer (VREFBUF) to generate the ADC/DAC V_{REF+} reference voltage.

ADC/DAC performance is directly impacted by the level of noise from the V_{REF+} source, and also by the noise level from the VDDA source (due to the VDDA power supply rejection ratio).

If the ADC/DAC are used in the application with a reference voltage, V_{REF+}, higher than 2 V, then the V_{DD_PERIPH} power source can be used to supply VDDA. A low-pass filter with low DC impedance can be inserted in between the VDD power source and VDDA depending on the required ADC/DAC performance.

VREF+ may be connected to the V_{DD_PERIPH} power source only if limited ADC / DAC performance is acceptable.

3.3 Low power modes and crash recovery management

STM32MP15x devices support several operating modes to reduce power consumption (see AN5109: "STM32MP1 Series using low-power modes" for details).).

The two MPU output pins, PWR_ON and PWR_LP, are automatically controlled depending on the operating mode. They are used to control the application regulators:

- PWR_ON: supply request signal (active high). Enables VDDCORE and the application peripheral power supplies. It is active in Run, Stop and Low-Power-Stop modes. It is inactive in Standby mode (and implicitly in VBAT and power Off modes when VDD is not present).
- PWR_LP: low-power mode request signal (active low). It is used to request a regulator or a peripheral to enter low-power state. It is active in LP_Stop and Standby modes. It is inactive in Run and Stop modes.

Note: With discrete-regulator applications, LPCFG (PWR_ON pin configuration in PWR_CR1 register) should always be set to 0.

Table 3 summarizes the power supply states for the application operating modes illustrated in *Figure 1*.

Table 3. System operating modes

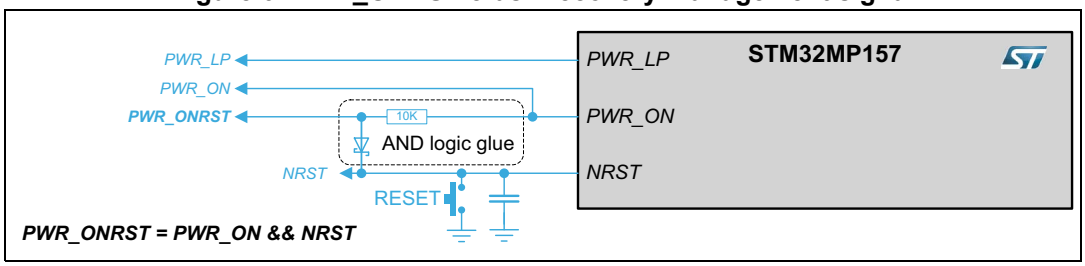
Power mode	NRST / NRST_CORE	VDD	PWR_ON / VDDCORE	PWR_ONRST / VDD_DDR VDD_PERIPH	PWR_LP / VTT
Run	1	On	1 / On	1 / On	1 / On
Stop	1	On	1 / On	1 / On	1 / On
LP-Stop	1	On	1 / On	1 / On	0 / Off
Standby	1	On	0 / Off	0 / Off	0 / Off
VBAT or Power off	-	Off (No VIN)	Off (No VIN)	Off (No VIN)	Off (No VIN)
Crash (watchdog elapsed)	0 (pulse)	On	1 / On	0 / Off	1 / VTT Off

3.3.1 Crash recovery management circuitry (optional)

PWR_ONRST is an additional signal dedicated to the management of crash recovery at the application level. As shown in *Figure 6*, the PWR_ONRST signal is generated from PWR_ON and NRST by a discrete logical AND circuit.

The following example is given for the STM32MP157 device. It is applicable for all STM32MP15x devices.

Figure 6. PWR_ONRST crash recovery management signal



The AND logic circuit is composed of a 10 kΩ resistor and a diode. Use of a Schottky diode such as BAT54 or BAT60 is recommended. The 10 kΩ value may be adapted according to the combined impedances of the regulator EN pin; especially if some or all of the regulator EN pins have built-in pull-down resistors.

The PWR_ONRST signal is equivalent to the PWR_ON signal. However, if a reset occurs (NRST signal low pulse), the PWR_ONRST signal goes low meaning that regulators controlled by this signal turn OFF for the NRST low pulse duration, then turn back ON after the reset is released to a high state.

This allows power-supply cycling to be performed on peripherals. It is recommended that correct restart and reset of peripherals be assured after an application reset occurs (NRST), especially for peripherals that do not have a reset input signal. Power cycling is especially recommended for peripheral boot devices / flash memory such as eMMC, NAND, NOR, and SD-Card.

STM32MP15x devices have a bidirectional pad reset (NRST) allowing the reset of external devices. If a crash occurs (iwdg1_out_rst or iwdg2_out_rst watchdog elapsed), a reset pulse is generated on the NRST signal. An identical pulse is generated on the PWR_ONRST signal to control power cycling of the peripheral power supplies. An example timing diagram is provided in *Section 4: Power sequence management*.

Note: The MPU's RPCTL (reset pulse control) allows control of the minimum pulse duration of the NRST pin. It should be enabled by software at boot-up, and set to an appropriate duration; for example 31 ms, by setting bitfield MRD[4:0] = 0x1F in the RCC_RDLSICR register.

This ensures that discrete regulator output voltages have enough time to drop before the pulse ends (transits to '1') and re-enables the regulators.

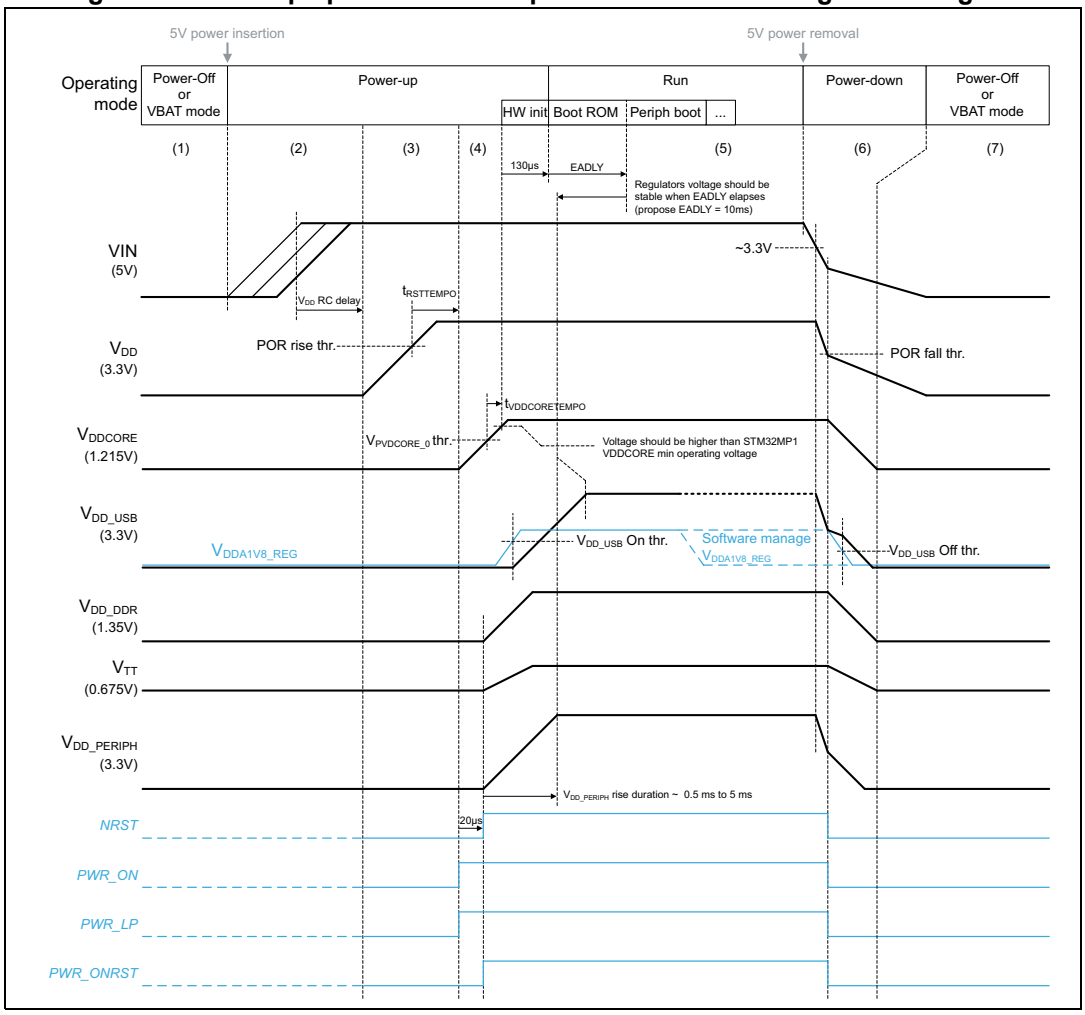
4 Power sequence management

In *Figure 7* through *Figure 10*, the V_{DDA1V8_REG} level and the signal waveforms associated with its management are shown in light blue for clarity.

4.1 Power-up/power-down sequence and reset management

The application power-up and power-down sequence is shown in *Figure 7* according to the implementation shown in *Figure 1: Discrete power supply topology example with IOs at 3.3 V and DDR3L*.

Figure 7. Power-up / power-down sequence and reset management diagram



1. The application is not powered, or the MPU is in VBAT mode (powered from VBAT to supply the VSW power domain).
2. A valid power supply source is connected to the application. The VIN voltage rises. After a delay (defined by a passive R-C network), to allow the VIN voltage to stabilize, the VDD regulator is enabled.
3. The V_{DD} voltage starts to rise:
   a) The NRST, PWR_ON, PWR_LP signals are set low by the MPU, forcing the PWR_ONRST signal low.
   b) Once the V_{DD} supply voltage is above the POR rising threshold level[a], a $t_{RSTTEMPO}$[b] delay is started.
4. Once $t_{RSTTEMPO}$ elapses, the PWR_ON and PWR_LP signals are set high by the MPU:
   a) After $t_{RSTTEMPO}$ elapses, the MPU waits for 20 µs[c] before releasing the NRST signal, making PWR_ONRST transit to a high level. V_{DD_PERIPH}, V_{DD_DDR}, and V_{TT} are enabled by the PWR_ONRST signal, and the V_{DD_PERIPH}, V_{DD_DDR}, and VTT voltages start to rise.
   b) The V_{DDCORE} regulator is enabled by the PWR_ON signal, and the V_{DDCORE} voltage starts to rise.
   c) Once the V_{DDCORE} voltage is above the $V_{PVDCORE\_0}$[d] rising threshold level, a $t_{VDDCORETEMPO}$[e] delay is started. As long as the $t_{VDDCORETEMPO}$ has not elapsed, the MPU is kept in internal reset.
5. Once the $t_{VDDCORETEMPO}$ delay elapses, the MPU is taken out of internal reset (V_{DDCORE_OK}):
   a) The V_{DDCORE} voltage should be higher than the VDDCORE[f] minimum operating voltage. This should be guaranteed by the V_{DDCORE} regulator slew rate.
   b) The V_{DDA1V8_REG} internal regulator is enabled. When the V_{DDA1V8_REG} voltage reaches V_{DD_USB} regulator enable threshold, the V_{DD_USB} regulator is enabled.
   c) The MPU performs an internal hardware initialization (enabling the HSI and option byte loading with a ~130 µs duration). It then enters in Run mode. The EADLY[g] delay timer (10 ms) is started.

a. POR rise threshold = V_{BOR0} rising edge = 1.67 V typ.

b. $t_{RSTTEMPO}$ = 377 µs typ.

c. Internal RCC delay of the MPU.

d. $V_{PVDCORE\_0}$ rising edge = 0.95 V min.

e. $t_{VDDCORETEMPO}$ = 200 µs min.

f. VDDCORE operating voltage = 1.18 V min.

g. The EADLY timer prevents the Boot ROM from performing any access to the boot peripheral before it is ready when recovering from Standby mode. Typically it waits for a stable voltage on the flash memory that is read by the Boot ROM to get the boot software. In this application, the default value (10 ms) is kept to wait for the V_{DD_PERIP} and V_{DD_USB} voltage to stabilize (RM0436 *[4]* for more details).

d) When EADLY has elapsed, the Boot ROM starts accessing the external peripherals to load and execute the boot software. Implicitly, when EADLY has elapsed, all regulator voltages should be stable; especially V_{DD_PERIPH} and VDD_USB, which are power domains supplying the flash memory and USB interfaces respectively.

e) After an application initialization, the software can disable V_{DDA1V8_REG} (VDD_USB) if no USB peripheral is attached.

6. Power supply source is removed from the application:

a) The VIN voltage drops.

b) When the VIN voltage is close to V_{DD}, V_{DD_USB} and V_{DD_PERIPH} (3.3 V), they start to drop in parallel with VIN.

c) Once the V_{DD} supply voltage is below the POR fall threshold[(a)], the MPU resets internally and disables V_{DDA1V8_REG}. The NRST, PWR_ON and PWR_LP signals are set low by the MPU. The PWR_ONRST signal is forced low by the NRST and PWR_ON signals. The V_{DDCORE}, V_{DD_DDR}, V_{TT}, V_{DD_PERIPH} regulators are disabled. The current consumption on VIN drops, making VIN fall slowly. When the V_{DDA1V8_REG} voltage reaches the regulator disable threshold for V_{DD_USB}, the V_{DD_USB} regulator is disabled.

7. The application has no power, or the MPU is in VBAT mode (powered from VBAT to supply the V_{SW} power domain.

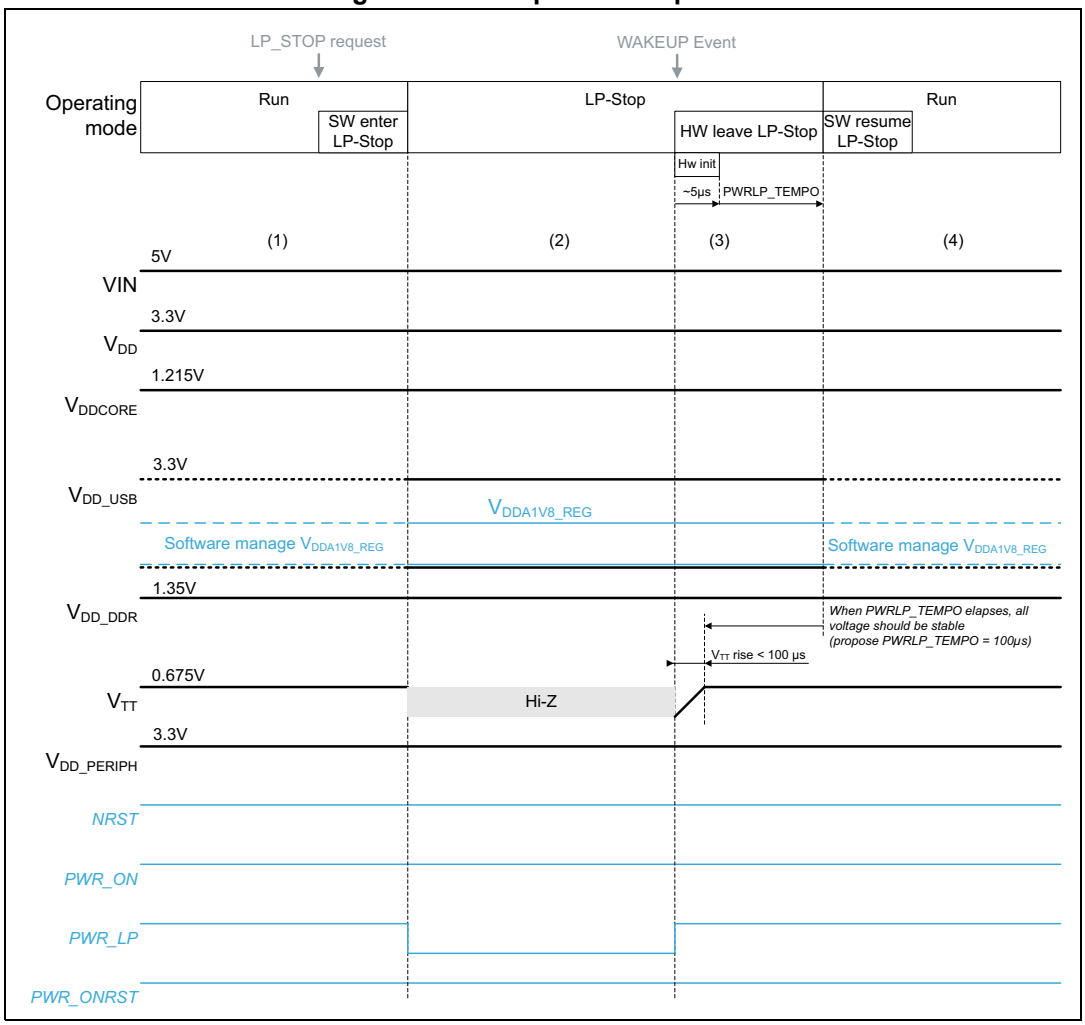
a. POR fall threshold = V_{BOR0} falling edge = 1.63 V typ (or = V_{BOR3} falling edge = 2.6 V max if option byte SELINBORH[0:1] = 11 (BOR = 2.7 V)).

4.2 Low-power mode management

4.2.1 LP-Stop mode

The application LP-Stop mode sequence is shown in *Figure 8: LP-Stop mode sequence* according to the implementation shown in *Figure 1: Discrete power supply topology example with IOs at 3.3 V and DDR3L*. In this application, V_{TT} is the only voltage regulator that supports low-power mode.

Figure 8. LP-Stop mode sequence



1. The application is powered and running. When LP_Stop mode is requested, the software prepares an LP_Stop entry (stops some clocks, sets DDR to self-refresh and sets PWRLP_TEMPO). It then sets the LPDS register to enter LP-Stop mode: the PWR_LP signal is asserted.
2. V_{TT} enters low power mode (high impedance).
3. On a wakeup event, the MPU leaves LP-Stop mode and de-asserts the PWR_LP signal:
   a) V_{TT} exits low power mode.
   b) A clock restore process is performed.
   c) Once the HSI clock oscillator is stable (after ~5 µs), the PWRLP_TEMPO[(a)] timer is timed out to wait for the V_{TT} regulator voltage to stabilize. In this application, the V_{TT} regulator recovery time is less than 100 µs. Hence, the PWRLP_TEMPO duration should be 100 µs minimum.
4. When PWRLP_TEMPO elapses, the application enters Run mode. The software resumes from LP-Stop mode (restores clocks, resumes DDR from self-refresh). Depending on the USB activity, the software may turn VDDA1V8_REG (internal regulator of the MPU) on or off, which automatically turns the V_{DD_USB} regulator on or off.

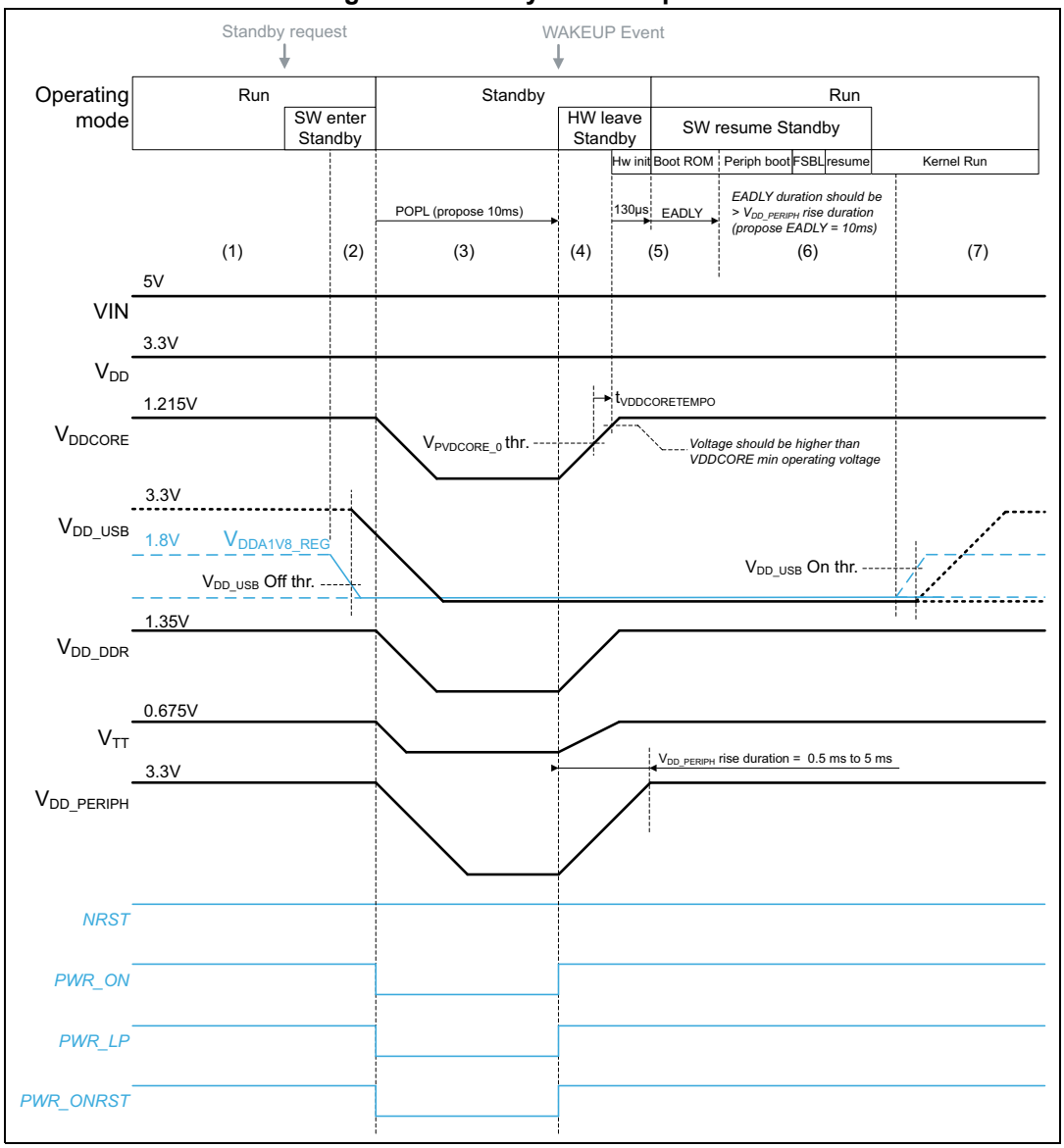
a. PWRLP_TEMPO is a dedicated timer designed to wait for regulators to recover when the application goes from LP-Stop mode to Run mode. The PWRLP_TEMPO delay value must be set in bitfield PWRLP_DLY[21:16] of the RCC_PWRLPDLYCR register.

4.2.2 Standby mode

The application Standby mode sequence is shown in *Figure 9* according to the implementation shown in *Figure 1: Discrete power supply topology example with IOs at 3.3 V and DDR3L*.

In this application, the flash memory used by the boot ROM to read the boot software (for example FSBL) is powered from the V_{DD_PERIPH} domain, and the DDR memory is powered OFF in Standby mode.

Figure 9. Standby mode sequence



1. The application is powered and running. When Standby mode is requested, the software prepares for Standby entry (stops some clocks, sets the POPL[a] and EADLY[b] timers, and so on).
2. The software may switch off the USB power domains by turning off V_{DDA1V8_REG}, making the V_{DD_USB} regulator switch off[c]. When the software is ready, the MPU enters Standby mode and the POPL timer starts automatically.
3. The PWR_ON signal is de-asserted and the PWR_LP signal asserted:
   a) The PWR_ONRST signal is forced low when PWR_ON is asserted.
   b) The V_{DDCORE} regulator is powered off by the PWR_ON signal.
   c) V_{DD_DDR}, V_{REF_DDR}, $V_{TT,}$ and V_{DD_PERIPH} are powered off by the PWR_ONRST signal.
4. On a wakeup event, the MPU leaves Standby mode[d], asserts the PWR_ON signal, and de-asserts the PWR_LP signal:
   a) The PWR_ONRST signal rises as both PWR_ON and NRST are high. V_{DD_DDR}, V_{REF_DDR}, VTT, and V_{DD_PERIPH} are enabled by the PWR_ONRST signal, and the V_{DD_DDR}, $V_{REF\_DDR,}$ V_{TT} and V_{DD_PERIPH} voltages start to rise.
   b) The VDDCORE regulator is enabled by the PWR_ON signal, and the V_{DDCORE} voltage starts to rise.
   c) Once the V_{DDCORE} voltage is above the $V_{PVDCORE\_0}$ rising minimum threshold, a $t_{VDDCORETEMPO}$ delay is started. As long as the $t_{VDDCORETEMPO}$ delay has not elapsed, the MPU is kept in internal reset.
5. Once the $t_{VDDCORETEMPO}$ elapses, the MPU is taken out of internal reset (V_{DDCORE_OK}):
   a) The V_{DDCORE} voltage should be higher than the V_{DDCORE} minimum operating voltage. This should be guaranteed by the V_{DDCORE} regulator slew rate.
   b) The MPU performs internal hardware initialization (enables the HSI and option-byte loading with 130 µs duration), then enters Run mode.
   c) The EADLY delay timer is started.

a. The POPL timer allows minimum Standby duration (minimum PWR_ON pulse low time) to be set. The POPL timer should be set in order to guarantee a minimum turn-off duration for the peripheral regulators. This is to ensure that peripherals restart properly from a low voltage. The POPL timer should be set according to the regulator having the slowest falling voltage (10 ms is suggested for this application).

b. The EADLY timer prevents the boot ROM from performing any access to the boot peripheral before it is ready when recovering from Standby mode. Typically this is to wait for stable supply voltage to the Flash-memory that is read by Boot ROM to get the boot software. In this application, the default value (10 ms) is suggested to wait for the V_{DD_PERIP} and V_{DD_USB} voltages to stabilize (see RM0436 *[1]* for more details).

c. Alternatively, if V_{DDA1V8_REG} is not turned off by software before entering Standby mode, it is automatically disabled by hardware at that time, turning V_{DD_USB} off. In this case, V_{DDA1V8_REG} is automatically turned on by hardware when leaving Standby mode, turning V_{DD_USB} on.

d. The STM32MP15x waits for POPL timer to elapse before leaving Standby mode; even if a wakeup event occurs before.

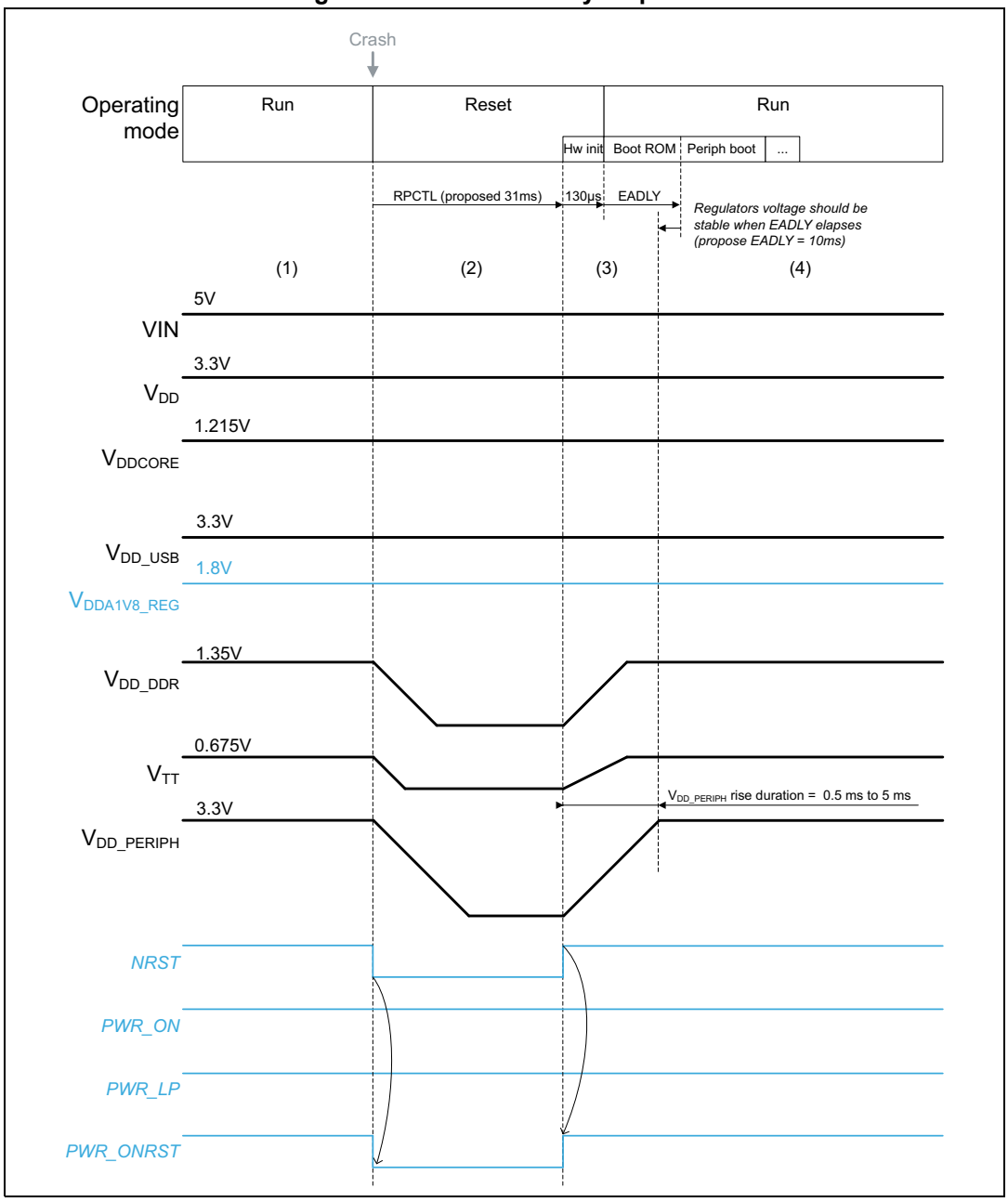
6. When EADLY elapses, the boot ROM starts accessing external peripherals (flash memory) to load and execute the boot software. Implicitly, when EADLY elapses, all regulators voltage should be stable; especially V_{DD_PERIPH}, which is the power domain supplying flash memory:
   a) The boot ROM is read (Periph boot), and the FSBL is verified and executed.
   b) The software detects an ‘exit from Standby mode’ and resumes the Kernel software accordingly.
7. Once the software resumes, it may switch the USB power domains on by turning V_{DDA1V8_REG} on, making the V_{DD_USB} regulator switch on, depending on the presence of USB devices.

4.3 Crash recovery management

As shown in *Section 3.3.1: Crash recovery management circuitry (optional)*, an optional external discrete circuitry can be added to the design (see *Figure 6: PWR_ONRST crash recovery management signal*), to perform peripheral power cycling. This allows peripherals to restart properly after a crash. This is especially suitable for flash memory, which does not have a reset input to restart it properly after a crash.

The sequence show in *Figure 10* illustrates a crash recovery sequence according to the implementation shown in *Figure 1: Discrete power supply topology example with IOs at 3.3 V and DDR3L*.

Figure 10. Crash recovery sequence



1. The application is powered and running. The RPCTL timer (see *Section 3.3.1*) is set to 31 ms and EADLY to 10 ms during the application initialization. A crash occurs (iwdg1_out_rst or iwdg2_out_rst watchdog elapsed) or an NRST pulse is performed from the user reset button.
2. The MPU asserts the NRST signal and the RPCTL timer starts:
   a) A low pulse is generated on NRST_CORE and the PWR_ONRST signal is forced low by the NRST signal.
   b) V_{DD_DDR}, V_{REF_DDR}, $V_{TT,}$ and V_{DD_PERIPH} regulator are powered off by the PWR_ONRST signal.
   c) The V_{DD_DDR}, V_{REF_DDR}, V_{TT} and V_{DD_PERIPH} voltages fall.
3. The RPCTL timer elapses (after 31 ms):
   a) The MPU releases the NRST signal.
   b) The NRST_CORE signal is already high and the PWR_ONRST signal rises because both PWR_ON and NRST signals are high.
   c) The V_{DD_DDR}, V_{REF_DDR}, V_{TT}, and V_{DD_PERIPH} regulators are powered on by the PWR_ONRST signal, and the V_{DD_DDR}, V_{REF_DDR}, $V_{TT,}$ and V_{DD_PERIPH} voltages start to rise.
   d) The MPU performs an internal hardware initialization (enable HSI and option-byte loading with 130 µs duration), and then enters Run mode.
   e) The EADLY delay timer is started.
4. When EADLY elapses, the boot ROM starts accessing external peripherals (for example flash memory), to load and execute the boot software (Periph Boot). Implicitly, when EADLY has elapsed, all regulator voltages should be stable; especially V_{DD_PERIPH}, which is the power domain supplying flash memory.

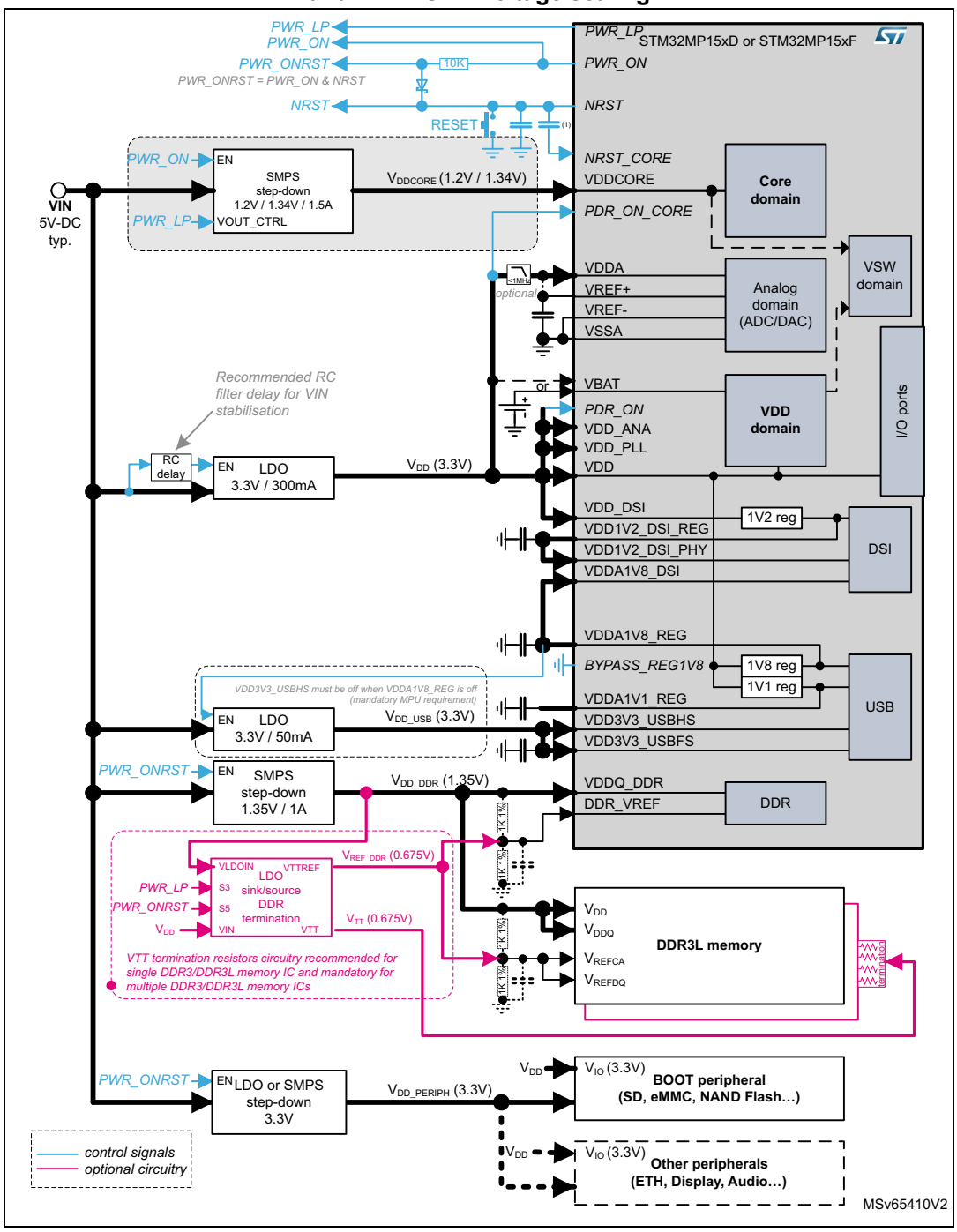
5 STM32MP15xD and STM32MP15xF enhanced CPU frequency supply management

The STM32MP15xD and STM32MP15xF devices have an enhanced consumer mission profile (see AN5438 *[8]*). This profile allows the ARM® dual Cortex®-A7 CPUs to run at a higher clock frequency (see DS12505 *[5]* for details and limitations).

Accordingly, the V_{DDCORE} supply voltage must be increased when the CPU frequency (Fmpuss_ck) operates above 650 MHz. When it does not operate in Run mode above 650 MHz, the VDDCORE supply voltage must be set back to its nominal voltage (1.2 V typ.). This means that the voltage regulator module must support two output voltages. In this application note, we have chosen to use LP-Stop mode. Consequently, the two output voltages are driven by the PWR_LP signal of the MPU. See *Section 6.2.1: VRM specification for VDDCORE power domain for STM32MP15xD and STM32MP15xF devices* for details about VRM.

Figure 11 shows the same application as the one in *STM32MP15x with DDR3L and 3.3 V I/O voltage interface*, except for the VDDCORE supply power source.

Figure 11. Discrete power supply topology example with IOs at 3.3 V, DDR3L and VDDCORE voltage scaling



1. It is recommended to add a capacitor between NRST and NRST_CORE when V_{DD} = 3.3V. It is also possible to connect NRST_CORE directly to NRST.
2. MPU decoupling scheme is not shown (see AN5031).
3. SMPS and LDO regulator product part numbers and discrete components are not shown, but their electrical specifications are detailed in *Section 6: Voltage regulator module (VRM) specification*.
4. Additional protection on VIN, such as ESD, EMI filtering, or over-voltage is not shown.

5.1 Crash recovery management and specific system operating modes

The information given in *Section 3.3: Low power modes and crash recovery management* also applies to the STM32MP15xD and STM32MP15xF devices, except *Table 3: System operating modes* which is replaced by *Table 4: System operating modes*.

This table summarizes power supply states for the application operating modes illustrated in *Figure 11: Discrete power supply topology example with IOs at 3.3 V, DDR3L and VDDCORE voltage scaling*.

Table 4. System operating modes

Power mode	**NRST NRST_CORE**	**VDD**	**PWR_ON / VDDCORE**	**PWR_ON / VDDCORE**	**PWR_LP / VTT**
Run	1	On	1 / On_hv(1)	1 / On	1 /On
Stop	1	On	1 / On_hv(2)	1 / On	1 / On
LP-Stop	1	On	1 / On_nom(3)	1 / On	0 / Off
Standby	1	On	0 / Off	0 / Off	0 / Off
VBAT or Power off	-	**Off** (No VIN)	**Off** (No VIN)	**Off** (No VIN)	**Off** (No VIN)
Crash (watchdog elapsed)	0 (pulse)	On	1 / On_hv	0 / Off	1 / VTT Off

1. On high voltage: VDDCORE = 1.34 V enhanced CPU frequency voltage.
2. Regarding reliability of enhanced CPU frequency mission profile, using Stop with 'high voltage' is considered as a RUN. With the VRM described in this application note, it is recommended to use LP-Stop instead of Stop mode.
3. On nominal voltage: VDDCORE = 1.2 V nominal voltage.

5.2 Power-up/power-down sequence and reset management

The data given in *Section 4.1: Power-up/power-down sequence and reset management* are also valid for the STM32MP15xD and STM32MP15xF devices, except the VDDCORE voltage value: 1.34 V instead of 1.215 V.

5.3 Low-power mode management

5.3.1 LP-Stop mode

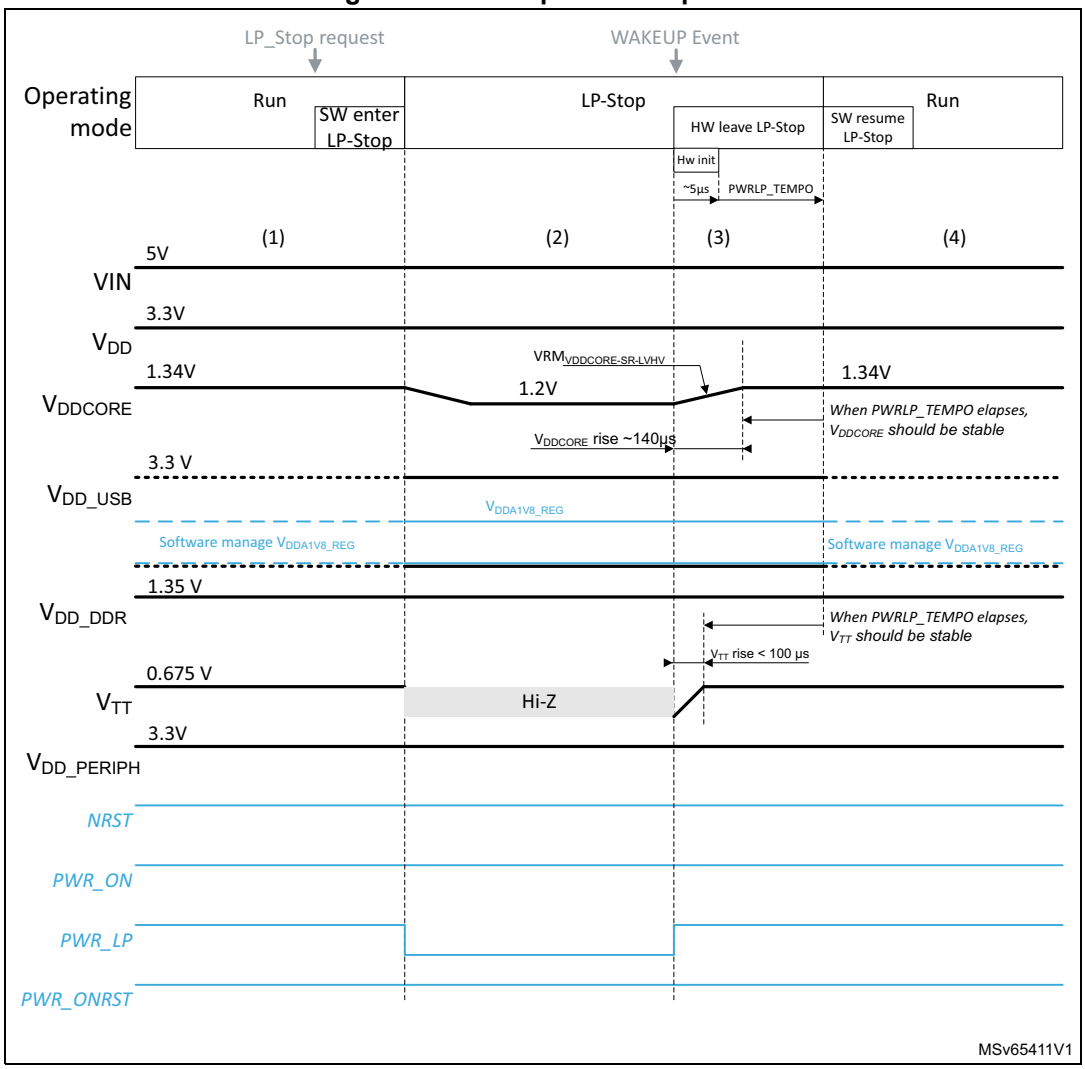
The application LP-Stop mode sequence is shown in *Figure 12: LP-Stop mode sequence* according to the implementation shown in *Figure 11: Discrete power supply topology example with IOs at 3.3 V, DDR3L and VDDCORE voltage scaling*.

In this application, VDDCORE is driven with two voltages:

- 1.34 V in Run mode for enhanced CPU frequency support
- 1.2 V in Low power stop mode

In Low power mode, the V_{TT} regulator is set in high impedance.

Figure 12. LP-Stop mode sequence



1. The application is powered and running. When LP_Stop mode is requested, the software prepares an LP_Stop entry (stops some clocks, sets DDR to self-refresh, sets PWRLP_TEMPO, and so on). It then sets the LPDS register to enter LP-Stop mode: the PWR_LP signal is asserted:
   a. V_{TT} enters low power mode (high impedance).
   b. V_{DDCORE} voltage decreases to $VRM_{VDDCORE-LPSTOP}$ voltage (1.2V) and is stabilized.
2. On a wakeup event, the MPU leaves LP-Stop mode and de-asserts the PWR_LP signal:
   a. V_{TT} exits low power mode.
   b. V_{DDCORE} voltage rises to $VRM_{VDDCORE-RUN}$ voltage (1.34V) with $VRM_{VDDCORE-SR-LVHV}$ slew rate and is stabilized.
   c. A clock restore process is performed.
   d. Once the HSI clock oscillator is stable (after ~5µs), the PWRLP_TEMPO timer is timed out to wait for the V_{TT} regulator, and V_{DDCORE} voltages to stabilize. In this application, the V_{TT} regulator recovery is below 100 µs and VDDCORE regulator recovery is approximately 140 µs. Hence, the PWRLP_TEMPO duration should be 140 µs minimum (max rising duration value between V_{TT} and V_{DDCORE}).
3. When PWRLP_TEMPO elapses, the application enters Run mode. The software resumes from LP-Stop mode (restores clocks, resumes DDR from self-refresh, and so on). Depending on the USB activity, the software may turn VDDA1V8_REG (internal regulator of MPU) on or off, which automatically turns the VDD_USB regulator on or off.

5.3.2 Standby mode

The data given in *Section 4.2.2: Standby mode* are also valid for the STM32MP15xD and STM32MP15xF devices, except the VDDCORE voltage value: 1.34 V instead of 1.215 V.

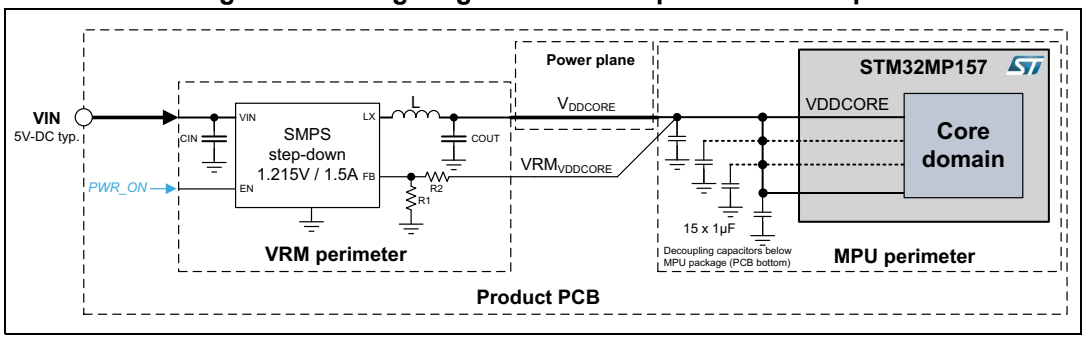
6 Voltage regulator module (VRM) specification

This section provides the electrical specifications of the voltage regulator module (VRM) that supplies the MPU power domains.

The product designer must design the VRM (see *Figure 13*) according to these electrical specifications by selecting a regulator IC and the associated discrete components.

This section is only applicable if the MPU decoupling scheme (see AN5031 *[1]*) and layout recommendations are carefully followed in order to minimize the impedance of the power delivery network.

Figure 13. Voltage regulator module perimeter example



6.1 VRM specification for VDD (V_{DD_ANA}, V_{DD_PLL}, V_{DD_DSI}) power domain

V_{DD} is the main supply for IO voltage interfaces and internal parts kept powered during Standby mode. V_{DD_ANA}, V_{DD_PLL} and V_{DD_DSI} must be connected to V_{DD}. V_{DD} is usually 1.8 V or 3.3 V, can be set in the 1.71 V to 2 V or 2.7 V to 3.6 V ranges.

This supply is always enabled as long as VIN voltage is present. Choosing a regulator with an EN pin is not necessary. Nevertheless, an EN pin may require a discrete RC filter to be added to delay the regulator startup for the purpose of input voltage stabilization.

Table 5. VRM specification for VDD power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
VRM_{VDD}	Output voltage range	Including VRM_{VDD-N}	1.71 2.7	1.8 3.0 or 3.3	2.0 3.6	V
$VRM_{VDD-ACC}$	Output voltage accuracy	Including line regulation, load regulation and temperature variation	-5	-	+5	%
VRM_{VDD-N}	Output noise voltage (ripple voltage for SMPS)	I_{OUT} = 10 µA to 300 mA f = 10 Hz to 5 MHz	-	-	30	mV_{p-p}
VRM_{IDD}	Continuous output current		300	-	-	mA
$VRM_{VDD-TRANS}$	Load transient regulation	I_{OUT} = 1 mA to 100 mA or 100 mA to 1 mA in 1 µs	-	-	+/-30	mV

6.2 VRM specification for VDDCORE power domain

V_{DDCORE} is the main digital voltage supplying the whole MPU core parts including the dual-core Arm® Cortex®-A7 CPU and the 3D Vivante® GPU. Significant current load transients therefore occur on the V_{DDCORE} supply. Accordingly, special attention on MPU decoupling capacitor placement and layout should be done to minimize the power delivery network impedance.

As V_{DDCORE} is turned OFF in Standby mode, a regulator having the EN pin is required to support Standby mode. In addition to the selection of a regulator with an output discharge resistor, it is recommended to allow a fast voltage decrease when the regulator is disabled. This is in order to minimize the POPL timer MPU register settings when the application enters standby mode).

Table 6. VRM specification for VDDCORE power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
$VRM_{VDDCORE}$	Output voltage		-	1.215	-	V
$VRM_{VDDCORE-ACC}$	Output voltage accuracy	Including line regulation, load regulation and temperature variation	-2.88	-	+2.88	%
$VRM_{VDDCORE-RIPPLE}$	Output noise / ripple voltage	I_{OUT} = 1 mA to 1500 mA f = 10 Hz to 5 MHz	-	-	30	mV_{p-p}
VRM_{ICORE}	Continuous output current		1500	-	-	mA
$VRM_{VDDCORE-TRANS}$	Load transient regulation	I_{OUT} = 1 mA to 450 mA or 450 mA to 1 mA in 1 µs	-	-	+/-30(1)	mV
$VRM_{VDDCORE-SR}$	Output voltage slew rate at start-up	$VRM_{VDDCORE}$ from $V_{PVDCORE\_0}$ to $V_{DDCORE-Min}$	1.15	-	-	mV/µs

1. Voltage overshoot / undershoot caused by load transients must not go higher than $VRM_{VDDCORE}$ + $VRM_{VDDCORE-TRANS}$ for a negative transient current, and must not go lower than $VRM_{VDDCORE}$ - $VRM_{VDDCORE-TRANS}$ for a positive current transient. Implicitly, output voltage noise / ripple ($VRM_{VDDCORE-RIPPLE}$) is included in the $VRM_{VDDCORE-TRANS}$ budget.

6.2.1 VRM specification for VDDCORE power domain for STM32MP15xD and STM32MP15xF devices

When the Arm® dual Cortex®-A7 operates in enhanced mode at an 800-MHz clock frequency, the VRM must provide $VRM_{VDDCORE-RUN}$ voltage to V_{DDCORE} of the MPU. When the application operates in LP-Stop mode, the VRM must provide $VRM_{VDDCORE-LPSTOP}$ voltage to V_{DDCORE} of the MPU. Consequently, the VRM must support two controllable output voltages that are driven by the PWR_LP signal of the MPU (see *Table 12* for further details).

The VRM electrical specifications are provided in *Table 7*.

Section 7.3 provides an example of a VRM circuit.

Table 7. VRM specification for VDDCORE power domain with voltage scaling for 800 MHz support

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
$VRM_{VDDCORE-RUN}$	Output voltage in Run mode	STM32MP15xF above 650 MHz in Run mode	-	1.34	-	V
$VRM_{VDDCORE-LPSTOP}$	Output voltage in LP-Stop mode	STM32MP15xF in LP-Stop mode		1.2		V
$VRM_{VDDCORE-ACC}$	Output voltage accuracy in Run or LP-Stop mode	including line regulation, load regulation and temperature variation	-2.98	-	+2.98	%
$VRM_{VDDCORE-SR-LVHV}$	Output voltage slew rate from LP-Stop to RUN operating mode	$VRM_{VDDCORE}$ from $VRM_{VDDCORE-LPSTOP-Min}$ to $VRM_{VDDCORE-RUN-Min}$	(see (1))	-	-	mV/µs

1. There is no technical constraint on the $VRM_{VDDCORE-SR-LVHV}$ value. Nevertheless, as described in *Section 5.3.1: LP-Stop mode*, the PWRLP_TEMPO timer of the MPU should be set according to the $VRM_{VDDCORE-SR-LVHV}$ value. For example, if VRM has a 1 mV/µs slew rate, the recovery voltage duration from $VRM_{VDDCORE-LPSTOP}$ to $VRM_{VDDCORE-RUN}$ takes 140 µs = (1340 mV – 1200 mV) × 1mV/µs. In this example, the PWRLP_TEMPO timer of the MPU should be set to 140 µs minimum. Adding a 10-20% margin is recommended to cover worst case conditions (temperature, tolerance, and so on). A slew rate from 1 to 10 mV/µs is recommended. A low slew rate value increases the current transient but decreases the output voltage recovery duration during LP-Stop to Run mode transition, and reciprocally for a high slew rate value.

The other VRM electrical specifications ($VRM_{VDDCORE-RIPPLE}$, VRM_{ICORE}, $VRM_{VDDCORE-TRANS}$, and $VRM_{VDDCORE-SR}$) are those defined in *Table 6: VRM specification for VDDCORE power domain*.

6.3 VDDQ_DDR power domain VRM specification

V_{DDQ_DDR} supplies the MPU DDR IO voltage interfaces. In addition to V_{DDQ_DDR}, the VRM should also supply the DDR ICs. This section only covers the VRM specification for dual DDR3L (see *Figure 1: Discrete power supply topology example with IOs at 3.3 V and DDR3L* for details). Special attention should be paid to decoupling capacitor placement and layout in order to minimize the power delivery network impedance for both the MPU V_{DDQ_DDR} supply, and DDR3L ICs. Please refer to AN5122 *[6]* for details.

As DDR memory is turned OFF in Standby mode, a regulator having an EN pin is needed to support Standby mode. Additionally, selection of regulator with output discharge resistor is recommended in order to allow a fast voltage decrease when the regulator is disabled (when application enters Standby mode).

Assumptions:

- The DDR3L supply voltage is 1.283 V to 1.45 V and 1.35 V typ. (from JEDEC JESD79-3-1A)
- 1.425 V maximum DC value (from JEDEC JESD79-3-1A) = 1.35 V + 5.5%
- VDDR max AC value = 25 mV (1.45 V – 1.425 V)
- Same value to be used for VDDR min AC
- 1.308 V minimum DC value (1.283 V + 0.025) = 1.35 V – 3.1%

Table 8. VRM specification for VDDQ_DDR and DDR3L IC power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
VRM_{VDDR}	Output voltage		-	1.35	-	V
$VRM_{VDDR-ACC}$	Output voltage accuracy	Including line regulation, load regulation and temperature variation	-3 (-3.1)(1)	-	+3 (+5.5)(1)	%
$VRM_{VDDR-RIPPLE}$	Output noise / ripple voltage	I_{OUT} = 1 mA to 1 A f = 10 Hz to 5 MHz	-	-	25	mV_{p-p}
VRM_{IDDR}	Continuous output current		1000	-	-	mA
$VRM_{VDDR-TRANS}$	Load transient regulation	I_{OUT} = 1 mA to 450 mA or 450 mA to 1 mA in 1 µs	-	-	+/-25(2)	mV
$VRM_{VDDR-SS}$	Soft start duration	Duration from EN pin rising (VRM_{VDDR} ~ 0) to 95% of VRM_{VDDR}	-	-	10(3)	ms

1. Values based on assumptions. Both are reduced to +/-3%.
2. Voltage overshoot / undershoot caused by load transients must not be higher than VRM_{VDDR} + $VRM_{VDDR-TRANS}$ for a negative transient current, and must not be lower than VRM_{VDDR} - $VRM_{VDDR-TRANS}$ for a positive current transient. Implicitly, output voltage noise / ripple ($VRM_{VDDR-RIPPLE}$) is included in the $VRM_{VDDR-TRANS}$ budget.
3. 10 ms is the reset value of MPU's EADLY timer. EADLY is an MPU timer that is set by software to wait for the regulator voltage to be ready before entering Run mode, as detailed in *Section 4: Power sequence management*.

7 Voltage regulator module examples

7.1 VRM example for 5 V DC to 3.3 V DC - 300 mA

Figure 14. VRM 5 V to 3.3 V - 300 mA details

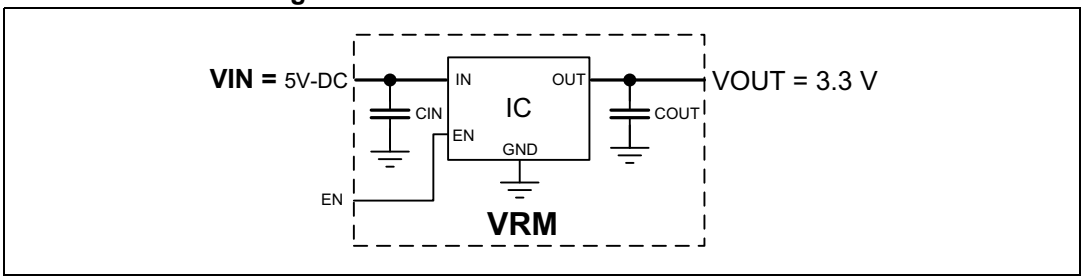


Table 9. VRM example for 5 V to 3.3 V - 300 mA

Component	Description
IC	Fixed 3.3 V LDO DFN4-1x1 mm - ON Semiconductor NCP161AMX330TBG
CIN / COUT	MLCC - 1 µF - 6.3 V - 0402 - Murata GRM155R60J105KE19

7.2 VRM example for 5 V DC to 1.215 V DC - 1500 mA

Figure 15. VRM 5 V to 1.215 V / 1500 mA details

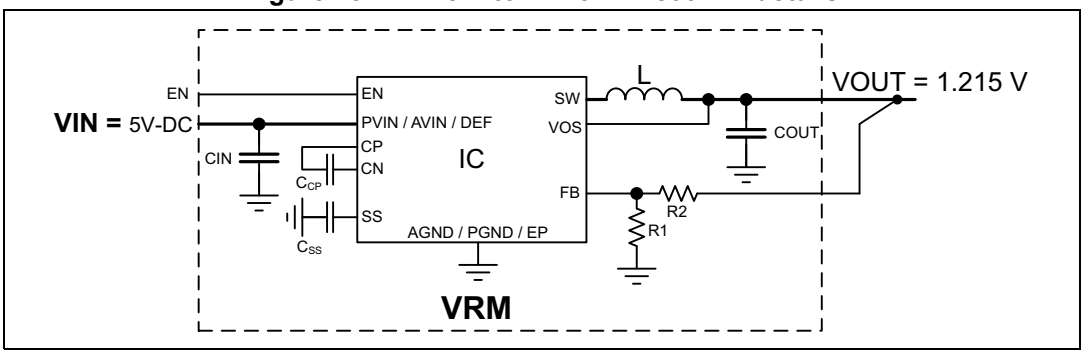
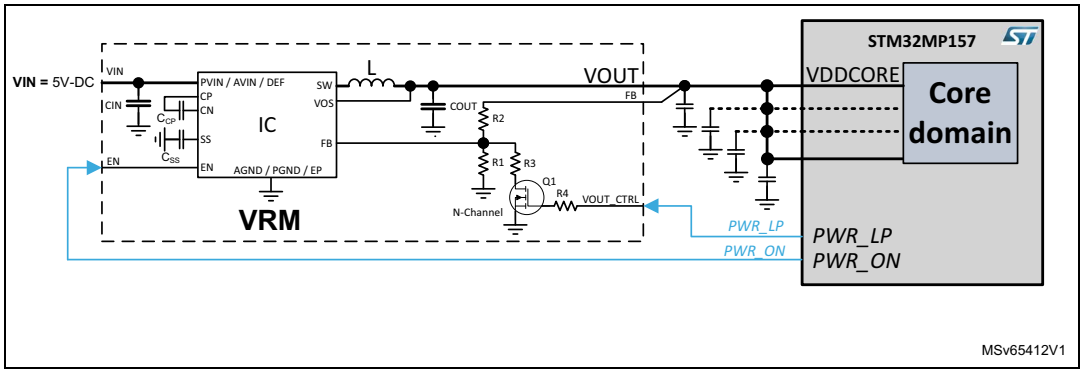


Table 10. VRM example for 5 V to 1.215 V - 1500 mA

Component	Description
IC	Adjustable 3A step-down SMPS - VQFN-3x3 mm – Ti TLV62090RGT
L	Power inductor – 1 µH – 3.22 A – 14 mΩ – Wurth 74404043010A
CIN	MLCC - 10 µF - 10 V - 0603 - Murata GRM188R61A106KE69D
COUT	2 x MLCC – 22 µF – 6.3 V – 0603 – Murata GRM188R60J226MEA0J
C_{CP} / C_{SS}	MLCC – 10 nF - 16 V - 0402 – Yageo CC0402KRX7R7BB103
R1	160 kΩ - 1%
R2	82.5 kΩ - 1%

7.3 VRM example for 5V DC to scalable 1.34 V / 1.2 V DC - 1500 mA

Figure 16. VRM 5 V to scalable 1.34 V / 1.2 V - 1500 mA details



The VRM in *Figure 16* has an additional circuit inserted into the feedback loop which allows to control two output voltages (see *Section 7.3.1: Vout (R1, R2, R3, R4) computation example* for details).

Table 11. VRM example for 5 V to 1.34V / 1.2 V - 1500 mA

Component	Description
IC	Adjustable 3 A step-down SMPS - VQFN-3x3 mm – Ti TLV62090RGT
L	Power inductor – 1 µH – 3.22 A – 14 mΩ – Wurth 74404043010A
CIN	2 x MLCC – 10 µF - 10 V - 0603 - Murata GRM188R61A106KE69D
COUT	2 x MLCC – 22 µF – 6.3 V – 0603 – Murata GRM188R60J226MEA0J
C_{CP} / C_{SS}	MLCC – 10 nF - 16 V - 0402 – Yageo CC0402KRX7R7BB103
R1	150 kΩ - 1%
R2	75 kΩ- 1%
R3	430 kΩ- 1%
R4	150 kΩ - 5%
Q1 (1)	N-Channel MOSFET, Vgs(th):1V, Vds:20 V, Id:0.5 A - Vishay Si1062x

1. Key parameter for Q1 MOSFET selection:
   - N-Channel
   - I_{DSS} << 2µA (condition: Vds = 0.8V, Vgs = 0 V)
   - $V_{GS(th)}$ < 1.8 V (should be below PWR_LP IO voltage; so below VDD voltage of the MPU)
   - I_D min > 2 µA
   - V_{DS} > 0.8 V
   - Crss recommended below 20pF (this is to avoid energy transfers from the PWR_LP signal to the Q1 Gate-to-Drain (through Crss) and then to the feedback node of IC during the PWR_LP signal transition. This energy transfer can disturb the feedback node of IC causing a small overshoot and undershoot during PWR_LP signal transition for a few µs).

Table 12. VRM 1.34V / 1.2 V truth table

EN	VOUT_CTRL	VOUT
0	-	0 V (OFF)
1	0	1.2 V
1	1	1.34 V

7.3.1 Vout (R1, R2, R3, R4) computation example

The IC (step-down SMPS) used in *Figure 16* has a feedback voltage equal to V_{BF} = 0.8 V.

1. When VOUT_CTRL = 0 (LP-Stop mode), the MOSFET Q1 is open and the Q1 Drain node is floating. The output voltage VOUT is minimum and is equal to:
   $VOUT_0 = (R1 + R2) / R1 \times V_{FB} = (150 + 75) / 150 \times 0.8 = 1.2$ V
2. When VOUT_CTRL = 1 (Run mode), the MOSFET Q1 is closed and the Q1 Drain node is grounded (Q1 R_{DSON} neglected compared to the R3 value). The output voltage VOUT is maximum and is equal to:
   $VOUT_1 = (R1//R3 + R2) / R1//R3 \times V_{FB} = (111.2 + 75) / 111.2 \times 0.8 = 1.339$ V

R1 and R2 need to be selected first to reach an output voltage of $VOUT_0$ = 1.2 V.

In this first step, choose an arbitrary value for R1 or R2. In the second step, R3 should be selected to reach $VOUT_1$ = 1.34 V.

R4 has a high value to increase the miller plate effect duration to reduce the turn-on delay time of the Q1 transistor. R4 value should be adapted to reach a reasonable output voltage slew rate ($VRM_{VDDCORE-SR-LVHV}$) in between 1 to 10 mV/µs.

7.4 VRM example for 5V DC to 1.35 V DC - 1000 mA

Figure 17. VRM 5 V to 1.35 V - 1000 mA details

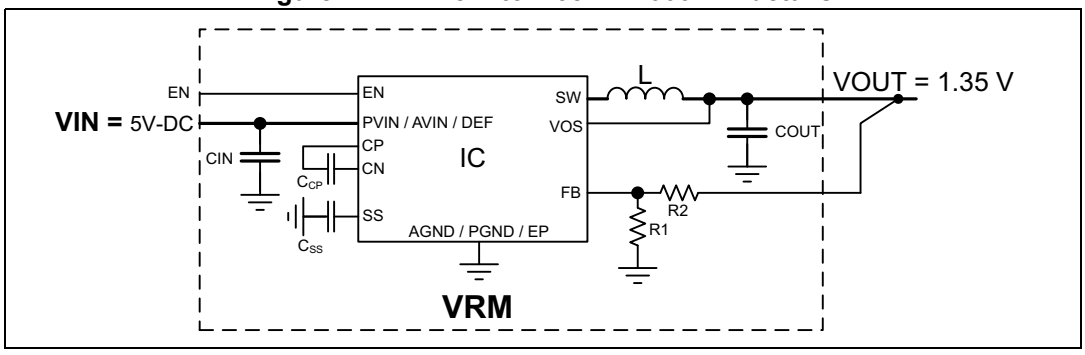


Table 13. VRM example for 5 V to 1.35 V - 1000 mA

Component	Description
IC	Adjustable 3 A step-down SMPS - VQFN-3x3 mm – Ti TLV62090RGT
L	Power inductor – 1 µH – 3.22 A – 14 mΩ – Wurth 74404043010A
CIN	MLCC - 10 µF - 10 V - 0603 - Murata GRM188R61A106KE69D
COUT	2 x MLCC – 22 µF – 6.3 V – 0603 – Murata GRM188R60J226MEA0J
C_{CP} / C_{SS}	MLCC – 10 nF - 16 V - 0402 – Yageo CC0402KRX7R7BB103
R1	160 kΩ - 1%
R2	110 kΩ - 1%

7.5 VRM example for 5V DC to 3.3 V DC - 2000 mA

Figure 18. VRM 5 V to 3.3 V - 2000 mA details

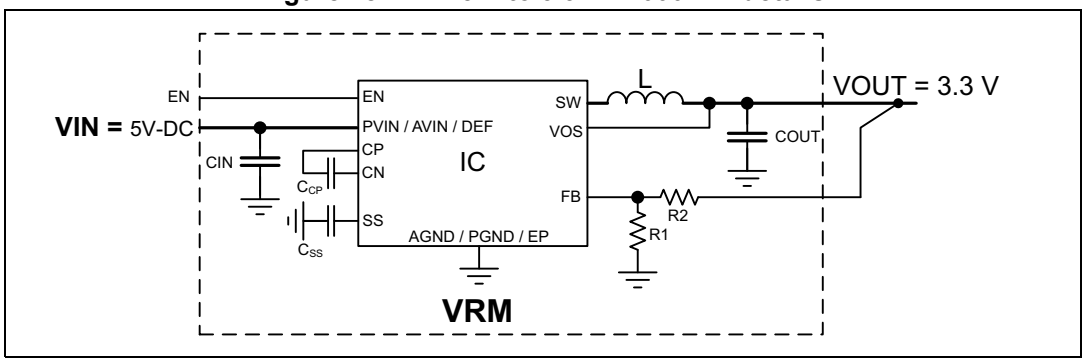


Table 14. VRM example for 5 V to 3.3V - 2000 mA

Component	Description
IC	Adjustable 3 A step-down SMPS - VQFN-3x3 mm – Ti TLV62090RGT
L	Power inductor – 1 µH – 3.22 A – 14 mΩ – Wurth 74404043010A
CIN	MLCC - 10 µF - 10 V - 0603 - Murata GRM188R61A106KE69D
COUT	2 x MLCC – 22 µF – 6.3 V – 0603 – Murata GRM188R60J226MEA0J
C_{CP} / C_{SS}	MLCC – 10 nF - 16 V - 0402 – Yageo CC0402KRX7R7BB103
R1	150 kΩ - 1%
R2	470 kΩ - 1%

8 Revision history

Table 15. Document revision history

Date	Revision	Changes
11-Jul-2019	1	Initial version.
14-Feb-2020	2	Added information on STM32MP15xD and STM32MP15xF devices (800 MHz extended frequency supported): – Added *Section 5: STM32MP15xD and STM32MP15xF enhanced CPU frequency supply management*, *Section 6.2.1: VRM specification for VDDCORE power domain for STM32MP15xD and STM32MP15xF devices*, *Section 7.3: VRM example for 5V DC to scalable 1.34 V / 1.2 V DC - 1500 mA* and *Section 7.3.1: Vout (R1, R2, R3, R4) computation example*. Updated *Table 1: Reference documents*, *Figure 1: Discrete power supply topology example with IOs at 3.3 V and DDR3L* and *Figure 4: Discrete power supply topology example with IOs at 1.8 V and DDR3L* Updated *Section 3.1.2: Regulator topology recommendations for LDO or SMPS*, *Section 3.3: Low power modes and crash recovery management*, *Section 6.2: VRM specification for VDDCORE power domain* and *Section 6.3: VDDQ_DDR power domain VRM specification*. Modified note 2 in *Table 8: VRM specification for VDDQ_DDR and DDR3L IC power domain* Changed title of *Section 7.4: VRM example for 5V DC to 1.35 V DC - 1000 mA* (1000 mA and 1.35V) Changed title of *Table 14: VRM example for 5 V to 3.3V - 2000 mA* (2000 mA and 3.3V)
25-Nov-2022	3	Added one capacitor between NRST and NRST_CORE in *Figure 1: Discrete power supply topology example with IOs at 3.3 V and DDR3L*, *Figure 4: Discrete power supply topology example with IOs at 1.8 V and DDR3L* and *Figure 11: Discrete power supply topology example with IOs at 3.3 V, DDR3L and VDDCORE voltage scaling* and added note 1 to *Figure 1* and *Figure 4* Modified notes 2.a) and 3.b) below *Figure 10: Crash recovery sequence*.