AN5268
Application note

Driving high power DC motor by paralleling M0-7 VNHD7xxxAY H-Bridge and M0-7 high-side driver

Introduction

This document gives some guidelines in order to drive a high power DC motor using VNHDxxxAY and one HSD switched in parallel. By doing this the equivalent Rd_{son} is decreased and matched with the motor current profile.

The relevant verification in this document is performed on the combination of VNHD7008AY in parallel with VND7020AJ.

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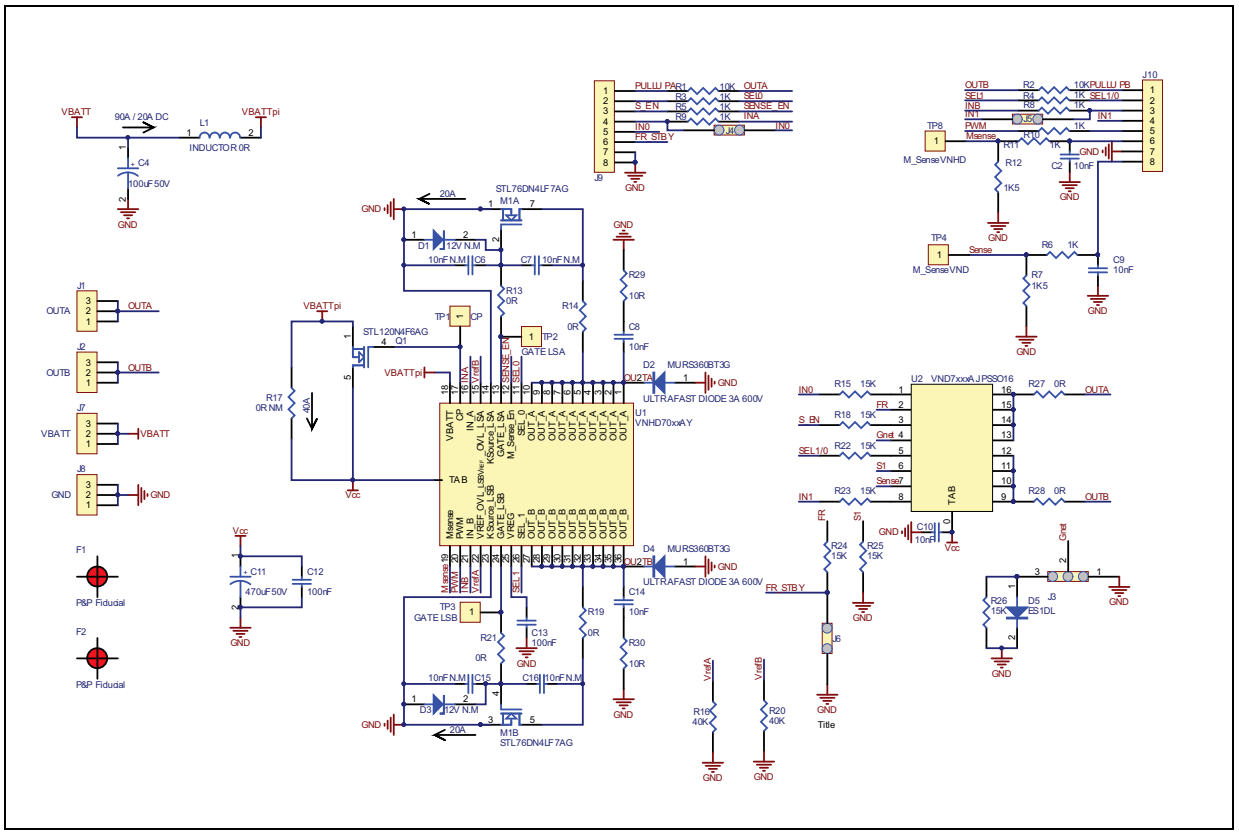
1 High power DC motor driving

1.1 Reference schematic and layout

Figure 1. Used Application Schematic

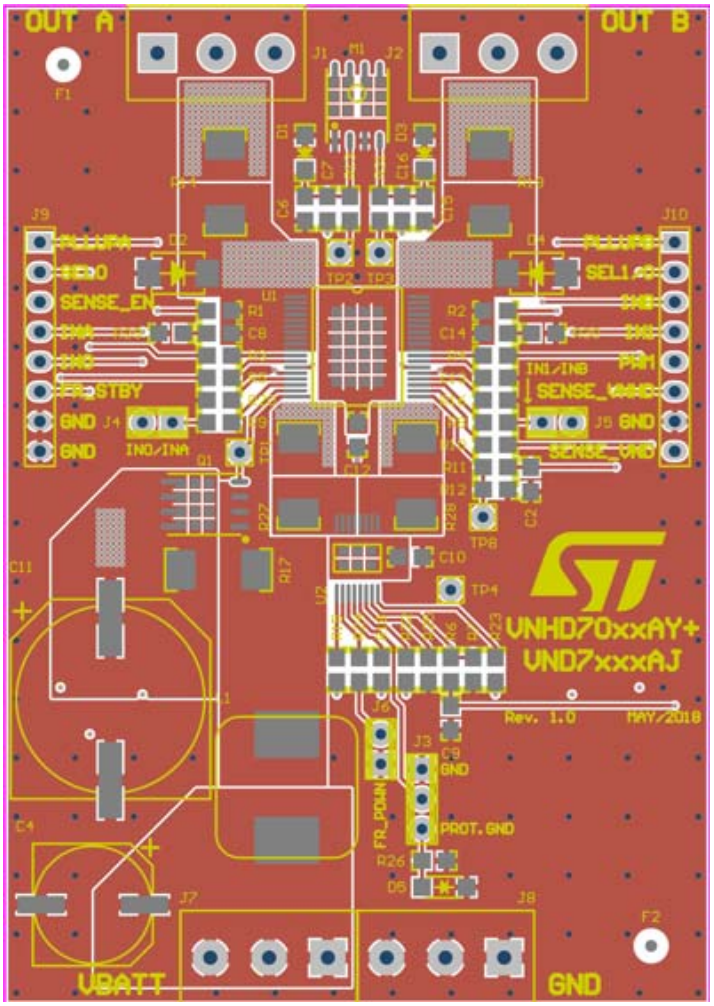


Note: *- Symmetric connection with both source pins of the external Mosfets and GND*

- Optimized connection between the K source pin and the source of the external Mosfets

- Drain of external Mosfets must be connected with the Outx pin with the lowest impedance path.

Figure 2. PCB Layout



In the standard configuration the jumper J3 is in the position 1-2 and the reverse battery protection MOSFET (STL120N4) is shared between VNHD7008AY and VND7020AJ. Diodes D2 and D4 are not mounted.

1.2 General

Both VNHD7008AY and VND7020AJ belong to the same (M0-7 High Side Drivers).

PWM: In this application the assumption is that there is no usage of frequency toggled PWM.

Latch-OFF mode: It is recommended that devices are set in the Latch-OFF mode. The H-bridge has the latch mode already integrated, but this function is configurable in the VND7020AJ. Therefore the “Fault_RST” pin has to be set to High.

Current distribution: The current distribution is not equal between the two device channels. A general assumption, without considering any other condition, is based on the device Rdson.

Example. If load current = 80A; VND7020AJ ~ 22A, VNHD7008AY ~ 58A

Vcc: both devices are connected to the same battery line. We consider that HSA is paralleled with HS0 and that HSB is paralleled with HS1.

1.3 Reverse battery protection and GND network

A centralized protection (a unique device placed on Vcc) can be applied in the given configuration. The suggestion is to use an N-MOS on Vcc line. The gate of the N-MOS can be driven directly by the embedded CP pin of VNHD7008AY. This solution avoids the usage of a dedicated GND network for VND7020AJ.

1.4 Inductive short circuit

The inductive OUT to GND short-circuit current circulates in the parasitic body diodes of the Low Side PowerMOS.

1.5 Activation timings (timing tables extracted from datasheets)

The devices have the same technology (M0-7) but the timings are different.

Turn ON and OFF switching times of VND7020AJ are typically longer than the ones of VNHD7008AY (see *Section Appendix A: Document references*).

Figure 3. Extract of VNHD7008AY Datasheet, switching times

VNHD7008AY Electrical specifications

Table 8. HSD switching (V_{CC} = 13 V; RLOAD = 1.1 Ω)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	Input rise time < 1 µs; MultiSense_EN = 5 V (no standby); $SEL_{0,1}$ = 0; PWM = 0 (see *Figure 6*)		53		µs
$t_{d(off)}$	Turn-off delay time	Input rise time < 1 µs; MultiSense_EN = 5 V (no standby); $SEL_{0,1}$ = 0; PWM = 0 (see *Figure 6*)		20		µs

Figure 4. Extract of VND7020AJ Datasheet, switching times

VND7020AJ Electrical specification

Table 6: Switching

V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ (1)	Turn-on delay time at T_j = 25 °C	R_L = 4.3 Ω	10	60	120	µs
$t_{d(off)}$ (1)	Turn-off delay time at T_j = 25 °C		10	40	100	
$(dV_{OUT}/dt)_{on}$ (1)	Turn-on voltage slope at T_j = 25 °C	R_L = 4.3 Ω	0.1	0.36	0.7	V/µs
$(dV_{OUT}/dt)_{off}$ (1)	Turn-off voltage slope at T_j = 25 °C		0.1	0.36	0.7	

1.6 Static Cross current

The cross current could appear in this application only in case of deactivation of the motor when HSD is turned off and PWM is high.

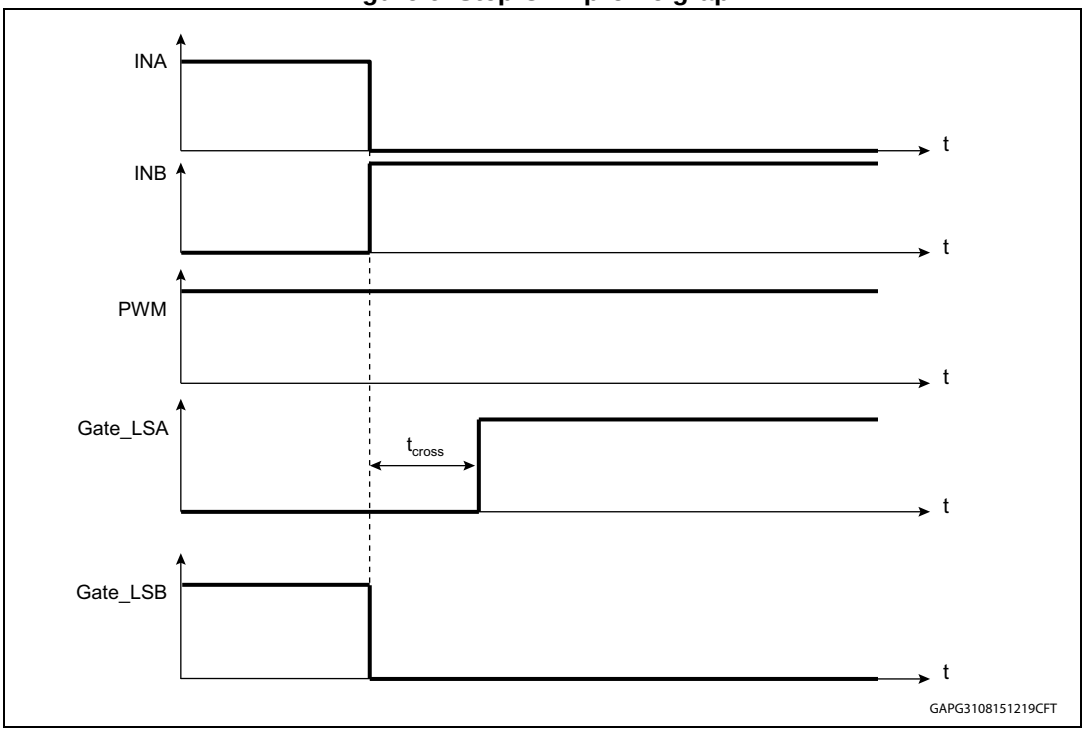
The VNHD7008AY integrates a cross current protection mechanism. This is not present in VND7020AJ which is a simple HSD.

The protection consists of a delay in turning on the LSA (LSB) after INA (INB) goes from high to low as described in *Figure 5* (see *Section Appendix A: Document references*):

Figure 5. Extract of VNHD7008AY Datasheet, tcross limits

t_{cross}	Low-side turn-on delay time	Input rise time < 1 µs (see *Figure 7*)	40	160	300	µs

Figure 6. Step CLK profile graph



1.7 Dynamic cross current

Dynamic cross current or shoot through, may happen whenever one Low Side is turned ON (due to capacitive effect on the HSD in off state).

If the VinA / VinB is high, the Vout commutation (due to PWM transition) generates a dV/dt that is able to reactivate the off High Side of VND7020AJ.

Dynamic cross current can be avoided by limiting dV/dt on VND7020AJ output as explained in the user manual UM1922 chapter 11. In the following section a method is shown in order to avoid any dynamic cross current on VND7020AJ.

1.7.1 Turn ON phase:

Assumption is that the input pins of VNHD7008AY and VND7020AJ are connected in parallel. When motor has to be activated, it is recommended to follow the following steps:

1. Leave the standby state setting one control pin (for example MultiSense_EN) from Low to High whilst all other control pins are left Low
2. Set PWM pin from Low to High
3. Set INA=IN0 (resp. INB=IN1) from Low to High to activate the motor clockwise (resp. anticlockwise)

Step 2 and 3 can be done together since transition of the Low Side MOSFET is much faster than the transition of both VNHD7008AY and VND7020AJ.

Test description

- Voltage: 16V;
- Temperature: 25°C, -40°C;
- VinA = Vin0 = 0V;
- VinB = Vin1 = 5V;
- VND7020AJ configured in Auto-restart mode;
- Load: Fan Motor loaded;
- PWM = 0 → 5V

1.8 Turn OFF phase

The main effect which has to be considered in case of turning OFF of the motor is the fact that VND7020AJ has no intrinsic circuitry against any cross current (neither static - related to no contemporary ON state of one High Side nor one Low Side on the same leg - nor dynamic related to a high dV/dt on VND7020AJ output).

It is suggested to anticipate PWM setting form High to Low versus VINA (or VINB) setting from High to Low. The following test has been conducted in order to check this topic. Assumption is that the input pins of VNHD7008AY and VND7020AJ are connected in parallel.

Test description:

- Voltage: 13V;
- Temperature: 25°C;
- Load: Fan Motor loaded;
- VinB = Vin0 = 0V → 5V → 0V;
- VinA = Vin1 = 0V;
- VND7020AJ configured in Auto-restart mode;
- PWM = 0V → 5V → 0V; (anticipated versus VinB/A)

Result:

- During switch OFF, the VND7020AJ reactivation is avoided if VinA is pulled down when the motor current recirculation has already finished. For this reason it is suggested to anticipate the setting of PWM from High to Low versus VINA (or VINB) from High to Low. The anticipation time depends on mechanical/electrical motor parameters.

In *Figure 7* it is shown the case where the deactivation of VINB is shifted versus PWM so that recirculation current of the motor is still flowing through the HSB and HS0 and parasitic diode of HSA and HS1. There is a dynamic cross current flowing in the HSB VND7020AJ due to high dV/dt in OUTPUTB.

In *Figure 8* it is shown the case where the deactivation of VINB is shifted versus PWM so that recirculation current of the motor is already exhausted. Dynamic cross current is in this case avoided.

Figure 7. Delay between PWM high and input low less than recirculation time

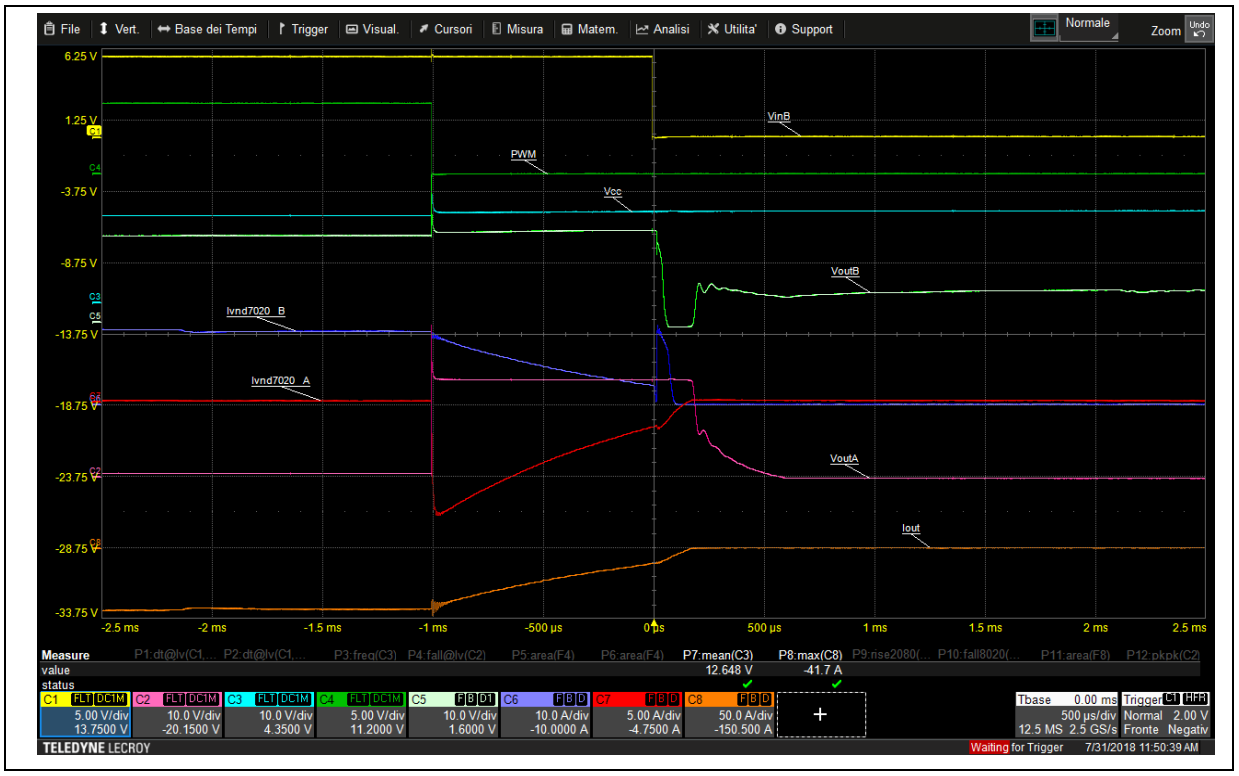


Figure 8. Delay between PWM high and input low is higher than recirculation time

1.9 Motor direction changing (Dynamic Turning ON / OFF the legs)

In case of motor directing changing, the above described turning ON / OFF will be performed on each H-bridge leg periodically. Therefore please refer to the above recommendations.

Appendix A Document references

- *H-bridge motor driver for automotive DC motor driving* (Datasheet, DS11459)
- *Double channel high-side driver with MultiSense analog feedback for automotive applications* (Datasheet, DS7213)

Revision history

Table 1. Document revision history

Date	Revision	Changes
07-Jan-2019	1	Initial release.