EVALKITSTKNX user guide and performance report

Introduction

The EVALKITSTKNX in Figure 1 is the evaluation kit of the STKNX integrated circuit: a miniature KNX-certified (Figure 2) transceiver for Twisted Pair medium TP1-256. This document describes how to use the EVALKITSTKNX, its characteristics, and explains the electrical choices of the peripheral components to the STKNX. In addition, Section 4 KNX physical layer performance vs. 8/2/2 tests contains the electrical results of the EVALKITSTKNX for the Physical Layer tests according to the System Conformance Testing specification 8/2/2.

The kit offers the user the possibility to both evaluate the performances of the STKNX circuit and to build the prototype of a KNX device. Configuration jumpers allow testing of every possible configuration offered by STKNX regarding power supply, fan-in and isolation. The system is controlled by the STM32F103RBT6 microcontroller and can be customized thanks to extension connectors compatible with Arduino and Morpho ST standard, by plugging a custom daughterboard or an existing STM32 Nucleo expansion board.

The EVALKITSTKNX also embeds the ST-LINK/V2-1 debugger/programmer to simplify project setup for the development of custom firmware.

Figure 1. STKNX evaluation kit (70 x 155 mm)

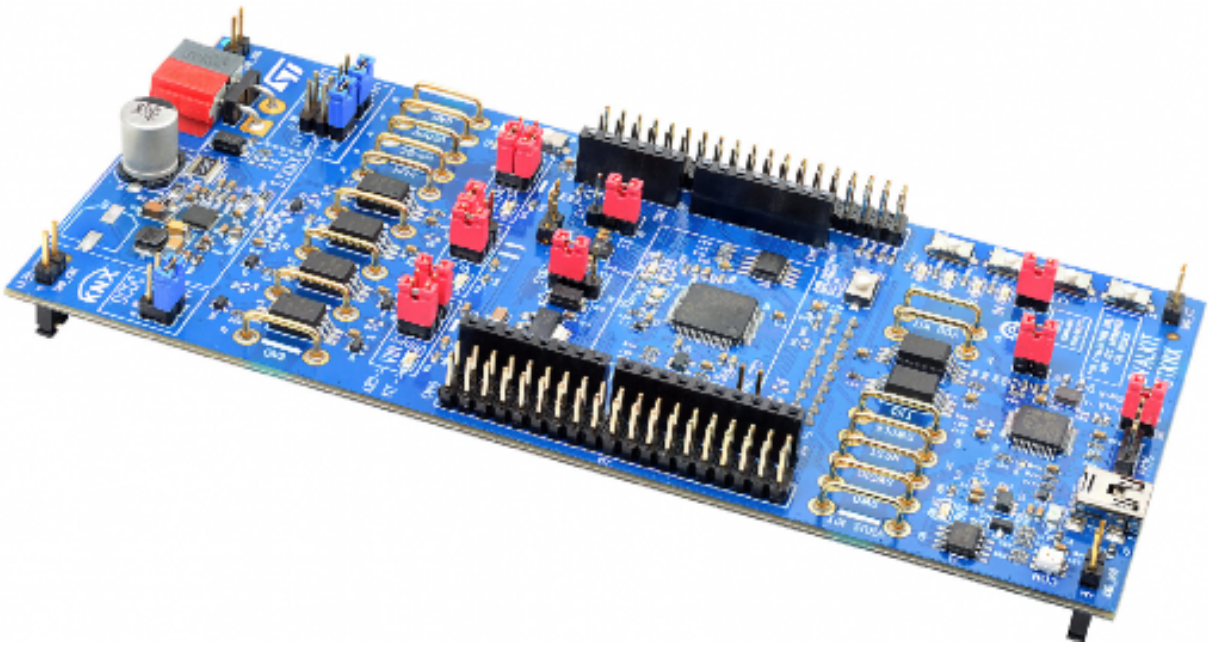


Figure 2. **STKNX certificate of conformity**

KNX CERTIFICATE OF CONFORMITY

CERTIFICATE No: ***447/14356/17***

Delivered to

STMICROELECTRONICS INTERNATIONAL N.V.
SWITZERLAND

This is to certify that the underneath listed product:

ST KITT 864L

Order number: **STKNXTR**
Application program: **STKNX**

has been satisfactorily assessed by KNX Association as regards software (report No. ***A1/114/1/17*** *from* ***2/23/2017***) under the rules of the KNX certification system against the requirements of the KNX specifications v2.1.

The certificate holder is granted right of entry of the above product into the KNX register of qualified products (established for the first time on ***3/29/2017***).

The certificate holder may use the KNX or EIB (see above) trademark in accordance with the relevant trademark rules, as laid down in the KNX trademark and certification documentation (KNX issue 02/2006).

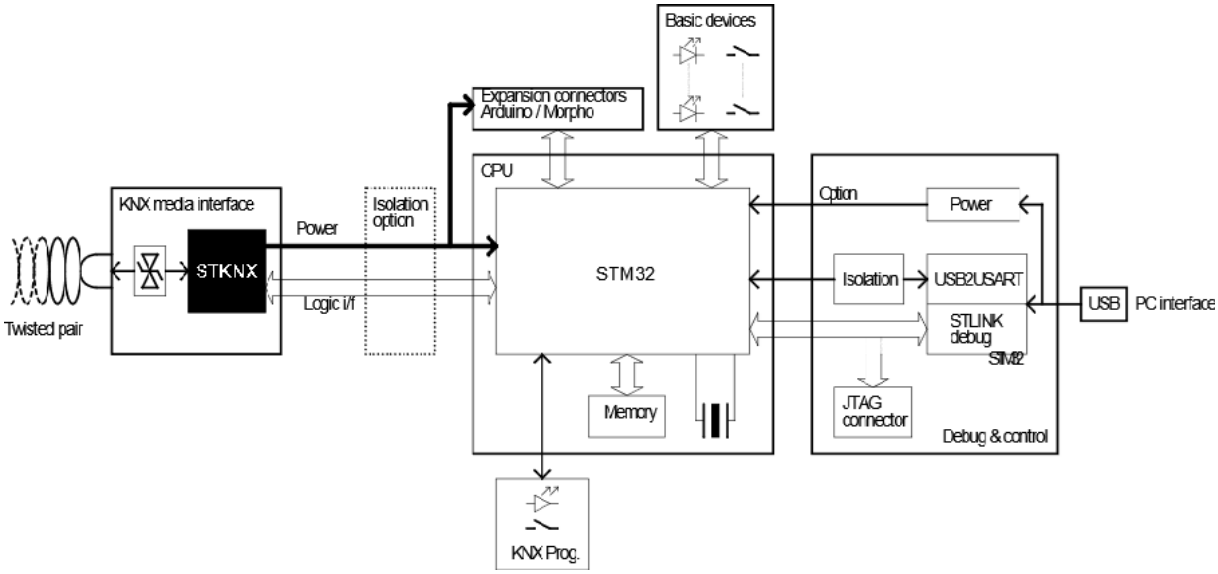
Subject to continuing compliance with the rules and the declaration previously given this certificate has an unlimited validity.

Joost Demarest, CTO
KNX Association

Date: 02 July 2018

1 EVALKITSTKNX presentation

Figure 3. **EVALKITSTKNX functional block diagram**



The STKNX transceiver and the STM32 controller sections make up the basic KNX node.

The STKNX section includes jumpers to configure and test the different possible settings of the circuit voltage regulators. The kit schematic indicates also the BOM changes that have to be applied to modify the DC-DC converter output voltage or the kit fan-in.

The default configuration of the EVALKITSTKNX is the following:

- Emulation of a KNX device with fan-in = 30 mA
- STKNX linear regulator voltage set to 3.3 V for CPU section supplying STKNX DC-DC converter voltage set to 5 V for external application.

The STM32 is connected to several peripherals:

- STKNX for KNX data transfer
- One key and one LED for the KNX programming function
- One EEPROM memory for configuration storing (not used by default firmware)
- Four keys emulating basic sensors or for any other application purpose
- Four LEDs emulating basic actuators or for any other application purpose
- Extension connectors for interfacing a daughterboard and customizing the kit.

Optional optocouplers are present to isolate the STKNX section if a non-safety voltage is present on the daughterboard (e.g., Remote Powered Device).

The debug section embeds a second STM32 which hosts:

- ST-LINK/V2-1 debugging environment for debugging purposes
- A mass-storage profile for ST-LINK development
- An isolated USB2UART connection to the target STM32 USART
- All of them, accessible from a single USB connector.

2 Quick start

2.1 System requirements

- A windows, Linux or Mac OSX PC
- A type A to mini-B USB cable

2.2 Getting started

Follow the sequence below to configure the EVALIKITSTKNX, launch demo software, or prepare to develop your own application:

1. Check that the jumpers on the kit are configured as described in Section 3.5.4.1 STKNX mode DC-DC 5 V (default) and that both jumpers M32 and M43 are open and M39 is connected. On the kit, the paired jumpers are named “Mxx” for the removable ones and “Jxx” for the soldered connectors.
2. Check that every gold colored jumper (see Figure 4 below) is connected. If one jumper is missing, it is possible to replace it with jumper M2 (redundant with M15 for GND connection)
3. Connect the kit to the KNX bus though the male connector J13. A female connector is supplied with the kit
4. Check that LED D13 (3V3) lights on
5. Connect your PC to the USB connector J31
6. Follow the instructions in the Quick Start Guide UM2409 available on www.st.com
7. If you disconnect the USB cable from the kit, please remove the golden jumper M37 (NRST).

Figure 4. Gold colored jumper

3 EVALKITSTKNX hardware description

The description below relates to the electrical schematic and hardware layout of the EVALKITSTKNX available on www.st.com .

Note: *Note: On the kit, the paired jumpers are named “Mxx” for the removable ones and “Jxx” for the soldered connectors.*

3.1 Power consumption characteristics

The typical current consumption characteristics of the EVALKITSTKNX measured in multiple configurations are shown in the following table.

Every test has been performed with V_{BUS} = 30 V, unless otherwise specified.

Table 1. EVALKITSTKNX power consumption figures

Symbol	Parameter	Conditions	Typ.	Unit
Idle I_{BUS}	Idle KNX bus power consumption	No transmission, no activity on bus STKNX voltage regulators enabled but not loaded	0.6	mA
Tx I_{BUS}	Transmit KNX bus power consumption	STKNX transmitting 0/1 toggled(1) STKNX voltage regulators enabled but not loaded	21	mA
Rx I_{BUS}	Receive KNX bus power consumption	STKNX receiving 0/0 toggled(2) STKNX voltage regulators enabled but not loaded	0.8	mA
Sys I_{BUS}	System KNX bus power consumption	CPU hosting typical firmware with Tapko demo protocol stack - no bus activity CPU section supplied by STKNX linear regulator (3.3V) (see Section 3.5.4.1 STKNX mode DC-DC 5 V (default)) - V_{BUS} = 30V	12.5	mA
Sys I_{BUS}	System KNX bus power consumption	CPU hosting typical firmware with Tapko demo protocol stack - no bus activity CPU section supplied by STKNX DC-DC converter (3.3V) (see Section 3.5.4.2 STKNX mode DC-DC 3V3) - V_{BUS} = 30V	2.6	mA
Sys I_{BUS}	System KNX bus power consumption	CPU hosting typical firmware with Tapko demo protocol stack - no bus activity CPU section supplied by STKNX DC-DC converter (3.3V) (see Section 3.5.4.2 STKNX mode DC-DC 3V3) - V_{BUS} = 20V	3.7	mA
ICPU	CPU section power consumption (3V3_KIT)	CPU hosting typical firmware with Tapko demo protocol stack - no bus activity	12	mA
IOPTO-IN	KNX_TX optocoupler input stage consumption	Optocoupler LED off (KNX_TX = 3.3V)	0	mA
IOPTO-IN	KNX_TX optocoupler input stage consumption	Optocoupler LED on (KNX_TX = 0V)	1.6	mA
IOPTO-IN	KNX_TX optocoupler input stage consumption	KNX_TX toggling 0/1(1)	1.3	mA
IOPTO-OUT	KNX_TX optocoupler output stage consumption	Optocoupler LED off (KNX_TX = 3.3V)	0.77	mA
IOPTO-OUT	KNX_TX optocoupler output stage consumption	Optocoupler LED on (KNX_TX = 0V)	0.79	mA
IOPTO-OUT	KNX_TX optocoupler output stage consumption	KNX_TX toggling 0/1(1)	0.78	mA
ISTLINK	STLINK/V2-1 section power consumption (USB_VCC)	PC connected to USB J31 connector	50	mA

(1) STKNX-TX signal is set high / 35 µs and Low / 173µs.

(2) Alternate (Drop-35 µs + Equalization-69 µs) / (Null-104 µs) analog signal is applied on VBUS.

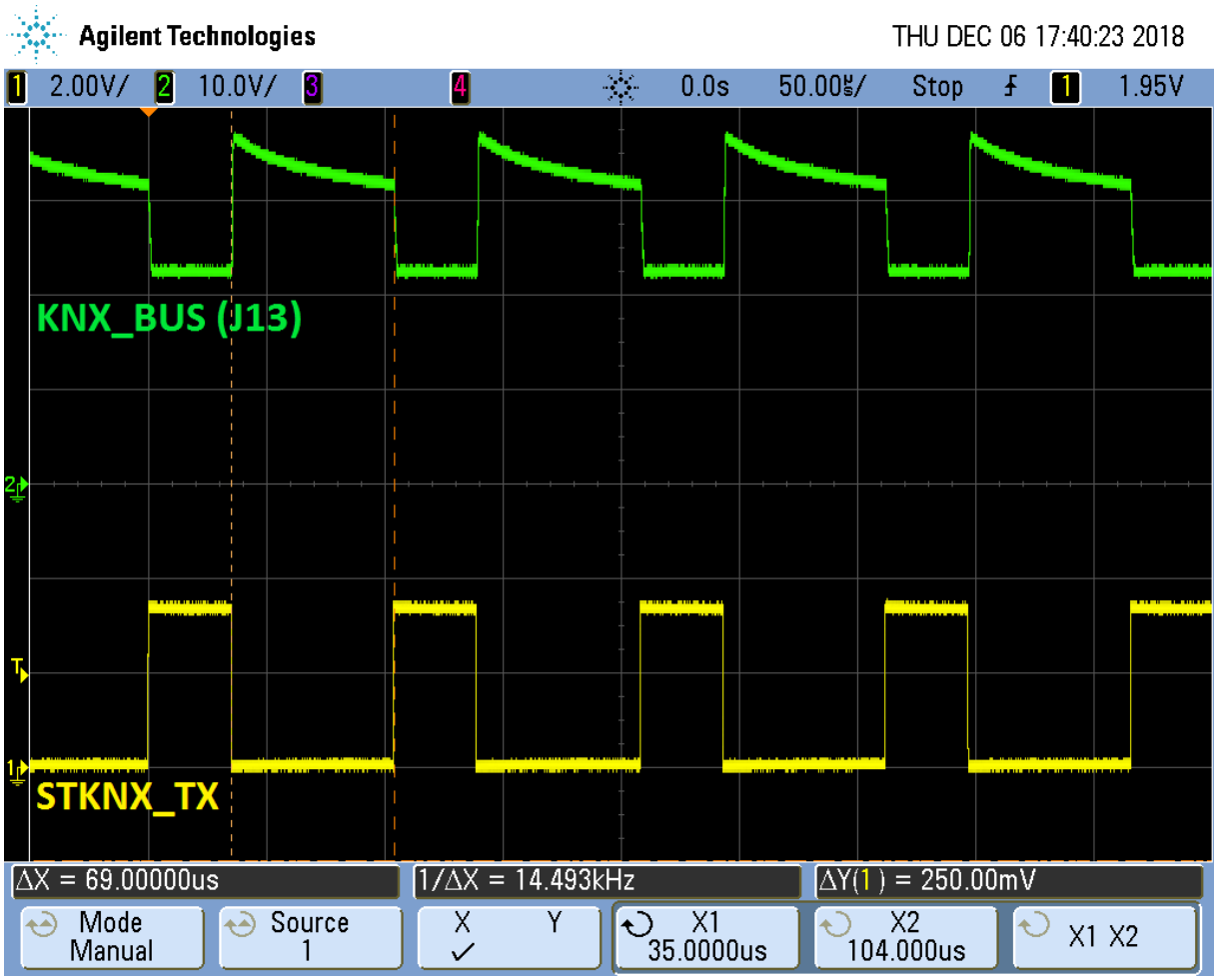
3.2 STKNX section

3.2.1 Electrical description

The STKNX circuit is assembled with every necessary discrete peripheral part in order to build the function of a KNX transceiver with a fan-in 30mA and a DC-DC converter with a 5 V output voltage.

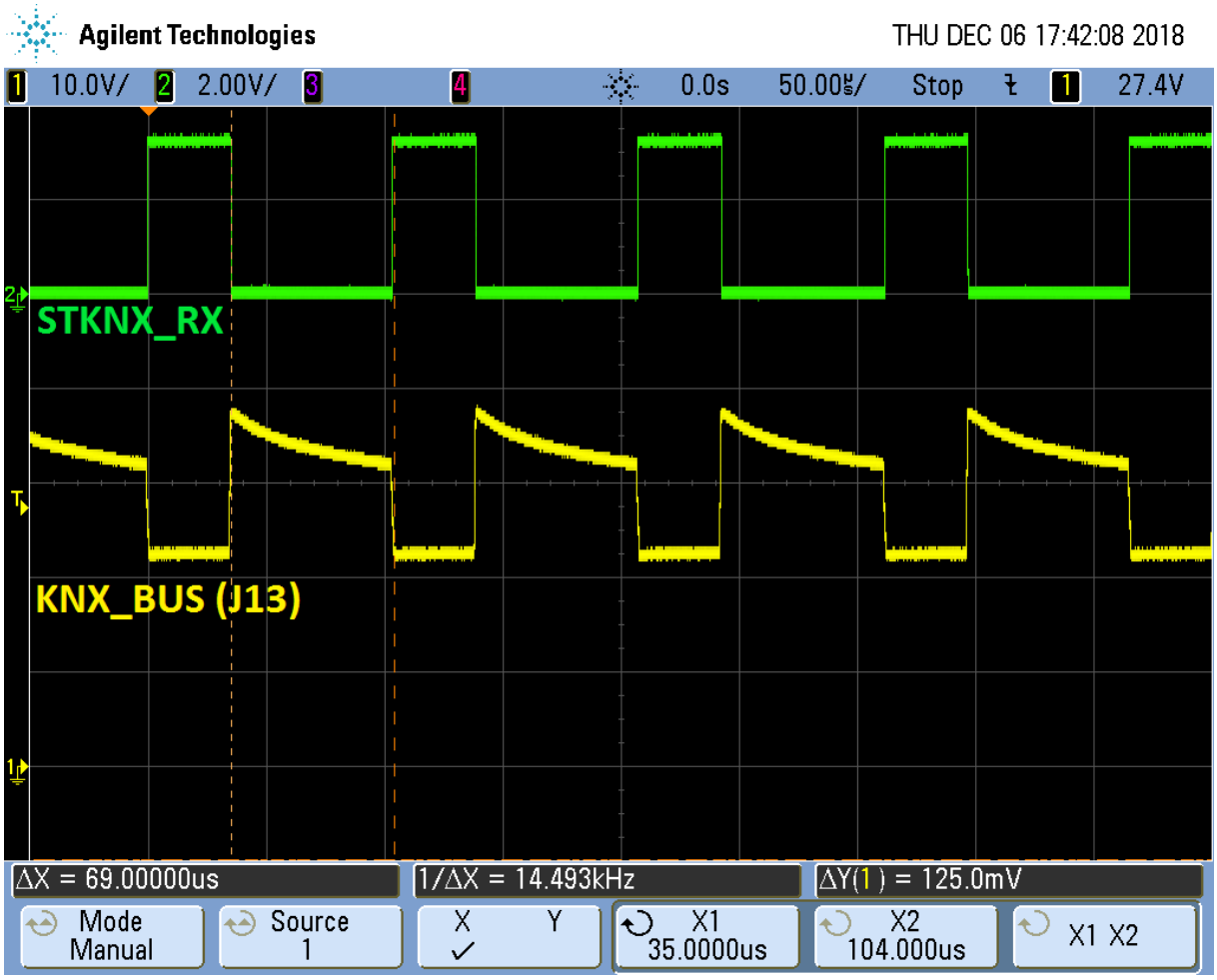
This section represents the interface between the analog signal on KNX bus connected to J13 and the digital signals KNX_TX, KNX_RX, KNX_OK and VCC_OK connected to the microcontroller U11 GPIOs (PA6, PA7), PA0, PC13, PB13, respectively.

Figure 5. KNX signals during transmission



break

Figure 6. **KNX signals during reception**



The discrete parts around STKNX have been selected according to the circuit datasheet recommendations, so the EVALKITSTKNX can be used as a reference for parts selection. It is also possible to use equivalent components with respect to the characteristics specified in the STKNX datasheet.

The capacitor Cgate requires specific attention:

Its capacitance directly determines the slope of the input current which is submitted to a specified limit in the test Section 4.4 Power Conversion (Load Changes) (8/2/2 - test 4.4).

- When selecting the capacitor in addition to voltage rating (≥ 10 V), the DC bias characteristic has to be checked in order to verify the capacitance change when the DC bias is tuned from approximately 2 V to 6 V. If the capacitance dropped excessively, input current slope would be higher than expected, because the effective capacitance would be significantly lower than the nominal one. Usually capacitance drop is higher in smaller case capacitors.
- Figure 7. Recommended DC bias characteristic for Cgate illustrates fairly constant DC bias characteristic, recommended for Cgate (fan-in = 30 mA), while Figure 8. Non-recommended DC bias characteristic for Cgate illustrates a DC bias characteristic with strong capacitance drop.

Figure 7. **Recommended DC bias characteristic for Cgate**

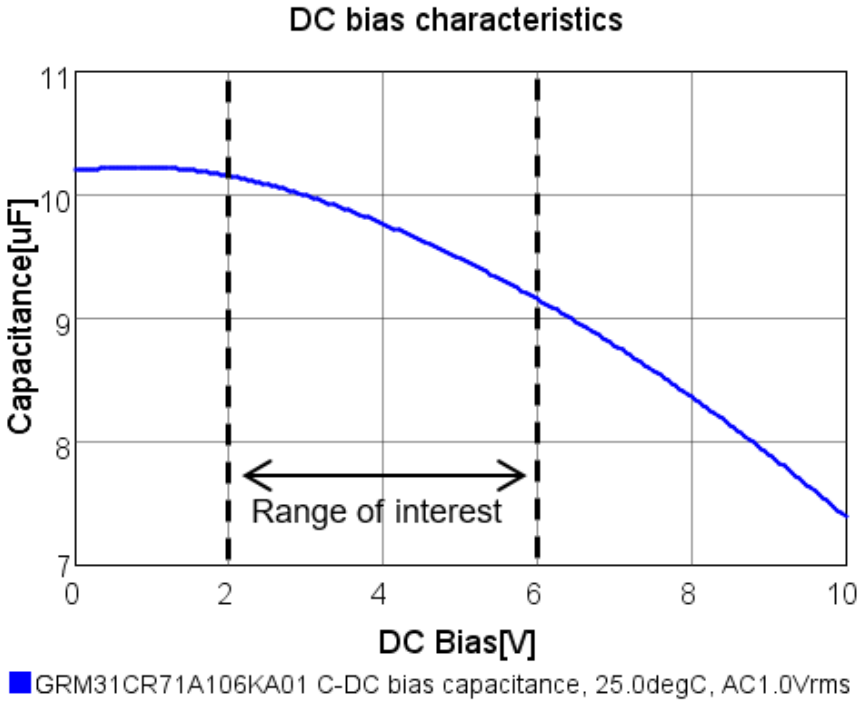
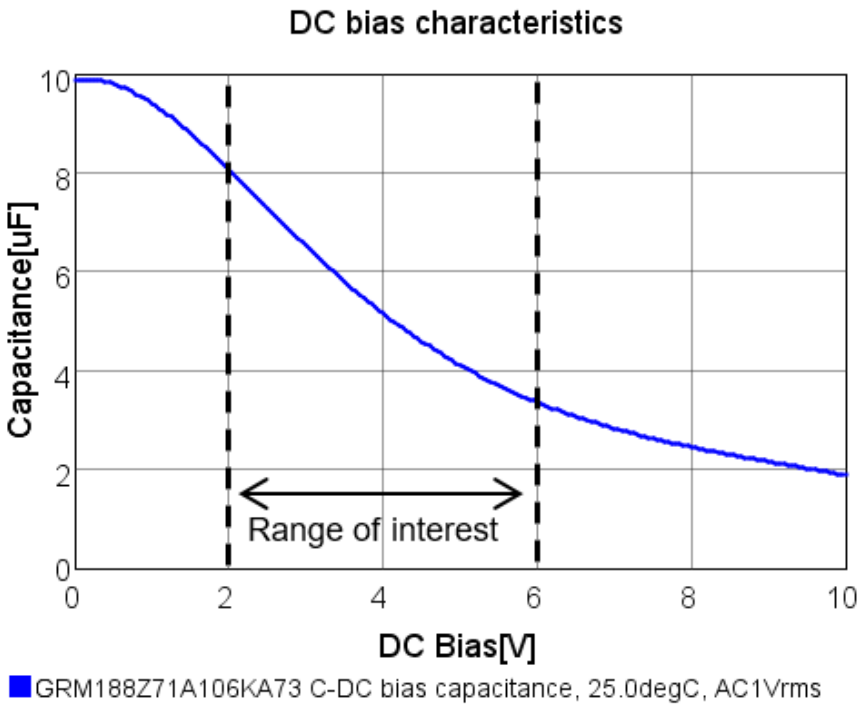


Figure 8. **Non-recommended DC bias characteristic for Cgate**



- Some optional components are also present on the schematic:

- C61 is present to avoid applying permanent voltage on pin KNX_TX as described in section “Transmitter” of the STKNX datasheet. Given the inductive impedance of KNX TP1 bus, forcing KNX_TX high for time duration longer than the one specified by the standard for active pulse (35 µs) can lead to excessive current drawn from the bus and should be avoided. Particular attention should be paid during firmware development in order to prevent conditions in which KNX_TX may be stuck high. C61 has been placed as a protection against such unexpected condition.
- R96-D16 pads are present to allow control of discharge and clamping of KNX_TX node at STKNX input because of C61 coupling capacitor. However, with default C61 value (1 nF) they are not necessary on EVALKITSTKNX design.
- R99-C62 are not populated. They offer a location for a filter to increase the ratio A1/A2 in the test 5.1-Pulse-Impedance. They have never been used on EVALKISTKNX.
- C7 is an option for an additional bulk capacitor on VDDHV rail. More bulk capacitor can store additional energy to supply the STKNX loads for a limited period of time after a loss of power of the bus (signaled by KNX_OK going low), allowing the CPU to run shutdown routines or similar tasks.

Thanks to jumpers J7, J8 and J9, it is possible to test several configurations for the STKNX:

- DC-DC converter status (J8):
  - ON, input voltage = VDDHV
  - OFF, input voltage = GND or not connected
- Linear regulator status and supply (J7)
  - ON, input voltage = VDDHV
  - ON, input voltage = VDCDC: refer to datasheet for minimum supply input voltage
  - OFF, input voltage = VCCCORE
- Linear regulator output voltage (J9)
  - Output voltage = 3.3V
  - Output voltage = 5V

See Figure 27. Jumpers in STKNX section for more information.

The DC-DC converter output voltage can be changed (from 1 V to 12 V) by modifying the feedback resistors and capacitor. In the electrical schematic, a selection guide indicates the values to be applied to generate voltages 1 V, 3.3 V, 7.5 V and 12 V. If a different voltage is needed, please refer to STKNX datasheet to calculate the discrete components values.

The EVALKITSTKNX is originally configured as a device with a fan-in parameter equal to 30 mA. It is also possible optimize it for lower fan-ins by modifying the capacitors Cgate and Cvddhv. The recommended parts for fan-in = 10 mA and fan-in = 20 mA are indicated in the schematic.

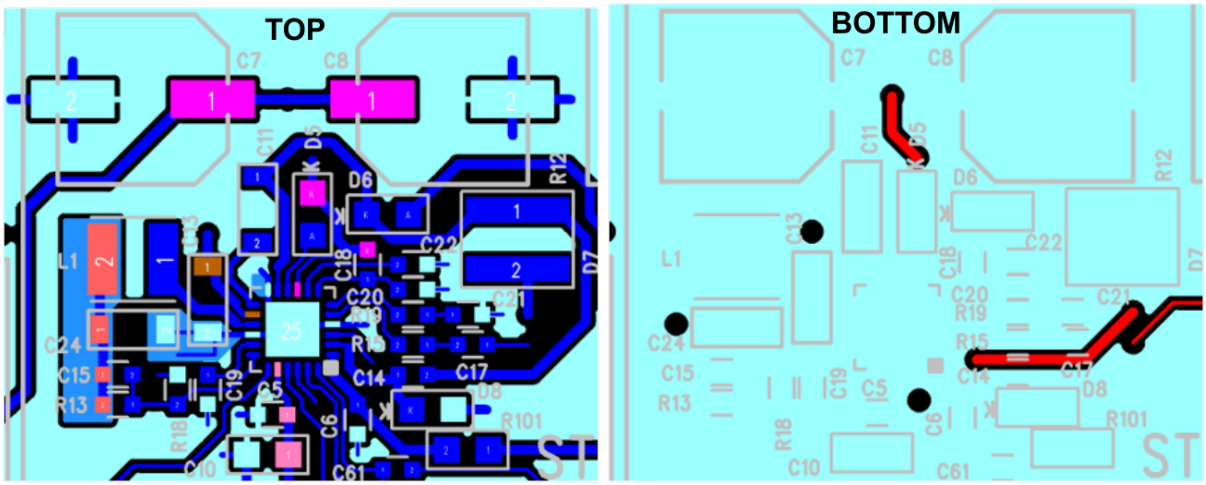
Regarding Cvddhv, a minimum value is recommended. That means, higher values for Cvddhv can be used, generally to improve the sustainability to KNX bus drops. However, attention must be paid to the peak current during the switch on test not to exceed the KNX limits.

3.2.2 Layout recommendations

PCB layout is an important part of DC-DC switching converter design. A poor board layout can compromise important parameters of the DC-DC converter such as efficiency, output voltage ripple, line and load regulation and stability.

Good layout for the STKNX can be implemented by following the few simple design rules listed in this section. These rules have been applied to the STKNX routed area on the STKNX evaluation board (EVALKITSTKNX), where only the TOP and BOTTOM layers have been used from the four available, so it can be transposed on a low cost 2-layer PCB. It is then easy to implement the rules on a final KNX product.

Figure 9. **STKNX area routed using top and bottom layers only**



Refer to Figure 10 and Figure 11 below for the recommendations described below:

- Place CIN (C13) close to the STKNX and connect it between pins VIN and DCDC_GND directly on top layer (DCDC_LX trace crosses between CIN pads)
- Connect COUT (C24) to DCDC_GND directly on top layer
- Keep the following power loops short:
  - CIN → DCDC_IN → DCDC_LX → L1 → COUT → CIN (green)
  - COUT → DCDC_GND → DCDC_LX → L1 → COUT (red)
  - CIN → DCDC_IN → DCDC_GND → CIN (purple)
- Use properly sized traces or shapes for power paths (DCDC_IN, DCDC_GND, VDCDC, LX)
  - Keep FB/Feedback and SS/Soft-Start components (Rfbx, Cfb1, Css) away from switching / noisy node (DCDC_LX), shielding with quiet nets (DCDC_GND in the image) is recommended (black)
  - Connect DCDC_GND pin (16) and KNX_B pins (4 and 12) to the exposed pad shape below the IC, as shown in Figure 11, to ensure ground consistency
  - Place several GND vias on STKNX package exposed pad (x9 in EVALKITSTKNX).

Figure 10. **Layout recommendations description**

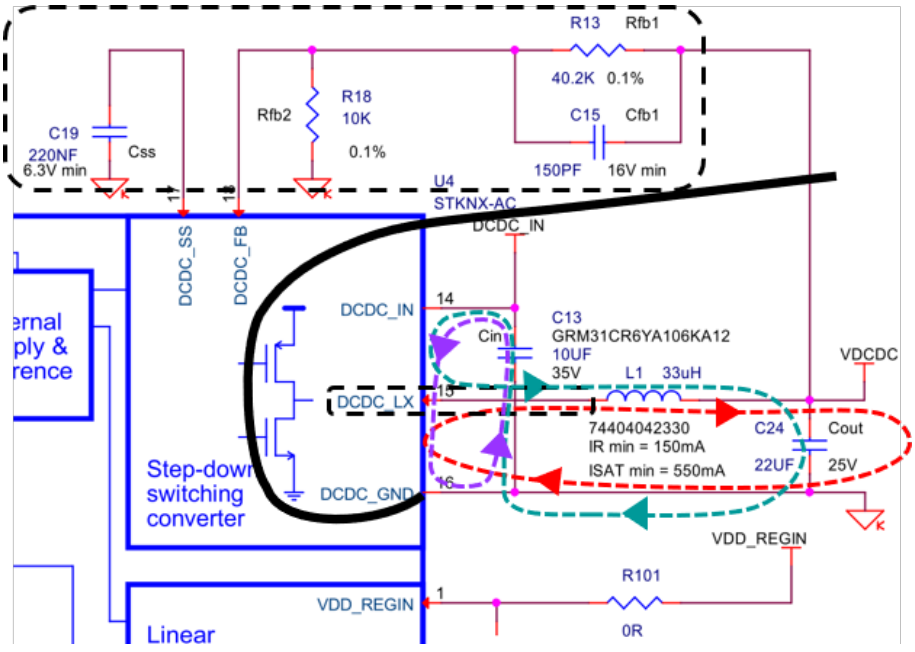
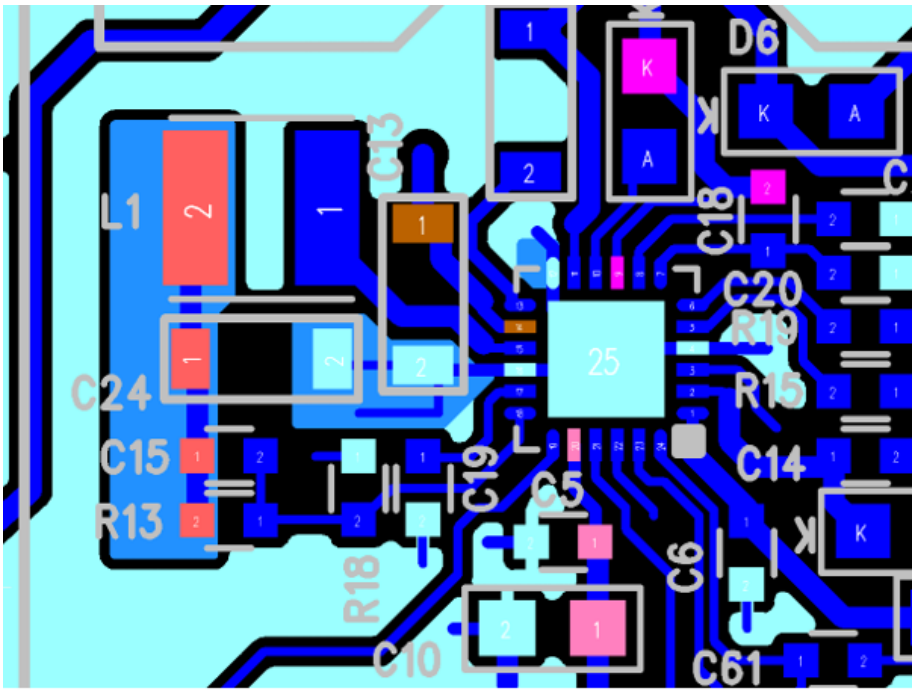


Figure 11. **Layout recommendations application**



RELATED LINKS

The source files of the PCB layout are available for download from the EVALKITSTKNX product page on the ST website

3.3 CPU section

The STM32F103RBT6 microcontroller has been selected as it is compatible with the free demo version of the Tapko KNX protocol stack “KAIstack”. Along with the minimum peripheral components, the crystal (Y1), KNX programming LED, button (D9, S5) and optional AND gate (U12), it forms the complementary circuitry to the STKNX section to create the basic KNX transceiver function.

Optional components EEPROM memory and 32.768kHz crystal are present to extend the feature possibilities for a custom development.

Button S6 is used to reset the CPU after a firmware download.

RELATED LINKS

See the TAPKO Technologies GmbH website

3.3.1 KNX_TX signal generation

The KNX transmit signal KNX_TX can be generated in two different ways linked to the embedded firmware: with or without an AND gate.

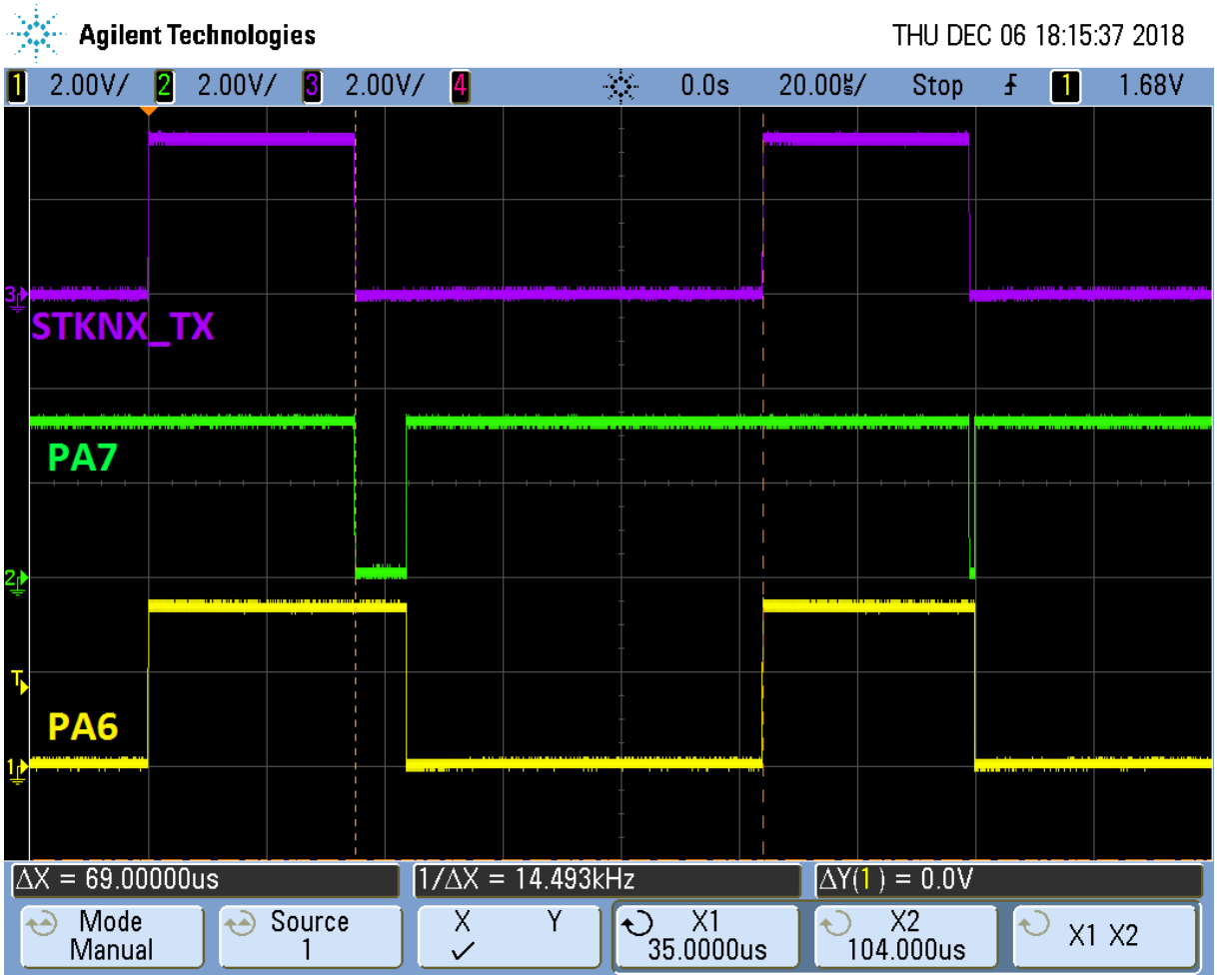
3.3.1.1 KNX_TX generated from AND gate

The firmware STSW-KITSTKNX version 1.0.0 available at www.st.com requires the use of the AND gate U12 to generate the KNX transmit signal.

The two GPIOs, PA6 and PA7 are used and combined in the AND gate U12 to generate the waveform of the KNX digital signal to transmit a logic level “0”. The GPIOs have been selected because they are multiplexed with the Timer TIM3 function of the STM32F103RBT6. The three channels CH1, CH2 and CH3 of the Timer TIM3 are necessary to manage internally the KNX transmit signal generation.

The following figure illustrates the generation of the KNX_TX signal.

Figure 12. **Transmit signal generation**

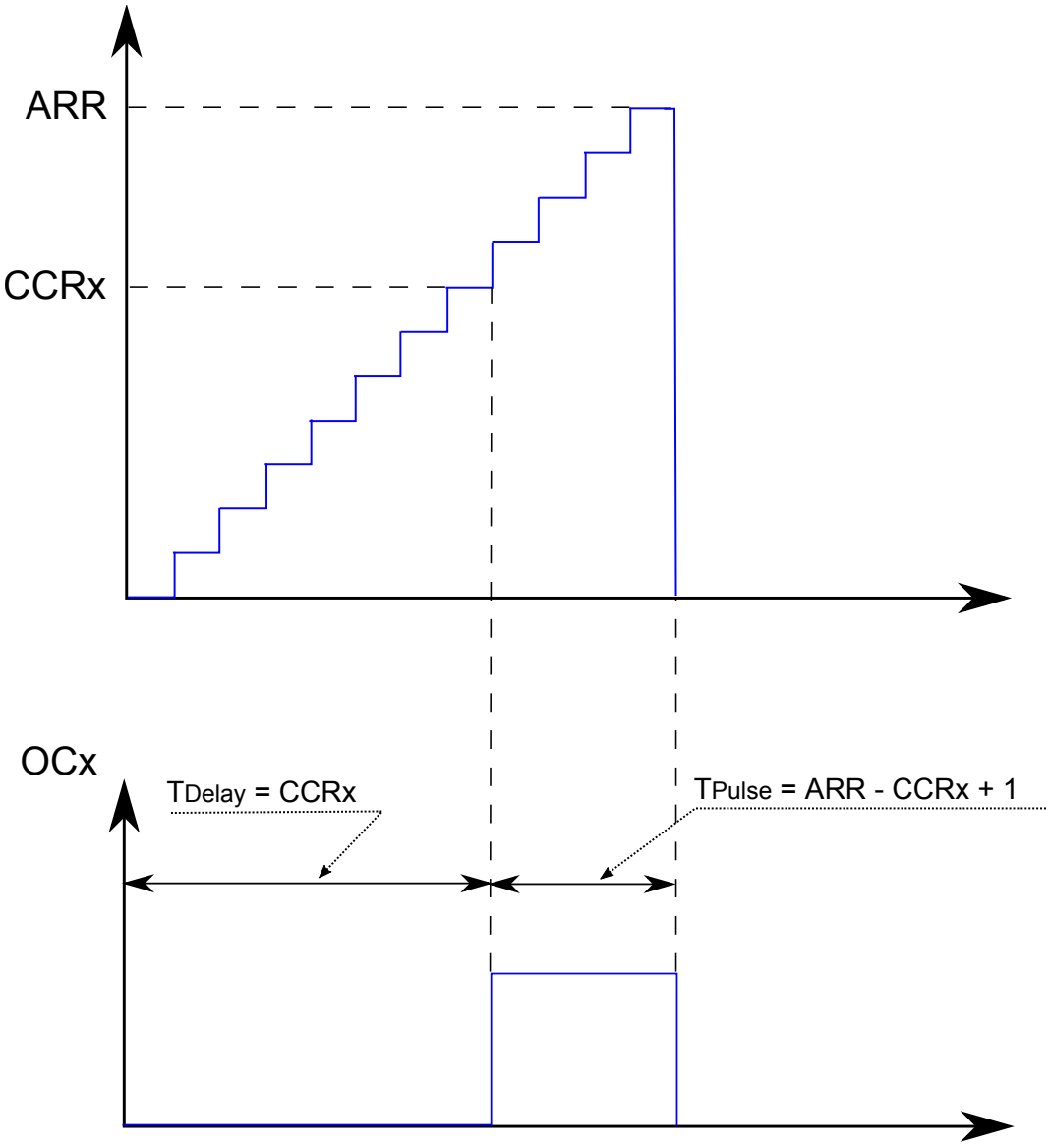


3.3.1.2 *KNX_TX generated from one single GPIO (no AND gate)*

STM32 MCU provides a feature called “one-pulse mode” (OPM) that can be used to generate the STKNX Tx signal without need for the AND gate U12.

The one-pulse mode (OPM) can be used together with the timer channels configured in output mode. It allows the timer to generate a pulse of a programmable width after a programmable delay on the timer channels configured in PWM1 or PWM2 output compare modes.

Figure 13. **One pulse mode**



Note: *Warning: In case the OPM is used to generate the Tx signal on pin PA6, don't forget to set PA7 to 1 if the AND gate is still present (case of EVALKITSTKNX)*

RELTABLE: FInd more information on one-pulse-mode in Application note AN4776: “General-purpose timer cookbook”

3.3.2 Crystals oscillators

The load capacitor values of the 16 MHz and 32.768 kHz CPU oscillators have been adjusted on the EVALKITSTKNX PCB by measuring the oscillators’ frequency drift across the -40°C/+85°C temperature range, and centering the frequency to the nominal value for T = 25°C.

Figure 14. 16MHz oscillator response and Figure 15. 32.768kHz oscillator response below display the frequency drift of the 16 MHz and 32.768 kHz oscillators, respectively, with the following load capacitors values:

- C31 = C32 = 15 pF
- C37 = C38 = 8.2 pF

Figure 14. **16MHz oscillator response**

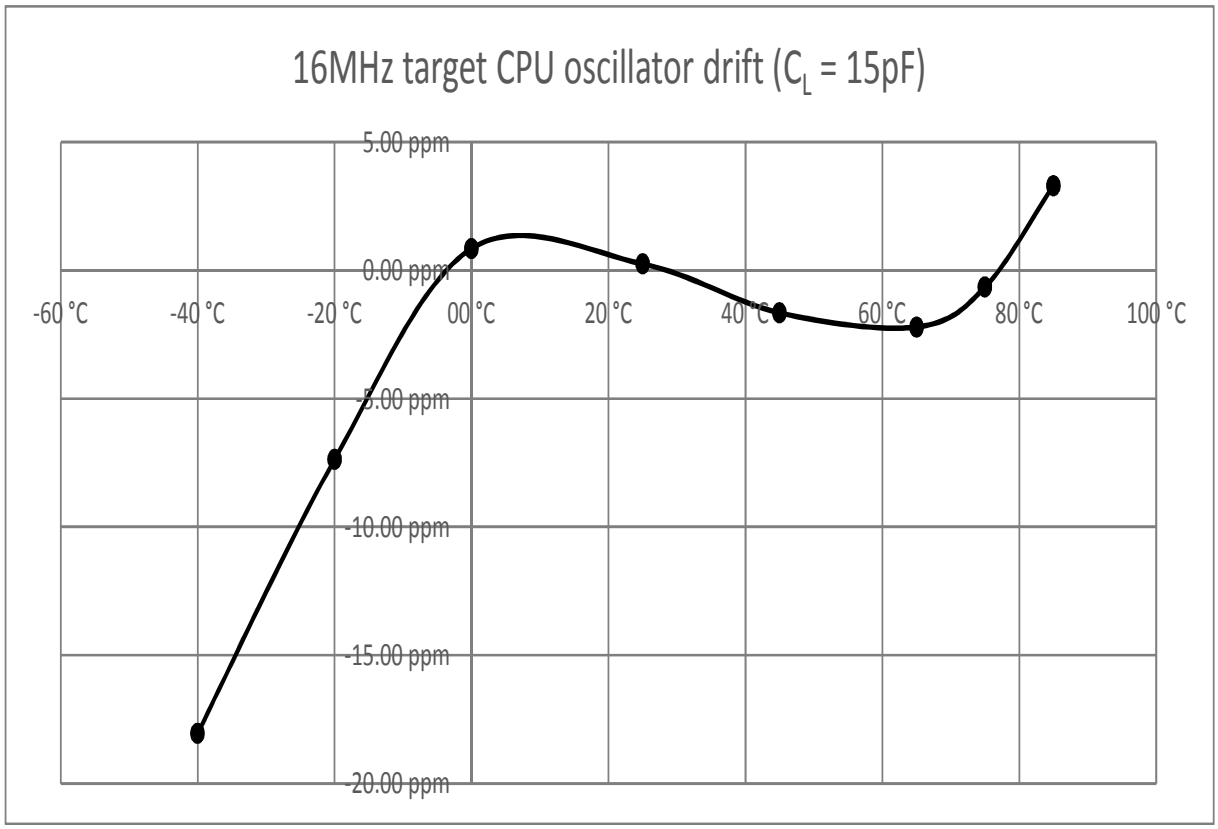
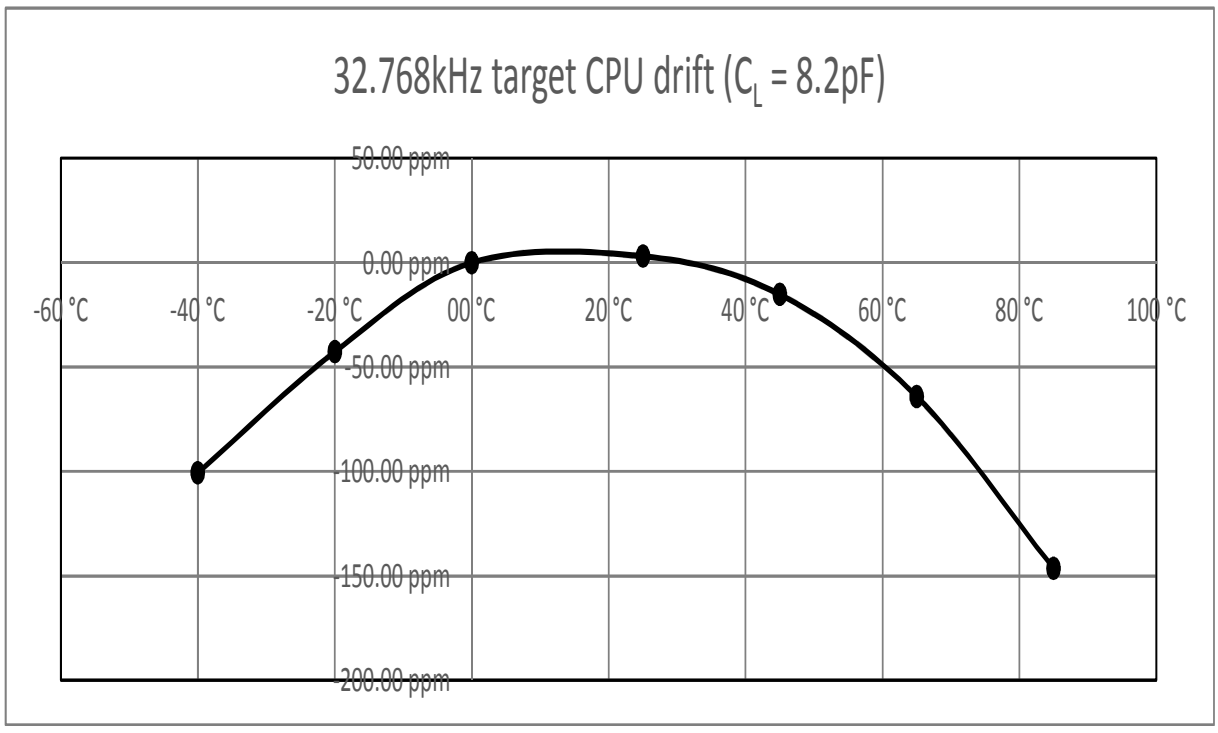


Figure 15. **32.768kHz oscillator response**



3.3.2.1 *Application and expansion section*

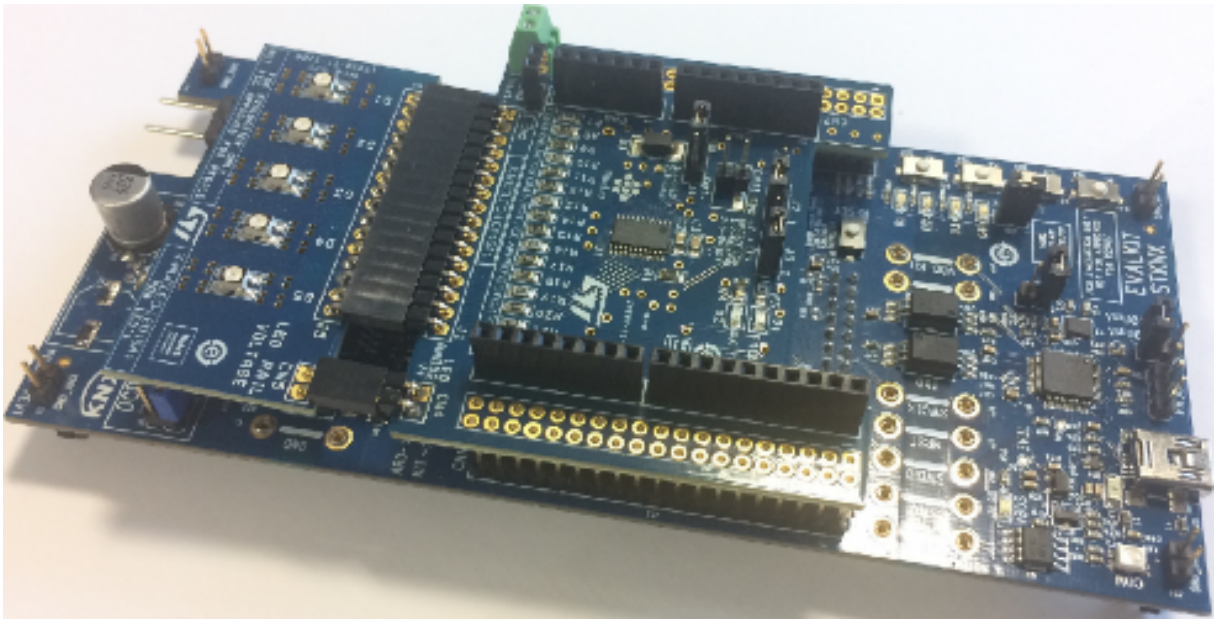
On the EVALKITSTKNX, buttons S1 to S4 and LEDs D1 to D4 are connected to CPU GPIOs to offer the user the possibility to emulate basic sensors and actuators, or some other purpose. The LEDs can be disabled by removing the jumper M29, and the associated GPIOs become free.

The extension connectors J21 to J26 are compatible with the ArduinoTM and ST morpho standard. They allow the user to connect an existing or custom daughterboard for specific application development, as illustrated in Figure 16. X-NUCLEO-LEDA1 board plugged on EVALKITSTKNX below.

Indeed, one application example has been internally developed by STMicroelectronics with the ST X-NUCLEO-LEDA1 daughterboard in order to realize a KNX LED dimming KNX actuator. See Section 3.5.4.4 Dimming mode (application example) for more information.

Note that some 0 Ω resistors are present to avoid conflict between KNX signals and Arduino/Morpho reserved signals.

Figure 16. X-NUCLEO-LEDA1 board plugged on EVALKITSTKNX



3.4 Isolation section

Optional optocouplers U2, U3, U5 and U8 are present on the kit to ensure a galvanic isolation between the STKNX section and the rest of the system, which is necessary in the development of a Remote Powered Device (RPD).

Two optocouplers are also permanently placed between the STLINK CPU and the target microcontroller USART in order to isolate the user PC if the USART only(b) is used. They follow the same rules as described below for the STKNX isolators. Also, jumpers M33 and M35 to M40 are removed to guarantee the PC isolation.

Note: Be careful, the PC cannot be isolated during debug

3.4.1 STKNX optocouplers enabling

Note that the optocouplers in the STKNX section are originally disconnected, unpowered and shorted with golden jumpers. To activate them, it is necessary to:

- remove the x9 golden jumpers
- solder the power resistors R1 and R5
- solder the serial resistors R3, R6, R8, R9, R14, R16, R20, R21.

It is then not possible to use the STKNX voltage regulators to supply the system. The recommended setting for STKNX regulators is:

- DC-DC converter disabled: M8 = J8:3-4
- Linear regulator voltage = 3.3 V: M9 = J9:1-2 (to supply STKNX internal digital I/Os and optocouplers)

- Linear regulator input = VDDHV: M7 = J7:1-2.

3.4.2 STKNX optocoupler connections

The Avago optocouplers ACPL-W61L-000E have been selected for their low forward LED current. We notice they are working in negative logic: that means, when the input diode is activated with a direct current I_F, the optocoupler output voltage Vo is set Low.

For this reason, the AND gate (U12) output signal KNX_TX is connected to the cathode of the optocoupler LED in order to realize a non-inverter function with the STKNX_TX input signal of the STKNX circuit.

The signals STKNX_RX, STKNX_OK and VCC_OK driven by STKNX are managed differently:

- A logic inverter is used to drive the LED because direct LED driving would require excessive current to the STKNX digital outputs
- For the STKNX_RX signal, the inverter is connected to the anode of the LED in order to restore the correct polarity signal at CPU input (KNX_RX)
- For the VCC_OK and KNX_OK signals, the inverter is connected to the cathode of the LED in order to guarantee consistent signal status when the bus in not powered
  - When there is no power on KNX bus, the two signals VCC_OK and KNX_OK must be set low at CPU input. In this situation, since the optocoupler LED is off (V_ISO_KNX = 0, STKNX section supply missing), the optocouler output is high. Thus, an additional inverter needs to be inserted at optocoupler output, to restore correct polarity at CPU input
  - Due to this second inverter inserted in VCC_OK and KNX_OK chains, it is necessary to control the optocoupler diode from its cathode to ensure a non-inverting function from STKNX outputs to CPU inputs.

3.4.3 Optocoupler LED current

An external resistor Rs is placed serially with the optocoupler LED, computed to a maximum value in order to limit the power consumption.

For calculations, we have to consider the worst cases about the available voltages to supply the LED.

- The minimum power supply voltage which can be applied is V_ISO_KNX = 3V, i.e. $VCCCORE_{min}$ value extracted from STKNX datasheet. (the accuracy of U15 supplying V_ISO_KIT is tighter)
- The maximum voltage loss on the logic level applied: the worst case is VOH = 2.48 V (for I_{OH} = 4 mA) in AND gate U12 datasheet, meaning a voltage loss U_L = 0.52 V (the inverters U1-like have better performances).

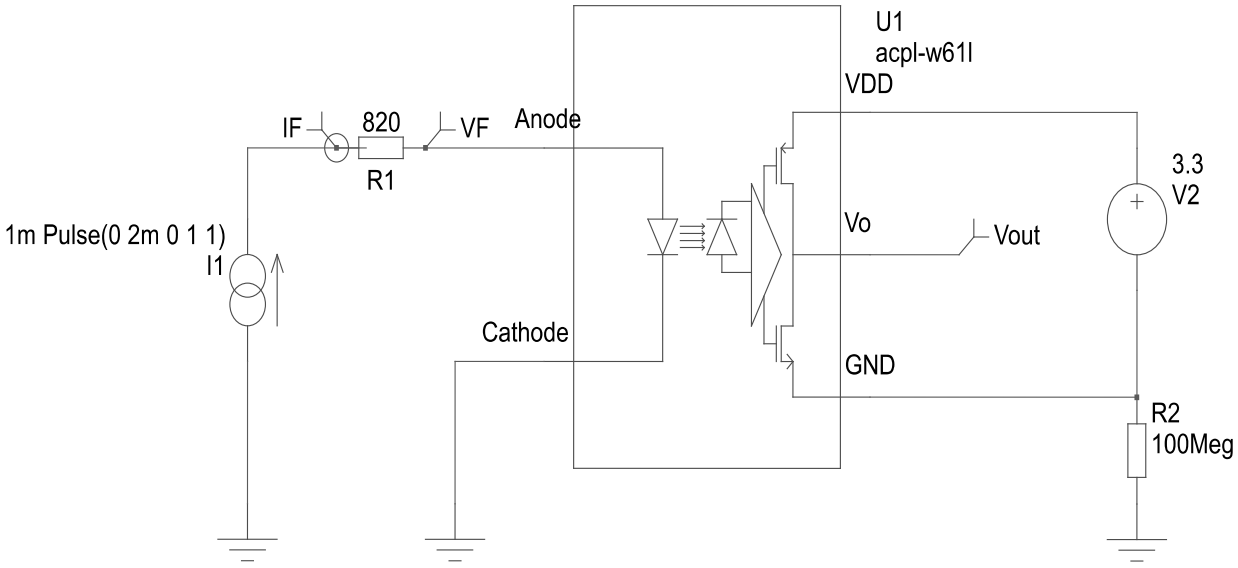
The value of the LED serial resistor Rs can be calculated by:

$$R_S = \frac{VCCORE_{min} - U_L - V_{Fmax}}{I_{Fmin}} \quad (1)$$

where V_F is the forward voltage and I_F the forward current of the optocoupler LED.

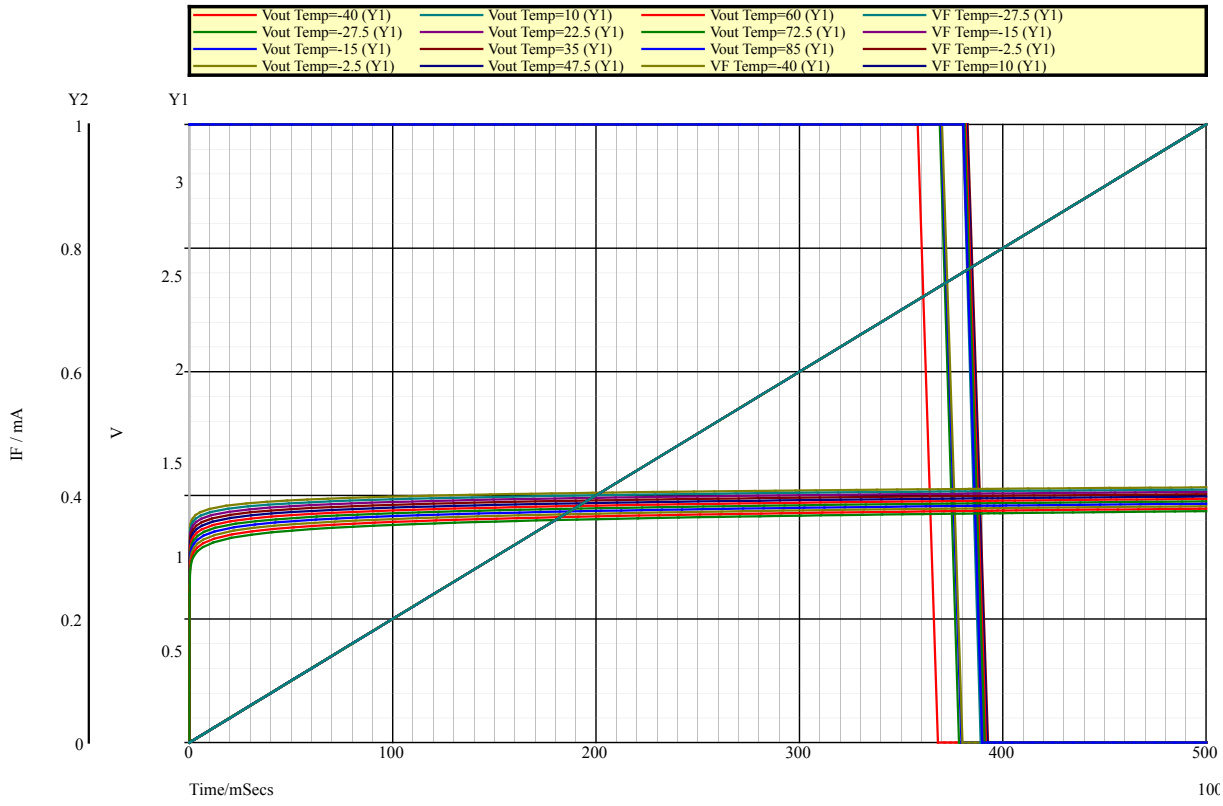
To determine V_{Fmax} and I_{Fmin}, a simulation has been carried on with the optocoupler model since those two parameters are linked together: indeed, when V_F is maximum, I_F is not minimum, so the parameters given in the datasheet do not allow determining the optimum value for R_S.

Figure 17. **Optocoupler simulation diagram**



The simulation has been executed from -40°C to +85°C (step 12.5°C). The result in Figure 18. Simulation results: -40°C to +85°C below shows that the maximum I_F current needed to activate the optocoupler output occurs at T = 35°C.

Figure 18. **Simulation results: -40°C to +85°C**

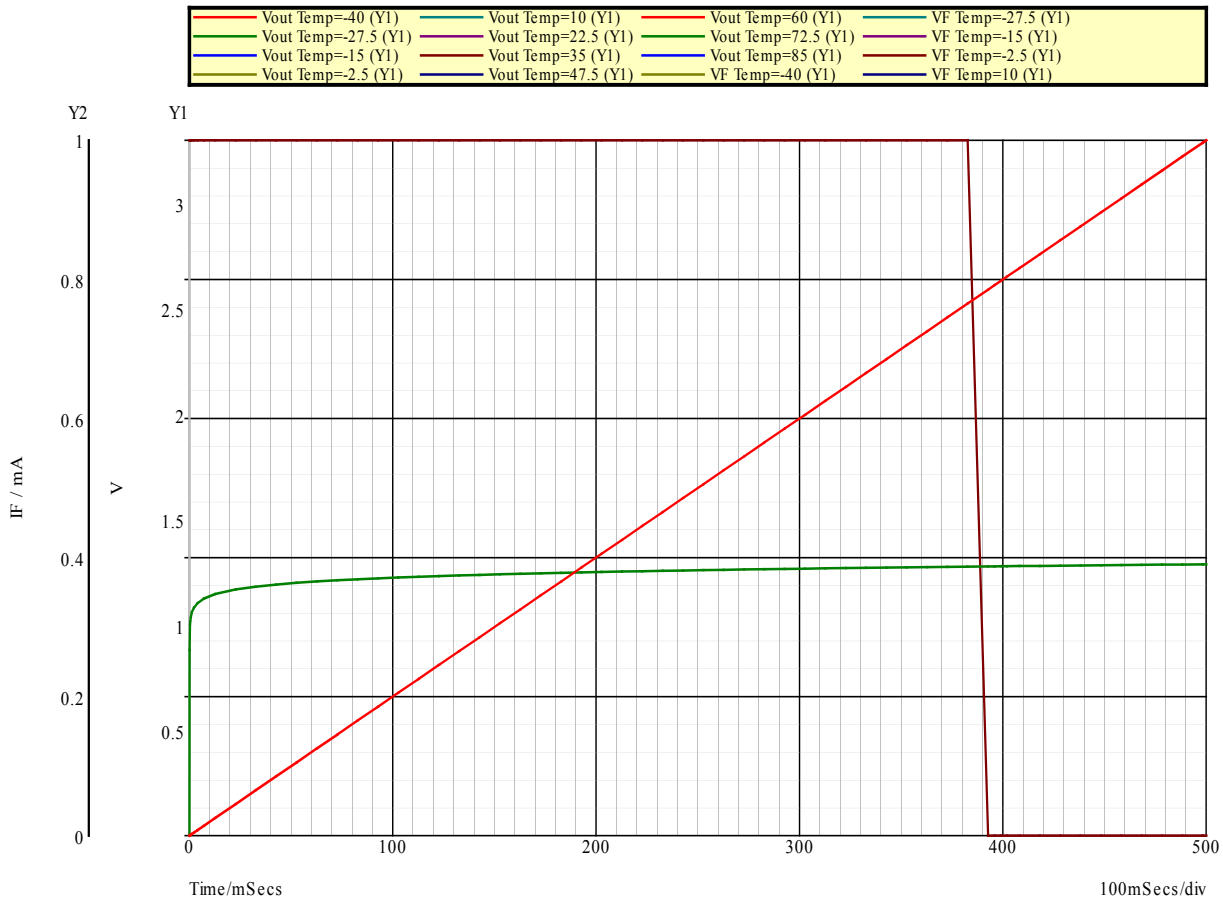


In Figure 19. Simulation results for T = 35°C below (simulation @ T = 35°C extracted), we can read that:

- I_F min = 0.78 mA
- V_F min = 1.28 V

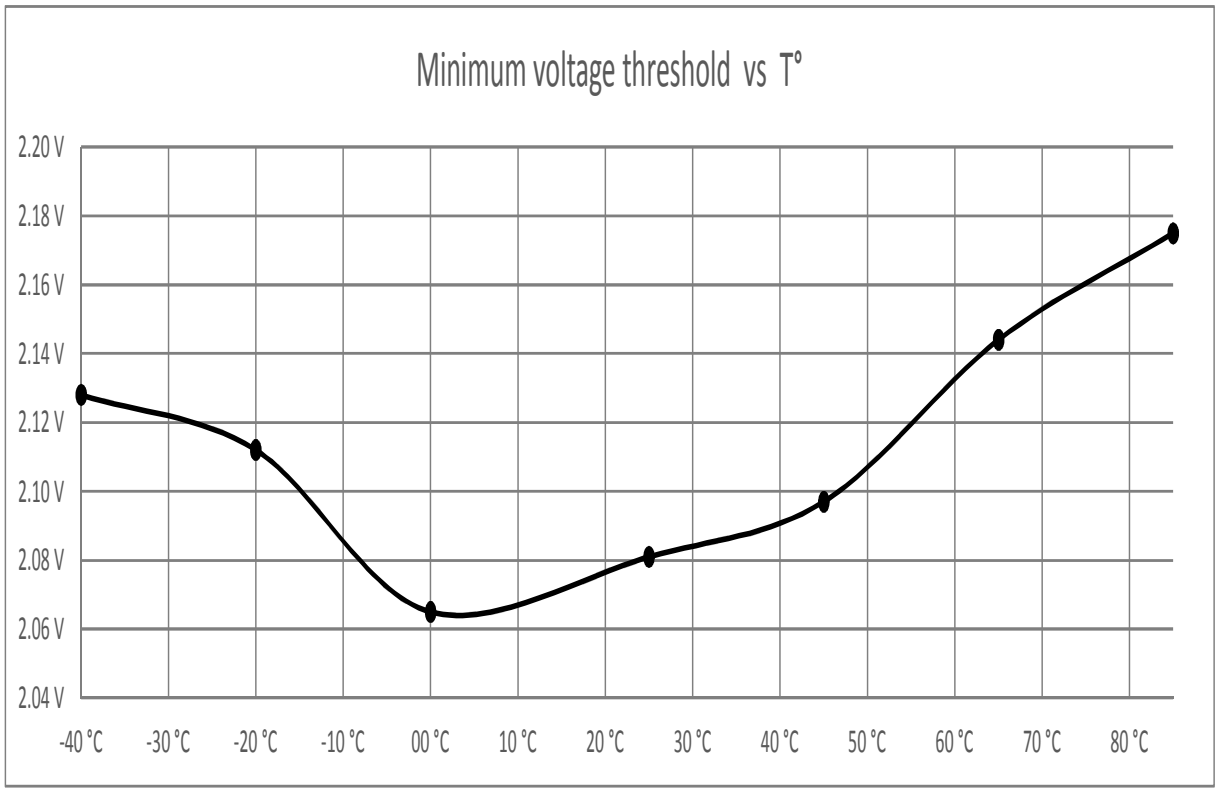
According to Eq. (1), we calculate R_S = 1.53 kΩ. So, in EVALKITSTKNX, the serial resistor has been fixed to 1.2 kΩ (taking into account the resistor's tolerance).

Figure 19. Simulation results for T = 35°C



Once R_S is fixed to 1.2 kΩ, the minimum voltage to be applied across the resistor and the optocoupler input has been measured on one board over the full temperature range (diode controlled from anode). The results in Figure 20. Optocoupler threshold current show that the maximum necessary voltage is < 2.18 V, which is compatible with the minimum available voltage applied: $VCCCORE_{min}$ - U_L = 3 V - 0.52 V = 2.48 V (refer to Eq. (1)).

Figure 20. **Optocoupler threshold current**



3.4.4 Optocouplers propagation delay

The KNX System Conformance Testing specification chapter 8/2/2 allows a maximum value (1 µs worst case) for the propagation delay of the transmitted and received signals through the KNX transceiver (i.e. STKNX).

Since this delay measurement is done between the microcontroller I/Os and the KNX bus, the propagation delay of the optocoupler is included and remains negligible compared to the 1 µs maximum value specified.

As shown in the figures below from Figure 21. Optocoupler delay - rising edge - cathode controlled to Figure 24. Optocoupler delay - falling edge - anode controlled, the maximum propagation delay through the optocouplers 63 ns, with R_S = 1.2 kΩ meets the requirement.

Figure 21. **Optocoupler delay - rising edge - cathode controlled**

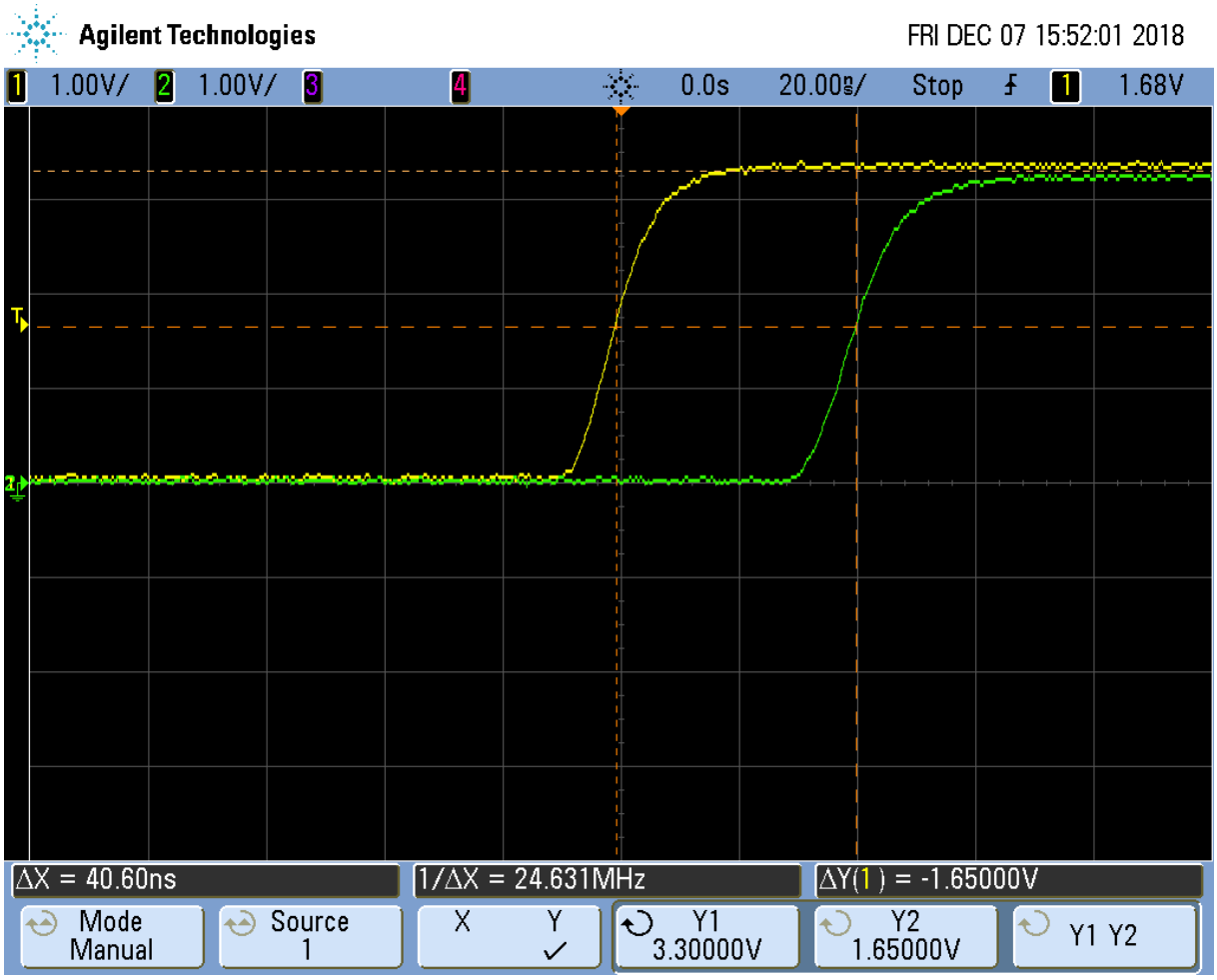


Figure 22. **Optocoupler delay - falling edge - cathode controlled**

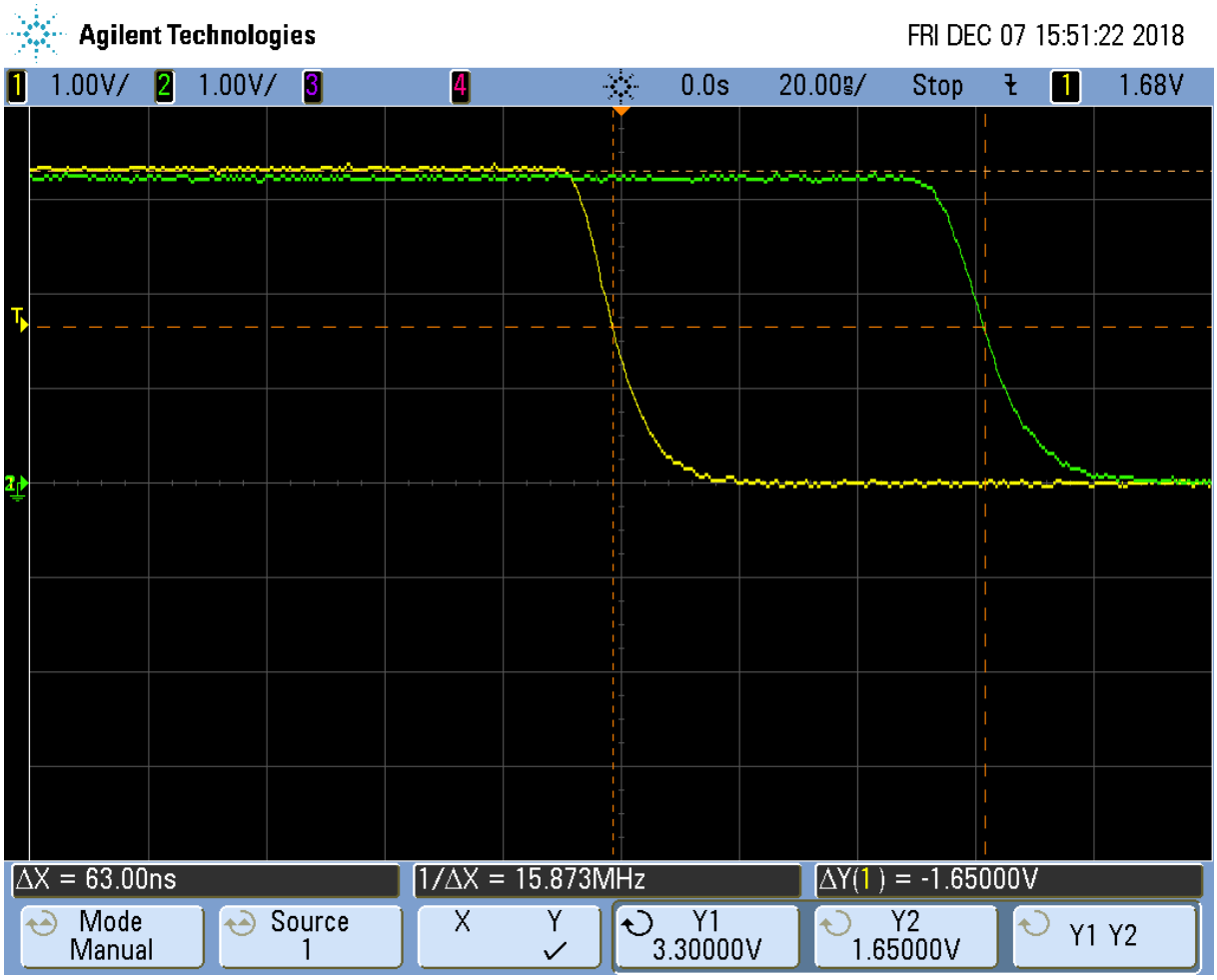


Figure 23. **Optocoupler delay - rising edge - anode controlled**

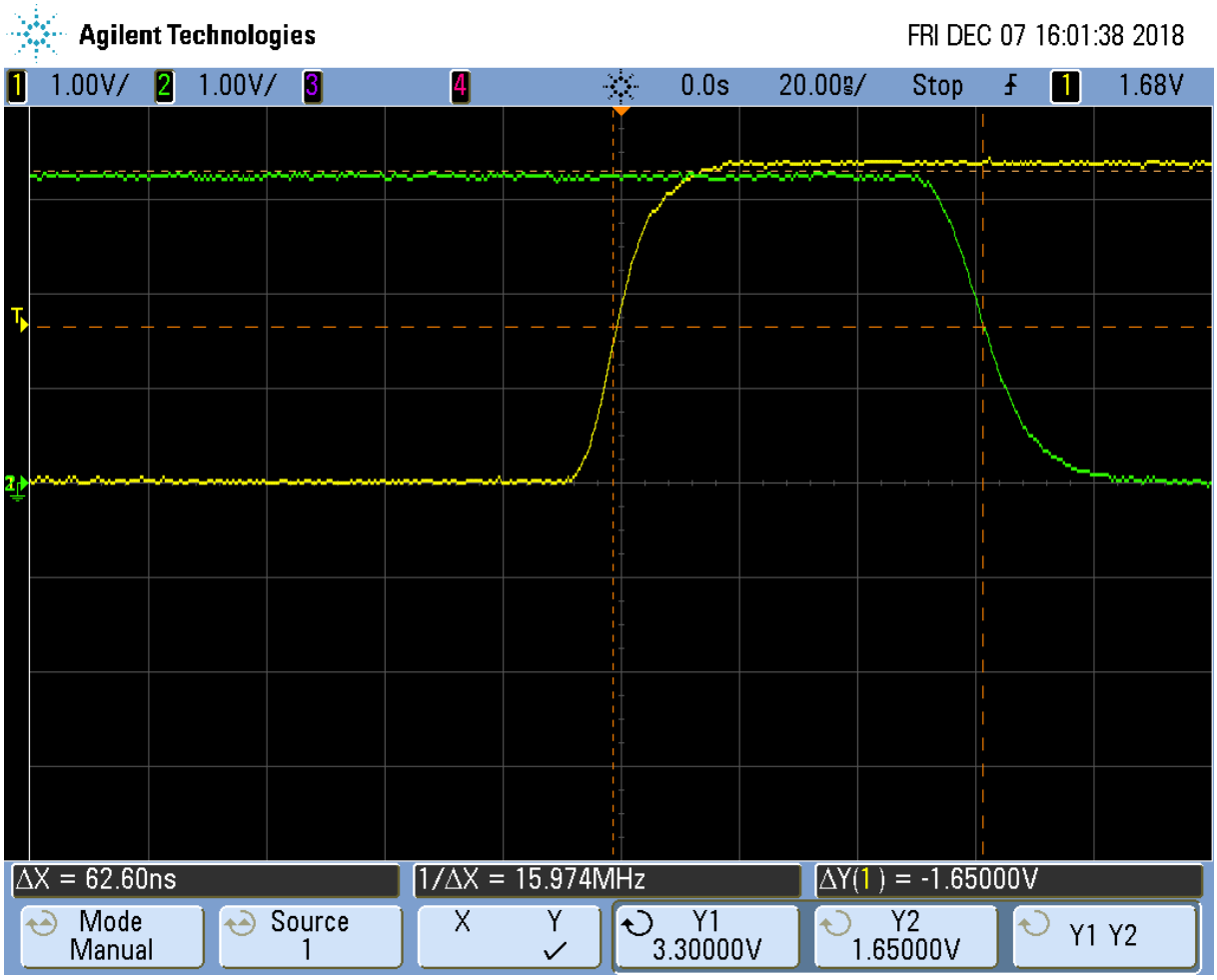
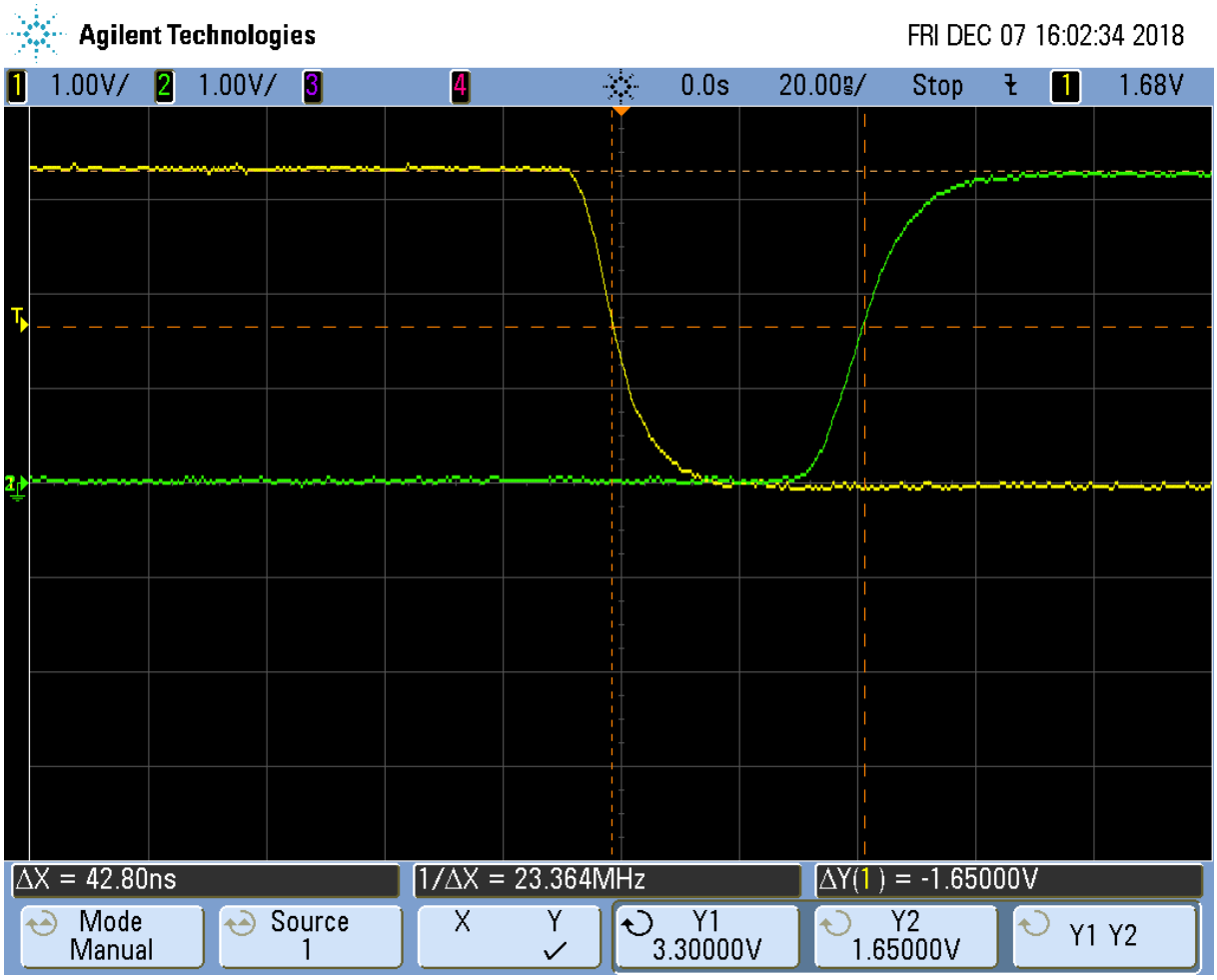


Figure 24. **Optocoupler delay - falling edge - anode controlled**



Measurements have been performed in the following sections to verify that the EVALKITSTKNX remains compatible with chapter 8/2/2 test specifications when optocouplers are enabled:

- Section 4.13.2.1 Signals waveforms for fan-in 10mA kit - not isolated,
- Section 4.13.2.4 Signals waveforms for fan-in 30mA kit - isolated,
- Section 4.14.2.2 Signals waveforms for fan-in 10mA kit - isolated,
- Section 4.14.2.4 Signals waveforms for fan-in 30 mA kit - isolated

3.5 EVALKITSTKNX power supply configuration

The EVALKITSTKNX can be powered in several alternative ways. You can supply the kit exclusively via USB connector (for SW development), exclusively via KNX bus (to demonstrate all the STKNX power capabilities), or partially from the expansion board.

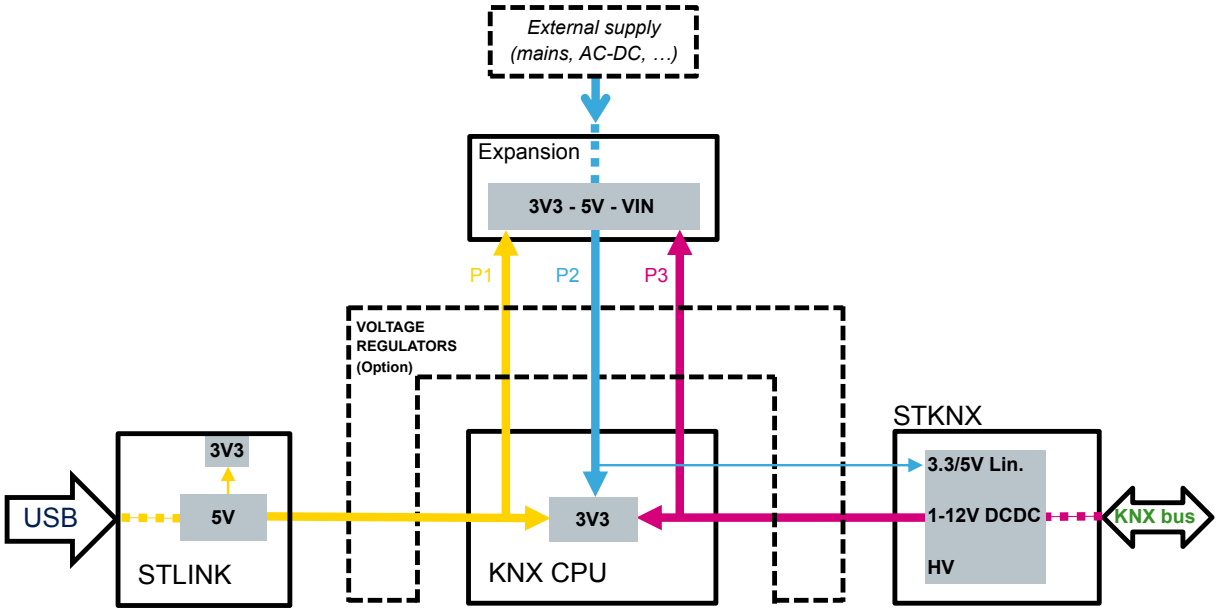
The modular design lets you perform all the necessary tests before building your own prototype.

The block diagram in Figure 25. EVALKITSTKNX block diagram with power supply routes shows the STKNX evaluation kit divided into five logical sections:

1. STKNX
2. KNX CPU
3. Expansion connectors
4. STLINK debug
5. Embedded regulators

These sections are able to transfer or receive (or both) power to and from the other sections.

Figure 25. EVALKITSTKNX block diagram with power supply routes



Regarding the power supply paths:

- Path P1 supplies the kit and any daughterboards through the USB connector, which is good for firmware editing and debugging. No supply is required (except KNX bus if bus communication is expected).
- Path P2 allows supplying the whole kit from the expansion board
- Path P3 supplies the entire kit through the STKNX device.

Note: *Note: When the USB cable is removed, you have to disconnect jumper M37 in order to release the target CPU reset pin.*

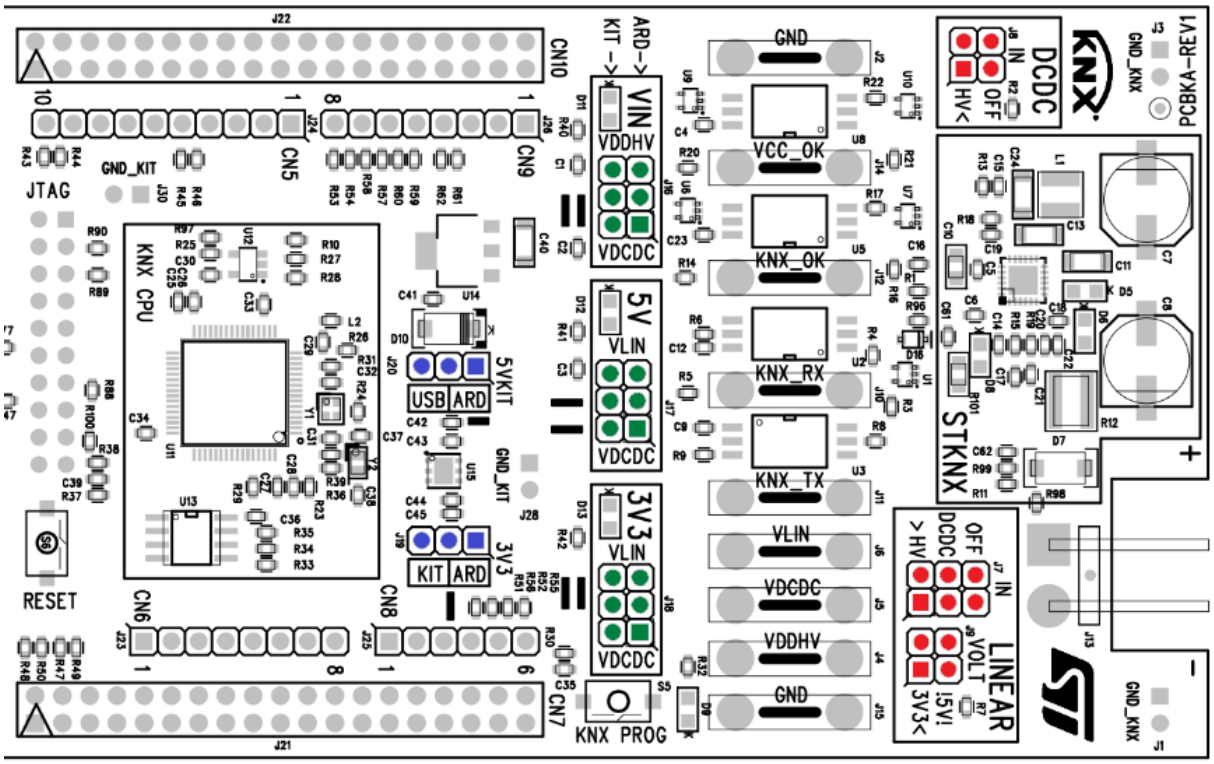
It is also possible to mix the three paths modes, thanks to two voltage regulators (5 V and 3.3 V) on the kit. However, when the CPU section is not supplied from STKNX, it is necessary to ensure that the CPU section is powered before the voltage on KNX bus is established, otherwise the two digital outputs KNX_OK and VCC_OK source abnormally the CPU section from digital connections.

You can configure and evaluate several power supply configurations through the jumpers on the kit.

Note: *The EVALKITSTKNX must be powered off before any modification of the jumper positions.*

The jumpers also offer an easy way to measure the power consumption of each kit section by connecting an ampere meter at the jumper position.

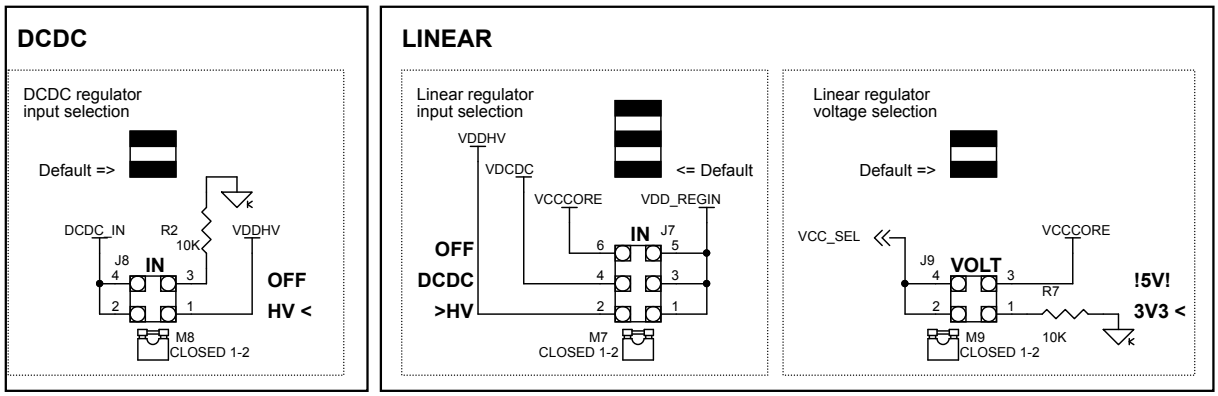
Figure 26. **Jumper locations for power supply routing and configuration**



3.5.1 Jumpers in STKNX section

Note: The paired jumpers are named Mxx for the removable ones and Jxx for the soldered connectors.

Figure 27. **Jumpers in STKNX section**



J8 lets you control the STKNX DC-DC switching converter (VDCDC):

- M8 pos 1-2: DC-DC enabled (default setting)
- M8 pos 3-4: DC-DC disabled

Note: DC-DC voltage can be configured through the external resistor divider on the DCDC_FB pin of the STKNX. See the STKNX datasheet for more information.

J7 lets you control the STKNX linear voltage regulator (VCCCORE):

- M7 pos 1-2: regulator fed by VDDHV (default setting)
- M7 pos 3-4: regulator fed by VDCDC

- M7 pos 5-6: regulator disabled: in this case, VCCCORE must be supplied externally and always AFTER VDDHV. So, VCCCORE should be supplied by some power supply derived from VDDHV or conditioned to VDDHV presence.

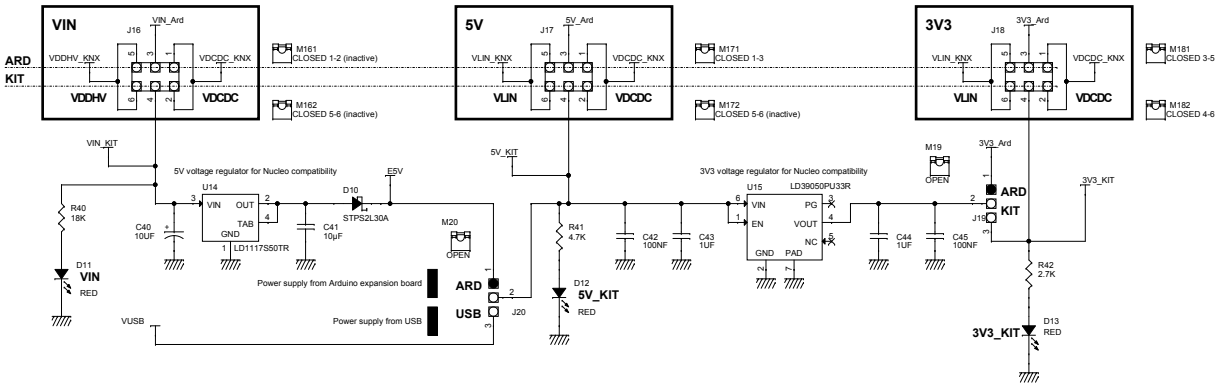
J9 allows to configure the voltage output of STKNX linear regulator (VCCCORE):

- M9 pos 1-2: VCCCORE = 3.3 V (default setting)
- M9 pos 3-4: VCCCORE = 5 V

Note: Be careful with 5 V output mode as it may damage the kit if 3.3 V components, like STM32, should mistakenly receive 5 V supply.

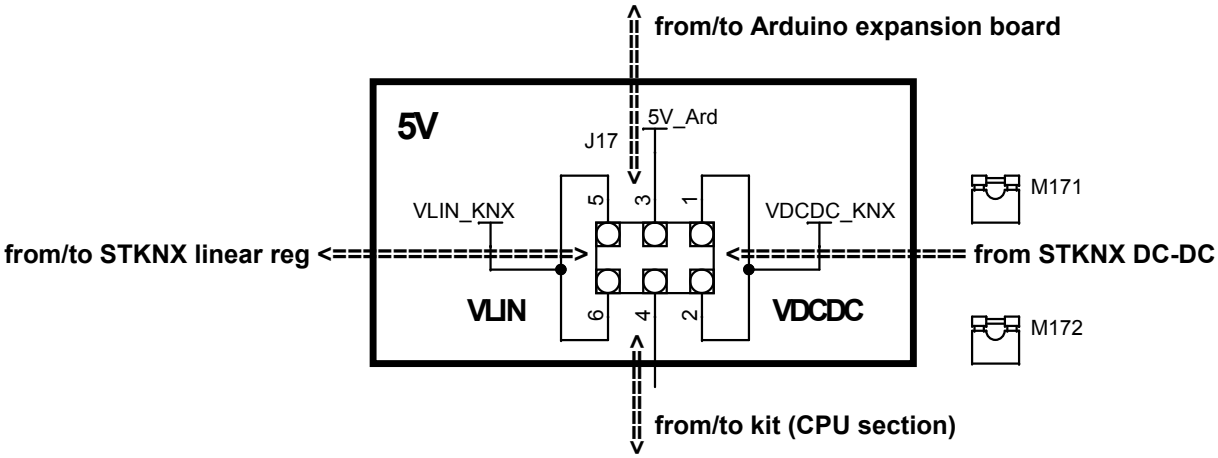
3.5.2 Jumpers for power supply routing

Figure 28. Jumpers for supply routing



Jumpers J16, J17 and J18 allow connection between power supply sources and loads.

Figure 29. Power supply routing with J16, J17 and J18



In the example below, J17 allows the following:

- Use STKNX DC-DC to supply the kit (pos. 2-4) and/or the Arduino daughterboard (pos. 1-3)
  - Do not use STKNX DC-DC (pos. 1-2)
- Use STKNX linear regulator to supply the kit (pos. 4-6) and/or the Arduino daughterboard (pos. 3-5), or vice versa supply STKNX VCCCORE from the kit or Arduino
  - Do not use STKNX linear regulator (pos. 5-6)
- Supply kit from Arduino or vice versa (pos. 3-4). The same principle applies to J16 and J18.

3.5.3 Jumpers for kit regulator routing

When it is not possible to use the STKNX DC-DC or linear regulator, you can use regulators U14 (5 V) and U15 (3.3 V) as an alternative. Jumpers J19 and J20 allow routing U14/5 V and/or U15/3.3 V to the Arduino board, the kit, or to STKNX VCCCORE.

J20 is also used to supply the kit via USB source.

RELATED LINKS

3.6.1 Kit power supply from USB connector on page 30

3.5.4 Power supply configuration examples

3.5.4.1 STKNX mode DC-DC 5 V (default)

Figure 30. STKNX mode DC-DC 5 V

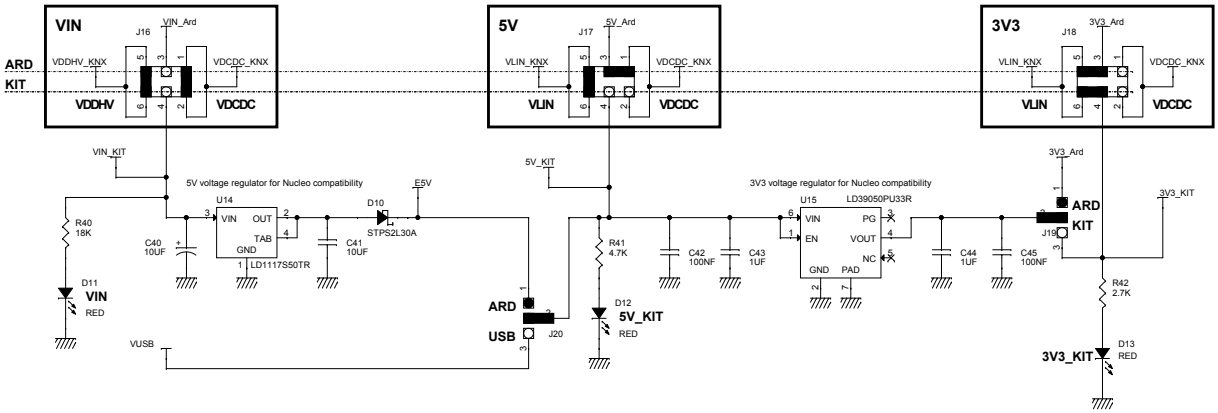
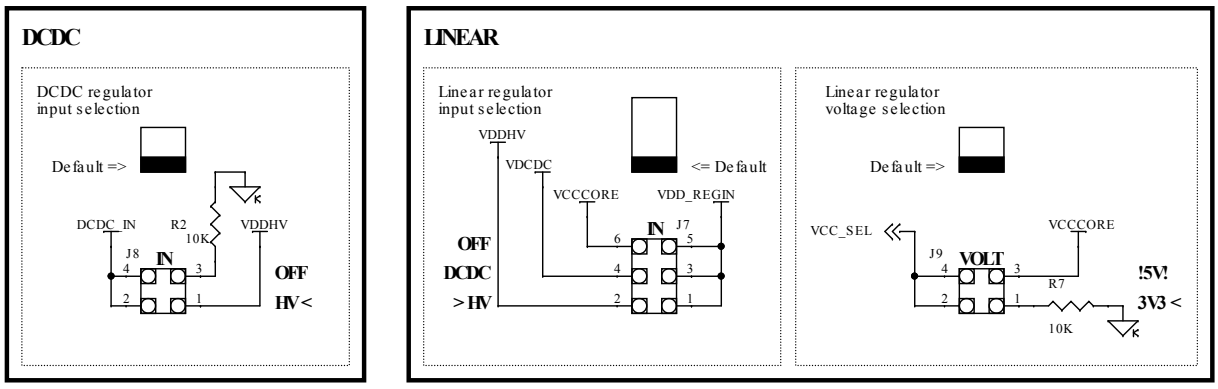


Figure 31. J7, J8 and J9 config for DC-DC 5 V mode



The default kit configuration is shown above:

- The STKNX linear regulator supplies the CPU section
- The STKNX DC-DC converter is available for the Arduino daughterboard
- The kit regulators are not used
- On the STKNX side, the DC-DC converter (5 V) and linear regulator are active
- Jumper M37 must be removed in order to release the target CPU reset pin
- Both jumpers M32 and M43 are open and M39 is connected.

3.5.4.2 STKNX mode DC-DC 3V3

Figure 32. **STKNX mode DC-DC 3V3**

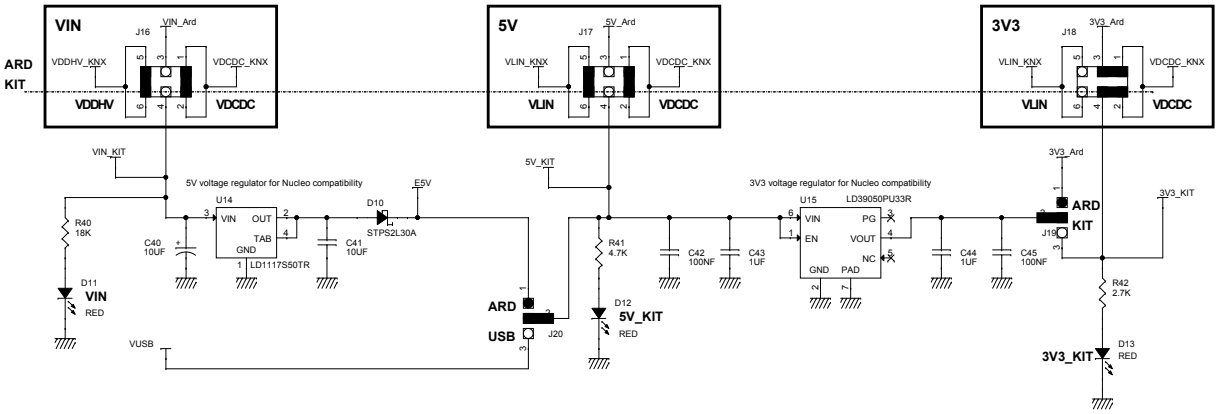
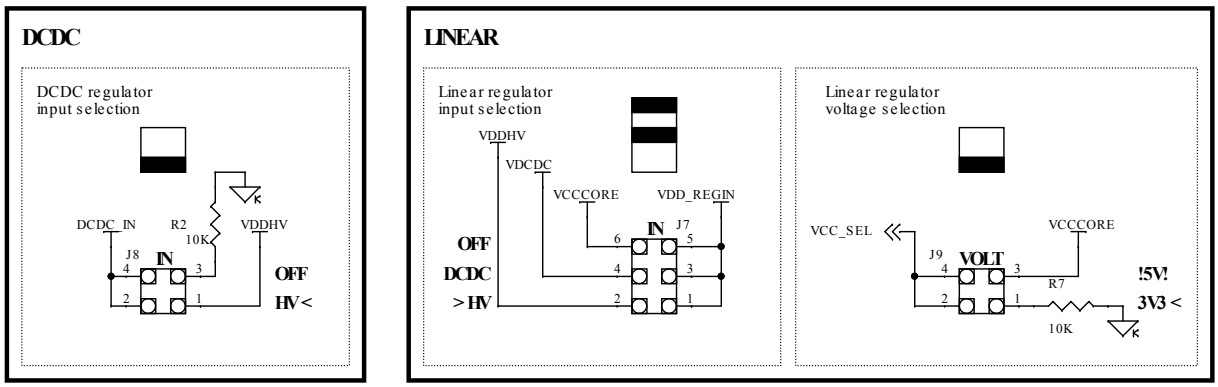


Figure 33. **J7, J8 and J9 config for DC-DC 3V3 mode**

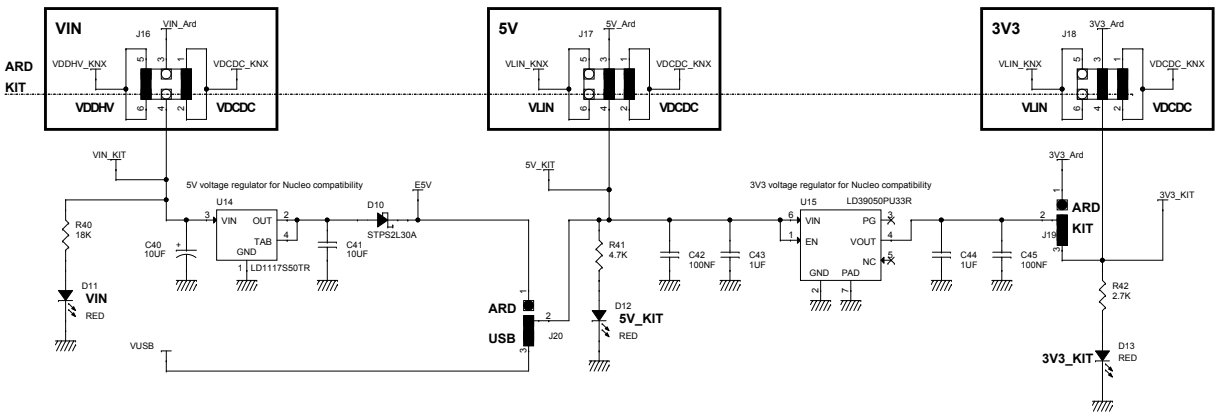


This mode offers the best consumption on KNX bus (see Table 1. EVALKITSTKNX power consumption figures).

- The DC-DC converter is tuned to 3.3 V and supplies both CPU section and Arduino board
- The STKNX linear regulator is disabled
- Jumper M37 must be removed in order to release the target CPU reset pin
- Both jumpers M32 and M43 are open and M39 is connected.

3.5.4.3 FW mode

Figure 34. **FW mode**



This mode lets you use the kit on a desk with a PC. As communication on the KNX bus is not necessary, STKNX section is not powered and a laboratory supply is not needed.

This mode is suitable for firmware editing and debugging:

- The +5 V generated from USB connector is available as VUSB and sent to Arduino board
- U15 allows generating 3.3 V voltage (from VUSB) for the kit and the Arduino board
- In case the KNX bus voltage is applied, the USB power must be already present
- The total power consumption sunk from the PC on USB_VCC should not exceed 300 mA. Please note that the consumption of the STLINK/V2-1 section is 50 mA.
- Jumper M37 must be set in order to control the target CPU reset pin
- Both jumpers M32 and M43 are open and M39 is connected.

3.5.4.4 *Dimming mode (application example)*

Figure 35. Dimming demonstration mode

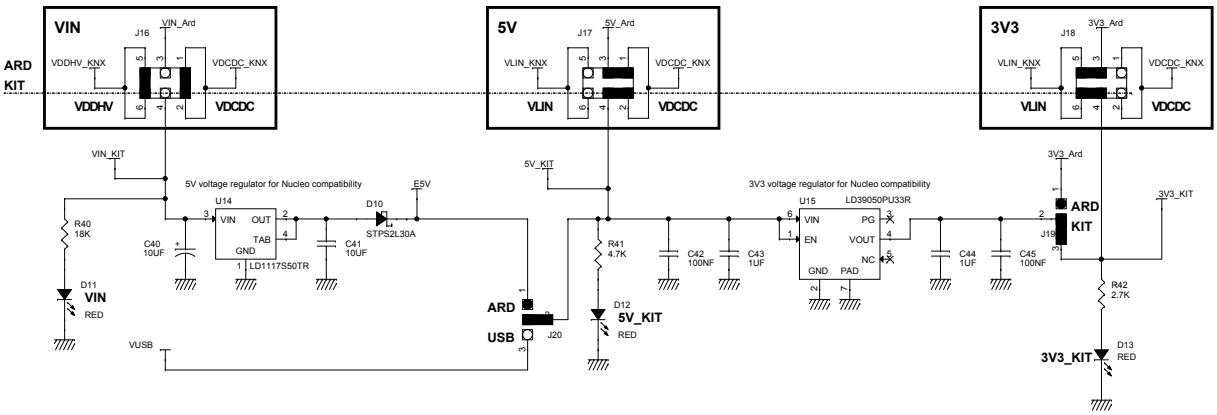
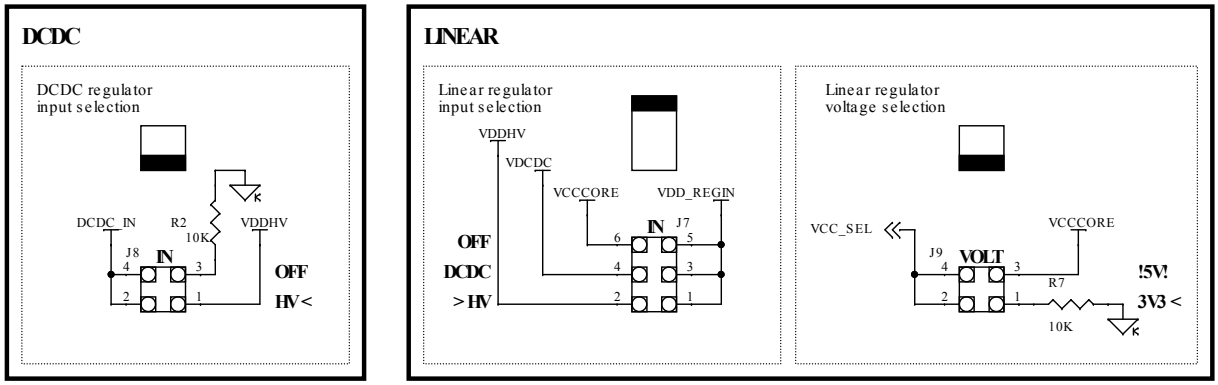


Figure 36. J7, J8 and J9 config for dimming demonstration mode



In this mode, an ST X-NUCLEO-LEDA1 daughterboard is plugged on the EVALKITSTKNX (see Figure 16. X-NUCLEO-LEDA1 board plugged on EVALKITSTKNX) and the STKNX supplies the entire kit (apart from ST-LINK) from the KNX bus:

- The STKNX DC-DC output is set to 5 V and supplies the dimming board and kit regulator U15.
- This 3.3 V regulator supplies the kit, the Arduino board, and the STKNX VCCCORE. This offers better current consumption than using the STKNX linear regulator fed by VDDHV.
- On the STKNX side, the DC-DC converter must be active and linear regulator disabled.
- Jumper M37 must be removed in order to release the target CPU reset pin.

3.6 Debug and control section

The EVALKITSTKNX embeds the STLINK/V2-1 programming and debugging tool, and is very similar to the STM32 Nucleo-64 board. It also integrates the following features:

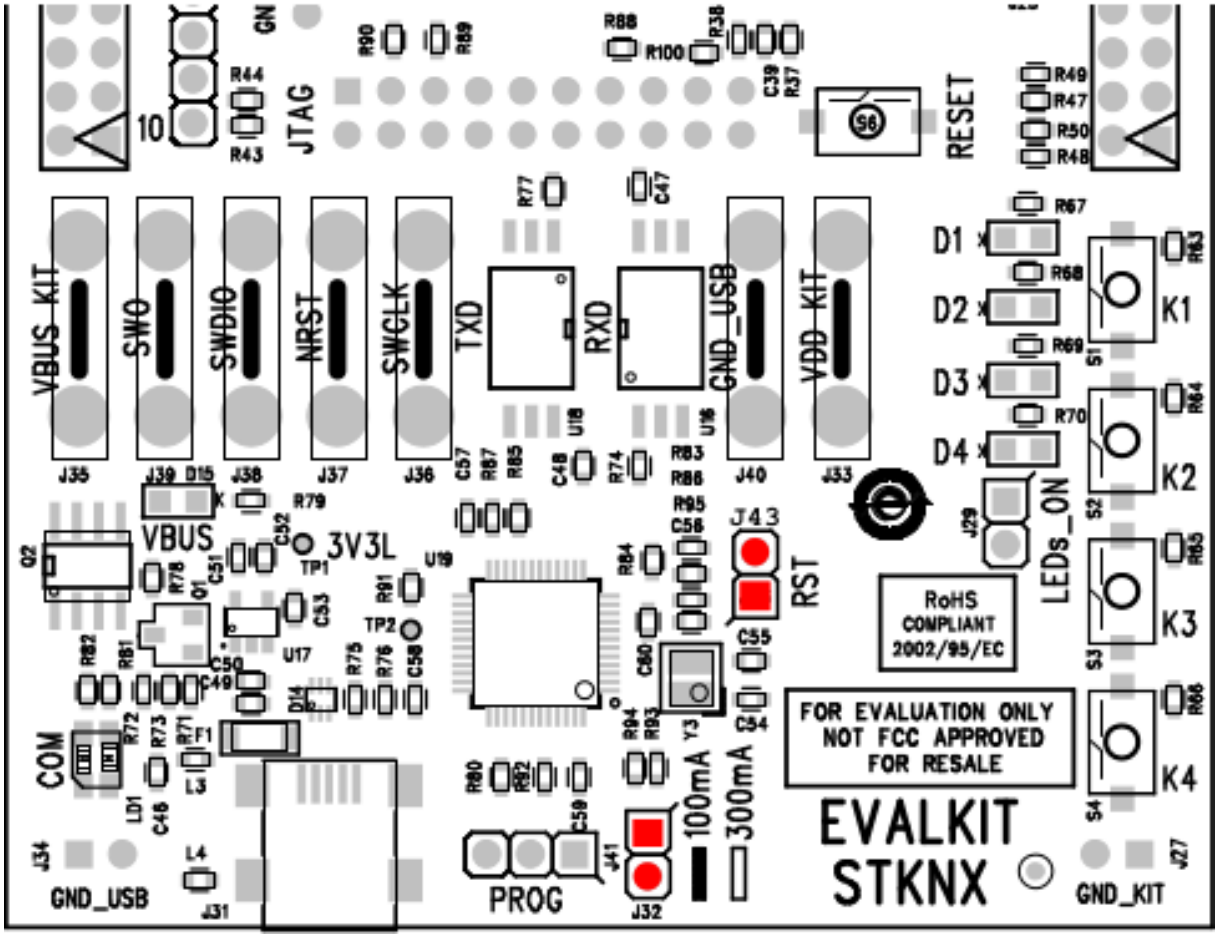
- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100 mA power on USB.

All these features are accessible from the USB connector J31 to which the user PC has to be connected.

For a proper use, please check that both jumpers M32 and M43 are open (highlighted in

The figure below).

Figure 37. EVALKITSTKNX M32 and M43



RELATED LINKS

The relevant information can be found in User manual UM1724 on the ST website

3.6.1 Kit power supply from USB connector

After a successful enumeration between the STLINK CPU U19 and the PC connected to the USB connector J31, the transistor Q2 is closed and VBUS (USB_VCC) voltage is available on VBUS_SWITCHED (D15 lights on). Assuming that the golden jumper M35 is closed, the voltage named VUSB is then available at J20.3 and offers the possibility to supply the whole kit from the PC, as described in Section 3.5.4.3 FW mode.

3.6.2 Debug/programming interface

Two hardware debug interfaces are available on EVALKISTKNX:

- The STLINK/V2-1 programming and debugging environment is available from the USB J31 connector and requires only a type A to mini-B USB cable to connect to the external PC. The golden jumpers M33 and M35 to M40 have to be inserted.
- The HE10 20-pin connector J42 is also provided (on the bottom side of the kit) to use any alternative debug environment through serial wire debug (SWD) and JTAG interfaces. An external probe has to be used in this case, and the golden jumpers M33 and M35 to M40 have to be removed.

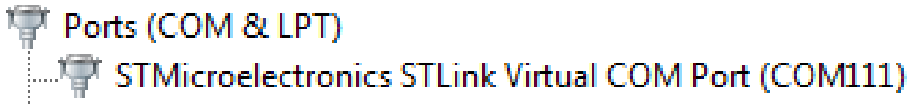
Note: Caution: During the debug, it is not possible to isolate the PC from the kit.

3.6.3 Virtual COM port

The USART3 interface (PC10, PC11) of the target microcontroller U11 is available from the PC as an isolated virtual COM Port thanks to STLINK/V2-1, as illustrated in the figure below. To ensure the isolation between the PC and the kit, the jumpers M33 and M35 to M40 have to be removed. Debug is not possible in isolated mode.

Ensure that the four resistors R47 to R50 are mounted as they were originally on the kit, to make the link between the target STM32 and the STLINK MCU.

Figure 38. Virtual COM port



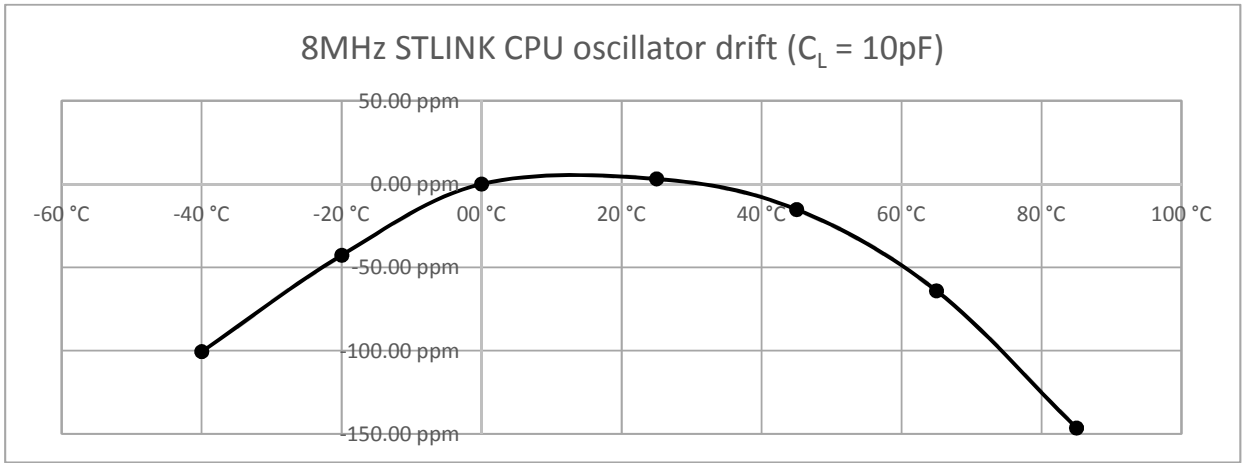
3.6.4 STLINK CPU crystal oscillator

The load capacitors values of the 8MHz oscillators have been adjusted through measurement of the oscillators' frequency drift across the -40°C/+85°C temperature range, and centering the frequency to the nominal value for T = 25°C.

The following figure shows the frequency drift of the 8 MHz with the following load capacitors values:

- C54 = C55 = 10 pF

Figure 39. 8MHz oscillator response



4 KNX physical layer performance vs. 8/2/2 tests

This section reports the performances results of the EVALKITSTKNX submitted to the tests described in the KNX System Conformance Testing document, Section 8/2/2 (Physical Layer) Version 01.04.02 AS.

As the EVALKITSTKNX is configurable, the tests are applied to several configurations of the kit, in order to cover a large portion of the use cases of STKNX. Several configurations of fan-in, voltage regulators outputs and loads, isolation, are tested:

- Fan-in : 10 mA and 30 mA
- DC-DC converter output voltage: 1 V, 3.3 V, 5 V, 12 V
- Linear regulator output voltage: 3.3 V, 5 V
- DC-DC converter and linear regulator loads: typical kit configuration, and maximum output current (determined either by the fan-in or the regulator capability)
- Optocouplers for isolation.

The tests have been executed on the hardware release V141 of the EVALKITSTKNX.

For each test specified in the section 8/2/2, a table reports the results of every configurations of the kit. The waveforms of the signals are also reported for the most significant tests of the table.

For detailed description of the tests, of their preparation and of their requirements, please refer to the KNX System Conformance Testing document, Section 8/2/2 of KNX standard.

4.1 General test setup

The following instruments are used for the performance tests:

- PSU: Agilent DC power supply E3631A
- DSO: Agilent oscilloscope DSO 6054A
- CP: Agilent current probe 1147B
  - a x10 turns loop is used to improve the current probe sensitivity, so a ÷ 10 divider factor must be applied to the measurements results
- AWG: Agilent Arbitrary Waveform generator 33250A.

The following EVALKITSTKNX has been used as BDUT for the tests related to fan-in = 10 mA:

- EVALKITSTKNX “KA030-141” with recommended BOM modifications for 10 mA fan-in:
  - Cgate = 47 µF Murata GRT31CR61A476KE13L
  - Cvddhv = 100 µF Panasonic EEEFK1V101XP

and the following EVALKITSTKNX for the tests related to fan-in = 30 mA:

- EVALKITSTKNX “KA084-141” with BOM modification:
  - Cgate = 10 µF Murata GRM31CR71A106KA01

When testing linear regulator and DC-DC converter output voltages at values different from those of the default configuration of the kit, the BOM options reported in EVALKITSTKNX schematic, at STKNX page have been applied.

Unless otherwise specified, the firmware used (for most tests) is EvalKitSTKNX_LedLevel_V1.0.bin, a demonstration firmware embedding a KNX protocol stack.

RELATED LINKS

Visit the EVALKISTKNX product page for the documents and the firmware used to execute the tests

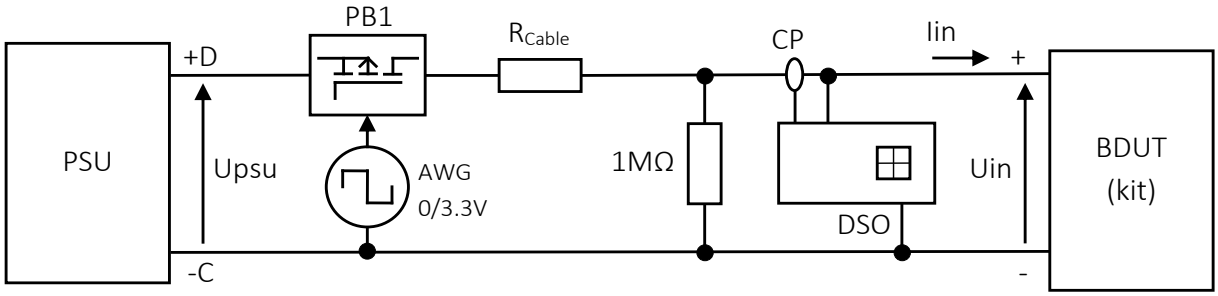
See UM2409 Quick start guide STKNX evaluation board (EVALKITSTKNX)

4.2 Power Conversion (Switch On Fast) (8/2/2 - test 4.2)

This test simulates the connection of a single bus device to an operating bus segment.

4.2.1 Test setup

Figure 40. **Switch On Fast test setup**

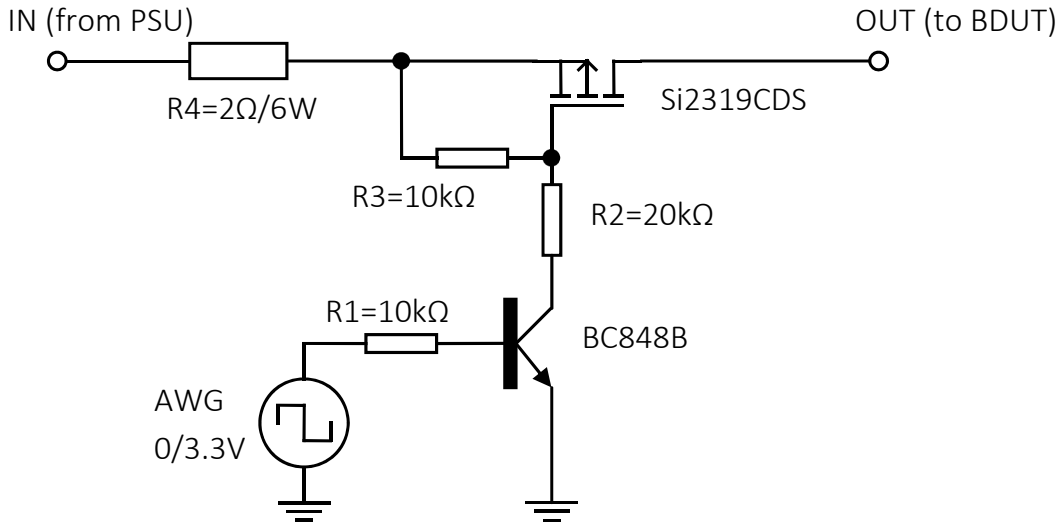


- Oscilloscope channels:
  - CH1: BP1 command
  - CH2: Uin
  - CH3: BDUT regulator voltage output
  - CH4: Iin
- Function generator period: 30 s
- Excepted when the default configuration of the kit is tested, every “isolation” jumper (between STKNX and CPU sections) is removed and the evaluated regulator/converter is loaded at its maximum load
- Embedded FW: EvalKitSTKNX_LedLevel_V1.0.bin (see Section 4.1 General test setup).

4.2.1.1 *PB1 description*

As suggested in KNX standard Section 8/2/2, the push button is replaced by the MOSFET based circuit, described in Figure 41, which allows making repetitive tests and prevents the bounces typical of mechanical switches.

Figure 41. **MOSFET circuit for power supply connection**



- Si2319CDS: MOSFET 40 V $R_{DS(on)}$ < 100 mΩ
- When the AWG applies a 3.3 V voltage, the MOSFET transistor is conducting thanks to the voltage Upsu/3 applied to V_{GS}
- R3 ensures V_{GS}=0 when the function generator output voltage = 0 V
- The low value resistor R4 allows limiting the inrush current at initial MSOFET closure, especially during the test “Switch On/Off Slow” where huge capacitors are present.

4.2.2 Tests results - fan-in = 10 mA

Table 2. Switch On Fast tests results - fan-in = 10 mA

EVALKITSTKNX configuration				Test conditions		Test results	
Linear Reg		DC-DC converter		Upsu- Rcable	Iin DC	Tstartup (Limit = 10s)	Iin max (Limit = 30mA)(1)
Voltage	Load	Voltage	Load				
Any	Any	Any	Any	30V - 0Ω	Any	-	159mA / 3µs
Any	Any	Any	Any	30V - 35Ω	Any	-	123mA / 3.2µs
Any	Any	Any	Any	20V - 0Ω	Any	-	64mA / 2.9µs
Any	Any	Any	Any	20V - 35Ω	Any	-	50mA / 2.9µs
3.3V	347Ω / 9.6mA	Disabled	Disabled	30V - 0Ω	**10mA (Fan-in)**	0.5s	32mA / 12ms
3.3V	347Ω / 9.6mA	Disabled	Disabled	30V - 35Ω	**10mA (Fan-in)**	0.5s	32mA / 12ms
3.3V	347Ω / 9.6mA	Disabled	Disabled	20V - 0Ω	**10mA (Fan-in)**	0.5s	25mA
3.3V	347Ω / 9.6mA	Disabled	Disabled	20V - 35Ω	**10mA (Fan-in)**	0.5s	24mA
5V	512Ω / 9.8mA	Disabled	Disabled	30V - 0Ω	**10mA (Fan-in)**	0.5s	26mA
5V	512Ω / 9.8mA	Disabled	Disabled	30V - 35Ω	**10mA (Fan-in)**	0.5s	25mA
5V	512Ω / 9.8mA	Disabled	Disabled	20V - 0Ω	**10mA (Fan-in)**	0.5s	18mA
5V	512Ω / 9.8mA	Disabled	Disabled	20V - 35Ω	**10mA (Fan-in)**	0.5s	18mA
Disabled	VDD_REGIN= VDDHV	**1V**	10Ω / 96mA	30V - 0Ω	6.2mA	0.5s	26mA
Disabled	VDD_REGIN= VDDHV	**1V**	10Ω / 96mA	30V - 35Ω	6.2mA	0.5s	25mA
Disabled	VDD_REGIN= VDDHV	**1V**	10Ω / 96mA	20V - 0Ω	**10mA (Fan-in)**	0.4s	18mA
Disabled	VDD_REGIN= VDDHV	**1V**	10Ω / 96mA	20V - 35Ω	**10mA (Fan-in)**	0.4s	18mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	30V - 0Ω	2.7mA	1s	26mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	30V - 35Ω	2.7mA	1s	25mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	20V - 0Ω	4mA	0.6s	18mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	20V - 35Ω	4mA	0.6s	18mA
Disabled	VCCORE= VDCDC	**3.3V**	102Ω / 33mA	30V - 0Ω	6.3mA	0.5s	26mA
Disabled	VCCORE= VDCDC	**3.3V**	102Ω / 33mA	30V - 35Ω	6.3mA	0.5s	25mA
Disabled	VCCORE= VDCDC	**3.3V**	102Ω / 33mA	20V - 0Ω	10mA (Fan-in)	0.4s	18mA
Disabled	VCCORE= VDCDC	**3.3V**	102Ω / 33mA	20V - 35Ω	10mA (Fan-in)	0.4s	17mA
Disabled	VCCORE= VDCDC	**5V**	102Ω / 33mA	30V - 0Ω	6.4mA	0.5s	26mA
Disabled	VCCORE= VDCDC	**5V**	102Ω / 33mA	30V - 35Ω	6.4mA	0.5s	25mA
Disabled	VCCORE= VDCDC	**5V**	102Ω / 33mA	20V - 0Ω	10mA (Fan-in)	0.4s	17mA
Disabled	VCCORE= VDCDC	**5V**	102Ω / 33mA	20V - 35Ω	10mA (Fan-in)	0.4s	17mA

EVALKITSTKNX configuration				Test conditions		Test results	
Linear Reg		DC-DC converter		Upsu- Rcable	Iin DC	Tstartup (Limit = 10s)	Iin max (Limit = 30mA)(1)
Voltage	Load	Voltage	Load				
Enabled	VDD_REGIN= VDCDC	**12V**	1.35kΩ / 9mA	30V - 0Ω	5.8mA	0.5s	25mA
Enabled	VDD_REGIN= VDCDC	**12V**	1.35kΩ / 9mA	30V - 35Ω	5.8mA	0.5s	25mA
Enabled	VDD_REGIN= VDCDC	**12V**	1.35kΩ / 9mA	20V - 0Ω	10mA (Fan-in)	0.4s	18mA
Enabled	VDD_REGIN= VDCDC	**12V**	1.35kΩ / 9mA	20V - 35Ω	10mA (Fan-in)	0.4s	17mA
				Cumulative result	PASS		

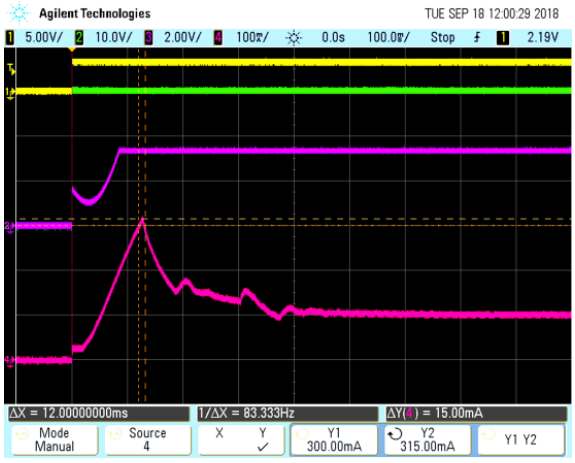
1. *Limits tolerate spikes of 45mA if width < 30ms and 500mA if width < 30µs.*

4.2.2.1 *Linear regulator 3.3 V waveforms (loaded to reach fan-in limit)*

Note: *Note: The default configuration of the kit cannot be tested with fan-in 10 mA because the total consumption of the kit is 12 mA when the CPU section is supplied by the STKNX linear regulator.*

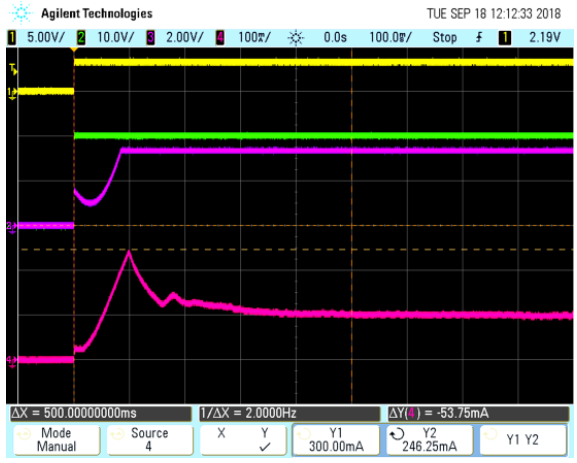
The linear regulator set to 3.3 V is supplied from VDDHV and loaded with 347 Ω/9.6 mA for a KNX bus consumption of 10 mA at 30 V. The DC-DC converter is disabled.

Figure 42. Upsu = 30V, Rcable = 0Ω (IinDC = 10mA)



Tstart-up = 0.5s	Limit = 10s
Iin max = 32mA	Limit = 45mA
Width above 30mA = 12ms	Limit = 30ms

Figure 43. Upsu = 20V, Rcable = 0Ω (IinDC = 10mA)



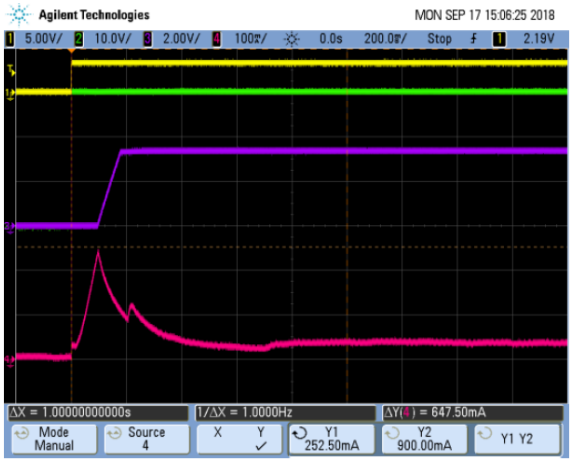
Tstart-up = 0.5s	Limit = 10s
Iin max = 25mA	Limit = 30mA

For the purpose of the test, the waveforms with Rcable = 35 Ω do not differ significantly from the ones with Rcable 0 Ω, shown above. They are reported only once for the test case DC- DC 3.3 V 10 mA in Section 4.2.2.3 DC-DC converter 3.3V waveforms (loaded to reach fan-in limit).

4.2.2.2 *DC-DC converter 3.3V waveforms (loaded with kit)*

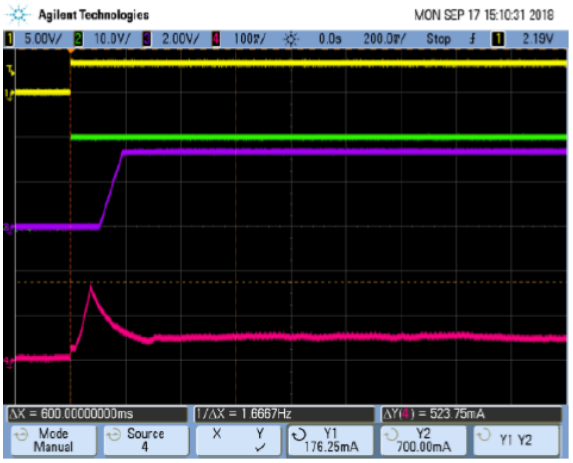
The DC-DC converter set to VDCDC = 3.3 V supplies the kit (3V3_KIT) with a 12 mA current. The linear regulator is disabled and VCCCORE is supplied with VDCDC.

Figure 44. Upsu = 30V, Rcable = 0Ω (IinDC = 2.7mA)



Tstart-up = 1s	Limit = 10s
Iin max = 26mA	Limit = 30mA

Figure 45. Upsu = 20V, Rcable = 0Ω (IinDC = 4mA)



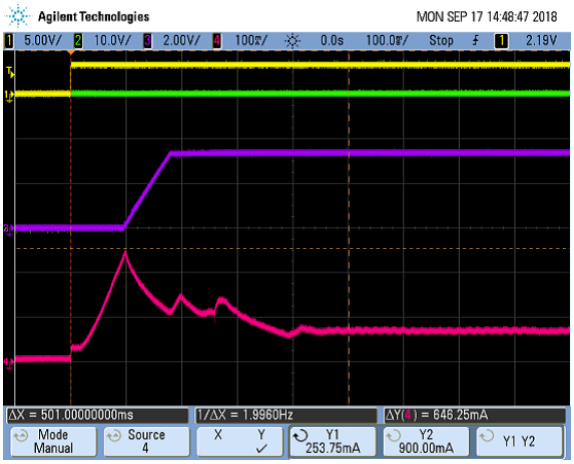
Tstart-up = 0.6s	Limit = 10s
Iin max = 18mA	Limit = 30mA

For the purpose of the test, the waveforms with Rcable = 35 Ω do not differ significantly from the ones with Rcable 0 Ω, shown above. They are reported only once for the test case DC-DC 3.3 V 10 mA in Section 4.2.2.3 DC-DC converter 3.3V waveforms (loaded to reach fan-in limit).

4.2.2.3 *DC-DC converter 3.3V waveforms (loaded to reach fan-in limit)*

The DC-DC converter set to VDCDC = 3.3 V is loaded with 102 Ω/33 mA for a KNX bus consumption of 10 mA at 20 V. The linear regulator is disabled and VCCCORE is supplied with VDCDC.

Figure 46. Upsu = 30V, Rcable = 0Ω (IinDC = 6.3mA)



Tstart-up = 0.5s	Limit = 10s
Iin max = 26mA	Limit = 30mA

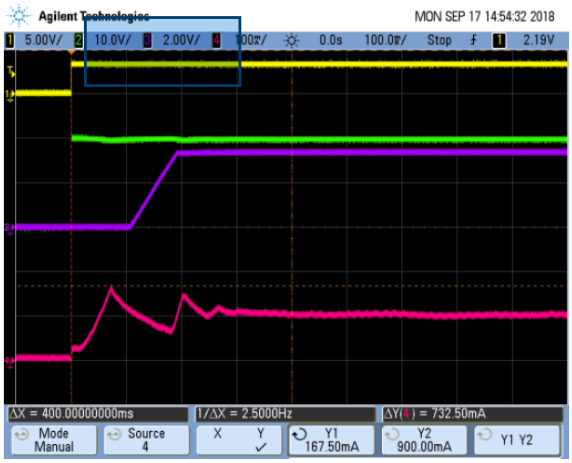
Figure 47. Upsu = 20V, Rcable = 0Ω (IinDC = 10mA)

Tstart-up = 0.4s	Limit = 10s
Iin max = 18mA	Limit = 30mA

Figure 48. Upsu = 30V, Rcable = 35Ω (IinDC = 6.3mA)

Tstart-up = 0.5s	Limit = 10s
Iin max = 25mA	Limit = 30mA

Figure 49. Upsu = 20V, Rcable = 35Ω (IinDC = 10mA)



Tstart-up = 0.4s	Limit = 10s
Iin max = 17mA	Limit = 30mA

4.2.2.4 *DC-DC converter 12 V waveforms (loaded to reach fan-in limit)*

The DC-DC converter set to VDCDC = 12 V is loaded with 1.35 kΩ/9 mA for a KNX bus consumption of 10 mA at 20 V. The linear regulator is enabled, not loaded and supplied from VDCDC.

Figure 50. Upsu = 30V, Rcable = 0Ω (IinDC = 5.8mA)

Tstart-up = 0.5s	Limit = 10s
Iin max = 25mA	Limit = 30mA

Figure 51. Upsu = 20V, Rcable = 0Ω (IinDC = 10mA)

Tstart-up = 0.4s	Limit = 10s
Iin max = 18mA	Limit = 30mA

For the purpose of the test, the waveforms with Rcable = 35 Ω do not differ significantly from the ones with Rcable 0 Ω, shown above. They are reported only once for the test case DC-DC 3.3 V 10 mA in Section 4.2.2.3 DC-DC converter 3.3V waveforms (loaded to reach fan-in limit).

4.2.3 Tests results - fan-in = 30 mA

Table 3. **Switch On Fast tests results - fan-in = 30 mA**

EVALKITSTKNX configuration				Test conditions		Test results	
Linear Reg		DC-DC converter		Upsu- Rcable	Iin DC	Tstartup (Limit = 10s)	Iin max / duration (Limit = 90mA) (1)
Voltage	Load	Voltage	Load				
Any	Any	Any	Any	30V - 0Ω	Any	-	159mA / 3µs
Any	Any	Any	Any	30V - 35Ω	Any	-	122mA / 3.2µs
Any	Any	Any	Any	20V - 0Ω	Any	-	64mA / 2.9µs
Any	Any	Any	Any	20V - 35Ω	Any	-	50mA / 2.9µs
3.3V	**Kit / 12mA**	5V	NO	30V - 0Ω	13mA	0.5s	60mA
3.3V	**Kit / 12mA**	5V	NO	30V - 35Ω	13mA	0.5s	50mA
3.3V	**Kit / 12mA**	5V	NO	20V - 0Ω	13mA	0.4s	51mA
3.3V	**Kit / 12mA**	5V	NO	20V - 35Ω	13mA	0.4s	49mA
3.3V	**20mA (max.)**	Disabled	Disabled	30V - 0Ω	21mA	0.6s	61mA
3.3V	**20mA (max.)**	Disabled	Disabled	30V - 35Ω	21mA	0.6s	61mA
3.3V	**20mA (max.)**	Disabled	Disabled	20V - 0Ω	21mA	0.5s	52mA
3.3V	**20mA (max.)**	Disabled	Disabled	20V - 35Ω	21mA	0.5s	52mA
5V	**20mA (max.)**	Disabled	Disabled	30V - 0Ω	21mA	0.6s	61mA
5V	**20mA (max.)**	Disabled	Disabled	30V - 35Ω	21mA	0.6s	59mA
5V	**20mA (max.)**	Disabled	Disabled	20V - 0Ω	21mA	0.5s	48mA
5V	**20mA (max.)**	Disabled	Disabled	20V - 35Ω	21mA	0.5s	50mA
Disabled	VDD_REGIN= VDDHV	**1V**	7Ω / 150mA **(max.)**	30V - 0Ω	16mA	0.6s	49mA
Disabled	VDD_REGIN= VDDHV	**1V**	7Ω / 150mA **(max.)**	30V - 35Ω	16mA	0.6s	50mA
Disabled	VDD_REGIN= VDDHV	**1V**	7Ω / 150mA **(max.)**	20V - 0Ω	21mA	0.6s	37mA
Disabled	VDD_REGIN= VDDHV	**1V**	7Ω / 150mA **(max.)**	20V - 35Ω	21mA	0.6s	39mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	30V - 0Ω	3mA	0.5s	51mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	30V - 35Ω	3mA	0.5s	50mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	20V - 0Ω	4.6mA	0.5s	37mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	20V - 35Ω	4.6mA	0.5s	39mA
Disabled	VCCORE= VDCDC	**3.3V**	33Ω / 100mA	30V - 0Ω	19mA	0.6s	53mA
Disabled	VCCORE= VDCDC	**3.3V**	33Ω / 100mA	30V - 35Ω	19mA	0.6s	51mA
Disabled	VCCORE= VDCDC	**3.3V**	33Ω / 100mA	20V - 0Ω	**30mA (Fan-in)**	0.6s	39mA
Disabled	VCCORE= VDCDC	**3.3V**	33Ω /	20V - 35Ω	**30mA (Fan-in)**	0.6s	38mA

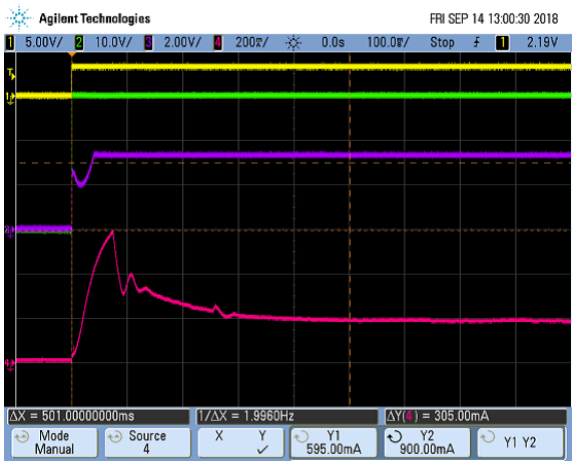
EVALKITSTKNX configuration				Test conditions		Test results	
Linear Reg		DC-DC converter		Upsu- Rcable	Iin DC	Tstartup (Limit = 10s)	Iin max / duration (Limit = 90mA) (1)
Voltage	Load	Voltage	Load				
			100mA				
Disabled	VCCORE= VDCDC	**5V**	74kΩ / 69mA	30V - 0Ω	19mA	0.6s	52mA
Disabled	VCCORE= VDCDC	**5V**	74kΩ / 69mA	30V - 35Ω	19mA	0.6s	50mA
Disabled	VCCORE= VDCDC	**5V**	74kΩ / 69mA	20V - 0Ω	**30mA (Fan-in)**	0.6s	40mA
Disabled	VCCORE= VDCDC	**5V**	74kΩ / 69mA	20V - 35Ω	**30mA (Fan-in)**	0.6s	42mA
Enabled	VDD_REGIN= VDCDC	**12V**	404kΩ / 31mA	30V - 0Ω	19mA	0.6s	52mA
Enabled	VDD_REGIN= VDCDC	**12V**	404kΩ / 31mA	30V - 35Ω	19mA	0.6s	50mA
Enabled	VDD_REGIN= VDCDC	**12V**	404kΩ / 31mA	20V - 0Ω	**30mA (Fan-in)**	0.6s	37mA
Enabled	VDD_REGIN= VDCDC	**12V**	404kΩ / 31mA	20V - 35Ω	**30mA (Fan-in)**	0.6s	39mA
				Cumulative result	PASS		

1. *Limits tolerate spikes of 135mA if width < 30ms and 1.5A if width < 30µs.*

4.2.3.1 *Default kit configuration waveforms*

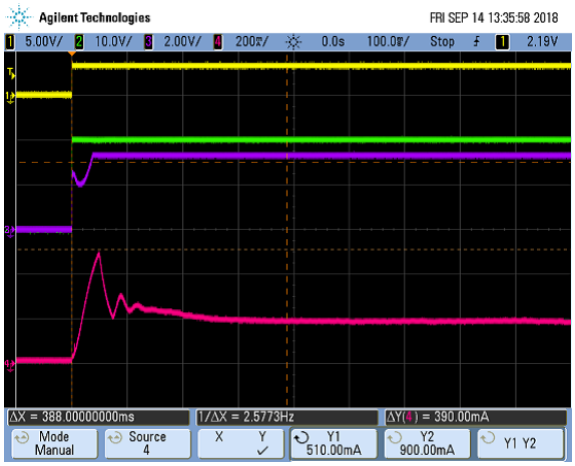
This configuration is described in Section 3.5.4.1 STKNX mode DC-DC 5 V (default). The linear regulator 3.3 V is supplying the kit (3V3_KIT) and the 5 V DC-DC converter is not loaded.

Figure 52. Upsu = 30V, Rcable = 0Ω (IinDC = 12.5mA)



Tstart-up = 0.5s	Limit = 10s	Tstart-up = 0.4s	Limit = 10s
Iin max = 60mA	Limit = 90mA	Iin max = 51mA	Limit = 90mA

Figure 53. Upsu = 20V, Rcable = 0Ω (IinDC = 12.4mA)

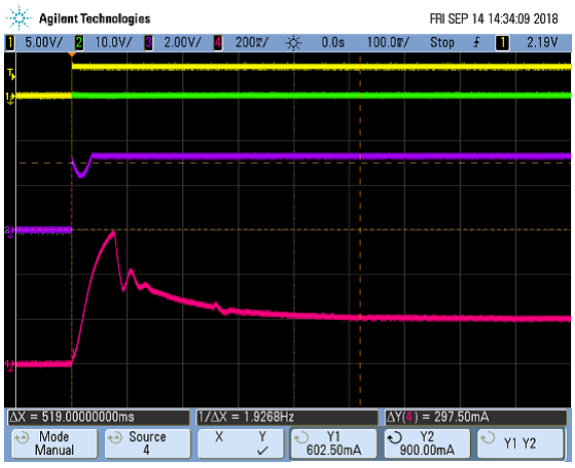


For the purpose of the test, the waveforms with Rcable = 35 Ω do not differ significantly from the ones with Rcable = 0Ω shown above. They are reported only once for the test case DC-DC 3.3V 30mA in Section 4.2.3.4 DC-DC converter 3.3 V waveforms (loaded to reach fan-in limit).

4.2.3.2 *Linear regulator 3.3 V waveforms (load = 20 mA)*

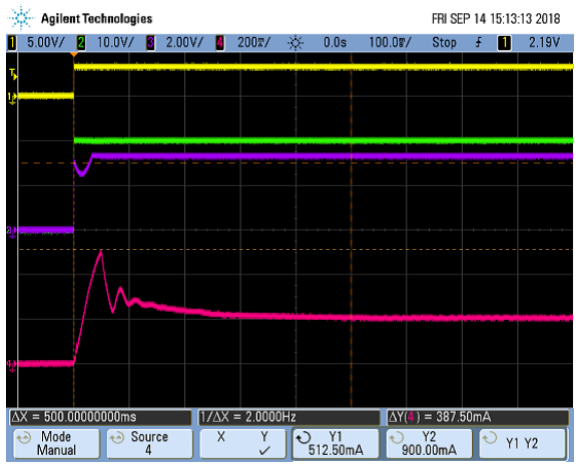
The linear regulator set to 3.3 V is loaded with 169 Ω and is supplying its maximum current 20 mA. The DC-DC converter is disabled.

Figure 54. Upsu = 30V, Rcable = 0Ω (IinDC = 21mA)



Tstart-up = 0.6s	Limit = 10s
Iin max = 61mA	Limit = 90mA

Figure 55. Upsu = 20V, Rcable = 0Ω (IinDC = 21mA)



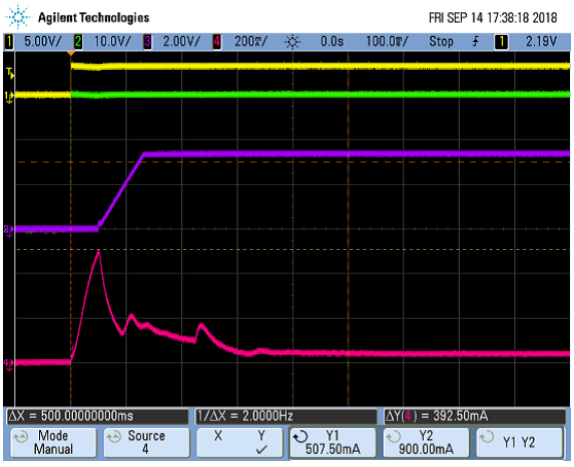
Tstart-up = 0.5s	Limit = 10s
Iin max = 52mA	Limit = 90mA

For the purpose of the test, the waveforms with Rcable = 35 Ω do not differ significantly from the ones with Rcable = 0Ω shown above. They are reported only once for the test case DC-DC 3.3 V 30 mA in Section 4.2.3.4 DC-DC converter 3.3 V waveforms (loaded to reach fan-in limit).

4.2.3.3 *DC-DC converter 3.3 V waveforms (loaded with kit)*

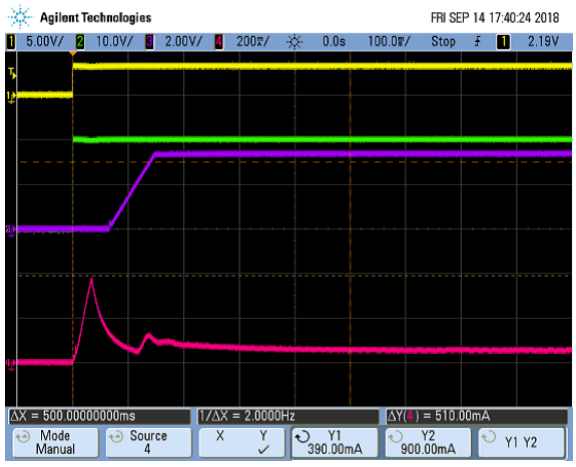
The DC-DC converter set to 3.3 V is supplying the kit (3V3_KIT) with a 12 mA current. The linear regulator is disabled and VCCCORE is supplied with VDCDC.

Figure 56. Upsu = 30V, Rcable = 0Ω (IinDC = 3mA)



Tstart-up = 0.5s	Limit = 10s

Figure 57. Upsu = 20V, Rcable = 0Ω (IinDC = 4.6mA)



Tstart-up = 0.5s	Limit = 10s

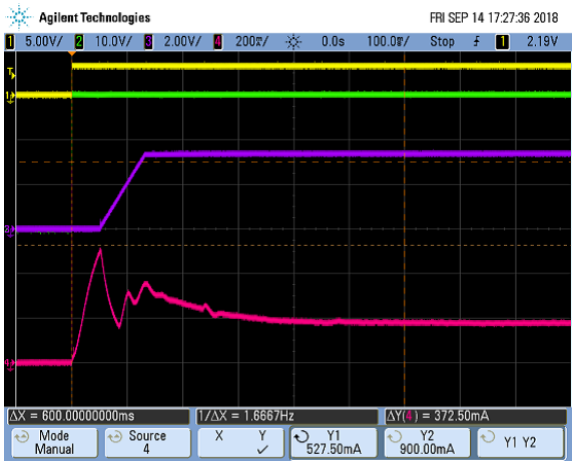
Iin max = 51mA	Limit = 90mA	Iin max = 39mA	Limit = 90mA

For the purpose of the test, the waveforms with Rcable = 35 Ω do not differ significantly from the ones with Rcable = 0Ω shown above. They are reported only once for the test case DC-DC 3.3 V 30 mA in Section 4.2.3.4 DC-DC converter 3.3 V waveforms (loaded to reach fan-in limit).

4.2.3.4 *DC-DC converter 3.3 V waveforms (loaded to reach fan-in limit)*

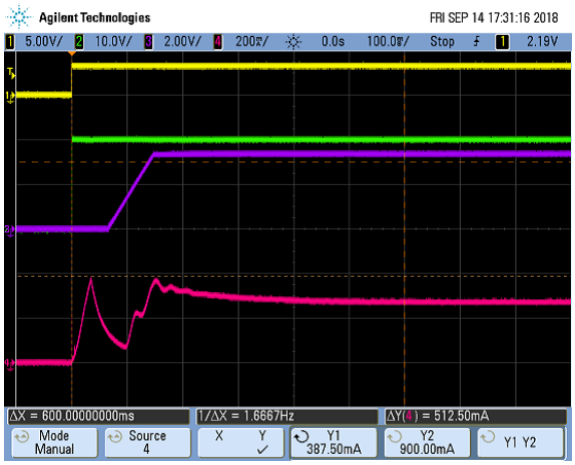
The DC-DC converter set to 3.3 V is loaded with 33 Ω / 100 mA for a KNX bus consumption of 30 mA at 20 V. The linear regulator is disabled and VCCCORE is supplied with VDCDC.

Figure 58. Upsu = 30V, Rcable = 0Ω (IinDC = 18.5mA)



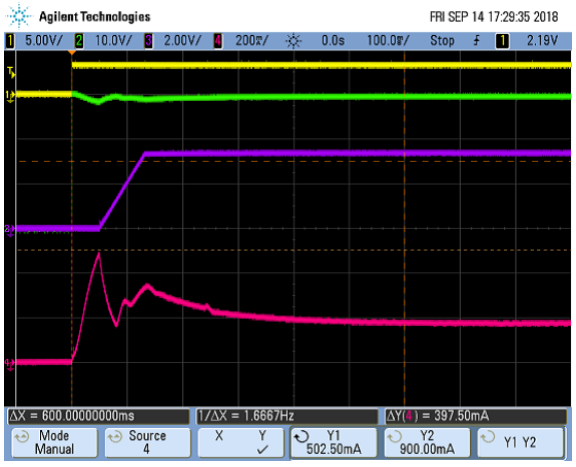
Tstart-up = 0.6s	Limit = 10s
Iin max = 53mA	Limit = 90mA

Figure 59. Upsu = 20V, Rcable = 0Ω (IinDC = 30mA)



Tstart-up = 0.6s	Limit = 10s
Iin max = 39mA	Limit = 90mA

Figure 60. Upsu = 30V, Rcable = 35Ω (IinDC = 18.5mA)



Tstart-up = 0.6s	Limit = 10s
Iin max = 51mA	Limit = 90mA

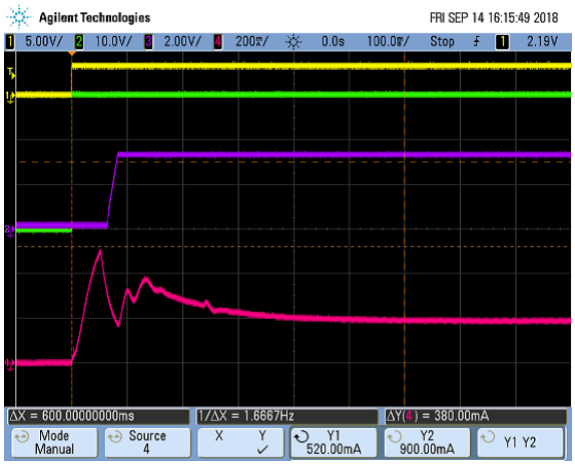
Figure 61. Upsu = 20V, Rcable = 35Ω (IinDC = 30mA)

Tstart-up = 0.6s	Limit = 10s
Iin max = 38mA	Limit = 90mA

4.2.3.5 *DC-DC converter 12 V waveforms (loaded to reach fan-in limit)*

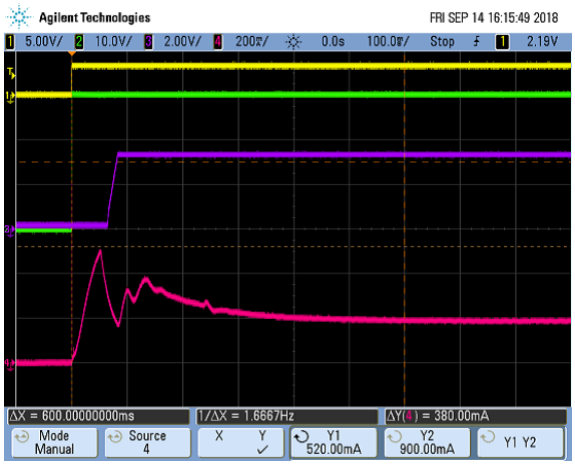
The DC-DC converter set to 12 V is loaded with 404 Ω / 31 mA for a KNX bus consumption of 30 mA at 20 V. The linear regulator is enabled, not loaded and supplied from VDCDC.

Figure 62. Upsu = 30V, Rcable = 0Ω (IinDC = 19mA)



Tstart-up = 0.6s	Limit = 10s
Iin max = 52mA	Limit = 90mA

Figure 63. Upsu = 20V, Rcable = 0Ω (IinDC = 30mA)



Tstart-up = 0.6s	Limit = 10s
Iin max = 39mA	Limit = 90mA

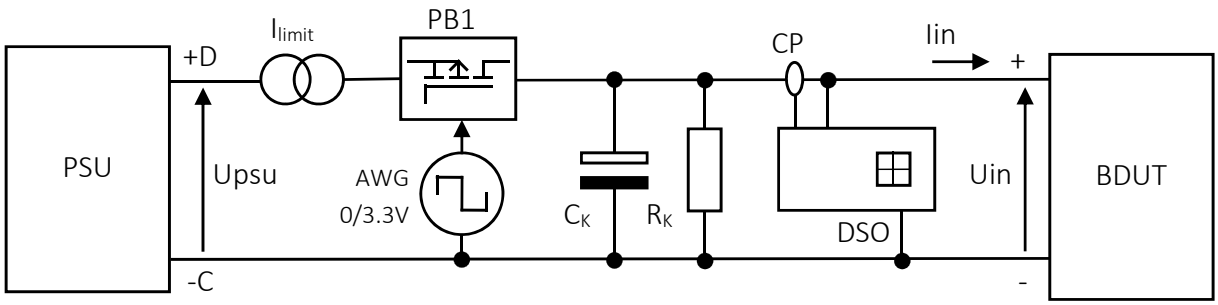
For the purpose of the test, the waveforms with Rcable = 35 Ω do not differ significantly from the ones with Rcable = 0Ω shown above. They are reported only once for the test case DC-DC 3.3 V 30 mA in Section 4.2.3.4 DC-DC converter 3.3 V waveforms (loaded to reach fan-in limit).

4.3 Power Conversion (Switch On/Off Slow) (8/2/2 - test 4.3)

This test simulates the powering up of a fully equipped physical segment.

4.3.1 Test setup

Figure 64. Switch On/Off Slow test setup



- Oscilloscope channels:
  - CH1: BP1 command
  - CH2: Uin
  - CH4: Iin
- PB1: see Section 4.2.1.1 PB1 description
- Function generator period: 40 s
- Excepted when the default configuration of the kit is tested, every “isolation” jumper (between KNX section and CPU section) is removed and the evaluated regulator/converter is loaded at its maximum load.

4.3.2 Tests results - fan-in = 10 mA

Test settings:

- R_K = 1 kΩ
- C_K = 4.7 mF
- I_{limit} = 50 mA
- Embedded FW: EvalKitSTKNX_LedLevel_V1.0.bin (see Section 4.1 General test setup).

Table 4. Switch On/Off Slow tests results - fan-in = 10 mA

EVALKITSTKNX configuration				Test conditions		Test results	
Linear Reg		DC-DC converter		Upsu	Iin DC	Tstartup (Limit = 10s)	Iin max. (Limit = 30mA)(1)
Voltage	Load	Voltage	Load				
3.3V	347Ω / 9.6mA	Disabled	Disabled	30V	**10mA (Fan-in)**	7s	12mA
3.3V	347Ω / 9.6mA	Disabled	Disabled	20V	**10mA (Fan-in)**	2.8s	22mA
5V	512Ω / 9.8mA	Disabled	Disabled	30V	**10mA (Fan-in)**	6.7s	12mA
5V	512Ω / 9.8mA	Disabled	Disabled	20V	**10mA (Fan-in)**	2.7s	12mA
Disabled	VDD_REGIN= VDDHV	**1V**	10Ω / 96mA	30V	6.2mA	5.9s	16mA (hold-up = 22mA)
Disabled	VDD_REGIN= VDDHV	**1V**	10Ω / 96mA	20V	**10mA (Fan-in)**	2.5s	16mA (hold-up = 22mA)
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	30V	2.7mA	4.7s	9.4mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	20V	4mA	5s	9.1mA
Disabled	VCCORE= VDCDC	**3.3V**	102Ω / 33mA	30V	6.3mA	6s	15mA (hold-up = 20mA)
Disabled	VCCORE= VDCDC	**3.3V**	102Ω / 33mA	20V	10mA (Fan-in)	2.4s	15mA (hold-up = 20mA)
Disabled	VCCORE= VDCDC	**5V**	220Ω / 23mA	30V	6.4mA	6s	16mA (hold-up = 21mA)
Disabled	VCCORE= VDCDC	**5V**	220Ω / 23mA	20V	10mA (Fan-in)	2.6s	16mA (hold-up = 21mA)
Enabled	VDD_REGIN= VDDHV	12V	1.35Ω / 9mA	30V	5.8mA	5.8s	12mA
Enabled	VDD_REGIN= VDDHV	12V	1.35Ω / 9mA	20V	10mA (Fan-in)	2.8s	12mA
				Cumulative result	PASS		

1. *When exceeding the max. current during start-up time, the max. current during hold-up time is reported but is not subject to any limit.*

4.3.2.1 *Linear regulator 3.3 V waveforms (loaded to reach fan-in limit)*

Note: *Note: The default configuration of the kit cannot be tested with fan-in 10 mA because the total consumption of the kit is 12 mA when the CPU section is supplied by the STKNX linear regulator.*

The linear regulator set to 3.3 V is supplied from VDDHV and loaded with 347 Ω/9.6 mA for a KNX bus consumption of 10 mA at 30 V. The DC-DC converter is disabled.

Figure 65. Upsu = 30V (IinDC = 10mA)

Tstart-up = 6.8s	Limit = 10s	Tstart-up = 2.8s	Limit = 10s
Iin max = 12mA	Limit = 30mA	Iin max = 12mA	Limit = 30mA

Figure 66. Upsu = 20V (IinDC = 10mA)

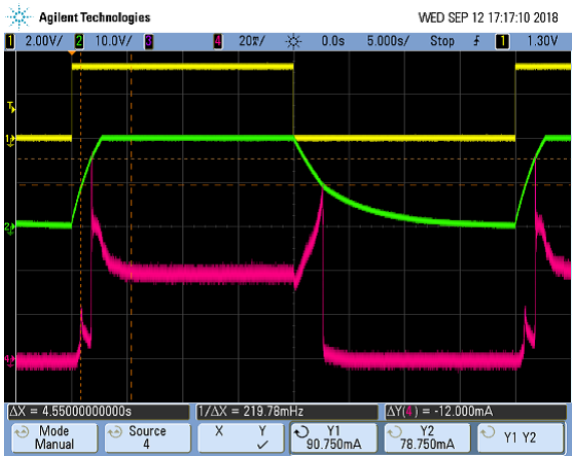
4.3.2.2 *DC-DC converter 3.3 V waveforms (loaded with kit)*

The DC-DC converter set to 3.3 V is supplying the kit (3V3_KIT) with a 12 mA current. The linear regulator is disabled and VCCCORE is supplied with VDCDC.

Figure 67. Upsu = 30V (IinDC = 2.7mA)

Tstart-up = 4.7s	Limit = 10s	Tstart-up = 5s	Limit = 10s
Iin max = 10mA(1)	Limit = 30mA	Iin max = 10mA(1)	Limit = 30mA

Figure 68. Upsu = 20V (IinDC = 4mA)



1. *The current during hold-up is higher than during startup but remains under start-up limit. No specification exists yet for hold-up current.*

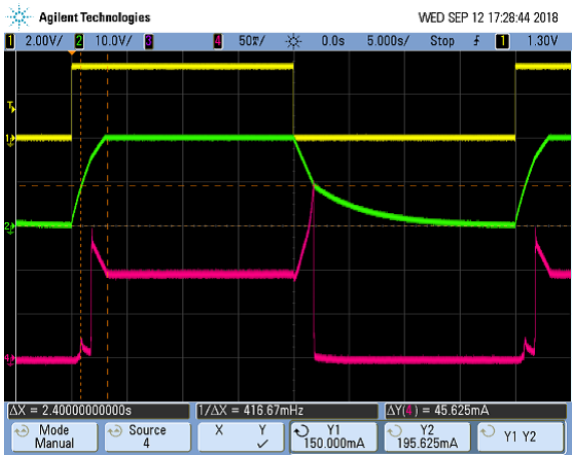
4.3.2.3 *DC-DC converter 3.3 V waveforms (loaded to reach fan-in limit)*

The DC-DC converter set to 3.3 V is loaded with 102 Ω/33 mA for a KNX bus consumption of 10 mA at 20 V. The linear regulator is disabled and VCCCORE is supplied with VDCDC.

Figure 69. Upsu = 30V (IinDC = 6.3mA)

Tstart-up = 6s	Limit = 10s
Iin max = 15mA(1)	Limit = 30mA

Figure 70. Upsu = 20V (IinDC = 10mA)



Tstart-up = 2.4s	Limit = 10s
Iin max = 15mA(1)	Limit = 30mA

1. *The current during hold-up is higher than during startup but remains under start-up limit. No specification exits yet for hold-up current.*

4.3.2.4 *DC-DC converter 12 V waveforms (loaded to reach fan-in limit)*

The DC-DC converter set to 12 V is loaded with 1.35 kΩ/9 mA for a KNX bus consumption of 10 mA at 20 V. The linear regulator is enabled, not loaded and supplied from VDCDC.

Figure 71. Upsu = 30V (IinDC = 5.8mA)

Tstart-up = 5.8s	Limit = 10s
Iin max = 12mA	Limit = 30mA

Figure 72. Upsu = 20V (IinDC = 10mA)

Tstart-up = 2.8s	Limit = 10s
Iin max = 12mA	Limit = 30mA

4.3.3 Tests results - fan-in = 30 mA

Test settings:

- R_K = 1 kΩ / 3
- C_K = 3 x 4.7 mF
- I_{limit} = 150 mA.

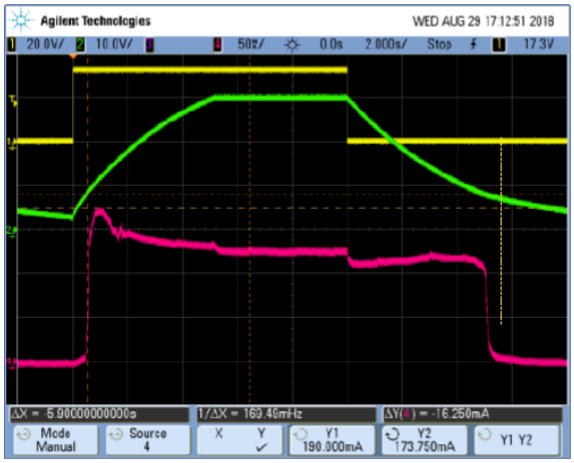
Table 5. Switch On/Off Slow tests results - fan-in = 30mA

EVALKITSTKNX configuration				Test conditions		Test results	
Linear Reg		DC-DC converter		Upsu	Iin DC	Tstartup (Limit = 10s)	Iin max. (Limit = 90mA)
Voltage	Load	Voltage	Load				
3.3V	**Kit / 12mA**	5V	NO	30V	13mA	5.9s	18mA
3.3V	**Kit / 12mA**	5V	NO	20V	13mA	4s	18mA
3.3V	**20mA (max.)**	Disabled	Disabled	30V	21mA	5.6s	24mA
3.3V	**20mA (max.)**	Disabled	Disabled	20V	21mA	2.3s	24mA
5V	**20mA (max.)**	Disabled	Disabled	30V	21mA	5.1s	23mA
5V	**20mA (max.)**	Disabled	Disabled	20V	21mA	1.9s	24mA
Disabled	VDD_REGIN= VDDHV	**1V**	7Ω / 150mA **(max.)**	30V	13mA	4.7s	31mA (hold-up = 38mA)
Disabled	VDD_REGIN= VDDHV	**1V**	7Ω / 150mA **(max.)**	20V	21mA	2s	8.5mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	30V	2.8mA	4.2s	8.5mA
Disabled	VCCORE= VDCDC	**3.3V**	**Kit / 12mA**	20V	3.9mA	4.8s	15mA (hold-up = 20mA)
Disabled	VCCORE= VDCDC	**3.3V**	33Ω / 100mA	30V	19mA	5.3s	43mA (hold-up = 60mA)
Disabled	VCCORE= VDCDC	**5V**	33Ω / 100mA	20V	**30mA (Fan-in)**	2.1s	43mA (hold-up = 60mA)
Disabled	VCCORE= VDCDC	**5V**	74Ω / 69mA	30V	19mA	5.2s	44mA (hold-up = 59mA)
Disabled	VCCORE= VDCDC	**5V**	74Ω / 69mA	20V	**30mA (Fan-in)**	1.9s	44mA (hold-up = 59mA)
Enabled	VDD_REGIN= VDDHV	**12V**	404Ω / 31mA	30V	19mA	5.3s	33mA
Enabled	VDD_REGIN= VDDHV	**12V**	404Ω / 31mA	20V	**30mA (Fan-in)**	2s	33mA
				Cumulative result		PASS	

4.3.3.1 *Default kit configuration waveforms*

This configuration is described in Section 3.5.4.1 STKNX mode DC-DC 5 V (default). The linear regulator 3.3 V is supplying the kit (3V3_KIT) and the 5 V DC-DC converter is not loaded.

Figure 73. Upsu = 30V (IinDC = 12.5mA)



Tstart-up = 5.9s	Limit = 10s
Iin max = 17.4mA	Limit = 90mA

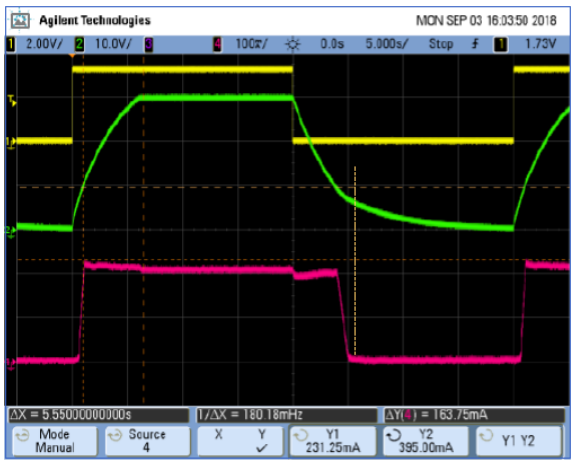
Figure 74. Upsu = 20V (IinDC = 12.4mA)

Tstart-up = 4s	Limit = 10s
Iin max = 17.5mA	Limit = 90mA

4.3.3.2 *Linear regulator 3.3 V waveforms (load = 20 mA)*

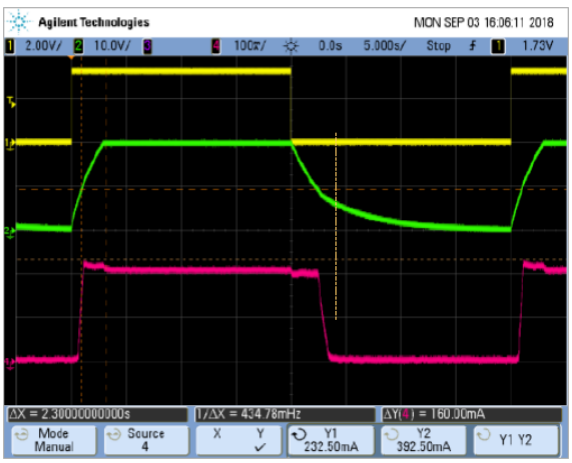
The linear regulator set to 3.3 V is loaded with 169 Ω and is supplying its maximum current of 20 mA. The DC-DC converter is disabled.

Figure 75. Upsu = 30V (IinDC = 20.7mA)



Tstart-up = 5.6s	Limit = 10s
Iin max = 23.1mA	Limit = 90mA

Figure 76. Upsu = 20V (IinDC = 20.7mA)



Tstart-up = 2.3s	Limit = 10s
Iin max = 23.2mA	Limit = 90mA

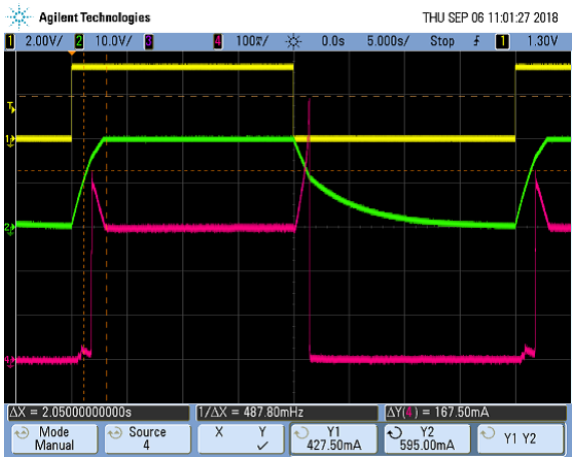
4.3.3.3 *DC-DC converter 3.3 V waveforms (loaded to reach fan-in limit)*

The DC-DC converter set to 3.3 V is loaded with 33 Ω/100 mA for a KNX bus consumption of 30 mA at 20 V. The linear regulator is disabled and VCCCORE is supplied with VDCDC.

Figure 77. Upsu = 30V (IinDC = 18.5mA)

Tstart-up = 5.3s	Limit = 10s
Iin max = 42.5mA(1)	Limit = 90mA

Figure 78. Upsu = 20V (IinDC = 30mA)



Tstart-up = 2.1s	Limit = 10s
Iin max = 42.8mA(1)	Limit = 90mA

1. *The current during hold-up is higher than during startup but remains under start-up limit. No specification exits yet for hold-up current.*

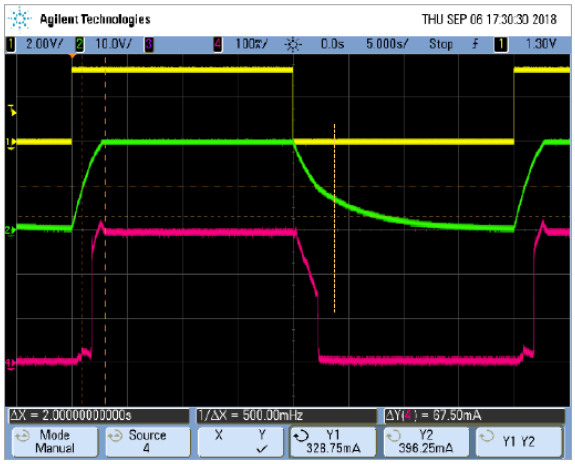
4.3.3.4 *DC-DC converter 12 V waveforms*

The DC-DC converter set to 12 V is loaded with 404 Ω/30.4 mA for a KNX bus consumption of 30 mA at 20 V. The linear regulator is enabled, not loaded and supplied from VDCDC.

Figure 79. Upsu = 30V (IinDC = 18.7mA)

Tstart-up = 5.3s	Limit = 10s
Iin max = 33mA	Limit = 90mA

Figure 80. Upsu = 20V (IinDC = 30mA)



Tstart-up = 2s	Limit = 10s
Iin max = 33mA	Limit = 90mA

4.4 Power Conversion (Load Changes) (8/2/2 - test 4.4)

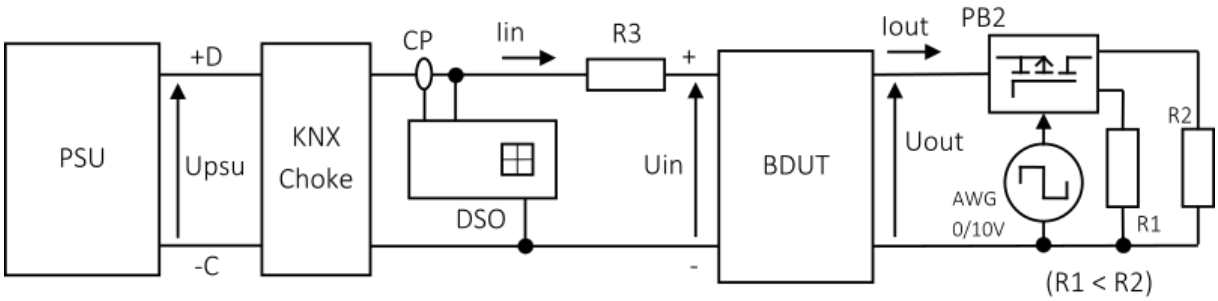
Switching from minimal to maximal load and vice versa simulates the changing of load.

A steep slope of the output current (Iout) has to be transferred to a controlled flat slope of the input current (Iin).

The input current slope measured in this section is controlled by the capacitor Cgate, which should be chosen according to the guidelines described in Section 3.2.1 Electrical description.

4.4.1 Test setup

Figure 81. **Load Changes test setup**



- Oscilloscope channels:
  - CH1: BP2 command
  - CH2: Uin
  - CH3: BDUT regulator voltage output Uout
  - CH4: Iin
- Function generator period: 30 s; active pulse width = 1 s.

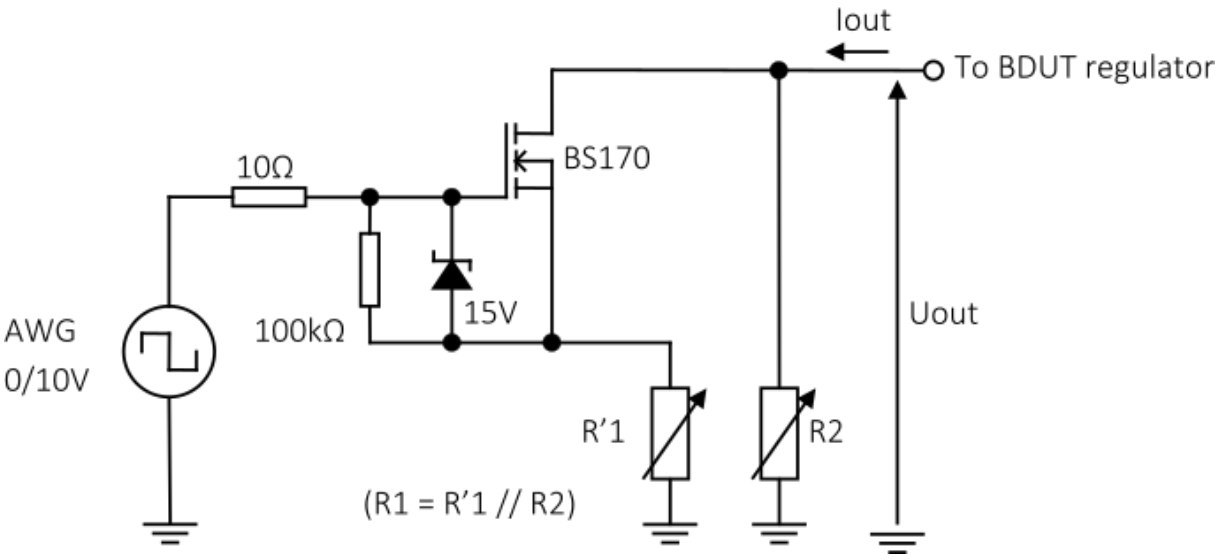
During the tests in this section, unless otherwise specified:

- R1 is tuned to sink the maximum load, adjusted to achieve Iin fan-in when Upsu = 20 V
- R2 is tuned to sink the minimum load adjusted to keep Iin peak under maximum limit (12 mA x fan-in) at load transition from R2 to R1
- Every “isolation” jumper (between KNX section and CPU section) is removed
- Embedded FW: EvalKitSTKNX_LedLevel_V1.0.bin (see Section 4.1 General test setup).

4.4.1.1 *PB2 description*

The debounced push button is replaced by a MOSFET based circuit described in which allows making repetitive tests.

Figure 82. **MOSFET circuit for load switching**



When the AWG applies a 10 V voltage, the MOSFET transistor is conducting and the load applied to the BDUT regulator is R1 = R'1 // R2

When the AWG signal is 0 V, the impedance applied to BDUT is R2.

4.4.2 Tests results - fan-in = 10 mA

Test settings:

- R3 = 100 Ω

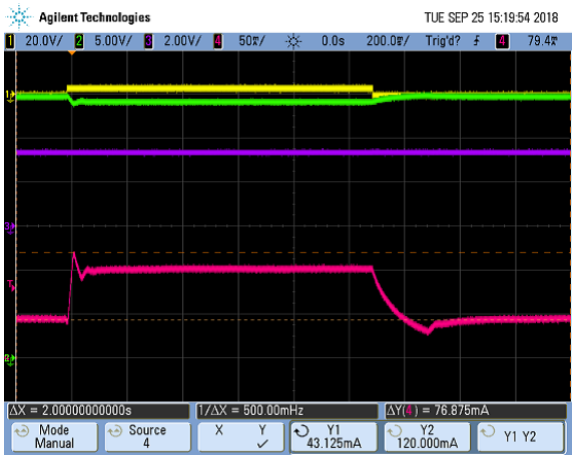
Table 6. Load Changes tests results - fan-in = 10 mA

EVALKITSTKNX configuration		Test conditions					Test results		
Linear regulator	DC-DC converter	Upsu	Iin DC max.	Iin DC min.	Iout DC max.	Iout DC min.	Iin overshoot max. (Limit = 12mA)	Iin rising slope max. (Limit = 0.5mA/ms)	Iin falling slope max. (Limit = 0.5mA/ms)
3.3V	Disabled	30V	**10mA**	4.2mA	9.8mA	4.5mA	**12mA**	0.42mA/ms	0.08mA/ms
3.3V	Disabled	20V	**10mA**	5.4mA	9.7mA	5.1mA	**12mA**	0.42mA/ms	0.09mA/ms
5V	Disabled	30V	**10mA**	4mA	9.4mA	3.6mA	**12mA**	0.39mA/ms	0.08mA/ms
5V	Disabled	20V	**10mA**	4.6mA	9.4mA	4.3mA	**12mA**	0.4mA/ms	0.01mA/ms
Disabled VDD_REGIN= VDDHV	**1V**	30V	6.3mA	3mA	88mA	38mA	7mA	0.23mA/ms	0.05mA/ms
Disabled VDD_REGIN= VDDHV	**1V**	20V	**10mA**	4.5mA	87mA	37mA	**12mA**	0.42mA/ms	0.09mA/ms
Disabled VCCORE= VDCDC	**3.3V**	30V	6.3mA	3.4mA	33mA	17mA	7mA	0.21mA/ms	0.05mA/ms
Disabled VCCORE= VDCDC	**3.3V**	20V	**10mA**	5mA	33mA	17mA	**12mA**	0.43mA/ms	0.11mA/ms
Disabled VCCORE= VDCDC	**5V**	30V	6.3mA	2.3mA	22mA	7mA	7mA	0.26mA/ms	0.05mA/ms
Disabled VCCORE= VDCDC	**5V**	20V	**10mA**	3mA	22mA	7mA	**12mA**	0.39mA/ms	0.09mA/ms
Enabled VDD_REGIN= VDCDC	**12V**	30V	6.3mA	3mA	9.2mA	3mA	7mA	0.14mA/ms	0.05mA/ms
Enabled VDD_REGIN= VDCDC	**12V**	20V	**10mA**	4mA	9.2mA	3mA	**12mA**	0.26mA/ms	0.09mA/ms
		Cumulative results	PASS						

4.4.2.1 *Linear regulator 3.3 V waveforms*

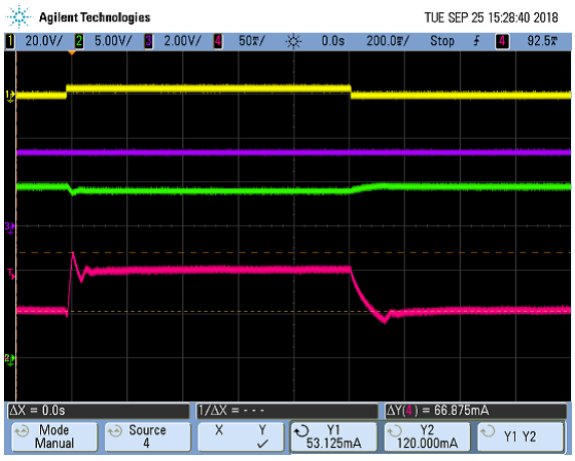
The linear regulator set to 3.3 V is supplied from VDDHV. The DC-DC converter is disabled.

Figure 83. Upsu = 30V



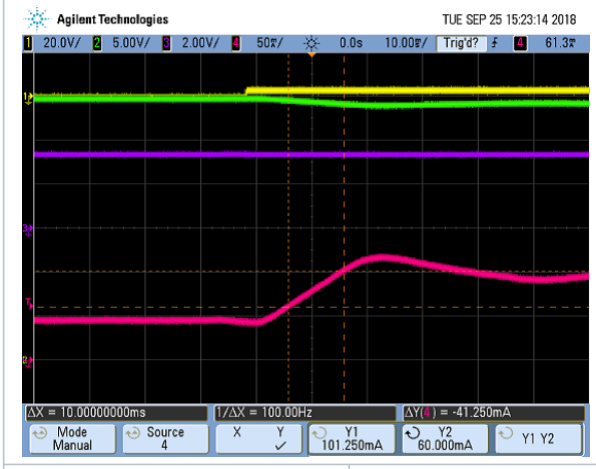
Iin max = 10mA Iin min = 4.2mA	Iout max = 9.8mA Iout min = 4.5mA
Iin max (overshoot) = 12mA	Limit = 12mA

Figure 84. Upsu = 20V



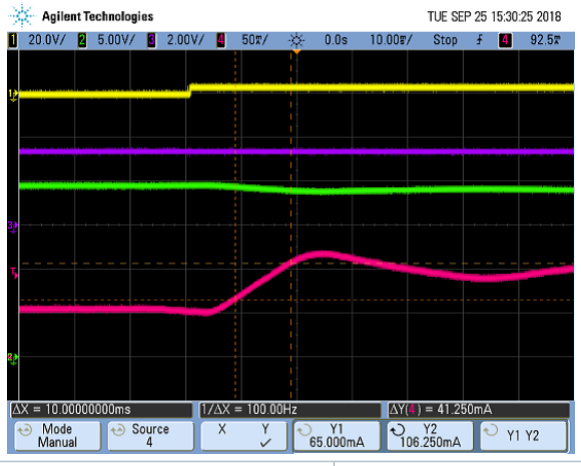
Iin max = 10mA Iin min = 5.4mA	Iout max = 9.7mA Iout min = 5.1mA
Iin max (overshoot) = 12mA	Limit = 12mA

Figure 85. Upsu = 30V



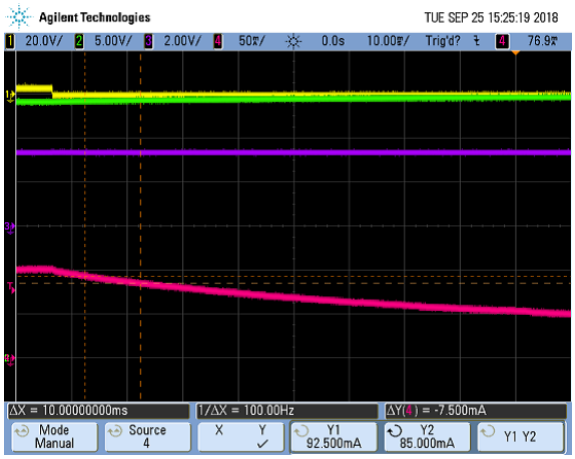
Rising slope = 0.42mA/ms	Limit = 0.5mA/ms

Figure 86. Upsu = 20V



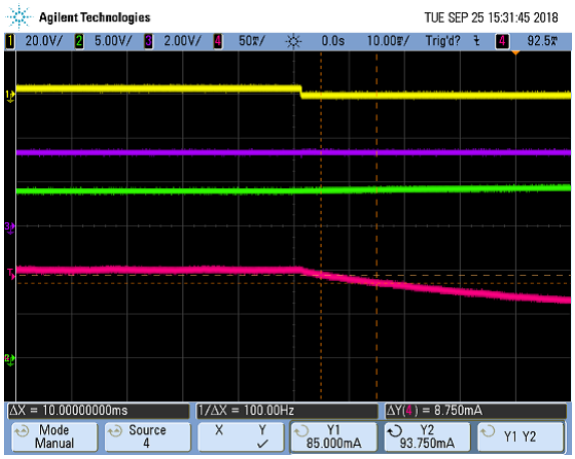
Rising slope = 0.42mA/ms	Limit = 0.5mA/ms

Figure 87. Upsu = 30V



Rising slope = 0.08mA/ms	Limit = 0.5mA/ms

Figure 88. Upsu = 20V



Rising slope = 0.09mA/ms	Limit = 0.5mA/ms

4.4.2.2 *DC-DC converter 1 V waveforms*

The DC-DC converter is enabled and tuned to 1 V output voltage. The linear regulator is enabled (3.3 V) for STKNX I/Os and supplied from VDDHV.

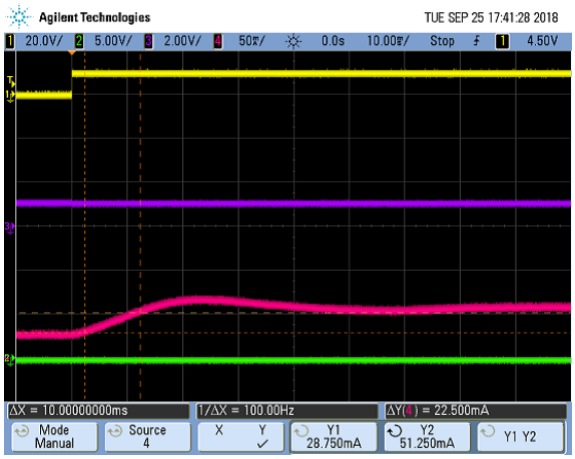
Figure 89. Upsu = 30V

Iin max = 6.3mA Iin min = 3mA	Iout max = 88mA Iout min = 38mA
Iin max (overshoot) = 7mA	Limit = 12mA

Figure 90. Upsu = 20V

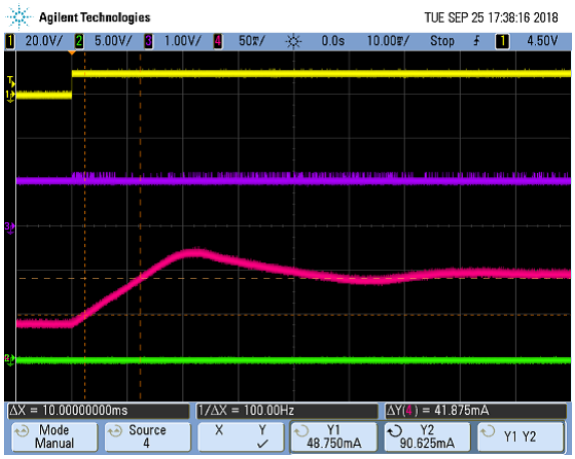
Iin max = 10mA Iin min = 4.5mA	Iout max = 87mA Iout min = 37mA
Iin max (overshoot) = 12mA	Limit = 12mA

Figure 91. Upsu = 30V



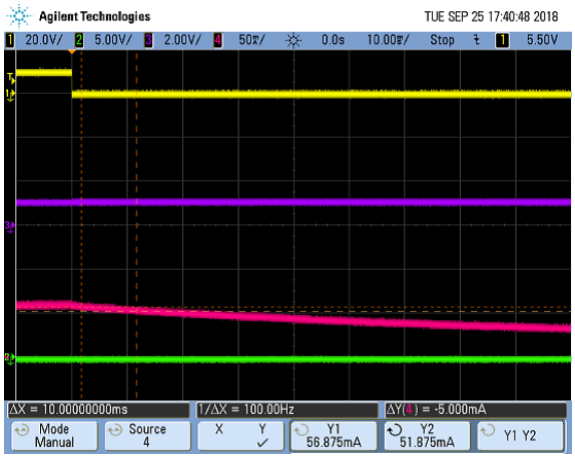
Rising slope = 0.23mA/ms | Limit = 0.5mA/ms

Figure 92. Upsu = 20V



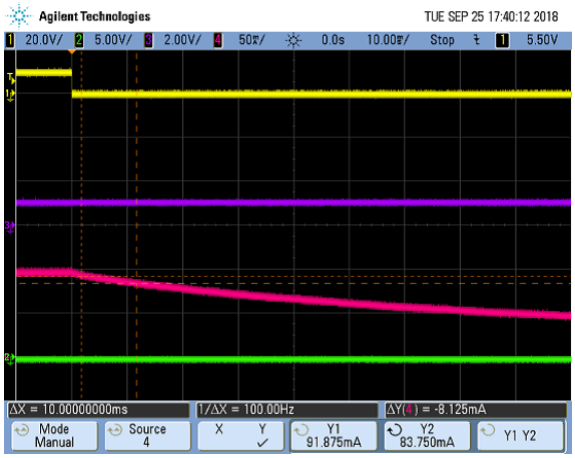
Rising slope = 0.42mA/ms | Limit = 0.5mA/ms

Figure 93. Upsu = 30V



Rising slope = 0.05mA/ms | Limit = 0.5mA/ms

Figure 94. Upsu = 20V

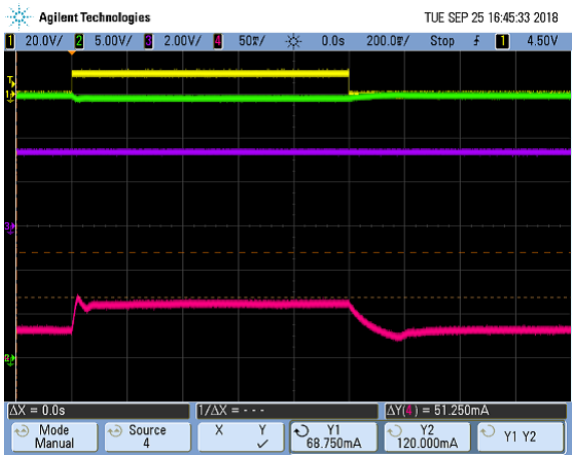


Rising slope = 0.09mA/ms | Limit = 0.5mA/ms

4.4.2.3 *DC-DC converter 3.3 V waveforms*

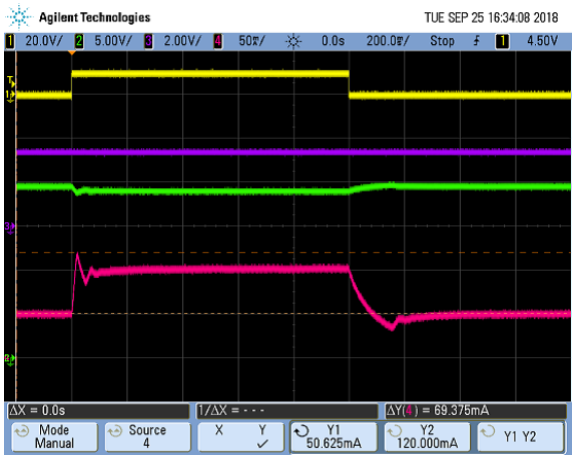
The DC-DC converter is enabled and tuned to 3.3 V output voltage. The linear regulator is disabled and VCCCORE is connected to VDCDC for STKNX I/Os supply.

Figure 95. Upsu = 30V



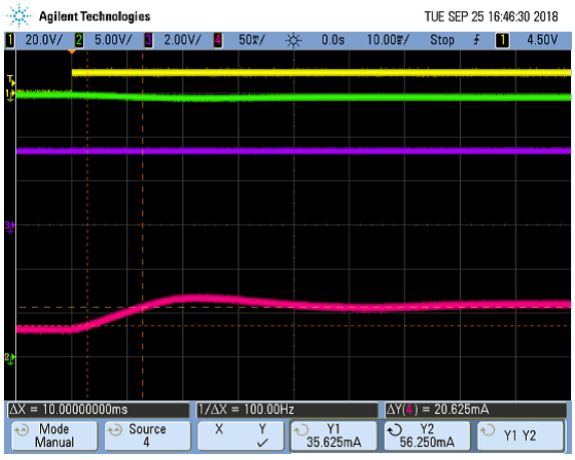
Iin max = 6.3mA Iin min = 3.4mA	Iout max = 33mA Iout min = 17mA
Iin max (overshoot) = 7mA	Limit = 12mA

Figure 96. Upsu = 20V



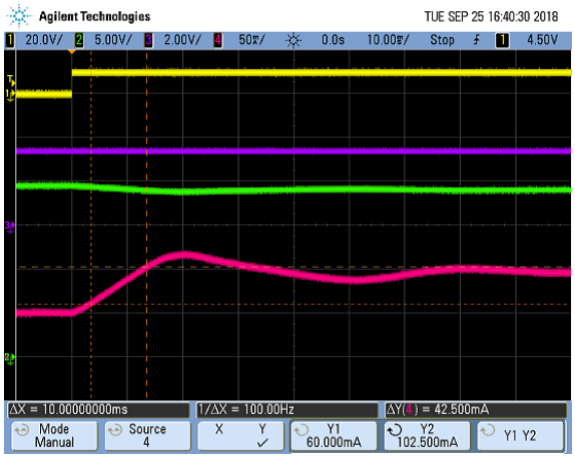
Iin max = 10mA Iin min = 5mA	Iout max = 33mA Iout min = 17mA
Iin max (overshoot) = 12mA	Limit = 12mA

Figure 97. Upsu = 30V



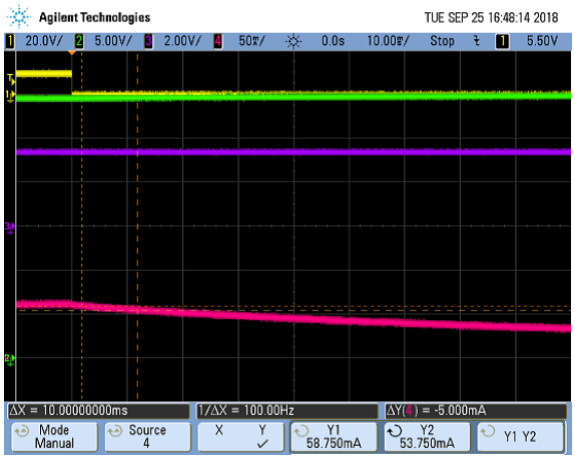
Rising slope = 0.21mA/ms	Limit = 0.5mA/ms

Figure 98. Upsu = 20V



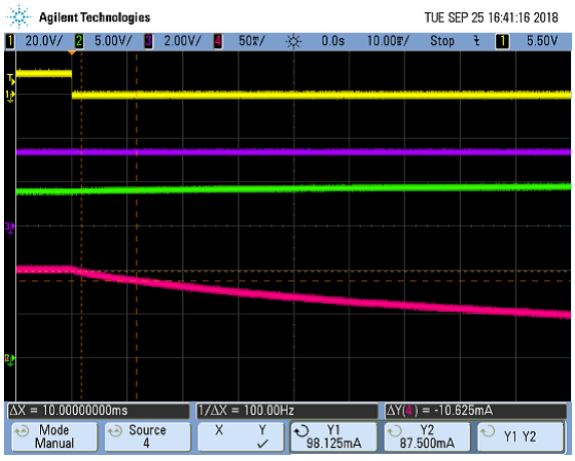
Rising slope = 0.43mA/ms	Limit = 0.5mA/ms

Figure 99. Upsu = 30V



Rising slope = 0.05mA/ms	Limit = 0.5mA/ms

Figure 100. Upsu = 20V



Rising slope = 0.11mA/ms	Limit = 0.5mA/ms

4.4.2.4 *DC-DC converter 12 V waveforms*

The DC-DC converter is enabled and tuned to 12 V output voltage. The linear regulator is enabled (3.3 V) for STKNX I/Os and supplied from VDCDC.

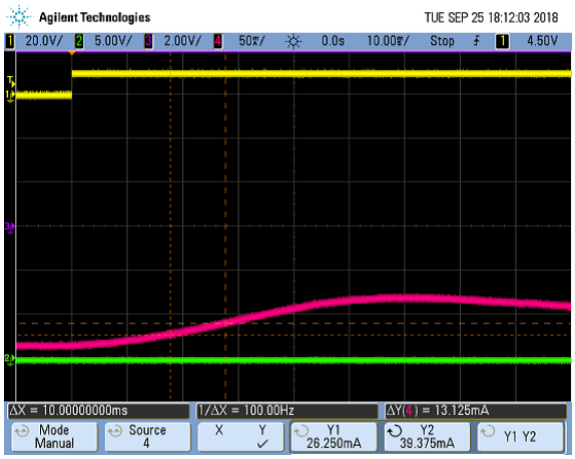
Figure 101. Upsu = 30V

Iin max = 6mA Iin min = 3mA	Iout max = 9.2mA Iout min = 3mA
Iin max (overshoot) = 7mA	Limit = 12mA

Figure 102. Upsu = 20V

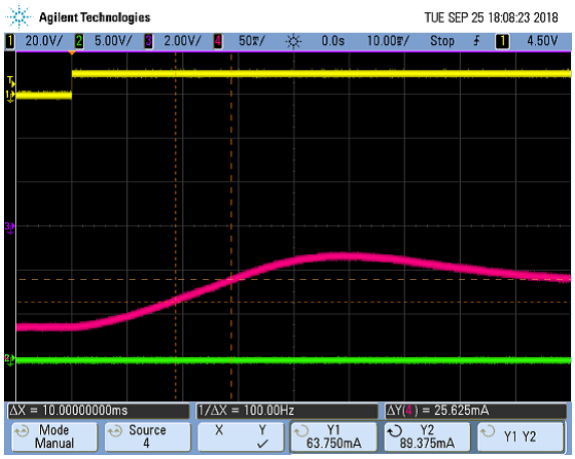
Iin max = 10mA Iin min = 4mA	Iout max = 9.2mA Iout min = 3mA
Iin max (overshoot) = 12mA	Limit = 12mA

Figure 103. Upsu = 30V



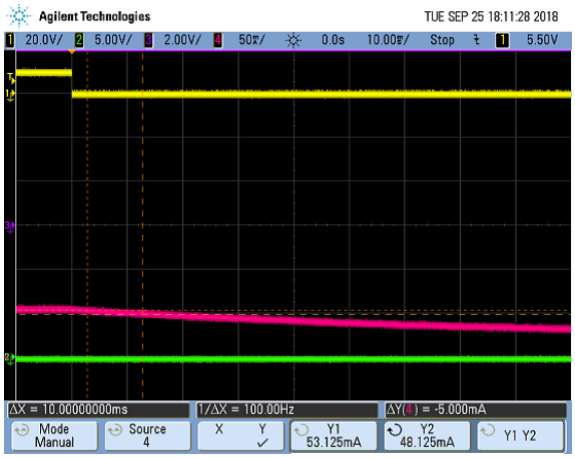
Rising slope = 0.14mA/ms | Limit = 0.5mA/ms

Figure 104. Upsu = 20V



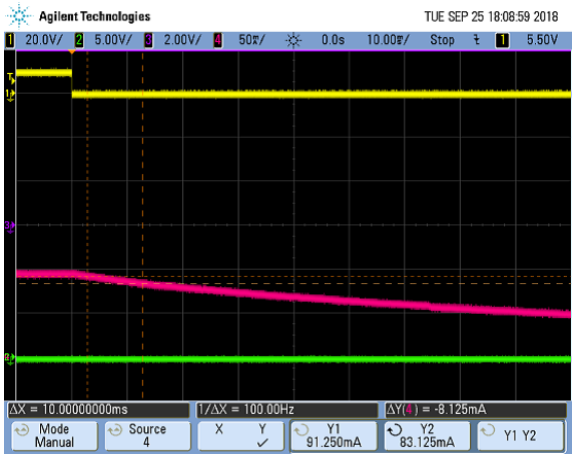
Rising slope = 0.26mA/ms | Limit = 0.5mA/ms

Figure 105. Upsu = 30V



Rising slope = 0.05mA/ms | Limit = 0.5mA/ms

Figure 106. Upsu = 20V



Rising slope = 0.09mA/ms | Limit = 0.5mA/ms

4.4.3 Tests results - fan-in = 30 mA

Test settings:

- R3 = 33 Ω

Table 7. Load Changes tests results - fan-in = 30 mA

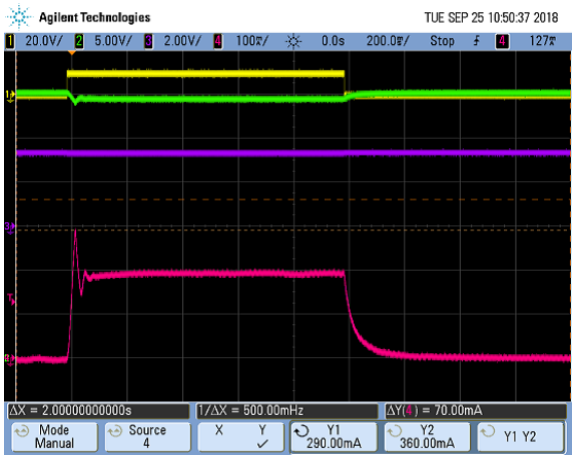
EVALKITSTKNX configuration		Test conditions					Test results		
Linear regulator	DC-DC converter	Upsu	Iin DC max	Iin DC min	Iout DC max	Iout DC min	Iin overshoot max. (Limit = 36mA)	Iin rising slope max. (Limit = 1.5mA/ms)	Iin falling slope max. (Limit = 1.5mA/ms)
3.3V	Disabled	30V	20.4mA	0.3mA	**20mA**	0mA	29mA	1.28mA/ms	0.48mA/ms
3.3V	Disabled	20V	20.4mA	0.3mA	**20mA**	0mA	30mA	1.22mA/ms	0.48mA/ms

EVALKITSTKNX configuration		Test conditions					Test results		
Linear regulator	DC-DC converter	Upsu	Iin DC max	Iin DC min	Iout DC max	Iout DC min	Iin overshoot max. (Limit = 36mA)	Iin rising slope max. (Limit = 1.5mA/ms)	Iin falling slope max. (Limit = 1.5mA/ms)
5V	Disabled	30V	20.4mA	0.4mA	**20mA**	0mA	30mA	1.27mA/ms	0.5mA/ms
5V	Disabled	20V	20.4mA	0.4mA	**20mA**	0mA	32mA	1.2mA/ms	0.5mA/ms
Disabled VDD_REGIN= VDDHV	**1V**	30V	11mA	0.4mA	**150mA**	0mA	22mA	1.14mA/ms	0.25mA/ms
Disabled VDD_REGIN= VDDHV	**1V**	20V	18mA	0.4mA	**150mA**	0mA	24mA	1.2mA/ms	0.39mA/ms
Disabled VCCORE= VDCDC	**3.3V**	30V	18mA	5mA	98mA	27mA	22mA	1.19mA/ms	0.4mA/ms
Disabled VCCORE= VDCDC	**3.3V**	20V	**30mA**	8mA	98mA	27mA	**36mA**	1.27mA/ms	0.78mA/ms
Disabled VCCORE= VDCDC	**5V**	30V	17mA	5mA	66mA	19mA	22mA	1.17mA/ms	0.42mA/ms
Disabled VCCORE= VDCDC	**5V**	20V	**30mA**	8mA	65mA	19mA	**36mA**	1.3mA/ms	0.86mA/ms
Enabled VDD_REGIN= VDCDC	**12V**	30V	18mA	4mA	30mA	6mA	22mA	1.22mA/ms	0.43mA/ms
Enabled VDD_REGIN= VDCDC	**12V**	20V	**30mA**	7mA	30mA	6mA	**36mA**	1.27mA/ms	0.83mA/ms
		Cumulative results					PASS		

4.4.3.1 *Linear regulator 3.3 V waveforms*

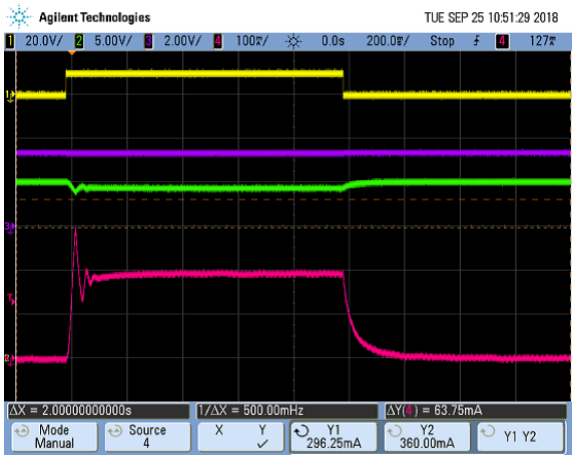
The linear regulator set to 3.3 V is supplied from VDDHV. The load R1 is configured to sink Iout = 20 mA which is the limit of the linear regulator. The DC-DC converter is disabled.

Figure 107. Upsu = 30V



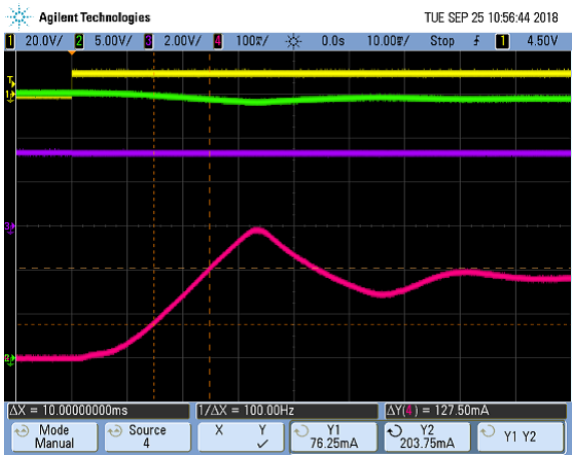
Iin max = 20.4mA Iin min = 0.3mA	Iout max = 20mA Iout min = 0mA
Iin max (overshoot) = 29mA	Limit = 36mA

Figure 108. Upsu = 20V



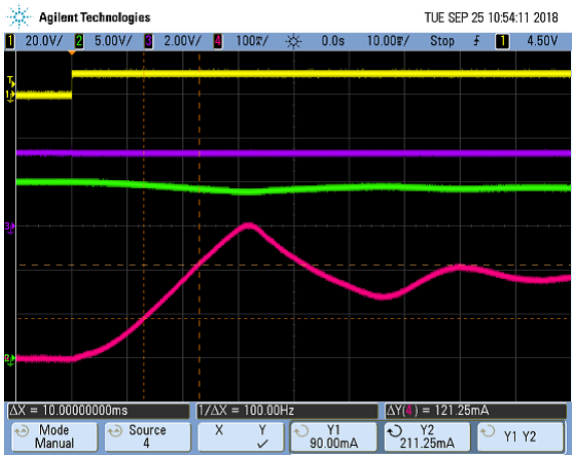
Iin max = 20.4mA Iin min = 0.3mA	Iout max = 20mA Iout min = 0mA
Iin max (overshoot) = 30mA	Limit = 36mA

Figure 109. Upsu = 30V



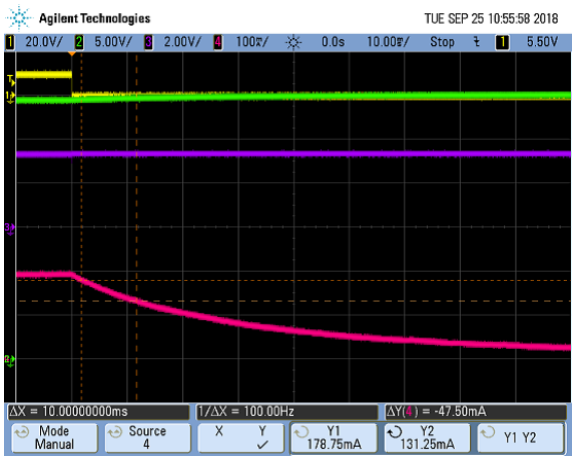
Rising slope = 1.28mA/ms	Limit = 1.5mA/ms

Figure 110. Upsu = 20V



Rising slope = 1.22mA/ms	Limit = 1.5mA/ms

Figure 111. Upsu = 30V



Rising slope = 0.48mA/ms	Limit = 1.5mA/ms

Figure 112. Upsu = 20V

Rising slope = 0.48mA/ms	Limit = 1.5mA/ms

4.4.3.2 *DC-DC converter 1 V waveforms*

The DC-DC converter is enabled and tuned to 1 V output voltage. The load R1 is configured to sink Iout = 150 mA which is the limit of the linear regulator. It is therefore not possible to reach Iin = 30 mA (fan-in) @ Uin = 20 V on the bus but only 18 mA. The linear regulator is enabled (3.3 V) for STKNX I/Os and supplied from VDDHV.

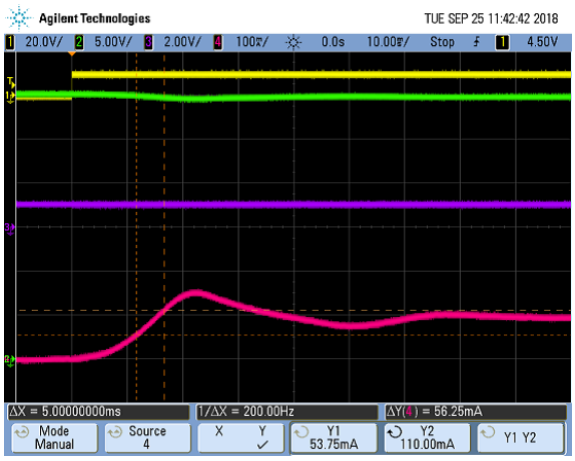
Figure 113. Upsu = 30V

Iin max = 11mA Iin min = 0.4mA	Iout max = 150mA Iout min = 0mA
Iin max (overshoot) = 22mA	Limit = 36mA

Figure 114. Upsu = 20V

Iin max = 18mA Iin min = 0.4mA	Iout max = 150mA Iout min = 0mA
Iin max (overshoot) = 24mA	Limit = 36mA

Figure 115. Upsu = 30V

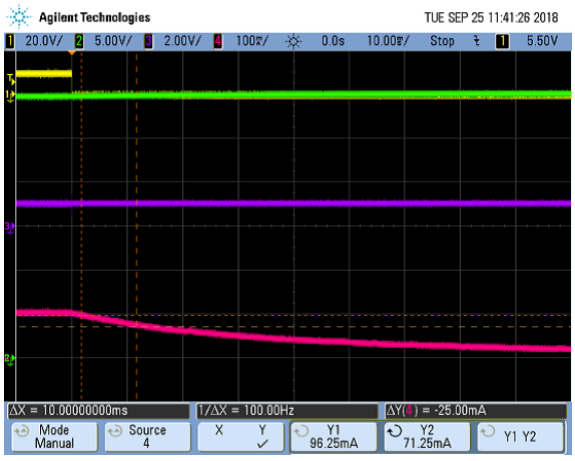


Rising slope = 1.14mA/ms	Limit = 1.5mA/ms

Figure 116. Upsu = 20V

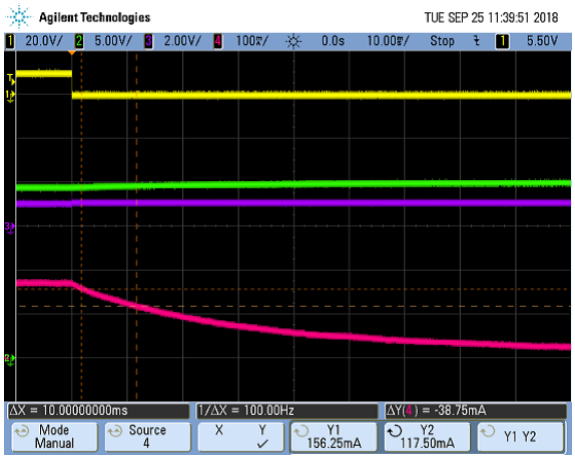
Rising slope = 1.2mA/ms	Limit = 1.5mA/ms

Figure 117. Upsu = 30V



Rising slope = 0.25mA/ms	Limit = 1.5mA/ms

Figure 118. Upsu = 20V

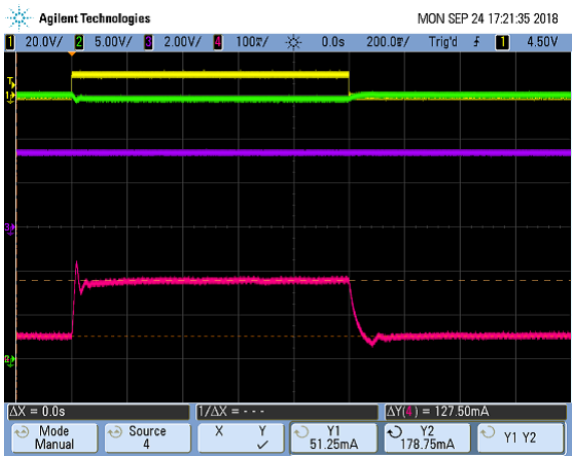


Rising slope = 0.39mA/ms	Limit = 1.5mA/ms

4.4.3.3 *DC-DC converter 3.3 V waveforms*

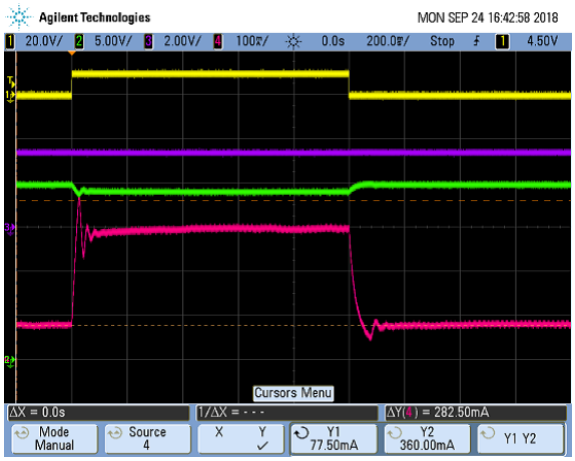
The DC-DC converter is enabled and tuned to 3.3 V output voltage. The linear regulator is disabled and VCCCORE is connected to VDCDC for STKNX I/Os supply.

Figure 119. Upsu = 30V



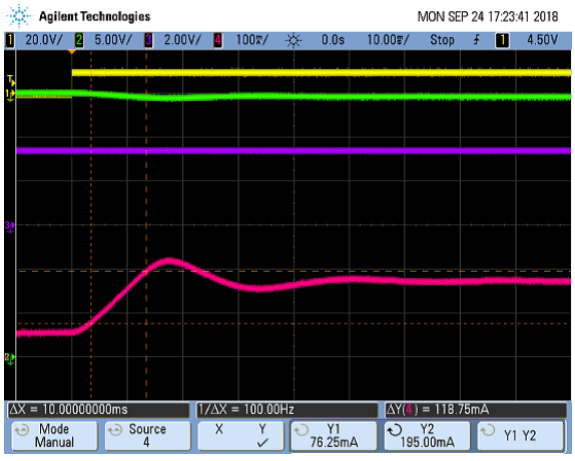
Iin max = 18mA Iin min = 5mA	Iout max = 98mA Iout min = 27mA
Iin max (overshoot) = 22mA	Limit = 36mA

Figure 120. Upsu = 20V



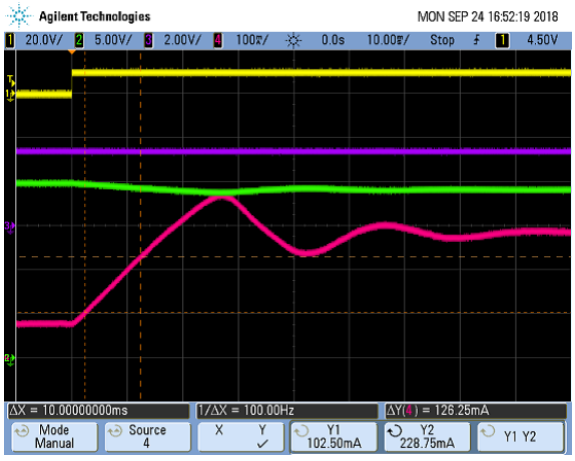
Iin max = 30mA Iin min = 8mA	Iout max = 98mA Iout min = 27mA
Iin max (overshoot) = 36mA	Limit = 36mA

Figure 121. Upsu = 30V



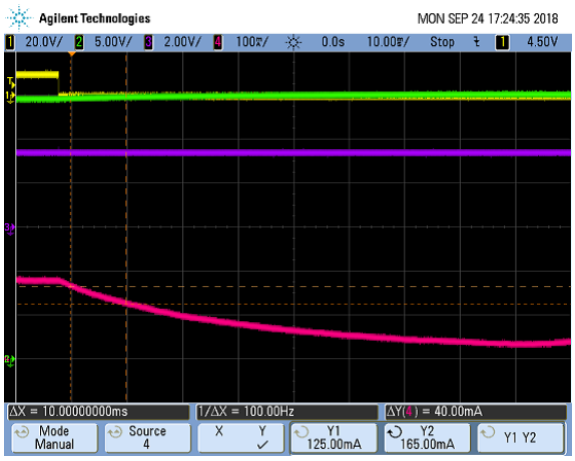
Rising slope = 1.19mA/ms	Limit = 1.5mA/ms

Figure 122. Upsu = 20V



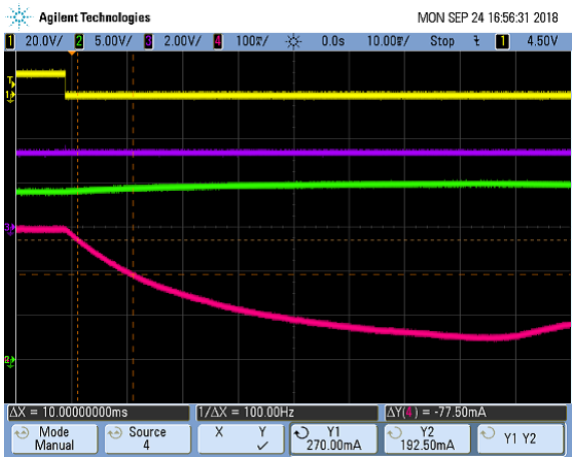
Rising slope = 1.27mA/ms	Limit = 1.5mA/ms

Figure 123. Upsu = 30V



Rising slope = 0.4mA/ms	Limit = 1.5mA/ms

Figure 124. Upsu = 20V



Rising slope = 0.78mA/ms	Limit = 1.5mA/ms

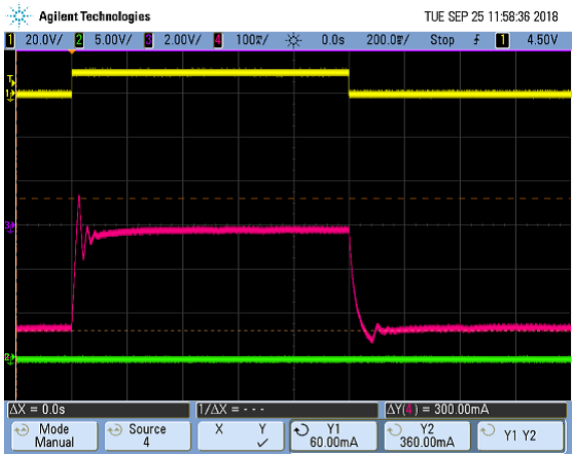
4.4.3.4 *DC-DC converter 12 V waveforms*

The DC-DC converter is enabled and tuned to 12 V output voltage. The linear regulator is enabled (3.3 V) for STKNX I/Os and supplied from VDCDC.

Figure 125. Upsu = 30V

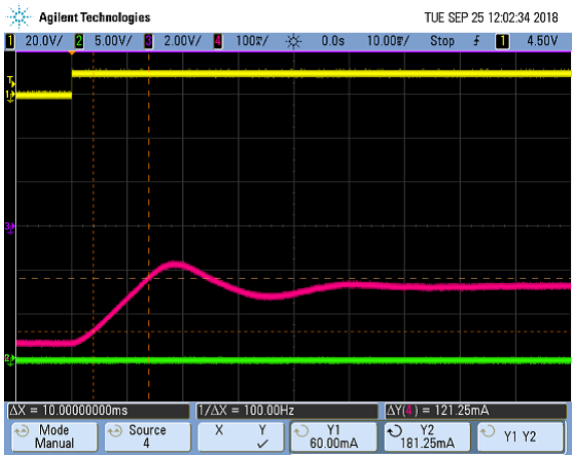
Iin max = 18mA Iin min = 4mA	Iout max = 30mA Iout min = 6mA
Iin max (overshoot) = 22mA	Limit = 36mA

Figure 126. Upsu = 20V



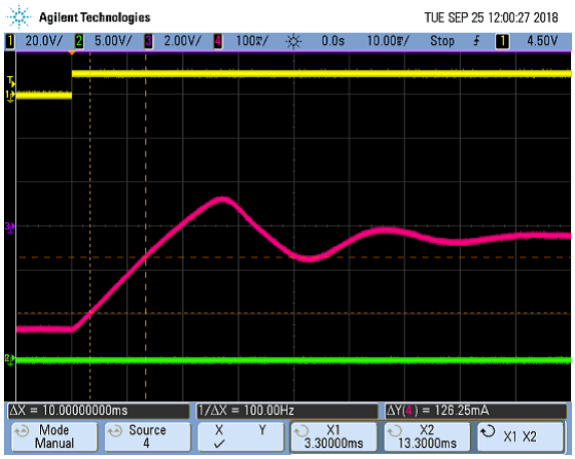
Iin max = 30mA Iin min = 7mA	Iout max = 30mA Iout min = 6mA
Iin max (overshoot) = 36mA	Limit = 36mA

Figure 127. Upsu = 30V



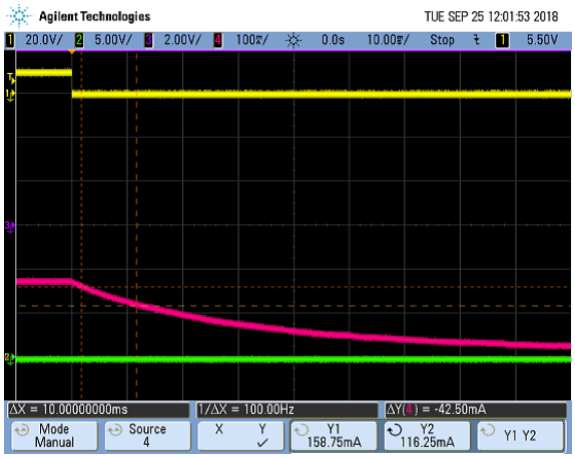
Rising slope = 1.22mA/ms | Limit = 1.5mA/ms

Figure 128. Upsu = 20V



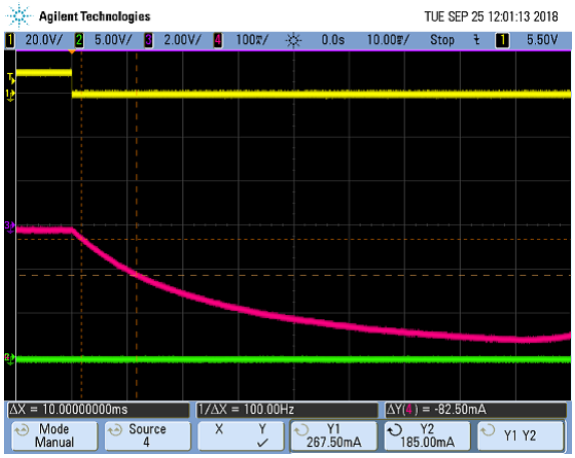
Rising slope = 1.27mA/ms | Limit = 1.5mA/ms

Figure 129. Upsu = 30V



Rising slope = 0.43mA/ms | Limit = 1.5mA/ms

Figure 130. Upsu = 20V



Rising slope = 0.83mA/ms | Limit = 1.5mA/ms

4.5 Power Conversion (Reverse Voltage Protection RVP) (8/2/2 - test 4.5)

4.5.1 Test setup

This test simulates the connection of a bus device to an operating bus segment, but with reverse polarity.

In case of reverse polarity connection of a bus device, that device should neither have a negative influence to the bus, nor be damaged, no matter how long the reverse connection lasts.

Almost the same setup as the test "Switch On Fast" is used, see Figure 40. Switch On Fast test setup. The only difference is the BDUT connected in reverse polarity to the KNX bus.

The reverse bus voltage is then applied by closing PB1. The current Iin is monitored during the test and compared to the maximum limit.

After the test, the correct polarity is restored and the operation of the BDUT is checked by pressing the KNX PROG button and verifying that the KNX PROG LED turns on.

- Oscilloscope channels:
  - CH1: BP1 command
  - CH2: Uin
  - CH3: DC-DC converter output
  - CH4: Iin
- Function generator period: 30 s
- Embedded FW: EvalKitSTKNX_LedLevel_V1.0.bin (see Section 4.1 General test setup).

4.5.2 Tests results - fan-in = 10 mA

The EVALKITSTKNX is tested with its default setting: DC-DC converter output voltage set to 5 V (not loaded) and linear regulator output voltage set to 3.3 V (loaded by CPU section).

Table 8. Reverse Voltage Protection tests results - fan-in = 10 mA.

EVALKITSTKNX configuration		Test conditions		Test results	
Linear regulator	DC-DC converter	Upsu	Rcable	Iin max. (Limit = 30mA)	Kit test after reverse polarity connection
3.3V supplying kit	5V enabled	30V	0Ω	28.5mA	Working
3.3V supplying kit	5V enabled	30V	35Ω	27.5mA	Working
3.3V supplying kit	5V enabled	20V	0Ω	18mA	Working
3.3V supplying kit	5V enabled	20V	35Ω	17.7mA	Working
		Cumulative result		PASS	

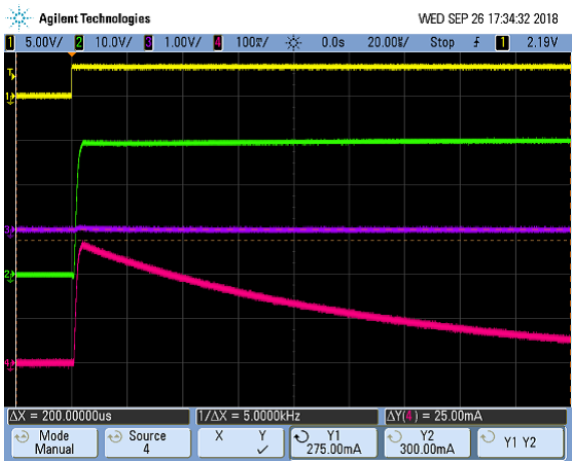
Figure 131. Upsu = 30V, Rcable = 0Ω

Iin max = 28.5mA	Limit = 30mA
KXN prog button pressed → KNX prog led switched	

Figure 132. Upsu = 20V, Rcable = 0Ω

Iin max = 18mA	Limit = 30mA
KXN prog button pressed → KNX prog led switched	

Figure 133. Upsu = 30V, Rcable = 35Ω



Iin max = 27.5mA	Limit = 30mA
KXN prog button pressed → KNX prog led switched	

Figure 134. Upsu = 20V, Rcable = 35Ω

Iin max = 17.7mA	Limit = 30mA
KXN prog button pressed → KNX prog led switched	

4.5.3 Tests results - fan-in = 30 mA

The EVALKITSTKNX is tested with its default setting: DC-DC converter output voltage set to 5 V (not loaded) and linear regulator output voltage set to 3.3 V (loaded by CPU section).

Table 9. Reverse Voltage Protection tests results - fan-in = 30 mA

EVALKITSTKNX configuration		Test conditions		Test results	
Linear regulator	DC-DC converter	Upsu	Rcable	Iin max. (Limit = 90mA)	Kit test after reverse polarity connection
3.3V supplying kit	5V enabled	30V	0Ω	27.7mA	Working
3.3V supplying kit	5V enabled	30V	35Ω	26.5mA	Working
3.3V supplying kit	5V enabled	20V	0Ω	17.9mA	Working
3.3V supplying kit	5V enabled	20V	35Ω	17.5mA	Working
		Cumulative result	PASS		

Figure 135. Upsu = 30V, Rcable = 0Ω

Figure 136. Upsu = 20V, Rcable = 0Ω

Iin max = 27.7mA	Limit = 90mA	Iin max = 17.9mA	Limit = 90mA
KXN prog button pressed → KNX prog led switched		KXN prog button pressed → KNX prog led switched	

Figure 137. Upsu = 30V, Rcable = 35Ω

Figure 138. Upsu = 20V, Rcable = 35Ω

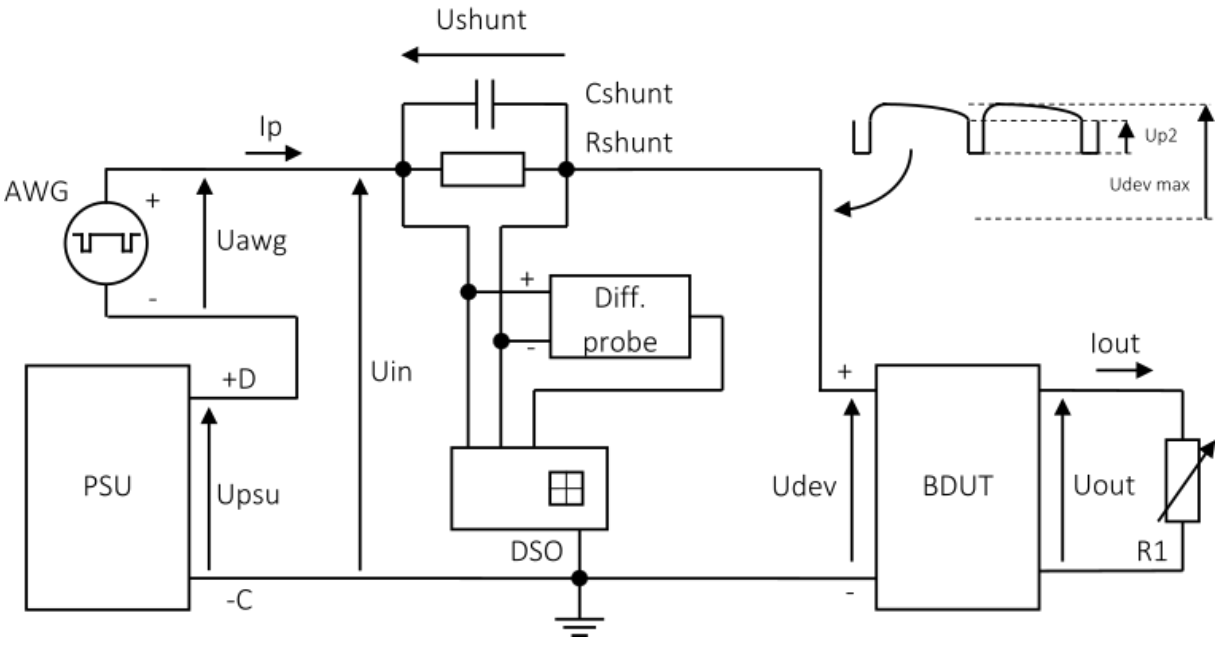
Iin max = 26.5mA	Limit = 90mA	Iin max = 17.5mA	Limit = 90mA
KXN prog button pressed → KNX prog led switched		KXN prog button pressed → KNX prog led switched	

4.6 Receiver - Pulse-Impedance (8/2/2 - test 5.1)

The input impedance of a KNX device has to be compliant to KNX standard requirements. This special test method checks the input impedance of the KNX device.

4.6.1 Test setup

Figure 139. Pulse-Impedance test setup



- Differential probe: Testec TT-SI 9001 position ÷10

- Oscilloscope channels (#8 Averaging Acquire mode for a better readability):
  - CH1: Uin
  - CH2: Udev
  - CH3: Ushunt

During the tests in this section, unless otherwise specified:

- R1 is tuned to sink Ip = fan-in

The connections from AWG+PSU to BDUT must be short, otherwise glitches are observed in Ushunt waveform.
For each test below, the power supply and Arbitrary Waveform Generator are initially configured as below:

- Upsu = 25 V
- Uawg = 6 Vpp; T = 300 µs; t1 = 35 µs

Then R1 is tuned to reach Ip = fan-in
From this state, Upsu, Uawg and R1 are tuned by iteration, until reaching the final state:

- Udev max. = 25 V
- Up2 = 6 V
- Ip = fan-in

See KNX standard Section 8/2/2 KNX System Conformance Testing for more information.
The areas ratio A1/A2 defined in 8/2/2, is then computed through a spreadsheet based on Ushunt samples acquired from the DSO.

- Embedded FW: EvalKitSTKNX_LedLevel_V1.0.bin (see Section 4.1 General test setup).

4.6.2 Tests results - fan-in = 10 mA

Test settings:

- Rshunt = 1 kΩ
- Cshunt = 2.2 nF

Table 10. Pulse Impedance tests results - fan-in = 10mA

EVALKITSTKNX configuration		Test conditions				Test results			
Linear regulator	DC-DC converter	Upsu	Uawq	Ip	Iout	A1/A2 L. limit = 1.1 U. limit = 4	Ia1 L. limit = 0.3 U. limit = 1.9	Ia2 L. limit = 0.32 U. limit = 2	Iend/Ia2 L. limit = 0 U. limit = 0.18
3.3V	Disabled	27.3V	6.6Vpp	**10mA**	8.2mA	1.19	0.62mA	0.67mA	0
5V	Disabled	27.3V	6.6Vpp	**10mA**	8.5mA	1.23	0.63mA	0.65mA	0
Disabled VDD_REGIN= VDDHV	**1V**	27.6V	6.6Vpp	**10mA**	87mA	1.26	0.62mA	0.63mA	0
Disabled VCCORE= VDCDC	**3.3V**	27.5V	6.6Vpp	**10mA**	36mA	1.26	0.63mA	0.68mA	0
Disabled VCCORE= VDCDC	**5V**	27.5V	6.6Vpp	**10mA**	mA	1.18	0.63mA	0.61mA	0
Enabled VDD_REGIN= VDCDC	**12V**	27.6V	6.7Vpp	**10mA**	mA	1.33	0.6mA	0.65mA	0
		Cumulative result				PASS			

4.6.2.1 *Linear regulator 3.3 V waveforms*

The linear regulator set to 3.3 V is supplied from VDDHV. The DC-DC converter is disabled.

Figure 140. Udev max & Up2 adjustments

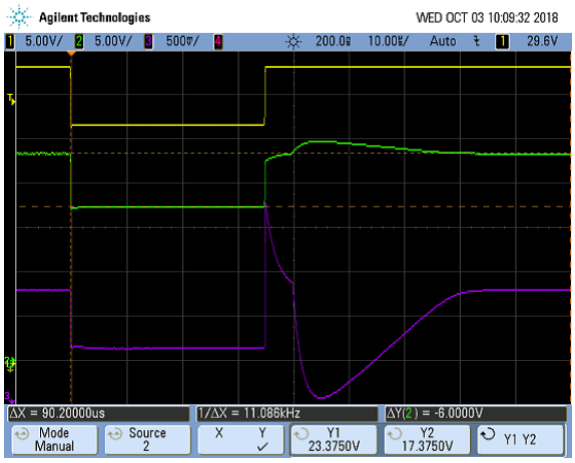
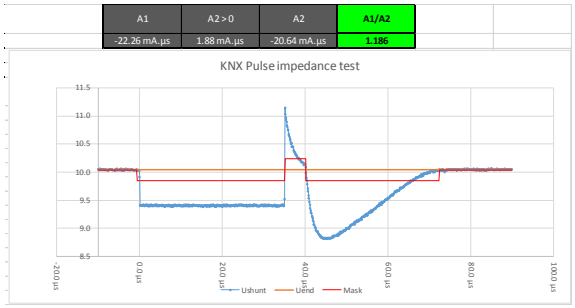


Figure 141. A1/A2



Upsu = 27.3VDC Uawg = 6.6Vpp Iout = 8.2mA	Ip = 10mA (CH2: 25V = 8th division on Y-scale)	A1/A2 = 1.19	1.1 ≤ Limits ≤ 4

Figure 142. Ia1 = Ushunt / Rshunt

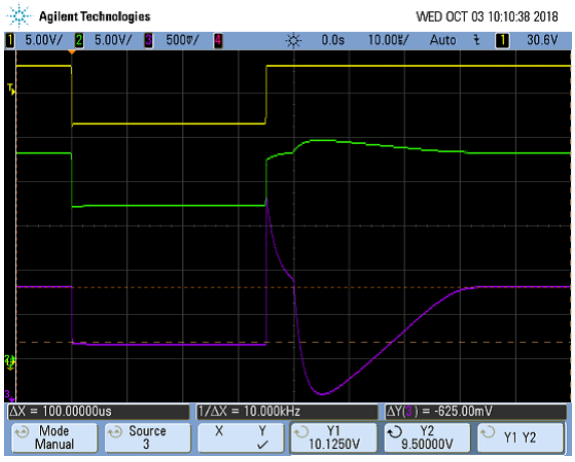
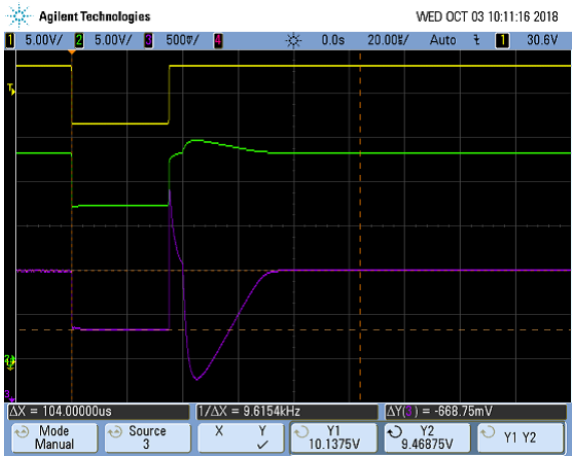


Figure 143. Ia2 = Ushunt / Rshunt & Iend/Ia2



Ia1 = 0.62mA	0.3mA ≤ Limits ≤ 1.9mA	Ia2 = 0.67mA Iend/Ia2 = 0	0.32mA ≤ Limits ≤ 2mA 0 ≤ Limits ≤ 0.18

4.6.2.2 *DC-DC converter 1 V waveforms*

The DC-DC converter is enabled and tuned to 1 V output voltage. The linear regulator is enabled (3.3 V) for STKNX I/Os and supplied from VDDHV.

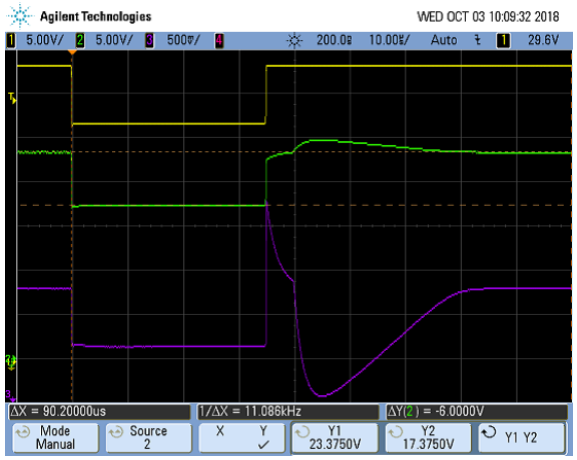
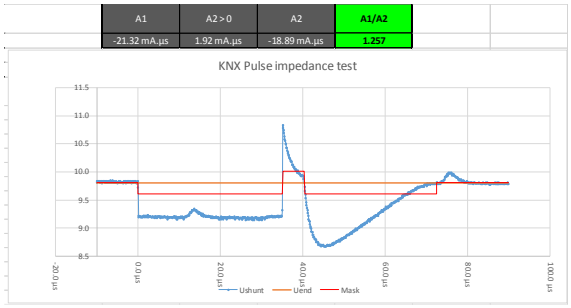
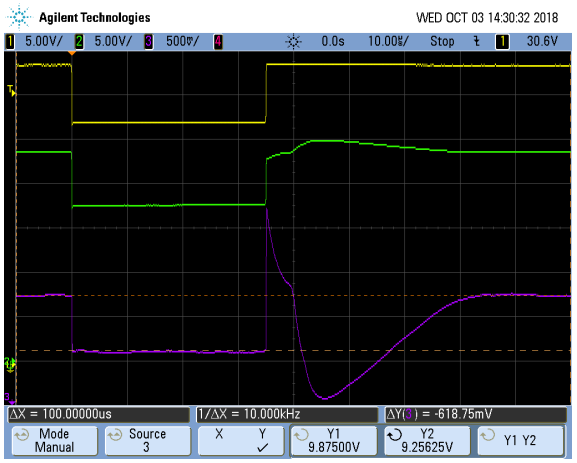
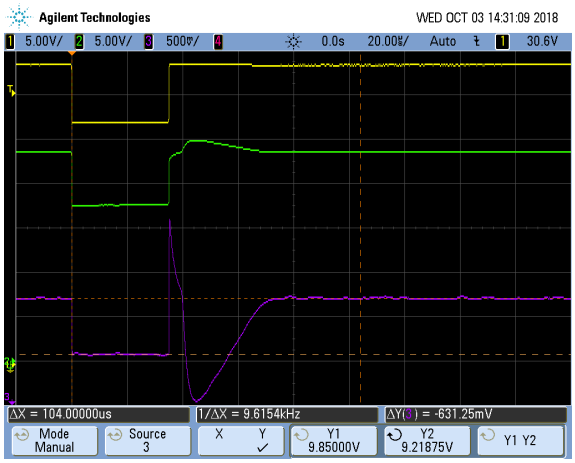
Udev max & Up2 adjustments 		**Figure 144. A1/A2** 	
Upsu = 27.6VDC Uawg = 6.6Vpp Iout = 87mA	Ip = 10mA (CH2: 25V = 8th division on Y-scale)	A1/A2 = 1.26	1.1 ≤ Limits ≤ 4

Figure 145. Ia1 = Ushunt / Rshunt 		**Figure 146. Ia2 = Ushunt / Rshunt & Iend/Ia2** 	
Ia1 = 0.62mA	0.3mA ≤ Limits ≤ 1.9mA	Ia2 = 0.63mA Iend/Ia2 = 0	0.32mA ≤ Limits ≤ 2mA 0 ≤ Limits ≤ 0.18

4.6.2.3 *DC-DC converter 3.3 V waveforms*

The DC-DC converter is enabled and tuned to 3.3 V output voltage. The linear regulator is disabled and VCCCORE is connected to VDCDC for STKNX I/Os supply.

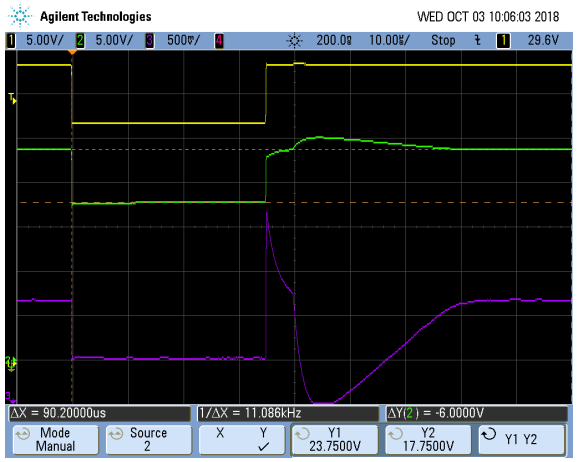
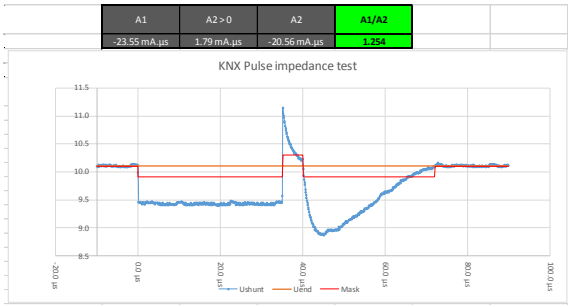
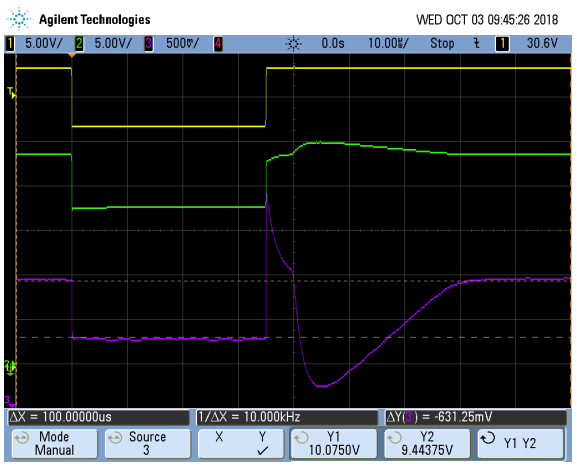
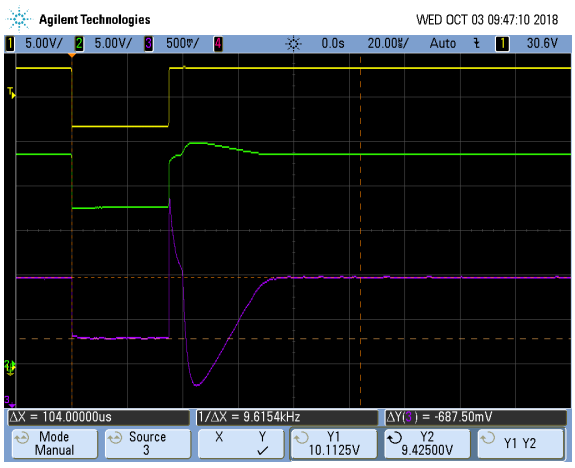
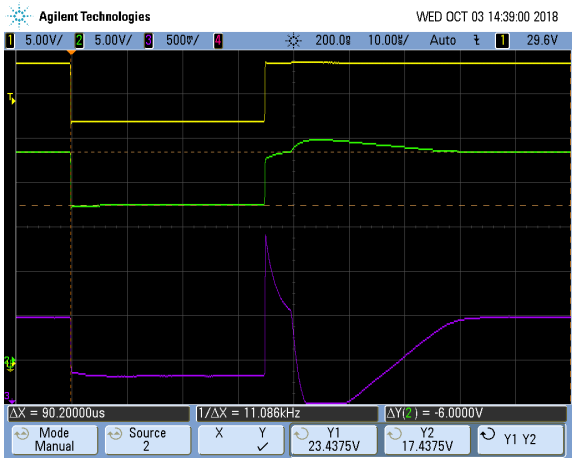
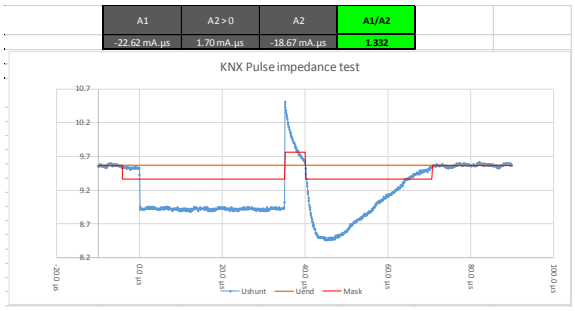
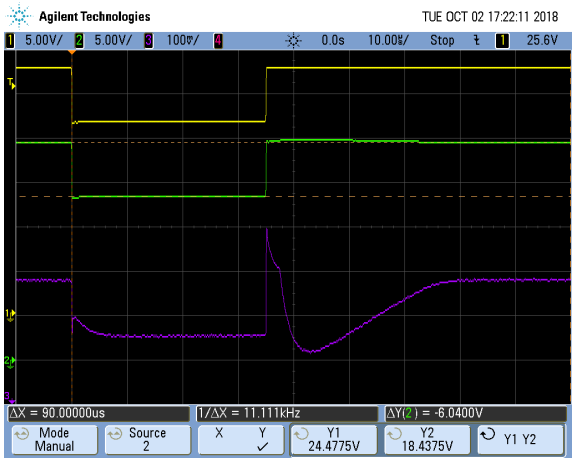
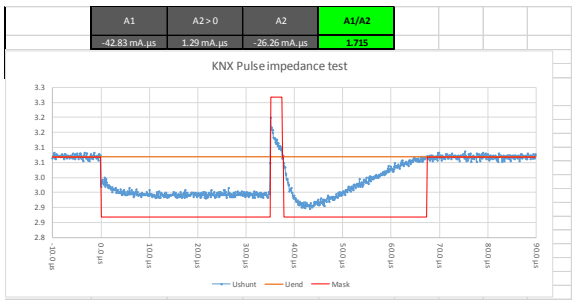
Udev max & Up2 adjustments 		**Figure 147. A1/A2** 	
Upsu = 27.5VDC Uawg = 6.6Vpp Iout = 36mA	Ip = 10mA (CH2: 25V = 8th division on Y-scale)	A1/A2 = 1.25	1.1 ≤ Limits ≤ 4

Figure 148. Ia1 = Ushunt / Rshunt 		**Figure 149. Ia2 = Ushunt / Rshunt & Iend/Ia2** 	
Ia1 = 0.63mA	0.3mA ≤ Limits ≤ 1.9mA	Ia2 = 0.69mA Iend/Ia2 = 0	0.32mA ≤ Limits ≤ 2mA 0 ≤ Limits ≤ 0.18

4.6.2.4 *DC-DC converter 12 V waveforms*

The DC-DC converter is enabled and tuned to 12 V output voltage. The linear regulator is enabled (3.3 V) for STKNX I/Os and supplied from VDCDC.

Udev max & Up2 adjustments 	Figure 150. **A1/A2** 		
Upsu = 27.5VDC Uawg = 6.6Vpp Iout = 11mA	Ip = 10mA (CH2: 25V = 8th division on Y-scale)	A1/A2 = 1.33	1.1 ≤ Limits ≤ 4

Udev max & Up2 adjustments 	Figure 151. **A1/A2** 		
Upsu = 22.9VDC Uawg = 6.2Vpp Iout = 26mA	Ip = 30mA (CH2: 25V = 8th division on Y-scale)	A1/A2 = 1.72	1.1 ≤ Limits ≤ 4

4.6.3 Tests results - fan-in = 30mA

Test settings:

- Rshunt = 100 Ω(1)
- Cshunt = 22 nF(2)

1. *Switching converters show negative input impedance, which can result in instability if supplied by high impedance source. To prevent test setup artificially induced instability, RSHUNT test resistor is reduced to 100Ω to perform pulse impedance test. The value of RSHUNT is chosen to be higher than 75Ω, which is the maximum loop resistance allowed TP1 cable (section 9/1 of KNX standard). This was suggested by KNX association.*
2. *To keep coherent the filtering of the signal Ushunt, Cshunt is set to 22 nF when associated to Rshunt = 100 Ω.*

Table 11. Pulse Impedance tests results - fan-in = 30mA

EVALKITSTKNX configuration		Test conditions				Test results			
Linear regulator	DC-DC converter	Upsu	Uawq	Ip	Iout	A1/A2 L. limit = 1.1 U. limit = 4	Ia1 L. limit = 0.3 U. limit = 1.9	Ia2 L. limit = 0.32 U. limit = 2	Iend/Ia2 L. limit = 0 U. limit = 0.18
3.3V	Disabled	22.9V	6.2Vpp	**30mA**	26mA	1.72	0.83mA	1.25mA	0
5V	Disabled	22.9V	6.2Vpp	**30mA**	26mA	1.69	0.86mA	1.22mA	0
Disabled VDD_REGIN= VDDHV	**1V**	22.9V	6.2Vpp	**17mA**	150mA	1.30	0.72mA	0.86mA	0
Disabled VCCORE= VDCDC	**3.3V**	23V	6.1Vpp	**30mA**	114mA	1.73	0.85mA	1.22mA	0
Disabled VCCORE= VDCDC	**5V**	23V	6.1Vpp	**30mA**	80mA	1.66	0.82mA	1.20mA	0
Enabled VDD_REGIN= VDCDC	**12V**	22.9V	6.2Vpp	**30mA**	35mA	1.72	0.86mA	1.21mA	0
		Cumulative results				PASS			

4.6.3.1 *Linear regulator 3.3 V waveforms*

The linear regulator set to 3.3 V is supplied from VDDHV. The DC-DC converter is disabled.

Udev max & Up2 adjustments

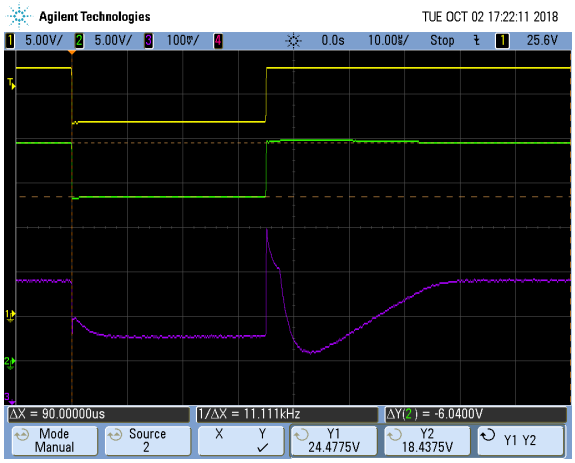
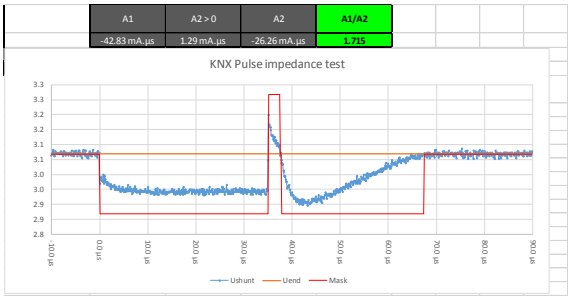
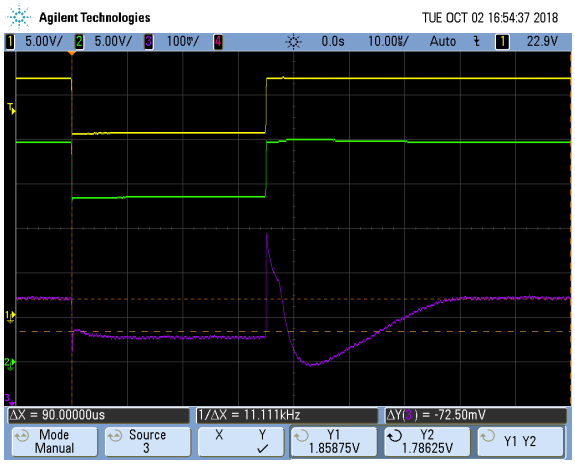


Figure 152. A1/A2



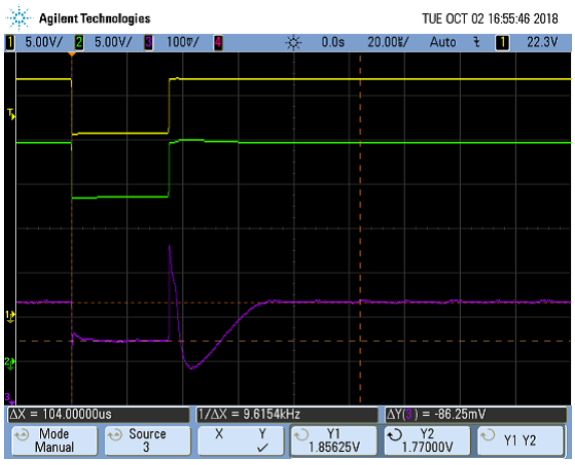
Upsu = 22.9VDC Uawg = 6.2Vpp Iout = 26mA	Ip = 30mA (CH2: 25V = 8th division on Y-scale)	A1/A2 = 1.72	1.1 ≤ Limits ≤ 4

Figure 153. Ia1 = Ushunt / Rshunt



Ia1 = 0.73mA	0.3mA < Limits < 1.9mA

Figure 154. Ia2 = Ushunt / Rshunt & Iend/Ia2

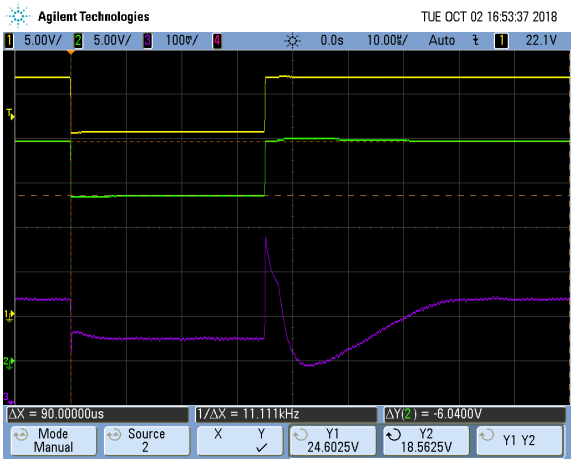


Ia2 = 0.86mA Iend/Ia2 = 0	0.32mA < Limits < 2mA 0 < Limits < 0.18

4.6.3.2 *DC-DC converter 1 V waveforms*

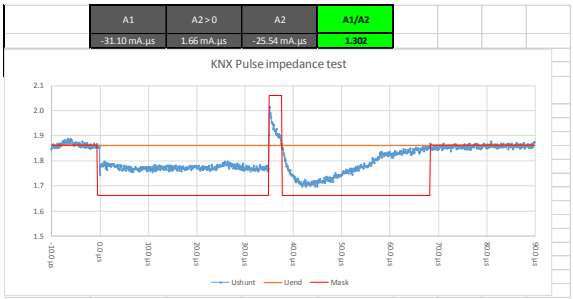
The DC-DC converter is enabled and tuned to 1 V output voltage. The load R1 is configured to sink Iout = 150 mA which is the limit of the DC-DC converter. It is therefore not possible to reach Ip = 30 mA (fan-in) on the bus but only 17 mA. The linear regulator is enabled (3.3 V) for STKNX I/Os and supplied from VDDHV.

Figure 155. Udev max & Up2 adjustments



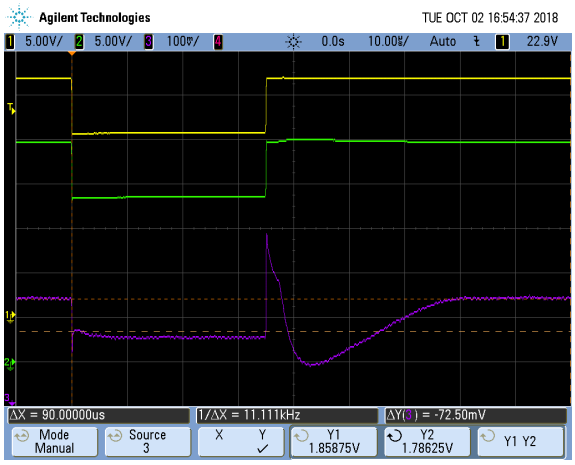
Upsu = 21.2VDC Uawg = 6.2Vpp Iout = 150mA	Ip = 17mA (CH2: 25V = 8th division on Y-scale)

Figure 156. A1/A2



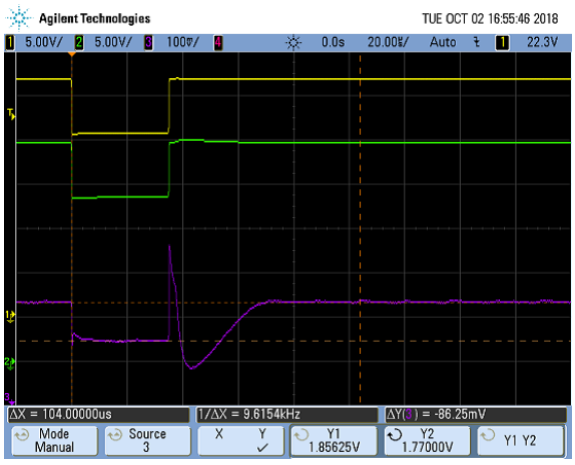
A1/A2 = 1.30	1.1 ≤ Limits ≤ 4

Figure 157. Ia1 = Ushunt / Rshunt



Ia1 = 0.73mA	0.3mA < Limits < 1.9mA

Figure 158. Ia2 = Ushunt / Rshunt & Iend/Ia2

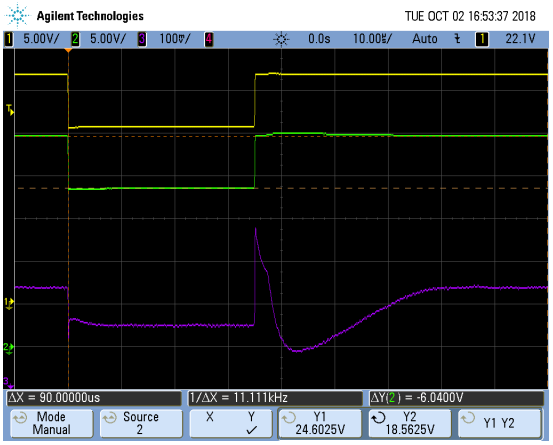


Ia2 = 0.86mA Iend/Ia2 = 0	0.32mA < Limits < 2mA 0 < Limits < 0.18

4.6.3.3 *DC-DC converter 3.3 V waveforms*

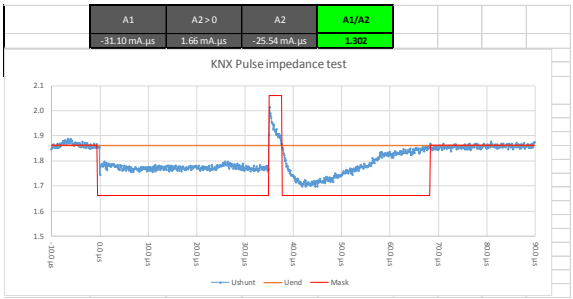
The DC-DC converter is enabled and tuned to 3.3 V output voltage. The linear regulator is disabled and VCCCORE is connected to VDCDC for STKNX I/Os supply.

Figure 159. Udev max & Up2 adjustments



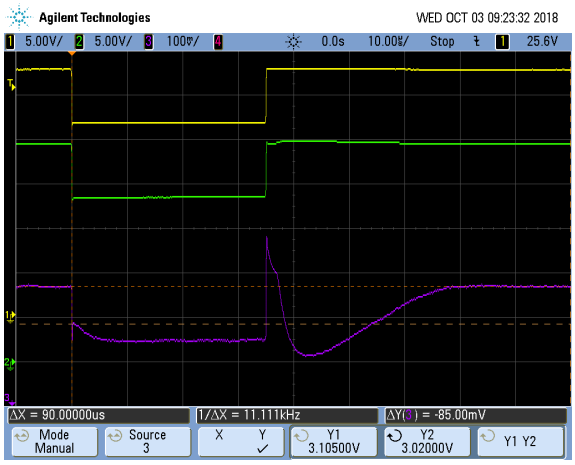
Upsu = 21.2VDC Uawg = 6.2Vpp Iout = 150mA	Ip = 17mA (CH2: 25V = 8th division on Y-scale)

Figure 160. A1/A2



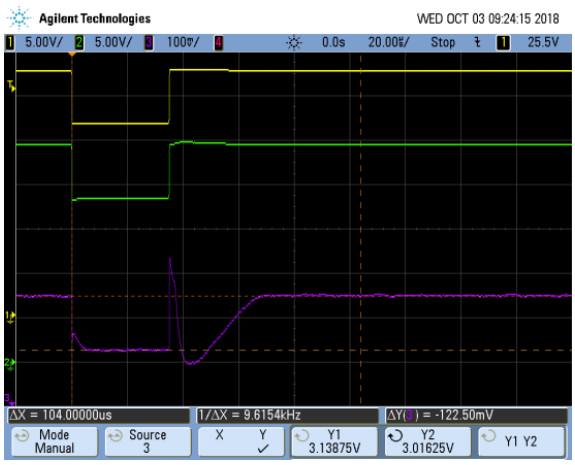
A1/A2 = 1.30	1.1 ≤ Limits ≤ 4

Figure 161. Ia1 = Ushunt / Rshunt



Ia1 = 0.85mA	0.3mA ≤ Limits ≤ 1.9mA	Ia2 = 1.23mA Iend/Ia2 = 0	0.32mA ≤ Limits ≤ 2mA 0 ≤ Limits ≤ 0.18

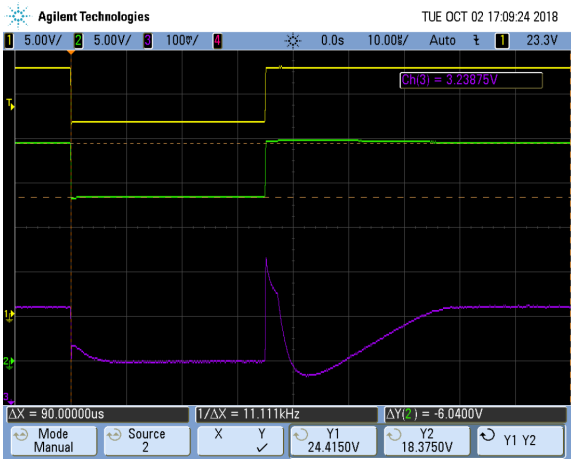
Figure 162. Ia2 = Ushunt / Rshunt & Iend/Ia2



4.6.3.4 *DC-DC converter 12 V waveforms*

The DC-DC converter is enabled and tuned to 12 V output voltage. The linear regulator is enabled (3.3 V) for STKNX I/Os and supplied from VDCDC.

Figure 163. Udev max & Up2 adjustments



Upsu = 22.9VDC Uawg = 6.2Vpp Iout = 35mA	Ip = 30mA (CH2: 25V = 8th division on Y-scale)	A1/A2 = 1.72	1.1 ≤ Limits ≤ 4

Figure 164. A1/A2

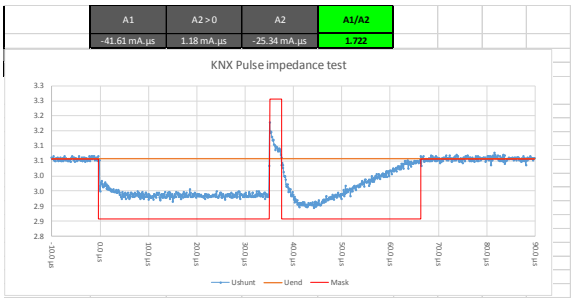
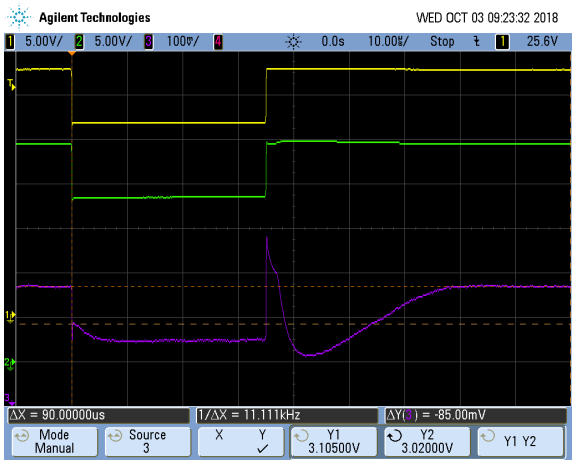
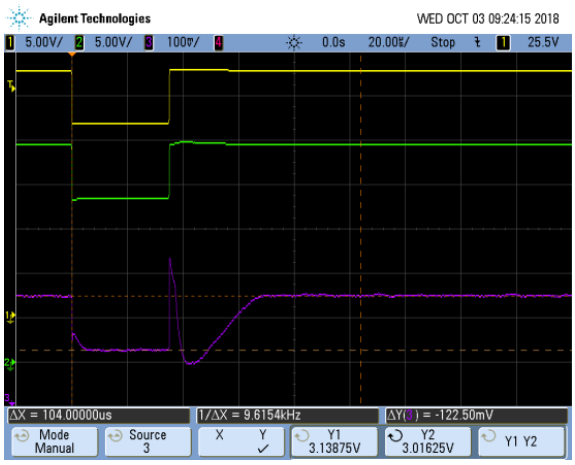


Figure 165. Ia1 = Ushunt / Rshunt



Ia1 = 0.85mA	0.3mA ≤ Limits ≤ 1.9mA

Figure 166. Ia2 = Ushunt / Rshunt & Iend/Ia2



Ia2 = 1.23mA Iend/Ia2 = 0	0.32mA ≤ Limits ≤ 2mA 0 ≤ Limits ≤ 0.18

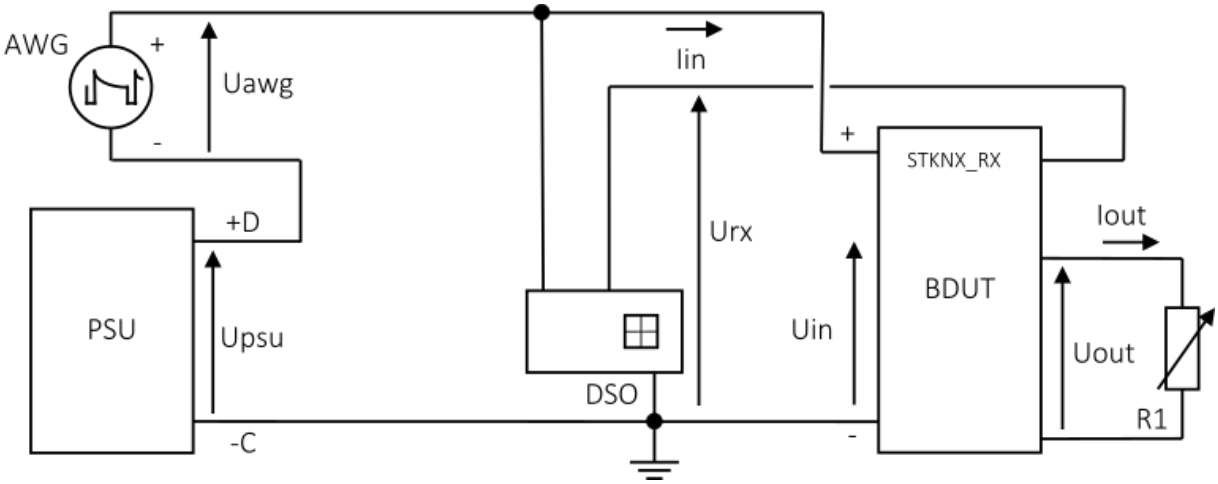
4.7 Receiver - Sensitivity (8/2/2 - test 5.2)

This test checks the thresholds and the sensitivity of the receiver. The receiver has to be able to detect both strong and weak analogue data signals.

In particular, the standard requires that signals with amplitude higher than Ua1 = 0.7 V, Ua2 = 0.5 V are detected, while signals with amplitude lower than Ua1 = Ua2 = 0.2 V are neglected.

4.7.1 Test setup

Figure 167. Sensitivity test setup



- Oscilloscope channels:
  - CH1: Uin
  - CH2: Urx
  - Averaging display #8 sometimes activated
- R1 is connected to DC-DC converter output and tuned to sink Iin = fan-in

The connections from AWG+PSU to BDUT must be short, otherwise glitches are observed in the Uin waveform.

The BDUT reception is checked by observing the STKNX_RX output (Urx) on scope. Both an EVALKITSTKNX fan-in 10 mA and 30 mA have been tested, in their default configuration: Linear regulator 3.3 V (not loaded) and DC-DC converter 5 V loaded with both maximum load (Iin = fan-in) and open load.

4.7.2 EVALKITSTKNX settings

Every "isolation" jumper (between KNX section and CPU section) is removed.

4.7.3 Waveform generation at BDUT input

The signal at Uawg is generated by computing samples with a spreadsheet and then transferring them into the AWG in Arbitrary Waveform mode. This signal is then superimposed to the PSU voltage to create the expected waveform at BDUT input, described in the following sections.

Both signals are tested at maximum (60 V/µs) and minimum (1 V/µs) slopes.

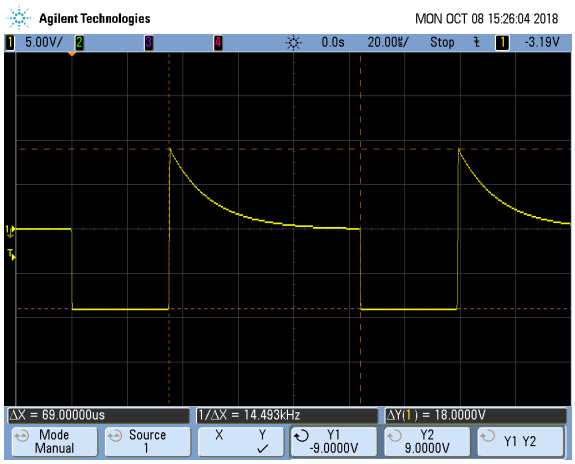
4.7.3.1 Ua1 = Ua2 = Ue = 9 V

Due to limitation of the frequency generator, the telegram required in the 08.02.02 cannot be entirely generated, but only a portion: 0x01E10081.

This word which is made of 32 bits duration 104 µs each has a length of 3328 µs.

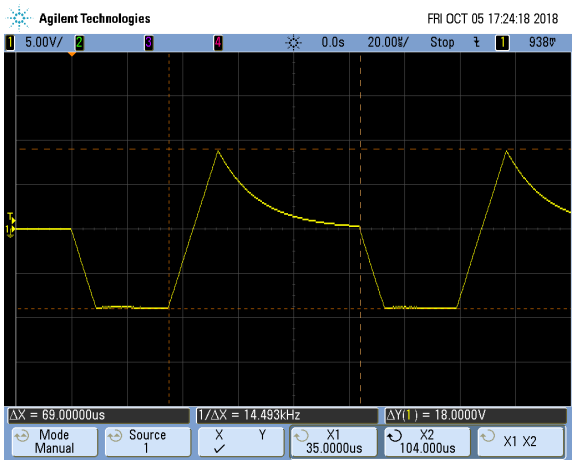
The sampling frequency of the AWG is set to 100 ns, low enough to generate a sufficient long word and high enough to generate the expected slope.

Figure 168. Rising and falling slopes ≈ 60V/µs



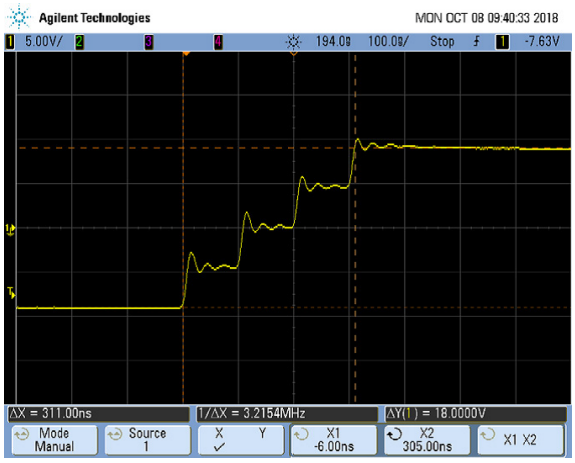
Ua1 = Ua2 = 9V

Figure 169. Rising and falling slopes ≈ 1V/µs



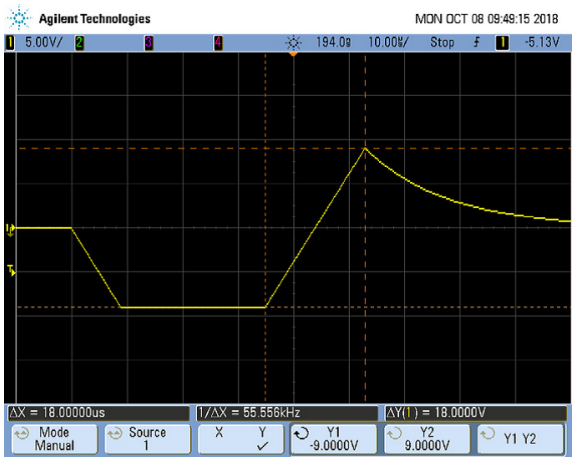
Ua1 = Ua2 = 9V

Figure 170. Rising and falling slopes ≈ 60V/µs



Slope = 18V / 311ns = 53V/µs

Figure 171. Rising and falling slopes ≈ 1V/µs



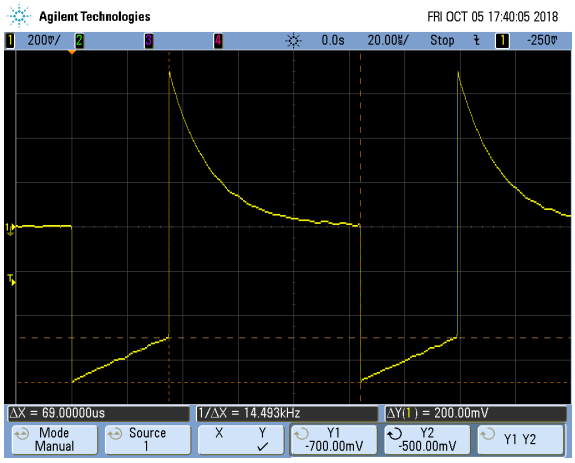
Slope = 18V / 18µs = 1V/µs

4.7.3.2 *Ua1 = Ue = 0.7 V; Ua2 = 0.5 V*

Due to the low voltage amplitude (0.5 V), the lowest sampling period of the AWG (5 ns) is used to be able to generate a slope of 60 V/µs ↔ 0.5 V/8.3 ns.

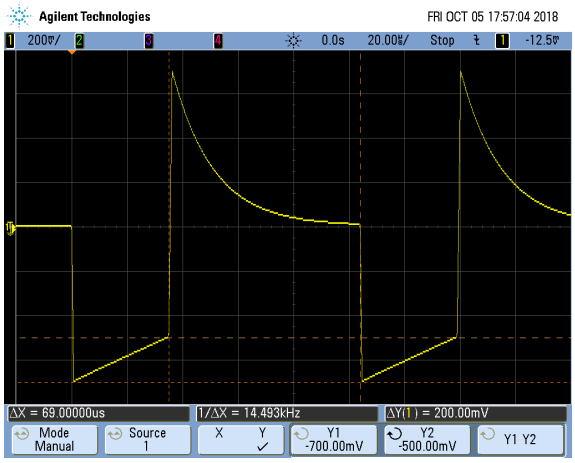
As a consequence, only a short word (3 bits) can be generated: 0b010, which is made of 62400 samples.

Figure 172. Rising and falling slopes ≈ 60V/µs



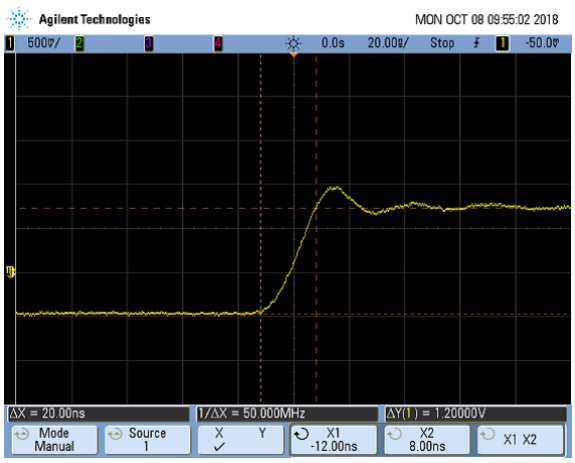
Ua1 = 0.7V; Ua2 = 0.5V

Figure 173. Rising and falling slopes ≈ 1V/µs



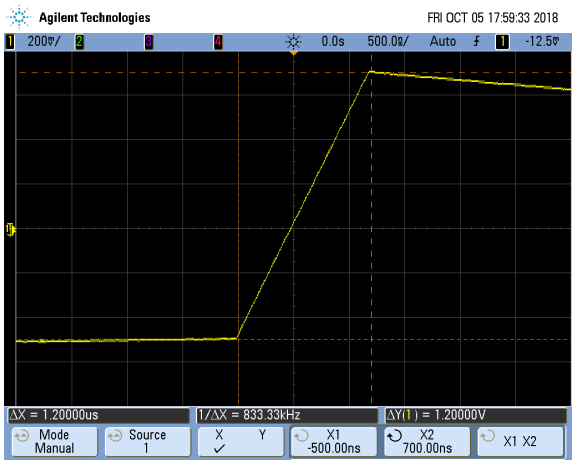
Ua1 = 0.7V; Ua2 = 0.5V

Figure 174. Rising and falling slopes ≈ 60V/µs



Slope = 1.2V / 20ns = 60V/µs

Figure 175. Rising and falling slopes ≈ 1V/µs



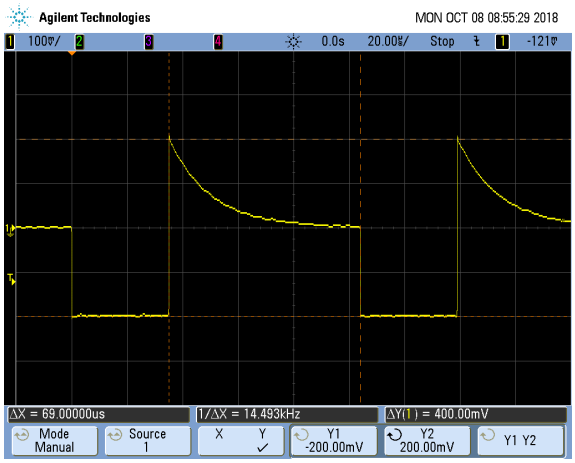
Slope = 1.2V / 1.2µs = 1V/µs

4.7.3.3 *Ua1 = Ua2 = Ue = 0.2V*

Due to the low voltage amplitude (0.2 V), the lowest sampling period of the AWG (5 ns) is used to be able to generate a slope of 60 V/µs ↔ 0.2 V/3.3 ns.

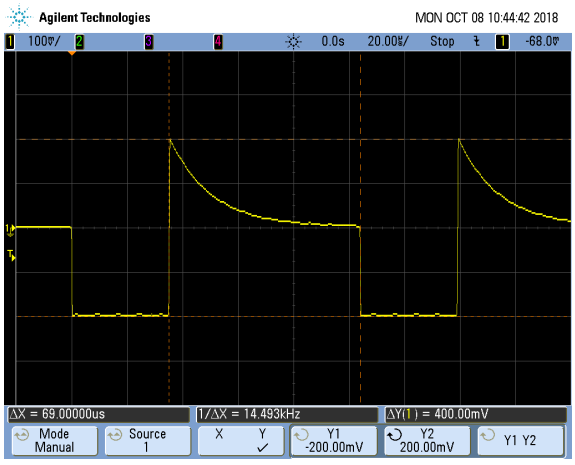
As a consequence, only a short word (3 bits) can be generated: 0b010, which is made of 62400 samples.

Figure 176. Rising and falling slopes ≈ 60V/µs



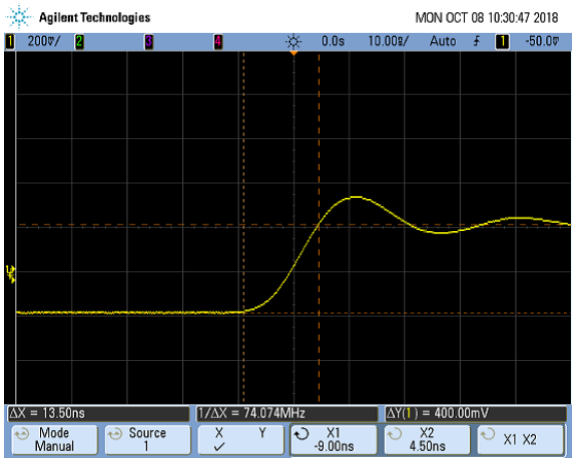
Ua1 = Ua2 = 0.2V

Figure 177. Rising and falling slopes ≈ 1V/µs



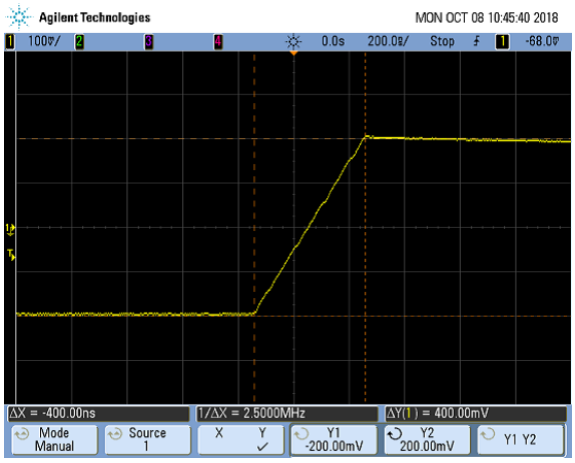
Ua1 = Ua2 = 0.2V

Figure 178. Rising and falling slopes ≈ 60V/µs



Slope = 0.4V / 13.5ns = 30V/µs

Figure 179. Rising and falling slopes ≈ 1V/µs



Slope = 0.4V / 0.4µs = 1V/µs

4.7.4 Test results

Every test result is reported in the table below. Some tests are illustrated in the following table with scope traces.

Table 12. Sensitivity tests results - fan-in = 10mA

EVALKITSTKNX configuration		Test conditions					Test results	
Linear regulator	DC-DC converter	Ua1	Ua2	Slopes	Upsu	Iin	Bits decoding	Verdict
3.3V	5V-loaded	9V	9V	60V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	9V	9V	60V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	9V	9V	1V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	9V	9V	1V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	0.7V	0.5V	60V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	0.7V	0.5V	60V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	0.7V	0.5V	1V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	0.7V	0.5V	1V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	0.2V	0.2V	60V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	0.2V	0.2V	60V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	0.2V	0.2V	1V/µs	30V	**10mA**	0%	PASS
3.3V	5V-loaded	0.2V	0.2V	1V/µs	20V	**10mA**	0%	PASS
3.3V	5V	9V	9V	60V/µs	30V	**<1mA**	0%	PASS
3.3V	5V	9V	9V	60V/µs	20V	**<1mA**	0%	PASS
3.3V	5V	9V	9V	1V/µs	30V	**<1mA**	100%	PASS
3.3V	5V	9V	9V	1V/µs	20V	**<1mA**	100%	PASS
3.3V	5V	0.7V	0.5V	60V/µs	30V	**<1mA**	100%	PASS
3.3V	5V	0.7V	0.5V	60V/µs	20V	**<1mA**	100%	PASS
3.3V	5V	0.7V	0.5V	1V/µs	30V	**<1mA**	100%	PASS
3.3V	5V	0.7V	0.5V	1V/µs	20V	**<1mA**	100%	PASS

EVALKITSTKNX configuration		Test conditions					Test results	
Linear regulator	DC-DC converter	Ua1	Ua2	Slopes	Upsu	Iin	Bits decoding	Verdict
3.3V	5V	0.2V	0.2V	60V/µs	30V	**<1mA**	0%	PASS
3.3V	5V	0.2V	0.2V	60V/µs	20V	**<1mA**	0%	PASS
3.3V	5V	0.2V	0.2V	1V/µs	30V	**<1mA**	0%	PASS
3.3V	5V	0.2V	0.2V	1V/µs	20V	**<1mA**	0%	PASS

Table 13. Sensitivity tests results - fan-in = 30mA

EVALKITSTKNX configuration		Test conditions					Test results	
Linear regulator	DC-DC converter	Ua1	Ua2	Slopes	Upsu	Iin	Bits decoding	Verdict
3.3V	5V-loaded	9V	9V	60V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	9V	9V	60V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	9V	9V	1V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	9V	9V	1V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	0.7V	0.5V	60V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	0.7V	0.5V	60V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	0.7V	0.5V	1V/µs	30V	**10mA**	100%	PASS
3.3V	5V-loaded	0.7V	0.5V	1V/µs	20V	**10mA**	100%	PASS
3.3V	5V-loaded	0.2V	0.2V	60V/µs	30V	**10mA**	0%	PASS
3.3V	5V-loaded	0.2V	0.2V	60V/µs	20V	**10mA**	0%	PASS
3.3V	5V-loaded	0.2V	0.2V	1V/µs	30V	**10mA**	0%	PASS
3.3V	5V-loaded	0.2V	0.2V	1V/µs	20V	**10mA**	0%	PASS
3.3V	5V	9V	9V	60V/µs	30V	**<1mA**	100%	PASS
3.3V	5V	9V	9V	60V/µs	20V	**<1mA**	100%	PASS
3.3V	5V	9V	9V	1V/µs	30V	**<1mA**	100%	PASS
3.3V	5V	9V	9V	1V/µs	20V	**<1mA**	100%	PASS
3.3V	5V	0.7V	0.5V	60V/µs	30V	**<1mA**	100%	PASS
3.3V	5V	0.7V	0.5V	60V/µs	20V	**<1mA**	100%	PASS
3.3V	5V	0.7V	0.5V	1V/µs	30V	**<1mA**	100%	PASS
3.3V	5V	0.7V	0.5V	1V/µs	20V	**<1mA**	100%	PASS
3.3V	5V	0.2V	0.2V	60V/µs	30V	**<1mA**	0%	PASS
3.3V	5V	0.2V	0.2V	60V/µs	20V	**<1mA**	0%	PASS
3.3V	5V	0.2V	0.2V	1V/µs	30V	**<1mA**	0%	PASS
3.3V	5V	0.2V	0.2V	1V/µs	20V	**<1mA**	0%	PASS

4.7.4.1 *Signals waveforms for fan-in 10 mA kit - Upsu = 30 V - Iin = 10 mA*

Figure 180. Ua1 = Ua2 = 9V, Slopes = 60V/µs

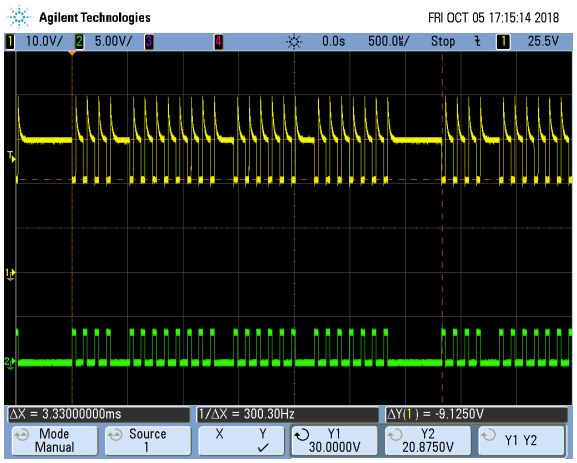


Figure 181. Ua1 = Ua2 = 9V, Slopes = 60V/µs (zoom)

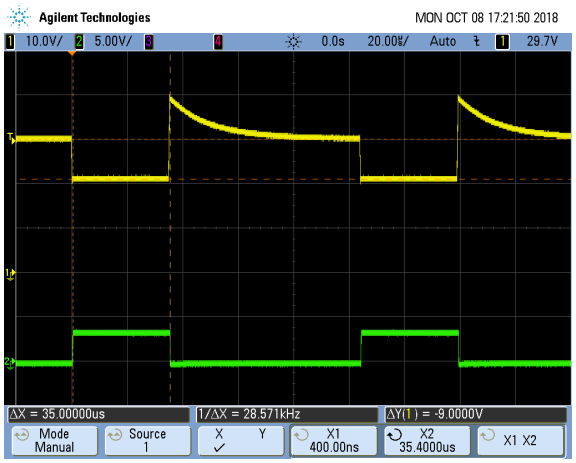


Figure 182. Ua1 = Ua2 = 9V, Slopes = 1V/µs

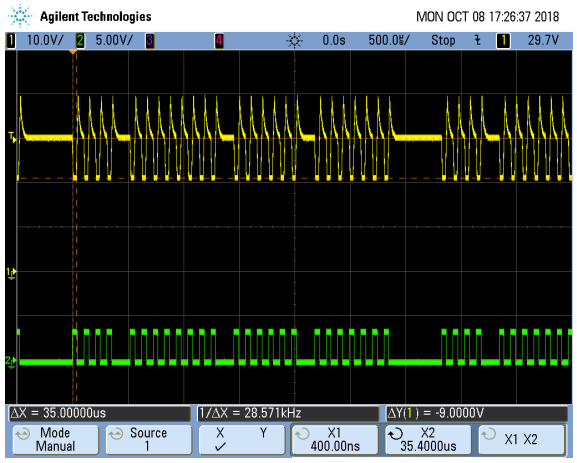


Figure 183. Ua1 = Ua2 = 9V, Slopes = 1V/µs (zoom)

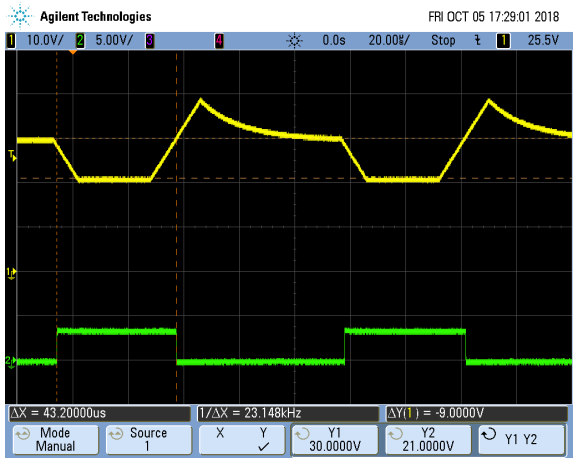


Figure 184. Ua1 0.7V, Ua2 = 0.5V, Slopes = 60V/µs

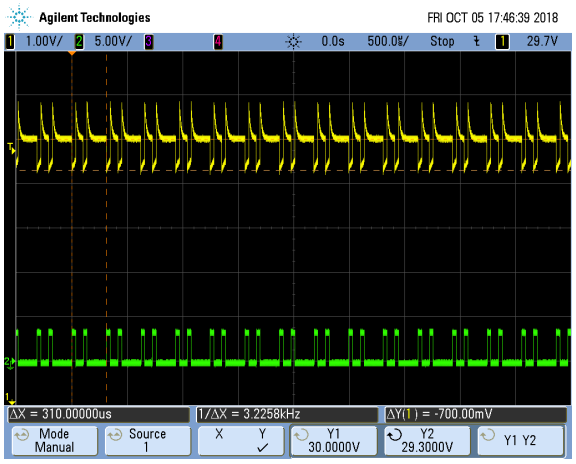


Figure 185. Ua1 0.7V, Ua2 = 0.5V, Slopes = 60V/µs (zoom)

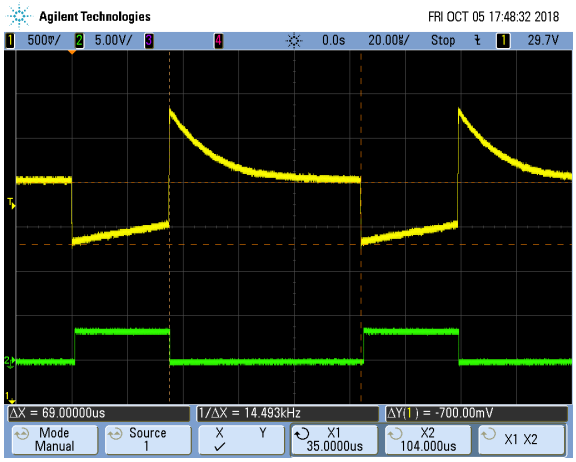


Figure 186. Ua1 0.7V, Ua2 = 0.5V, Slopes = 1V/µs

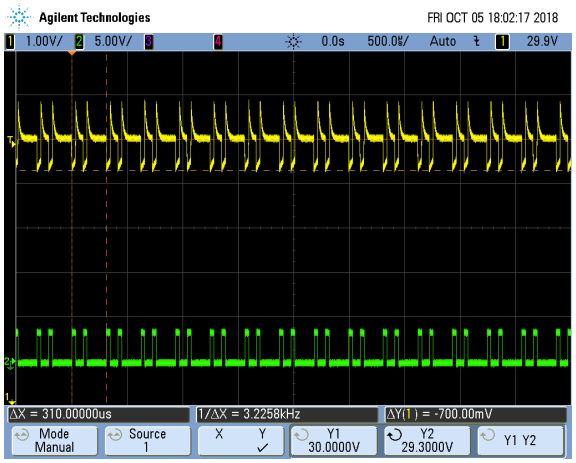


Figure 187. Ua1 0.7V, Ua2 = 0.5V, Slopes = 1V/µs (zoom)

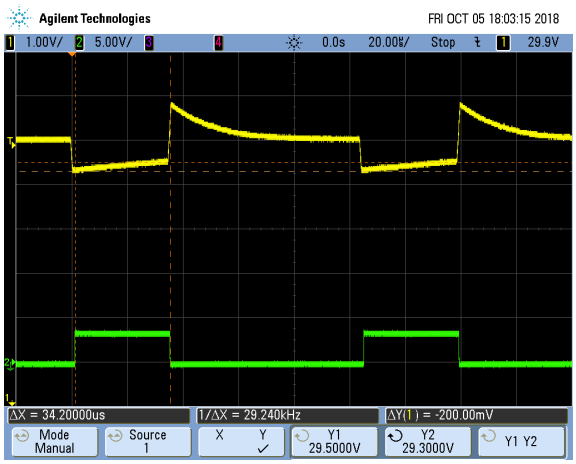


Figure 188. Ua1 0.2V, Ua2 = 0.2V, Slopes = 60V/µs

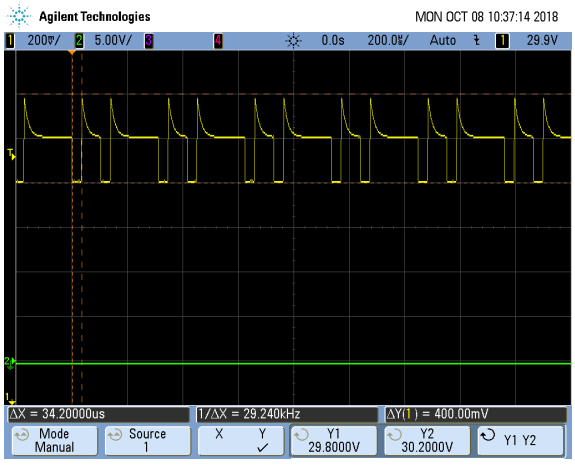
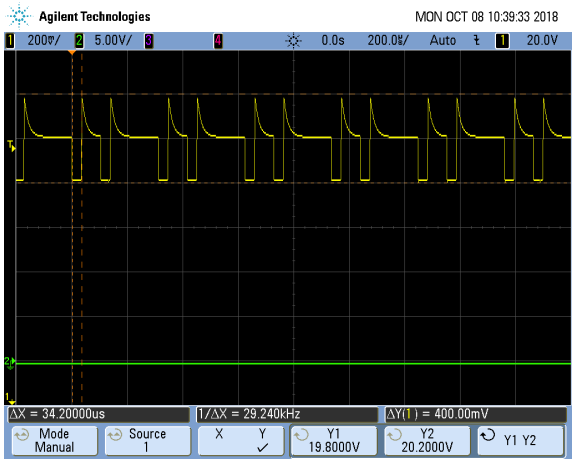


Figure 189. Ua1 0.2V, Ua2 = 0.2V, Slopes = 1V/µs

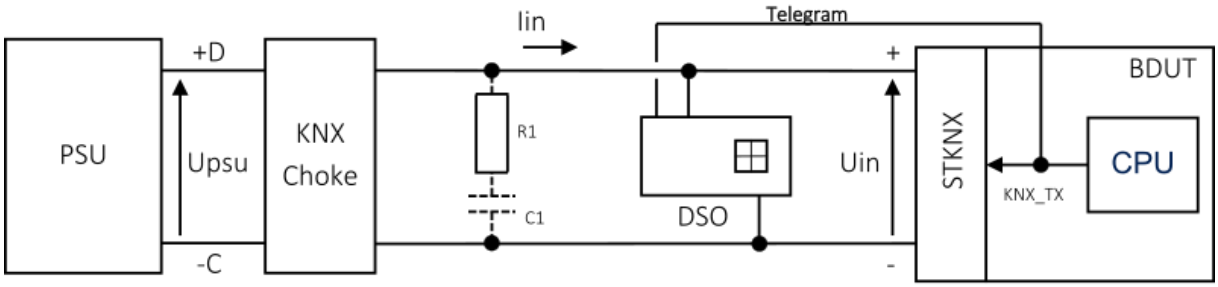


4.8 Transmitter tests setups (8/2/2 - tests 6.1, 6.2 and 6.3)

These tests check the ability of the transmitter to generate proper signals at different bus loads.

The transmitter tests 6.1, 6.2 and 6.3 in the following sections have the common setup described below:

Figure 190. Transmitter tests 6.1, 6.2 and 6.3 setup



Oscilloscope channels:

- CH1: KNX_TX (transmit data)
- CH2: Uin (DC and AC-Part)

Fan-in 10 mA kit: the CPU section consumption is 20 mA, so we have to use the DC-DC converter to keep the bus consumption lower than 10 mA fan-in. The configuration used is DC-DC converter voltage = 5 V, supplying the 3.3 V linear regulator U15:

- J17.2-4 closed
- J19.2-3 closed
- Other PSU config jumpers removed.

Fan-in 30 mA kit: the STKNX linear regulator is supplying the CPU section (19.2 mA consumption):

- J18.4-6
- Other PSU config jumpers removed.

A dedicated firmware in the CPU allows sending a specific telegram at STKNX data input.

The DC-DC converter output is charged with a resistor when we want to increase Iin up to fan-in value (for Upsu = 20 V).

Only the “isolation” jumpers KNX_TX, GND, VLIN, VDCDC (between KNX section and CPU section) are connected.

4.9 Transmitter Test (Normal Current) - Test 1 (8/2/2 - test 6.1)

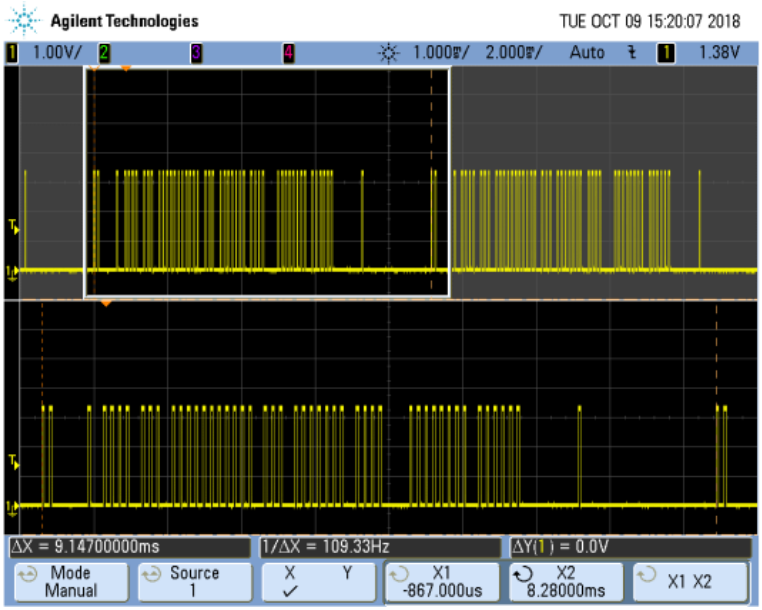
This test represents the sending of one device to the bus, which is equipped only with a few bus devices.

4.9.1 Test setup

The setup used is described in Section 4.8 Transmitter tests setups (8/2/2 - tests 6.1, 6.2 and 6.3), in which:

- R1 = C1 = NP
- The dedicated firmware “DPT_1-001_Telegram_Generator.bin” available at www.st.com (document “Test firmwares for EVALKITSTKNX”) is loaded in the kit CPU to transmit continuously:
- the DPT 1.001 telegram (0x) BC 10 01 10 01 E1 00 81 BF
- a pause of x2 bytes 0xFF between each telegram.

Figure 191. **DPT 1.001 telegram emission from CPU**



4.9.2 Test results

Table 14. **Transmitter Test (Normal Current) - Test 1 test results**

EVALKITSTKNX configuration			Test conditions			Test results		
Fan-in	Linear regulator	DC-DC converter	Upsu	Iin (no TX)	Iin (TX)	Ua L. Limit = 6V U. Limit = 9V	Ua rising slope L. Limit = 1V/µs U. Limit = 100V/µs	Ua rising slope L. Limit = 1V/µs U. Limit = 100V/µs
10mA	3.3V not loaded	5V loaded with U15 to CPU section	30V	5.5mA	32mA	7.7V	6.9V/µs	40V/µs
10mA	3.3V not loaded	5V loaded with U15 to CPU section	20V	8.8mA	36mA	7.7V	5.7V/µs	42V/µs
10mA	3.3V not loaded	5V loadedwith U15 to (CPU section // 1.4kΩ)	30V	6.3mA	33mA	7.7V	6.9V/µs	40V/µs
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	20V	10mA	37mA	7.7V	5.8V/µs	42V/µs
30mA	3.3V not loaded CPU selection	5V not loaded	30V	19.8mA	51mA	7.7V	6.9V/µs	41V/µs
30mA	3.3V not loaded CPU selection	5V not loaded	20V	20mA	51mA	7.6V	5.7V/µs	38V/µs
30mA	3.3V not loaded CPU selection	5V loaded with 213Ω	30V	26mA	62mA	7.7V	6.9V/µs	40V/µs
30mA	3.3V not loaded CPU selection	5V loaded with 213Ω	20V	30mA	67mA	7.7V	5.8V/µs	42V/µs

EVALKITSTKNX configuration			Test conditions			Test results		
Fan-in	Linear regulator	DC-DC converter	Upsu	Iin (no TX)	Iin (TX)	Ua L. Limit = 6V U. Limit = 9V	Ua rising slope L. Limit = 1V/µs U. Limit = 100V/µs	Ua rising slope L. Limit = 1V/µs U. Limit = 100V/µs
			Cumulative result			PASS		

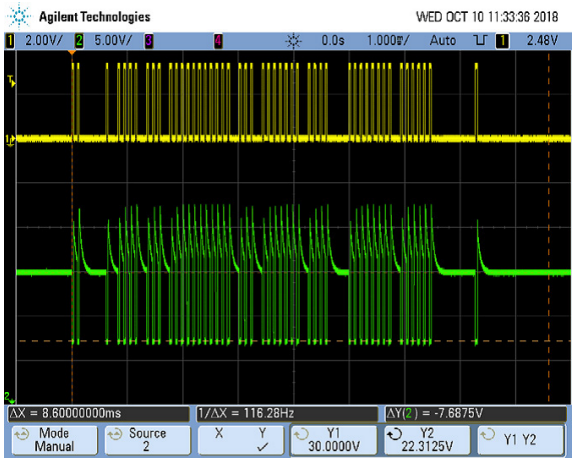
4.9.2.1 *Signals waveforms for fan-in 10 mA kit*

Below are reported the waveforms of the signals on the 10 mA fan-in kit, where the DC-DC converter 5 V is supplying the CPU section through the U15 3.3 V linear regulator.

When not transmitting, Iin = 5.5 mA. During transmission, Iin = 32 mA.

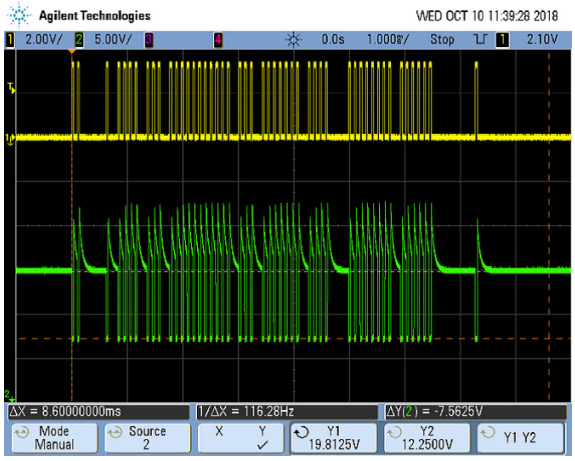
The tests were also performed when charging the DC-DC output with an additional resistor in order to sink Iin = 10 mA (fan-in), but no differences were observed on signals waveforms.

Figure 192. Upsu = 30V



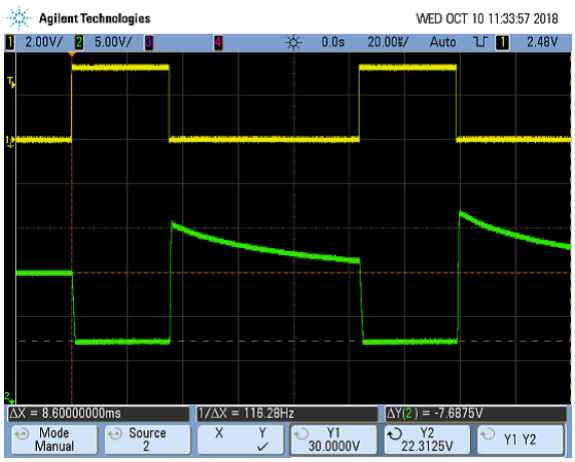
Ua = 7.69V | 6V ≤ Limits ≤ 9V

Figure 193. Upsu = 20V



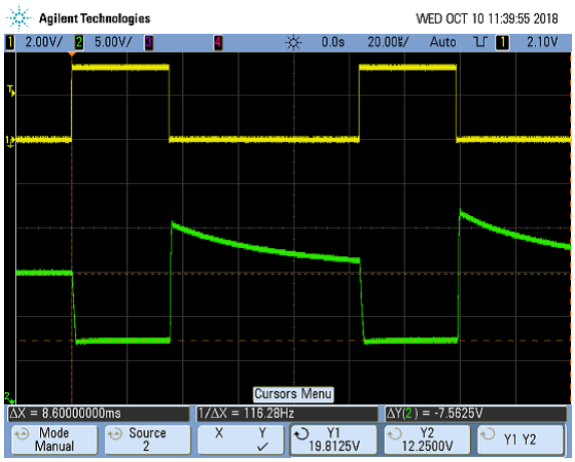
Ua = 7.69V | 6V ≤ Limits ≤ 9V

Figure 194. Upsu = 30V (zoom)



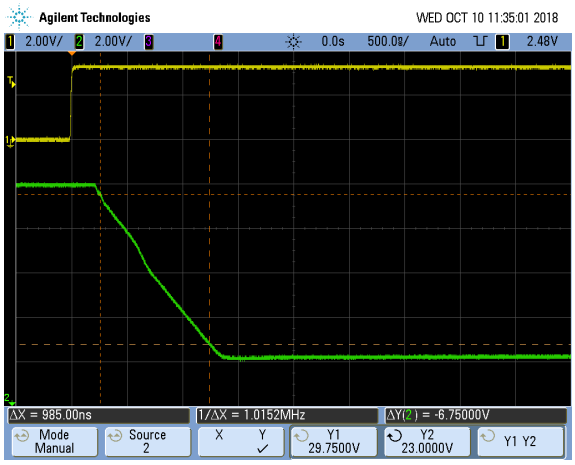
Ua = 7.69V | 6V ≤ Limits ≤ 9V

Figure 195. Upsu = 20V



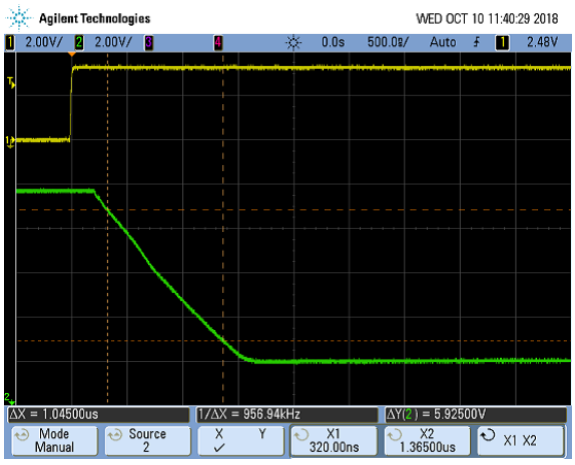
Ua = 7.69V | 6V ≤ Limits ≤ 9V

Figure 196. Upsu = 30V



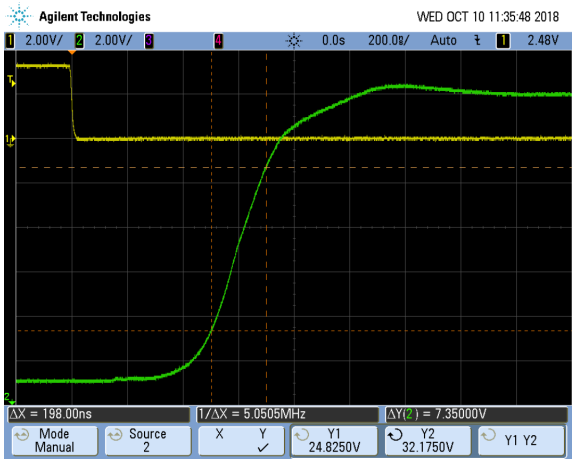
Rising slope = 6.9V/µs	1V/µs ≤ Limits ≤ 100V/µs

Figure 197. Upsu = 20V



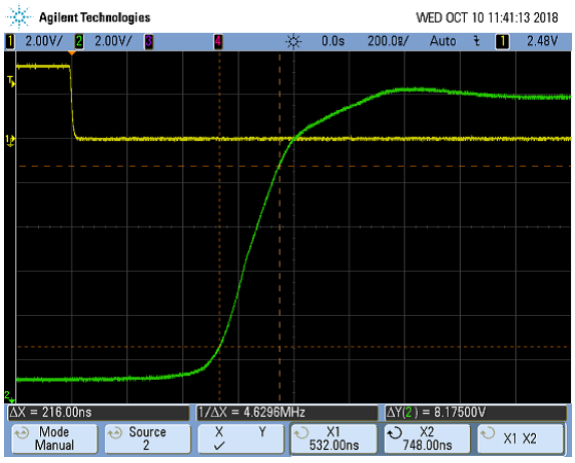
Rising slope = 5.7V/µs	1V/µs ≤ Limits ≤ 100V/µs

Figure 198. Upsu = 30V



Falling slope = 40V/µs	1V/µs < Limits < 100V/µs

Figure 199. Upsu = 20V



Falling slope = 42V/µs	1V/µs < Limits < 100V/µs

4.9.2.2 *Signals waveforms for fan-in 30 mA kit*

Below are reported the waveforms of the signals on the 30 mA fan-in kit, where the STKNX linear regulator is supplying the CPU section (19.2 mA consumption).

When not transmitting, Iin = 19.8 mA. During transmission, Iin = 50.5 mA.

The tests were also performed when charging the DC-DC output with a resistor in order to sink Iin = 30 mA (fan-in), but no differences were observed on signals waveforms.

Figure 200. Upsu = 30V

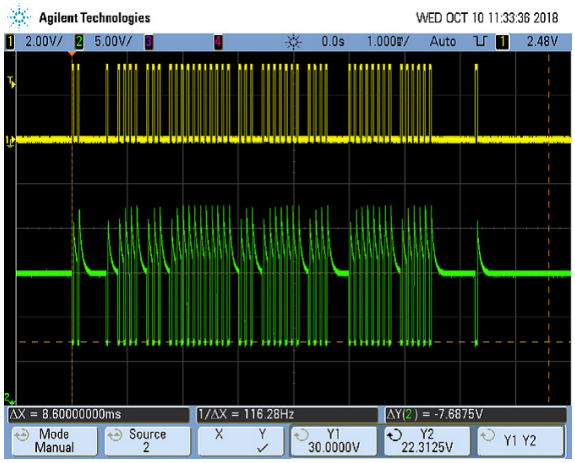


Figure 201. Upsu = 20V

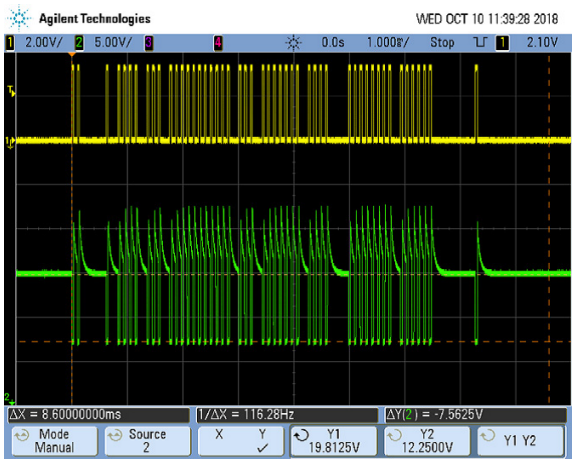


Figure 202. Upsu = 30V (zoom)

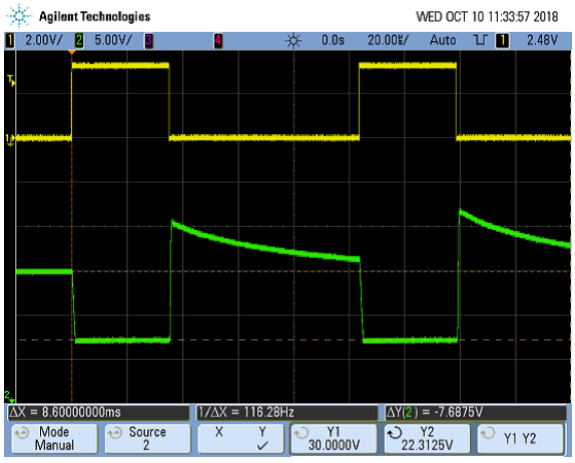
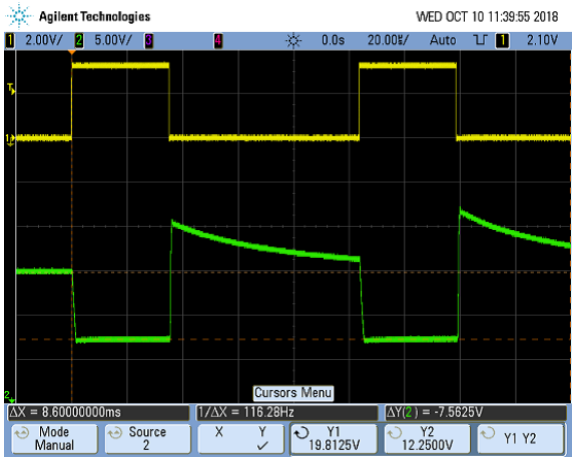


Figure 203. Upsu = 20V



Ua = 7.69V	6V ≤ Limits ≤ 9V	Ua = 7.56V	6V ≤ Limits ≤ 9V

Figure 204. Upsu = 30V

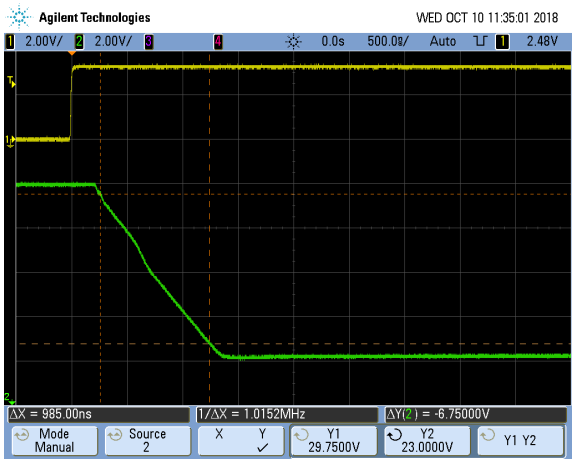
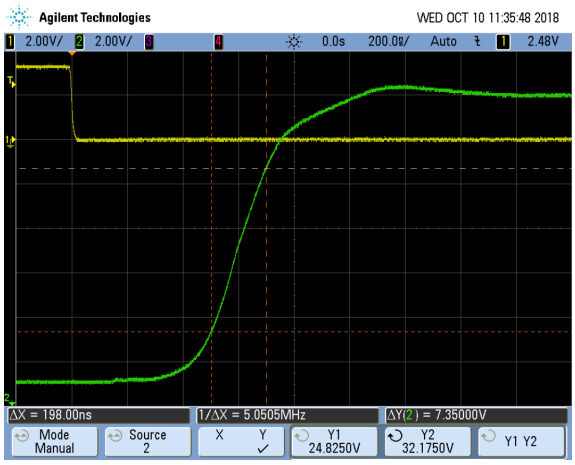


Figure 205. Upsu = 20V

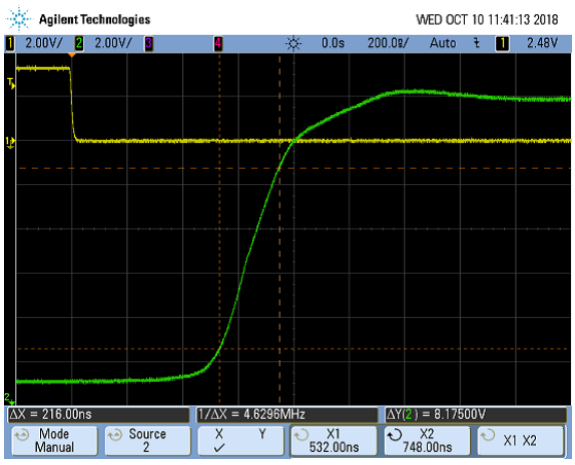
Rising slope = 6.9V/µs	1V/µs ≤ Limits ≤ 100V/µs	Rising slope = 5.7V/µs	1V/µs ≤ Limits ≤ 100V/µs

Figure 206. Upsu = 30V



Falling slope = 41V/µs | 1V/µs ≤ Limits ≤ 100V/µs

Figure 207. Upsu = 20V



Falling slope = 38V/µs | 1V/µs ≤ Limits ≤ 100V/µs

4.10 Transmitter Test (Normal Current) - Test 2 (8/2/2 - test 6.2)

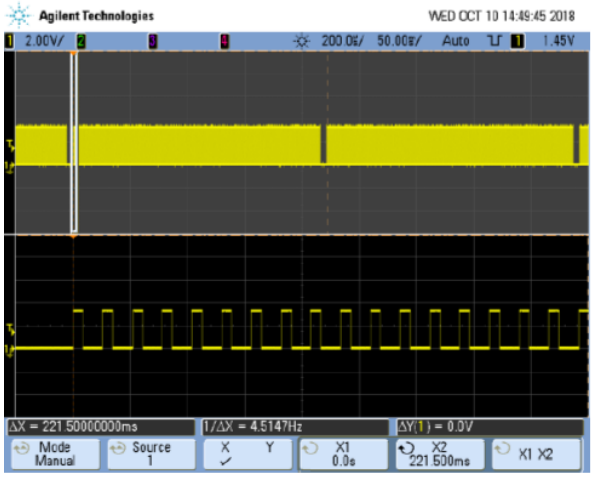
This test represents the sending of one device to the bus, which is equipped only with a few bus devices.

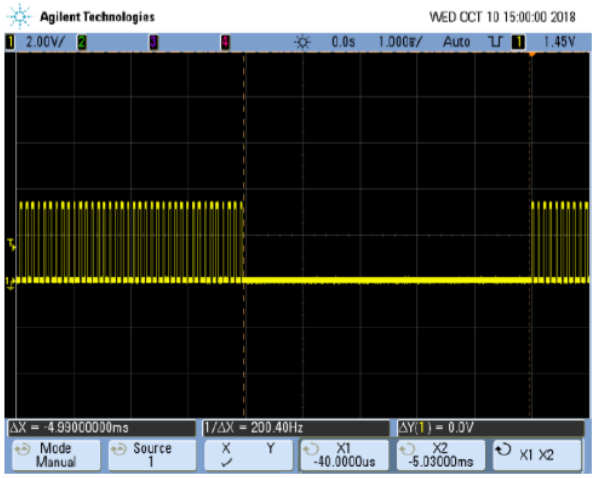
4.10.1 Test setup

The setup used is described in Section 4.10.1 Test setup, in which:

- R1 = C1 = NP
- The dedicated firmware “Zeros_x260_Frame.bin” available at www.st.com (document “Test firmwares for EVALKITSTKNX”) is loaded in the kit CPU to transmit continuously:
- the MAXDATA telegram made of 260 bytes 0x00
- a pause of x6 bytes 0xFF between each telegram.

Figure 208. MAXDATA telegram emission from CPU





4.10.2 Test results

Table 15. Transmitter Test (Normal Current) - Test 2 tests results

EVALKITSTKNX configuration			Test conditions			Test results
Fan-in	Linear regulator	DC-DC converter	Upsu	Iin (no TX)	Iin (TX)	Ua L. Limit = 6V U. Limit = 10.5V
10mA	3.3V not loaded	5V loaded with U15 to CPU section	30V	5.5mA	54mA	7.69V
10mA	3.3V not loaded	5V loaded with U15 to CPU section	20V	8.8mA	59mA	7.69V
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	30V	6.3mA	56mA	7.69V
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	20V	**10mA**	61mA	7.69V
30mA	3.3V loaded with CPU selection	5V not loaded	30V	19.8mA	78mA	7.69V
30mA	3.3V loaded with CPU selection	5V not loaded	20V	20mA	78mA	7.56V
30mA	3.3V loaded with CPU selection	5V loaded with 229Ω	30V	25mA	86mA	7.69V
30mA	3.3V loaded with CPU selection	5V loaded with 229Ω	20V	**30mA**	93mA	7.69V
			Cumulative result			PASS

4.10.2.1 *Signals waveforms for fan-in 10 mA kit*

Below are reported the waveforms of the signals on the 10 mA fan-in kit, where the DC-DC converter 5 V is supplying the CPU section through the U15 3.3 V linear regulator.

When not transmitting, Iin = 5.5 mA. During transmission, Iin = 54 mA.

The tests were also performed when charging the DC-DC output with an additional resistor in order to consume Iin = 10 mA (fan-in), but no differences were observed on signals waveforms.

Figure 209. Upsu = 30V

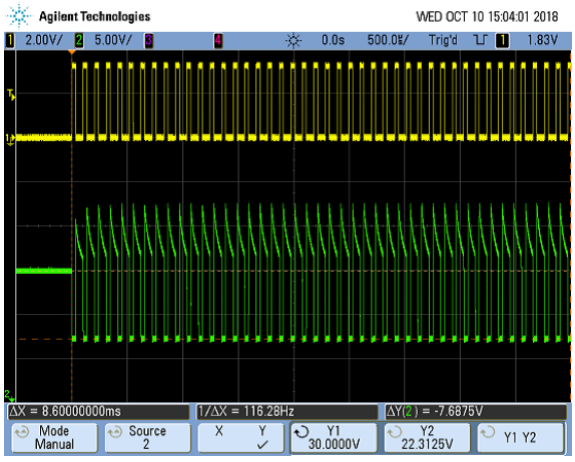


Figure 210. Upsu = 20V

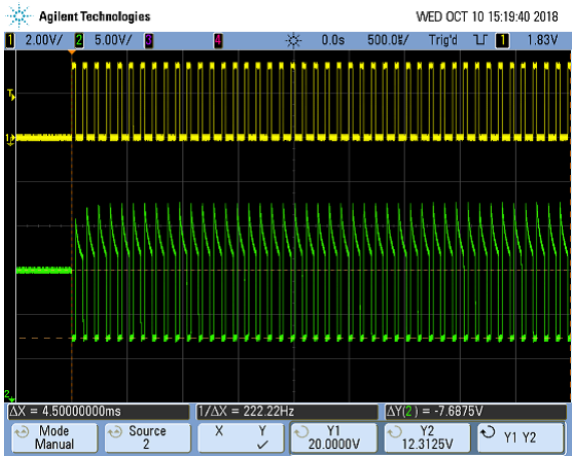
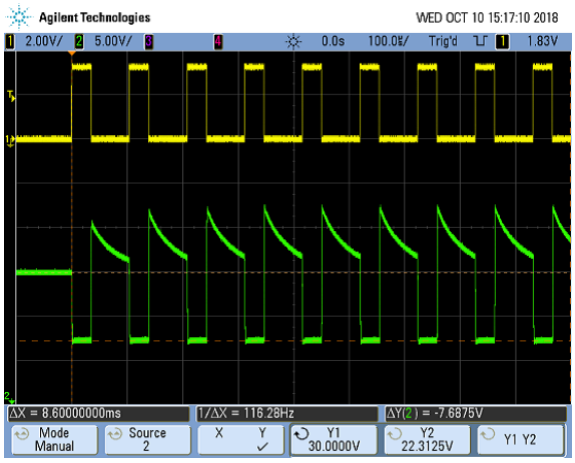
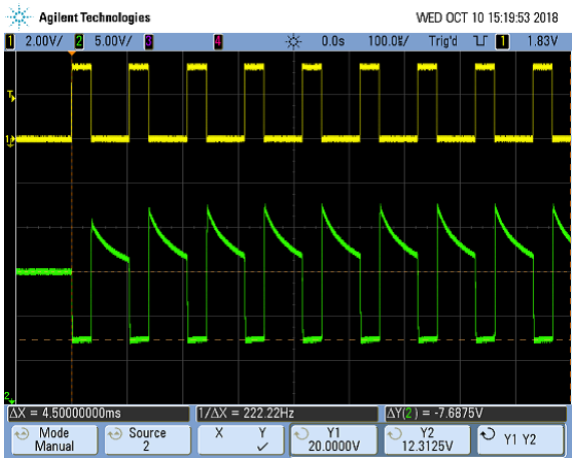


Figure 211. Upsu = 30V (zoom)



Ua = 7.69V	6V < Limits < 10.5V

Figure 212. Upsu = 20V (zoom)



Ua = 7.69V	6V < Limits < 10.5V

4.10.2.2 *Signals waveforms for fan-in 30 mA kit*

Below are reported the waveforms of the signals on the 30 mA fan-in kit, where the STKNX linear regulator is supplying the CPU section (19.2 mA consumption).

When not transmitting, Iin = 19.8 mA. During transmission, Iin = 50.5 mA.

The tests were also performed when charging the DC-DC output with a resistor in order to consume Iin = 30 mA (fan-in), but no differences were observed on signals waveforms.

Figure 213. Upsu = 30V

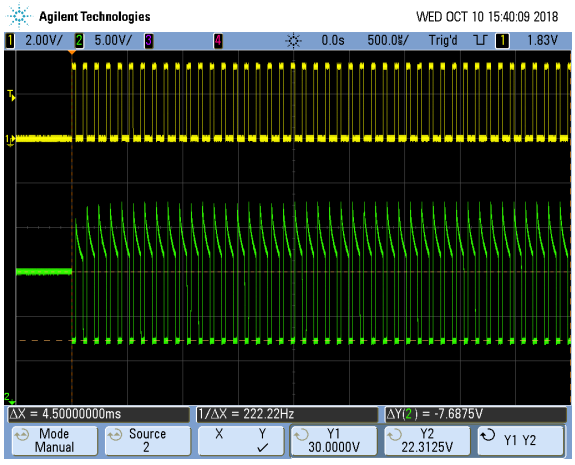


Figure 214. Upsu = 20V

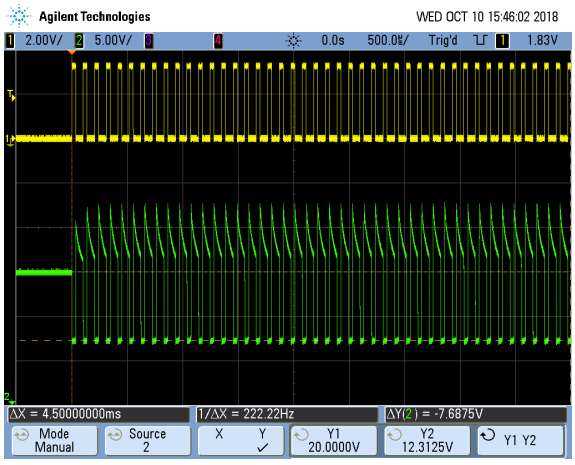
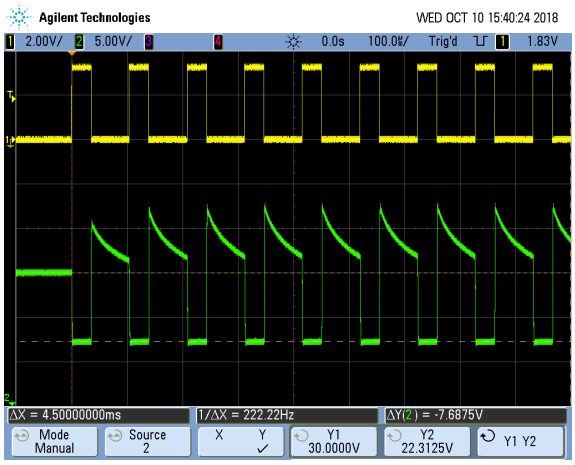
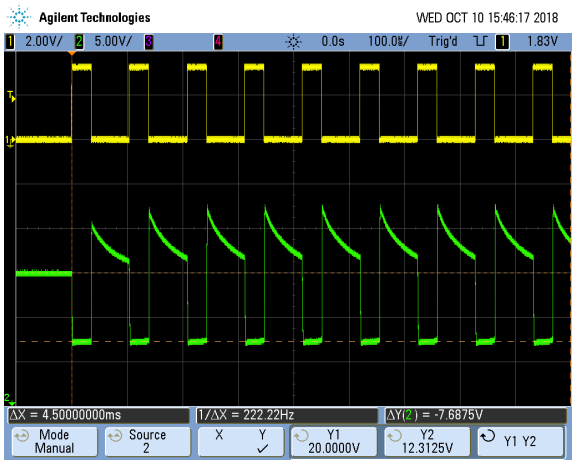


Figure 215. **Upsu = 30V (zoom)**



Ua = 7.75V (last bit) | 6V ≤ Limits ≤ 9V

Figure 216. **Upsu = 20V (zoom)**



Ua = 7.63V (last bit) | 6V ≤ Limits ≤ 9V

4.11 Transmitter Test (Maximal Current) (8/2/2 - test 6.3)

This test represents the sending of one device to the bus, which is equipped with maximal number of bus devices.

4.11.1 Test setup

The setup used is described in Section 4.8 Transmitter tests setups (8/2/2 - tests 6.1, 6.2 and 6.3), in which:

- R1 = 22 Ω
- C1 = 1000 µF

The DPT 1.001 telegram is transmitted by the CPU, see Section 4.9.1 Test setup for its description.

4.11.2 Tests results

Table 16. **Transmitter Test (Maximal Current) tests results**

EVALKITSTKNX configuration			Test conditions			Test results		
Fan-in	Linear regulator	DC-DC converter	Upsu	Iin (no TX)	Iin (TX)	Ua L. Limit (30V) = 4.5V L. Limit (20V) = 3V U. Limit = 9V	Ua rising slope L. Limit = 1V/µs U. Limit = 100V/µs	Ua rising slope L. Limit = 1V/µs U. Limit = 100V/µs
10mA	3.3V not loaded	5V loaded with U15 to CPU section	30V	5.5mA	70mA	5.3V	2.5V/µs	22V/µs
10mA	3.3V not loaded	5V loaded with U15 to CPU section	20V	8.8mA	52mA	3.4V	2.3V/µs	22V/µs
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	30V	6.3mA	71mA	5.3V	2.5V/µs	22V/µs
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	20V	**10mA**	54mA	3.4V	2.3V/µs	22V/µs

EVALKITSTKNX configuration			Test conditions			Test results		
Fan-in	Linear regulator	DC-DC converter	Upsu	Iin (no TX)	Iin (TX)	Ua L. Limit (30V) = 4.5V L. Limit (20V) = 3V U. Limit = 9V	Ua rising slope L. Limit = 1V/µs U. Limit = 100V/µs	Ua rising slope L. Limit = 1V/µs U. Limit = 100V/µs
30mA	3.3V loaded with CPU selection	5V not loaded	30V	19.8mA	67mA	5.3V	2.5V/µs	20V/µs
30mA	3.3V loaded with CPU selection	5V not loaded	20V	20mA	66mA	3.6V	2V/µs	20V/µs
30mA	3.3V loaded with CPU selection	5V loaded with 213Ω	30V	26mA	94mA	5.3V	2.5V/µs	20V/µs
30mA	3.3V loaded with CPU selection	5V loaded with 213Ω	20V	**30mA**	79mA	3.4V	2V/µs	20V/µs
			Cumulative result			PASS		

4.11.2.1 *Signals waveforms for fan-in 10 mA kit*

Below are reported the waveforms of the signals on the 10 mA fan-in kit, where the DC-DC converter 5 V is supplying the CPU section through the U15 3.3 V linear regulator.

When not transmitting, Iin = 5.5 mA. During transmission, Iin = 32 mA.

The tests were also performed when charging the DC-DC output with an additional resistor in order to consume Iin = 10 mA (fan-in), but no differences were observed on signals waveforms.

Figure 217. Upsu = 30V

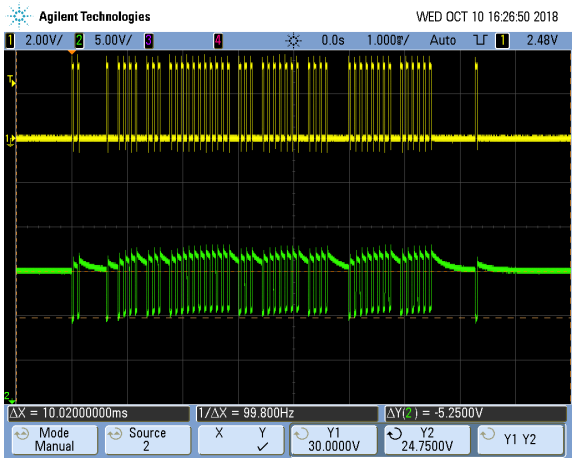


Figure 218. Upsu = 20V

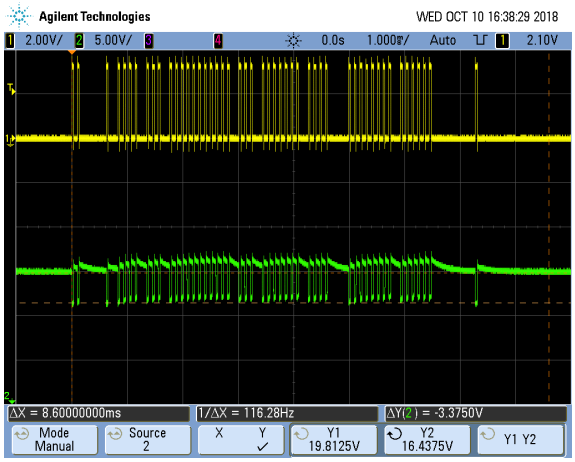
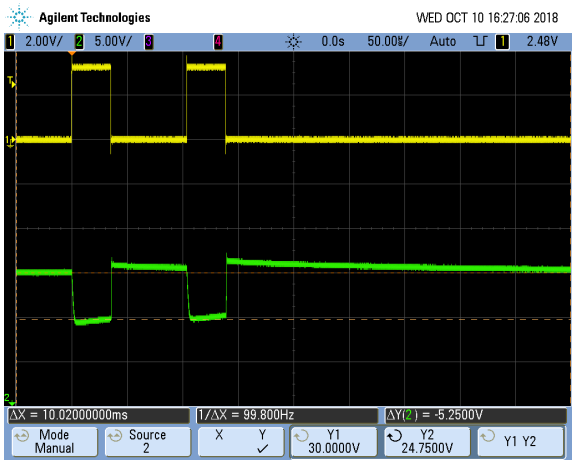
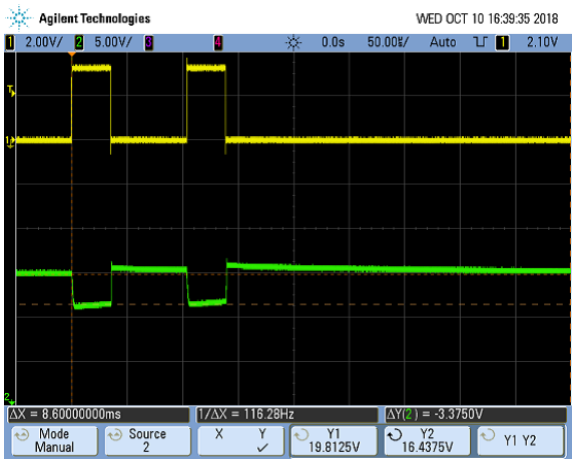


Figure 219. Upsu = 30V (zoom)



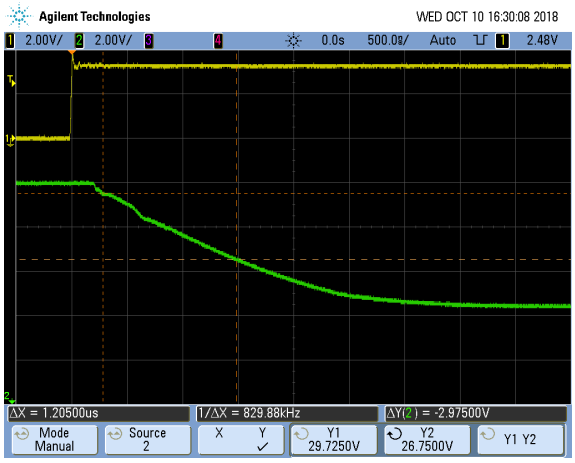
Ua = 5.25V	4.5V ≤ Limits ≤ 9V

Figure 220. Upsu = 20V (zoom)



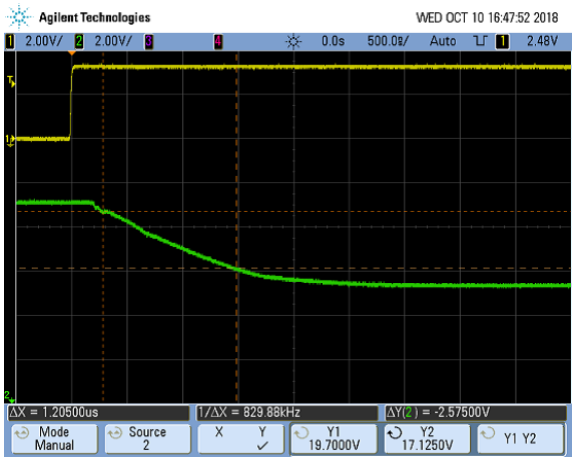
Ua = 3.4V	3V ≤ Limits ≤ 9V

Figure 221. Upsu = 30V



Rising slope = 2.5V/µs	1V/µs ≤ Limits ≤ 100V/µs

Figure 222. Upsu = 20V



Rising slope = 2.3V/µs	1V/µs ≤ Limits ≤ 100V/µs

Figure 223. Upsu = 30V

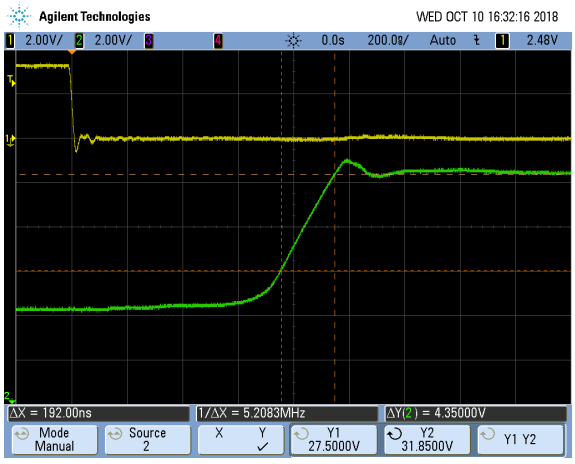
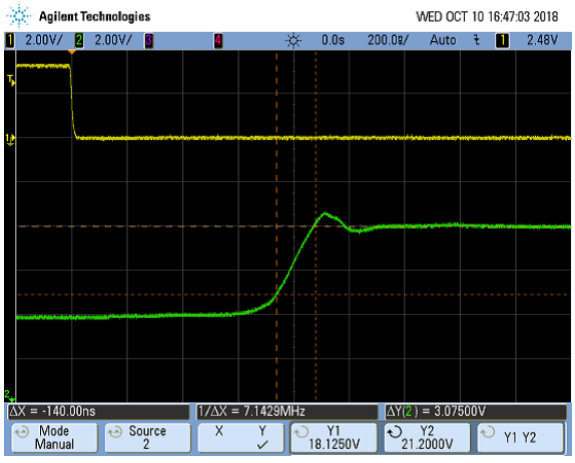


Figure 224. Upsu = 20V



Falling slope = 22V/µs	1V/µs ≤ Limits ≤ 100V/µs	Falling slope = 22V/µs	1V/µs ≤ Limits ≤ 100V/µs

4.11.2.2 *Signals waveforms for fan-in 30 mA kit*

Below are reported the waveforms of the signals on the 30 mA fan-in kit, where the STKNX linear regulator is supplying the CPU section (19.2 mA consumption).

When not transmitting, Iin = 19.8 mA. During transmission, Iin = 50.5 mA.

The tests were also performed when charging the DC-DC output with a resistor in order to consume Iin = 30 mA (fan-in), but no differences were observed on signals waveforms.

Figure 225. Upsu = 30V

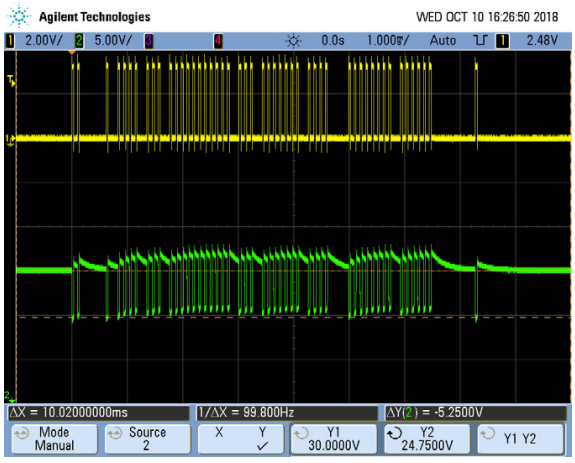


Figure 226. Upsu = 20V

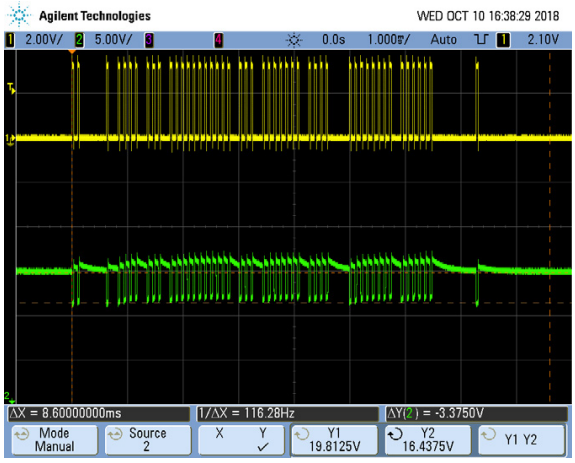


Figure 227. Upsu = 30V

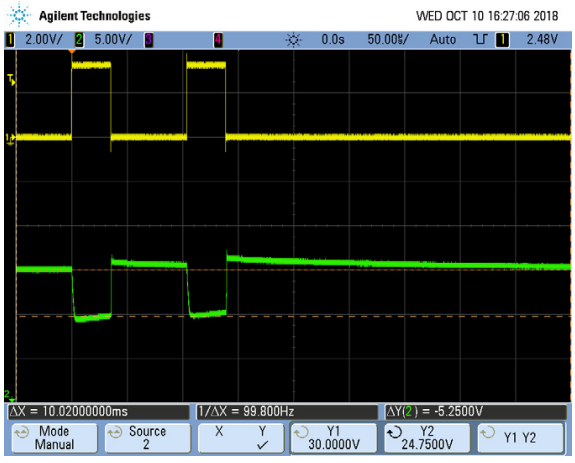
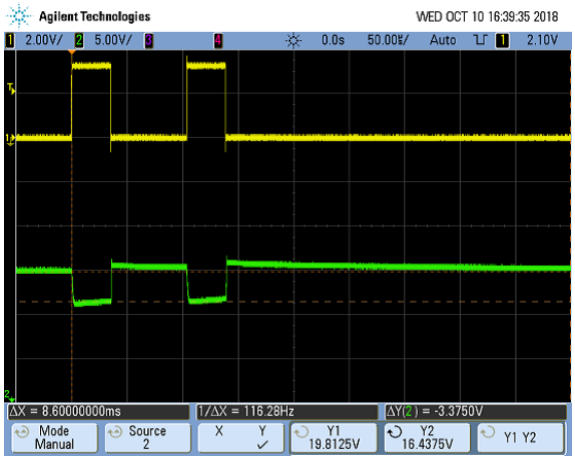
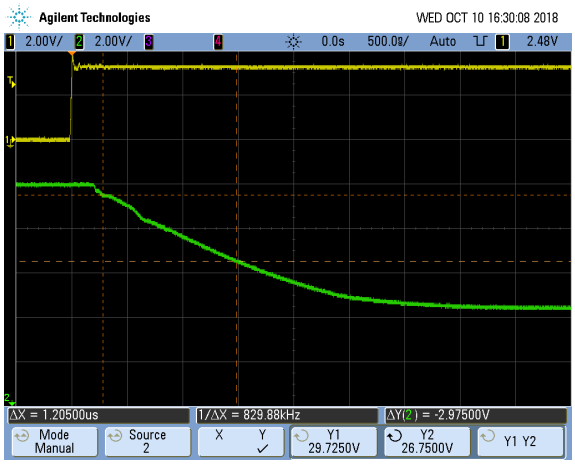


Figure 228. Upsu = 20V



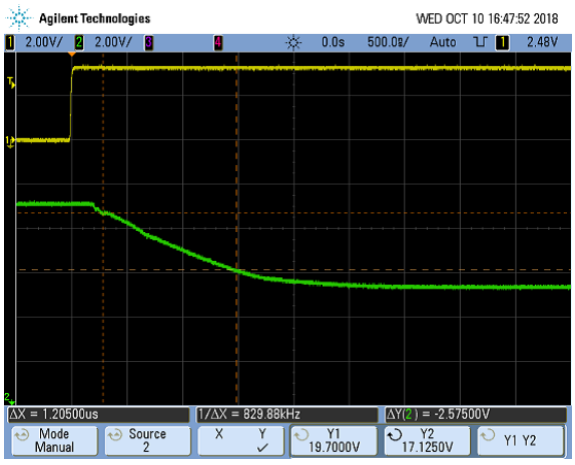
Ua = 5.25V	4.5V ≤ Limits ≤ 9V	Ua = 3.4V	3V ≤ Limits ≤ 9V

Figure 229. Upsu = 30V



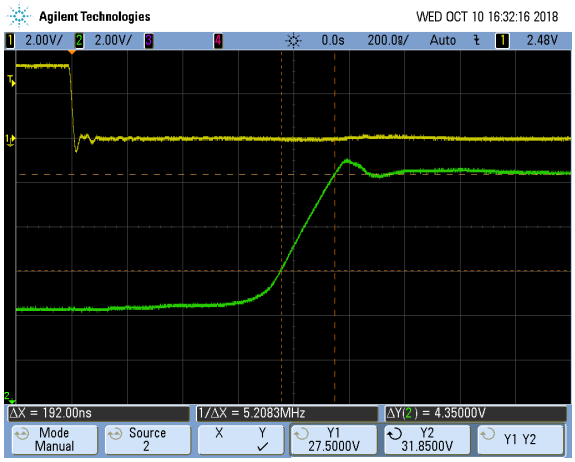
Rising slope = 2.5V/µs	1V/µs ≤ Limits ≤ 100V/µs

Figure 230. Upsu = 20V



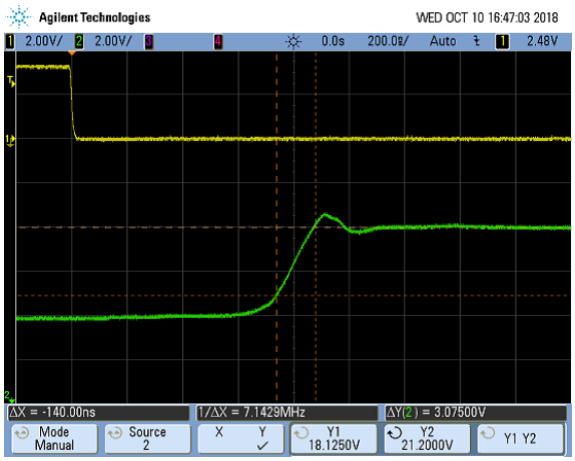
Rising slope = 2.3V/µs	1V/µs ≤ Limits ≤ 100V/µs

Figure 231. Upsu = 30V



Falling slope = 22V/µs	1V/µs ≤ Limits ≤ 100V/µs

Figure 232. Upsu = 20V



Falling slope = 22V/µs	1V/µs ≤ Limits ≤ 100V/µs

4.12 Transmitter Test (Minimal Current) (8/2/2 - test 6.4)

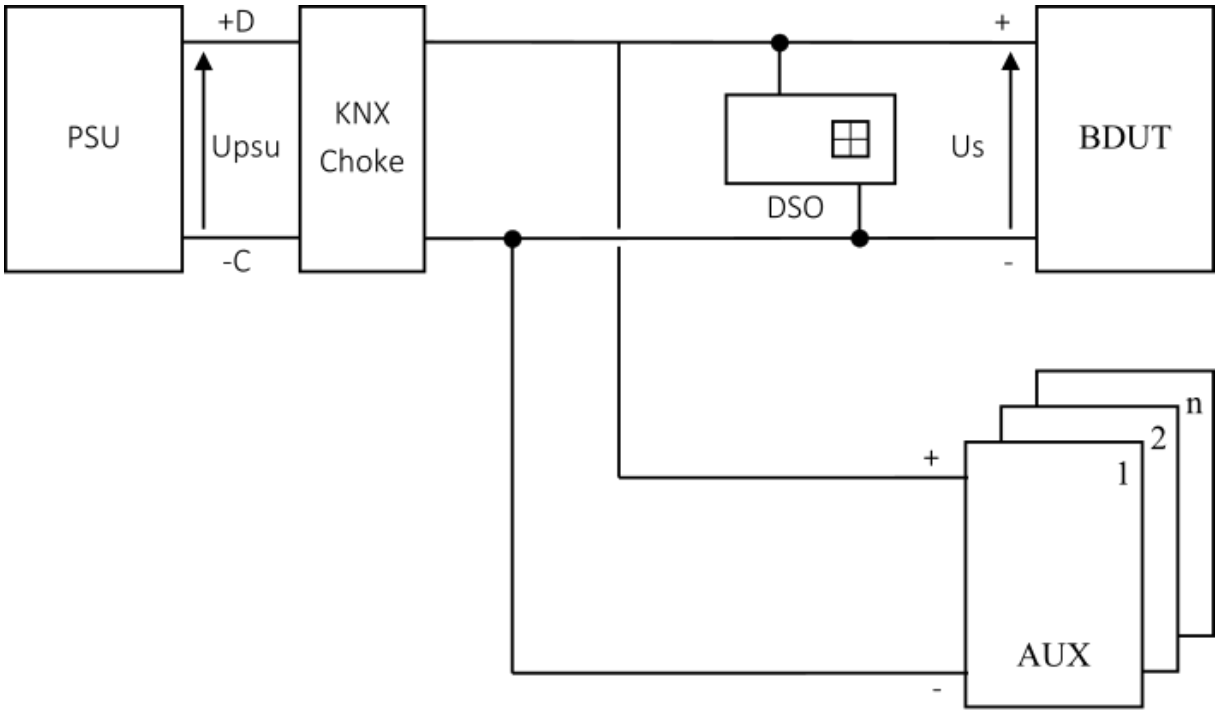
This test represents the simultaneous sending of the maximum number of devices at a bus segment.

The test requires a setup with 255 connected devices and was performed with the STKNX board used for KNX certification. It has not been repeated with the EVALKITSTKNX.

The results obtained with the certification board are shown below. No substantial difference is expected with the EVALKITSTKNX.

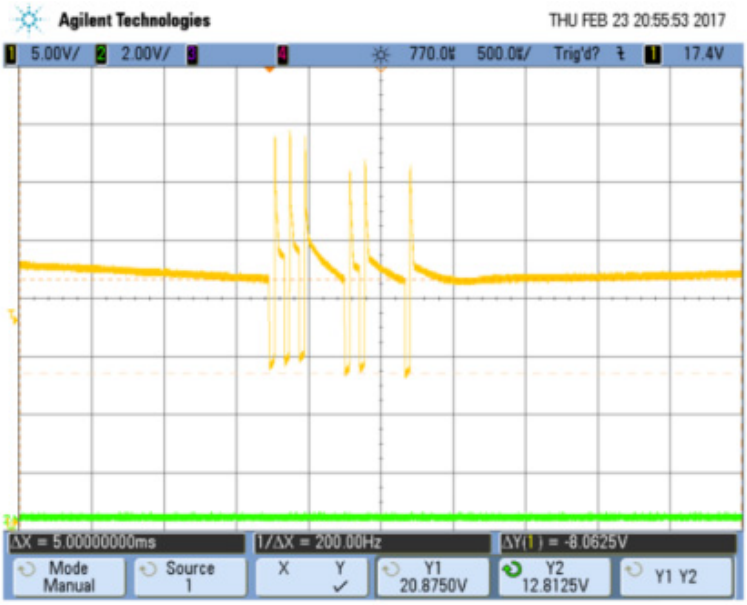
4.12.1 Test setup

Figure 233. **Transmitter test setup (minimal current)**



4.12.2 Tests results

Figure 234. **Upsu = 25V**



CH1: Us	
Ua min = 6.5V	Limit = 6V min
Ua max = 8.1V	Limit = 10.5V max

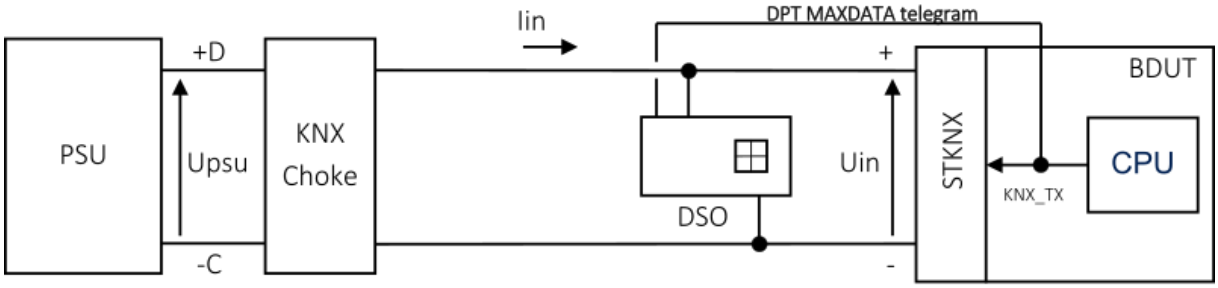
Ue min = 9.5V	Limit = 4V min
Ue max = 12.7V	Limit = 14.5V max
Cumulative results:	PASS

4.13 Propagation Delay (Transmitter) (8/2/2 - test 7.1)

This test checks the internal delay of the transmitter.

4.13.1 Test setup

Figure 235. Transmitter propagation delay test setup



Oscilloscope channels:

- CH1: KNX_TX (U12 AND gate output)(1)
- CH2: Uin

1. *the additional propagation delay in the gate is 8 ns maximum.*

The dedicated firmware “Zeros_x260_Frame.bin” available at www.st.com (document “Test firmwares for EVALKITSTKNX”) is loaded in the kit. See Section 4.10.1 Test setup for its description.

In non-isolated mode, the kit setting is identical to the setup described in Section 4.8 Transmitter tests setups (8/2/2 - tests 6.1, 6.2 and 6.3).

When the optocoupler is used, the following BOM modifications are applied.

- M11 open
- R1, R8, R5 populated
- CPU section is supplied from USB cable: J20.2-3 closed, J19.2-3 closed, every other supply jumpers open.

4.13.2 Tests results

Table 17. Transmitter Propagation Delay tests results

EVALKITSTKNX configuration				Test conditions		Test results	
Fan-in	Linear regulator	DC-DC converter	Optocoupler	Upsu	Iinx (no TX)	td1 Limit = 1µs	td2 Limit = 3µs
10mA	3.3V not loaded	5V loaded with U15 to CPU section	Not used	30V	5.5mA	206ns	412ns
10mA	3.3V not loaded	5V loaded with U15 to CPU section	Not used	20V	8.8mA	192ns	594ns
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	Not used	30V	6.3mA	206ns	412ns
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	Not used	20V	**10mA**	192ns	594ns

EVALKITSTKNX configuration				Test conditions		Test results	
Fan-in	Linear regulator	DC-DC converter	Optocoupler	Upsu	Iinx (no TX)	td1 Limit = 1µs	td2 Limit = 3µs
30mA	3.3V loaded with CPU section	5V not loaded	Not used	30V	20mA	233ns	434ns
30mA	3.3V loaded with CPU section	5V not loaded	Not used	20V	20mA	218ns	616ns
30mA	3.3V loaded with CPU section	5V loaded with 213Ω	Not used	30V	26mA	233ns	434ns
30mA	3.3V loaded with CPU section	5V loaded with 213Ω	Not used	20V	**30mA**	218ns	616ns
10mA	Loaded with isolators	Not loaded	Included	30V	3mA	243ns	536ns
10mA	Loaded with isolators	Not loaded	Included	20V	3mA	244ns	662ns
10mA	Loaded with isolators	Not loaded	Included	30V	6.3mA	233ns	434ns
10mA	Loaded with isolators	Not loaded	Included	20V	**10mA**	218ns	616ns
30mA	Loaded with isolators	Not loaded	Included	30V	3mA	258ns	540ns
30mA	Loaded with isolators	Not loaded	Included	20V	3mA	238ns	668ns
30mA	Loaded with isolators	Not loaded	Included	30V	26mA	258ns	540ns
30mA	Loaded with isolators	Not loaded	Included	20V	**30mA**	238ns	668ns
				Cumulative result	PASS		

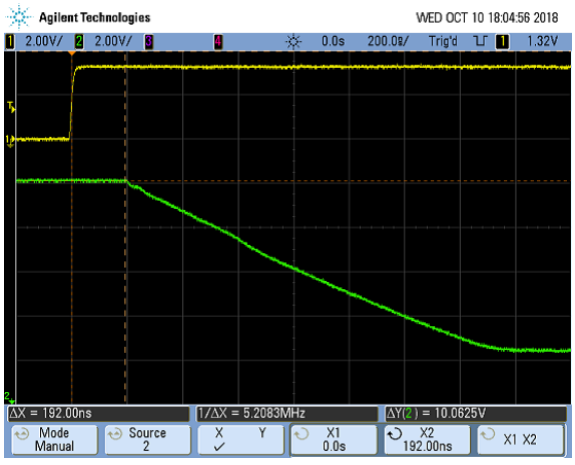
4.13.2.1 *Signals waveforms for fan-in 10mA kit - not isolated*

Below are reported the waveforms of the signals KNX_TX (U12 AND gate output) and Uin (AC and DC part) on the 10mA fan-in kit, when the optocoupler is not used.

Figure 236. Upsu = 30V

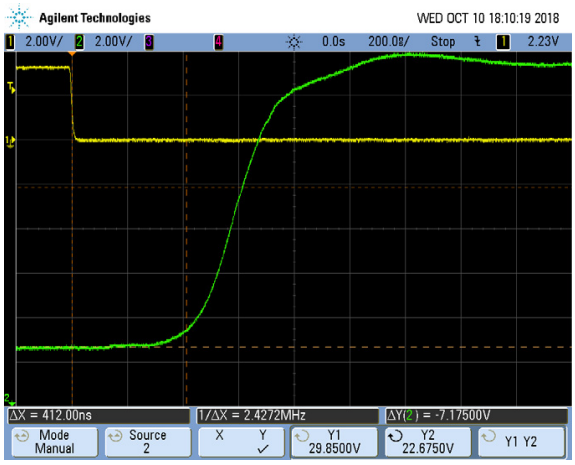
td1 = 206ns | Limits = 1µs max

Figure 237. Upsu = 20V



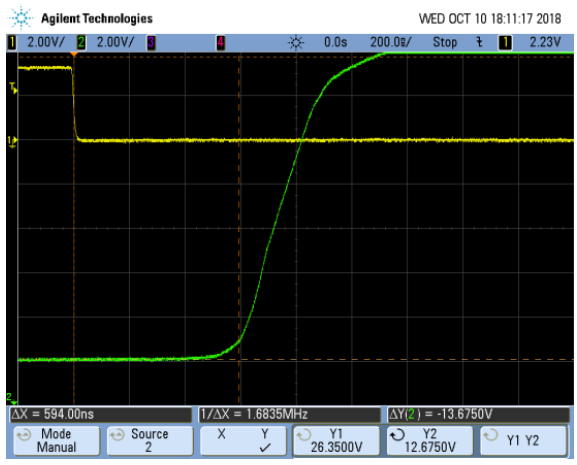
td1 = 192ns | Limits = 3µs max

Figure 238. Upsu = 30V



td1 = 412ns | Limits = 1µs max

Figure 239. Upsu = 20V

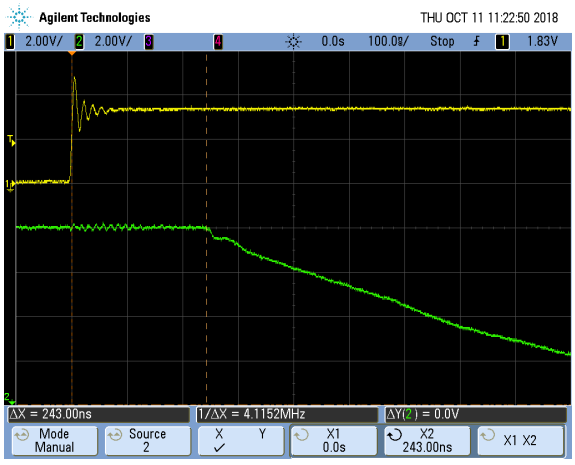


td1 = 594ns | Limits = 3µs max

4.13.2.2 *Signals waveforms for fan-in 10mA kit - isolated*

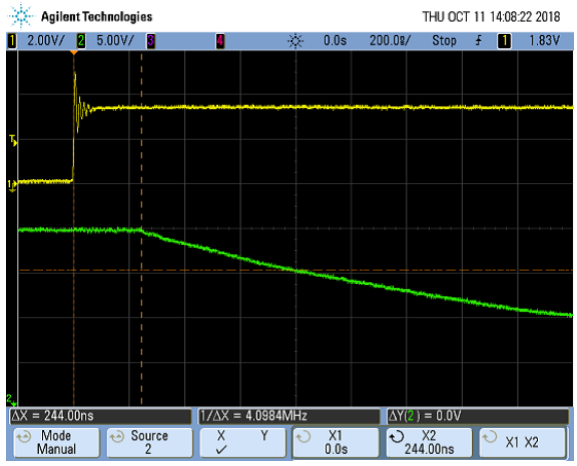
Below are reported the waveforms of the signals KNX_TX (U12 AND gate output) and Uin (AC and DC part) on the 10mA fan-in kit, when the optocoupler is used.

Figure 240. Upsu = 30V



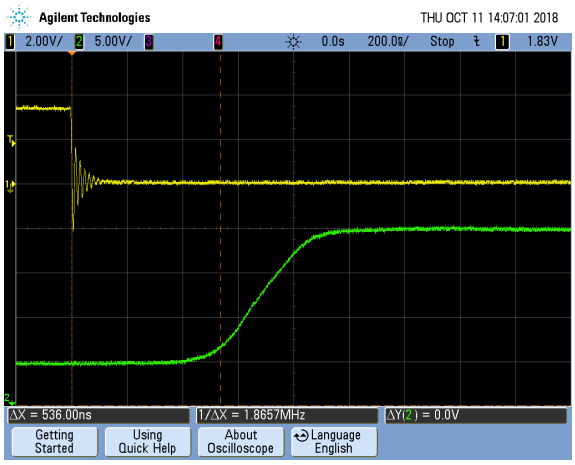
td1 = 243ns | Limits = 1µs max

Figure 241. Upsu = 20V



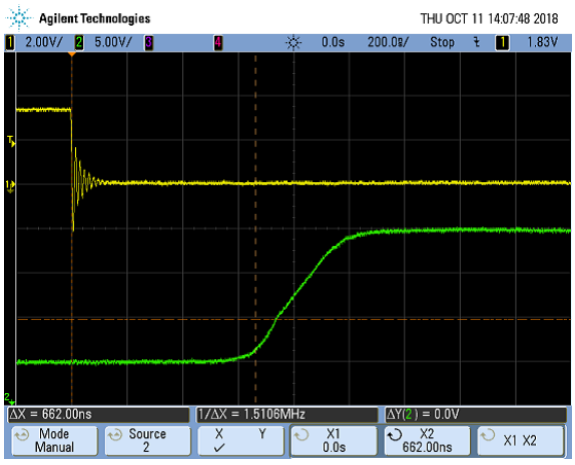
td1 = 244ns | Limits = 3µs max

Figure 242. Upsu = 30V



td1 = 536ns | Limits = 1µs max

Figure 243. Upsu = 20V

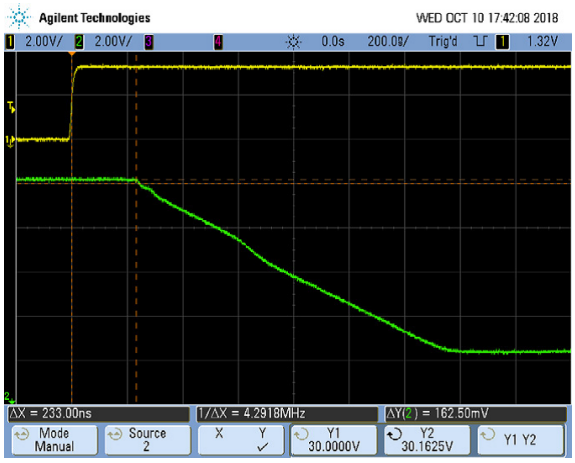


td1 = 662ns | Limits = 3µs max

4.13.2.3 *Signals waveforms for fan-in 30mA kit - not isolated*

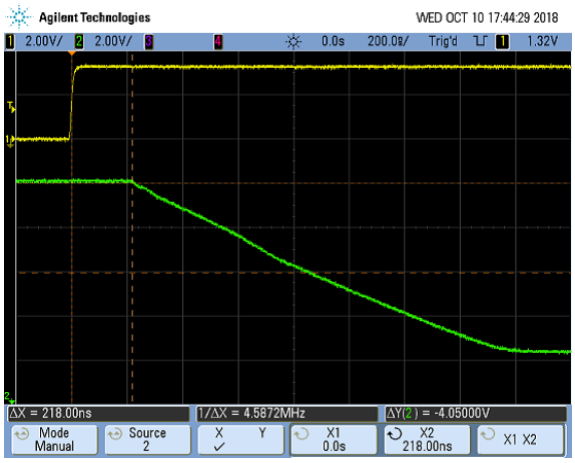
Below are reported the waveforms of the signals KNX_TX (U12 AND gate output) and Uin (AC and DC part) on the 10mA fan-in kit, when the optocoupler is not used.

Figure 244. Upsu = 30V



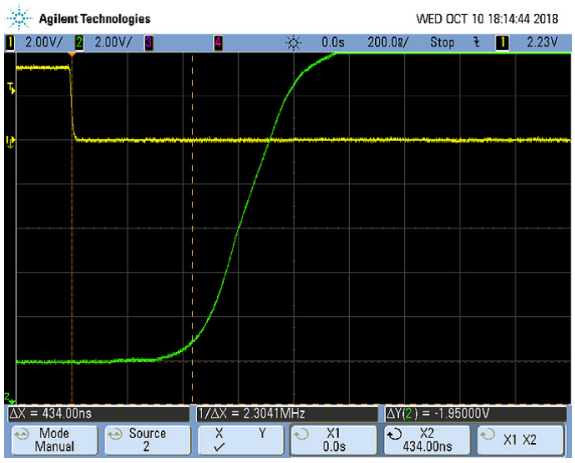
td1 = 233ns | Limits = 1µs max

Figure 245. Upsu = 20V



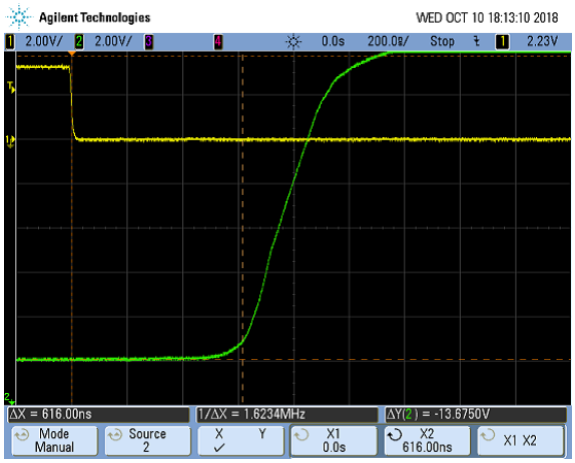
td1 = 218ns | Limits = 3µs max

Figure 246. Upsu = 30V



td1 = 434ns | Limits = 1µs max

Figure 247. Upsu = 20V

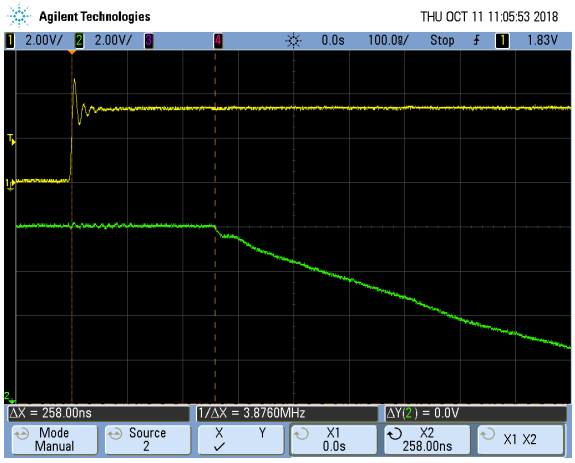


td1 = 616ns | Limits = 3µs max

4.13.2.4 *Signals waveforms for fan-in 30mA kit - isolated*

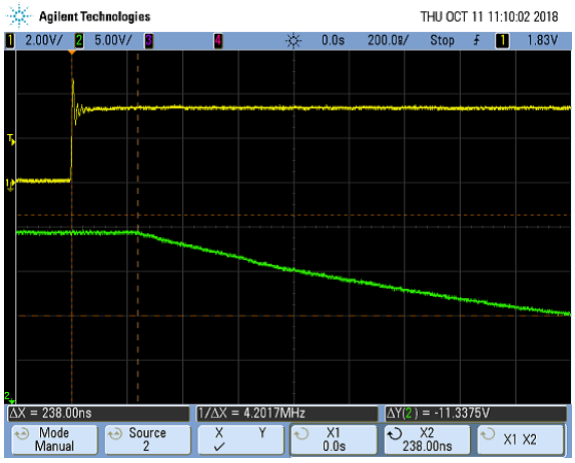
Below are reported the waveforms of the signals KNX_TX (U12 AND gate output) and Uin (AC and DC part) on the 10mA fan-in kit, when the optocoupler is used.

Figure 248. Upsu = 30V



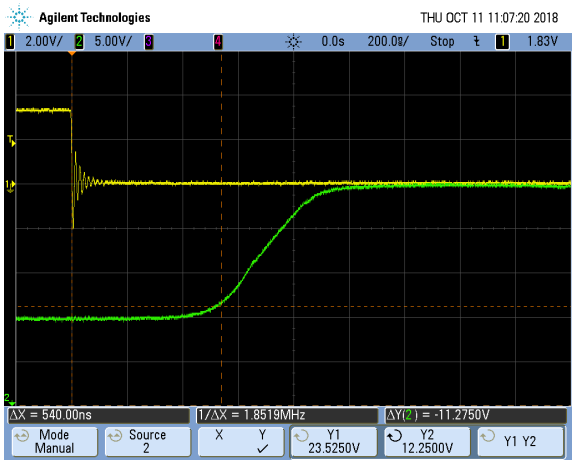
td1 = 258ns | Limits = 1µs max

Figure 249. Upsu = 20V



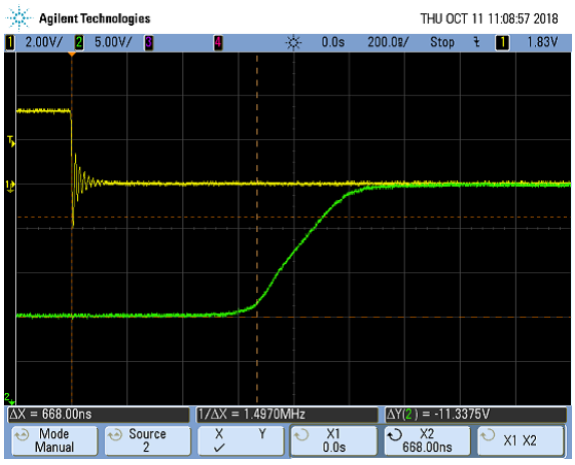
td1 = 238ns | Limits = 3µs max

Figure 250. Upsu = 30V



td1 = 540ns | Limits = 1µs max

Figure 251. Upsu = 20V



td1 = 668ns | Limits = 3µs max

4.14 Propagation Delay (Receiver) (8/2/2 - test 7.2)

This test checks the internal delay of the receiver.

4.14.1 Test setup

The setup is identical to the sensitivity test described in Section 4.7.1 Test setup. The only difference is the AWG sending a continuous series of zero bits at the bus, with two distincts amplitudes values for Ua: Ua = 10V and Ua = 0.7V:

- Oscilloscope channels:
  - CH1: Uin
  - CH2: KNX_RX (CPU input PA0)

Figure 252. Ua = 10V

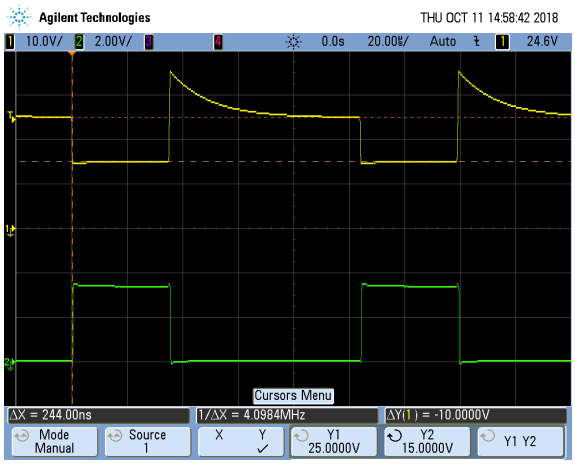
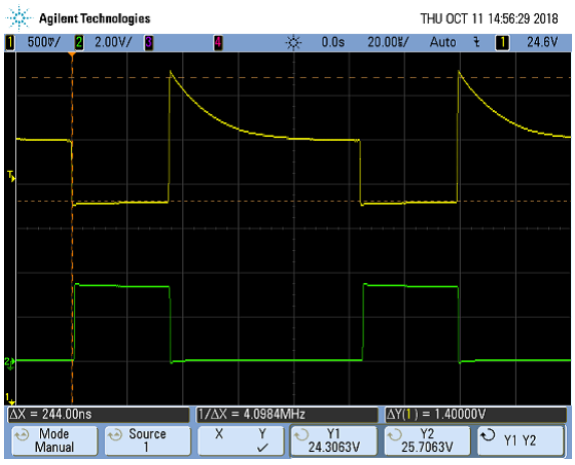


Figure 253. Ua = 0.7V



In non-isolated mode, the kit setting is the one described in Section 4.14.1 Test setup. When the optocoupler is used, the following BOM modifications are applied

- M10 open
- R3, R6, R8, R5 populated
- CPU section is supplied from USB cable: J20.2-3 closed, J19.2-3 closed, every other supply jumpers open

4.14.2 Tests results

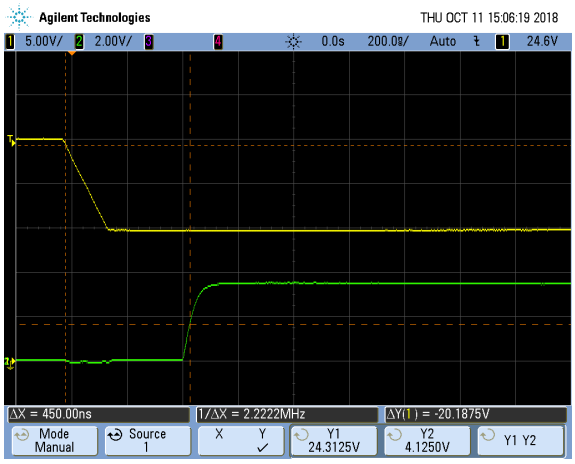
Table 18. Receiver Propagation Delay tests results

EVALKITSTKNX configuration				Test conditions		Test results			
Fan-in	Linear regulator	DC-DC converter	Optocoupler	Ua (Upsu=25V)	Iin (no TX)	Vh	Vl	td1 Limit = 3µs/ Ua=10V Limit = 5µs/ Ua=0.7V	td2 Limit = 3µs
10mA	3.3V not loaded	5V loaded with U15 to CPU section	Not used	10V	5mA	3.4V	50mV	450ns	466ns
10mA	3.3V not loaded	5V loaded with U15 to CPU section	Not used	0.7V	5mA	3.4V	50mV	928ns	382ns
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	Not used	10V	6.3mA	3.4V	50mV	450ns	466ns
10mA	3.3V not loaded	5V loaded with U15 to (CPU section // 1.4kΩ)	Not used	0.7V	**10mA**	3.4V	50mV	928ns	382ns
30mA	3.3V loaded with CPU section	5V not loaded	Not used	10V	3mA	3.32V	50mV	450ns	466ns
30mA	3.3V loaded with CPU section	5V not loaded	Not used	0.7V	26mA	3.3V	25mV	894ns	396ns
30mA	3.3V loaded with CPU section	5V loaded with 213Ω	Not used	10V	26mA	3.32V	50mV	450ns	466ns
30mA	3.3V loaded with CPU section	5V loaded with 213Ω	Not used	0.7V	**30mA**	3.3V	25mV	894ns	396ns
10mA	Loaded with isolators	Not loaded	Included	10V	5mA	3.3V	25mV	484ns	524ns
10mA	Loaded with isolators	Not loaded	Included	0.7V	5mA	3.25V	75mV	968ns	444ns
10mA	Loaded with isolators	Not loaded	Included	10V	6.3mA	3.3V	25mV	484ns	524ns
10mA	Loaded with isolators	Not loaded	Included	0.7V	**10mA**	3.25V	75mV	968ns	444ns
30mA	Loaded with isolators	Not loaded	Included	10V	3mA	3.3V	25mV	482ns	524ns
30mA	Loaded with isolators	Not loaded	Included	0.7V	3mA	3.25V	75mV	904ns	448ns
30mA	Loaded with isolators	Not loaded	Included	10V	26mA	3.3V	25mV	482ns	524ns
30mA	Loaded with isolators	Not loaded	Included	0.7V	**30mA**	3.25V	75mV	904ns	448ns
				Cumulative result	PASS				

4.14.2.1 *Signals waveforms for fan-in 10mA kit - not isolated*

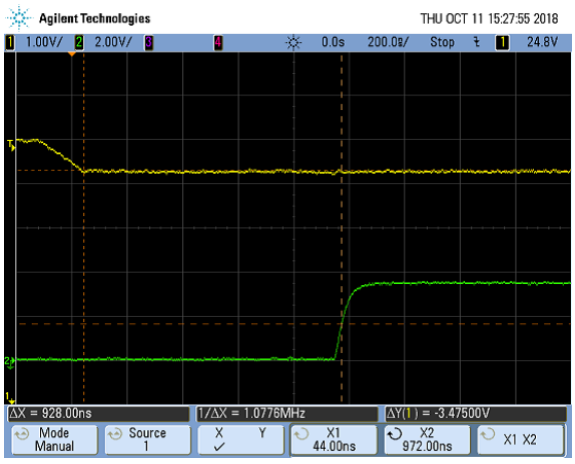
Below are reported the waveforms of the signals Uin (AC and DC part) and KNX_RX (CPU input PA0) on the 10mA fan-in kit, when the optocoupler is not used.

Figure 254. Ua = 10V



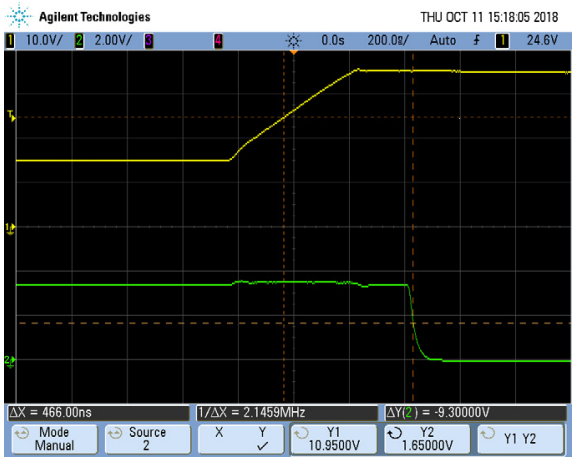
td1 = 450ns	Limits = 3µs max

Figure 255. Ua = 0.7V



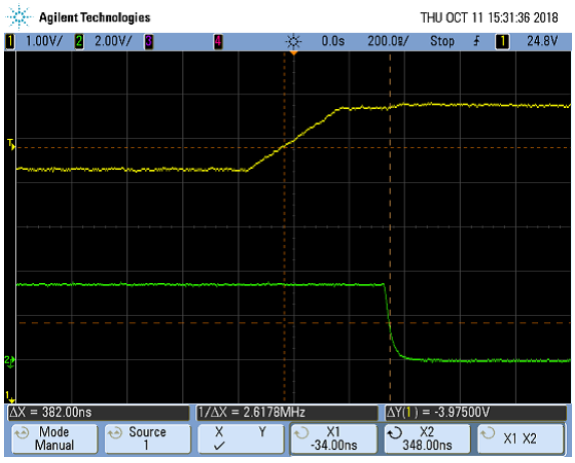
td1 = 928ns	Limits = 5µs max

Figure 256. Ua = 10V



td2 = 466ns	Limits = 3µs max

Figure 257. Ua = 0.7V

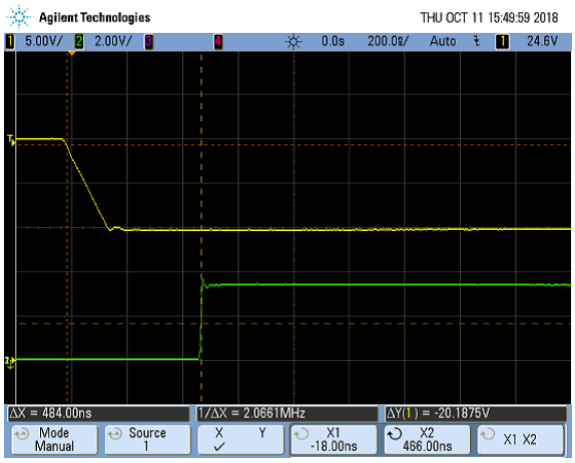


td2 = 382ns	Limits = 3µs max

4.14.2.2 *Signals waveforms for fan-in 10mA kit - isolated*

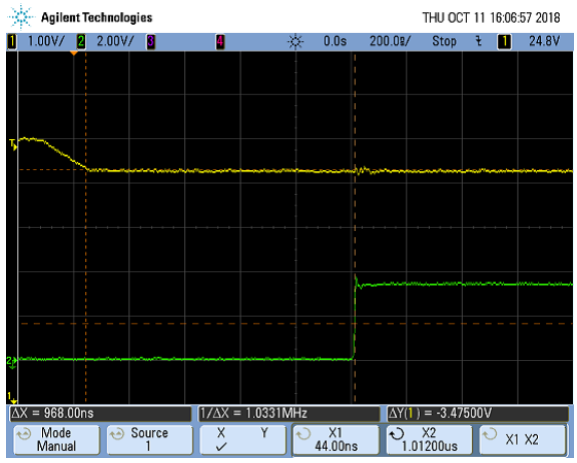
Below are reported the waveforms of the signals Uin (AC and DC part) and KNX_RX (CPU input PA0) on the 10mA fan-in kit, when the optocoupler is used.

Figure 258. Ua = 10V



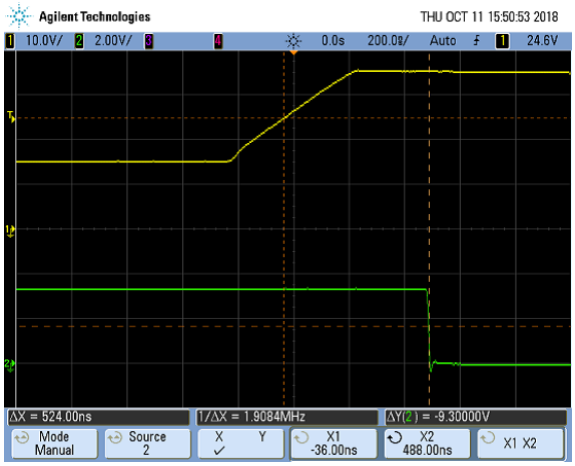
td1 = 484ns | Limits = 3µs max

Figure 259. Ua = 0.7V



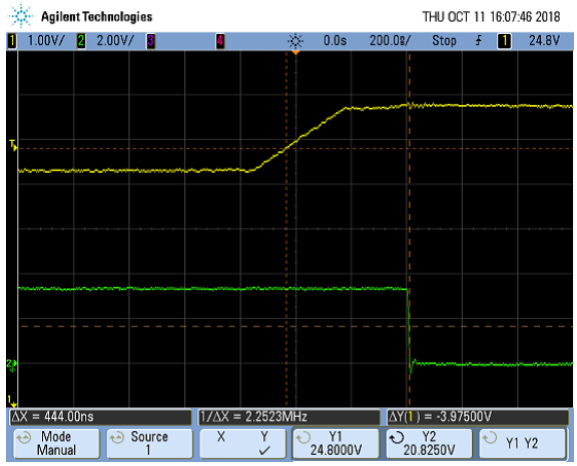
td1 = 968ns | Limits = 5µs max

Figure 260. Ua = 10V



td2 = 524ns | Limits = 3µs max

Figure 261. Ua = 0.7V

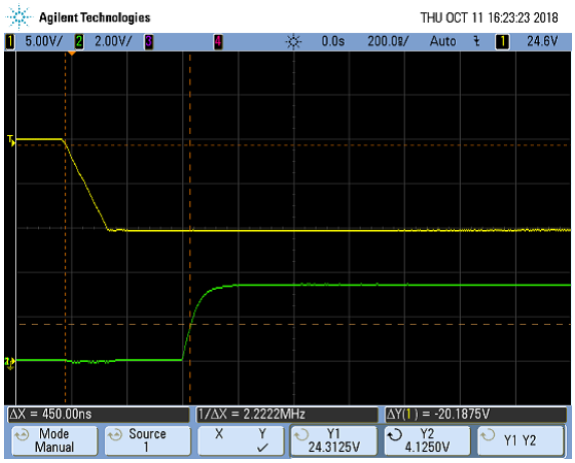


td2 = 444ns | Limits = 3µs max

4.14.2.3 *Signals waveforms for fan-in 30 mA kit - not isolated*

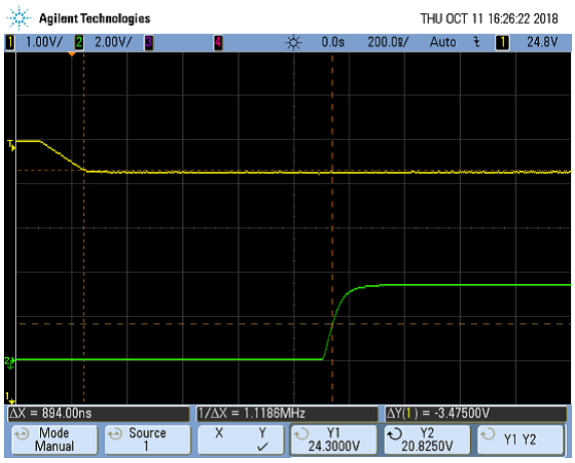
Below are reported the waveforms of the signals Uin (AC and DC part) and KNX_RX (CPU input PA0) on the 30 mA fan-in kit, when the optocoupler is not used.

Figure 262. Ua = 10V



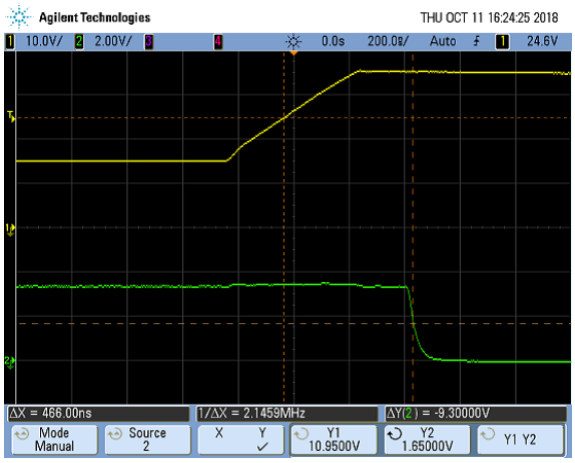
td1 = 450ns	Limits = 3µs max

Figure 263. Ua = 0.7V



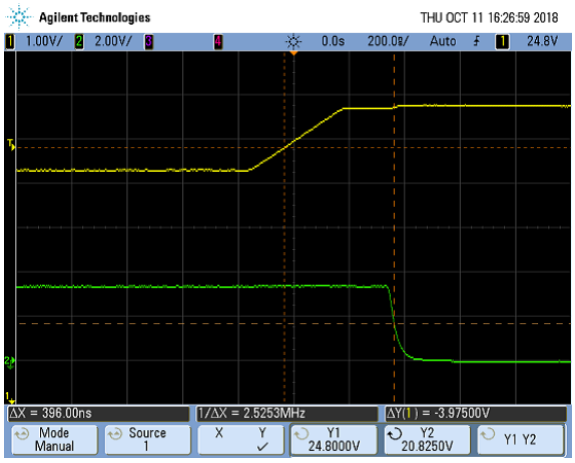
td1 = 894ns	Limits = 5µs max

Figure 264. Ua = 10V



td2 = 466ns	Limits = 3µs max

Figure 265. Ua = 0.7V

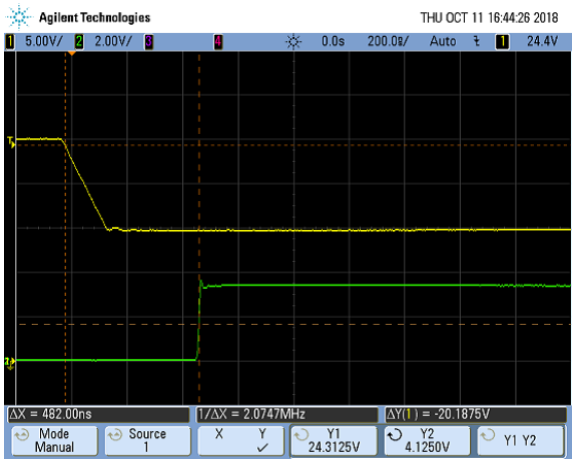


td2 = 396ns	Limits = 3µs max

4.14.2.4 *Signals waveforms for fan-in 30 mA kit - isolated*

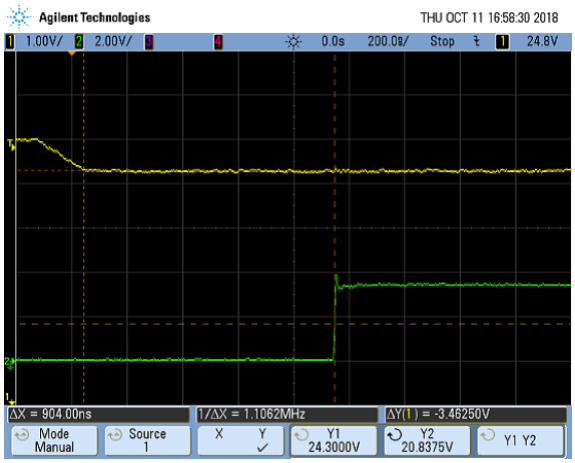
Below are reported the waveforms of the signals Uin (AC and DC part) and KNX_RX (CPU input PA0) on the 10 mA fan-in kit, when the optocoupler is used.

Figure 266. Ua = 10V



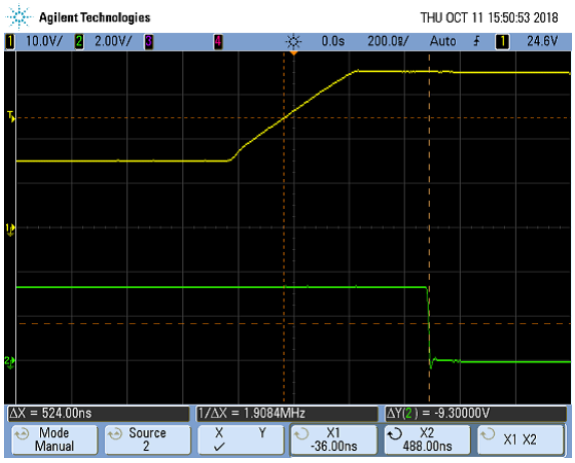
td1 = 482ns	Limits = 3µs max

Figure 267. Ua = 0.7V



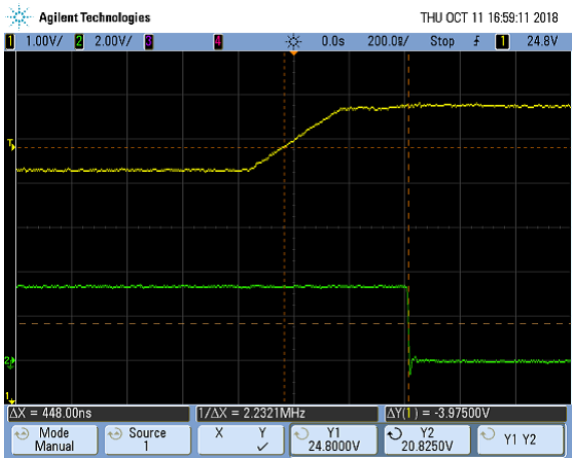
td1 = 904ns	Limits = 5µs max

Figure 268. Ua = 10V



td2 = 524ns	Limits = 3µs max

Figure 269. Ua = 0.7V



td2 = 448ns	Limits = 3µs max

5 References

8/2/2 KNX System Conformance Testing - Medium Dependant Layers Tests - TP1 Physical and Link Layer Tests - Version 01.04.02 AS.

9/1 Basic and System Components/Devices - Minimum Requirements - Standardized solutions - Tests KNX System Conformance Testing - Cables and Connectors – Version 01.02.01 AS.

Revision history

Table 19. **Revision history**

Date	Revision	Changes
19-Apr-2019	1	Initial release.
06-Nov-2019	2	Change to Section 3.3: CPU section, Section 3.3.1: KNX_TX signal generation, Section : 3.3.1.1 KNX_TX generated from AND gate and Section : 3.3.1.2 KNX_TX generated from one single GPIO (no AND gate). Additional bullet point added to Section : 3.6.4.4. Dimming mode (application example)
09-Jan-2021	3	In Section 3.2.2 Layout recommendations - updated Figure 9. STKNX area routed using top and bottom layers only - updated bullet point :"Keep the following power loops short:" - updated Figure 10. Layout recommendations description - updated Figure 11. Layout recommendations application

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