AN5280
Application note

36W USB charger with selectable output voltage (5-9-12 V @3A) based on STCH03L and SRK1000B

Introduction

This application note describes a 36 W, wide input voltage range, USB charger demonstration board, with selectable output voltage (5-9-12 V – @ 3 A output current), based on the STCH03L (with latched type OVP) and the SRK1000B. The operation and the results of the charger bench evaluation are also shown.

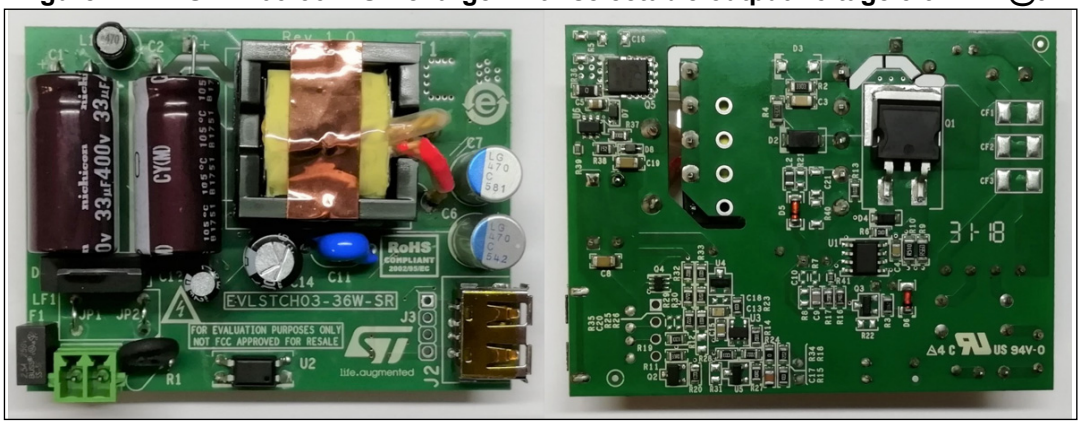
The selected charger topology is a quasi-resonant flyback converter, with secondary side synchronous rectification.

The STCH03L is a current-mode quasi-resonant (QR) controller, which combines a high-performance low-voltage PWM controller chip with a 650 V HV startup cell in the same package; it provides constant output current (CC) regulation by using primary-sensing feedback, eliminating the need of a dedicated current reference IC and of a current sensor, while still maintaining quite accurate output current regulation.

The SRK1000B controls the synchronous rectifier MOSFET at secondary side, driving its gate with minimum turn-on delay and maximizing the turn-off time instant (through an adaptive mechanism) so that the residual conduction of the SR MOSFET body diode after turn-off reduces to the target value of 300 ns.

The charger board (see *Figure 1*) has a very good high-power density per watt, providing high efficiency, very low no-load consumption (less than 20 mW), excellent EMI performances and a complete set of integrated protection features that considerably increase product safety and reliability.

Figure 1. EVLSTCH03-36W-SR charger with selectable output voltage 5-9-12 V @3A



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1 Main characteristics and circuit description

The main features of the charger shown in *Figure 1* are listed here below:

- Universal input mains range: 90 ÷ 264 Vac - frequency 47 ÷ 63 Hz
- Selectable output voltage: +5 V, +9 V, +12 V - @ 3 A continuous operation
- No-load consumption: < 20 mW at 230 Vac (with load disconnected)
- 4 points average efficiency: according to Eu CoC rev. 5 - Tier 2 (2016)
- 10% rated load efficiency: according to Eu CoC rev. 5 - Tier 2 (2016)
- Line conducted EMI: according to EN55022-Class-B
- Safety: according to EN60950
- Dimensions: 73 x 55 mm, 15 mm components max. height
- PCB: double layer, 70 µm, FR-4, mixed PTH/SMT

The charger electrical schematic is in *Figure 2*. The following sections describe the various circuit blocks.

1.1 Input stage and filtering

The input stage comprises a fuse F1 to prevent catastrophic failure and a series NTC to limit the capacitor inrush current at plug-in and protect the bridge rectifier (D1).

A low cost π-filter (C1 - L1 - C2) is implemented to filter the differential mode conducted EMI. The rectified voltage across the bulk capacitors supplies the DC-DC downstream converter.

1.2 Flyback converter

The downstream converter is a QR flyback topology with peak current mode control, based on the STCH03 IC. This PWM controller turns on and off the primary MOSFET Q1 in order to control (through the feedback loop) the peak current flowing through the primary winding of the flyback transformer T1 (and hence the energy stored inside its primary inductance during the ON time) allowing to get the required output regulation against input voltage and load variations. After the primary MOSFET turn-off, the stored energy is electromagnetically transferred to the secondary side capacitors and load.

The primary current (sensed across the resistors R9-R10 in series to the MOSFET) is internally compared to the feedback signal: when the current peak reaches the value programmed by the feedback loop, the primary MOSFET turns off.

For proper QR operation, the primary controller is provided with a zero-crossing sense pin (ZCD pin) to detect the transformer demagnetization and then turn on the primary MOSFET on the valley of the voltage ringing present at the primary MOSFET drain (thus minimizing the capacitive losses at turn-on). To sense the transformer demagnetization, the ZCD pin is connected through a resistive divider (R13 - R16//R17) to an auxiliary winding of the flyback transformer. In order to avoid the operating frequency increasing too much at reduced loads, the STCH03 uses a valley-skipping technique after demagnetization detection to turn on the primary MOSFET.

The CV regulation is achieved by secondary side feedback, transferring the output voltage information via an optocoupler (U2) and adjusting the voltage on the FB pin of the STCH03 to get the selected output voltage. The capacitor C9 on the FB pin and the internal equivalent resistance of the pin provide a high frequency pole, while the loop compensation is done at secondary side around the CV regulator U4.

The CC regulation loop is fully integrated into the IC and no external components are required, except the resistors connected to the sense pins (R7 and R8), used to adjust the CC set point at 3.25 A and the feed-forward resistor R13, to keep it constant in the input voltage range.

For deep understanding of STCH03 operation and its use, please refer to the datasheet [*1*].

The STCH03 combines the low-voltage PWM controller chip with an embedded HV start-up circuit with zero power consumption that, together with the extremely low quiescent current of the device, helps minimize the residual input consumption.

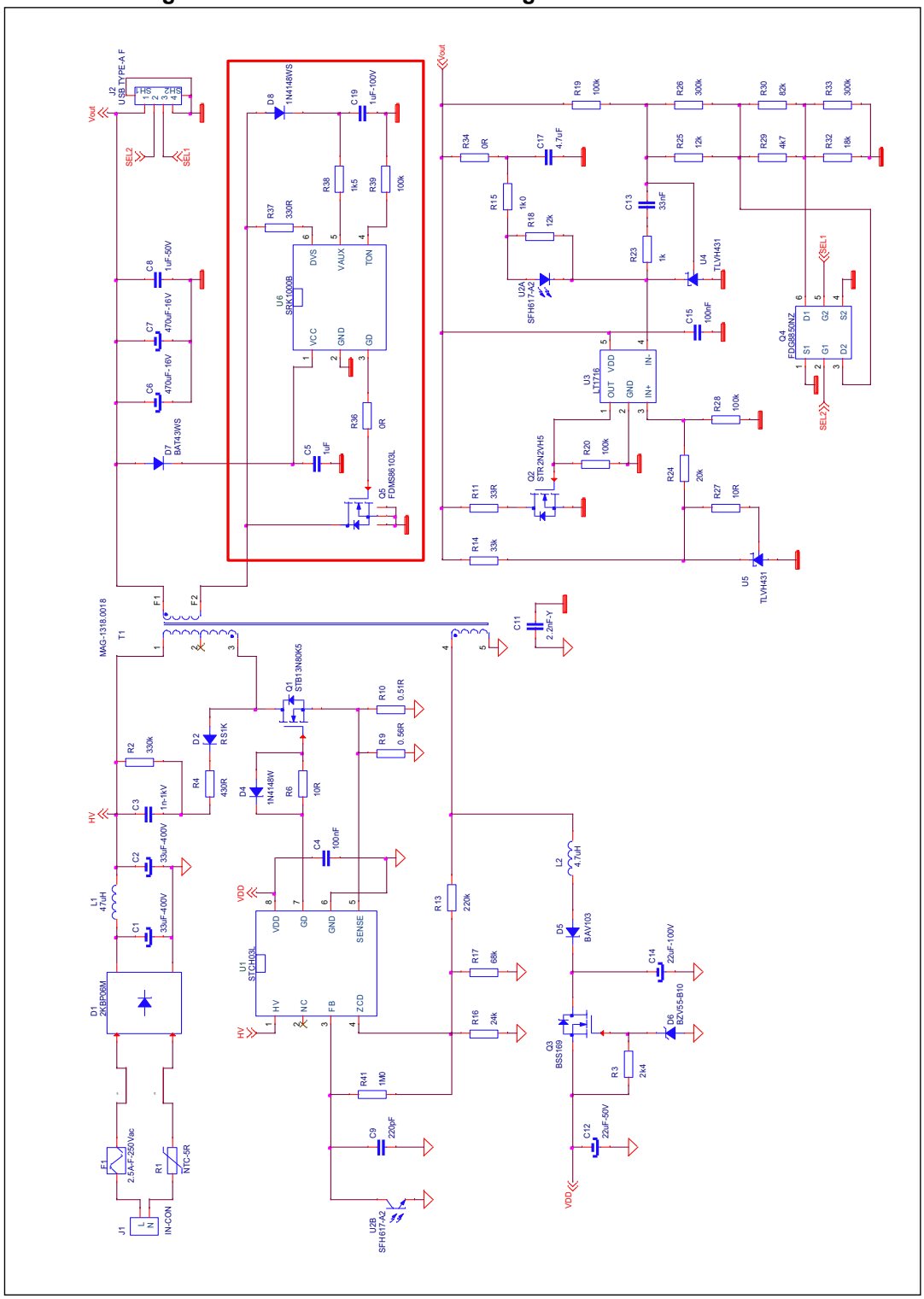
The power MOSFET Q1 is a D^2PAK, N-channel, 800 V BVdss, MDmesh™ K5 technology device, with $R_{DS(on)}$ = 0.37 Ω (typ.), which ensures a good compromise between low conduction losses and switching characteristics.

The flyback transformer uses 2xEFD25 ferrite cores and presents a primary inductance of 700 µH (refer to its specification in the *APPENDIX*).

1.3 R2CD clamp circuit

The clamping network (R2 - C3 - D2) limits the leakage inductance voltage spike peak, by dissipating the related energy at MOSFET turn-off, ensuring reliable power supply operation. The resistor R4 helps to reduce the residual ringing present across the primary MOSFET drain after the clamp action: R4 and C2 behave like a snubber circuit and damp the resonance oscillations arising due to the leakage inductance and the total equivalent capacitance across the primary MOSFET. For this reason, the clamp diode D3 needs to be still in low impedance at the end of the clamp action; therefore it has to be selected with a recovery time in the order of 500-800 ns.

Figure 2. EVLSTCH03-36W-SR charger electrical schematic.



1.4 Output stage

During the demagnetization period, the energy stored in the transformer primary inductance is transferred to the secondary side: the current flows through SR MOSFET Q5 to the output capacitors C6 - C7 and to the load, until the transformer is completely demagnetized. The output capacitors C6 and C7 are low ESR type to keep ripple voltage low according to charger requirements. The capacitor C8 is used to reduce further the output switching noise.

The SRK1000B controller is of course set for QR operation (no capacitor is present on TON pin): as soon as it senses that the current starts flowing through the SR MOSFET body diode, it turns on its gate with minimum delay. Then, the SR controller turns off the SR MOSFET with an adaptive mechanism such that the residual conduction of its body diode after turn-off matches the target value of 300 ns. The adaptive turn-off mechanism automatically compensates for the anticipation effect of any stray inductance in the current path and hence allows maximizing system efficiency.

In order to allow SR operation also during CC regulation, where the output voltage (that supplies also the SRK1000B through the decoupling diode D7) may sensibly decrease, the VAUX pin functionality is used. The circuit composed by D8, C19 and R38 rectifies the SR MOSFET drain-source voltage and provides a voltage to the VAUX pin that can charge the capacitor C5 (on the VCC pin) through an internal switch, when the output voltage is too low.

For deep understanding of SRK1000B operation, please refer to its datasheet [*2*] and to the application note AN5066 [*3*].

The SR MOSFET Q5 is a PowerFLAT package, N channel, 100 V BVdss, logic-level device, with $R_{DS(on)}$ = 11 mΩ (typ.) @ VGS = 4.5 V.

1.5 Auxiliary voltage

At power-up, the VDD pin capacitor (C12) for the STCH03 IC supply charges through the internal HV start-up circuit. Once the VDD UVLO voltage is surpassed, the controller starts the switching operation and the transformer auxiliary winding provides energy to the capacitor C14 through the diode D5 (and hence to the capacitor C12) so that in steady state the VDD supply to the controller is sustained by the auxiliary voltage. The inductor L2 in series to the auxiliary diode D5 filters the voltage spikes on the auxiliary winding (due to the leakage inductance), limiting the auxiliary voltage dependence on output power and input voltage.

The auxiliary voltage (across C14 capacitor) depends on the selected output voltage through the transformer turn ratio: it has to be large enough to provide VDD supply to the STCH03 controller at the lowest output voltage (+5 V output). Of course, at the highest selected output voltage (+12 V output), the auxiliary voltage is much larger. Therefore, a series regulator is necessary to limit the voltage provided on the STCH03 VDD pin. This regulator is implemented by discrete components Q3 (small signal N-channel 100 V depletion MOSFET), D6 and R3.

The transformer auxiliary winding is also used, through the resistive divider R13 - R16//R17, to properly bias the ZCD pin of STCH03, for transformer demagnetization sensing, for voltage feed-forward compensation and for overvoltage and undervoltage protections (OVP and UVP).

1.6 Output voltage selection interface

The resistive divider net composed by R19, R25, R26, R29, R30, R32, R33 senses the output voltage and provides the signal to the CV regulator U4 that, in turn, fixes the feedback current through the optocoupler diode and, through its CTR, transfers at primary side the proper feedback level on the STCH03 FB pin for regulation of the output voltage.

The output voltage selection is done through the signals SEL1 and SEL2 at the input of the USB connector. These two signals configure the low side part of the resistive divider net through the MOSFET switches inside Q4, to obtain the output voltage according to the following scheme:

SEL1 = "low" SEL2 = "low" ➔ VOUT = +5 V

SEL1 = "low" SEL2 = "high" ➔ VOUT = +9 V

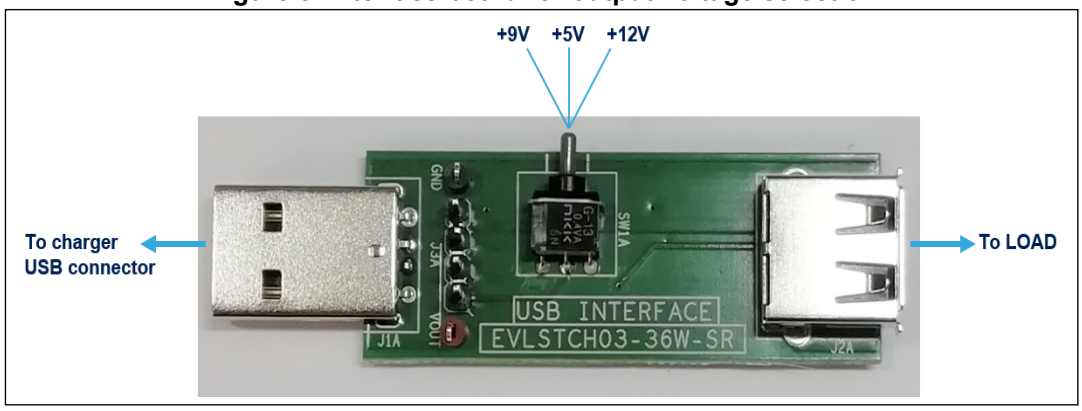
SEL1 = "high" SEL2 = "low" or "high" ➔ VOUT = +12 V

where the "low" level is 0 V and the "high" level is V_{OUT}.

During any transition of the output voltage from higher to lower level selection (whichever is the load level) or when the output cable is detached from the USB connector J2 (and the output voltage becomes +5 V), the output voltage capacitors need to be quickly discharged to the new required voltage level. This is accomplished through resistor R11 by turning on the MOSFET Q2 through the output of the comparator U3. In fact, during the voltage selection transition high to low, the feedback signal quickly goes low; the comparator U3 senses this drop (compared to the reference generate by U5) and turns on Q2 for the discharge.

In order to easily select the output voltage level, the charger demonstration board is provided together with a small interface board that allows changing the voltage between +5 V, +9 V and +12 V levels through a three-position switch, like shown in *Figure 3*. This allows the user to perform all the electrical tests on the board for each output voltages selection, in the various operating conditions, once the interface is plugged into the charger USB output connector from one side and connected to the load from the other side.

Figure 3. Interface board for output voltage selection



2 Electrical measurements

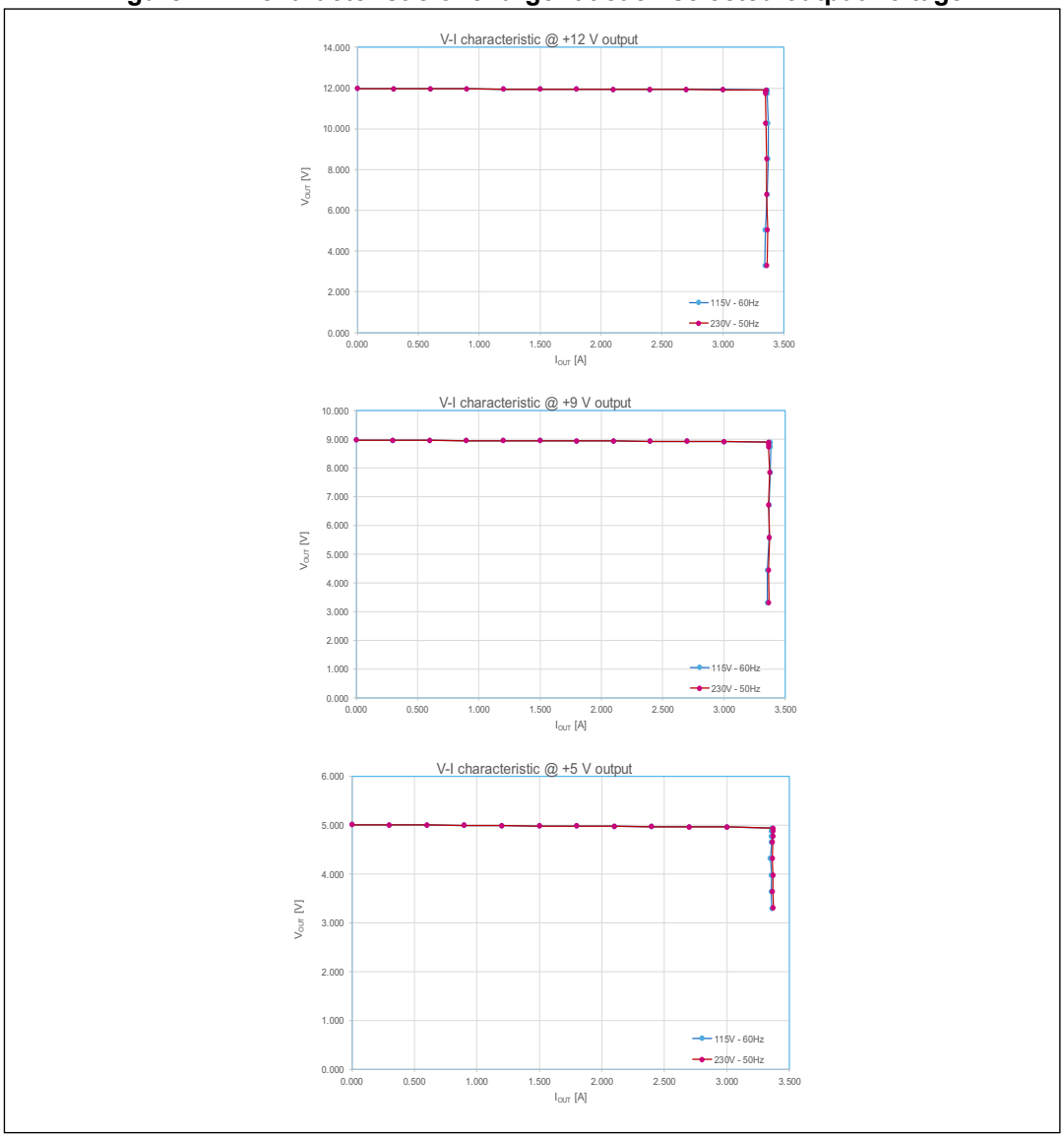
This section shows the measurements of the charger electrical characteristics.

The measurements are performed after a warm-up of 20 minutes.

2.1 Output CV-CC regulation

The CV-CC regulation is measured at both nominal input voltages (115 Vac and 230 Vac) and the V-I characteristic is plotted for each output voltage (+12 V, +9V, +5V) in the graphs shown in *Figure 4*. The results show excellent CV regulation, better than 2% and also very good CC regulation, better than 5%.

Figure 4. V-I characteristic of charger at each selected output voltage



2.2 Efficiency measurements

The charger efficiency is measured in the various operating conditions and the measurements show that the charger is compliant to Eu CoC rev. 5 - Tier 2 (2016), since the 4 points average efficiency (at 25%-50%-75%-100% of rated load) and efficiency at 10% of rated load are always higher than the minimum requirements shown in *Table 1*.

Table 1. EU CoC rev. 5 - Tier 2 (2016) efficiency requirements

	12Vout 3A	9Vout 3A	5Vout 3A
4 point avg eff. %	88.30%	87.30%	81.84%
10% of load eff. %	78.30%	77.30%	72.48%

The efficiency data are shown in *Table 2* here below. These data are also plotted and shown in *Figure 5*, *Figure 6*, and *Figure 7*

Table 2. Efficiency measurements summary

Percent of rated load	Efficiency %					
	12 V output		9 V output		5 V output	
	115 Vac 60 Hz	230 Vac 50 Hz	115 Vac 60 Hz	230 Vac 50 Hz	115 Vac 60 Hz	230 Vac 50 Hz
10%	**85.03%**	**82.02%**	**84.51%**	**80.29%**	**82.42%**	**76.73%**
25% 50% 75% 100%	88.73% 89.99% 90.37% 90.24%	87.58% 89.66% 90.39% 90.68%	88.58% 89.77% 90.06% 89.91%	86.67% 88.98% 89.71% 90.01%	87.26% 88.55% 88.70% 88.43%	83.66% 86.66% 87.57% 87.88%
avg eff. %	**89.83%**	**89.58%**	**89.58%**	**88.84%**	**88.24%**	**86.44%**

Figure 5. Efficiency plot for +12 V output

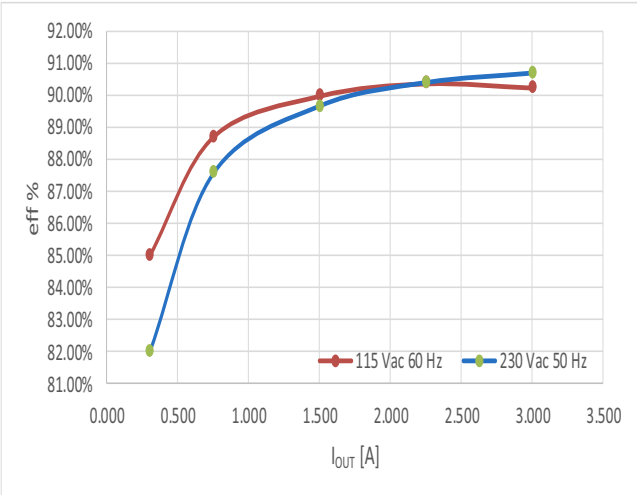


Figure 6. Efficiency plot for +9 V output

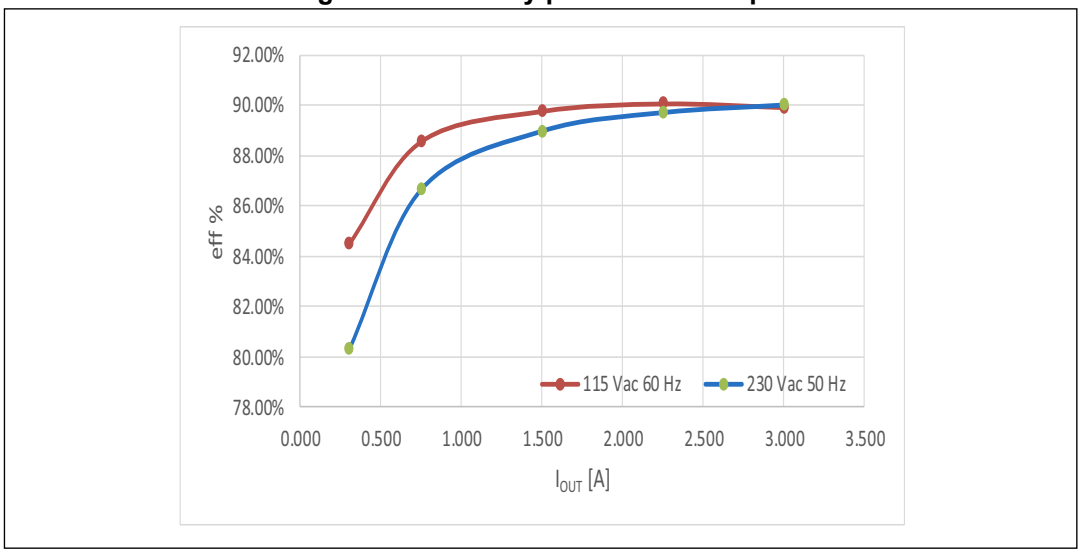
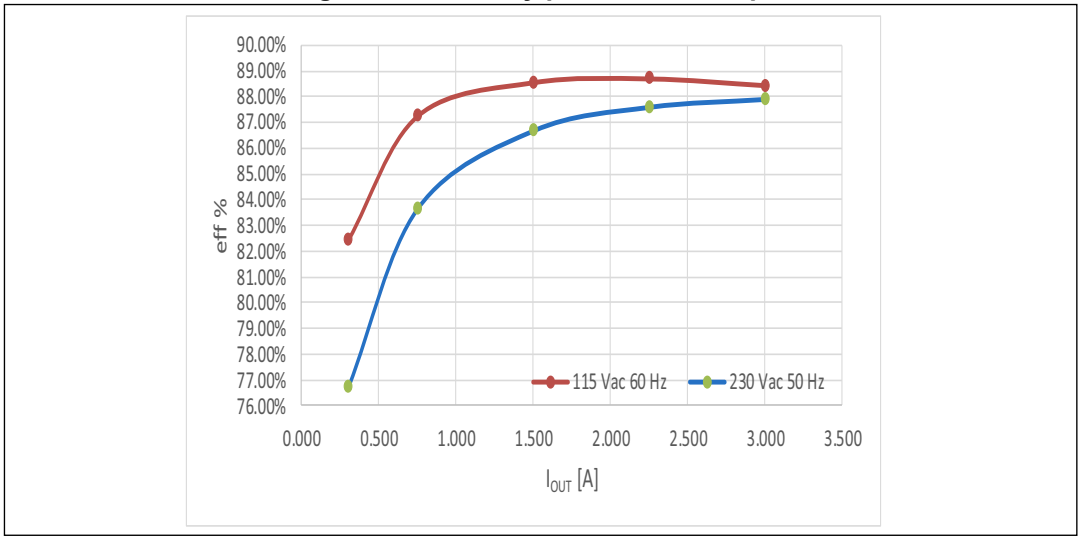


Figure 7. Efficiency plot for +5 V output



2.3 No-load consumption

The no-load consumption is measured at nominal input voltage (115 Vac and 230 Vac) with the USB interface board for output voltage selection disconnected from the charger. In this way, the output voltage automatically sets at +5 V. The measurements in *Table 3* below show a max. consumption at nominal 230 Vac lower than 20 mW.

Table 3. No-load consumption measurements

Input voltage	No-load consumption [mW]
115 Vac - 60 Hz	16.0
230 Vac - 50 Hz	16.7

3 Functional check

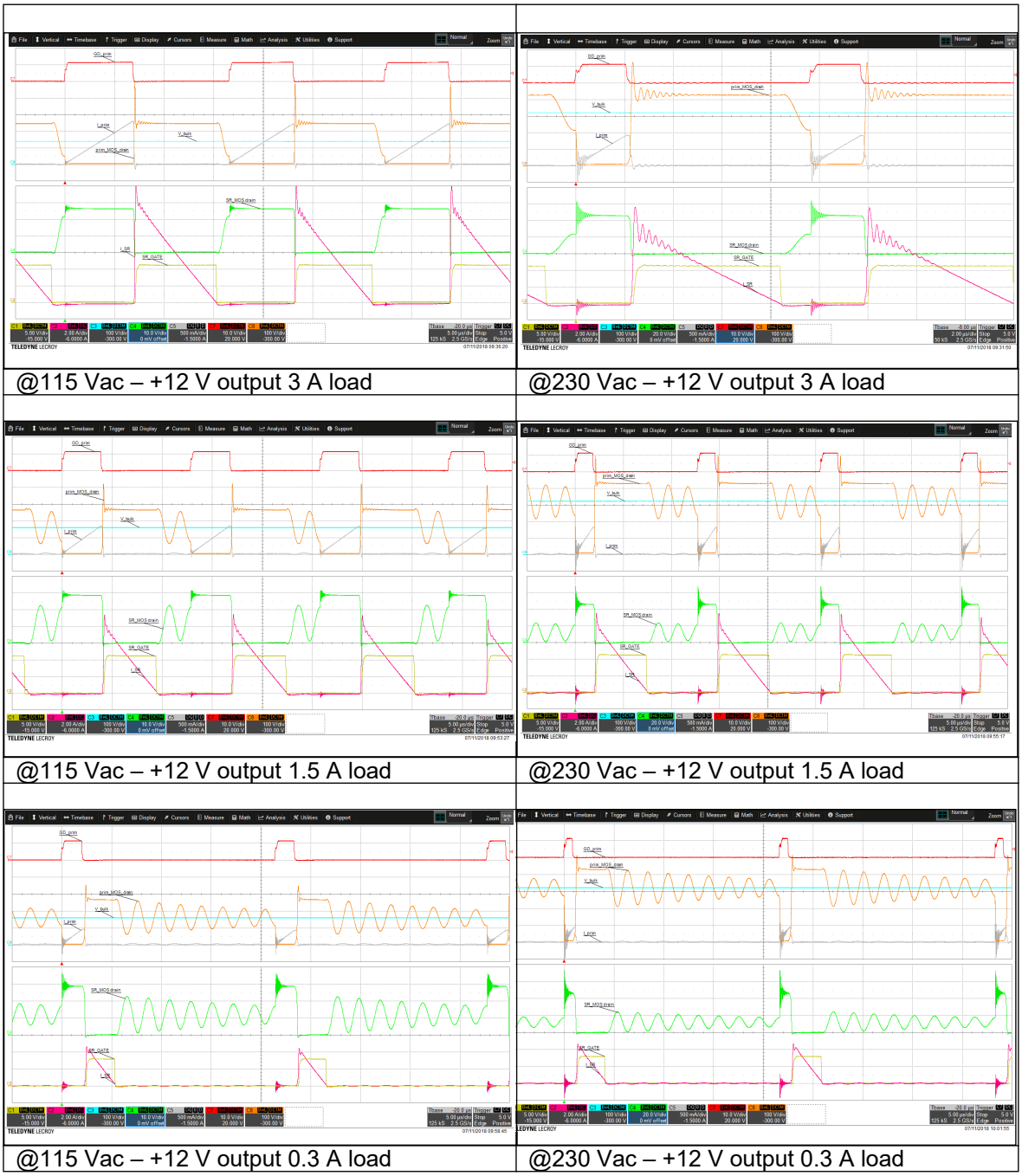
This section provides converter operation waveforms: typical current and voltage signals are shown of both primary power MOSFET and SR MOSFET, in various line and load conditions.

The behavior during startup, burst-mode and the dynamic load response are also provided. The final part of the section verifies the converter protections (OVP, UVP and short-circuit).

3.1 Typical waveforms (CV-CC regulation)

Typical waveforms of operation in CV regulation are provided in *Figure* and *Figure 9*.

Figure 8. CV regulation typical operation at +12 V output



@115 Vac – +12 V output 3 A load

@230 Vac – +12 V output 3 A load

@115 Vac – +12 V output 1.5 A load

@230 Vac – +12 V output 1.5 A load

@115 Vac – +12 V output 0.3 A load

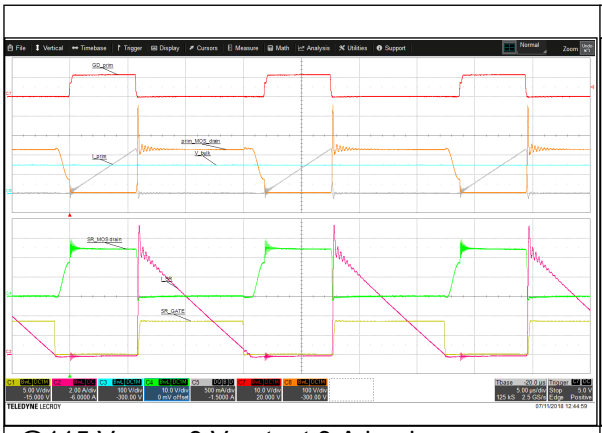
@230 Vac – +12 V output 0.3 A load

The pictures, at nominal input voltages (115 Vac and 230 Vac), show the QR operation at primary side with turn-on on the valley of MOSFET drain voltage and valley skipping at reduced load levels. At secondary side, the images show the turn-off mechanism of the SR MOSFET is correctly adapted in steady state condition, allowing to maximize the converter efficiency.

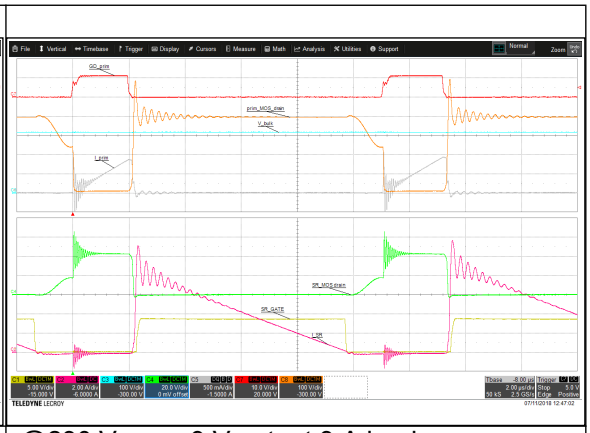
Typical waveforms of operation in CC regulation are provided in *Figure 10*. In order to simulate this operation mode, the electronic load has been set in constant voltage (at 3.5 V, 5 V and 7 V, lower than the respective CV regulation setpoint +5 V, +9 V +12 V) in order to

impose this level at charger output, forcing the primary side control to regulate the output current at the nominal value.

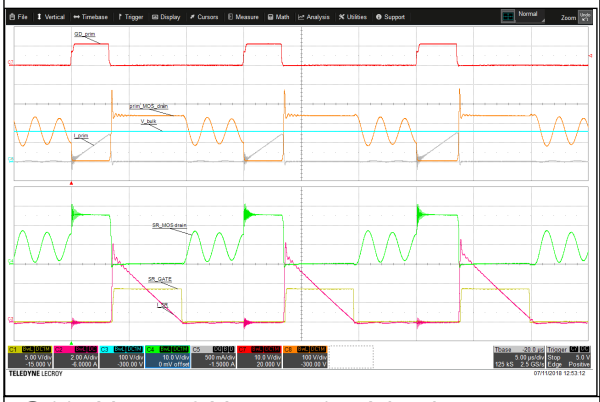
Figure 9. CV regulation typical operation at +9 V and +5 V output



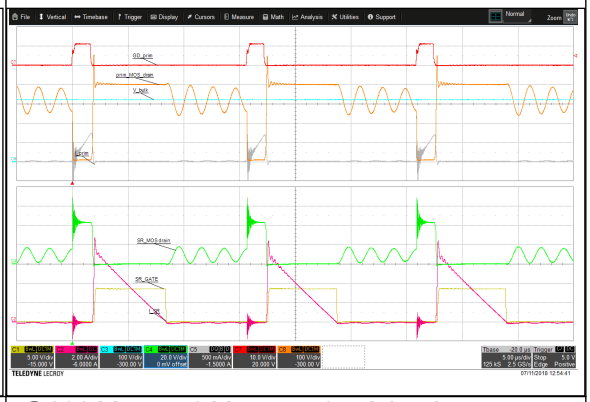
@115 Vac – +9 V output 3 A load



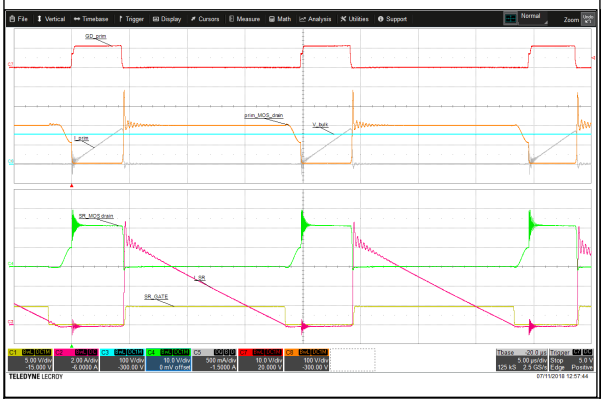
@230 Vac – +9 V output 3 A load



@115 Vac – +9 V output 1.5 A load



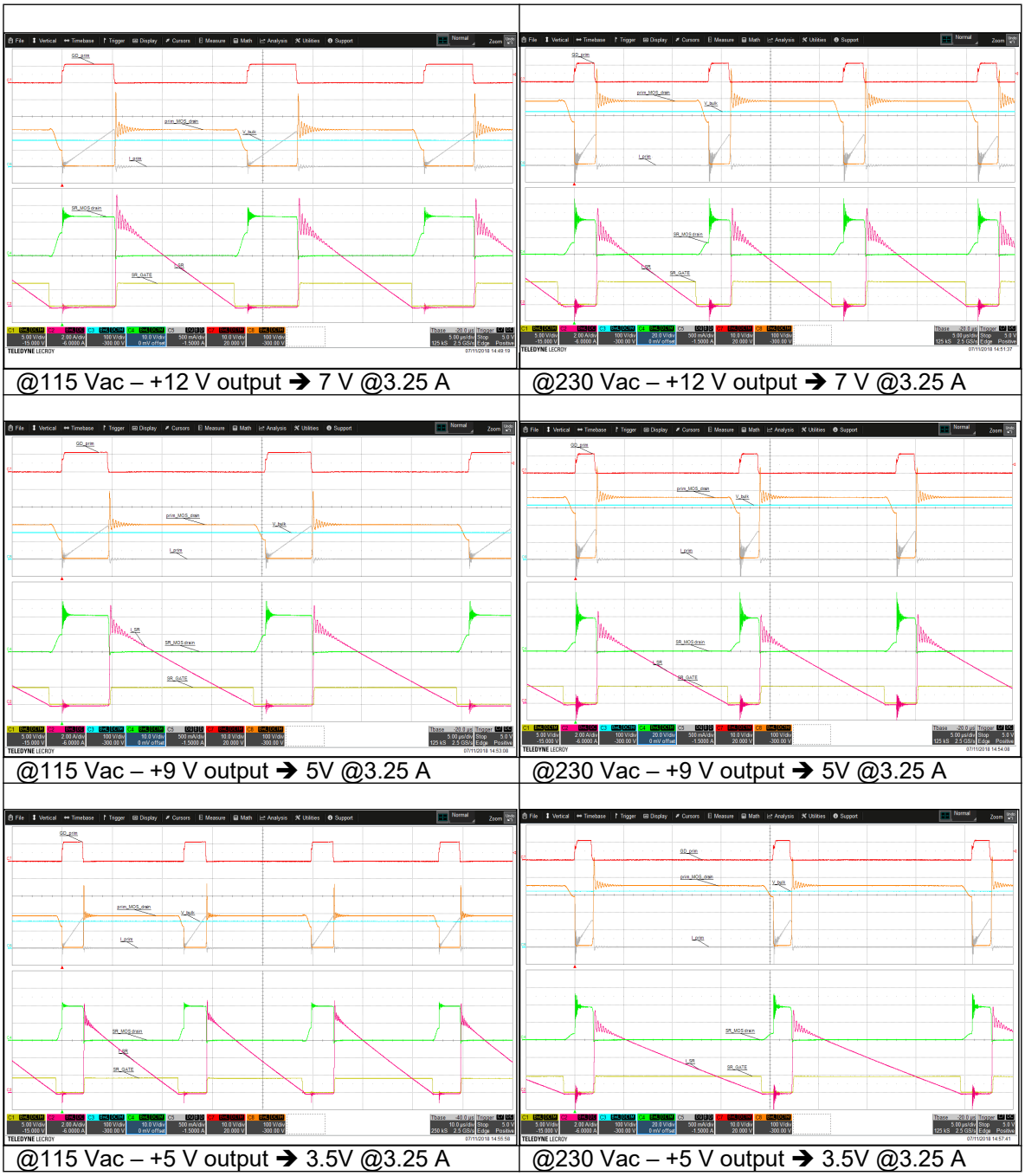
@230 Vac – +9 V output 1.5 A load



@115 Vac – +5 V output 3 A load

@230 Vac – +5 V output 3 A load

Figure 10. CC regulation typical operation



@115 Vac – +12 V output ➔ 7 V @3.25 A

@230 Vac – +12 V output ➔ 7 V @3.25 A

@115 Vac – +9 V output ➔ 5V @3.25 A

@230 Vac – +9 V output ➔ 5V @3.25 A

@115 Vac – +5 V output ➔ 3.5V @3.25 A

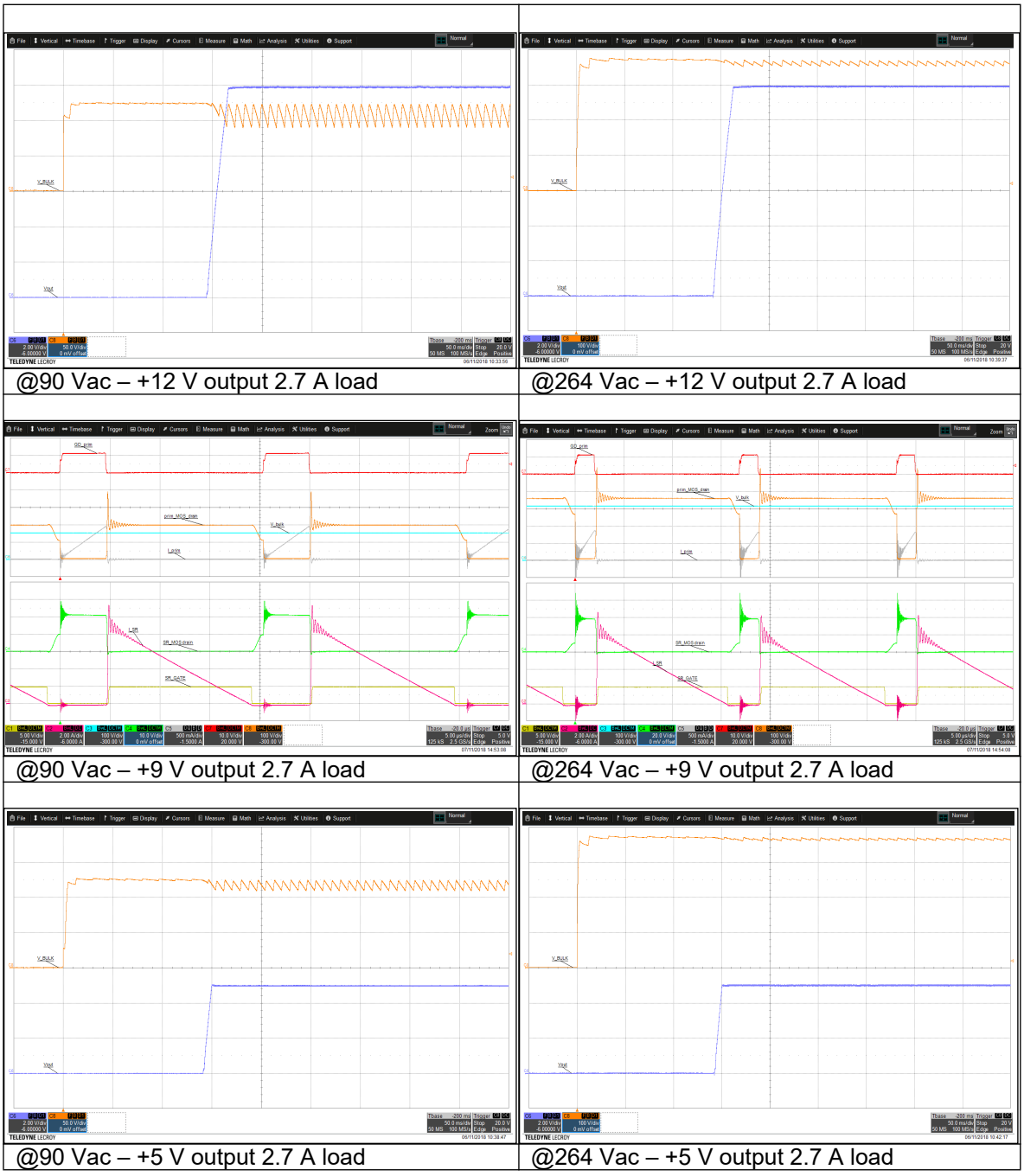
@230 Vac – +5 V output ➔ 3.5V @3.25 A

3.2 Converter startup

The output voltage starts increasing after a very short delay from input voltage turn-on, <150 ms from bulk capacitor voltage rising edge, and its rise time is lower than 30 ms as shown in *Figure 11*. The output voltage build-up is always monotone.

At input voltage turn-on, as soon as the supply voltage of the STCH03 (derived through the internal high-voltage start-up circuit) surpasses the UVLO threshold, the converter starts switching with soft-start, as shown in *Figure 12*: the images show a clean and safe ramp-up of the primary MOSFET current and its gate driving.

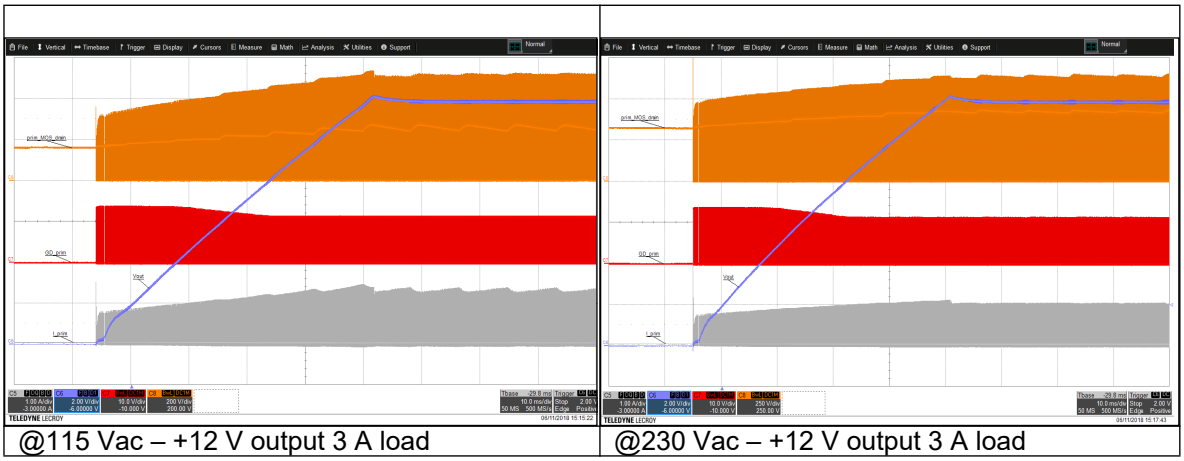
Figure 11. Output voltage start-up delay and rise time



Also at secondary side, the SR MOSFET driving at startup is clean and regular, without current inversions. Referring to the pictures in *Figure 13*, the SR MOSFET driving starts when the output voltage is still very low: this is because the supply voltage capacitor on pin

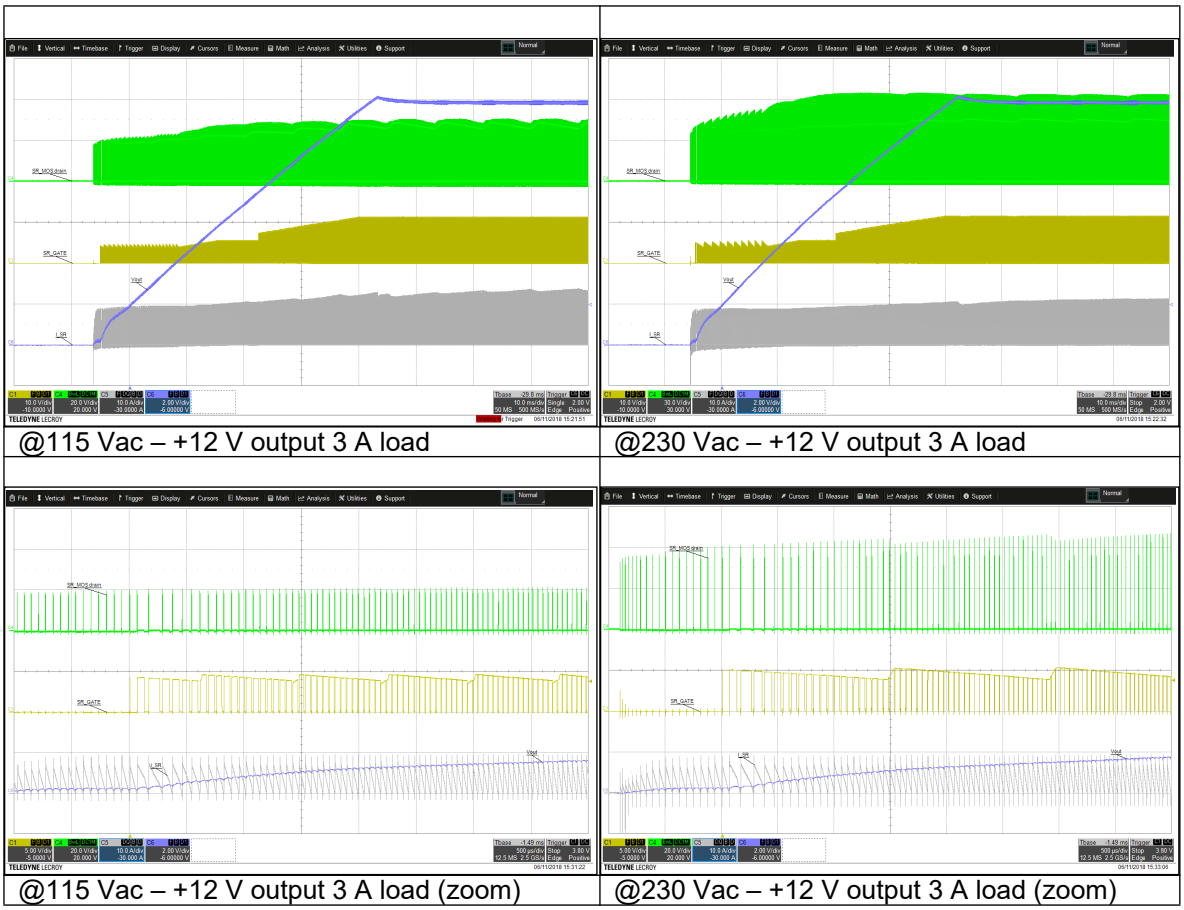
VCC of the SRK1000B is charged through the VAUX pin voltage connected to the rectified drain voltage of the SR MOSFET. The zoomed waveforms of *Figure 13* show that during the initial phase of the SR gate drive adapting, the current flowing through the SR MOSFET never inverts.

Figure 12. Primary side waveforms during startup (+12V output set)



@115 Vac – +12 V output 3 A load | @230 Vac – +12 V output 3 A load

Figure 13. Secondary side waveforms during startup (+12V output set)



@115 Vac – +12 V output 3 A load | @230 Vac – +12 V output 3 A load

@115 Vac – +12 V output 3 A load (zoom) | @230 Vac – +12 V output 3 A load (zoom)

3.3 Burst-mode operation

At reduced load, the converter enters burst-mode operation. *Table 4* below indicates the output load levels where the primary controller enters/exits burst-mode operation at the various input voltages from 90 Vac to 264 Vac for each output voltage setting (+5 V, +9 V, +12 V).

Table 4. Output load levels for burst-mode enter/exit

Burst-mode		90 Vac - 60 Hz		115 Vac - 60 Hz		230 Vac - 50 Hz		264 Vac - 50 Hz	
		enter	exit	enter	exit	enter	exit	enter	exit
+12V	Iout [mA]	73	75	79	81	103	105	127	129
	Vout [V]	11.870	11.870	11.870	11.870	11.869	11.869	11.869	11.869
	Pin [W]	1.236	1.254	1.327	1.345	1.815	1.835	2.203	2.223
+9V	Iout [mA]	103	105	112	115	148	150	181	183
	Vout [V]	8.920	8.920	8.920	8.920	8.919	8.919	8.919	8.919
	Pin [W]	1.227	1.243	1.331	1.363	1.874	1.891	2.278	2.294
+5V	Iout [mA]	199	201	220	222	272	274	328	330
	Vout [V]	4.971	4.971	4.971	4.971	4.970	4.970	4.969	4.969
	Pin [W]	1.242	1.251	1.381	1.391	1.863	1.870	2.249	2.252

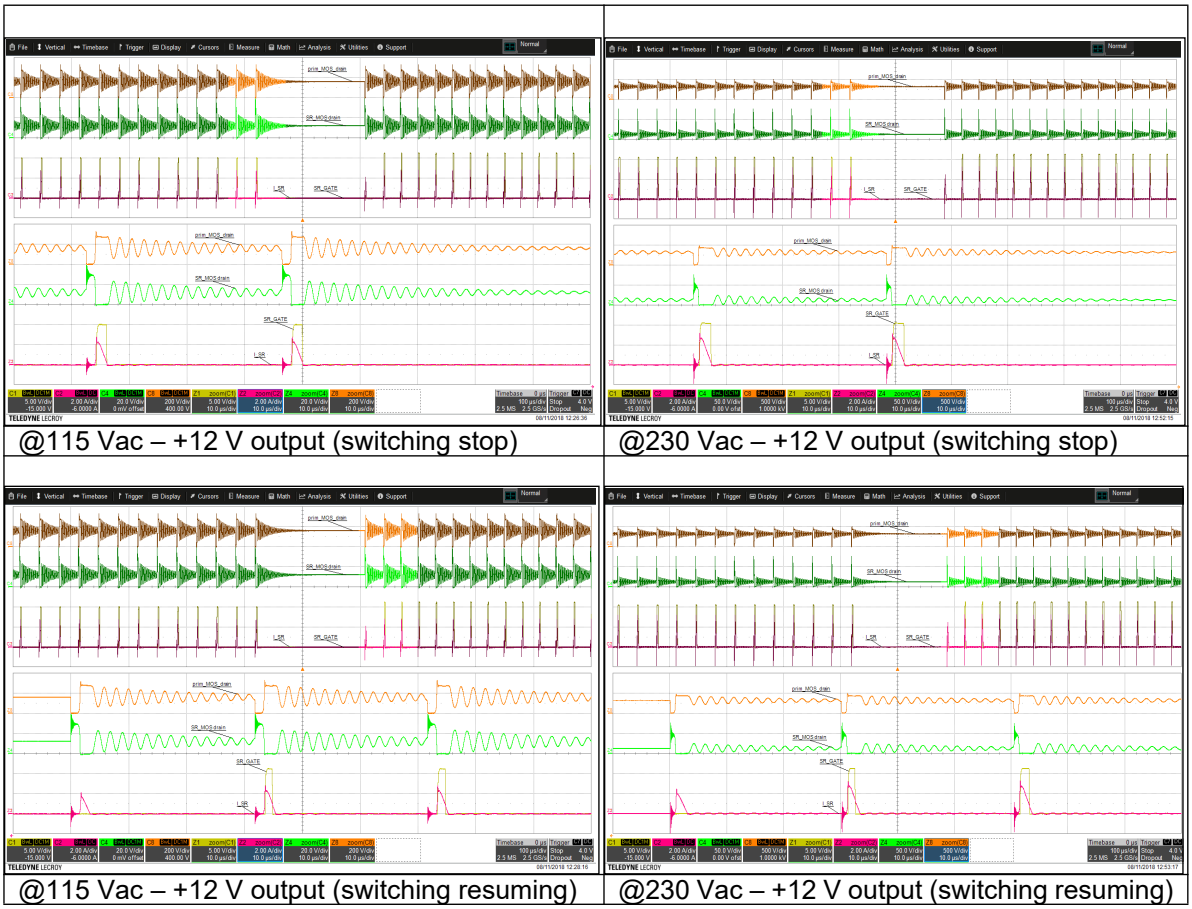
The images in *Figure 14* show the typical waveforms at burst-mode operation entering with output voltage set at +12 V: as the primary controller stops operation, the SR controller recognizes the switching stop and enters low-consumption. Then, at primary controller switching resuming, the SR driving also resumes, after a first skipped cycle (as per internal logic): the image shows that the turn-off rapidly adapts to maximize the rectifier conduction.

The burst-mode operation in no-load condition for +12 V setting is shown in *Figure 15*: the images show that, during the burst train, the SRK1000B is not driving. This is due to the fact that in this case the demagnetization time duration is shorter than the sleep-mode entering time programmed by the resistor on the TON pin and therefore the SR controller enters automatic sleep-mode.

The typical waveforms at burst-mode entering load level are also provided in the case of output voltage set at +9 V and at +5 V, respectively in *Figure 16* and *Figure 18*.

The typical burst-mode operation in no-load with the output voltage set at +9 V and at +5 V are shown in *Figure 17* and *Figure 19*, respectively. Differently from the case of +12 V output setting, at +9 V and at +5 V output voltage the SR controller does not enter sleep-mode in no-load, since the demagnetization time in these conditions is detected larger than the programmed sleep-mode entering time.

Figure 14. Typical operation at burst-mode entering load level for +12 V output



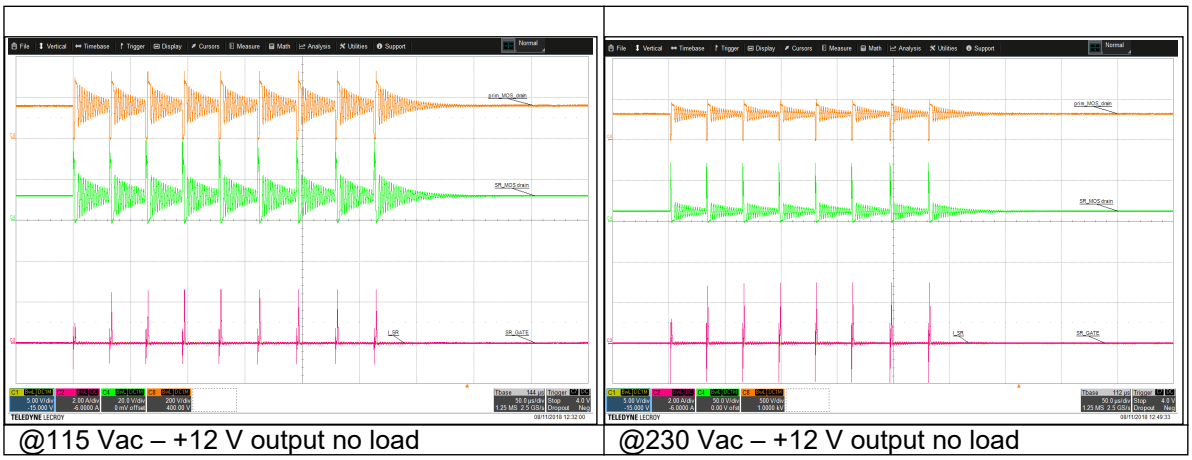
@115 Vac – +12 V output (switching stop)

@230 Vac – +12 V output (switching stop)

@115 Vac – +12 V output (switching resuming)

@230 Vac – +12 V output (switching resuming)

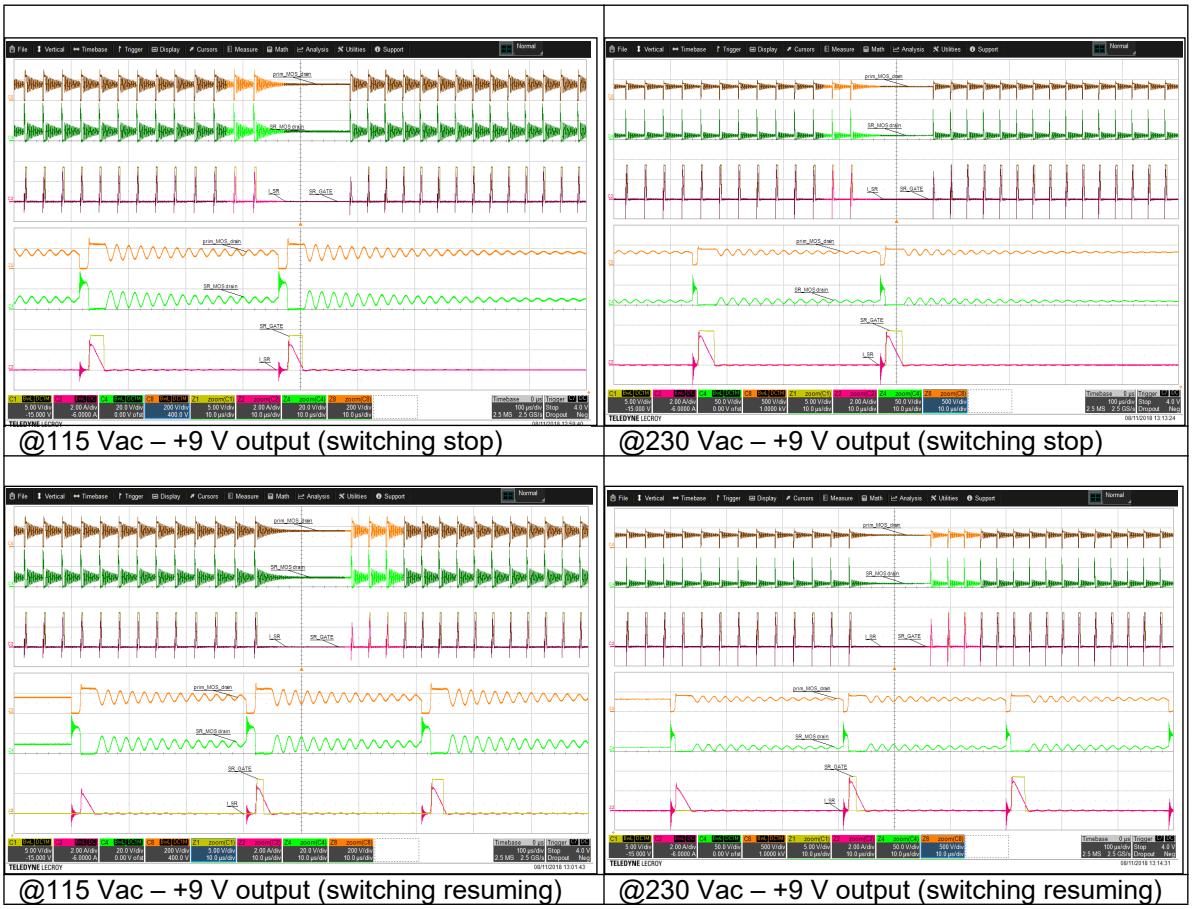
Figure 15. Typical burst-mode operation in no-load for +12 V output



@115 Vac – +12 V output no load

@230 Vac – +12 V output no load

Figure 16. Typical operation at burst-mode entering load level for +9 V output



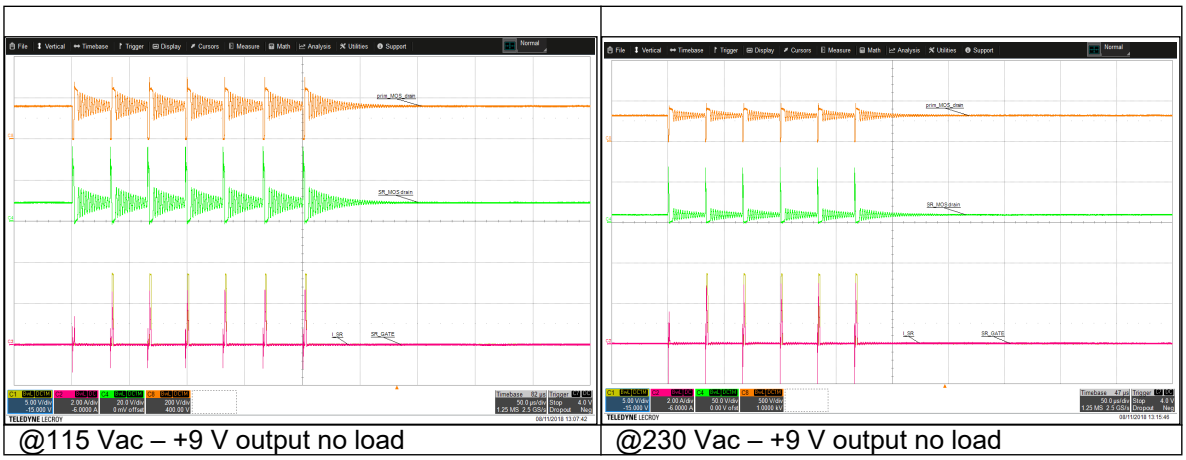
@115 Vac – +9 V output (switching stop)

@230 Vac – +9 V output (switching stop)

@115 Vac – +9 V output (switching resuming)

@230 Vac – +9 V output (switching resuming)

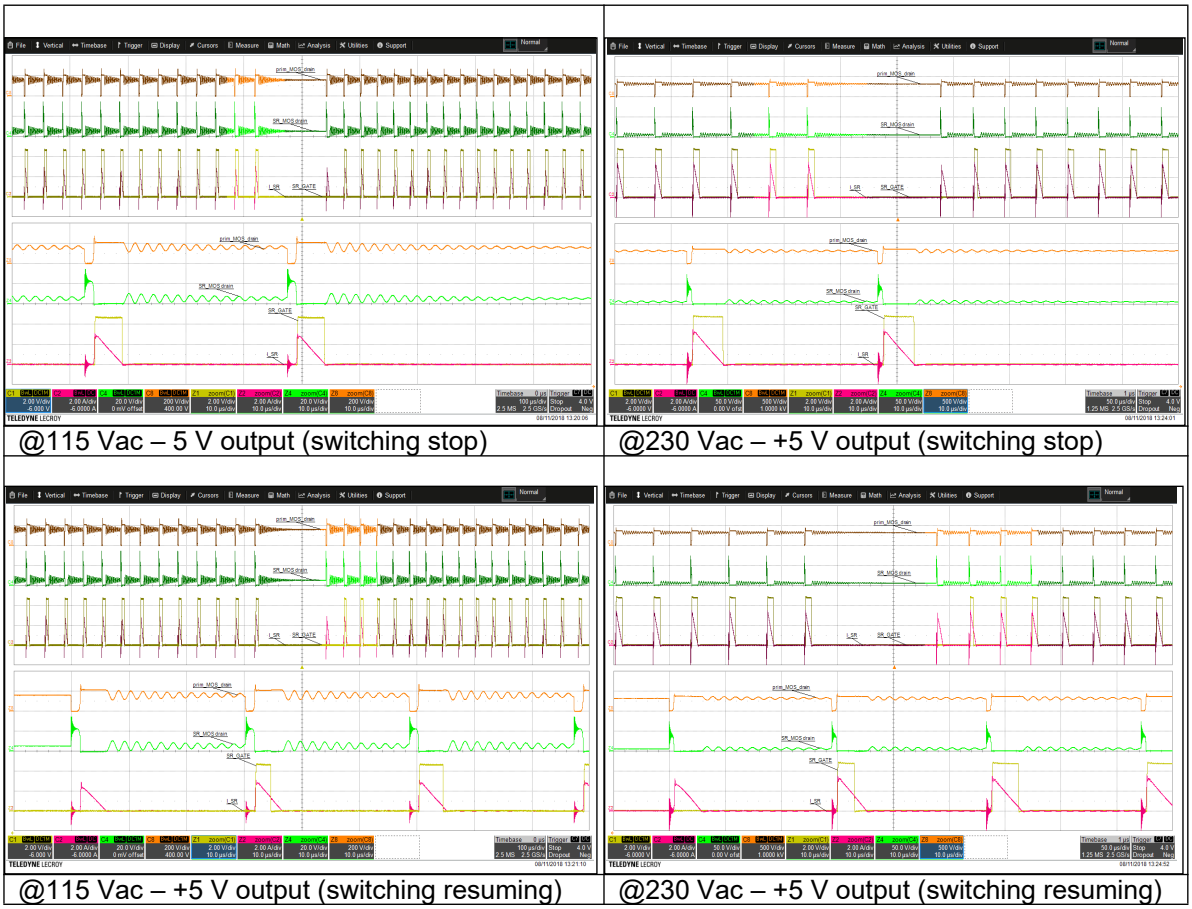
Figure 17. Typical burst-mode operation in no-load for +9 V output



@115 Vac – +9 V output no load

@230 Vac – +9 V output no load

Figure 18. Typical operation at burst-mode entering load level for +5 V output



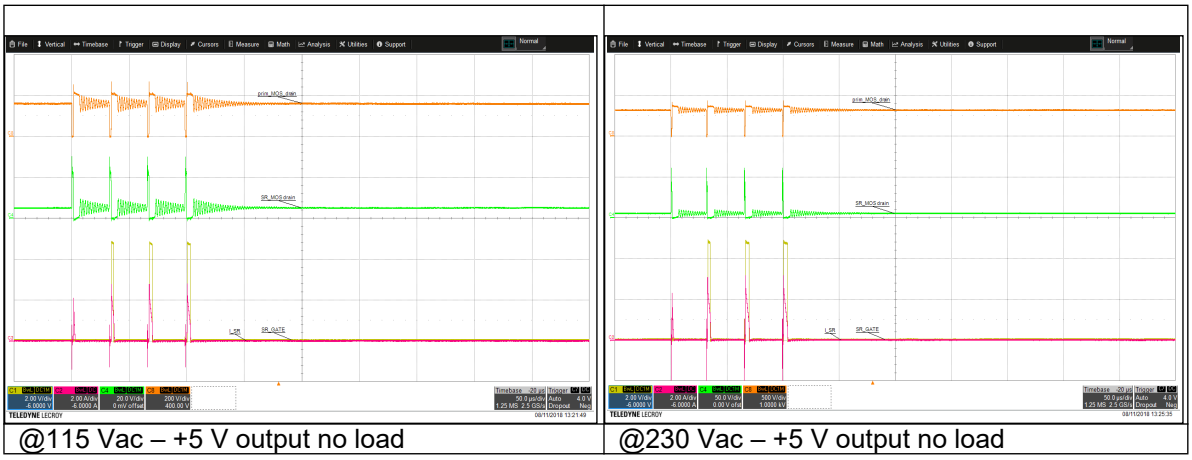
@115 Vac – 5 V output (switching stop)

@230 Vac – +5 V output (switching stop)

@115 Vac – +5 V output (switching resuming)

@230 Vac – +5 V output (switching resuming)

Figure 19. Typical burst-mode operation in no-load for +5 V output



@115 Vac – +5 V output no load

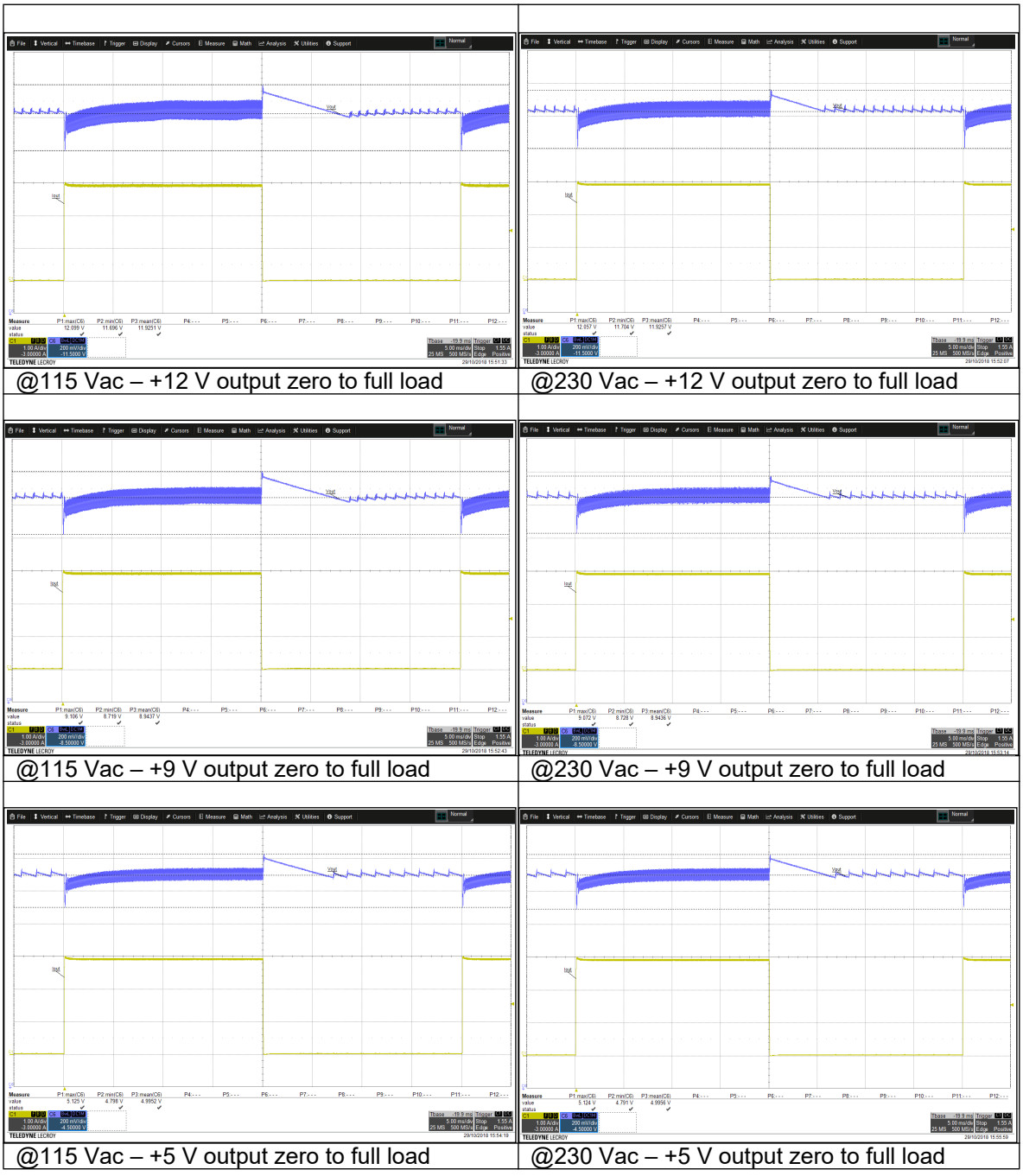
@230 Vac – +5 V output no load

3.4 Dynamic load transients

The charger has been subjected to repetitive dynamic load transitions zero to full load, with repetition rate 20 ms - 20 ms and 2.5 A/µs slew rate. The waveforms in *Figure 20* do not

show any abnormal oscillation on the output and present very limited overshoot and undershoot values (below ±5% of output voltage level).

Figure 20. Repetitive dynamic load transient zero to full load



@115 Vac – +12 V output zero to full load

@230 Vac – +12 V output zero to full load

@115 Vac – +9 V output zero to full load

@230 Vac – +9 V output zero to full load

@115 Vac – +5 V output zero to full load

@230 Vac – +5 V output zero to full load

3.5 Output ripple voltage

The output ripple measurements have been done with the voltage probe connected to the charger output connector, across a 1 µF bypass capacitor and with the oscilloscope

bandwidth set at 20 MHz. The waveforms are collected in *Figure 21*, *Figure 22* and *Figure 23* and the measurements show that the total output ripple voltage is:

< 150 mV @ +12 V output

< 120 mV @ +9 V output

< 100 mV @ +5 V output

Figure 21. Output peak-to-peak rippple voltage @ +12V

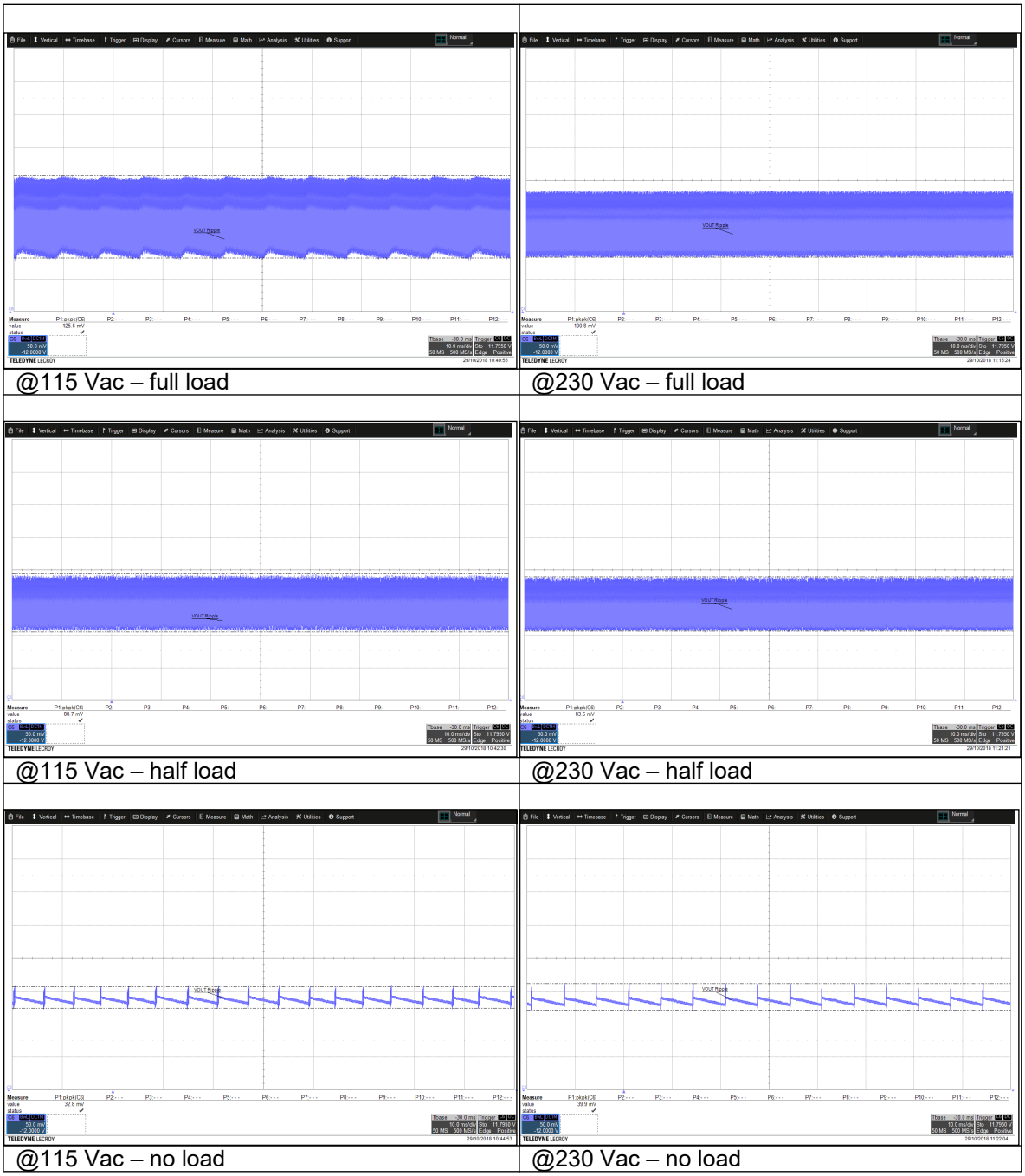
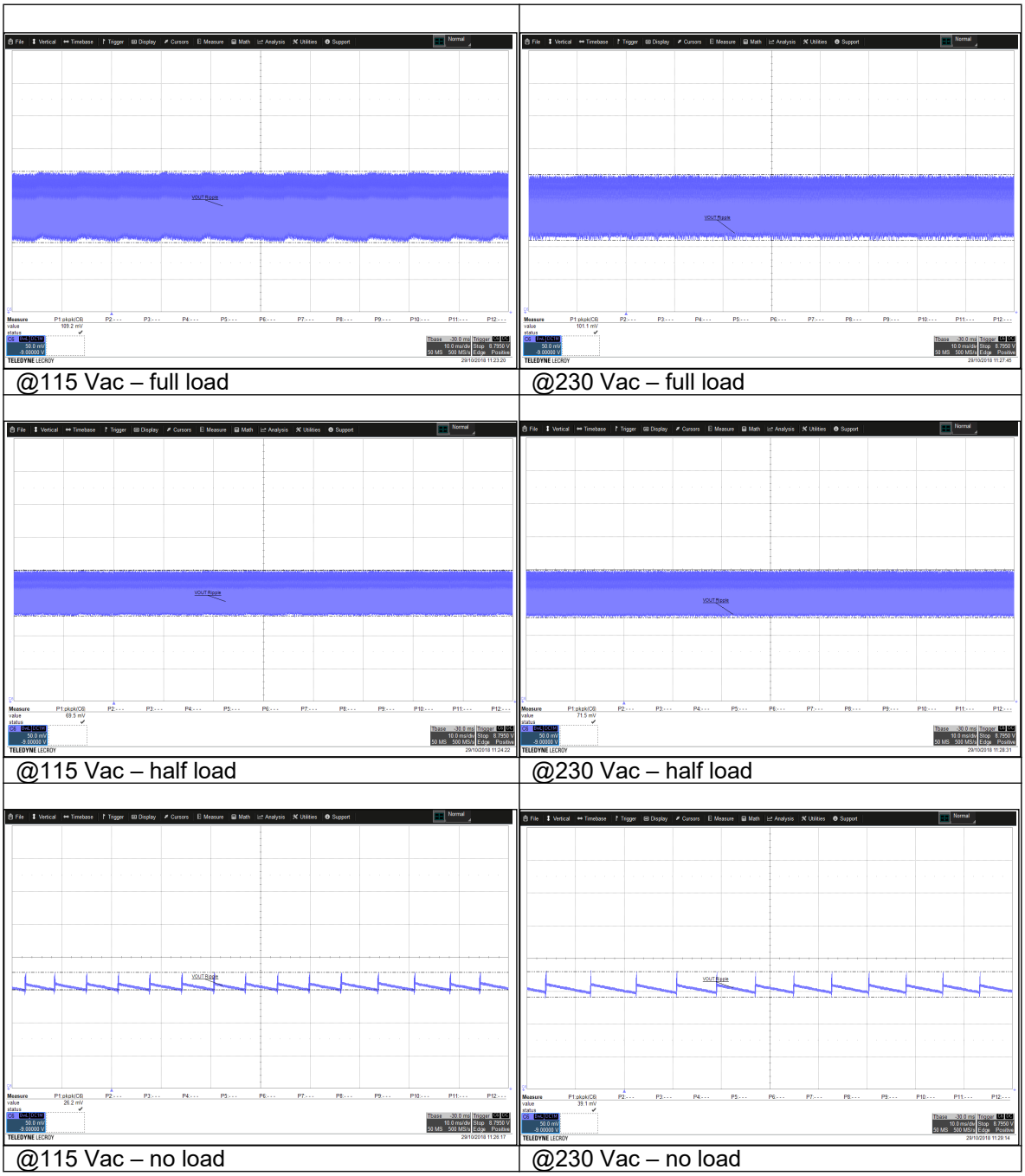


Figure 22. Output peak-to-peak ripple voltage @ +9V



@115 Vac – full load

@230 Vac – full load

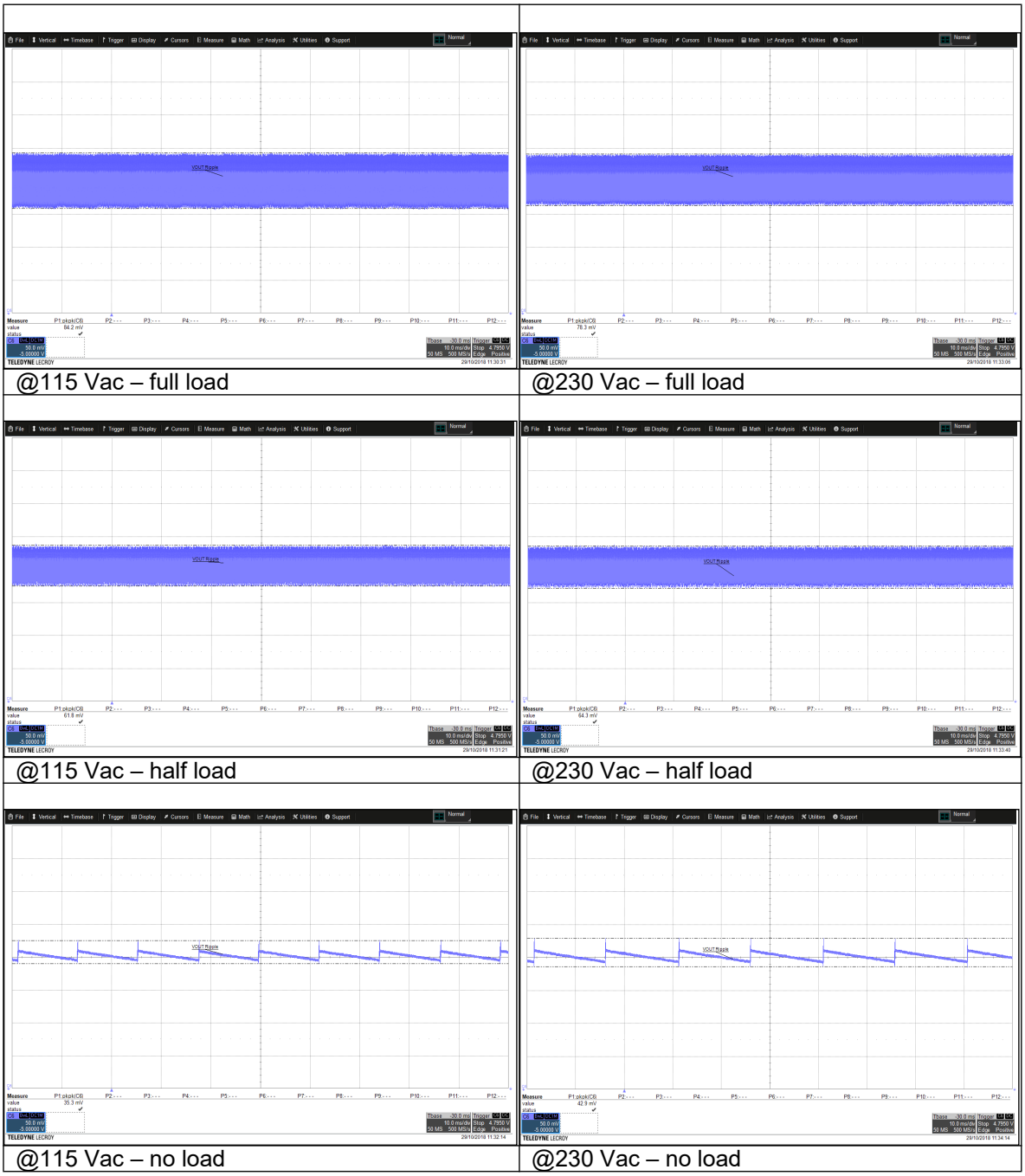
@115 Vac – half load

@230 Vac – half load

@115 Vac – no load

@230 Vac – no load

Figure 23. Output peak-to-peak rippple voltage @ +5V



@115 Vac – full load	@230 Vac – full load
@115 Vac – half load	@230 Vac – half load
@115 Vac – no load	@230 Vac – no load

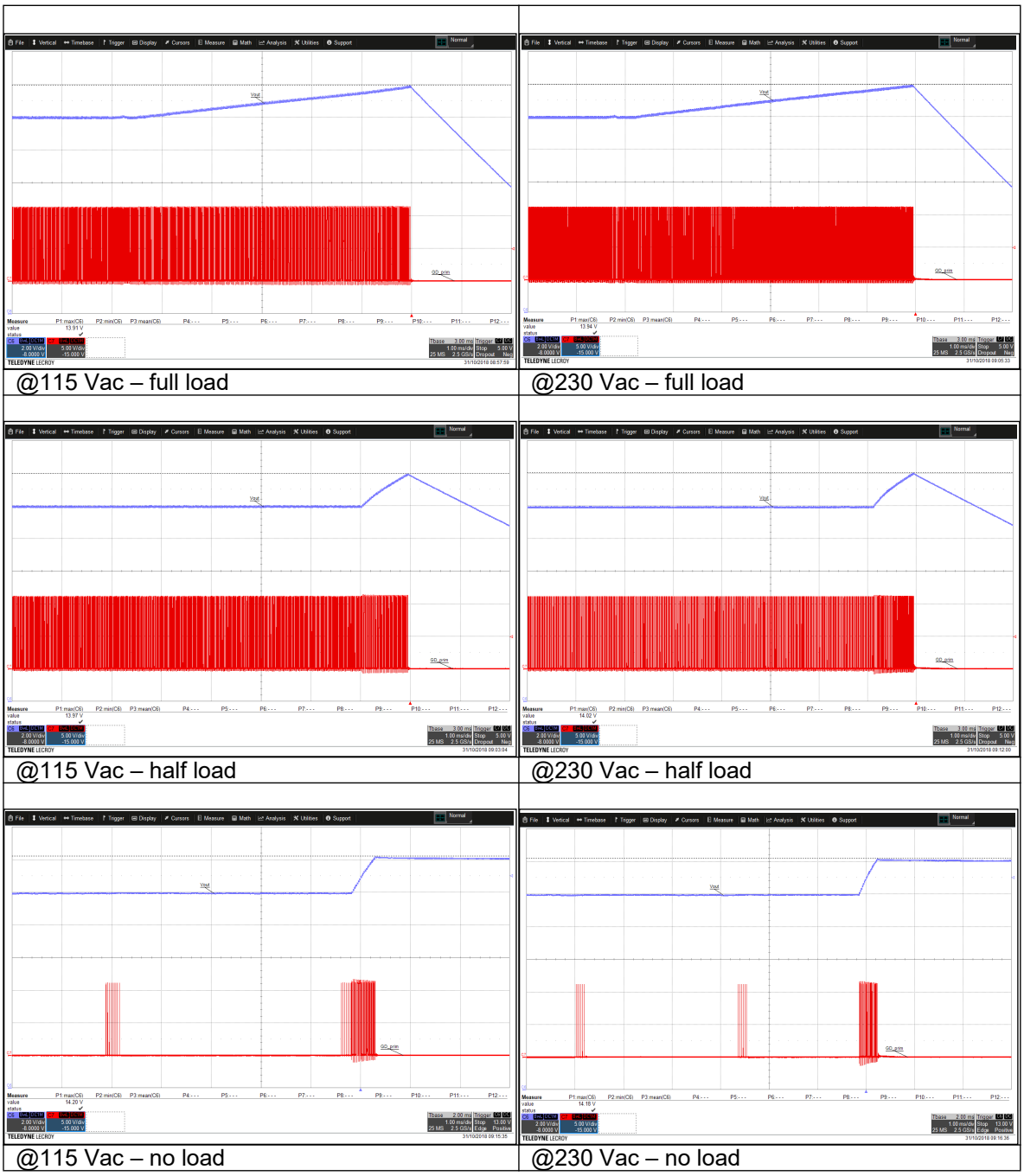
3.6 Protections (OVP - UVP - short-circuit)

Overvoltage protection: the output overvoltage protection is tested by shorting the opto-diode. This causes the converter to operate in open loop and therefore the excess power charges the output capacitance, increasing the output voltage until the protection triggers as soon as the voltage sensed on the ZCD pin of the STCH03 reaches the OVP threshold and

the converter stops switching (latched). For a restart attempt of the charger, the user needs to recycle the input voltage.

The images in *Figure 24* show the output voltage level where OVP triggers is ~14 V: since the protection is independent on output voltage setting, the test is done with Vout set at +12 V.

Figure 24. OVP triggering

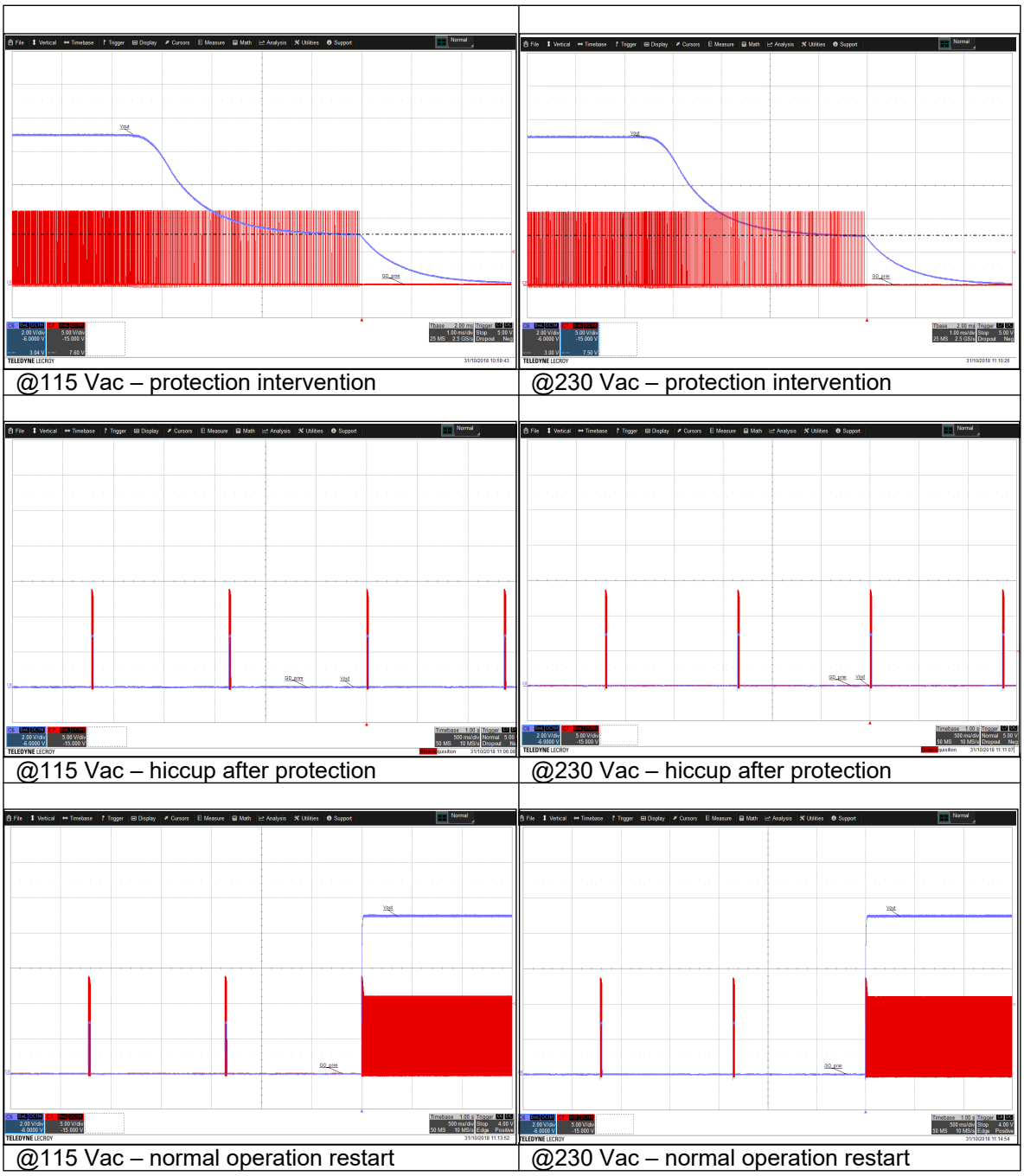


Undervoltage protection: the output undervoltage protection is tested by progressively increasing the load to enter deep CC regulation so that the output voltage and the auxiliary

voltage decrease: when this latter decreases to a level where the voltage on the ZCD pin of the STCH03 reaches the UVP threshold, the converter stops switching and starts operating in hiccup. When the load decreases, the charger restarts normal operation.

The images in *Figure 25* show the output voltage level where UVP triggers is ~3 V: since the protection is independent on output voltage setting, the test is done with V_{out} set at +9 V.

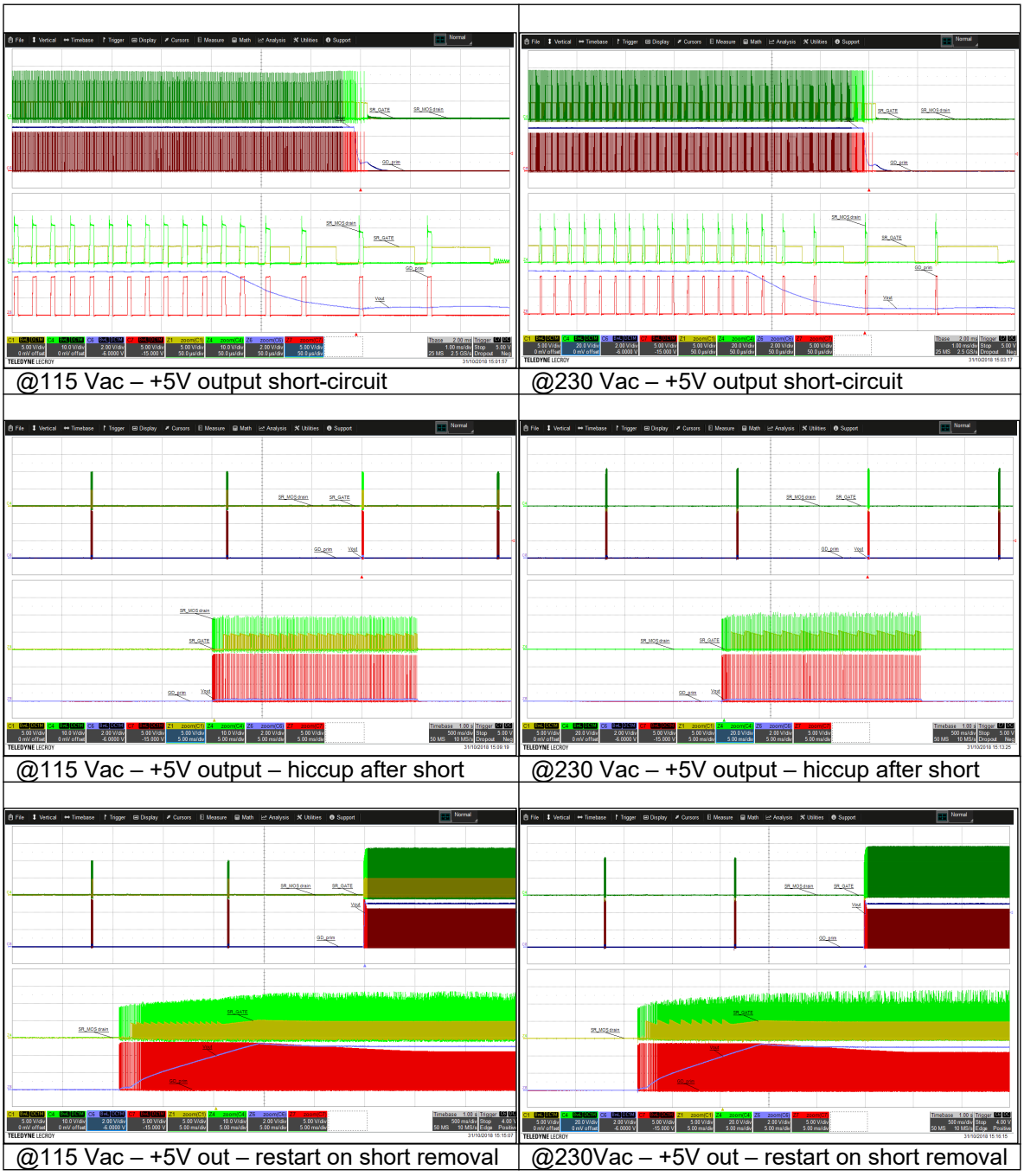
Figure 25. UVP triggering



Short-circuit: during short-circuit, since the output voltage drops to zero, also the transformer auxiliary winding voltage sensed by the ZCD pin of the STHC03 decreases, triggering the output undervoltage protection, which forces the converter to operate in hiccup, reducing in this way the input power to a value much lower than 1 W. The input power, measured by wattmeter through energy integration method, is about 130 mW at 115 Vac and 235 mW at 230 Vac.

The images in *Figure 26* show the short-circuit occurrence, with a very clean operation just before switching stop. Also the SR circuit operates correctly with no current inversion, both at protection triggering and during hiccup. After short removal, the operation resumption is correct.

Figure 26. Short-circuit protection



@115 Vac – +5V output short-circuit

@230 Vac – +5V output short-circuit

@115 Vac – +5V output – hiccup after short

@230 Vac – +5V output – hiccup after short

@115 Vac – +5V out – restart on short removal

@230Vac – +5V out – restart on short removal

4 Thermal map

A thermal analysis of the board has been performed by IR camera.

The board has been operated at nominal input voltages, with output voltage set at 12 V, and full load, and the thermal map has been taken at ambient temperature (25 °C), after 60 minutes warm-up (for thermal steady-state). The images in *Figure* and *Figure 28* below show the top-side and bottom-side thermal maps at 115 Vac and 230 Vac, respectively.

Some pointers, visible on the IR map pictures, have been placed across key components or components showing higher temperature and the data are collected in *Table 5* and *Table 6*.

Table 5. Temperature measurements at 115 Vac with Vout = 12 V @ full load

Ambient temperature:25 °C					
TOP-side components				**BOTTOM-side components**	
ITEM	Ref	Temp °C	ITEM	Ref	Temp °C
D1	A	60 °C	Q1	M	60 °C
L1	B	49 °C	Q3	N	64 °C
R1	C	75 °C	Q5	O	58 °C
C1	D	49 °C	U1	P	54 °C
C2	E	52 °C	U6	Q	60 °C
C6	F	44 °C	D2	R	68 °C
C7	G	45 °C	R2	S	72 °C
C12	H	39 °C	R4	T	80 °C
C14	I	45 °C	R9	U	57 °C
T1 (Fe)	J	65 °C	R10	V	57 °C
T1 (Cu)	K	60 °C			
U2	L	44 °C			

Table 6. Temperature measurements at 230 Vac with Vout = 12 V @ full load

Ambient temperature:25 °C					
TOP-side components				**BOTTOM-side components**	
ITEM	Ref	Temp °C	ITEM	Ref	Temp °C
D1	A	52 °C	Q1	M	68 °C
L1	B	45 °C	Q3	N	66 °C
R1	C	58 °C	Q5	O	62 °C

Table 6. Temperature measurements at 230 Vac with Vout = 12 V @ full load

Ambient temperature:25 °C						
TOP-side components				BOTTOM-side components		
C1	D	46 °C		U1	P	57 °C
C2	E	52 °C		U6	Q	64 °C
C6	F	42 °C		D2	R	75 °C
C7	G	43 °C		R2	S	77 °C
C12	H	40 °C		R4	T	87 °C
C14	I	46 °C		R9	U	56 °C
T1 (Fe)	J	68 °C		R10	V	56 °C
T1 (Cu)	K	63 °C				
U2	L	44 °C				

Figure 27. Thermal map at 115 Vac with Vout = 12 V @ full load

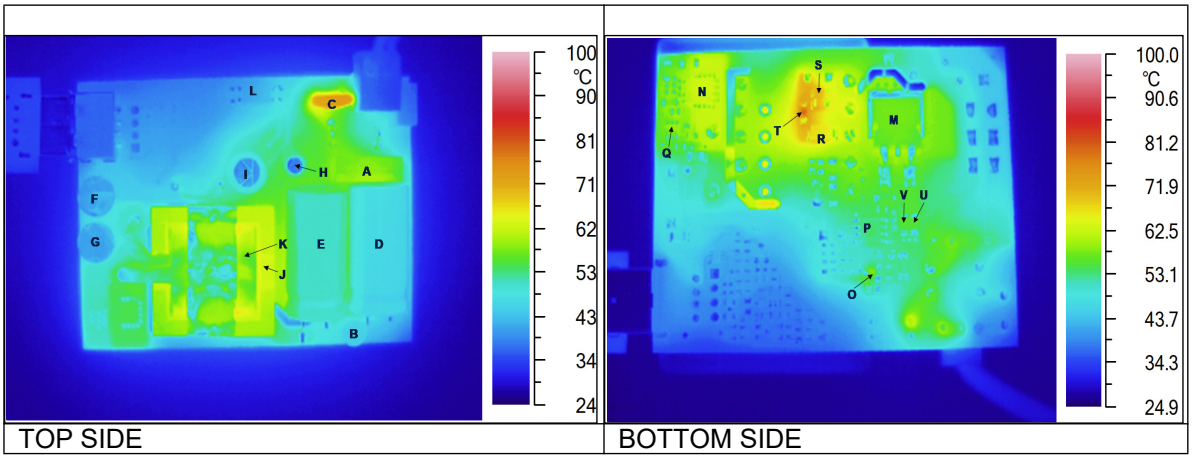
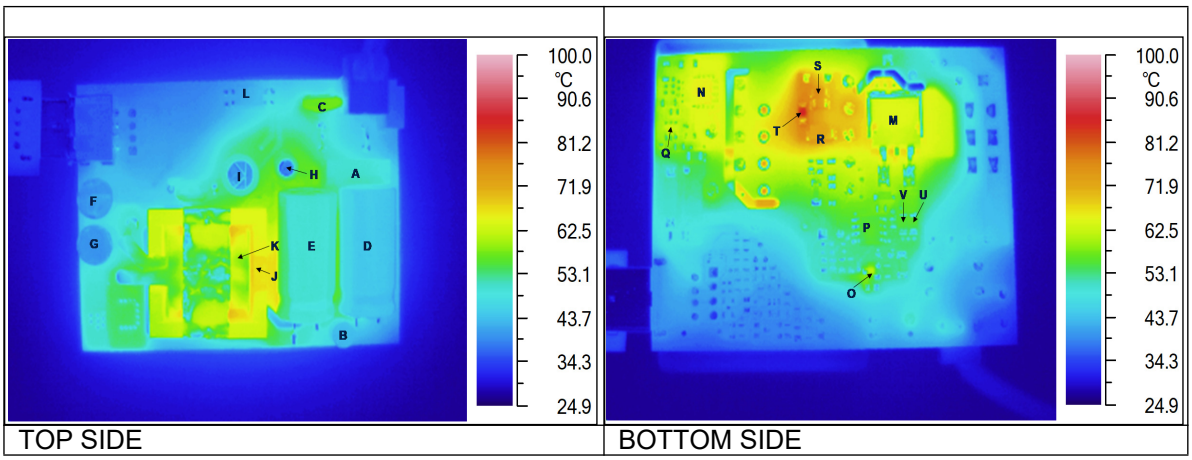


Figure 28. Thermal map at 230 Vac with Vout = 12 V @ full load



5 Line conducted interference

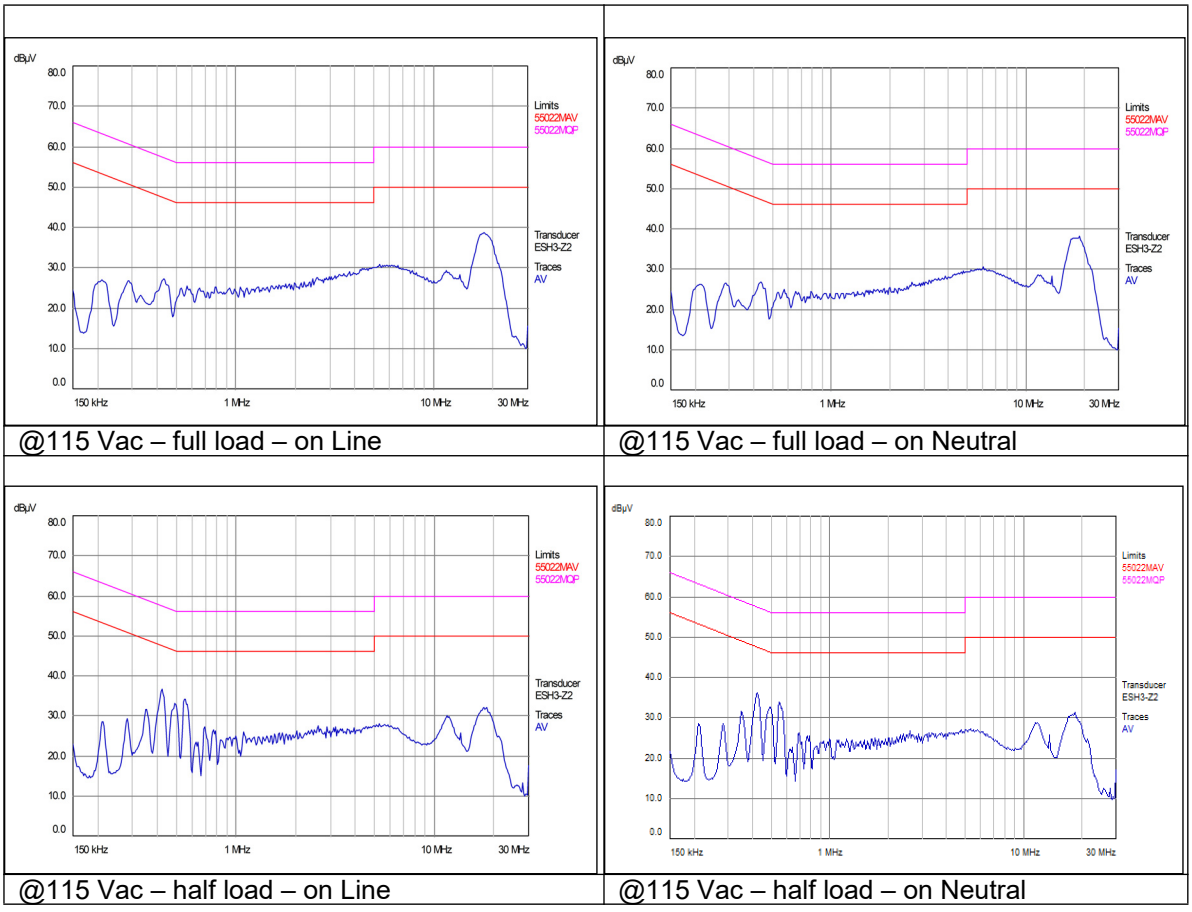
A pre-compliance test for EN55022 (Class B) European regulation for domestic equipment is performed, measuring the line conducted noise emissions at nominal mains voltages, at full and half load.

The various measurements shown in *Figure 29* to *Figure 34* below have been performed using the average EMI detector configuration of the EMC analyzer receiver.

The Class B limits for domestic equipment are more severe compared to the Class-A requirements, dedicated to information technology equipment. The lower limit in the graphs refers to the Class B average measurement set-up.

The results show a comfortable margin between the measurements and the required limits.

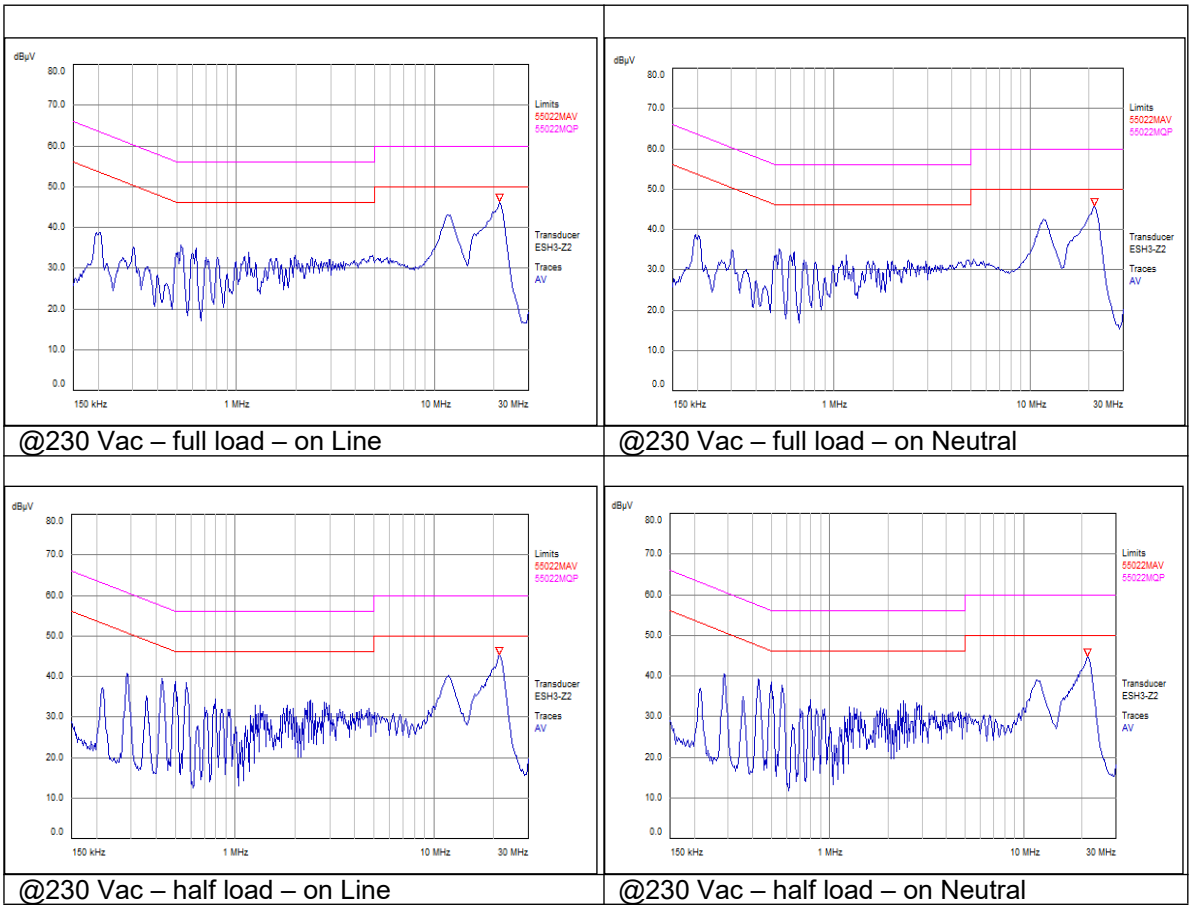
Figure 29. EMI measurements at low mains for +12 V output



@115 Vac – full load – on Line | @115 Vac – full load – on Neutral

@115 Vac – half load – on Line | @115 Vac – half load – on Neutral

Figure 30. EMI measurements at high mains for +12 V output



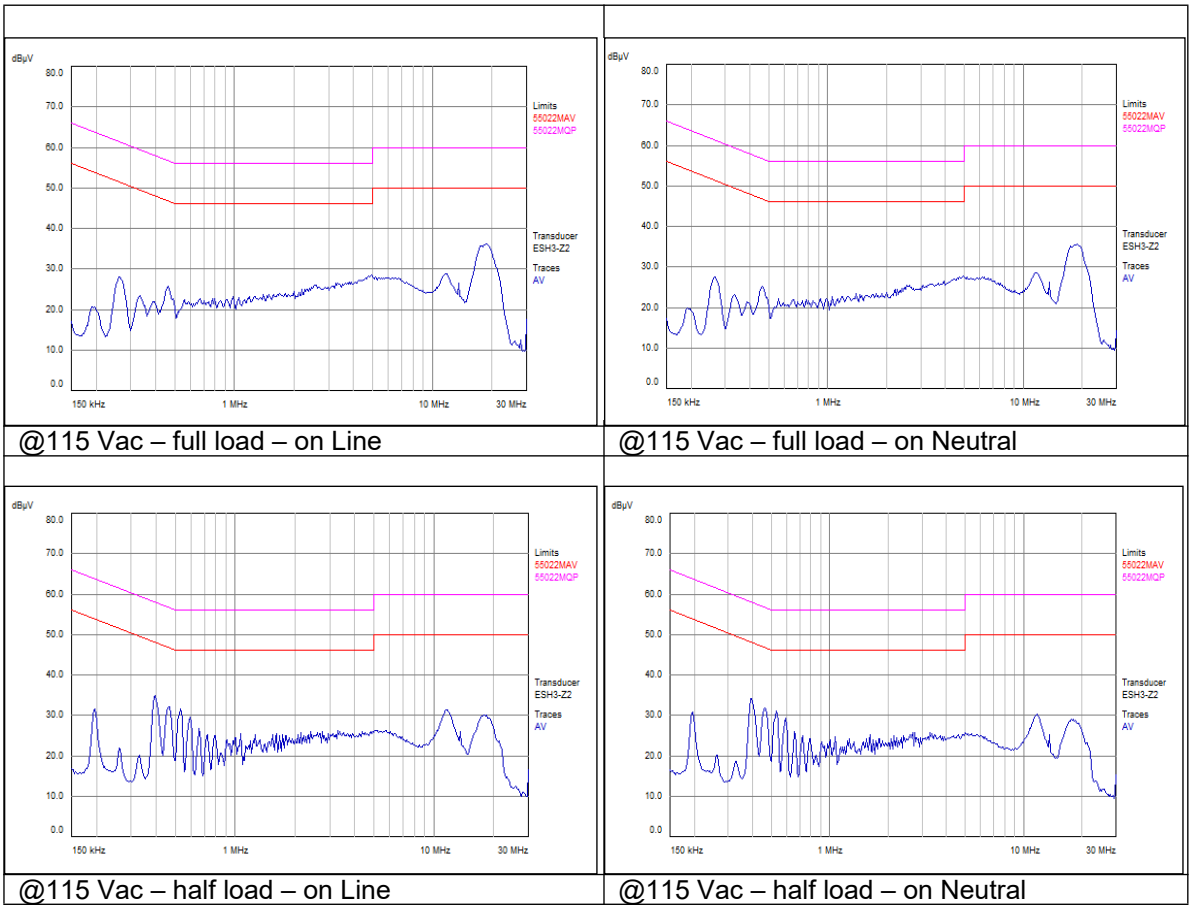
@230 Vac – full load – on Line

@230 Vac – full load – on Neutral

@230 Vac – half load – on Line

@230 Vac – half load – on Neutral

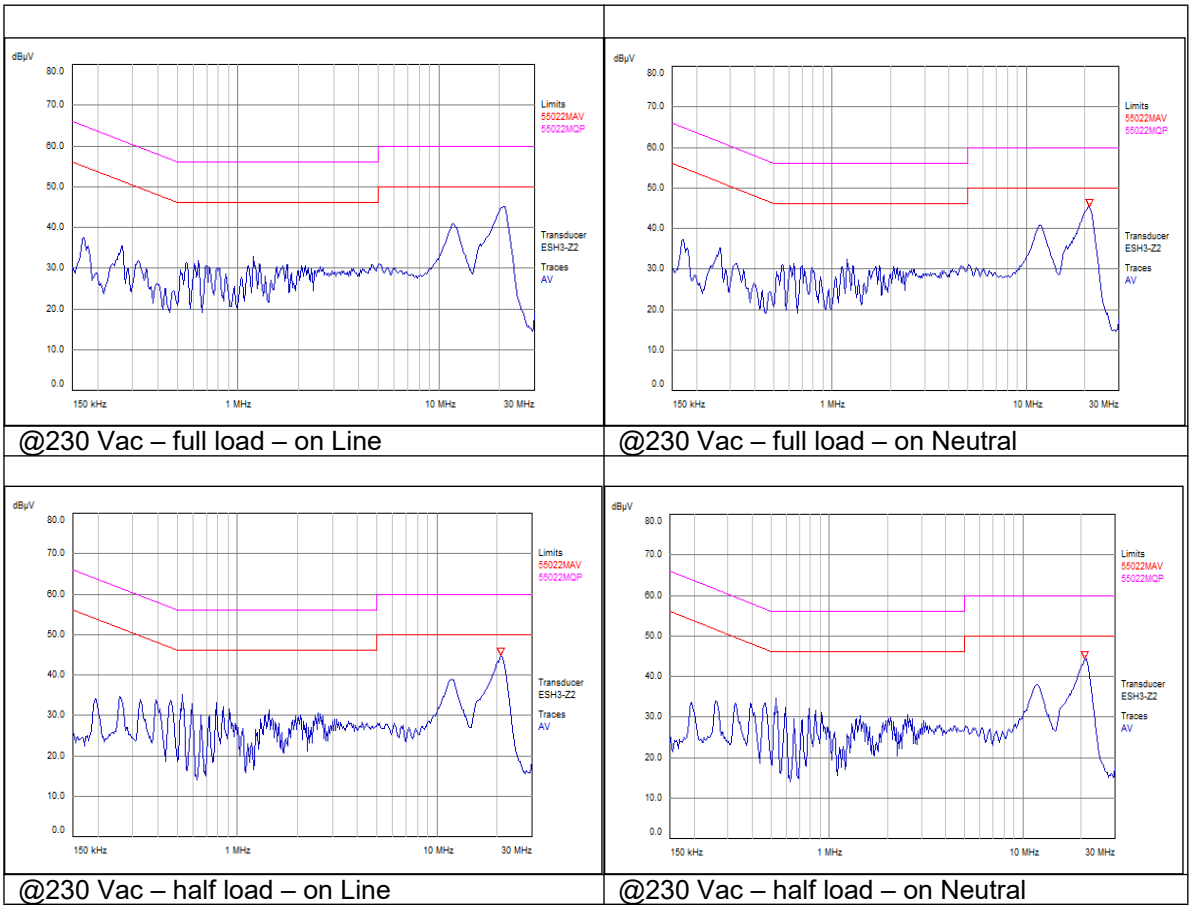
Figure 31. EMI measurements at low mains for +9 V output



@115 Vac – full load – on Line | @115 Vac – full load – on Neutral

@115 Vac – half load – on Line | @115 Vac – half load – on Neutral

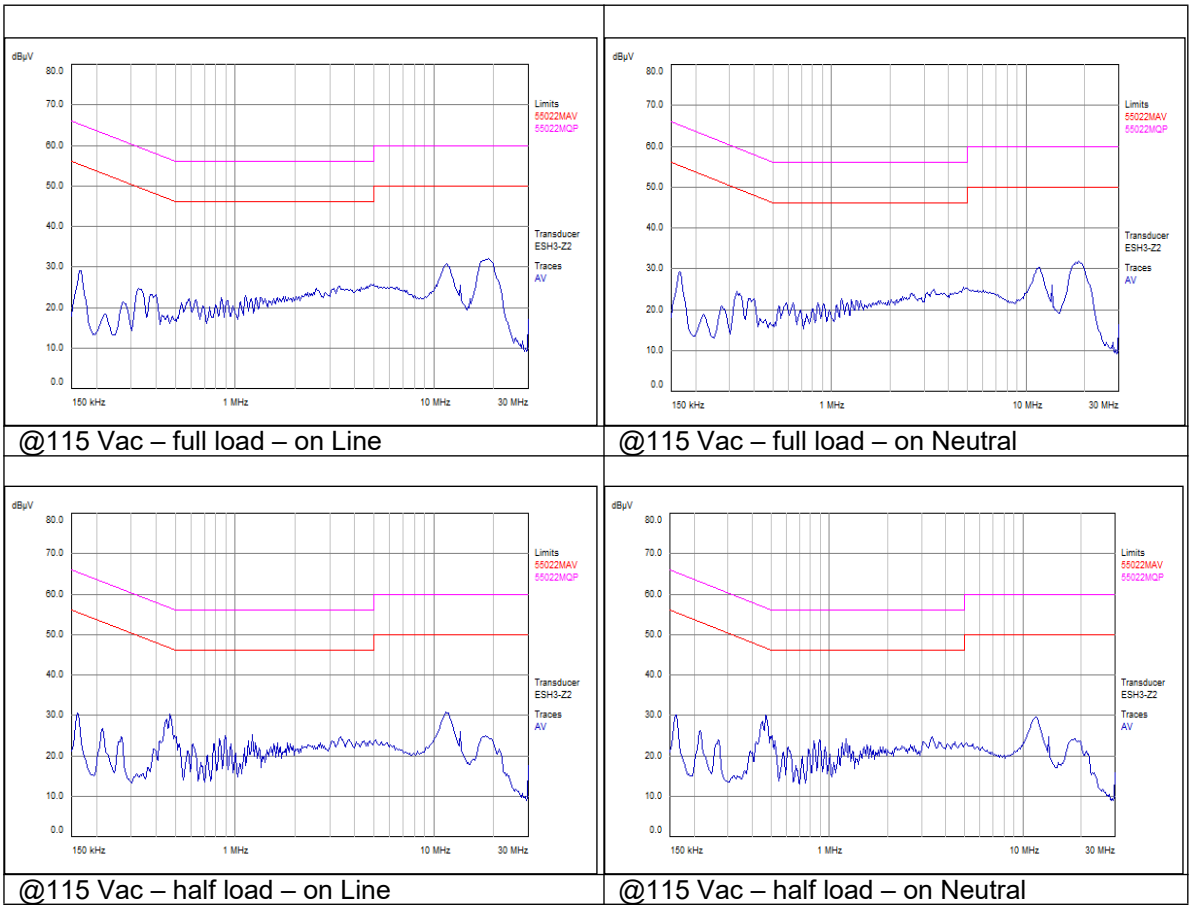
Figure 32. EMI measurements at high mains for +9 V output



@230 Vac – full load – on Line | @230 Vac – full load – on Neutral

@230 Vac – half load – on Line | @230 Vac – half load – on Neutral

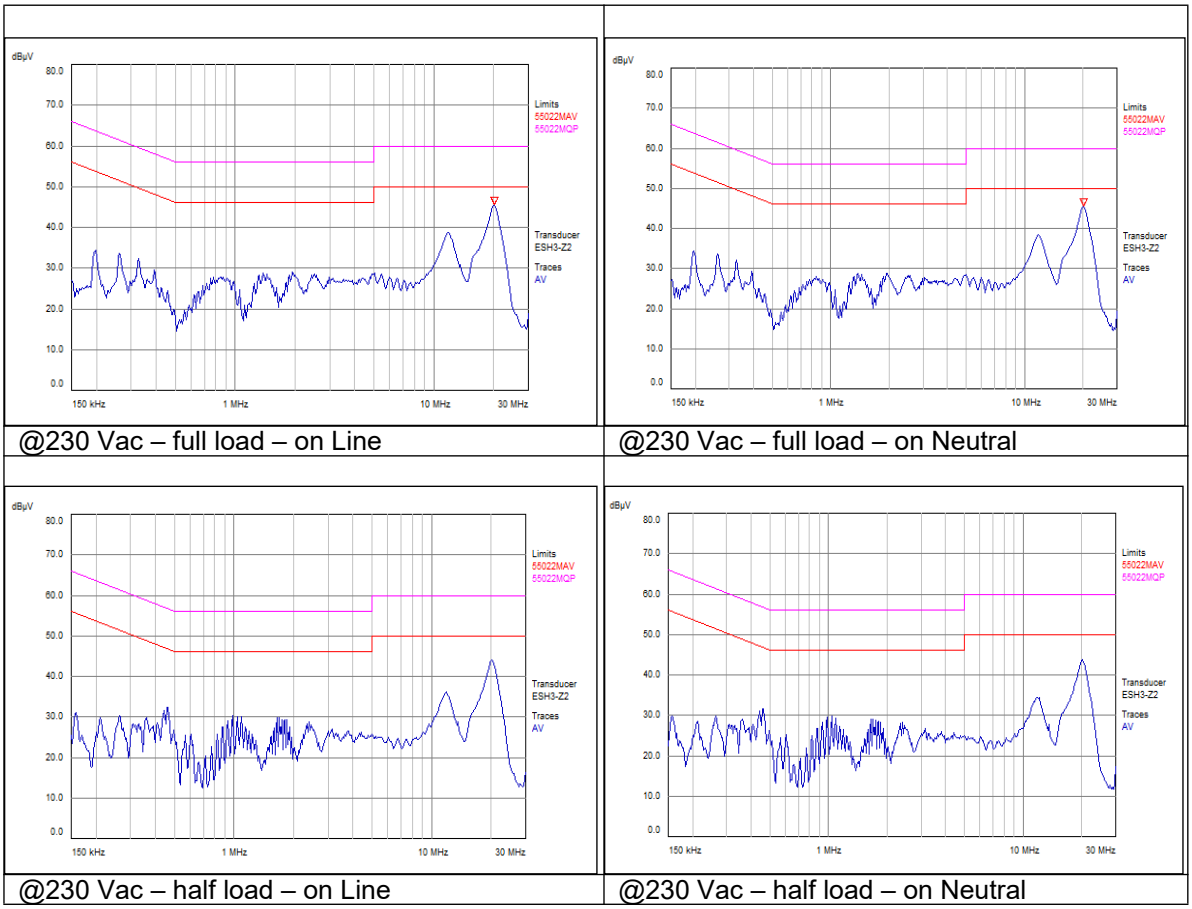
Figure 33. EMI measurements at low mains for +5 V output



@115 Vac – full load – on Line | @115 Vac – full load – on Neutral

@115 Vac – half load – on Line | @115 Vac – half load – on Neutral

Figure 34. EMI measurements at high mains for +5 V output



@230 Vac – full load – on Line | @230 Vac – full load – on Neutral

@230 Vac – half load – on Line | @230 Vac – half load – on Neutral

Appendix A APPENDIX

A.1 Bill of material

The bill of material of the EVLSTCH03-36W-SR board is listed in *Table 7* here below.

Table 7. EVLSTCH03-36W-SR - bill of material

Ref	Description	Value / PN	Supplier
C1	ALUMINIUM ELCAP - CY SERIES - 105°C - 400V	33uF-400V	NICHICON
C2	ALUMINIUM ELCAP - CY SERIES - 105°C - 400V	33uF-400V	NICHICON
C3	SMD-1206 1kV CERCAP X7R - GENERAL PURPOSE	1nF-1kV	AVX
C4	SMD-0805 50V CERCAP X7R - GENERAL PURPOSE	100nF	AVX
C5	SMD-0805 50V CERCAP X7R - GENERAL PURPOSE	1uF	MURATA
C6	CONDUCTIVE POLYMER ALUM. SOLID ELCAP - PLG SERIES - 105°	470uF-16V	NICHICON
C7	CONDUCTIVE POLYMER ALUM. SOLID ELCAP - PLG SERIES - 105°	470uF-16V	NICHICON
C8	SMD-1206 50V CERCAP X7R - GENERAL PURPOSE	1uF-50V	MURATA
C9	SMD-0805 50V CERCAP X7R - GENERAL PURPOSE	220pF	AVX
C11	CERAMIC X1/Y1 DISC CAPACITOR 900 SERIES 250 VAC	2.2nF-Y	KEMET
C12	ALUMINIUM ELCAP - YXF SERIES - 105°C	22uF-50V	RUBYCON
C13	SMD-0805 50V CERCAP X7R - GENERAL PURPOSE	33nF	AVX
C14	ALUMINIUM ELCAP - YXF SERIES - 105°C	22uF-100V	RUBYCON
C15	SMD-0805 50V CERCAP X7R - GENERAL PURPOSE	100nF	AVX
C17	SMD-0805 25V CERCAP X7R - GENERAL PURPOSE	4.7uF	TDK
C19	SMD-1206 100V CERCAP X7R - FIEXITERM SERIES	1uF-100V	AVX
D1	GLASS PASSIVATED BRIDGE RECTIFIER	2KBP06M	VISHAY
D2	HIGH VOLTAGE FAST RECTIFIER	RS1K	FAIRCHILD
D4	SMALL SIGNAL SWITCHING DIODE	1N4148W	VISHAY
D5	SMALL SIGNAL SWITCHING DIODE	BAV103	VISHAY
D6	ZENER DIODE BZV55 SERIES 2%	BZV55-B10	NXP
D7	SMALL SIGNAL SCHOTTKY DIODE	BAT43WS	DIODES ZETEX
D8	SMALL SIGNAL SCHOTTKY DIODE	1N4148WS	DIODES ZETEX
F1	FUSE SS-5F SERIES 2.5A-250 VAC FAST ACTING	2.5A-F-250Vac	BUSSMAN
J1	CONNECTOR MKDS 3.81	IN-CON	PHOENIX
J2	USB TYPE-A FEMALE CONNECTOR	USB TYPE-A F	WURTH ELEKTRONIK
L1	DRUM FILTER CHOKE WE-TI	47uH	WURTH ELEKTRONIK

Table 7. EVLSTCH03-36W-SR - bill of material (continued)

Ref	Description	Value / PN	Supplier
L2	WE-PMI CHIP MULTILAYER INDUCTOR	4.7uH	WURTH ELEKTRONIK
Q1	N-CHANNEL POWER MOSFET	STB13N80K5	STMicroelectronics
Q2	N-CHANNEL 20V MOSFET	STR2N2VH5	STMicroelectronics
Q3	SMALL SIGNAL N-CHANNEL DEPLETION MOSFET 100V	BSS169	INFINEON
Q4	DUAL N-CANNEL POWER TRENCH MOSFET	FDG8850NZ	FAIRCHILD
Q5	N-CHANNEL POWER MOSFET 100V LL	FDMS86103L	FAIRCHILD
R1	INRUSH CURRENT LIMITING RESISTOR NTC	NTC-5R	EPCOS
R2	SMD-1206 STAND. FILM RES - 1/4W - 5% - 200ppm/°C	330k	BC COMPONENTS
R3	SMD-0805 STAND. FILM RES - 1/8W - 5% - 250ppm/°C	2k4	BC COMPONENTS
R4	SMD-1206 STAND. FILM RES - 1/4W - 5% - 200ppm/°C	430R	BC COMPONENTS
R6	SMD-0805 STAND. FILM RES - 1/8W - 5% - 200ppm/°C	10R	BC COMPONENTS
R9	SMD-1206 STAND. FILM RES - 1/4W - 1% - 100ppm/°C	0.56R	BC COMPONENTS
R10	SMD-1206 STAND. FILM RES - 1/4W - 1% - 100ppm/°C	0.51R	BC COMPONENTS
R11	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	33R	BC COMPONENTS
R13	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	220k	BC COMPONENTS
R14	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	33k	BC COMPONENTS
R15	SMD-0805 STAND. FILM RES - 1/8W - 5% - 250ppm/°C	1k0	BC COMPONENTS
R16	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	24k	BC COMPONENTS
R17	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	68k	BC COMPONENTS
R18	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	12k	BC COMPONENTS
R19	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	100k	BC COMPONENTS
R20	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	100k	BC COMPONENTS
R23	SMD-0805 STAND. FILM RES - 1/8W - 5% - 200ppm/°C	1k	BC COMPONENTS
R24	SMD-0805 STAND. FILM RES - 1/8W - 5% - 250ppm/°C	20k	BC COMPONENTS
R25	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	12k	BC COMPONENTS
R26	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	300k	BC COMPONENTS
R27	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	10R	BC COMPONENTS
R28	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	100k	BC COMPONENTS
R29	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	4k7	BC COMPONENTS
R30	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	82k	BC COMPONENTS
R32	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	18k	BC COMPONENTS
R33	SMD-0805 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	300k	BC COMPONENTS
R34	SMD-0805 STAND. FILM RES - 1/8W - 5% - 250ppm/°C	0R	BC COMPONENTS
R36	SMD-1206 STAND. FILM RES - 1/4W - 5% - 200ppm/°C	0R	BC COMPONENTS

Table 7. EVLSTCH03-36W-SR - bill of material (continued)

Ref	Description	Value / PN	Supplier
R37	SMD-0805 STAND. FILM RES - 1/8W - 5% - 250ppm/°C	330R	BC COMPONENTS
R38	SMD-0805 STAND. FILM RES - 1/8W - 5% - 250ppm/°C	1k5	BC COMPONENTS
R39	SMD-0603 STAND. FILM RES - 1/8W - 1% - 100ppm/°C	100k	BC COMPONENTS
R41	SMD-0603 STAND. FILM RES - 1/8W - 5% - 250ppm/°C	1M0	BC COMPONENTS
T1	FLYBACK TRANSFORMER EFD25-700uH	MAG-1318.0018	AQ MAGNETICA
U1	OFF-LINE CC MODE PRIMARY-SENSING SWITCHING CONTROLLER	STCH03L	STMicroelectronics
U2	HR OPTOCOUPLER 400 MIL (OPT 6)	SFH617-A2	VISHAY
U3	PRECISION RAIL-TO-RAIL COMPARATOR	LT1716	LINEAR TECH.
U4	0.5% LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATOR	TLVH431	STMicroelectronics
U5	0.5% LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATOR	TLVH431	STMicroelectronics
U6	ADAPTIVE SYNCH RECTIFICATION FLYBACK CONTROLLER	SRK1000B	STMicroelectronics

A.2 Transformer specification

The part number of the flyback transformer is 1318.0018 by AQ Magnetica.

DESCRIPTION

The transformer uses two ferrite cores (2 x) EFD25 with material grade N87, center-leg gapped to obtain the required primary inductance of 700 µH. The max. leakage inductance is less than 2% of the primary inductance.

The coil former is a 5+4 pins type (with pin 6 removed), with flying secondary winding terminals (F1 and F2).

Two wound copper shields for EMI are realized internally, between primary and secondary windings, using copper wire with diameter 0.16 mm, connected to PIN 5.

A further external copper tape shield (10 mm x 35 µm) is placed around the ferrite core halves, (once they are assembled onto the coilformer) connected to PIN 5.

Table 8. Electrical data

Item name	Value	Measurement condition
Primary inductance $L_{3.1}$	700 µH ± 5%	@ 100kHz - 1V
Leakage inductance $L_{3.1}$	15 µH max. (< 2% of primary inductance)	@ 100kHz - 1V Pin 4-5 and F1-F2 shorted
Prim to Sec turn ratio	9.43 ± 5%	
Prim to Aux turn ratio	3.88 ± 5%	
Insulation	3kV/3sec/AC/5mA 1kV/3sec/AC/5mA 3kV/3sec/AC/5mA	Primary to secondary Primary to core Secondary to core

Figure 35. Electrical schematic and winding sequence

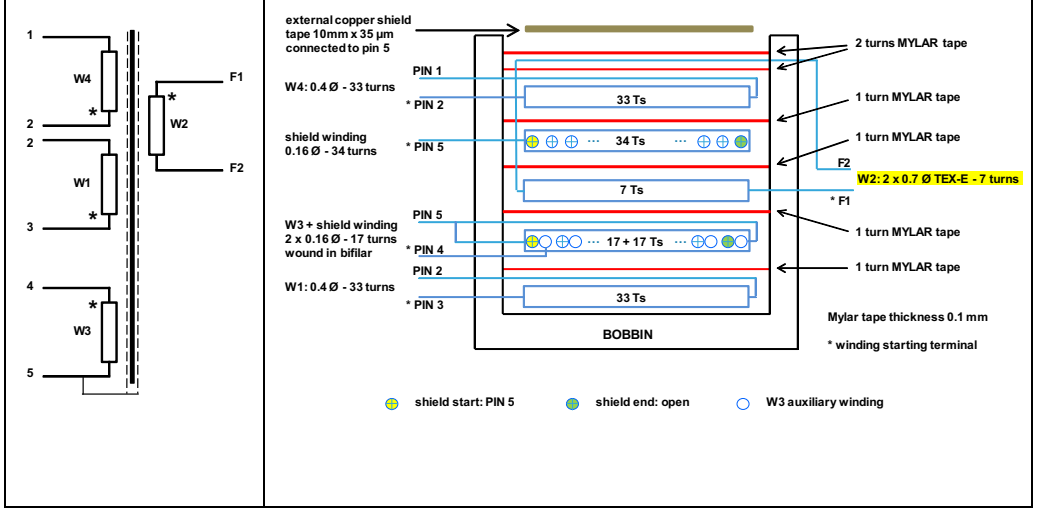
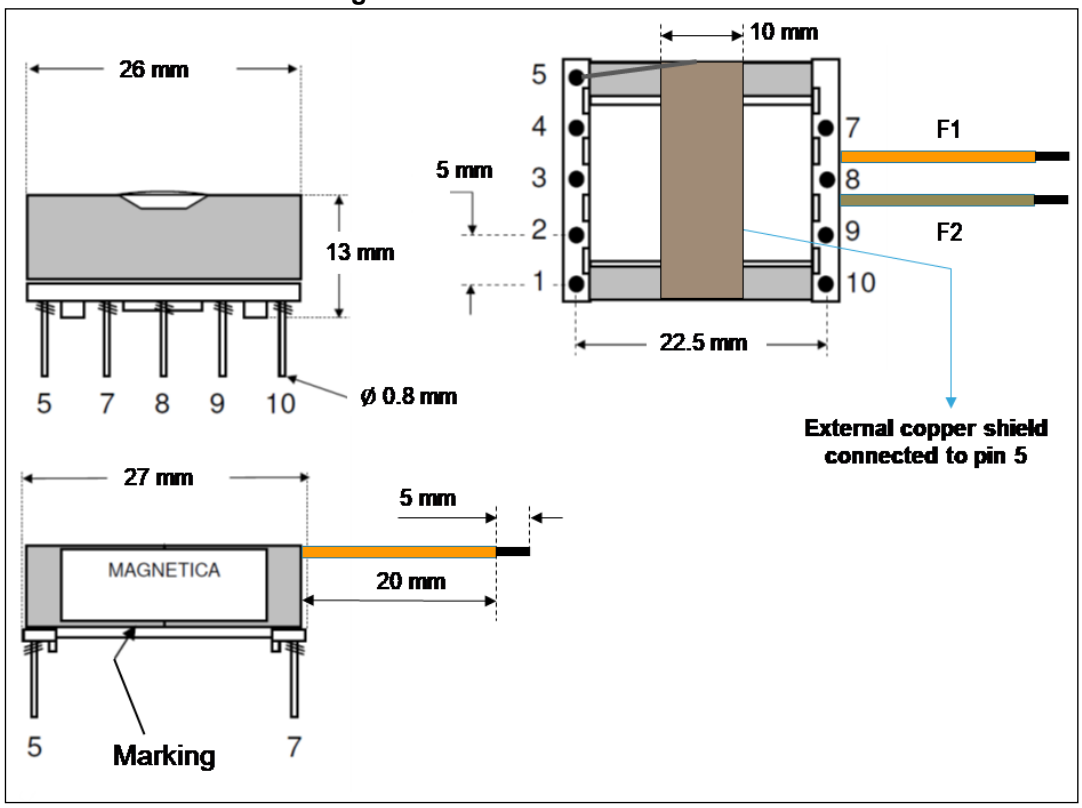


Figure 36. Mechanical dimensions

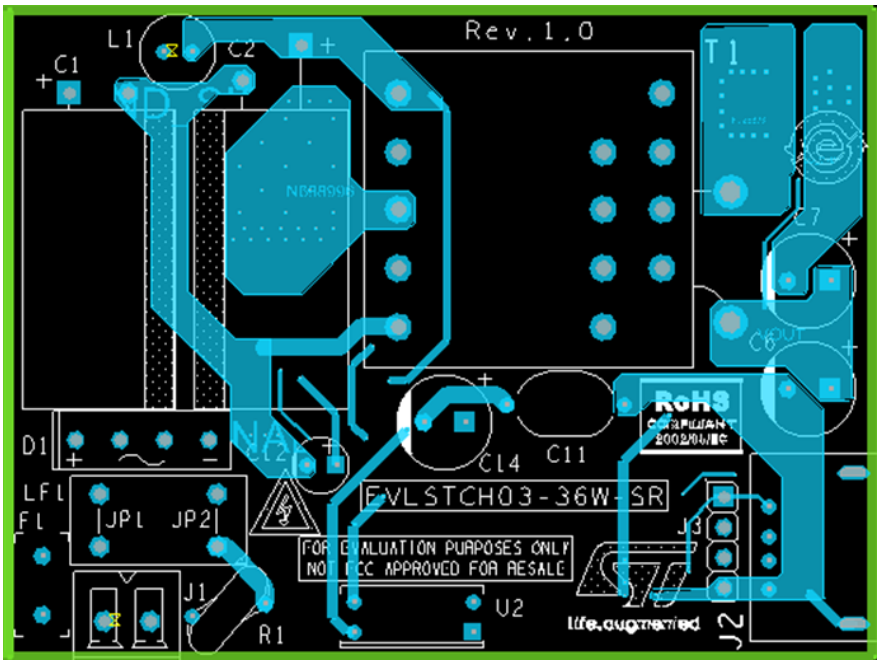


A.3 PCB layout

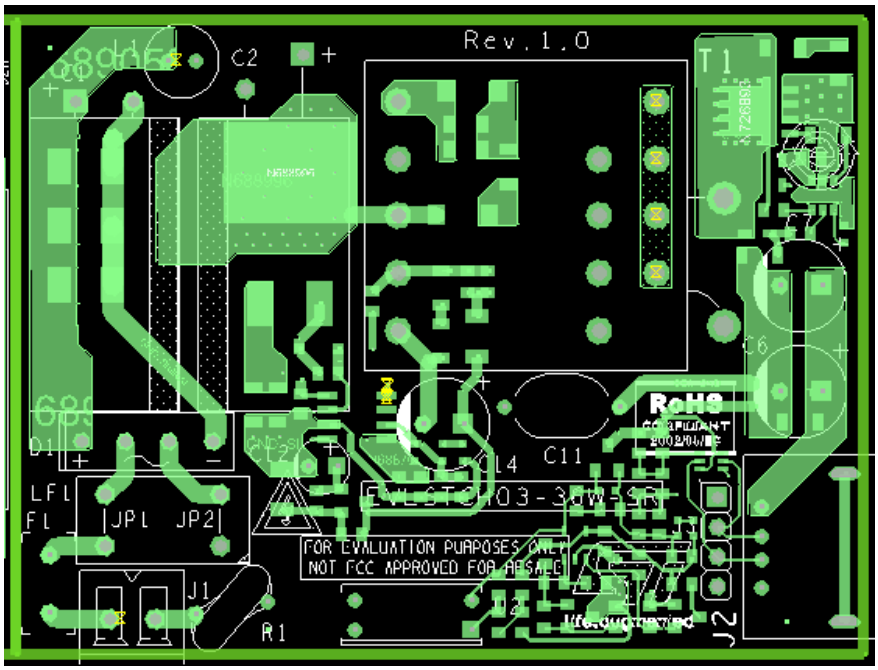
The PCB uses a two-layer technology, in FR4 material, RoHS compliant, with copper thickness of 70 µm. Dimensions are 73 mm x 55 mm. The PCB layout is shown in *Figure 37* here below.

Figure 37. Board layout (top and bottom layers)

Top layer



Bottom layer



6 References

1. STCH03 Datasheet: available at *www.st.com*/
2. SRK1000/SRK1000A/SRK1000B Datasheet: available at *www.st.com*
3. AN5066 application note: available at *www.st.com*

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Mar-2019	1	Initial release.