STEVAL-IPFC12V1 2 kW two channel interleaved PFC with STNRGPF12 digital controller featuring inrush current control

Introduction

The STEVAL-IPFC12V1 is a 2 kW interleaved PFC evaluation board for the STNRGPF12 digital configurable IC, which is able to manage the inrush current and drive up to two channels in an interleaved PFC for industrial applications.

The evaluation board achieves high power density, thanks to a compact layout with small magnetic components, which is possible because of the interleaving effect.

Moreover, the PFC is used to satisfy the IEC 61000-3-2 standard for electrical equipment.

Figure 1. STEVAL-IPFC12V1 evaluation board

The STNRGPF12 controller is embedded on a separate control board and implements mixed signal (analog/digital) average current mode control in CCM at a fixed frequency. The analog section ensures cycle by cycle current regulation, while digital control manages the non-time critical operations, providing further flexibility.

The device can be customized for different applications by using a dedicated software tool.

RELATED LINKS

Visit the STNRGPF12 web folder on www.st.com for all the available data and information regarding the device

1 Safety instructions

Danger:

The evaluation board uses voltage levels that can cause serious injury and even death.

Do not touch any of the boards immediately after disconnecting the input power supply as the charged capacitors need time to discharge.

Due to the high power density, the board components and the heat sink can become very hot and cause severe burns when touched.

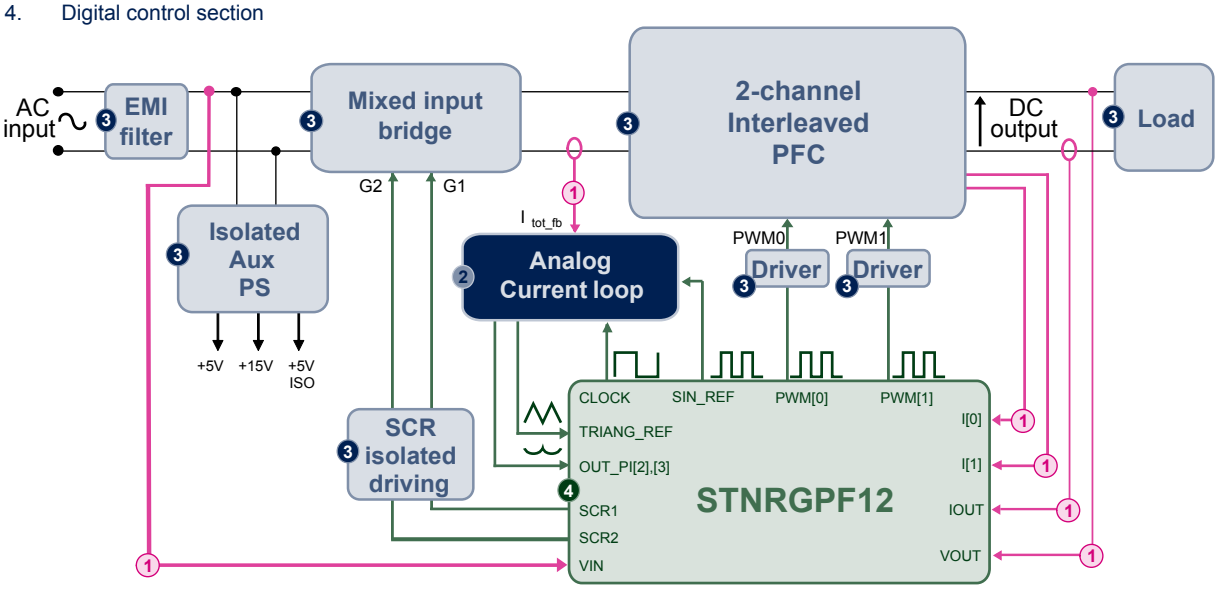
This board is intended for use by skilled technical personnel who are suitably qualified and familiar with the installation, use and maintenance of power electronic systems. The same personnel must be aware of and must apply national accident prevention rules.

The electrical installation shall be completed in accordance with the appropriate requirements (e.g., cross-sectional areas of conductors, fusing, and GND connections).

2 Functional overview

Figure 2. STEVAL-IPFC12V1 block diagram

1. I/O measurement signals
2. Analog circuitry
3. Power stages
4. Digital control section



When an AC input voltage in the appropriate range is supplied, the auxiliary power supply starts supplying voltages for the STNRGPF12 and drivers. The digital inrush current control then starts and the DC output voltage increases up to the peak value of the line input voltage.

I/O measurement signals are used to:

- Verify starting and operating conditions (for example, 50/60 Hz, load/no-load start-up etc.)
- Regulate DC output voltage
- Generate feed-forward compensation, phase shedding and current balance functions
- Trigger cooling system and safety shut-down (for example, due to over- or under-voltage conditions)

The STNRGPF12 outputs a sinusoidal current reference (SIN_REF) for the input current regulation performed by analog circuitry, which provides the signals (TRIANG_REF, OUT_PI[2],[3]) for triangular-carrier PWM modulation.

The PWM signals (PWM0, PWM1) drive the two interleaved channels, while the SCR1 and SCR2 pins are used to switch on the two SCRs of the mixed input bridge.

The status LEDs indicate the following conditions:

- Green LED: PFC_OK, start-up has completed
- Red LED: PFC_FAULT, a fault has occurred

Certain STNRGPF12 functions and parameters are configurable through the eDesign Suite tool.

RELATED LINKS

7 PFC controller customization with eDesign Suite on page 30

3 Power factor correction

In many applications, ranging from telecom to common industrial power supplies (SMPS), active Power Factor Corrector (PFC) converters are used as the first stage in AC/DC conversion to draw a sinusoidal-shape input current in phase with grid voltage.

PFCs allow any downstream electrical appliance to appear as a purely resistive load, and improve the overall grid efficiency.

3.1 Power factor (PF) - definition

The total power absorbed by a load connected to the grid is known as apparent power, which includes two components:

1. Real power: the power that actually produces work (e.g., motion, heating) in a system.
2. Reactive power: required by inductive loads for normal operation.

The ratio between real power and apparent power is known as power factor (PF):

$$PF = \frac{realpower}{apparentpower} \quad (1)$$

In a real system, the PF can be calculated as:

$$PF = displacementfactor \times distortionfactor = \frac{\cos\phi}{\sqrt{1+THD^2}} \quad (2)$$

where:

- $\cos\phi$ = displacement factor: the phase shift between input current and line voltage.
- $\frac{1}{\sqrt{1+THD^2}}$ = distortion factor: the PF degradation due to the harmonic component of input current.

The total harmonic distortion (THD) takes into account the amplitude of input current harmonics with respect to the fundamental component:

$$THD = \sqrt{\Sigma_i^n = 2\left(\frac{I_i}{I_1}\right)^2} \quad (3)$$

Where:

- I_1 = input current at fundamental frequency
- I_i = ith harmonic of input current

The ideal condition is to have a displacement factor of one and a THD as low as possible, so the apparent power is minimized and the size and cost of generators and transmission lines can be reduced.

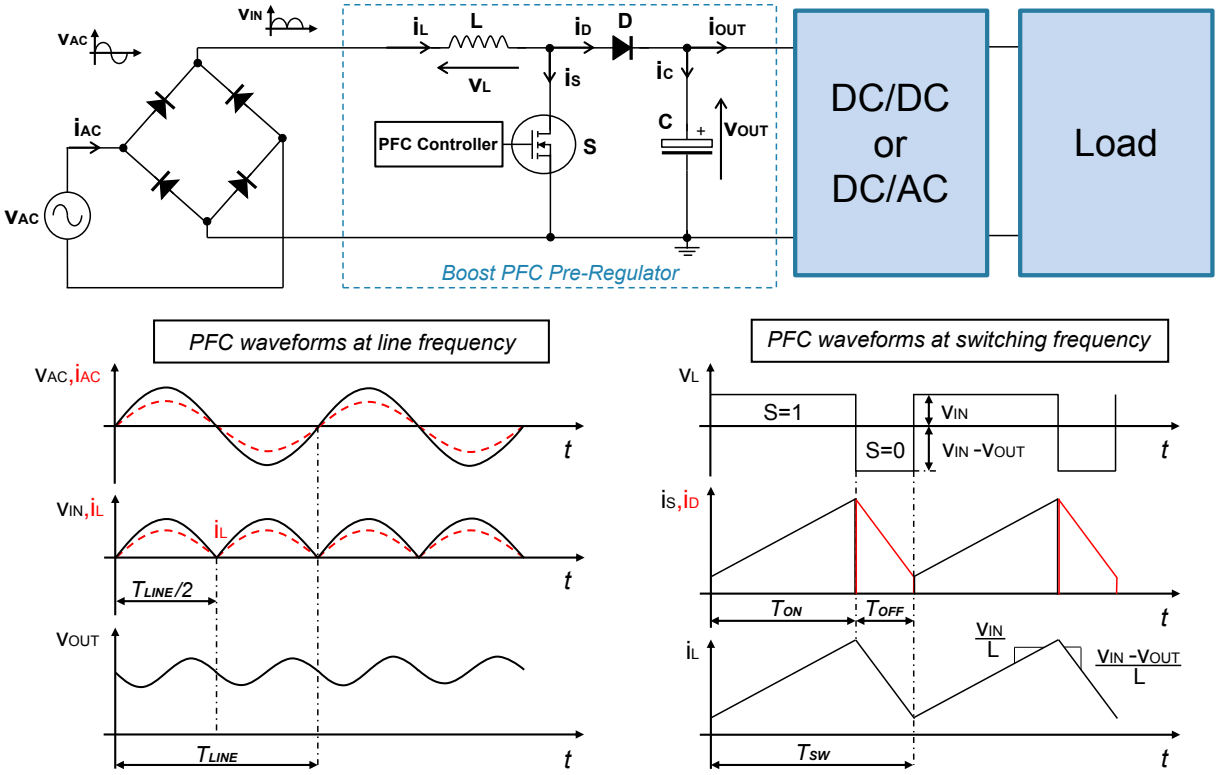
3.2 Active PFC

As boost circuits are relatively straightforward to design and drive, they are the preferred topology for implementing PFC's.

The boost PFC pre-regulator receives input from the bridge rectifier and delivers a constant DC output voltage (higher than the peak line voltage), while shaping input current at twice the line frequency.

A second conversion stage provides the appropriate voltage for a generic DC or AC load.

Figure 3. **PFC boost circuit and ideal waveforms**



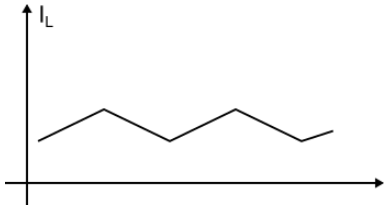
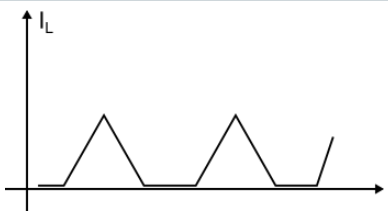
As shown in the above figure, the switching period (Tsw) can be divided into the following intervals:

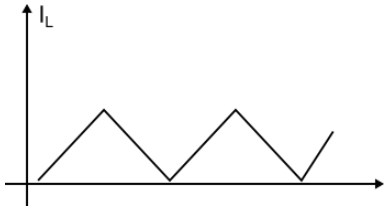
1. T_{ON} during which the inductor current increases linearly through a switch (S=1).
2. T_{OFF} after the switch is closed (S=0) and the inductor current flows through the boost diode towards the load.

The following operation modes are defined according to the level which the inductor current drops during T_{OFF}:

1. Continuous Conduction Mode (CCM)
2. Discontinuous Conduction Mode (DCM)
3. Critical Conduction Mode (CrM)

Table 1. **Boost operation modes**

Inductor current waveform	Operation Mode	Features
	Continuous Conduction Mode (CCM)	• Always hard-switching • Inductor value is largest • Minimal rms current
	Discontinuous Conduction Mode (DCM)	• Highest rms current • Reduce coil inductance • Best stability

Inductor current waveform	Operation Mode	Features
	Critical Conduction Mode (CrM)	• Largest rms current • Switching frequency is not fixed

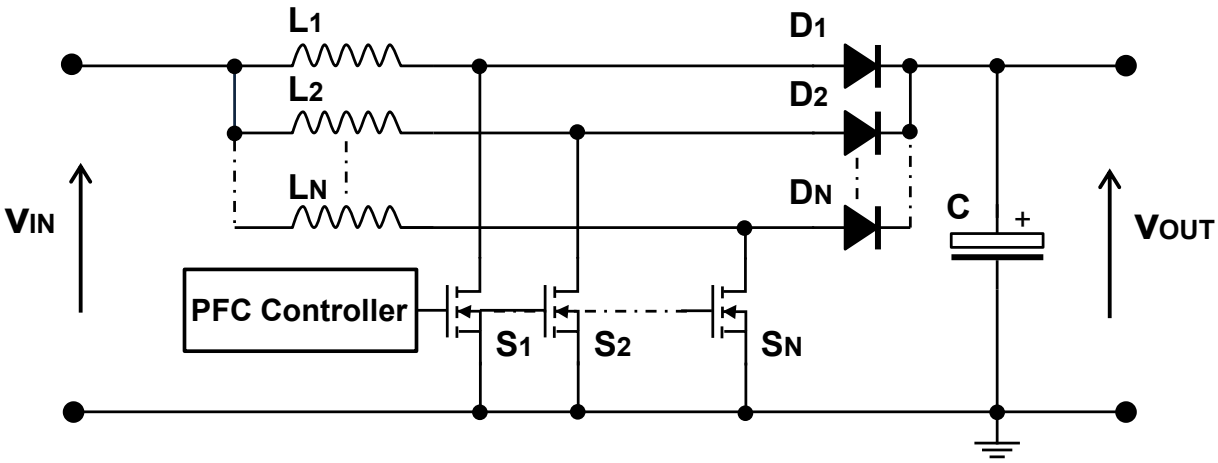
CCM is the preferred mode for high power PFC converters because it offers advantages like low input peak current (low turn-off switching losses), low input current THD and high power factor.

CCM generates high turn-on switching losses (hard switching), however, which is why parallel solutions are often preferable.

3.2.1 Interleaving

Interleaving consists of paralleling two or more small stages (channels) instead of one larger channel. The advantages of interleaving come at the expense of circuit simplicity, so this architecture is usually reserved for high power applications, above 600 W.

Figure 4. Interleaved boost circuit N-channel



During normal operation, the PWM driving signals are out of phase by the following amount:

$$phaseshift = \frac{360°}{number of channels} \quad (4)$$

The total power is shared among the parallel circuits.

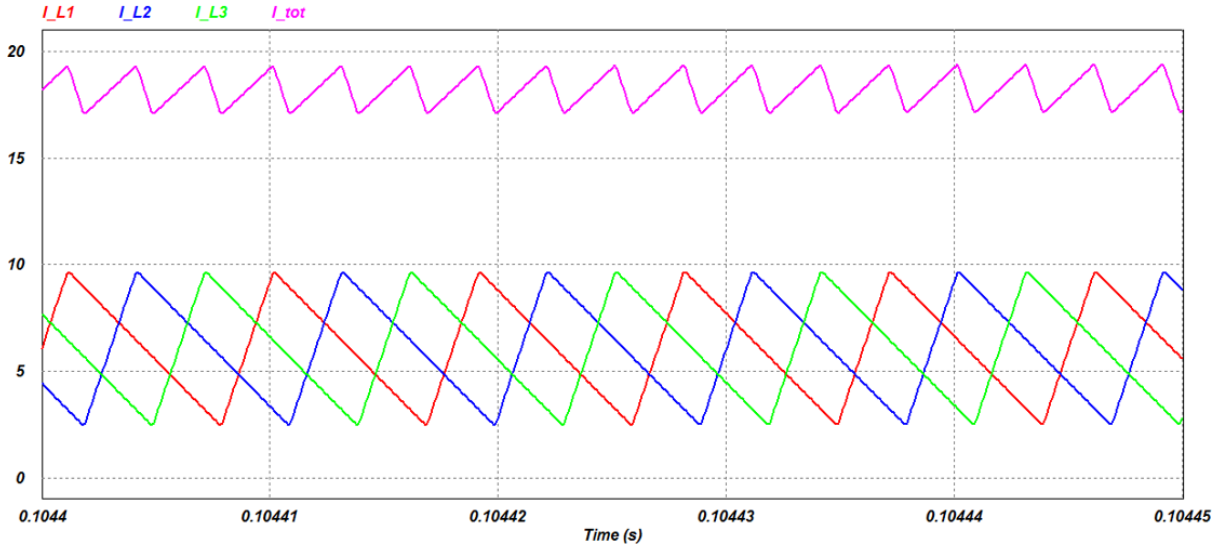
The interleaved topology has the following advantages over a traditional single-stage PFC:

- Input current ripple reduction
- EMI filter volume reduction
- Inductor volume reduction
- Output capacitor RMS current value reduction
- Better power management for the switches
- higher efficiency thanks to channel power management

Through interleaving, the equivalent inductor current ripple is reduced and completely eliminated for certain duty cycle values (e.g., at D=0.5 for two-channel boost; D=0.33 and D=0.66 for 3-channel PFC).

The EMI filter size can therefore be reduced thanks to the higher equivalent switching frequency.

Figure 5. **Channel inductor currents vs total current for 3-channel PFC**

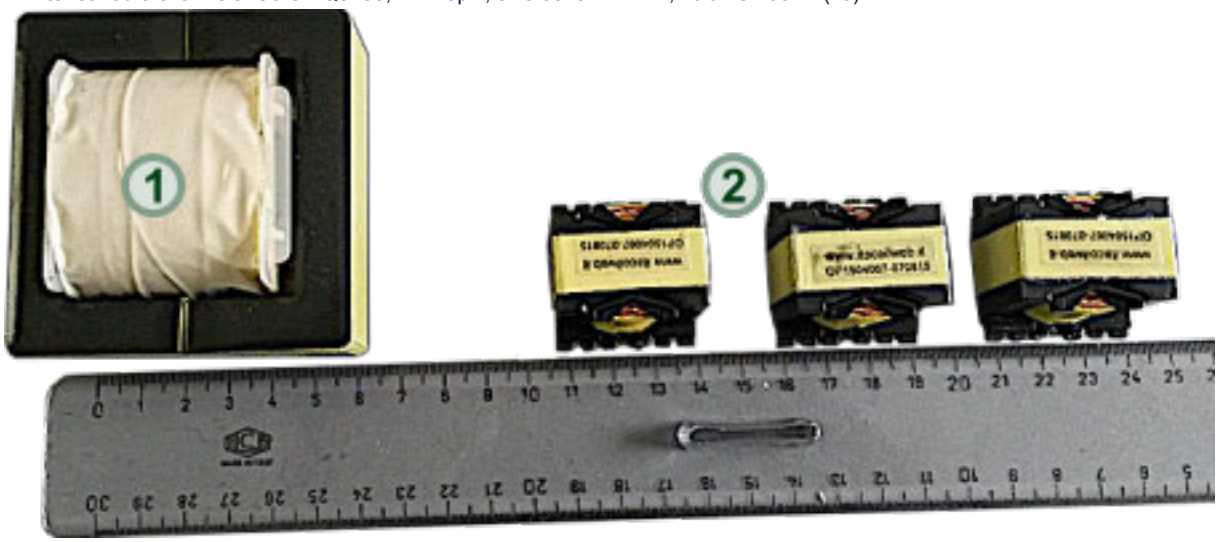


The following diagram shows the difference in inductor size for a single channel PFC with respect to a 3-channel interleaved solution. The 3-channel solution occupies over 40% less volume.

Figure 6. **Inductor volume comparison for 3 kW PFC**

Switching frequency = 100 KHz

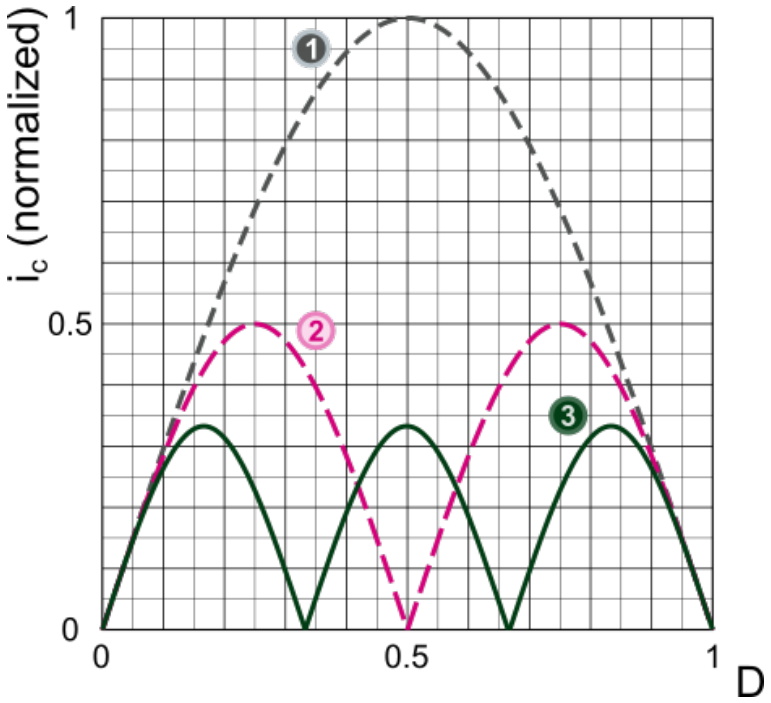
1. Single channel: Core EE70, L=150µH, size 70x66x31mm, volume 143cm^3
2. Interleaved 3 channels: Core PQ3230, L=120µH, size 30x32x27mm, volume 26cm^3 (x3)



Interleaving also allows a lower switching frequency than a single-channel PFC for the same power rating, which also helps improve efficiency. Moreover, the inductor current ripple reduction produces a reduced RMS output capacitor current, so capacitors with higher ESR (lower cost) can be used.

Figure 7. Output capacitor current ripple vs duty cycle

1. Single channel
2. Two channels
3. Three channels



Converter efficiency can also be improved by enabling or disabling the parallel channels depending on load percentage (phase shedding).

Even if interleaving leads to an increase in the number of switches, they are still smaller and less costly because the switches only manage a portion of total power. Interleaving also allows the distribution of power dissipation more evenly over the channels.

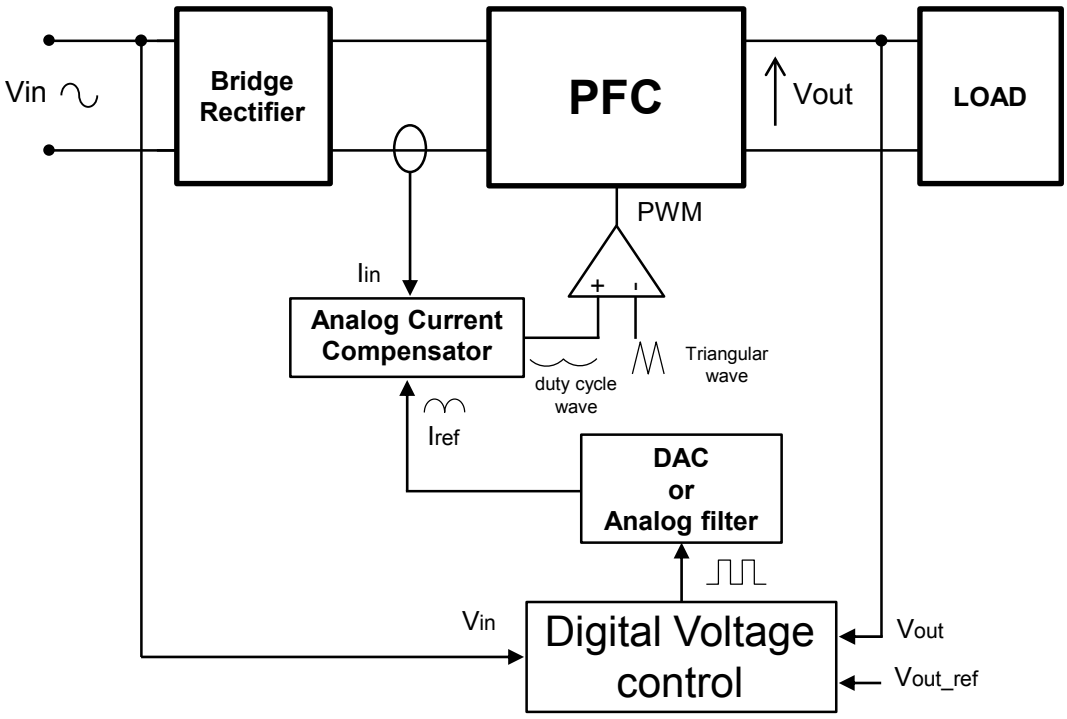
3.3 Mixed signal approach

Programmable digital solutions can provide adequate regulation across the entire input and output range of a power supply, which analog ICs alone often cannot deliver. Fully digital solutions, however, require high performance microcontrollers able to manage the high bandwidth of the current control loop.

A good compromise is mixed signal control, where:

- The current loop is managed by a hardware analog compensator, ensuring cycle by cycle regulation.
- The voltage loop is managed by a relatively low-cost digital controller, which provides output voltage regulation and non-time critical functions such as multiplier, feed-forward compensation, and undervoltage or overvoltage protection on the input and output voltages.

Figure 8. **Mixed signal block diagram**



For lower end controllers that do not include a DAC, the current reference can be generated through a PWM waveform, which is then filtered to become the sinusoidal reference (I_{ref}) for the current loop.

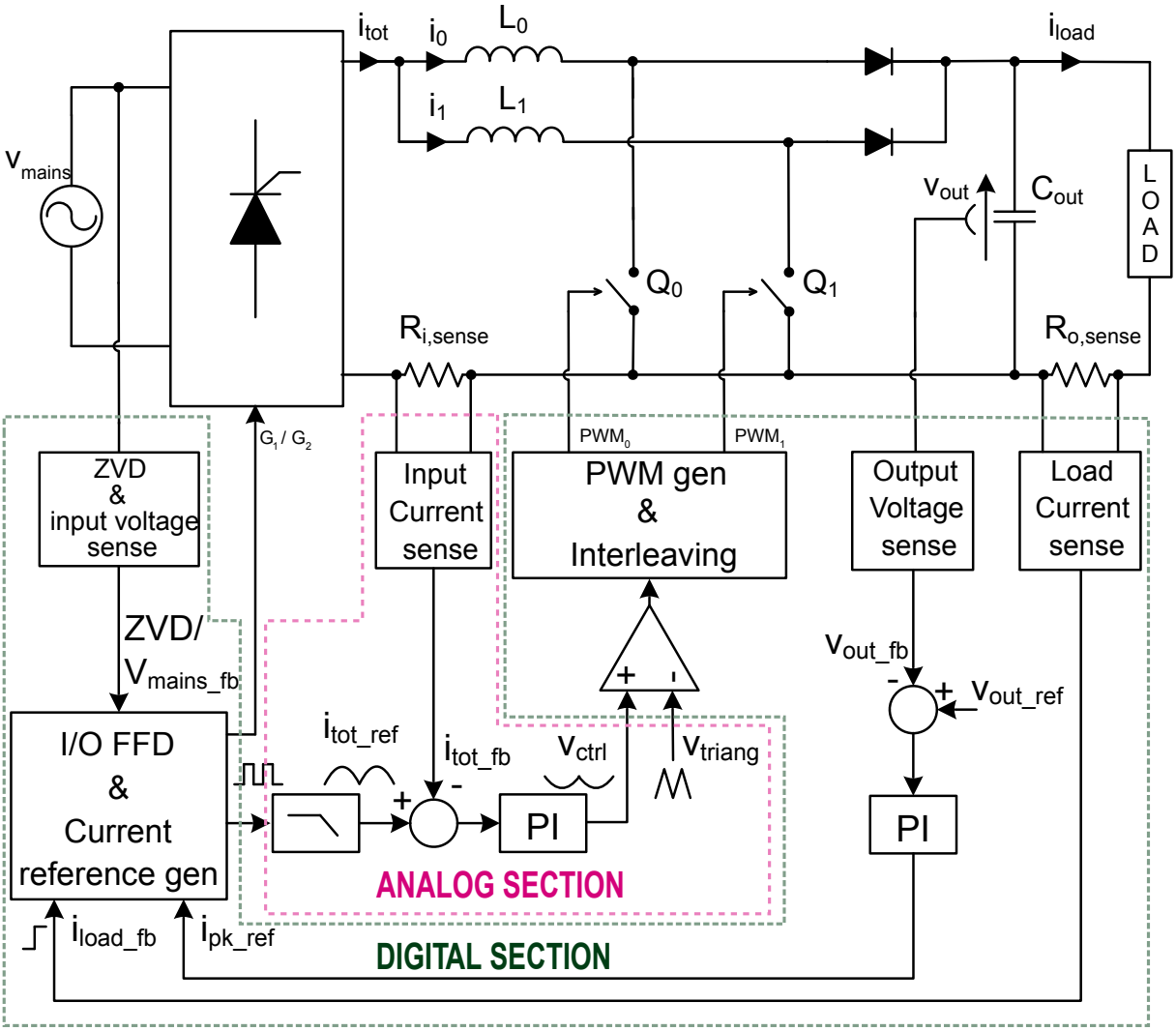
4 PFC control

The STNRGPF12 two-channel interleaved CCM PFC digital controller offers the advantages of a very high end digital solution without the typical limits of analog controllers.

The STNRGPF12 can drive a PFC in CCM at a fixed frequency, using mixed signal (analog/digital) Average Current Mode control (ACM) to deliver lower inductor ripple current, less EMI filtering, reduced RMS input current and operation at high power levels.

The following figure shows cascaded control of voltage and current loops, which determines the output voltage by regulating the total average inductor current.

Figure 9. STNRGPF12 mixed signal block scheme



This type of control is designed for fast transient responses to avoid large over and under-shoots on the output voltage when the mains voltage changes suddenly or a load current step occurs.

The system works in the following way:

1. The difference between output voltage feedback v_{out_fb} and reference v_{out_ref} is sent to a digital PI, which calculates the peak total input average current i_{pk_ref}.
2. The PFC current reference is internally generated and exits the I/O FFD block as a PWM waveform; after filtering it becomes the total average sinusoidal input current reference i_{tot_ref} for the inner current loop (analog section, red dashed line). The SCR driving signals are provided by the I/O FF block as well.

3. The difference between current reference i_{tot_ref} and input current feedback i_{tot_fb} is sent to an analog PI; the master PWM signal is generated by comparing the analog PI output v_{ctrl} and a triangular wave v_{triang} at switching frequency.
4. Finally, interleaving produces two 180° phase shifted PWM signals to drive the two power switches.

4.1 Converter modeling

The interleaved boost converter small-signal transfer functions are obtained through the following operations:

1. State-space averaging (SSA), used to average the converter behavior over a switching period, so the resulting small-signal model is only valid if the control loop bandwidth is suitably lower than the switching frequency.
2. Linearization with Taylor's series around an operating point.

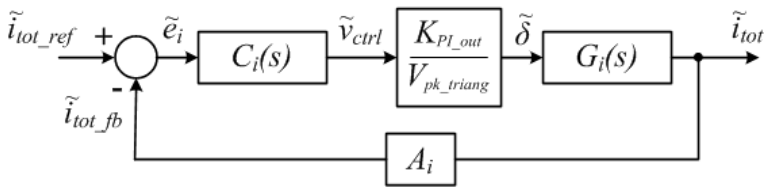
The small-signal transfer functions are useful to calculate the PI regulator parameters and satisfy bandwidth and phase margin specifications for control loops.

For the sake of simplicity, we shall assume that:

- The converter operates in CCM mode only.
- Active and passive components are ideal.
- The parallel boost inductors are identical and the total power is shared symmetrically across the channels.
- Perturbations on the main voltage are neglected and the voltage is assumed to be constant across several switching cycles.

4.2 Current loop design

Figure 10. Current loop block diagram



Note: In the following equations, the tilde (~) symbol above a letter indicates a small-signal variable, while uppercase letters refer to steady-state operating point variables.

The control-to-input current transfer function is:

$$G_i(s) = \frac{\tilde{i}_{tot}}{\tilde{\delta}} = \frac{C_{OUT}V_{OUT}^3 s + P_{OUT}\left(1+\frac{1}{\eta}\right)V_{OUT}}{C_{OUT}L_{PFC}V_{OUT}^2 s^2 + L_{PFC}P_{OUT}s + N_{ch}V_{IN}^2} \quad (5)$$

Where:

- $\tilde{i}_{tot}$ = small-signal total input average inductor current
- $\tilde{i}_{tot\_ref}$ = small-signal total input average current reference
- $\tilde{i}_{tot\_fb}$ = small-signal total input average inductor current sensing
- $\tilde{e}_i$ = small-signal current error
- $\tilde{v}_{ctrl}$ = small-signal control voltage (analog PI out)
- $\tilde{\delta}$ = small-signal duty cycle
- V_{pk_triang} = peak-to-peak voltage of triangular wave (carrier at switching frequency)
- K_{PI_out} = scale factor used to match PI maximum out voltage and V_{pk_triang} (resistive divider)
- V_{IN} = rms input voltage
- V_{OUT} = rms output voltage
- P_{OUT} = output power

- N_{ch} = number of channels
- L_{PFC} = single channel boost inductor
- C_{OUT} = output capacitor
- η = estimated efficiency
- A_i = Input current sensing gain
- $C_i(s)$ = Input current compensator transfer function

While this formula suggests that $G_i(s)$ depends on the number of channels and operating input voltage, the following figures show that they do not affect the Bode diagram behavior at high frequencies (current loop crossover frequency).

Figure 11. Control-to-input current TF vs main voltage V_{IN} (rms)

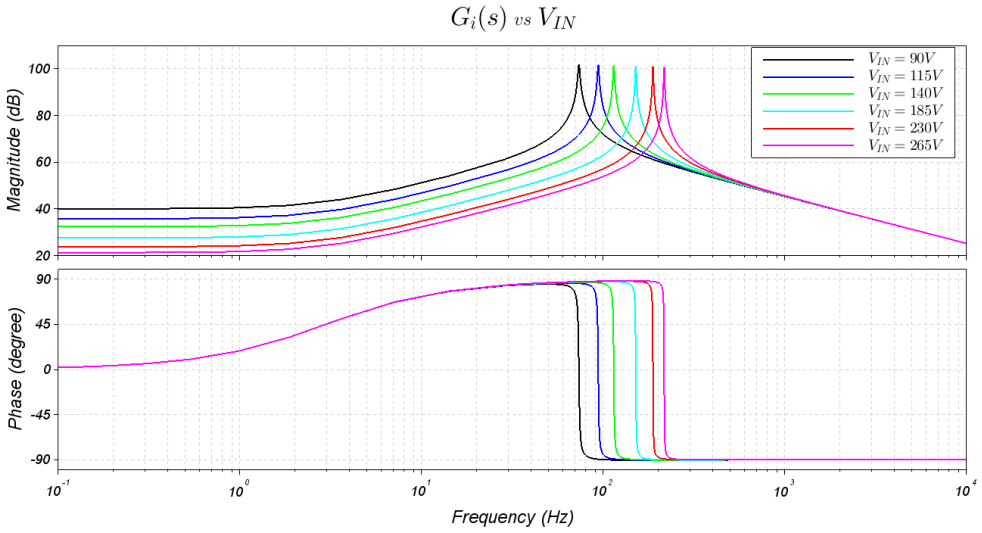
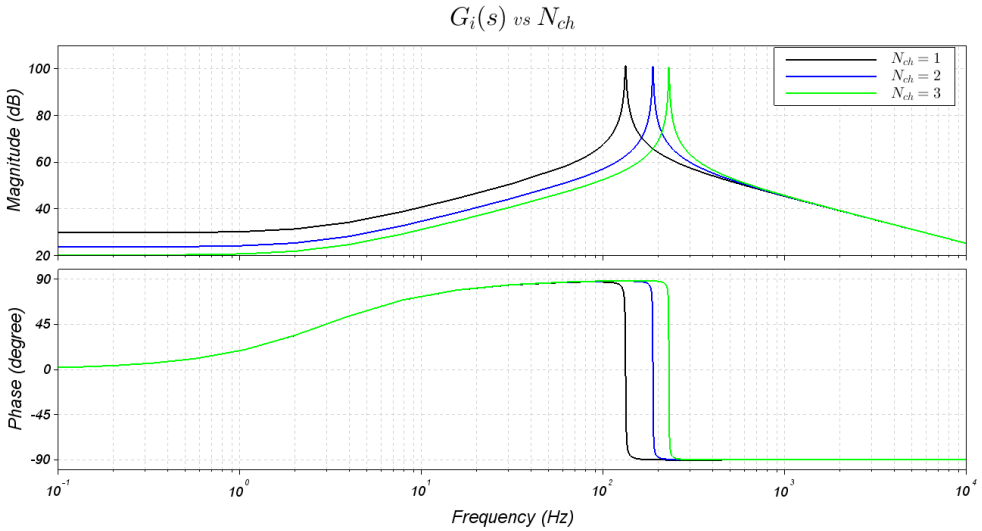


Figure 12. Control-to-input current TF vs Number of active channels N_{ch}



so $G_i(s)$ can be simplified as:

$$G_i(s) = \frac{\tilde{i}_{tot}}{\tilde{\delta}} \simeq \frac{V_{OUT}}{sL_{PFC}} \quad (6)$$

The typical PI compensator transfer function is:

$$C_i(s) = \frac{K_{P\_Itot}s + K_{I\_Itot}}{s} \quad (7)$$

with one pole at zero frequency $p_i = 0$ to reset the steady-state error and one zero $z_i = -\frac{K_{I\_Itot}}{K_{P\_Itot}}$ to achieve the desired phase margin at crossover frequency of the following open loop transfer function:

$$T_i(s) = C_i(s)L_i(s) \quad (8)$$

Where:

- $L_i(s) = \frac{K_{PI\_out}}{V_{pk\_triang}} A_i G_i(s)$

Based on general Bode criteria, the following equations ensure system stability for a desired bandwidth ω_{Ti_des} (crossover pulsation) and phase margin PM_{i_des}

$$\begin{cases} \left|T_i\left(j\omega_{Ti\_des}\right)\right| = 1 \\ \angle T_i\left(j\omega_{Ti\_des}\right) = -180° + PM_{i\_des} \end{cases} \quad (9)$$

Current loop crossover frequency $f_{Ti\_des} = \frac{\omega_{Ti\_des}}{2\pi}$ must be selected in the range:

$$f_{line} \ll f_{Ti\_des} \ll \frac{f_{sw}}{2} \quad (10)$$

Where:

- f_{line} = line voltage frequency
- f_{sw} = switching frequency

This relationship is necessary for good input current regulation and switching noise immunity. Crossover frequency and phase margin for current loop are typically selected as:

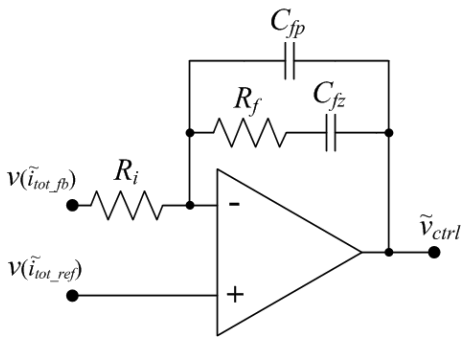
$$\begin{cases} f_{Ti_{des}} = 2 - 10kHz \\ PM_{i_{des}} = 45 - 60° \end{cases} \quad (11)$$

So the compensator parameters are calculated by:

$$\begin{cases} K_{I\_Itot} = \frac{\omega_{Ti\_des}}{\left|L_i\left(j\omega_{Ti\_des}\right)\right|\sqrt{1+\tan^2\left(PM_{i\_des} - 90° - \angle L_i\left(j\omega_{Ti\_des}\right)\right)}} \\ K_{P\_Itot} = \frac{K_{I\_Itot}\tan\left(PM_{i\_des} - 90° - \angle L_i\left(j\omega_{Ti\_des}\right)\right)}{\omega_{Ti\_des}} \end{cases} \quad (12)$$

As the current loop is performed in hardware, a PI Type II OP-AMP compensator is used:

Figure 13. PI Type II OP-AMP compensator



The transfer function is:

$$C_{i\_opamp}(s) = \frac{1}{(C_{fz}+C_{fp})R_i}\frac{C_{fz}R_f s+1}{s\left(\frac{C_{fz}C_{fp}R_f}{(C_{fz}+C_{fp})}s+1\right)} \quad (13)$$

the locations of the poles and zero are:

- $f_{pi0} = 0$
- $f_{pi1} = \frac{(C_{fz}+C_{fp})}{2\pi C_{fz}C_{fp}R_f} \approx \frac{1}{2\pi C_{fp}R_f}$
- $f_{zi1} = \frac{1}{2\pi C_{fz}R_f}$

Comparing Eq. (7) with Eq. (13), an additional high-frequency pole appears in Eq. (13). It is given by capacitor C_{fp} and is usually set to between half and one of the switching frequency to attenuate switching noise without interfering with current loop regulation:

$$\begin{cases} C_{fp} \ll C_{fz} \\ \frac{f_{sw}}{2} \le f_{pi1} \le f_{sw} \end{cases} \quad (14)$$

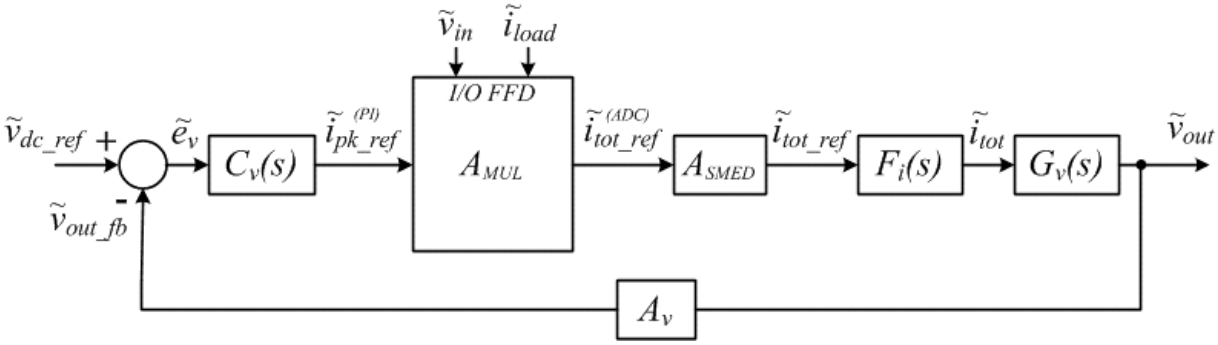
Proportional and integral gain of the compensator determines the passive network design:

$$\begin{cases} R_i = \frac{1}{C_{fz}K_{I\_Itot}} \\ R_f = R_i K_{P\_Itot} \\ C_{fp} = \frac{1}{2\pi f_{pi1}R_f} \end{cases} \quad (15)$$

As we need to calculate four components from three equations, capacitor C_{fz} must be set. Due to the high-frequency pole, the actual phase margin decreases a few degrees (with respect to a simple PI compensator), which is compensated by using a slightly larger phase margin.

4.3 Voltage loop design

Figure 14. Complete control loop block diagram



Note: In the following equations, the tilde (~) symbol above a letter indicates a small-signal variable, while uppercase letters refer to steady-state operating point variables.

The control-to-output voltage transfer function is:

$$H_v(s) = \frac{\tilde{v}_{out}}{\tilde{\delta}} = \frac{2\left(N_{ch}V_{IN} - \frac{P_{OUT}}{\eta V_{IN}}L_{PFC}s\right)V_{OUT}^2}{C_{OUT}L_{PFC}V_{OUT}^2 s^2 + L_{PFC}P_{OUT}s + N_{ch}V_{IN}^2} \quad (16)$$

But in this case, it is useful to exploit the input current-to-output voltage transfer function:

$$G_v(s) = \frac{\tilde{v}_{out}}{\tilde{i}_{tot}} = \frac{\tilde{v}_{out}}{\tilde{\delta}}\frac{\tilde{\delta}}{\tilde{i}_{tot}} = \frac{2\left(N_{ch}V_{IN} - \frac{P_{OUT}}{\eta V_{IN}}L_{PFC}s\right)V_{OUT}^2}{C_{OUT}V_{OUT}^3 s + P_{OUT}\left(1+\frac{1}{\eta}\right)V_{OUT}} \quad (17)$$

Where:

- $\tilde{v}_{out}$ = small-signal output voltage
- $\tilde{v}_{out\_fb}$ = small-signal output voltage sense
- $\tilde{v}_{dc\_ref}$ = small-signal output voltage reference
- $\tilde{v}_{in}$ = small-signal input voltage sense
- $\tilde{i}_{load}$ = small-signal load current sense
- $\tilde{e}_v$ = small-signal voltage error
- $\tilde{i}_{pk\_ref}^{(PI)}$ = small-signal PI peak current reference
- $\tilde{i}_{tot\_ref}^{(ADC)}$ = small-signal digital sinusoidal current reference
- $F_i(s)$ = Input current closed-loop transfer function
- $C_v(s)$ = Output voltage compensator transfer function
- A_{MUL} = Digital multiplier gain for digital current reference generation
- A_{SMED} = Digital to analog gain for analog current reference generation
- A_v = Output voltage sensing gain

Since the voltage loop crossover frequency is generally selected in the 5-15 Hz range, the right half plane zero (higher frequencies > 20 kHz) can be neglected.

The I/O FFD is currently seen as a constant gain (A_{MUL}). The output voltage loop regulation is performed by a digital PI:

$$C_v(s) = \frac{K_{P\_Vdc}s + K_{I\_Vdc}}{s} \tag{18}$$

so the PI parameter calculations can be performed by using the same procedure as in current loop design. Starting from system specifics:

$$\begin{cases} f_{Ti\_des} = 5 - 15Hz \\ PM_{i\_des} = 45 - 60° \end{cases} \tag{19}$$

The design equations are:

$$\begin{cases} \left|T_v(j\omega_{Tv\_des})\right| = 1 \\ \angle T_v(j\omega_{Tv\_des}) = -180° + PM_{v\_des} \end{cases} \tag{20}$$

Where:

- $T_v(s) = C_v(s)L_v(s)$
- $L_v(s) = A_{MUL}A_{SMED}F_iG_v(s)A_v$

Hence, the compensator parameters are:

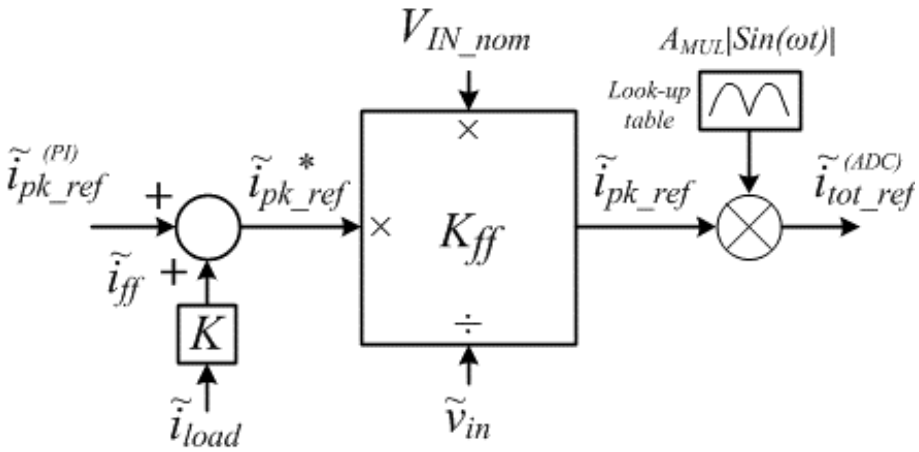
$$\begin{cases} K_{I\_Vdc} = \dfrac{\omega_{Tv\_des}}{\left|L_i(j\omega_{Tv\_des})\right|\sqrt{1+\tan^2\left(PM_{v\_des} - 90° - \angle L_v(j\omega_{Tv\_des})\right)}} \\ K_{P\_Vdc} = \dfrac{K_{I\_Vdc}\tan\left(PM_{v\_des} - 90° - \angle L_v(j\omega_{Tv\_des})\right)}{\omega_{Tv\_des}} \end{cases} \tag{21}$$

4.4 I/O feed-forward and current reference generation

When the main voltage or load current changes suddenly, the low bandwidth of the voltage loop may cause output voltage fluctuations.

To counter this effect, the I/O FFD block performs two feed-forwards to reduce the system transient response time.

Figure 15. **I/O FFD block**



Note: In the following equations, the tilde (~) symbol above a letter indicates a small-signal variable, while uppercase letters refer to steady-state operating point variables.

The first feed-forward is a load feed-forward that adds a portion of the load current $\tilde{i}_{ff}$ to the PI output, which helps to rapidly change the peak current reference $\tilde{i}^{*}_{pk\_ref}$ when a load step occurs.

$$\tilde{i}^{*}_{pk\_ref} = \tilde{i}^{(PI)}_{pk\_ref} + \tilde{i}_{ff} \tag{22}$$

For the second feed-forward, $\tilde{i}^{*}_{pk\_ref}$ is multiplied by coefficient K_{ff} to factor in input voltage fluctuations:

$$\tilde{i}_{pk\_ref} = \frac{\tilde{i}^{*}_{pk\_ref}}{\frac{\tilde{v}_{in}}{V_{IN\_nom}}} = \tilde{i}^{*}_{pk\_ref} K_{ff} \tag{23}$$

From the above equation, it is clear that an increase in rms input voltage causes a decrease in $\tilde{i}_{pk\_ref}$ and vice versa, so the output voltage is maintained relatively constant.

A pseudo-sinusoidal shaped current reference is obtained by multiplying $\tilde{i}_{pk\_ref}$ for a look-up table:

$$\tilde{i}^{(ADC)}_{tot\_ref} = \tilde{i}_{pk\_ref} A_{MUL} |\sin(\omega t)| \tag{24}$$

and for Digital to Analog gain:

$$\tilde{i}^{(ANALOG)}_{tot\_ref} = \tilde{i}^{(ADC)}_{tot\_ref} A_{SMED} \tag{25}$$

The current reference is a PWM signal that must be filtered with appropriate hardware to generate the reference for analog current loop.

4.5 Control design example

Typical design parameters for a 2 kW power rating are shown in the following table.

Table 2. **Power stage, sensing and current loop parameters**

Design parameter	Description	Value
P_{OUT}	output power	2 kW
N_{ch}	Number of channels	2
V_{IN}	rms nominal input voltage	230 V
V_{OUT}	rms nominal output voltage	400 V
f	line frequency	50 Hz
η	estimated efficiency	97 %

Design parameter	Description	Value
L_{PFC}	single channel boost inductor	350 µH
C_{OUT}	output capacitor	2x680 µF
V_{pk_triang}	peak-to-peak voltage of triangular wave	2 V
K_{PI_out}	PI out scale factor	0.4054
A_i	Input current sensing gain	0.2236
A_v	Output voltage sensing gain	1.9109
A_{MUL}	Digital multiplier gain	3.3086
A_{SMED}	Digital to analog gain	0.001042
f_{sw}	Switching frequency	60 kHz
f_{Ti_des}	Current loop crossover frequency	7.5 kHz
f_{Tv_des}	Voltage loop crossover frequency	10 Hz
PM_{i_des}	Current loop phase margin	60°
PM_{v_des}	Voltage loop phase margin	60°
f_{PI_ctrl}	Voltage loop control frequency	1 kHz

Using the values in the above table, the compensator parameters in Eq. (12) are calculated as:

$$\begin{cases} K_{I\_Itot} = 21411 \\ K_{P\_Itot} = 0.7873 \end{cases} \quad (26)$$

For a zero capacitor $C_{fz} = 8.2nF$, the input PI resistor is:

$$R_i = \frac{1}{C_{fz} K_{I\_Itot}} = \frac{1}{8.2 \cdot 10^{-9} \cdot 21411} = 5696\Omega \quad (27)$$

So a commercial 5.6 kΩ resistor is appropriate.
The feedback resistor value is given by:

$$R_f = R_i K_{P\_Itot} = 5696 \cdot 0.7873 = 4484\Omega \quad (28)$$

So a commercial 4.3 kΩ resistor is appropriate.

Finally, the high-frequency pole capacitor $f_{pi1} = \frac{3 \cdot f_{sw}}{4}$ is calculated with:

$$C_{fp} = \frac{1}{2\pi f_{pi1} R_f} = \frac{1}{2\pi \cdot 45 \cdot 10^3 \cdot 4484} = 0.7887nF \quad (29)$$

So an 820 pF capacitor is appropriate.

Figure 16. **Current compensator $C_i(s)$ Bode diagram**

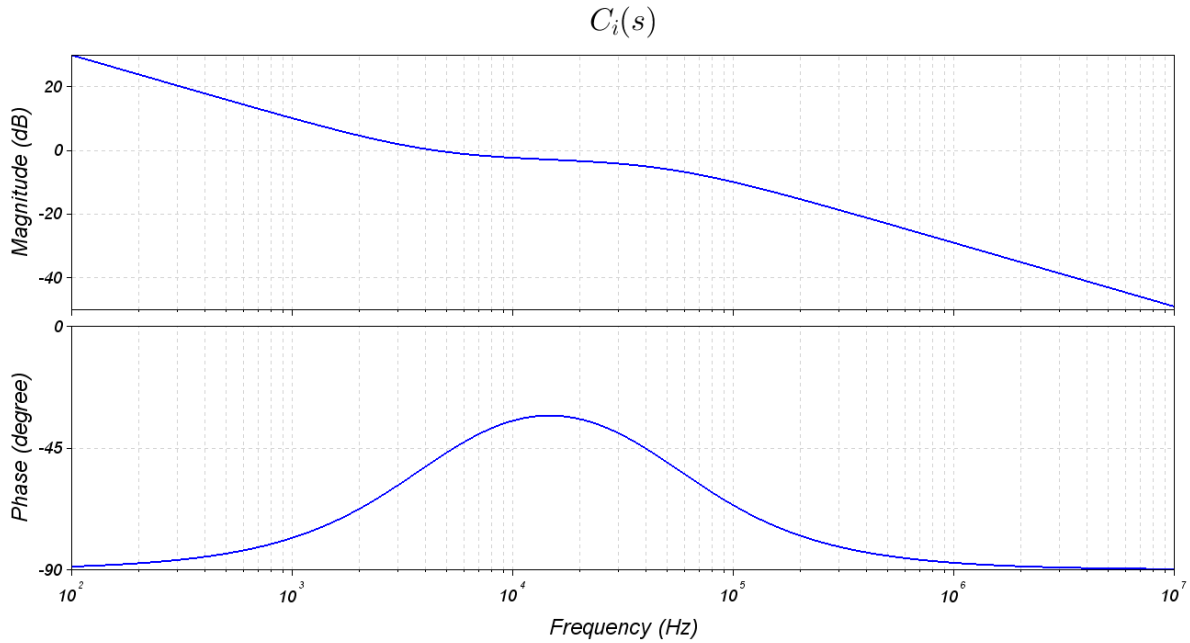
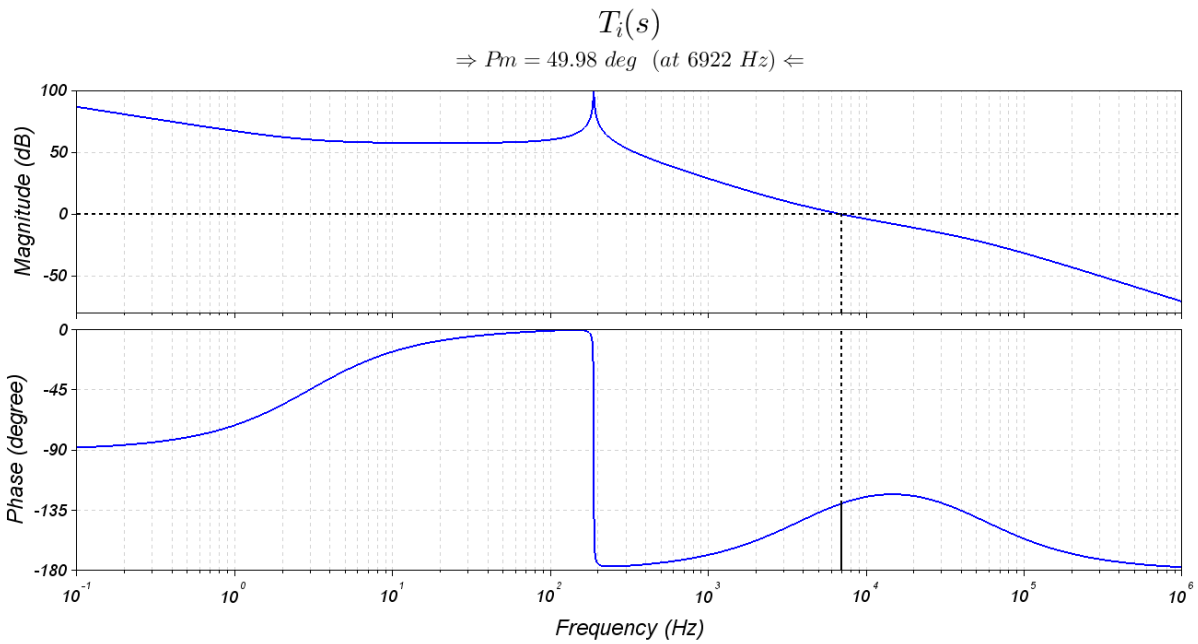


Figure 17. **Current open loop transfer function $T_i(s)$ Bode diagram**



The voltage loop compensator parameters in Eq. (21) can also be calculated:

$$\begin{cases} K_{I\_Vdc}{}^* = 59.8985 \\ K_{P\_Vdc} = 0.9065 \end{cases} \tag{30}$$

Note that the integral gain $K_{I\_Vdc}{}^*$ cannot be directly used in the firmware calculation routine, but must be divided by the operation frequency of the digital PI, hence:

$$K_{I\_Vdc} = \frac{K_{I\_Vdc}{}^*}{f_{PI_{ctrl}}} = \frac{59.8985}{1000} = 0.0598985 \tag{31}$$

Figure 18. **Voltage compensator $C_V(s)$ Bode diagram**

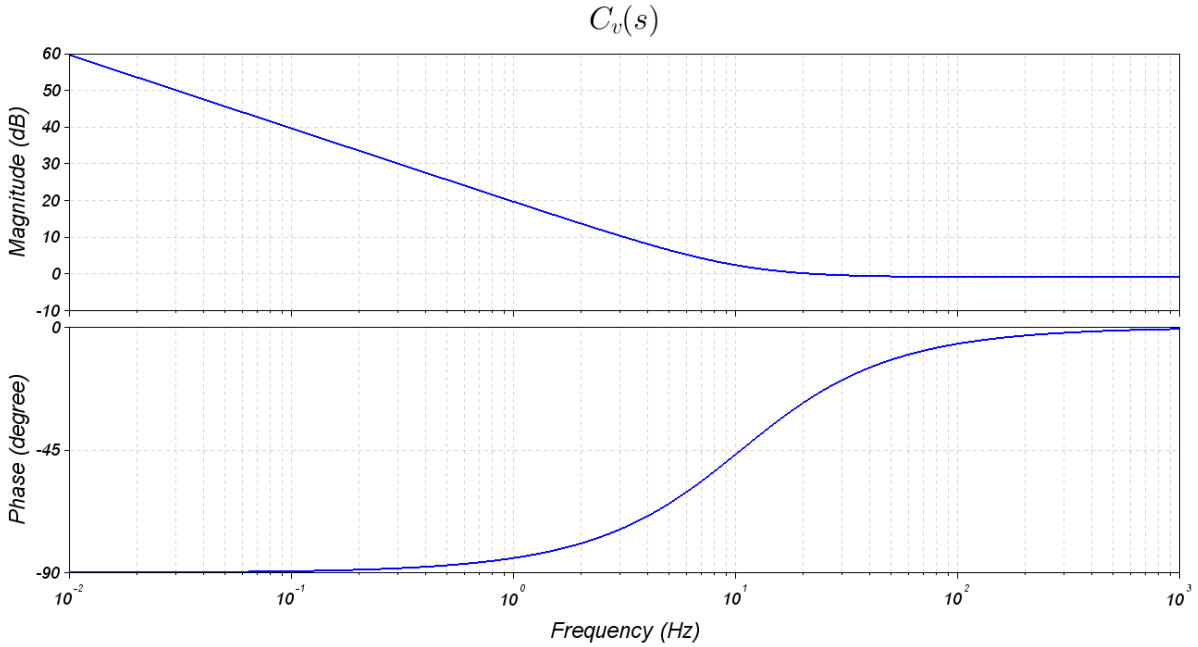
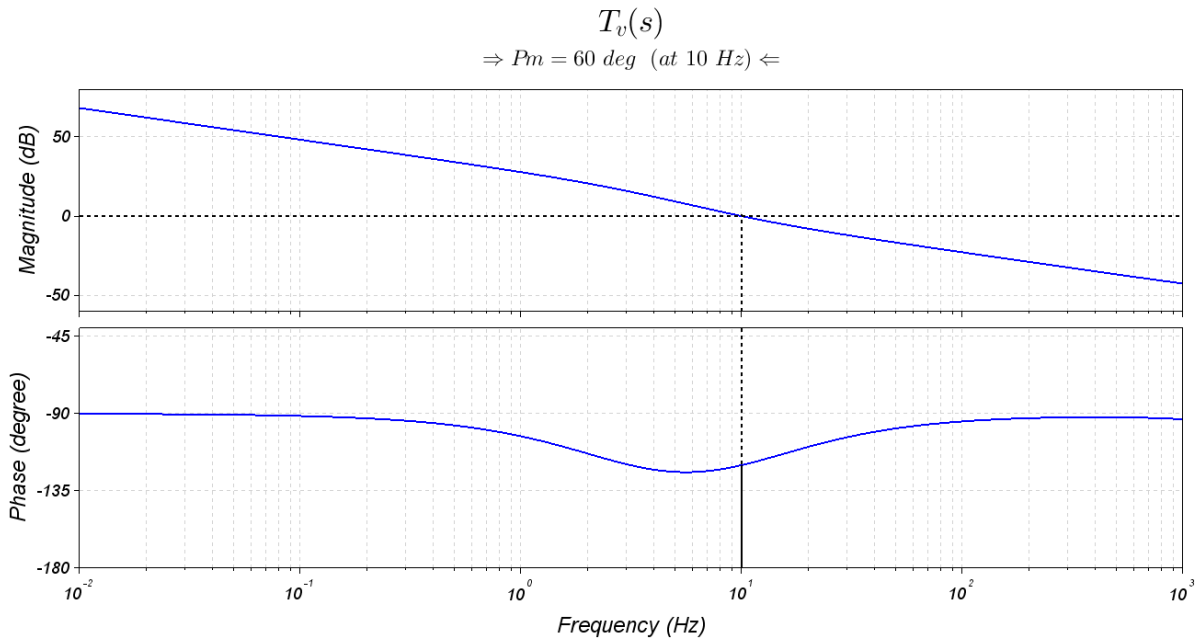


Figure 19. **Voltage open loop transfer function $T_V(s)$ Bode diagram**



5 Power stage design equations

5.1 Mixed input bridge

The mixed input bridge (two high-side rectifier SCRs plus two low-side diodes) selection is based on maximum average and RMS input currents:

$$I_{IN\_rms(MAX)} = \frac{P_{OUT}}{\eta \cdot V_{IN\_rms(MIN)} \cdot PF} = \frac{2000}{0.97 \cdot 185 \cdot 0.99} = 11.25\ A \quad (32)$$

$$I_{IN\_avg(MAX)} = \frac{2\sqrt{2}}{\pi} I_{IN\_rms(MAX)} = 10.13\ A \quad (33)$$

Where:

- $I_{IN\_rms(MAX)}$ = maximum input current (rms)
- $I_{IN\_avg(MAX)}$ = maximum average input current
- $V_{IN\_rms(MIN)}$ = minimum input voltage (rms)
- P_{OUT} = output power
- η = PFC efficiency
- PF = power factor

The STBR3012WY and associated TN3050H-12WY SCR have been selected. This pair of 1200 V devices are particularly suitable for input bridges, thanks to their low forward voltage drop and surge current/voltage handling capability: a higher current rated bridge device usually experiences a lower voltage drop, which helps reduce bridge power losses. Moreover, they can be used in place of resistor and relay pair for inrush current limiting in automotive applications, where mechanical reliability is an issue due to vibrations that can damage relays.

Power dissipation for the STBR3012WY and TN3050H-12WY are calculated in the same way from the datasheet values:

$$P_{BRIDGE\_diode} = 0.96 \cdot I_{IN\_avg(MAX)} + 0.008 \cdot I^2_{IM\_rms(MAX)} = 0.96 \cdot 10.13 + 0.008 \cdot 11.25^2 = 10.74W \quad (34)$$

$$P_{BRIDGE\_scr} = V_{TO} \cdot I_{IN\_avg(MAX)} + R_D \cdot I^2_{IN\_rms(MAX)} = 0.88 \cdot 10.13 + 0.014 \cdot 11.25^2 = 10.68\ W \quad (35)$$

Where:

- V_{TO} = threshold voltage of TN3050H-12WY (at T_j = 150 °C)
- R_D = dynamic resistance of TN3050H-12WY (at T_j = 150 °C)

So the total power loss of mixed input bridge is:

$$P_{BRIDGE\_tot} = P_{BRIDGE\_diode} + P_{BRIDGE\_scr} = 10.74 + 10.68 = 21.4\ W \quad (36)$$

RELATED LINKS

Search www.st.com for AN4606: "Inrush-current limiter circuits (ICL) with Triacs and Thyristors (SCR) and controlled bridge design tips"

Search www.st.com for UM2076: "Getting started with the STEVAL-ISF003V1" (section 8: SCR switch insulated control)

5.2 Input capacitor

The input capacitor must filter high frequency ripple in the input current. A polypropylene film capacitor rated for maximum input voltage is recommended.

The calculation formula is:

$$C_{in} = \frac{\frac{k_r}{N_{ch}} \cdot I_{IN\_rms(MAX)}}{2\pi \cdot f_{sw} \cdot r \cdot V_{IN\_rms(MIN)}} = = \frac{\frac{0.55}{2} \cdot 11.25}{2\pi \cdot 60 \cdot 10^3 \cdot 0.05 \cdot 185} = 887\ nF \quad (37)$$

Where:

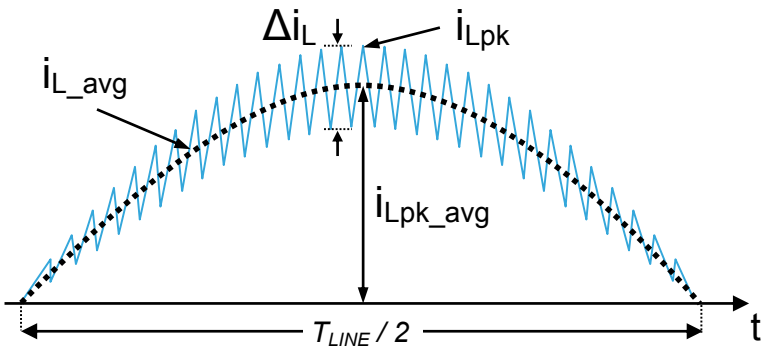
- k_r = inductor current ripple factor
- r = maximum high frequency voltage ripple factor ($\Delta V_{IN}/V_{IN}$ = 2-10%)
- f_{sw} = switching frequency
- N_{ch} = number of interleaved channels

A commercially available 1 µF input capacitor is used.

5.3 Boost inductor

The boost inductor is designed to work in CCM.

Figure 20. Average inductor current



The duty cycle and maximum average inductor current are evaluated at the minimum line voltage for the rated output power:

$$I_{Lpk\_avg} = \frac{\sqrt{2} \cdot \frac{P_{OUT}}{\eta \cdot N_{ch}}}{V_{IN\_rms(MIN)}} = \frac{\sqrt{2} \cdot \frac{2000}{0.97 \cdot 2}}{185} = 7.88\ A \quad (38)$$

$$D = \frac{V_{OUT} - \sqrt{2} \cdot V_{IN\_rms(MIN)}}{V_{OUT}} = \frac{400 - \sqrt{2} \cdot 185}{400} = 0.346 \quad (39)$$

Where:

- V_{OUT} = nominal output voltage.

So, once the maximum allowable ripple (k_r) is set, the boost inductor for each channel can be calculated as:

$$L_{PFC} = \frac{\sqrt{2} \cdot V_{IN\_rms(MIN)} \cdot D}{f_{sw} \cdot k_r \cdot I_{Lpk\_avg}} = \frac{\sqrt{2} \cdot 185 \cdot 0.346}{60 \cdot 10^3 \cdot 0.55 \cdot 7.88} = 348\ \mu H \quad (40)$$

$$I_{Lpk} = I_{Lpk\_avg} \cdot \left(1 + \frac{k_r}{2}\right) = 7.88 \cdot \left(1 + \frac{0.55}{2}\right) = 10\ A \quad (41)$$

Hence, the saturation current must be greater than 10 A (typical inductor value tolerance is ±10%).

5.4 Power switch

The power switch (MOSFET or IGBT) is selected for minimal power losses. The maximum switch current is evaluated at minimum line voltage (worst case):

$$I_{sw\_rms} = \frac{P_{OUT}/N_{ch}}{V_{IN\_rms(MIN)} \cdot \sqrt{2}} \sqrt{2 - \frac{16 \cdot V_{IN\_rms(MIN)} \cdot \sqrt{2}}{3 \cdot \pi \cdot V_{OUT}}} \quad (42)$$

$$= \frac{2000/2}{185 \cdot \sqrt{2}} \sqrt{2 - \frac{16 \cdot 185 \cdot \sqrt{2}}{3 \cdot \pi \cdot 400}} = 3.6\ A$$

5.4.1 IGBT

The STGW20H65FB of the HB IGBT series is used as boost switch. The device is based on an advanced proprietary trench gate field-stop structure and features a low conduction loss thanks to a low $V_{CE(sat)}$ and high switching speed thanks to a minimized tail current profile.

The device datasheet provides the necessary values to perform loss calculations.

Conduction losses (V_{CEsat_rms} = 0.988 V, obtained graphically from output characteristics):

$$P_{S\_cond} = V_{CEsat\_rms} \cdot I_{sw\_rms} = 0.988 \cdot 3.6 = 3.56\,W \quad (43)$$

Where:

- V_{CEsat_rms} = Collector-emitter saturation voltage at T_j=125 °C and I_c=I_{sw_rms}

Switching losses (calculated using E_{on} and E_{off} from switching energy vs collector current behavior):

$$P_{S\_sw} = \left(E_{on\_rms} + E_{off\_rms}\right) \cdot f_{sw} = \left(18.56 \cdot 10^{-6} + 50.92 \cdot 10^{-6}\right) \cdot 60 \cdot 10^{3} = 4.17\,W \quad (44)$$

Where:

- E_{on_rms} = On-switching energy at T_j = 125 °C and I_c=I_{sw_rms}
- E_{off_rms} = Off-switching energy at T_j = 125 °C and I_c=I_{sw_rms}

Total IGBT power loss:

The total power loss is the sum of each specific loss multiplied by the number of interleaved channels:

$$P_{S\_tot} = \left(P_{S\_cond} + P_{S\_sw}\right) \cdot N_{ch} = (3.56 + 4.17) \cdot 2 = 15.46W \quad (45)$$

5.5 Boost diode

Like the power switch, appropriate boost diode selection is critical for PFC operation in CCM at high frequencies, in order to minimize the power losses.

The STPSC12065 650 V power Schottky silicon carbide diode offers fast recovery with negligible reverse recovery charge (Qrr) and the minimal capacitive turn-off behavior is independent of temperature.

The average and rms diode currents are calculated from the maximum output power and minimum input voltage, after which the conduction and switching losses can be determined.

$$I_{D\_avg} = \frac{P_{OUT}/N_{ch}}{V_{OUT}} = \frac{2000/2}{400} = 2.5A$$

$$I_{D\_rms} = \frac{P_{OUT}/N_{ch}}{V_{IN\_rms(MIN)} \cdot \sqrt{2}} \sqrt{\frac{16 \cdot V_{IN\_rms(MIN)} \cdot \sqrt{2}}{3 \cdot \pi \cdot V_{OUT}}} = \frac{2000/2}{185 \cdot \sqrt{2}} \sqrt{\frac{16 \cdot 185 \cdot \sqrt{2}}{3 \cdot \pi \cdot 400}} = 4A$$

Conduction losses:

$$P_{D\_cond} = V_{th} \cdot I_{D\_avg} + R_d \cdot I_{D\_rms}^2 = 1.02 \cdot 2.5 + 0.065 \cdot 4^2 = 3.6\,W \quad (46)$$

Where:

- V_{th} = diode threshold voltage
- R_d = diode differential resistance

Switching losses:

$$P_{D\_sw} = 0.5 \cdot V_{OUT} \cdot Q_{Cj} \cdot f_{sw} = 0.5 \cdot 400 \cdot 36 \cdot 10^{-9} \cdot 60 \cdot 10^{3} = 0.43\,W \quad (47)$$

Where:

- Q_{Cj} = total capacitive charge

Total diode power loss:

$$P_{D\_tot} = \left(P_{D\_cond} + P_{D\_sw}\right) \cdot N_{ch} = (3.6 + 0.43) \cdot 3 = 8.1\,W \quad (48)$$

5.6 Output capacitor

One of the factors for determining the output capacitor is the PFC output voltage ripple at twice the line frequency:

$$C_{OUT\_R} \geq \frac{P_{OUT}}{2\pi \cdot f \cdot \Delta V_{OUT} \cdot V_{OUT}} = \frac{2000}{2\pi \cdot 47 \cdot 20 \cdot 400} = 846\mu F \quad (49)$$

Where:

- ΔV_{OUT} = output voltage ripple target
- f = minimum line frequency

Another factor is the PFC output voltage after a line interruption of a certain duration (hold-up time):

$$C_{OUT\_H} \geq \frac{2 \cdot P_{OUT} \cdot t_{hold\_up}}{\left(V_{OUT} - \frac{\Delta V_{OUT}}{2}\right)^2 - V_{OUT(MIN)}^2} = \frac{2 \cdot 2000 \cdot 20 \cdot 10^{-3}}{\left(400 - \frac{20}{2}\right)^2 - 300^2} = 1288\mu F \quad (50)$$

Where:

- $V_{OUT(MIN)}$ = minimum allowable output voltage after a line interruption
- t_{hold_up} = hold-up time

We select the larger of the two factors:

$$C_{OUT} \geq \max\left(C_{OUT\_R}, C_{OUT\_H}\right) = 1288\mu F \quad (51)$$

So 2 parallel 680 µF capacitors would normally be selected.

However, when $C_{OUT\_H} > C_{OUT\_R}$, the actual ripple may be much lower than the target.

Therefore, to avoid capacitor oversizing and ensure both factors are satisfied, the target ΔV_{OUT} can be progressively decreased (through iteration) until $C_{OUT\_R} = C_{OUT\_H}$.

The result is:

$$\begin{cases} \Delta V_{OUT} = 12.9V \\ C_{OUT\_R} = C_{OUT\_H} = 1238\mu F \end{cases} \quad (52)$$

So 2 parallel 680 µF capacitors is confirmed.

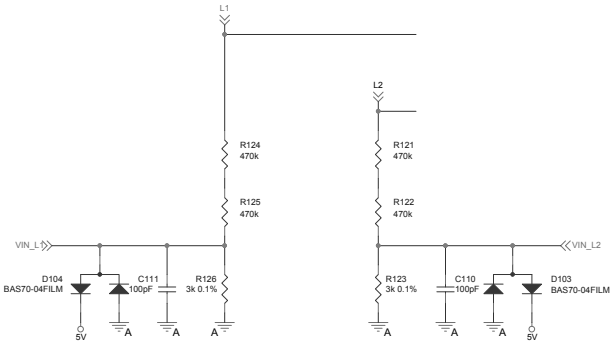
6 Sensing design

Sensing circuits must be designed with appropriate voltage, power rating and tolerance selections, as well as bandwidth and slew rates when using OP-AMP circuits.

6.1 Input voltage sensing

Two voltage dividers are used to sense the line and neutral input voltages for an internal differential measurement.

Figure 21. Input voltage sensing



V_{IN_L1} is obtained from the equation:

$$V_{IN\_L1} = V_{L1\_pk}\frac{R_{126}}{R_{124}+R_{125}+R_{126}} \quad (53)$$

The maximum peak of the sensed voltage must not exceed 1.25 V so, if we set R124 and R125 to 470 kΩ, R126 can be calculated as:

$$R_{126} \leq \frac{V_{IN\_L1(MAX)}\cdot\left(R_{124}+R_{125}\right)}{V_{L1\_pk(MAX)}-V_{IN\_L1(MAX)}} = \frac{1.25\cdot\left(470+470\right)\cdot 10^{3}}{1.04\cdot 265\cdot\sqrt{2}-1.25} = 3.02k\Omega \quad (54)$$

Where:

- $V_{IN\_L1(\max)} = 1.04 \cdot V_{L1\_pk}$ is the maximum peak line voltage increased by a certain margin (4% in this design)

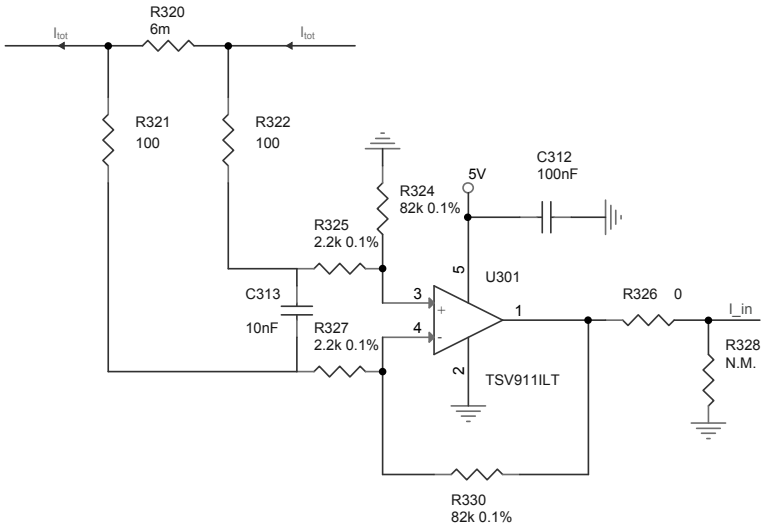
Identical values are used for V_{IN_L2} sensing.

You should use R126(123) with 0.1% tolerance and insert a low-pass filter as close as possible to VIN[0]([1]) PIN 31(38) (10 kΩ, 1 nF in this design).

6.2 Input current sensing

Shunt resistor R320 converts the total input current into a voltage. A differential OP-AMP circuit (TSV911: single supply, rail-to-rail) is used to amplify the sensing signal.

Figure 22. **Input current sensing circuit**



For adequate sensing margins due to component tolerances, the maximum total inductor peak current is increased by a certain percentage (15% in our example).

The relationship $\frac{R_{324}}{R_{325}} = \frac{R_{330}}{R_{327}}$ must be satisfied to reduce the Common Mode Rejection Ratio (CMRR), so 0.1% tolerance input and feedback resistors are recommended.

In this configuration, the output voltage is proportional to the difference between positive and negative input voltage:

$$V_{I\_in} = I_{tot} \cdot R_{320} \cdot \frac{R_{330}}{R_{327}} \tag{55}$$

The maximum value must not exceed 4.7 V. So, if R325 and R327 are set at 2.2 kΩ, R330 can be derived:

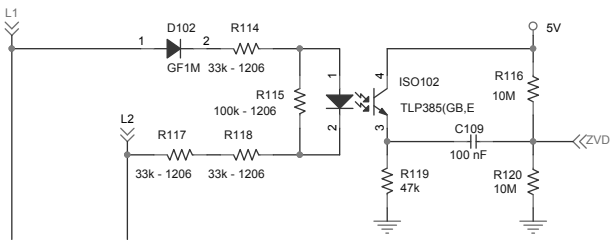
$$R_{330} \leq \frac{V_{I\_in(MAX)} \cdot R_{327}}{I_{tot(MAX)} \cdot R_{320}} = \frac{4.7 \cdot 2200}{20.6 \cdot 0.006} = 83.6k\Omega \tag{56}$$

Hence an 82 kΩ 0.1% resistor can be selected.

6.3 ZVD sensing

A zero voltage detection (ZVD) isolated circuit is used to synchronize PFC operation with the zero crossing of the input voltage.

Figure 23. **ZVD circuit**

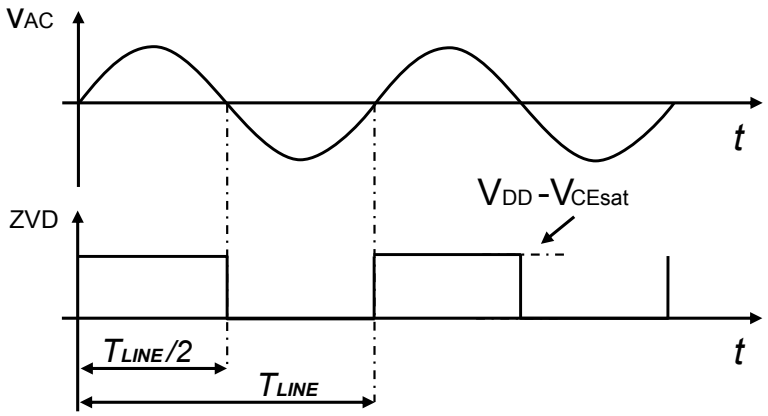


Resistors R114, R117 and R118 limit the sensing current to a few milliamps, while R115 sets the voltage for correct conduction of the optocoupler diode.

During the positive half-cycle, diode D102 is directly polarized and the optocoupler is turned on, so capacitor C109 is charged and ZVD voltage is clamped to V_{DD}-V_{CEsat}.

During the negative half-cycle, the optocoupler is open, so the capacitor is discharged (through R119) and the ZVD voltage equals GND.

Figure 24. **ZVD circuit waveform**

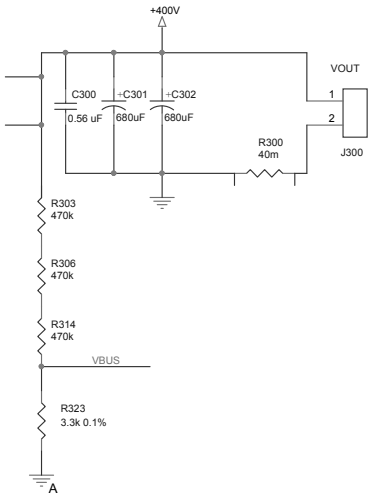


You should insert a low-pass filter as near as possible to ZVD PIN 17 (10 kΩ 100 pF, in this design).

6.4 Output voltage sensing

A common voltage divider is used to sense the PFC output voltage.

Figure 25. **Output voltage sensing**



The sensing voltage must not exceed 1.25 V and is calculated with the following equation:

$$V_{BUS} = V_{OUT}\frac{R_{323}}{R_{303} + R_{306} + R_{314} + R_{323}} \quad (57)$$

Starting again from R303=R306=R314= 470 kΩ, we can determine the lower resistor:

$$R_{326} \leq V_{BUS(MAX)} \cdot \frac{R_{303} + R_{305} + R_{314}}{V_{OUT(MAX)} - V_{BUS(MAX)}} = 1.25 \cdot \frac{\left(470 + 470 + 470\right) \cdot 10^3}{1.25 \cdot 400 - 1.25} \cdot 3.53 \quad (58)$$

$k\Omega$

Where:

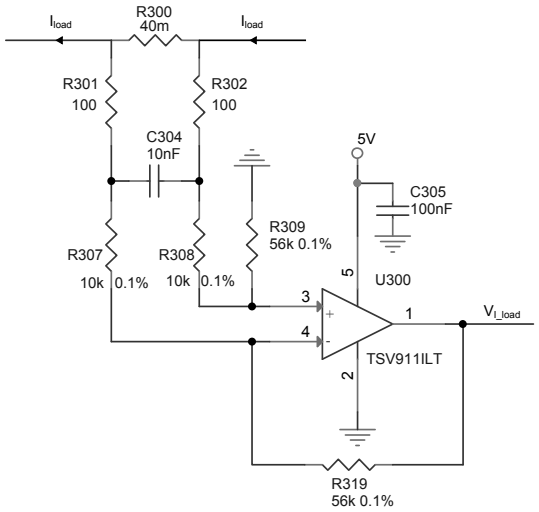
- $V_{OUT(MAX)}$ is the nominal output voltage increased by a certain margin (25% in this design).

A 3.3 kΩ 0.1% resistor is used and a low-pass filter should be placed as near as possible to VOUT PIN 34 (10 kΩ 220 nF, in this design)

6.5 Output current sensing

Similar to input current sensing, a shunt resistor (R300) and a differential OP-AMP circuit are used to sense the output current.

Figure 26. Output current sensing circuit



The equation for the output is:

$$V_{I\_load} = I_{load} \cdot R_{300} \cdot \frac{R_{319}}{R_{307}} \quad (59)$$

The maximum output voltage must not exceed 1.25 V. The relationship $\frac{R_{309}}{R_{308}} = \frac{R_{319}}{R_{307}}$ must be satisfied (0.1% tolerance resistors) and a sensing margin is applied (10%).
If R307=R308=10 kΩ and R300=40 mΩ:

$$R_{319} \leq \frac{V_{I\_load(MAX)} \cdot R_{307}}{I_{load(MAX)} \cdot R_{300}} = \frac{1.25 \cdot 10000}{1.1 \cdot 5 \cdot 0.040} = 56.8k\Omega \quad (60)$$

Where:

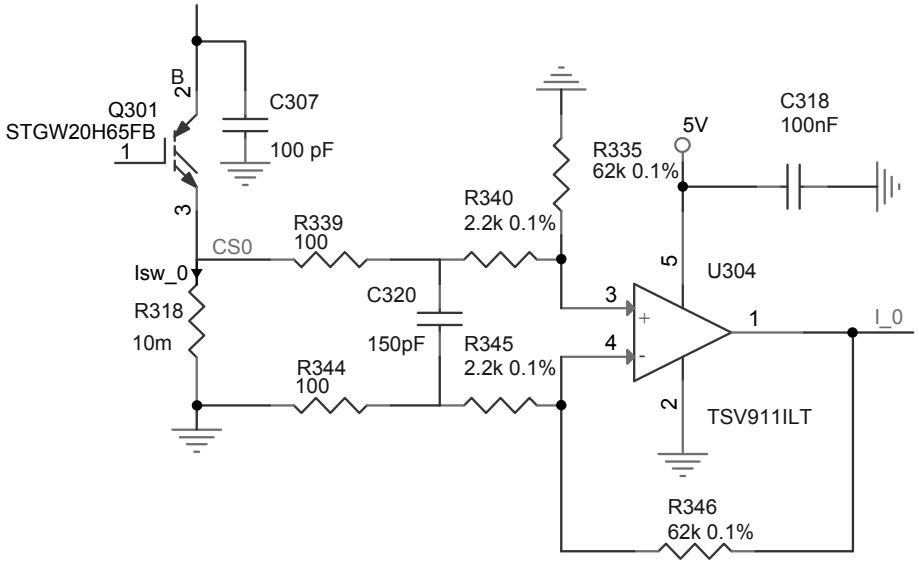
- $I_{load(MAX)}$ is the maximum output current increased by a certain margin (10% in this design).

So a 56 kΩ 0.1% resistor is selected.
You should place a low-pass filter as near as possible to IOUT PIN 33 (10 kΩ 15 nF, in this design).

6.6 Switch current sensing

Two circuits similar to the output current sensing circuit are used to sense the switch current of each channel.

Figure 27. **Switch current sensing circuit**



The maximum output voltage is set at 4.7 V in order to maximize the sensing dynamic and the noise immunity. In this case, the maximum input current is the inductor saturation current (10% margin).

If R340=R345=2.2 kΩ and R318=10 mΩ:

$$R_{346} \leq \frac{V_{I\_0(MAX)} \cdot R_{345}}{I_{sw\_0(MAX)} \cdot R_{318}} = \frac{4.7 \cdot 2200}{1.1 \cdot 15 \cdot 0.010} = 65.6k\Omega \quad (61)$$

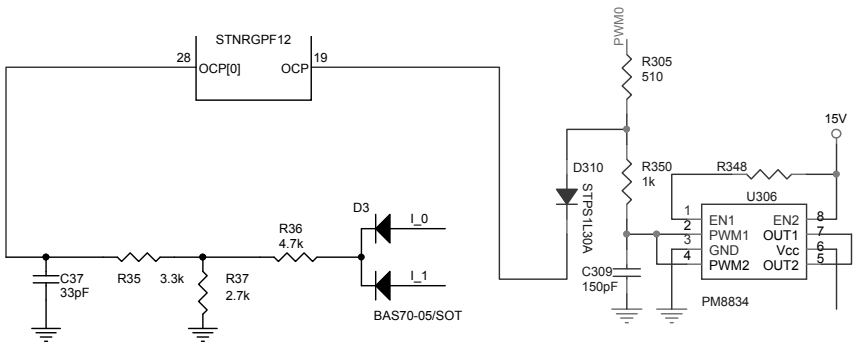
So a 62 kΩ 0.1% is selected.

The sensed current is used by the hardware fast overcurrent protection (OCP) and switch average current balance (CB) functions (signals coming from I_0 and I_1 are filtered and sent to PIN 35 and 36, respectively).

6.7 Overcurrent protection circuit

The peak current of each switch needs to be limited to prevent inductor saturation, which could cause very high currents and damage the board.

Figure 28. **Overcurrent protection circuit**



The two switching currents (I_0, I_1) are sent to an internal comparator in OR configuration.

A voltage divider is used to adapt the output of switching current sensing to the internal protection threshold 1.23V ($V_{th(CMP)}$) on OCP[0] PIN 28. For example, if the maximum peak current is set at 13 A, the output of switch current sensing is:

$$V_{I\_0(OCP)} = I_{sw\_0(OCP)} \cdot R_{318} \cdot \frac{R_{346}}{R_{345}} = 13 \cdot 0.010 \cdot \frac{62000}{2200} = 3.66V \quad (62)$$

The output of the comparator is forced HIGH when one of the two signals exceeds $V_{I\_0(OCP)}$, so for R36=4.7 kΩ, R37 can be calculated:

$$R_{37} \leq V_{th(CMP)} \frac{R_{36}}{V_{I\_0(OCP)} - V_{f\_diode} - V_{th(CMP)}} = 1.23 \cdot \frac{4700}{3.66 - 0.3 - 1.23} = 2.71k\Omega \quad (63)$$

A 2.7 kΩ resistor is selected.

When the internal comparator is activated, PIN 19 (normally HIGH) becomes LOW and fast switches off the input of all the drivers (PM8834). The red LED lights up to indicate a FAULT condition on the STNRGPF12.

7 PFC controller customization with eDesign Suite

The eDesignSuite suite software tool developed by STMicroelectronics helps you configure ST products power conversion applications. You can use it to customize the PFC controller for a specific application: you start by entering the main specifications for your design and then generate an automatic design or follow a sequential process to build a highly customized design.

Figure 29. PFC specifications

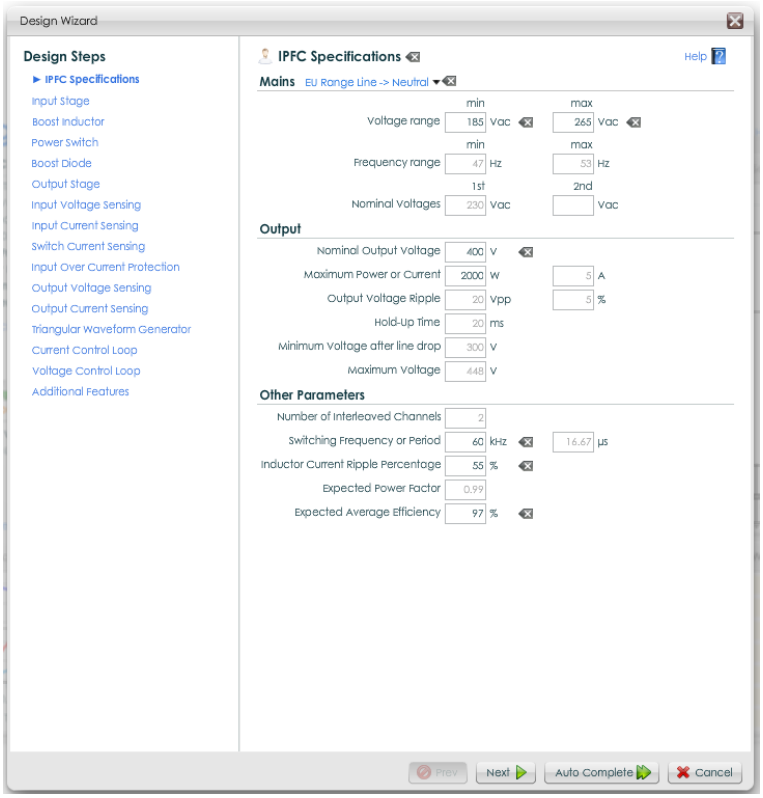


Figure 30. **PFC step-by-step design**

RELATED LINKS

See RM0446 for details on how to use eDesignSuite to generate specialized firmware

8 Experimental results: steady-state, dynamic waveforms and typical PFC performance curves

8.1 Startup behavior

Following connection to the grid, the auxiliary power supply starts and the device is supplied. During the output capacitor pre-charging phase, the inrush current is managed by digital control of the SCRs, which are fired with an incremental step of 40 µs backwards (with respect to the relative zero voltage crossing) each half-cycle. As soon as the pulse width is large enough (firing angle greater than 90 degrees) the SCR control is set and locked at 50% of duty cycle for the line frequency.

The board is designed to start in a no load condition, and if the grid parameters (voltage and frequency) are within the correct range, the board initiates a no-load startup with burst mode operation and output voltage regulated between 416 V and 436 V.

Once the startup phase has finished, a green LED indicates that the PFC is ready for a load connection.

Figure 31. No-load startup at 115 V_{AC}

green: output voltage
yellow: input current

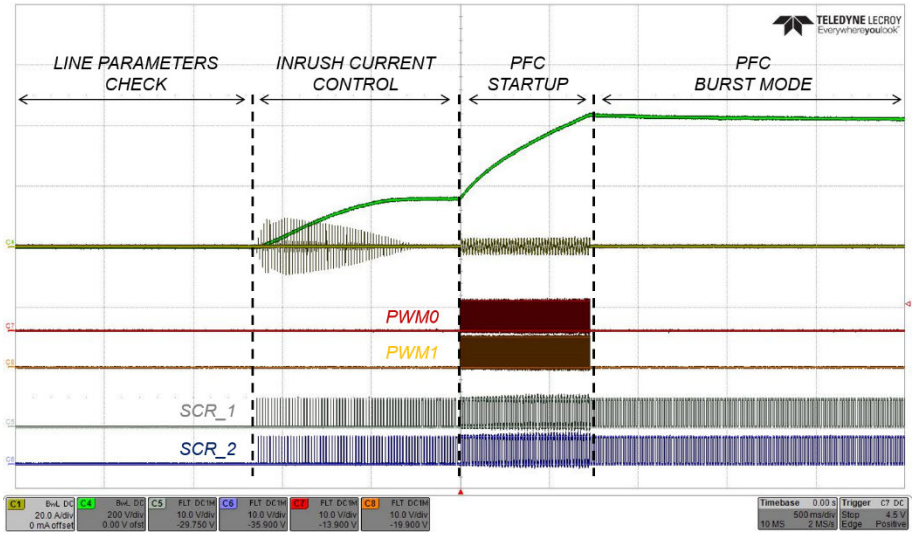


Figure 32. No-load startup at 230 V_{AC}

green: output voltage
yellow: input current

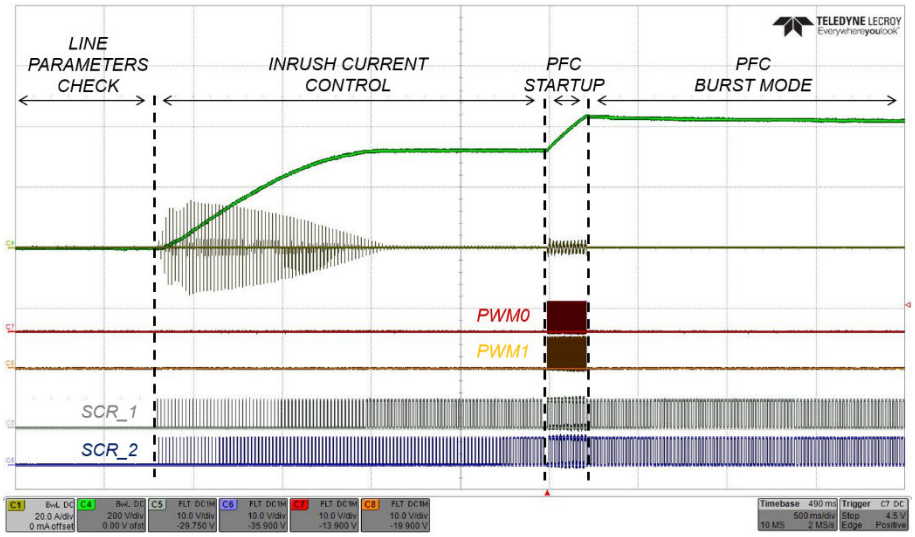


Figure 33. Inrush current control detail at 230V_{AC}

green: output voltage
magenta: input voltage
yellow: input current

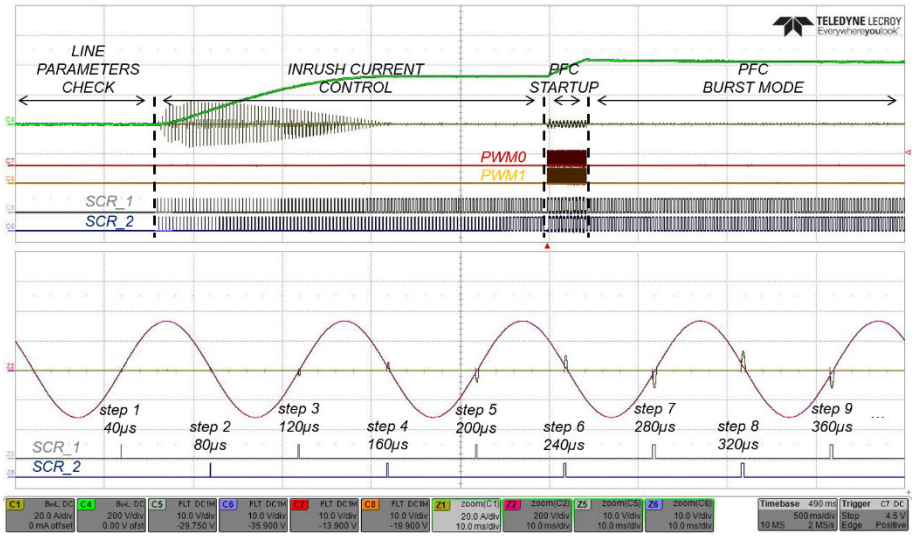
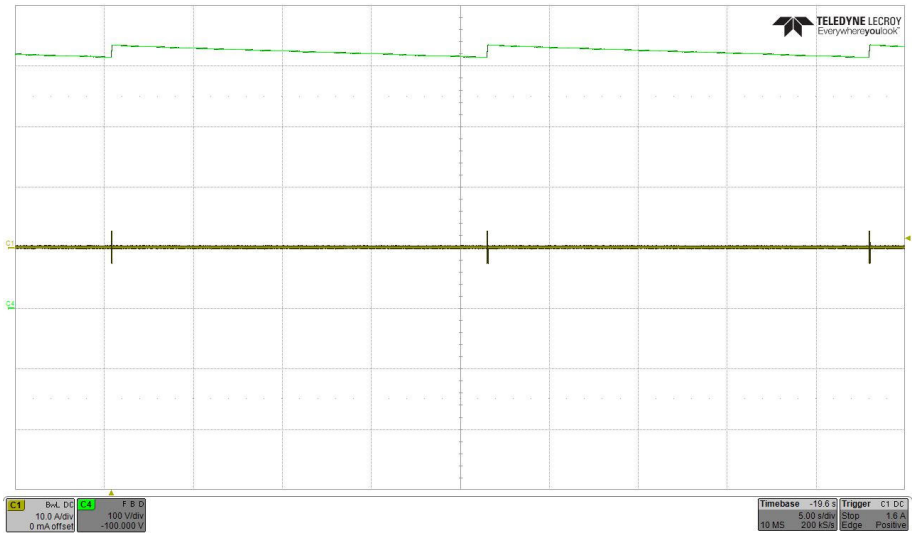


Figure 34. Burst Mode operation

green: output voltage
yellow: input current



RELATED LINKS

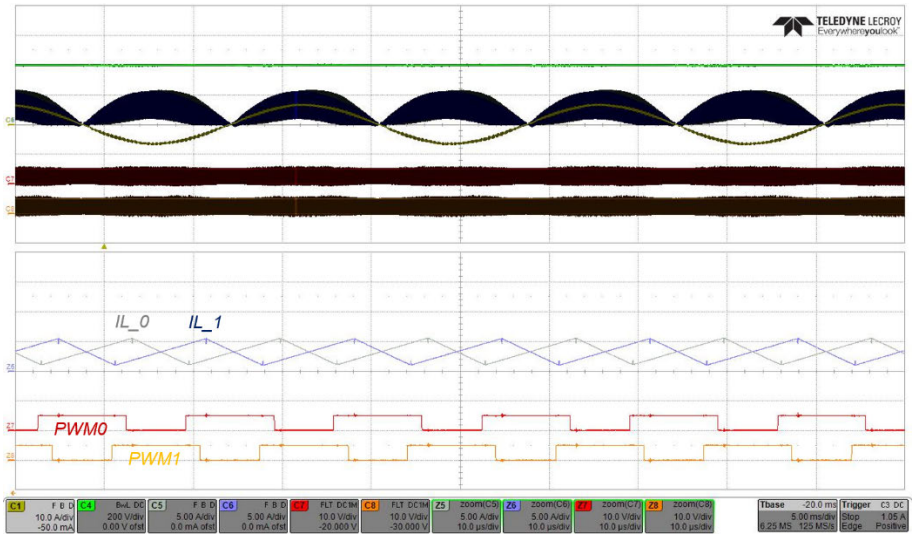
For more information on SCR control, search www.st.com for UM2076: "Getting started with the STEVAL-ISF003V1" (section 8: SCR switch insulated control)

8.2 Inductor currents

The following figure shows the inductor currents waveforms of the converter. The interleaving operation is evident and the channels currents are phase shifted 180 degrees. In this case, the master PWM signal (red) has a duty cycle of about 60%.

Figure 35. Inductor currents at 115 V_{AC}

gray: master inductor current
blue: slave inductor current



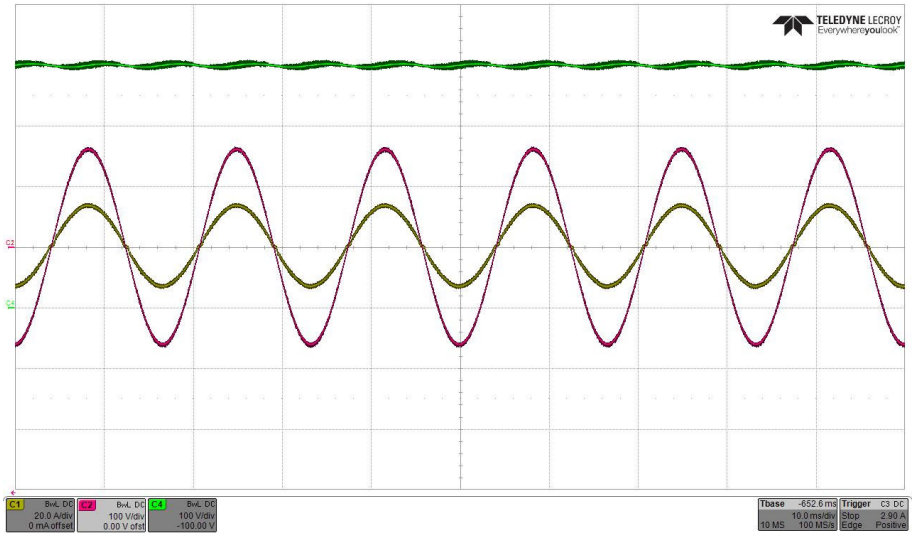
8.3 Behavior during operation

An Agilent 6813B AC power source is used to supply the board at low line: 115 V_{AC} with 1 kW load (the maximum power that the converter can manage is de-rated for 115 V_{AC} for thermal reasons).

The line current in the figure below is a perfect sinusoidal wave and in phase with the line voltage, while the output voltage is regulated at 400 V.

Figure 36. PFC input voltage and current at 1 kW and 115 V_{AC} input

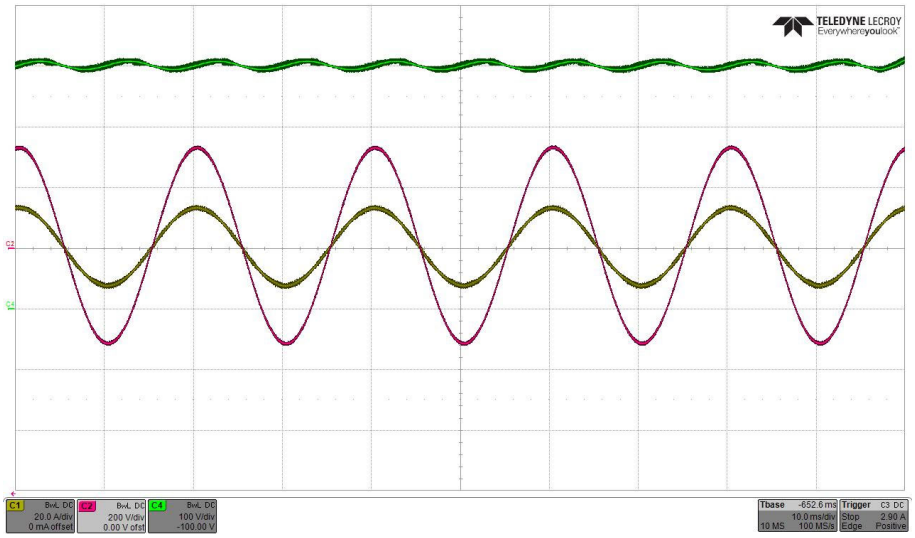
Green: output voltage
Magenta: input voltage
Yellow: input current



The high performance of the proposed control scheme is also evident at 230 V_{AC} and nominal power. The line current adheres to the current reference properly.

Figure 37. PFC input voltage and current at 2 kW with 230 V_{AC} input

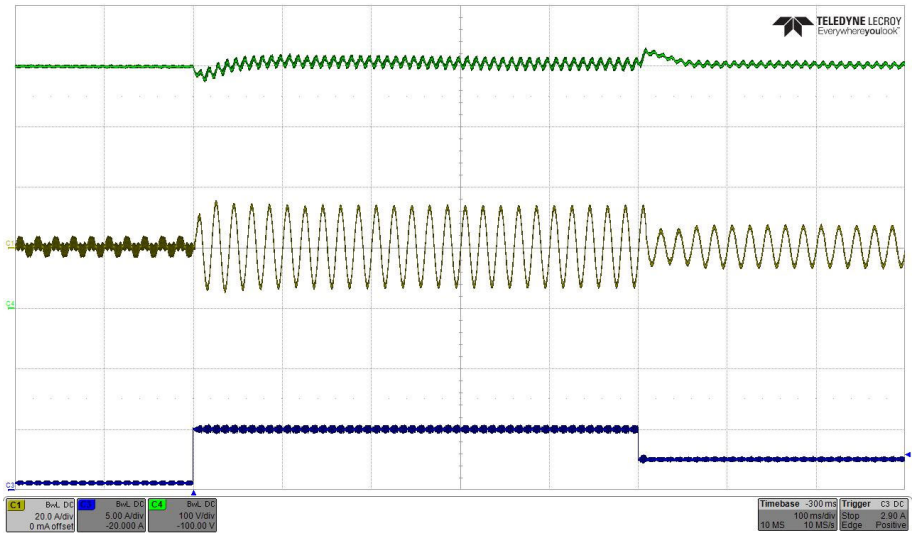
Green: output voltage
Magenta: input voltage
Yellow: input current



During a load step sequence 10% - 100% - 50%, the PFC demonstrates a rapid dynamic response thanks to the load feed-forward. Also, the DC bus voltage is tightly regulated at the reference value.

Figure 38. **10% to 100% to 50% load transition at 230 V_{AC}**

Green: output voltage
Yellow: input current
Blue: output current



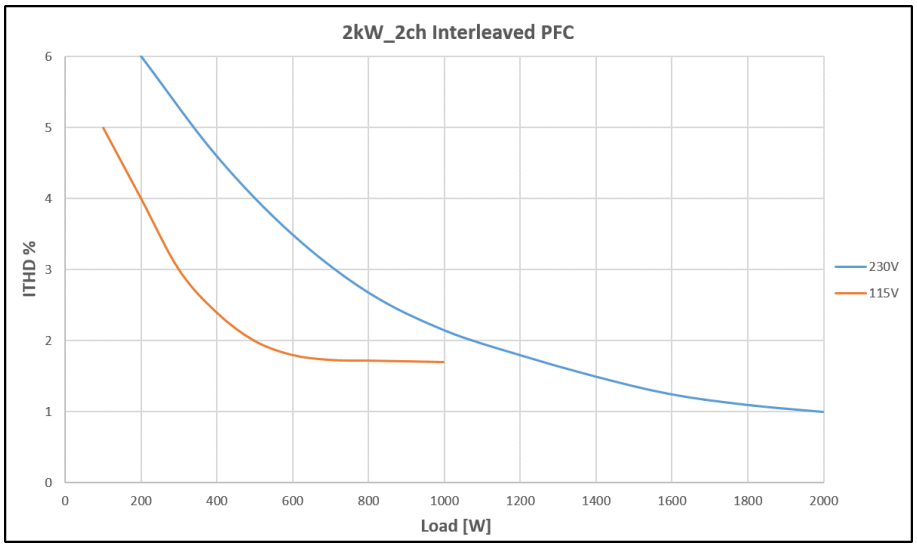
8.4 Steady state performance

A universal power analyzer (Voltech PM6000) is used to evaluate the steady state performance of the PFC.

8.4.1 THD

The input current THD is below 5% for a load higher than 20%. It decreases down to 1% at 230 V_{AC} (full load) and below 2% at 115 V_{AC} (1 kW).

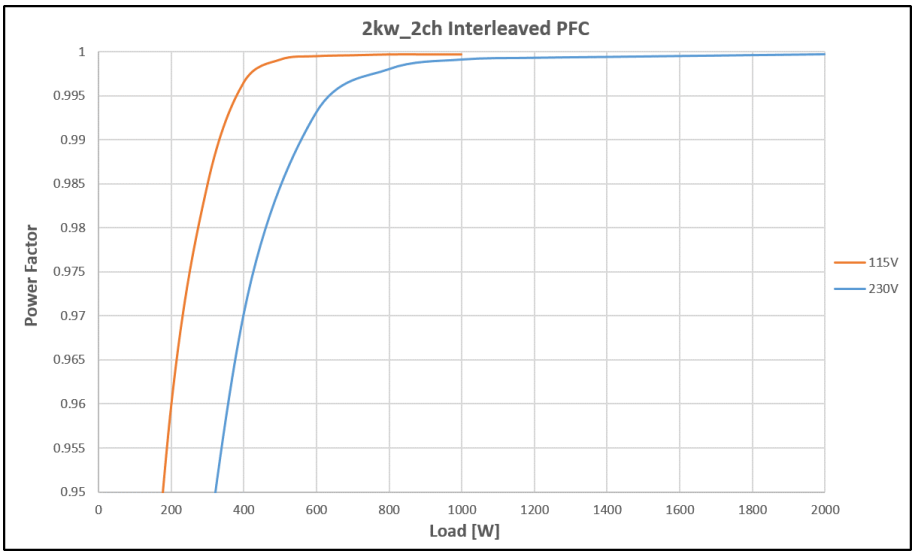
Figure 39. **Input current THD% vs output power**



8.4.2 Power factor

An almost unity power factor is achieved, with values higher than 0.99 for loads above 20% of rated power.

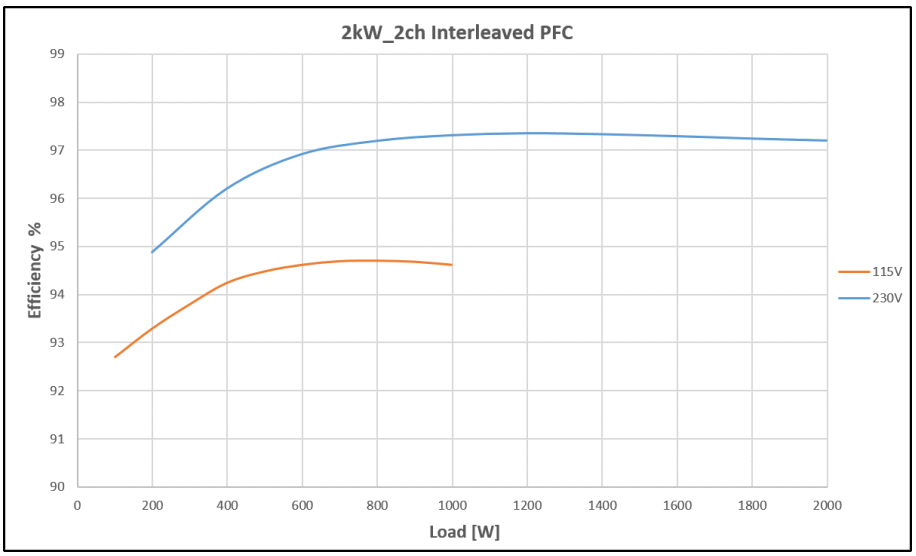
Figure 40. **PFC power factor vs output power**



8.4.3 Efficiency

The phase shedding control strategy produces a flat curve (97.3% at 230 V_{AC}) in the measured efficiency results.

Figure 41. **PFC efficiency vs output power**



9 Conclusions

We presented a 2 kW, 2-channel interleaved PFC with digital inrush current control for industrial applications in this document. The interleaving technique used on the STEVAL-IPFC12V1 yielded very good power density (52 W/inch3) and mixed signal control provided optimal PFC performance.

In particular, the analog current loop allowed us to achieve a high power factor (PF>0.99) and very low THD (<2%) for the rated power, while digital voltage loop helped to maintain excellent output voltage regulation (I/O feed-forwards) and flat efficiency curve, just below 97.5% from 50% to 100% load (phase shedding).

Once bandwidth and phase margins are specified, the design procedure discussed in this document lets you calculate the key control parameters and ensure system stability through the small-signal transfer functions.

The proposed control scheme is implemented on the STNRGPF12 controller, which is able to drive the application and respond appropriately to input and output conditions.

You can also customize the controller and the entire application with the eDesignSuite software tool, which can take the complexity out of the design work and eliminate firmware development efforts altogether.

10 Schematics

10.1 STEVAL-IPFC12P1 power board schematics

Figure 42. **STEVAL-IPFC12P1 schematic - input section**

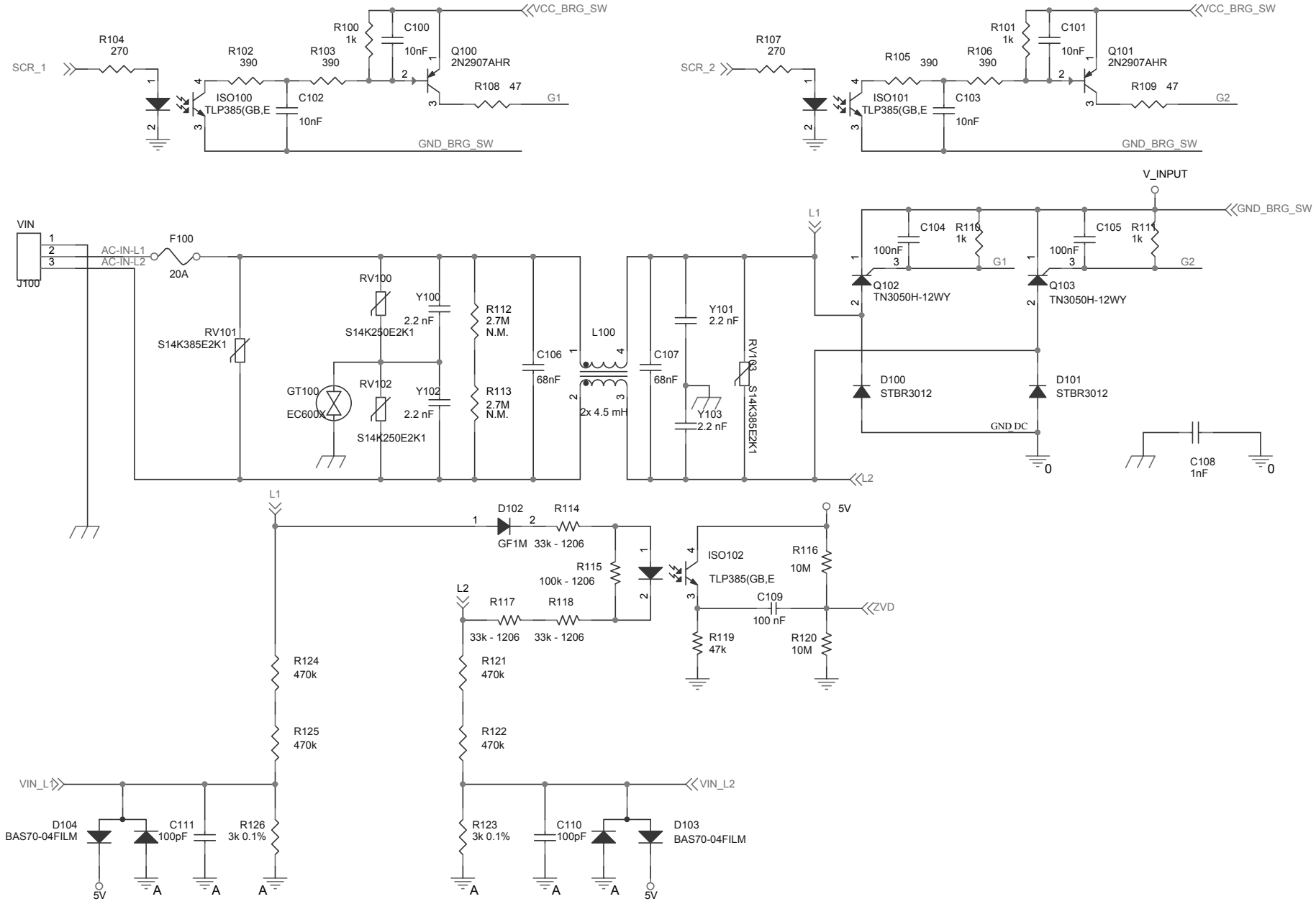


Figure 43. STEVAL-IPFC12P1 schematic - auxiliary power supply

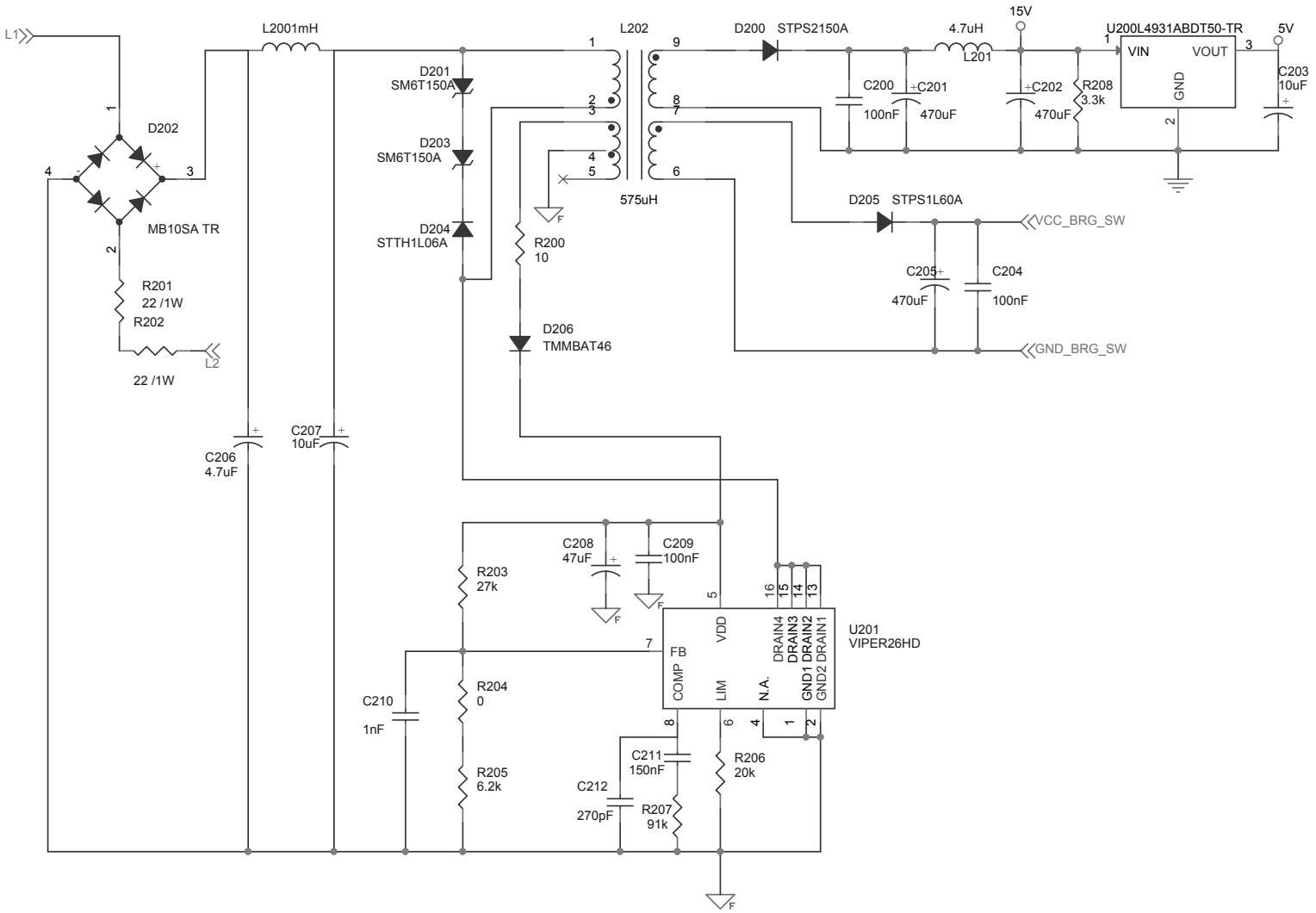
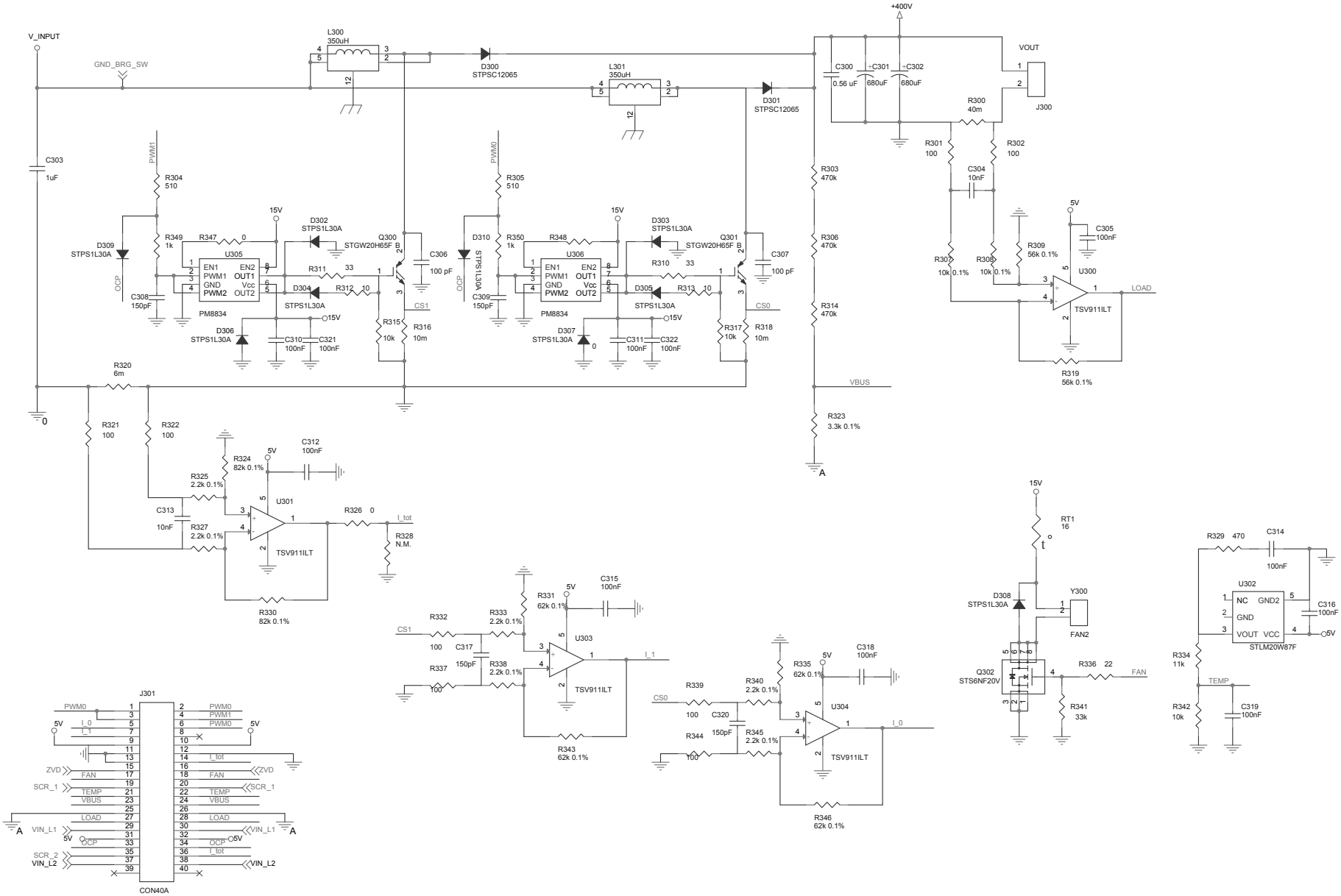
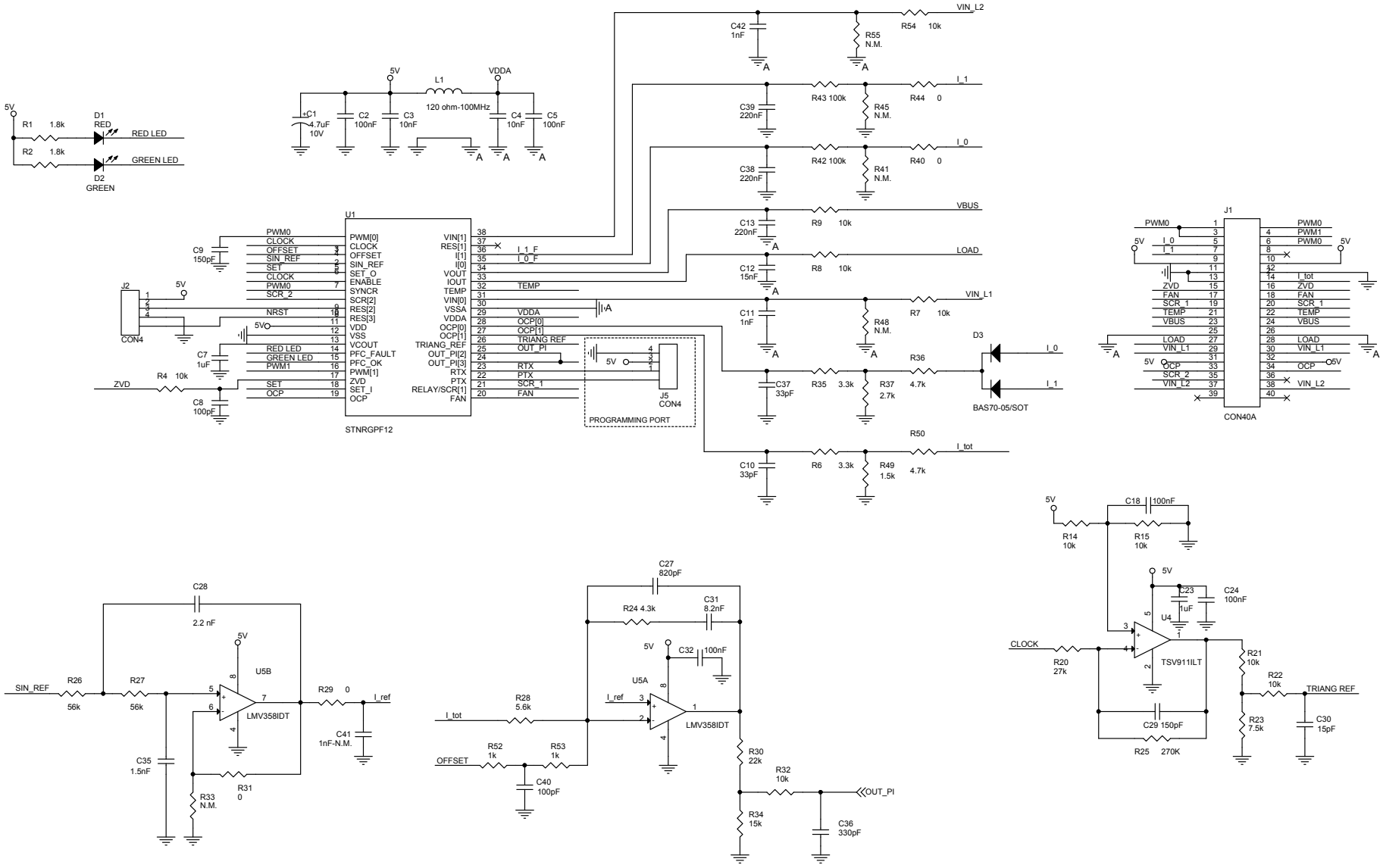


Figure 44. STEVAL-IPFC12P1 schematic - boost interleaving section



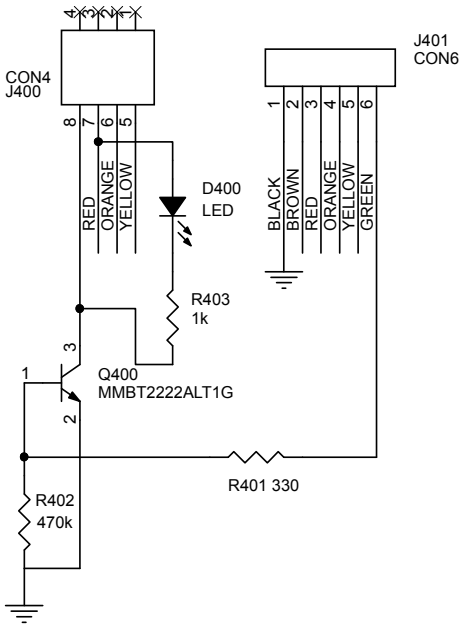
10.2 STEVAL-IPFC12C1 control board schematic

Figure 45. **STEVAL-IPFC12C1 schematic**



10.3 STEVAL-IPFC01A1 adapter board schematic

Figure 46. **STEVAL-IPFC01A1 schematic**



11 Layouts

11.1 STEVAL-IPFC12P1 power board layout

Figure 47. **STEVAL-IPFC12P1 silkscreen - top**

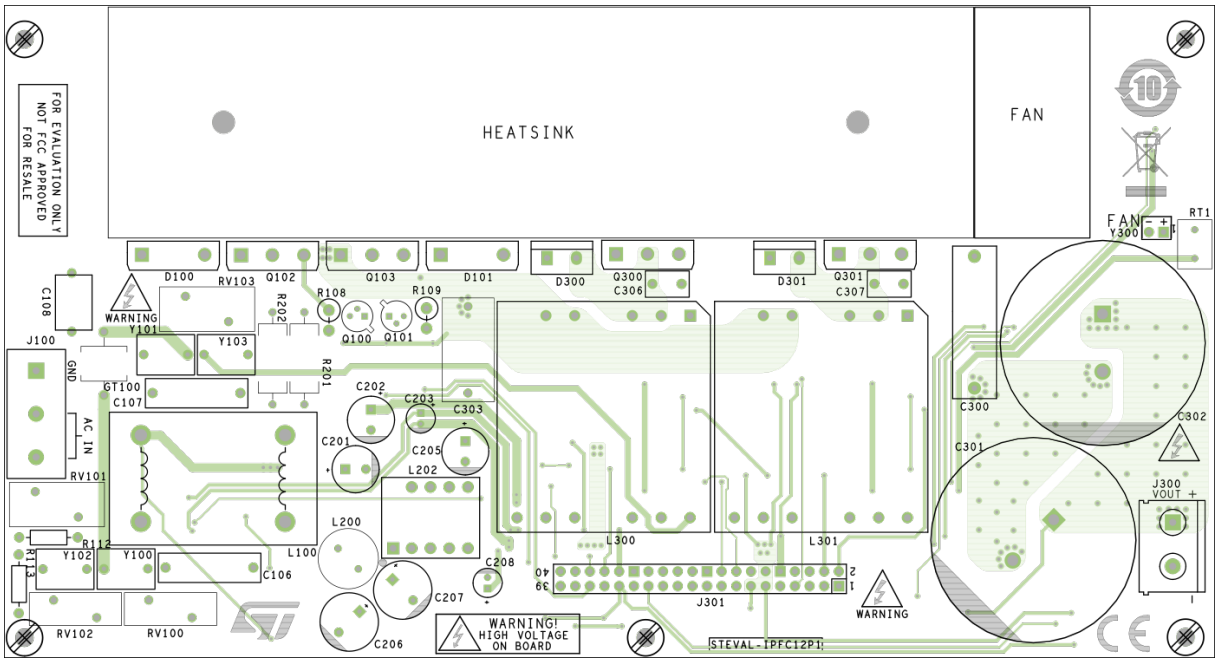
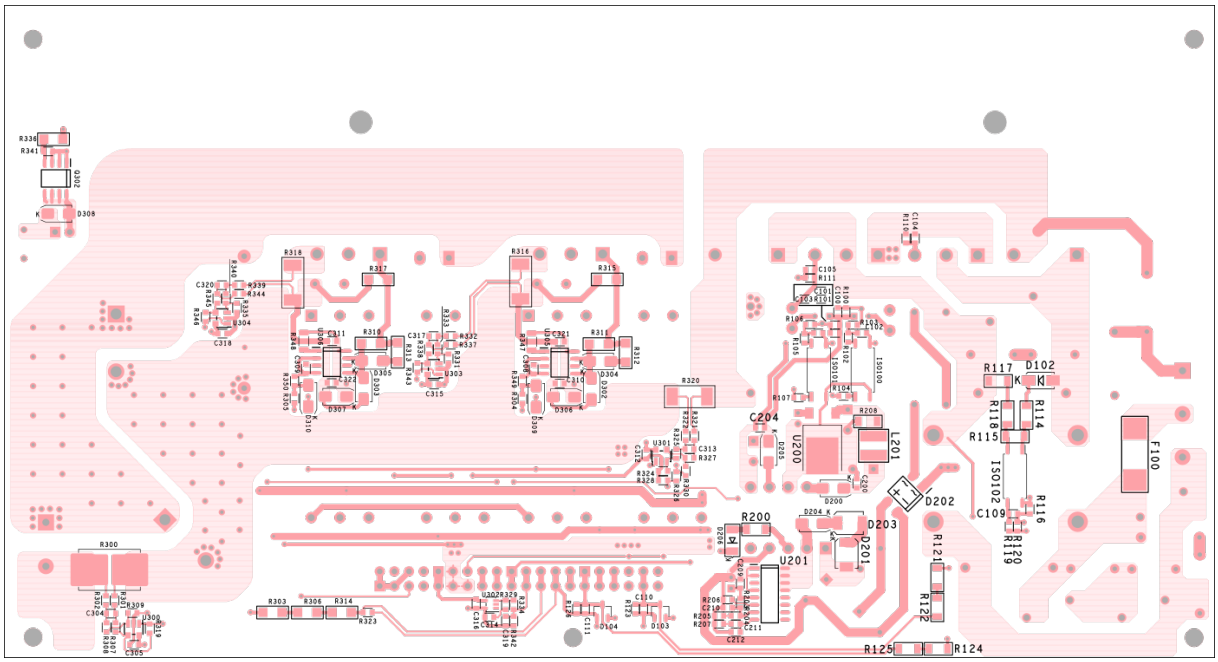
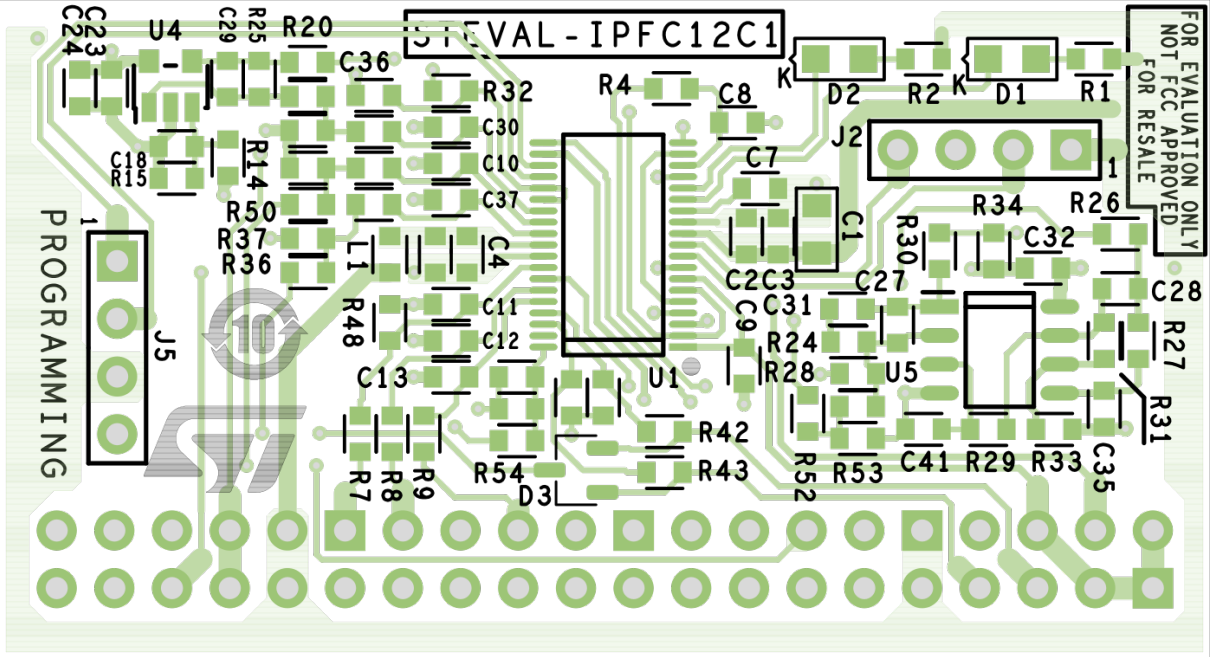


Figure 48. **STEVAL-IPFC12P1 silkscreen - bottom**



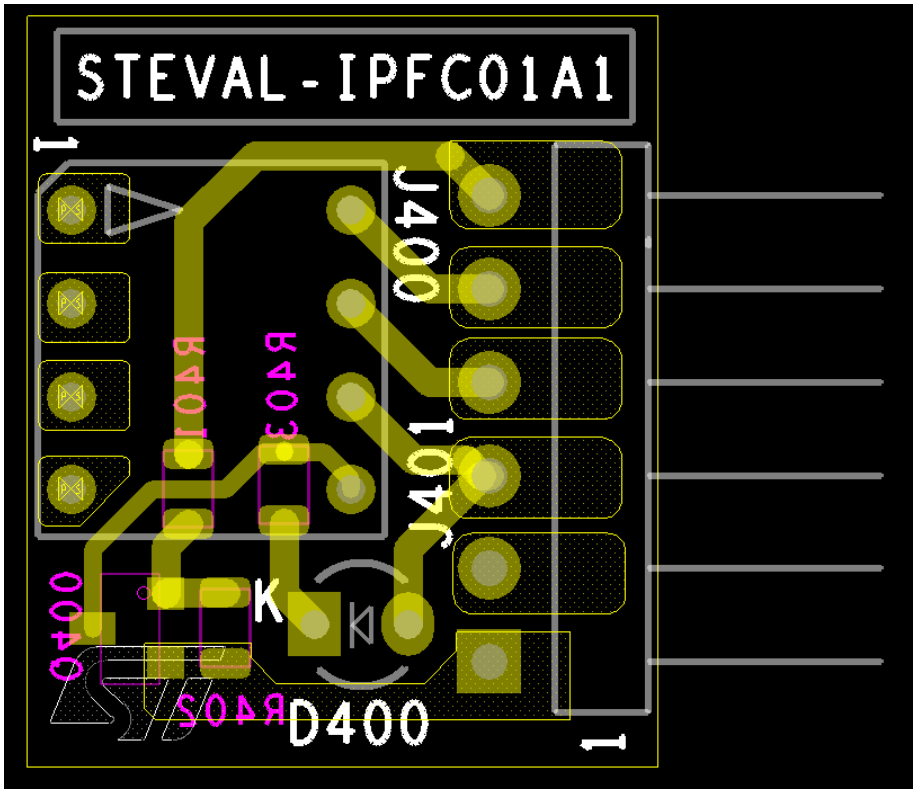
11.2 STEVAL-IPFC12C1 control board layout

Figure 49. STEVAL-IPFC12C1 silkscreen - top



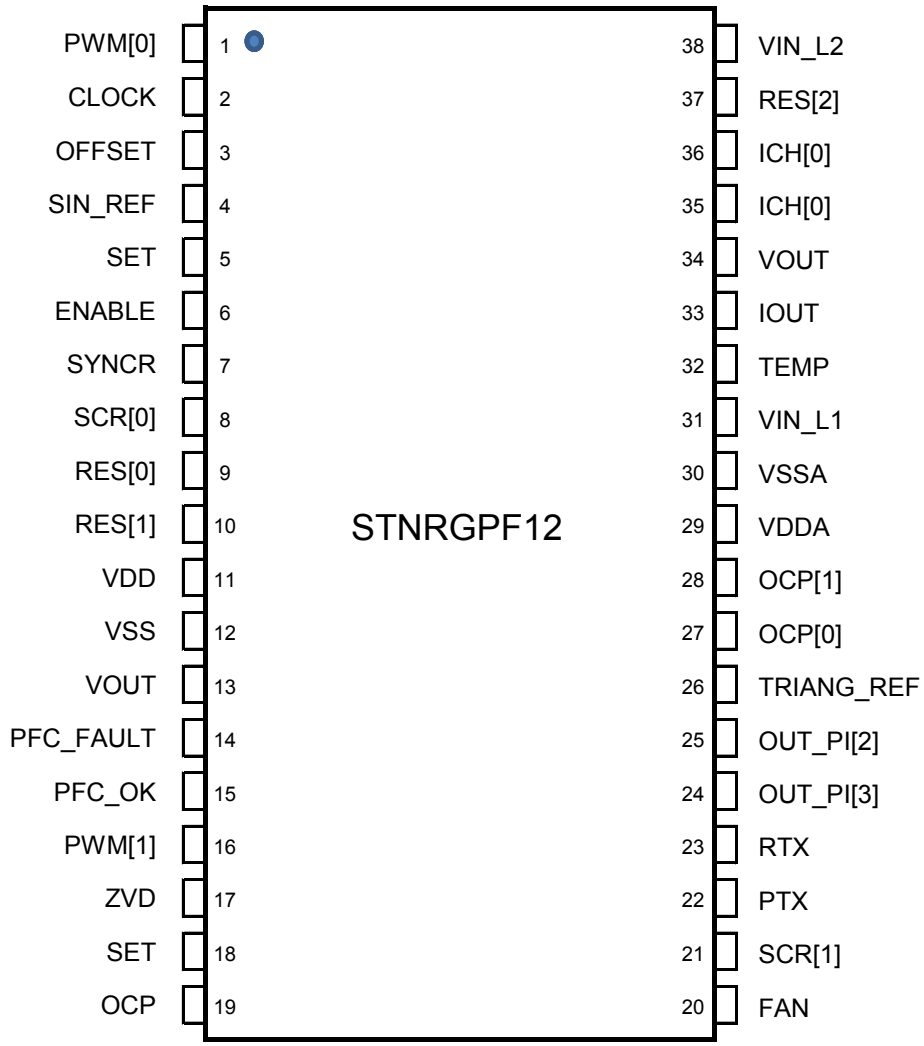
11.3 STEVAL-IPFC01A1 adapter board layout

Figure 50. STEVAL-IPFC01A1 silkscreen - top



12 STNRGPF12 pinout

Figure 51. **STNRGPF12 pinout**



Revision history

Table 3. **Document revision history**

Date	Version	Changes
03-Apr-2019	1	Initial release.

Contents

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