

35 W wide input range flyback converter using HVLED001B quasi-resonant flyback controller and STF10LN80K5

Introduction

The EVAL-PSR01B-35W is intended to provide a stable and insulated 48 V voltage bus suitable to supply secondary side circuitry with a total output power of 35 W when a wide range of input voltages is applied at its input.

A very high power factor is obtained thanks to the features of the HVLED001B. Input voltage variations, excessive input voltage (overvoltage like surge or bursts) and insufficient input voltage are managed by the HVLED001B protections, which improve the reliability of the application.

Output short-circuit and overload protections are auto-restart for safe operation.

Extremely low input power is obtained at no load.

Figure 1. EVAL-PSR01B-35W board



1 Specifications

- Input voltage: V_{in} : 90 - 305 V_{RMS}, f: 45-66 Hz
- Output voltage: 48 V / 730 mA
- PFC / THD:
 - >0.98 / <10% @ 230 V_{AC}, >0.99 / <6% @ 115 V_{AC} @ full load
 - >0.88 / <18% @ 230 V_{AC}, >0.95 / <10% @ 115 V_{AC} @ half load
- No load: better than 150 mW
- Average (4 points) efficiency: 90% at 115 V_{AC} and 230 V_{AC}
- Short-circuit protection with auto-restart
- EMI: compliant with EN51022.

Table 1. Main components

Main components	
HVLED001B	Quasi-resonant flyback controller
STF10LN80K5	N-channel 800 V, 0.55 Ohm typ., 8 A MDmesh K5 Power MOSFET in a TO-220FP package
STPS4S200S	SHOTTKY rectifier diode

The schematic diagram illustrates a 100W LED driver circuit. It begins with a 12V AC input (V_{IN}) connected to a transformer (T1) with a 1:1 ratio. The secondary winding (2) is connected to a bridge rectifier (D1-D4) and a filter capacitor (C1). The output of the rectifier is connected to a buck converter. The buck converter consists of a MOSFET (Q1, STP10LN80K5) driven by a gate driver (U1, HVL6001B) and a diode (D5, 1SMA5942BT3G). The buck converter's output is connected to a 100W LED strip (H1) through a current-sense resistor (R1). The circuit includes various passive components such as resistors (R1-R19), capacitors (C1-C19), and inductors (L1, L2). The output voltage (V_{OUT}) is 48V, and the output current (I_{OUT}) is 750mA. The power dissipation (P_{OUT}) is 35W at V_{IN} = 198-265V.

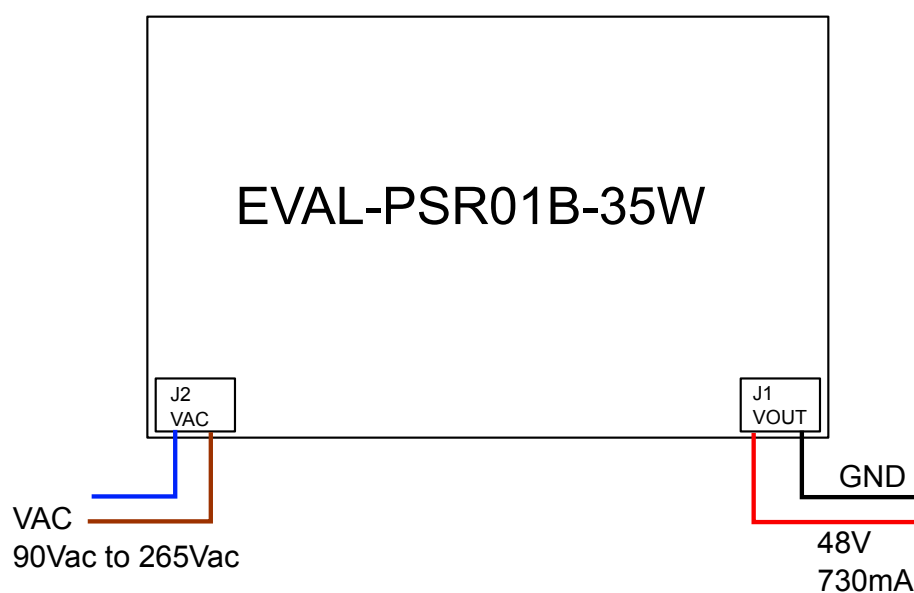
Table 2. Part list

Qty	Ref	Value – Part number	Volt / Watt / Amp	Tol	Notes
1	C1	2.2nF	200V	10%	Not Mounted
1	C2	220nF	100V - 105°C	10%	
1	C3	2.2nF 400V	400V	10%	
1	C4	220nF 310Vac	310V _{AC}	10%	
2	C5,C6	680uF 63V	63V - 105°C	20%	
1	C7	1nF	1kV	20%	
1	C8	10pF	100V	5%	
1	C9	100n	100V	10%	
2	C10, C11	100nF 310Vac X2	310Vac	10%	
1	C12	220pF	1kV	10%	
1	C13	22uF 50V	35V - 105°C	20%	
1	C14	220pF	50V	10%	
1	C15	22nF	50V	10%	
1	C16	220nF	50V	10%	
1	C17	220pF	50V	10%	
1	C18	3.3nF	50V	10%	
1	C19	22uF 50V	6.3V - 105°C	20%	
1	D1	STPS4S200S	100Vr - 0.2AIf		
1	D2	2KBP08M	800V - 2A		
1	D3	BZX384-C33	33V - 0.3W		
1	D4	RS1K	800V / 1A / 500ns		
1	D5	1SMA5942BT3G	51V - 1.3W		
5	D6,D7, D8,D9, D10	1N4148WS	100Vr - 0.2AIf		
1	D11	BZV55-C16	18V - 500mW		
1	F1	1A	250V _{AC}		
1	L1	Wurth - 7447480102 Itacoil - SLD0912102	1mH- 1.2ohm	10%	Alt. part for L1
1	L2	Wurth - 750341636 TDK - B82732F2801B001 Itacoil - SCQ16393	0.8ohm - Lstray>760uH		Alt. part for L2 Alt. part for L2
1	Q1	STF10LN80K5			
1	HS1	HEATSINK			
2	RV1,RV2	TDK - B72210S0301K101	275V _{AC}		
1	R1	10k		1%	Not Mounted
1	R2	10M		5%	
1	R3	100k	0.5W	1%	
1	R4	360R		1%	

Qty	Ref	Value – Part number	Volt / Watt / Amp	Tol	Notes
1	R5	1k		1%	
1	R6	470k		1%	
1	R7	1k		1%	
1	R8	15R		1%	
2	R9,R10	47k		1%	
1	R11	100k		1%	
1	R12	220R		1%	
1	R13	220k		1%	Not Mounted
1	R14	220R		1%	
1	R15	10k		1%	
1	R16	36k		1%	
2	R17,R19	0R62		1%	
1	R18	1k		1%	
2	R20,R21	18.2k		1%	
1	T1	Würth - 750315710	35W - EV25		
		Itacoil - TSLEV2539			Alt. part for T1
1	U1	HVLED001B			

Where not otherwise stated, the capacitance tolerance is equal or better than $\pm 5\%$, the resistor tolerance is equal or better than $\pm 1\%$, while the ratings have to be considered as the minimum requirement.

Figure 3. Board connections



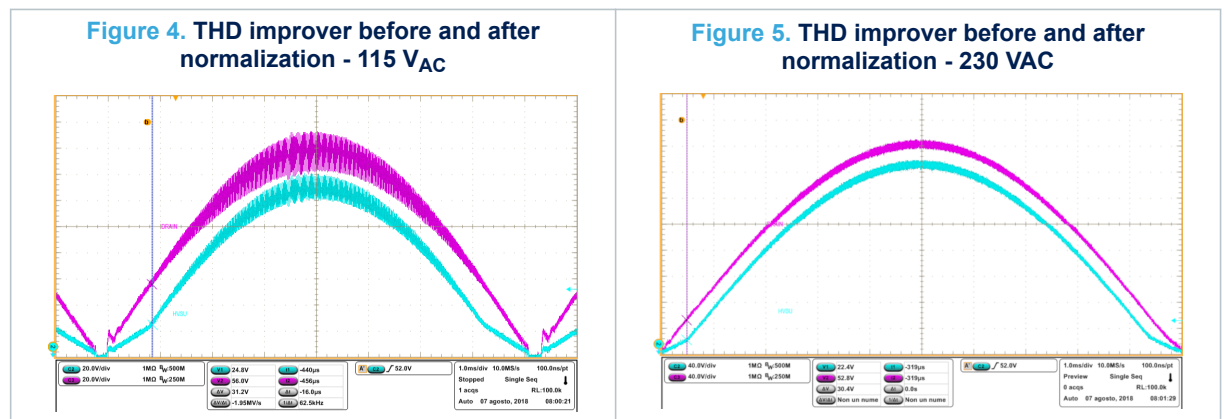
2 Design considerations

The design of this board starts with the selection of the appropriate transformer. The voltage is selected at 150 V in order to meet performance expectations (regulation and efficiency) and to allow the use of an 800 V MOSFET with 305 VAC input voltage.

While a primary inductance value above 240 μH is sufficient to guarantee proper operation of the application, a value of higher than 500 μH will ensure better regulation, lower switching losses and safer EMC figure: the adopted criteria is to obtain a demagnetization time longer than 1.7 μs when the current sense threshold is approximately 300 mV (40% of the max. current sense level).

The theory of QR flybacks used to obtain a high power factor 3. states that an intrinsic THD exists, so a robust method to reduce the THD to values below 10% is implemented on the board: D3 and R2 pre-distorts the input voltage pin of the HVLED001B.

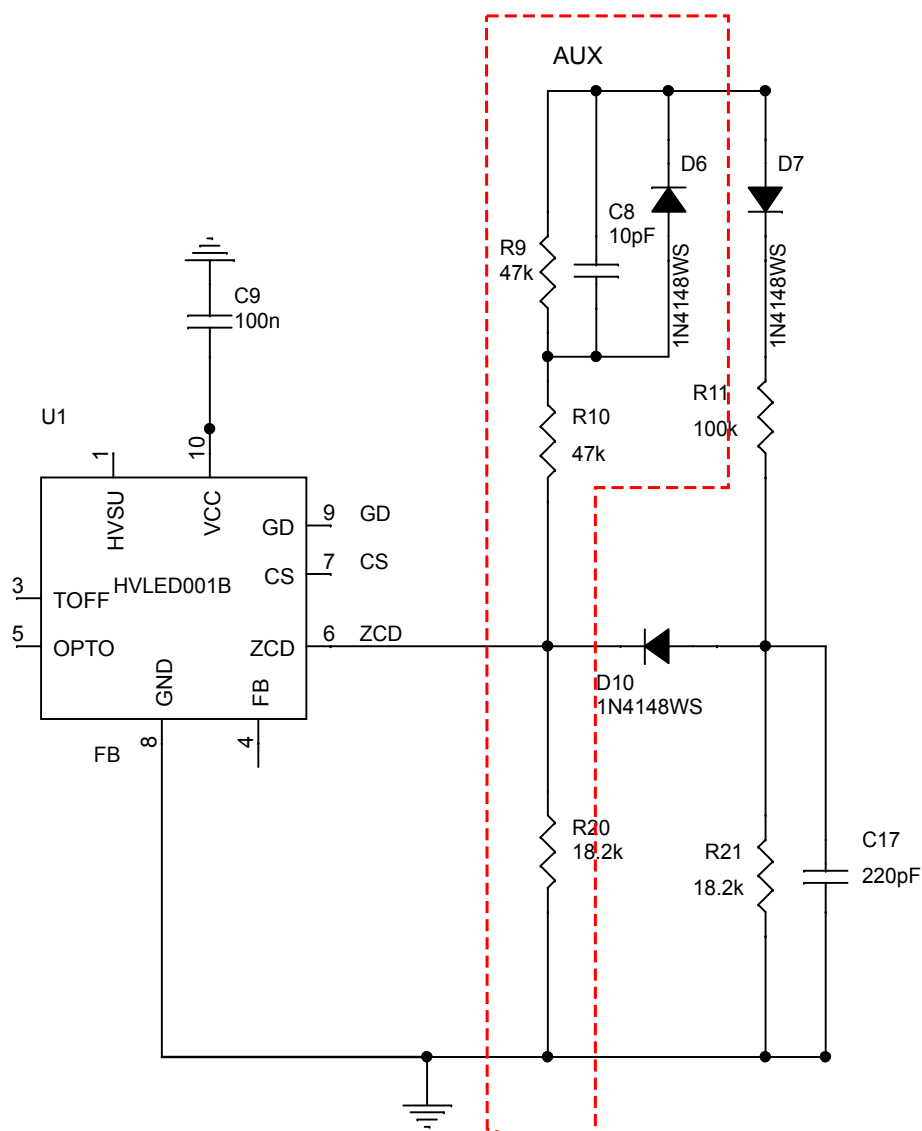
The following figure shows the effect of the THD improver: the red line is the traditional envelop signal, while the blue line shows the improved envelop signal for the current sense threshold.



The HVLED001B embeds a high accuracy reference voltage and a proprietary error amplifier able to control the output voltage by reading the auxiliary winding connected to the ZCD pin. A proper arrangement of both transformer winding arrangement and ZCD voltage divider are suggested to optimize the load and line regulation. The auxiliary winding referred to the primary side is placed further out than the secondary side power winding so the auxiliary winding covers the magnetic field generated by secondary side current during the demagnetization time.

The ZCD voltage divider includes a speed-up structure that contributes to the THD optimization: the size of the capacitor is set to achieve a time constant of 235 ns ($C8 * R9 // R10$)(see Figure 6).

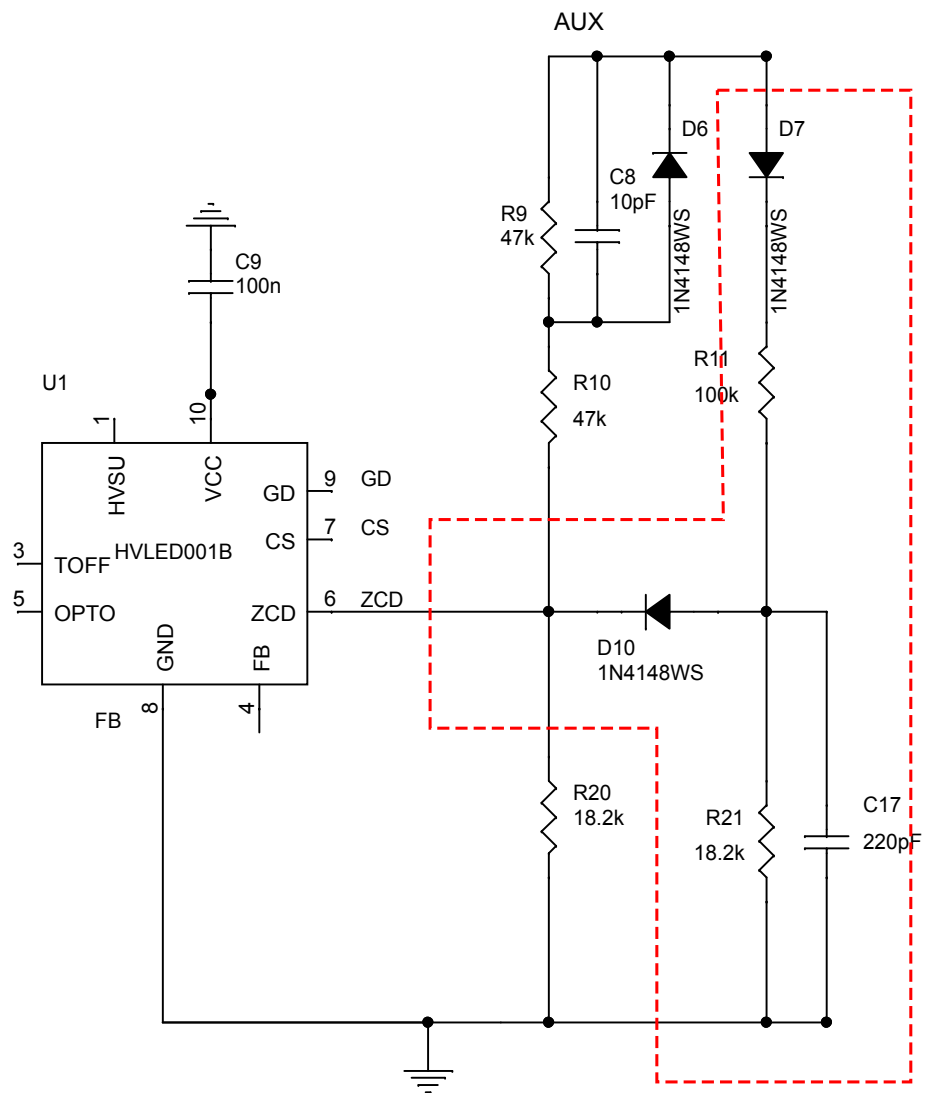
Figure 6. ZCD speed-up structure



A further, optional structure is used to better synchronize the MOSFET turn-on with the the overall efficiency by at least 1%. The delay is generated by capacitor C17, which is charged to a voltage lower than V_{OUT} regulation reference ($V_{REF,PSR}$) and reduces the slope of the ZCD voltage when the voltage of the ZCD drops due to resonance oscillation.

D10 decouples the ZCD voltage divider by the delay generator (see [Figure 7](#)).

Figure 7. ZCD delay structure



3 Measurement results

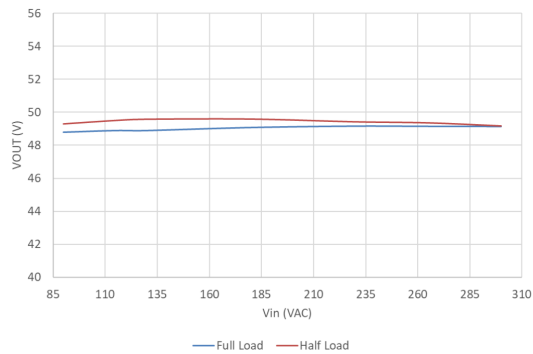
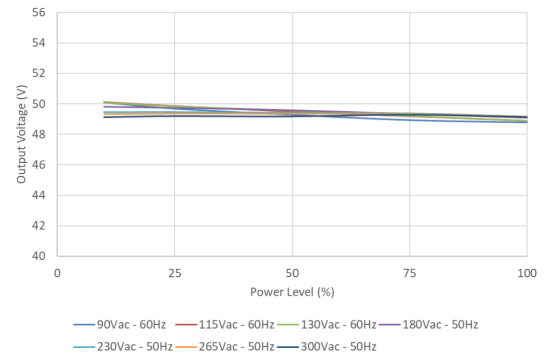
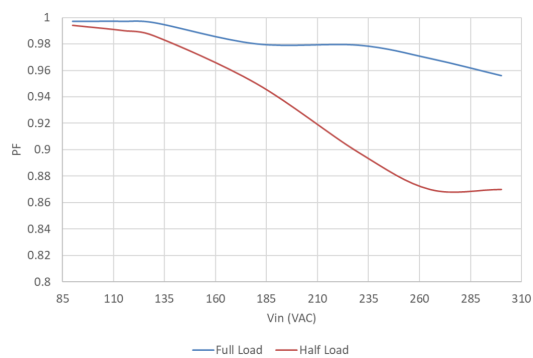
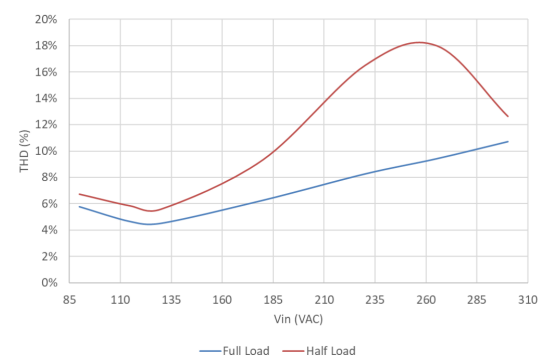
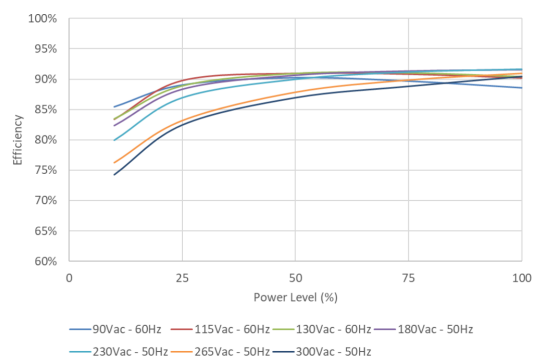
Figure 8. Line regulation

Figure 9. Load regulation

Figure 10. Power factor

Figure 11. Total harmonic distortion

Figure 12. Efficiency vs. load


Table 3. Efficiency table

Load%	$V_{in} = 115 V_{ac}$	$V_{in} = 230 V_{ac}$
100	90.2%	91.6%
75	90.8%	91.2%
50	90.9%	91.6%
25	89.7%	86.9%
Average	90.42%	90.32%
10	83.3%	80.0%

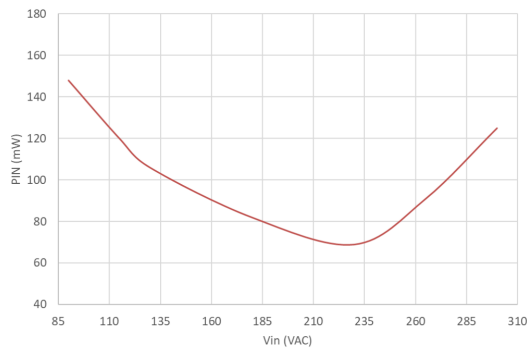
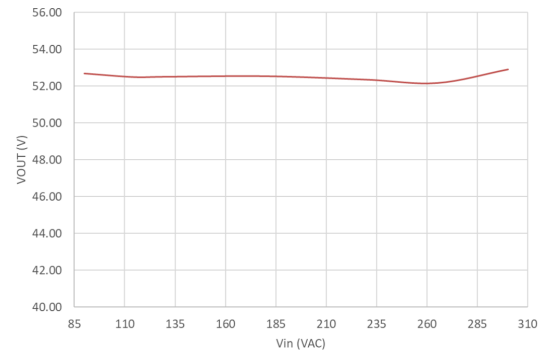
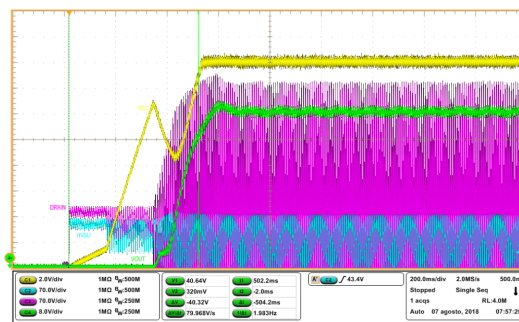
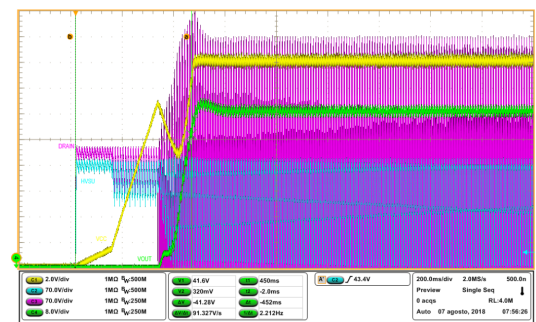
Figure 13. No load input power

Figure 14. Open load voltage

Figure 15. Start-up 115 V_{AC}

Figure 16. Start-up 230 V_{AC}


Figure 18. Load transients 230 V_{AC} 100%-10%-100%

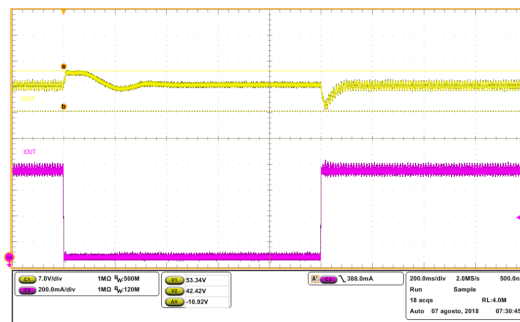


Figure 20. Load transients 230 V_{AC} 75%-25%-75%



4 **References**

1. HVLED001B Datasheet (www.st.com)
2. AN4932, HVLED001A - enhanced QR high power factor flyback controller for LED drivers (www.st.com)
3. AN1059, Design equations of high-power-factor flyback converters based on the L6561 (www.st.com)

Revision history

Table 4. Document revision history

Date	Version	Changes
20-May-2019	1	Initial release.
26-May-2020	2	Updated some data inside Section 2

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