
Automatic antenna tuning (AAT)
for ST25R3916/16B and ST25R3920/20B devices

Introduction

State of the art NFC devices offer high output power together with various bit rates and communication protocols. Higher bit rates and output power can be impaired by detuning of the NFC antenna. Antenna parameters like inductance, self-resonance frequency and Q factor can reduce output power or cause distorted and non-standard compliant signals.

This application note describes how to use the measurement functions available on the ST25R3916, ST25R3916B, ST25R3920, and ST25R3920B devices to implement custom tuning algorithms. Although the document is based on ST25R3916, its content is applicable to the other devices as well.

An implementation of the mentioned algorithms is carried out in the STSW-ST25RFAL002 package, which is, in turn used in X-CUBE-NFC6 and STSW-ST25R011, among others.

This application note must be used with the ST25R antenna matching tool software (STSW-ST25R004), which supports the calculation of the matching components and reduces the tuning iteration effort to a minimum. Along with the tool, an open source simulator is provided for basic system validation via simulation.

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1 Detuning effects

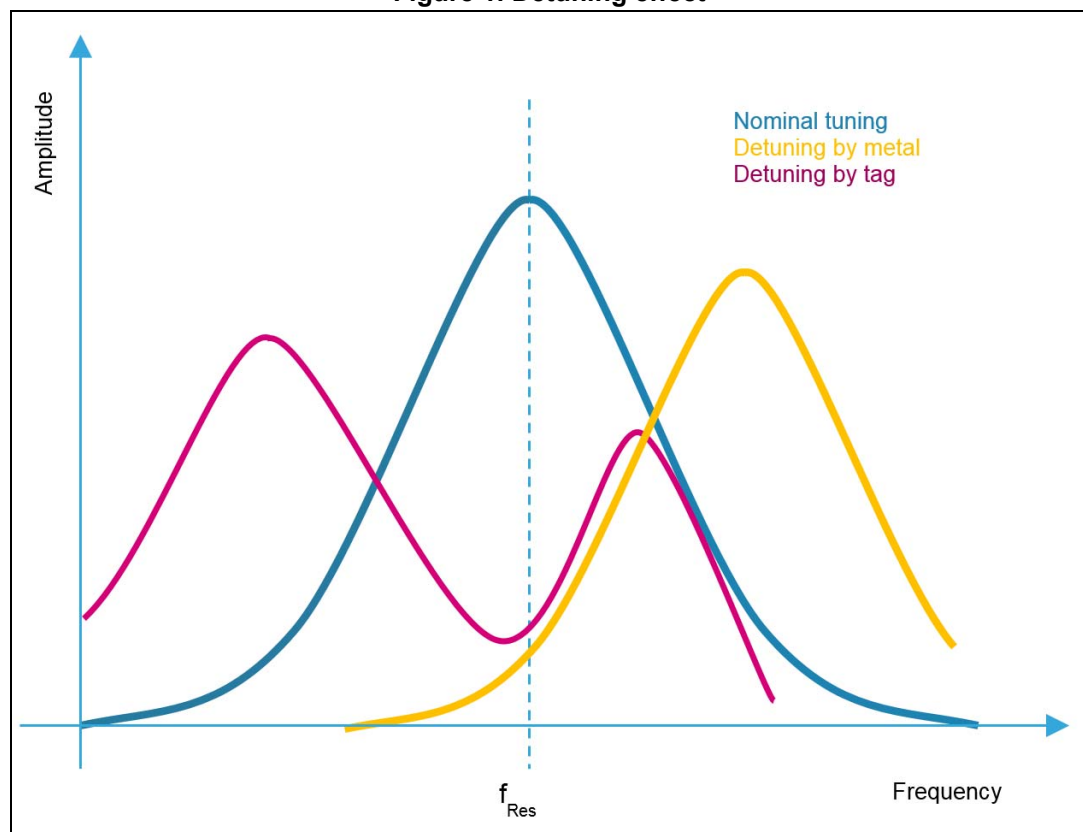
A near field communication (NFC) device is designed to operate with a specific antenna. The antenna-matching network transforms the inductance of the antenna into a real ohmic load seen by NFC reader IC. The NFC device ends up with an antenna tuned to 13.56 MHz and a desired system quality factor (Q), chosen to enable high output power and to support high bit rates. The matching impedance seen by the NFC reader IC is a main factor when adjusting the power consumption.

Detuning effects are influencing this parameter.

An approaching metal object, for example, increases the self-resonance frequency (SRF) of the antenna. Due to eddy currents and ensuing losses in the metal, the Q drops and the read range of the reader is reduced. If the antenna resonance is shifted to a higher frequency, the reader still sends a 13.56 MHz signal. An antenna tuned to a higher frequency generates overshoots and ringing. The signal can be wrongly interpreted by other NFC devices or cards and may not be compliant with the NFC standards.

The card resonance frequency (f_{Res}) is observable in [Figure 1](#), which shows the detuning effects for a nominally tuned reader. Metal objects close to the reader shift the nominal tuning towards higher frequencies. A card tuned to a frequency higher than 13.56 MHz pushes down the nominal tuning.

Figure 1. Detuning effect



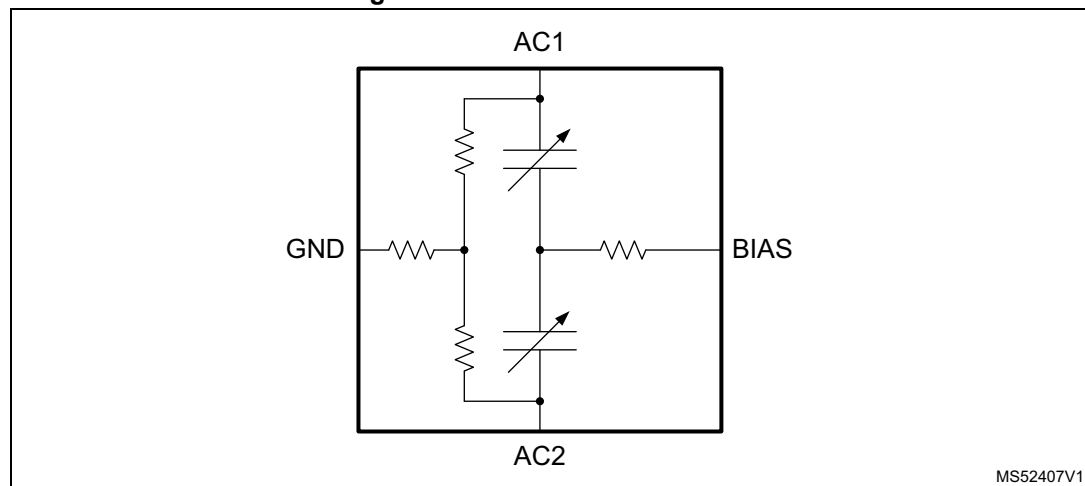
2 Voltage controlled capacitors

A voltage controlled capacitor (VCC) is a four-pin device, where the capacitance changes according to the control voltage.

The tuning range depends upon the manufacturer and the manufacturing process. In this document two VCCs are considered, both with a maximum tuning capacitance of 200 pF:

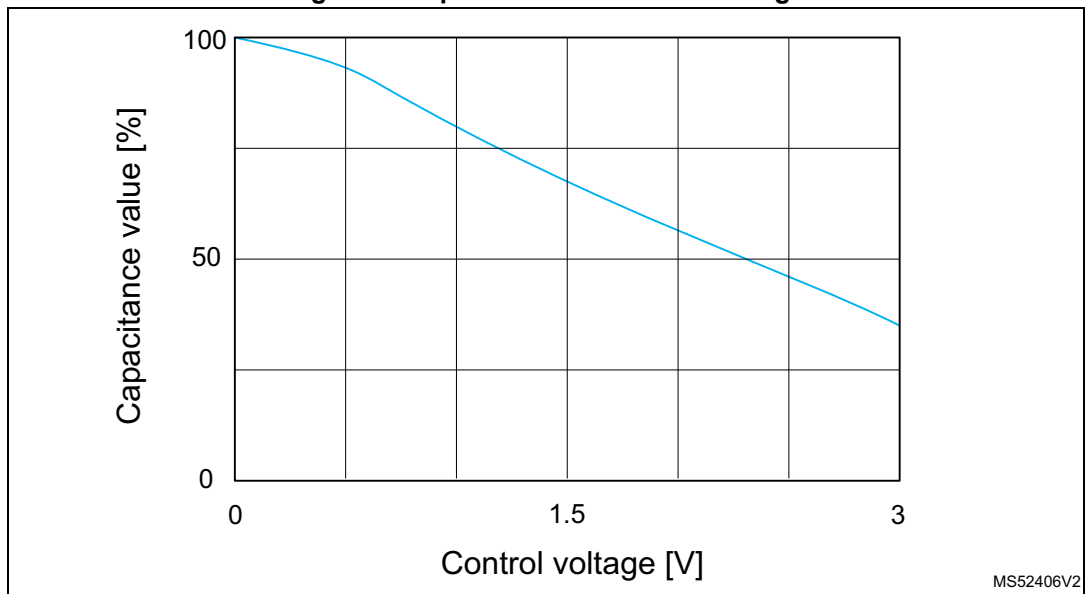
- Murata LXRW0YV201 (chosen as default configuration for the ST25R3916-DISCO)
- STMicroelectronics STPTIC-0N200, whose scheme is shown in [Figure 2](#).

Figure 2. STPTIC-0N200 scheme



Usually the tuning range is between 100 and 50 or 35% of the capacitance value (corresponding, respectively, to a control voltage of 0 and 3 V). The relation between tuning voltage and capacitance can be estimated as linear, but a closer look at the VCC datasheet reveals that it is more complex. [Figure 3](#) shows the relation between capacitance and control voltage for the STMicroelectronics device.

Figure 3. Capacitance vs. control voltage



Due to the internal circuitry of the VCC device, a change in the control voltage results in a delayed change of the capacitance value. The delay is device dependent, and is typically comprised between 1 and 10 ms. This behavior must be considered when controlling the VCC dynamically by software.

3 Second and third harmonics

Another side effect of the internal structures of the VCC device is third harmonic generation. The third harmonic magnitude depends upon two factors, namely the AC voltage across the capacitance pins and the control voltage applied to the VCC device.

Figure 4 shows the correlation between the radiated third harmonic and the parallel VCC control voltage. The measurements have been carried out using the default configuration shown in *Figure 10*. Step by step fixed capacitors have been added in parallel to the VCC. To keep the same matching impedance, the control voltage of the VCC has been increased, therefore the overall parallel capacitance of the matching circuit remains the same.

Figure 4. Third harmonic vs. parallel VCC control voltage

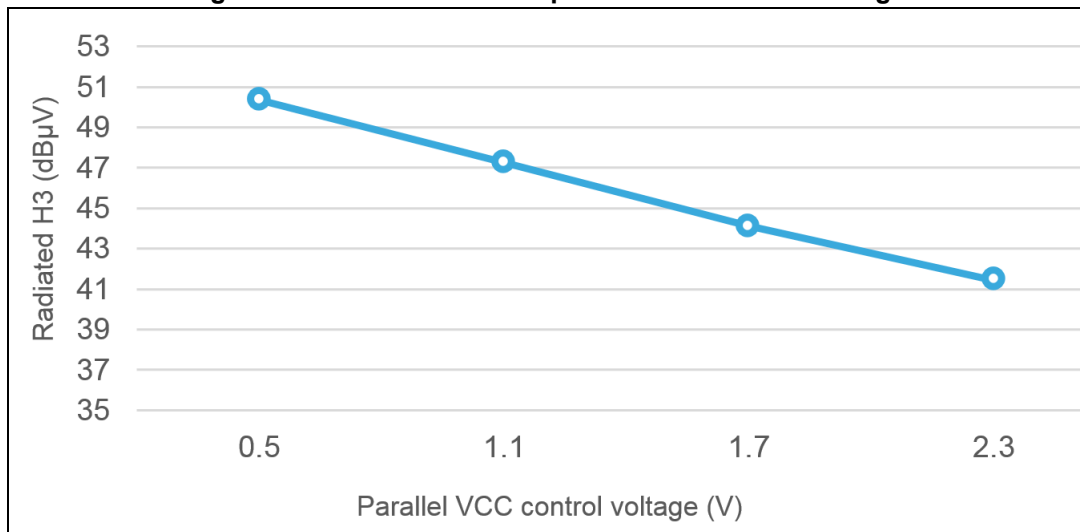


Figure 5 shows the relation between driver supply voltage (V_{DD_RF}) and occurrence of the fundamental, second and third harmonic. The VCC control voltage has been kept constant for this measurement. The driver supply has been changed from 4.5 to 3.6 V. The fundamental wave slightly drops while reducing the supply voltage, a significant drop of the second and third harmonic can be seen on the DUT using VCC devices (dashed lines).

Figure 5. Harmonics vs. driver supply voltage

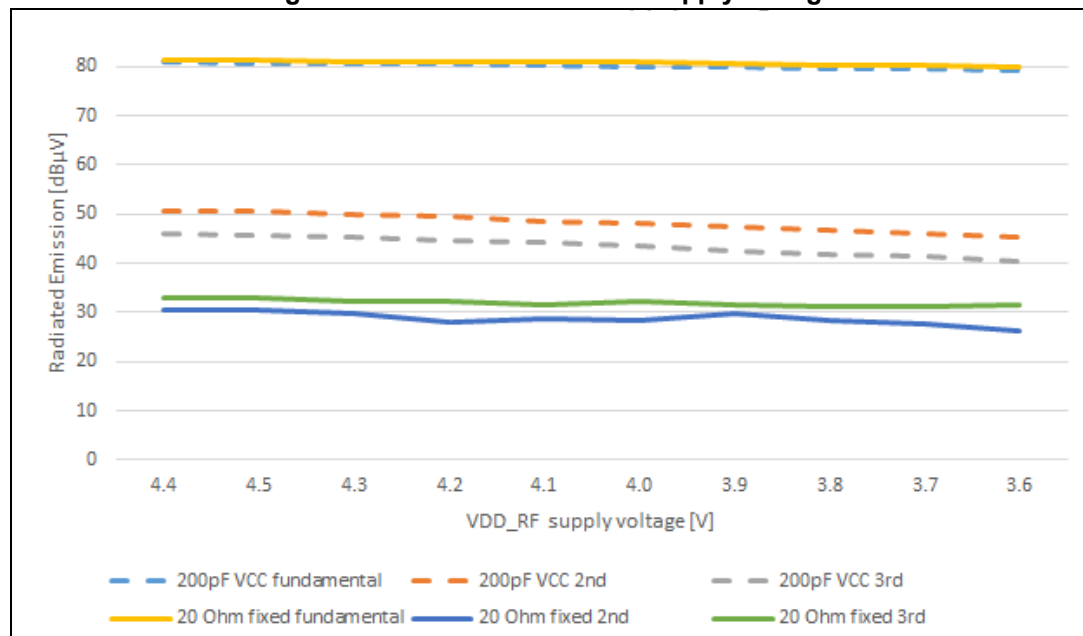


Table 1 details some of the results shown in Figure 5. The schematic with 200 pF VCC capacitor (blue dotted line) shows a fundamental wave drop of -1.6 dBμV along the variation of V_{DD_RF} . The schematic without VCC devices and a fixed matching of 20 Ω shows a similar drop of the fundamental wave. The drop for the second and the third harmonic is significantly larger when using VCCs.

Table 1. Measurement data harmonics (dBμV) vs. driver supply voltage (V)

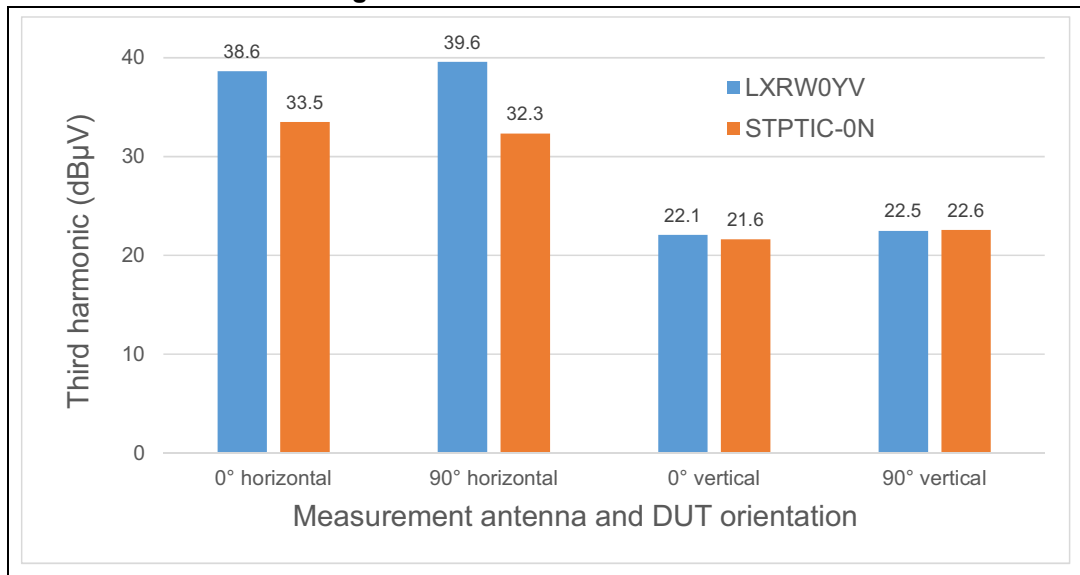
V_{DD_RF}	200 pF VCC			20 Ω fixed		
	Fundamental	Second	Third	Fundamental	Second	Third
4.5	80.8	50.6	45.9	81.2	30.5	32.9
4.0	80.0	48.2	43.4	80.8	28.5	32.3
3.6	79.2	45.4	40.4	79.9	26.3	31.4

The data shown in Table 1 and Figure 5 illustrate that the second and third harmonic are higher when using VCC devices. This fact has to be considered during the design process. The amount of second and third harmonic generated by the VCC device can be requested to the manufacturer.

4 Harmonics comparison

[Figure 6](#) shows the comparison between Murata LXRW0YV and STMicroelectronics STPTIC-0N, carried out with the default schematic ([Figure 10](#)). Fixed MLCC capacitors are added in parallel to the four VCCs to have the same target matching impedance of $18\ \Omega$ with STPTIC-0N and LXRW0YV devices.

Figure 6. STPTIC-0N vs. LXRW0YV



Both tested configurations have the same control voltage applied on series and parallel capacitors. The control voltage of the parallel capacitor has been set to approximately 2.25 V. A difference of approximately 6 dBμV is measured when the measurement antenna is parallel to the DUT antenna.

5 AAT implementation using variable capacitors

Typical values (C_{Max} to C_{Min}) are in the 200 to 75 pF, 100 to 35 pF and 50 to 20 pF ranges.

The ideal tuning range depends on the chosen antenna SFR and application. Higher antenna SFRs need bigger parallel capacitors to tune the antenna to 13.56 MHz.

The ST25R antenna matching tool (STSW-ST25R004, available on www.st.com) can be used to calculate the matching component values based on the measured antenna parameters. The process of matching the NFC antenna using this tool is described in AN5276, available on www.st.com. The latest version of the matching tool supports also topologies including AAT.

In [Figure 7](#) the matching network is calculated without including variable capacitors, while in [Figure 8](#) some static capacitors have been replaced with variable ones.

Figure 7. Example of calculation without variable capacitors

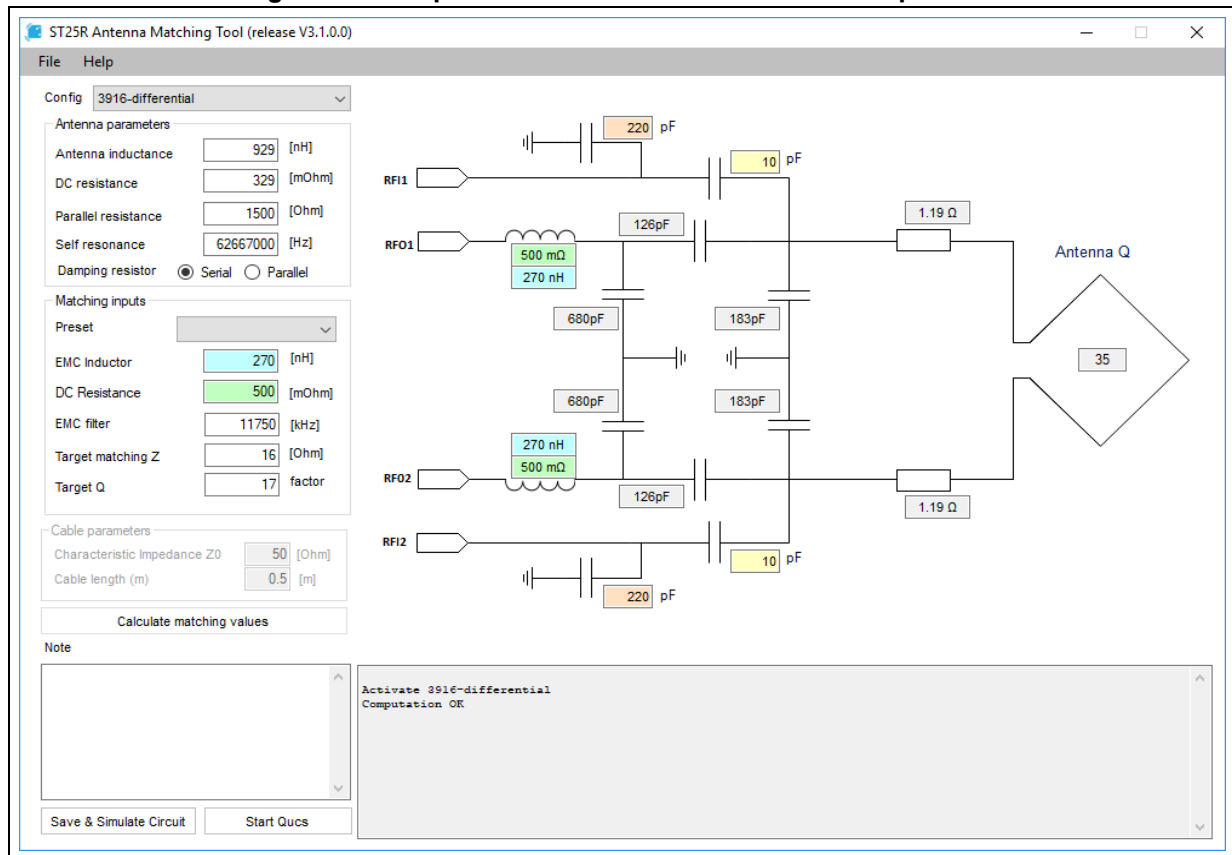
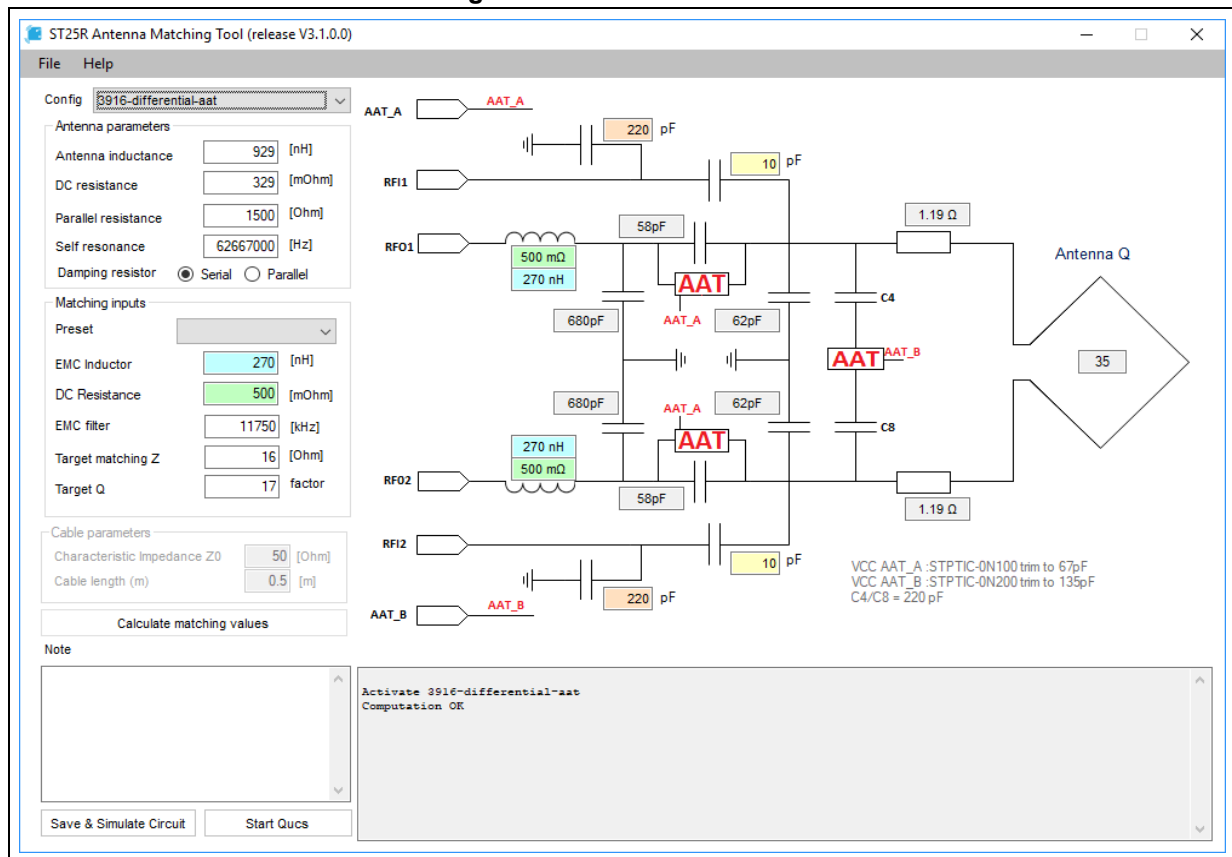


Figure 8. Three VCCs circuit



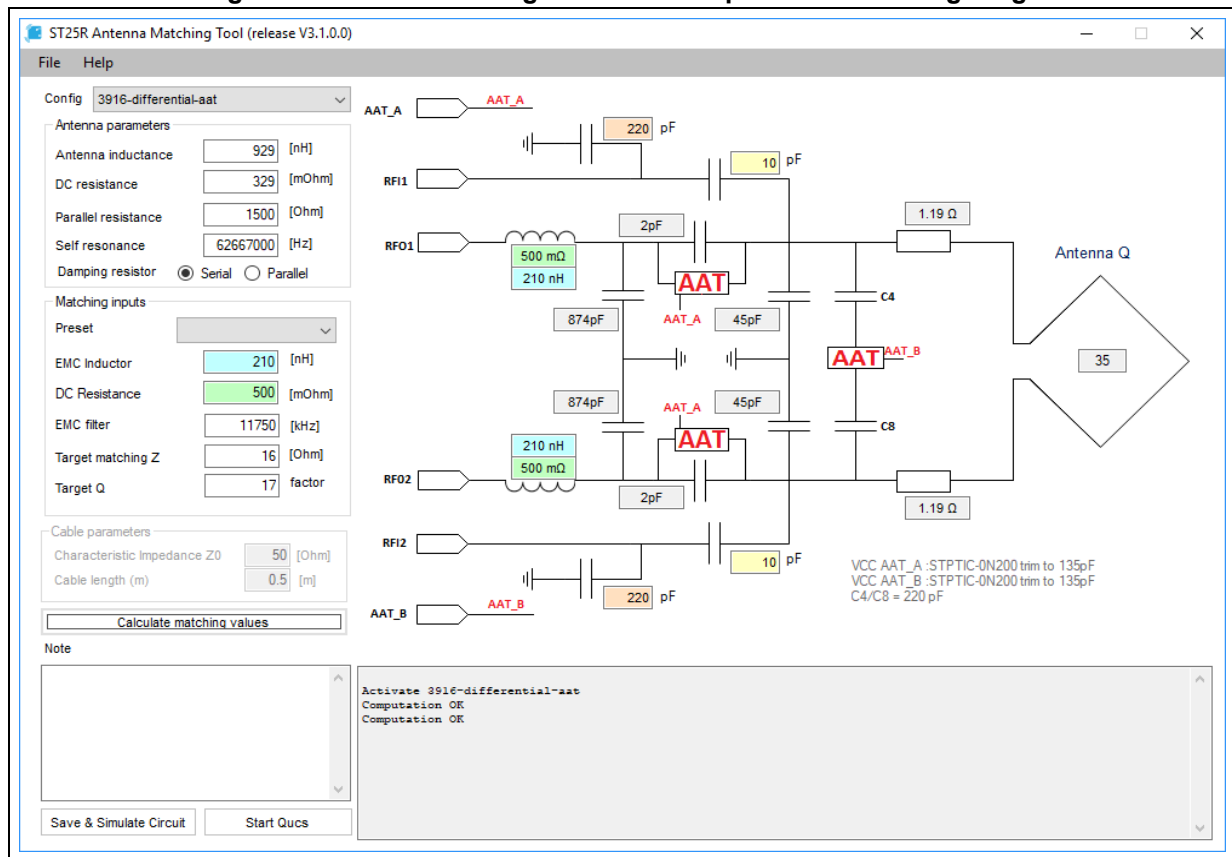
The tool automatically chooses one of the typical varicaps assuming to use its mid value achieved at 1.5 V DAC control voltage (135, 67.5 or 34 pF).

In [Figure 8](#) it has chosen STPTIC-0N200 as parallel capacitor, with an approximate mid-point of 135 pF, and has added Cp1 (62 pF) to achieve an overall parallel capacitance of 183 pF. C4 and C8 have been considered as 220 pF MLCC capacitors.

Changing the EMC inductor value without changing the EMC cutoff frequency can move the required series capacitance value to a more suitable region.

For the example shown in [Figure 6](#) it is possible to move the target matching impedance at the center of the VCC tuning range by changing the EMC inductor from 270 to 210 nH.

Figure 9. Default matching circuit with improved AAT tuning range



The calculated series capacitor value is close to 135 pF, exactly the middle of a 200 pF VCC tuning range. The tool calculates a theoretical 2 pF for Cs1, which can be neglected.

6 VCC tuning range

The tuning range or type of VCC is selected by the application. Larger environmental changes require a wider tuning range, while for fine tuning only a small tuning range is suitable. [Figure 10](#) shows the tuning range of a 200 pF parallel VCC (the control voltage of the parallel VCC is set to 0 / 3 V, respectively, for the maximum / minimum capacitance).

Figure 10. Example of AAT schematic

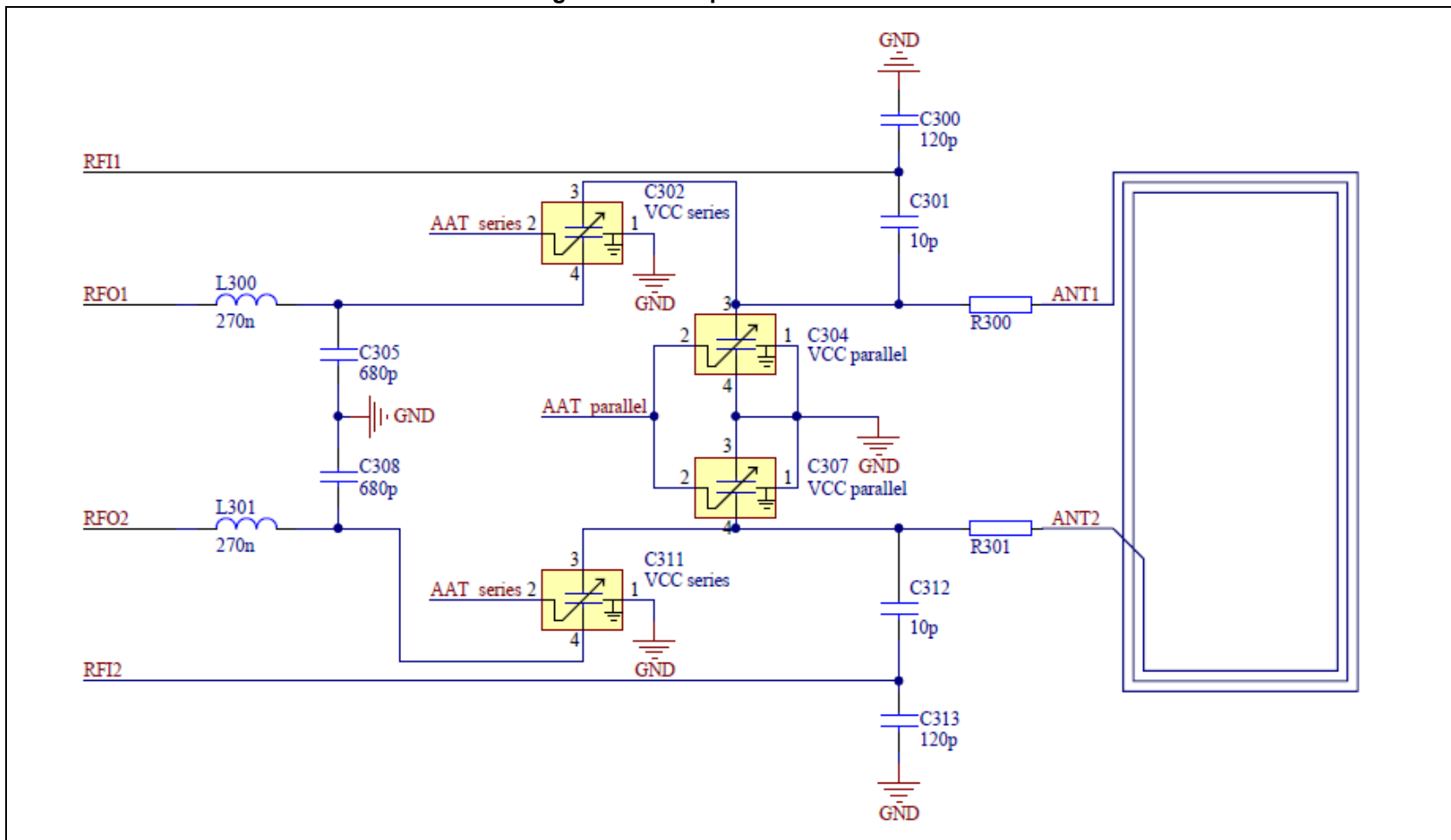


Figure 11 and Figure 12 show, respectively, the maximum and the minimum VCC capacitance, The antenna is resonating, respectively, below and above 13.56 MHz.

Figure 11. Maximum tuning capacitance

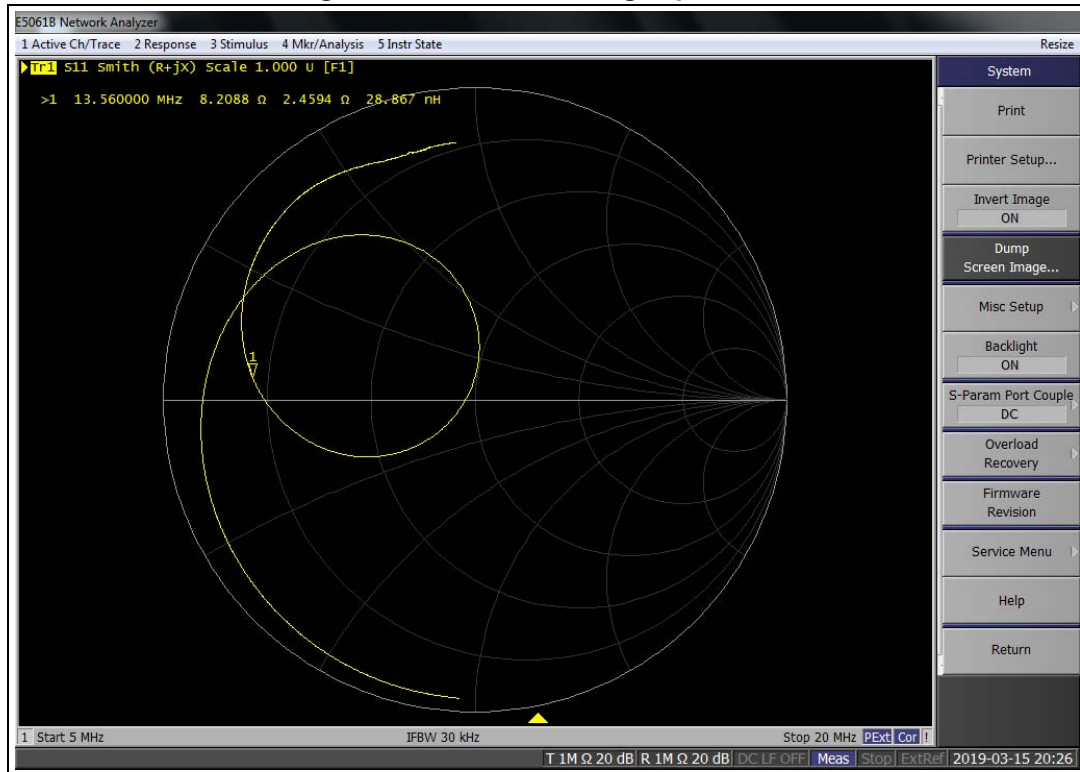
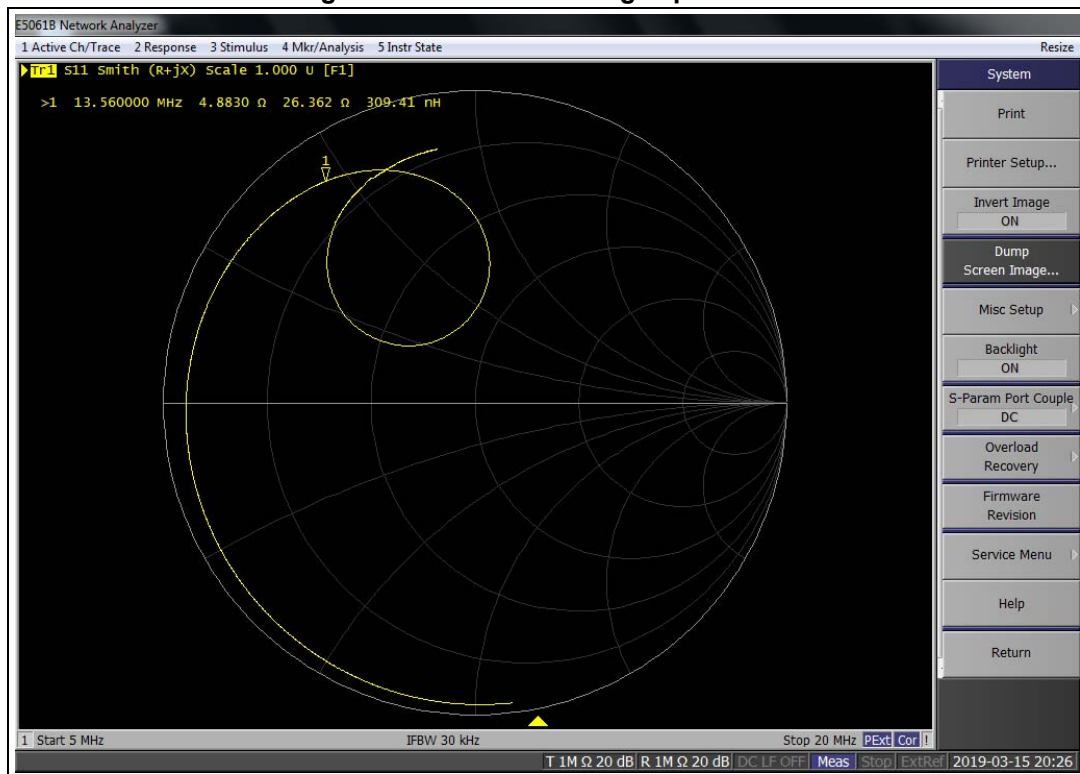


Figure 12. Minimum tuning capacitance



Both series and parallel VCCs have been changed. The series VCC changes the diameter of the resonance circle, it can be used to compensate losses and damping. The parallel VCC changes the antenna resonance, it can be used to tune the resonance frequency of the NFC antenna and therefore compensate detuning by conductive objects.

To limit the above-mentioned generation of second and third harmonic the default control voltage must be in the upper range of the 1.5 to 3 V VCC control voltage. Additional MLCC capacitors (C4, C8) are used to limit the AC antenna voltage applied to the capacitors and thus reduce the third harmonic.

The schematics in [Figure 13](#) and [Figure 14](#) are proposed to reduce the voltage across the VCCs.

Figure 13. Three VCC schematic

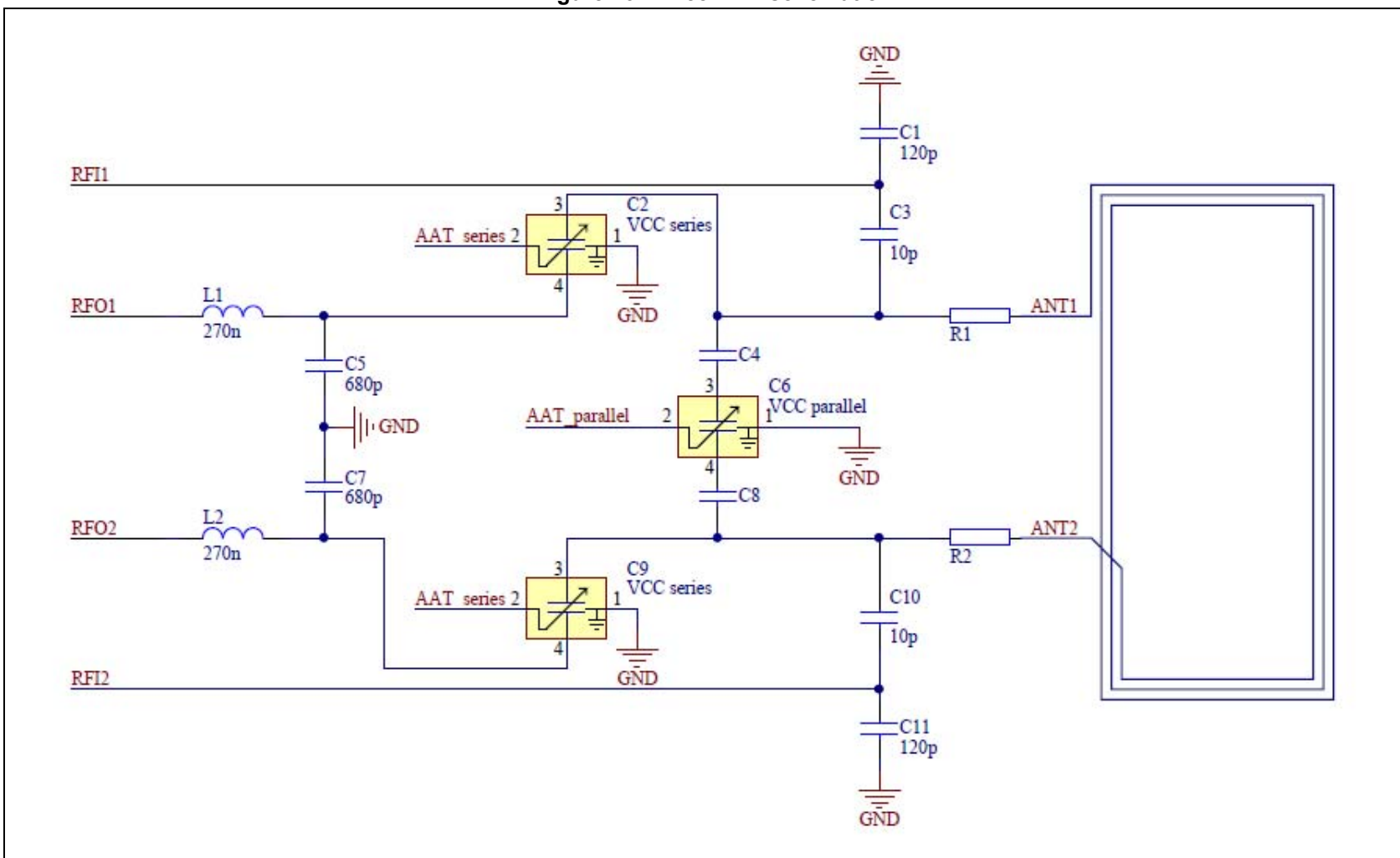
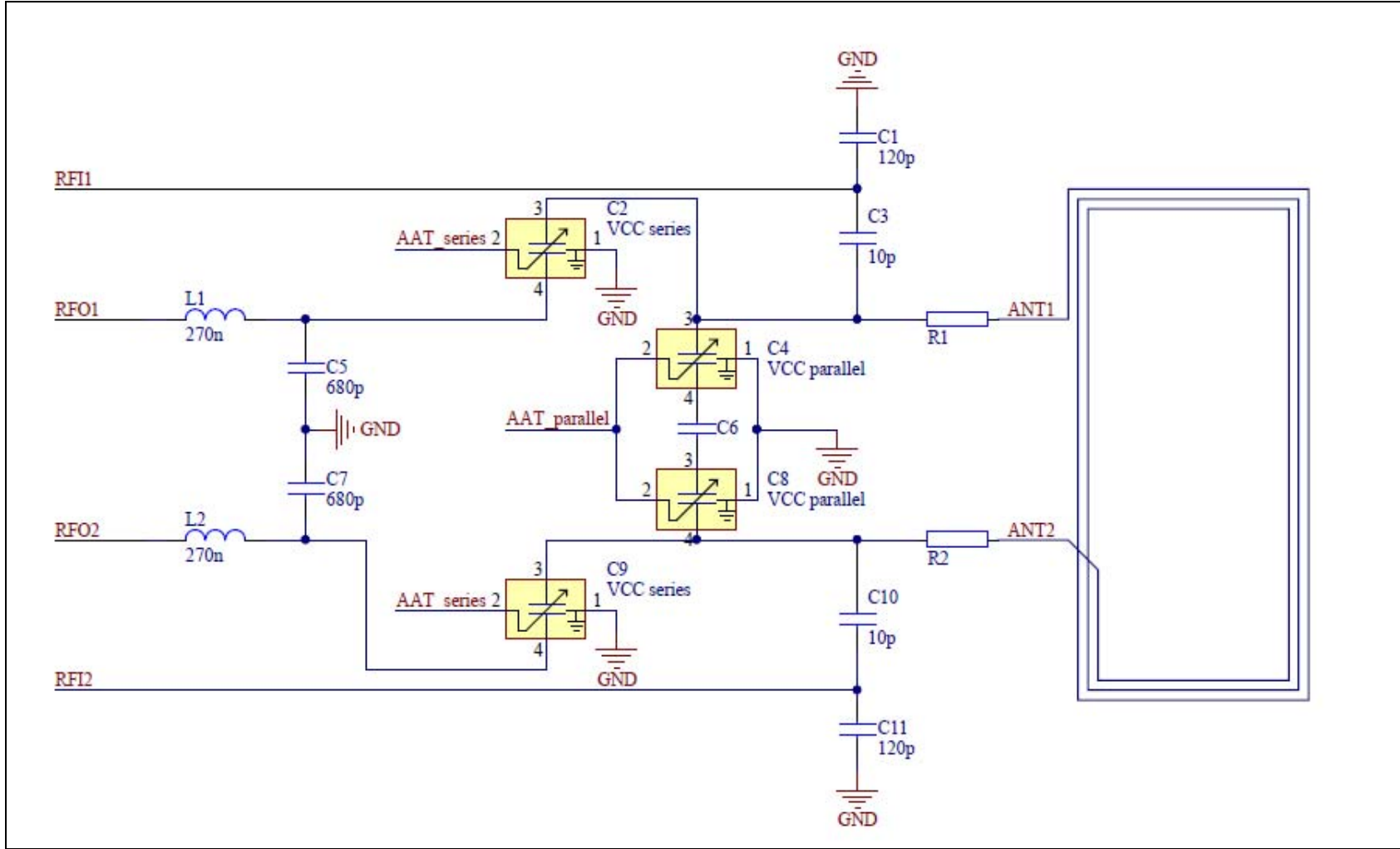


Figure 14. Four VCC schematic



Each of the these schematics has some advantages:

- the default one offers the biggest tuning range but sees the highest AC voltage across the VCC device
- the one using three VCC devices is more cost-oriented but has a reduced tuning range
- the schematic with four VCC devices offers a larger tuning range, and the AC voltage across the antenna is better distributed over the two VCC devices and the MLCC capacitor.

The tuning range can be calculated as series connection of the parallel capacitors, C_{Min} and C_{Max} values are summarized in [Table 2](#).

Table 2. Tuning range comparison

Schematic		C_{Max} (pF)	C_{Min} (pF)	Delta (pF)
Four VCCs without additional MLCs (Figure 9)		100	37.5	62.5
Three VCCs (Figure 13)	$C4 = C8 = 220$ pF	71.0	44.6	26.4
Four VCCs (Figure 14)	$C6 = 220$ pF	68.8	32.0	36.8

The distribution of a 60 V_{pp} antenna voltage is detailed in [Table 3](#).

Table 3. Voltage distribution

Schematic		V_{cmin} (V_{pp})	V_{cmax} (V_{pp})
Four VCCs without additional MLCs (Figure 9)		30	30
Three VCCs (Figure 13)	$C4 = C8 = 220$ pF	35.7	21.3
Four VCCs (Figure 14)	$C6 = 220$ pF	25.5	20.6

7 Measuring the matching impedance

To measure the matching impedance while the board is powered it is necessary to turn off the driver stage.

Note: If the reader is powered, ensure that register 0x28 is set to 0x0F and tr_am bit is set to "1" to avoid power transfer (and therefore damage) to the VNA ports.

After turning off the driver stage, it is possible to connect the VNA in parallel to the RFO pins. The 0x26 and 0x27 register can now safely be used to change the matching impedance using VCC devices.

8 Enabling AAT in ST25R3916 PC GUI

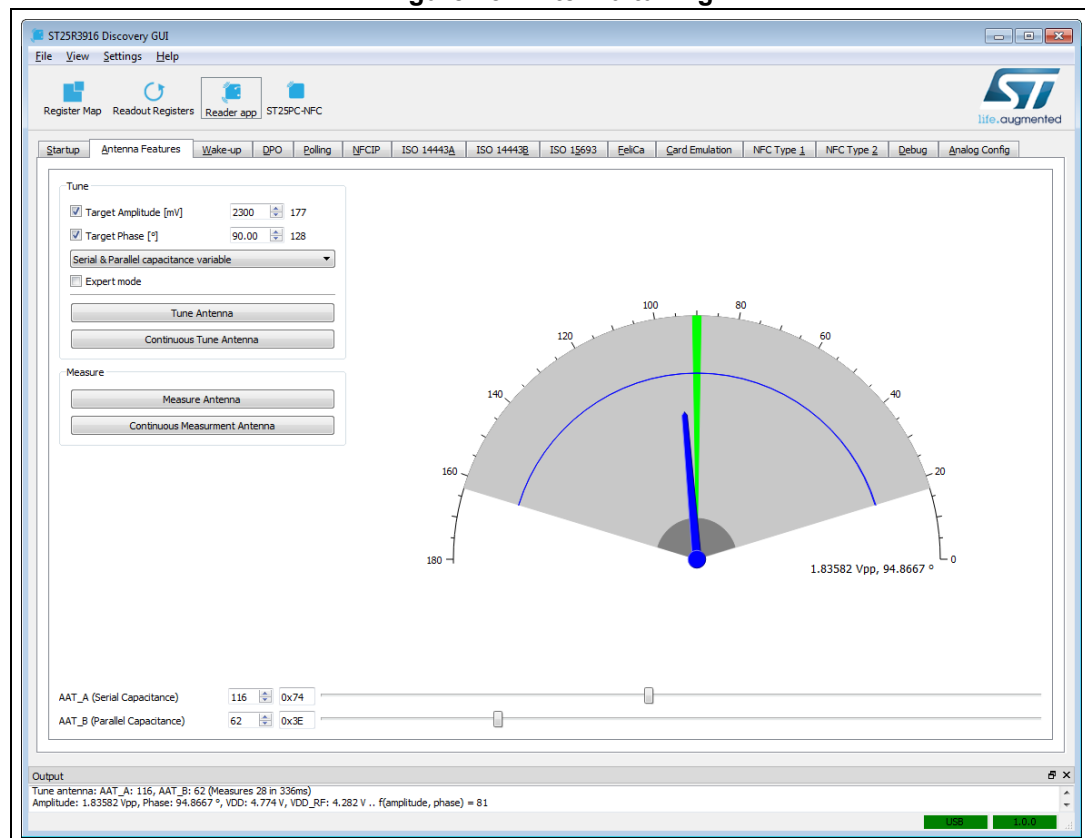
8.1 Antenna tab

Figure 15 shows the non-expert mode of the Antenna Features tab. In this tab it is possible to play either manually with the values of the AAT_A and AAT_B pins of the ST25R3916 and observe the resulting amplitude and phase, or to execute an algorithm to tune the antenna.

The most important GUI elements are:

- Serial & Parallel capacitance variable: allows the user to restrict the tuning algorithm to use also only serial or only parallel capacitance to tune to the target.
- Tune Antenna: Runs the software based algorithm in firmware. The result is presented by adjusting the two capacitance sliders and adjusting the needle in the gauge according to the measured amplitude and phase.
- Continuous Tune Antenna: performs the Tune Antenna step repeatedly and displays the results.
- Measure Antenna: performs a single measurement with the currently configured AAT_A and AAT_B and adapts the needle.
- Continuous Measurement Antenna: useful to play with AAT_A and AAT_B, and to see the effects on amplitude and phase.

Figure 15. Antenna tuning



Note: *Disabling DPO (dynamic power output) as AAT affects the deciding criteria for DPO. The user can get stuck in either High-power or Low-power DPO mode. Refer to UM2517 “ST25R3916-DISCO reference graphical user interface”, available on www.st.com for further details.*

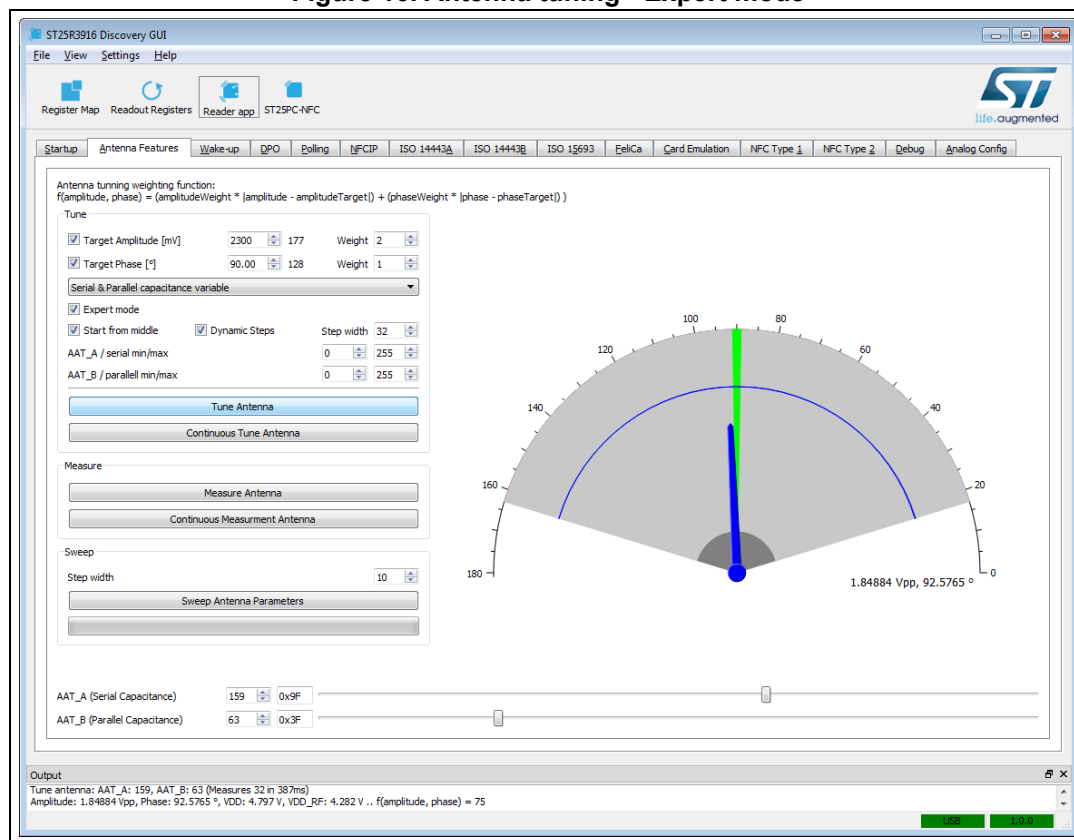
For all of these actions the log area displays additional information on measurements and tuning steps required. The performance of tuning points is evaluated using a linear function designating a weighted distance from the target values: The lower the values the better was the target reached.

When selecting the “Expert mode” additional settings can be adapted (see [Figure 16](#)).

- “Start from middle” puts the start for the algorithm always in the middle of the AAT_A, AAT_B range instead of the current AAT_A, AAT_B values.
- “Dynamic Steps” defines whether the tuning algorithm should subsequently reduce the step size if not better points are to be found.
- “Step width” defines the step size to be used, the starting step size in case of “Dynamic steps”

There are limits within which the tuning algorithm is allowed to search.

Figure 16. Antenna tuning - Expert mode



All these settings are directly transformed into parameters of the firmware based implementation described in [Section 9](#).

8.2 Analog configuration

The normal analog configurations cause AAT_A and AAT_B to be set to different static values while polling (POLL_COMMON) and while doing card emulation (LISTEN_ON), as shown, respectively, in [Figure 17](#) and [Figure 18](#) (registers 0x26 and 0x27).

Figure 17. Polling (POLL_COMMON)

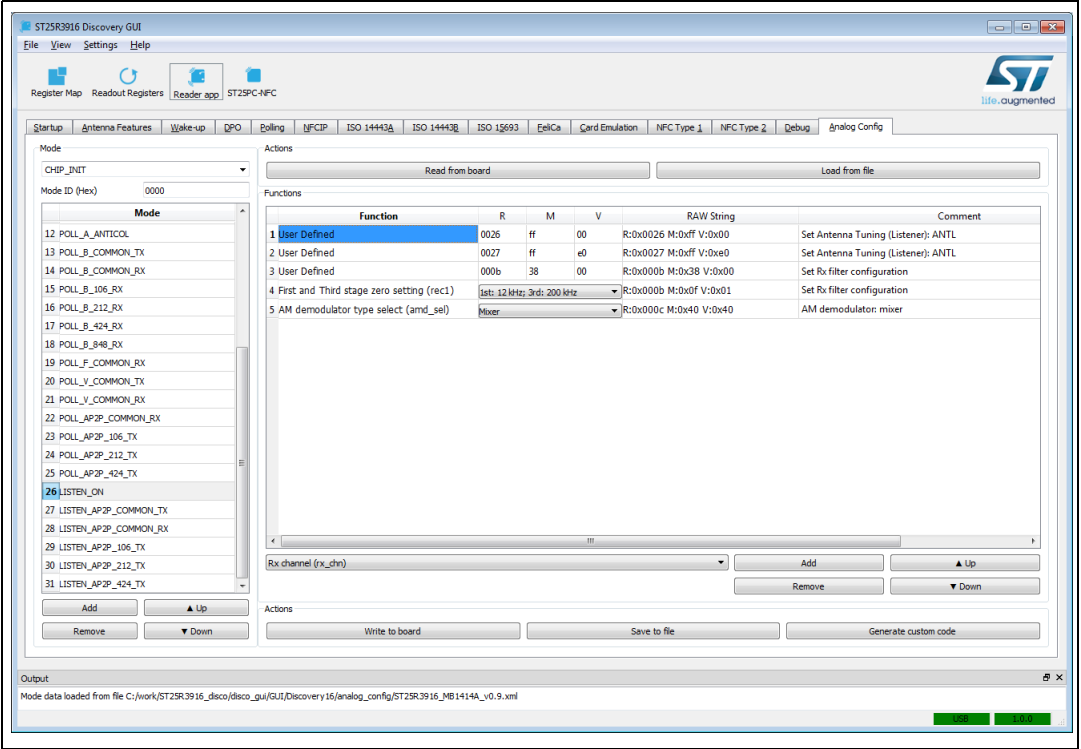
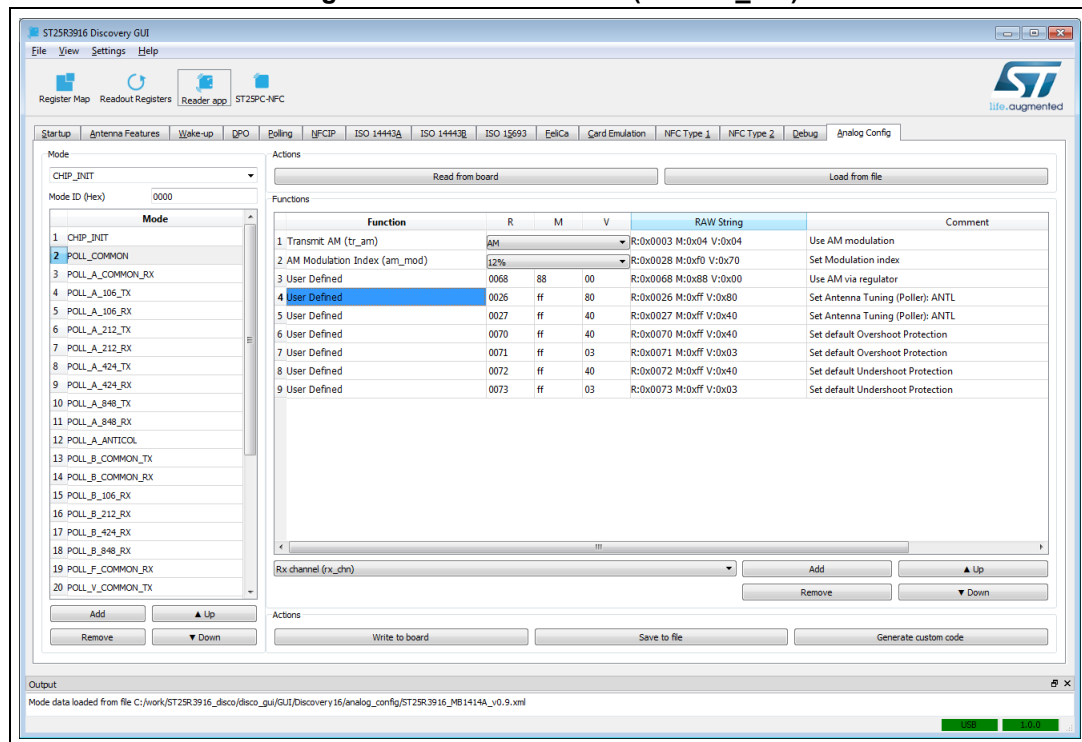


Figure 18. Card emulation (LISTEN_ON)



To see the effect of a re-tuned antenna during card communication it is necessary to remove these settings, or to load pre-built configuration files named “MB1414..._for_aat.xml” using “Load from file”.

8.3 Polling tab

Using the “Tune antenna when there are no tags” the effect of retuning can be observed. For this purpose most of the values configured in the Antenna Features tab are used.

Exceptions are:

- step size fixed to 4
- no dynamic steps
- start from current capacitances.

The GUI shows the resulting amplitude, the phase and the value of the weighted distance function in the output log.

9 Tuning algorithm

The tuning algorithm is implemented in firmware, within the `st25r3916_aat.c` file. The implemented algorithm is a steep descent / hill climb. Due to the varicap settling time (typically 2 to 3 ms) its efficiency in terms of required number of measurements is very important.

The steepest slope has been optimized to avoid redundant measurements and to perform gradual steps, without evaluating the complete environment.

The main parameters of the algorithm are the following:

```
struct st25r3916AatTuneParams{
    uint8_t aat_a_min;           /*<! min value of A cap */
    uint8_t aat_a_max;           /*<! max value of A cap */
    uint8_t aat_a_start;         /*<! start value of A cap */
    uint8_t aat_a_stepWidth;     /*<! increment stepWidth for A cap */
    uint8_t aat_b_min;           /*<! min value of B cap */
    uint8_t aat_b_max;           /*<! max value of B cap */
    uint8_t aat_b_start;         /*<! start value of B cap */
    uint8_t aat_b_stepWidth;     /*<! increment stepWidth for B cap */

    uint8_t phaTarget;           /*<! target phase */
    uint8_t phaWeight;           /*<! weight of target phase */
    uint8_t ampTarget;           /*<! target amplitude */
    uint8_t ampWeight;           /*<! weight of target amplitude */

    bool doDynamicSteps;         /*<! dynamically reduce step size */
    uint8_t measureLimit;        /*<! max number of allowed
steps/measurements */
};
```

10 Conclusion

AAT with VCC devices offers the possibility to adapt the NFC antenna matching to optimize output power. Different use cases (like production calibration of resonance frequency or continuous retuning between polling cycles) can be covered with this approach.

The continuous retuning between polling cycles can greatly improve communication with phones in close proximity. The measurement functions available on the ST25R3916 and ST25R3920 devices together with the provided software examples give large flexibility and the possibility to implement custom tuning algorithms.

11 Revision history

Table 4. Document revision history

Date	Revision	Changes
29-Apr-2019	1	Initial release.
24-Apr-2020	2	Updated Section 2: Voltage controlled capacitors , Section 5: AAT implementation using variable capacitors and Section 6: VCC tuning range . Updated Figure 3: Capacitance vs. control voltage , Figure 8: Three VCCs circuit and Figure 9: Default matching circuit with improved AAT tuning range . Added Figure 7: Example of calculation without variable capacitors . Updated Table 2: Tuning range comparison and Table 3: Voltage distribution . Minor text edits across the whole document.
14-Sep-2020	3	Document scope extended to ST25R3920 device. Updated document title and Introduction .
03-May-2022	4	Document scope extended to ST25R3916B and ST25R3920B devices. Updated document title and Introduction .

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