SRK1001 adaptive synchronous rectification controller for flyback converter evaluation board family

Introduction

The EVLSRK1001 demonstration boards in Figure 1 are designed for the evaluation of the SRK1001 controller in flyback converters with synchronous rectification (SR) at transformer secondary side.

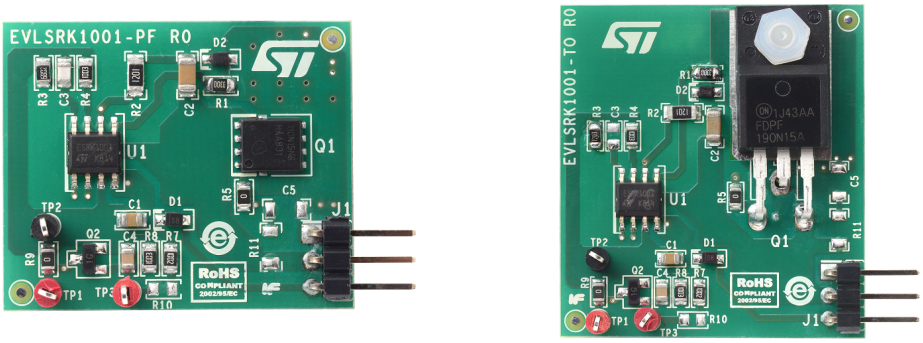
The first part of this application note describes the features of the IC along with some applicative information. The evaluation board schematics are then described and suggestions are provided on how to connect to an existing flyback converter. The document concludes with a discusion on circuit and layout optimization principles.

The PCB layout is available in two different configurations according to the mounted SR MOSFET package. The board codes are provided in the following Table 1.

Table 1. Demonstration board ordering codes

Ordering code	SR MOSFET P/N	MOSFET Package	MOSFET		Controller
			V_{DSS}	R_{DS_on}	
EVLSRK1001-TO	FDPF190N15A	TO220FP	150 V	19 mΩ	SRK1001
EVLSRK1001-PF	BSC110N15NS5	PwFlat 5x6	150 V	11 mΩ	SRK1001

Figure 1. EVLSRK1001 – SR adaptive control for flyback converter



1 SRK1001 main characteristics

Note: The values of the parameters mentioned in the following text are reported in the SRK1001 datasheet [1.]. Refer to the datasheet for more detailed device operation information.

The SRK1001 SR controller implements a control scheme that is specific for secondary-side synchronous rectification in flyback converters, suitable for the operation in QR and mixed CCM/DCM. It provides a high-current gate-drive output capable of directly driving the N-channel power MOSFET.

This IC turns on the SR MOSFET as soon as it senses the current flowing through the body diode: once triggered on the falling edge of the DVS signal decreasing below the cycle comparator threshold V_{TH_A}, the SRK1001 turns on the SR MOSFET after a very short delay T_{D_On}. The controller then turns the SR MOSFET off when the current approaches zero. There are two coexisting turn-off mechanisms (whichever triggers first): the first based on an adaptive algorithm, the second on the internal timer.

The adaptive turn-off consists of a ZCD_OFF comparator, where the DVS signal is compared with an adapting threshold in such a way that, in the steady state, the measured residual conduction time of the SR MOSFET body diode after turn-off meets the target value T_{diode_off}.

In steady state, the internal timer turns off the SR MOSFET with a fixed T_{ant_timer} anticipation time with respect to the first rising edge of the DVS signal (above the V_{TH_A} threshold), based on the duration of the previous switching period in case of fixed frequency CCM operation, or of the previous demagnetization time in case of QR operation.

SRK1001 controller starts operation when the VCC pin voltage exceeds the turn-on threshold V_{CC_On}; then it stops operation when the V_{CC} voltage drops below the turn-off threshold V_{CC_Off}.

In order to ensure SR switching even with low V_{CC} supply voltage, as in the case of chargers operating in CC regulation, the device is provided with the VAUX pin. When the VCC pin voltage decreases below the threshold $V_{CC\_SO\_On}$ (> V_{CC_Off}), an internal switch is turned on. This allows the capacitor on the VCC pin to be charged up to the V_{CC_On} turn-on threshold by a current drawn through the VAUX pin, which may for example be connected to the rectified SR MOSFET drain voltage or to another auxiliary voltage of the flyback transformer.

For maximum flexibility in all kinds of applications and to overcome noise and ringing problems that may arise after turn-on and turn-off events, the SRK1001 allows users to program the blanking time after turn-on and after turn-off by means of two resistors connected from the TON pin to ground and from the TOFF pin to ground, respectively.

The device enters the low consumption mode when it detects primary controller burst-mode operation or when the SR MOSFET conduction falls below the programmed minimum T_{ON}. This improves converter efficiency at light-load, where synchronous rectification is no longer beneficial.

After the converter restarts switching or the IC detects that the current conduction in the rectifiers has increased 20% above the minimum T_{ON} programmed value, the IC exits low consumption mode and resumes normal switching operation.

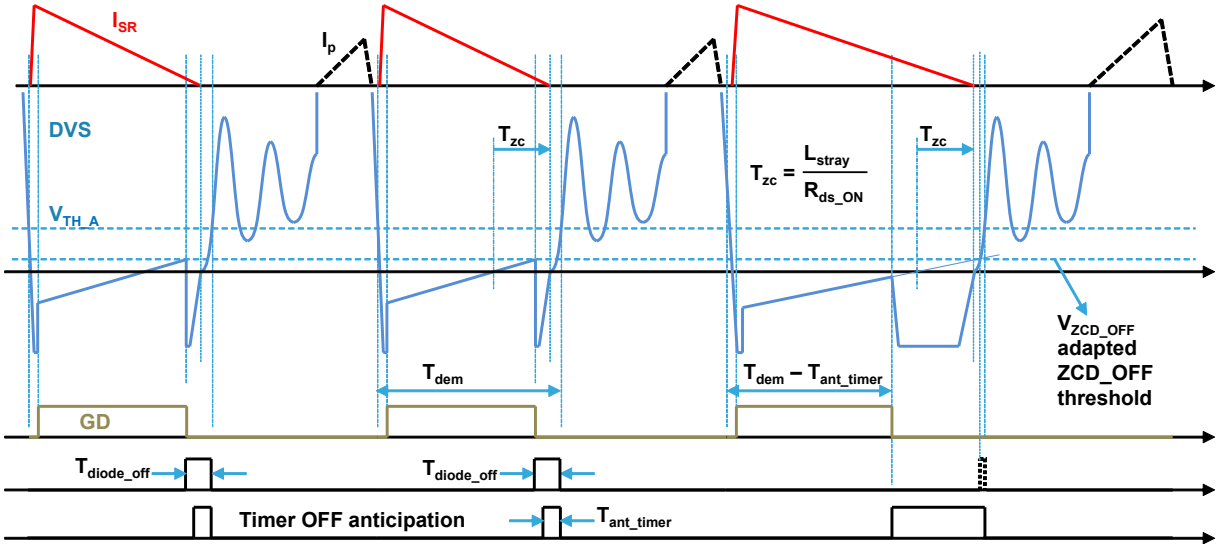
1.1 QR and FF operation

As already mentioned, the controller can operate both in quasi-resonant applications and in fixed frequency (FF) mixed DCM-CCM applications. For each of these two operating modes, the SRK1001 internal timer needs to be differently for correct operation. For this purpose, the user can select the proper timer mode through an external capacitor on the TON pin, whose presence is detected during the pinstrap phase at device start-up:

- for QR operation: no capacitor mounted on TON pin
- for FF mixed DCM-CCM operation: 100pF capacitor mounted on TON pin

The timer operation in QR application is configured so that during the current cycle it provides a turn-off with an anticipation T_{ant_timer} with respect to the duration of the demagnetization time in the previous cycle. This is illustrated in Figure 2 below.

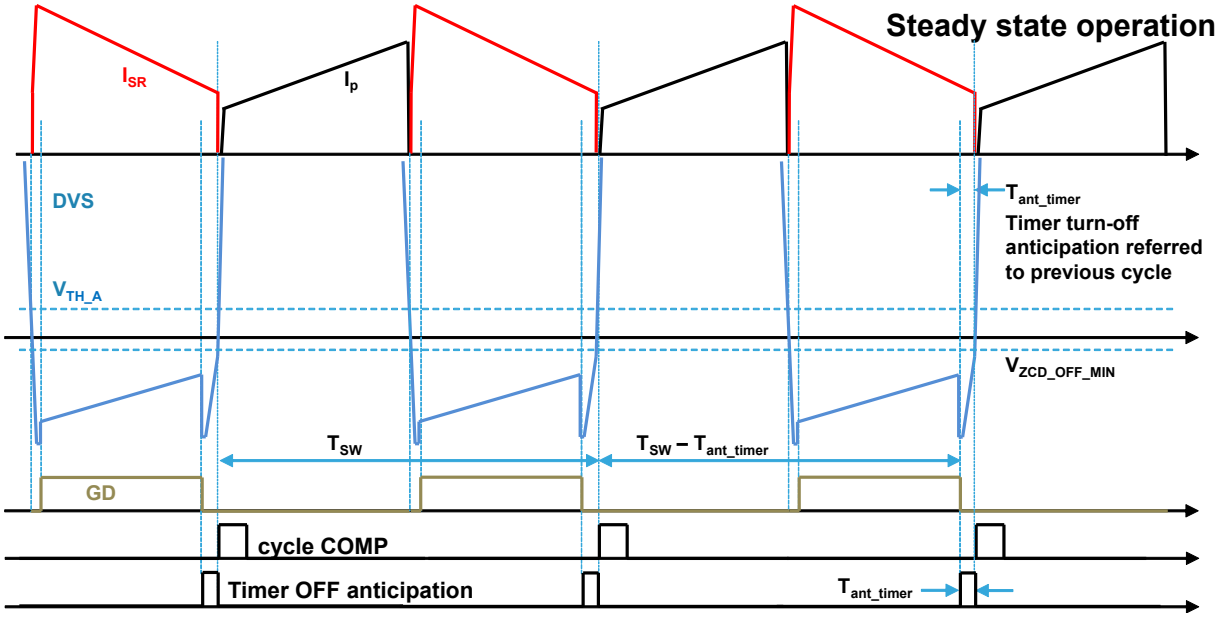
Figure 2. **Timer turn-off in QR applications**



Suppose the circuit is in steady state condition and the adaptive threshold of ZCD comparator is adapted (i.e., the residual conduction of the body diode is T_{diode_off}, while the ZCD comparator accomplishes the turn-off). In this condition, the timer is also ready for the turn-off: if T_{dem} is the steady state demagnetization time in the cycle on the left of Figure 2, in the subsequent cycle, the timer would turn off with a delay of $T_{dem} - T_{ant\_timer}$ after the DVS signal falls below V_{TH_A}. In this steady state condition, the ZCD turn-off always anticipates the timer turn-off, (since $T_{diode\_off} > T_{ant\_timer}$ is always true). If a low-to-high load transition occurs and the demagnetization time increases (due to a sudden output voltage decrease) as in the last cycle of Figure 2, the ZCD turn-off would be too late (as the ZCD adapted threshold remains unchanged): in this case, the timer will accomplish the turn-off, thus avoiding undesired current inversion.

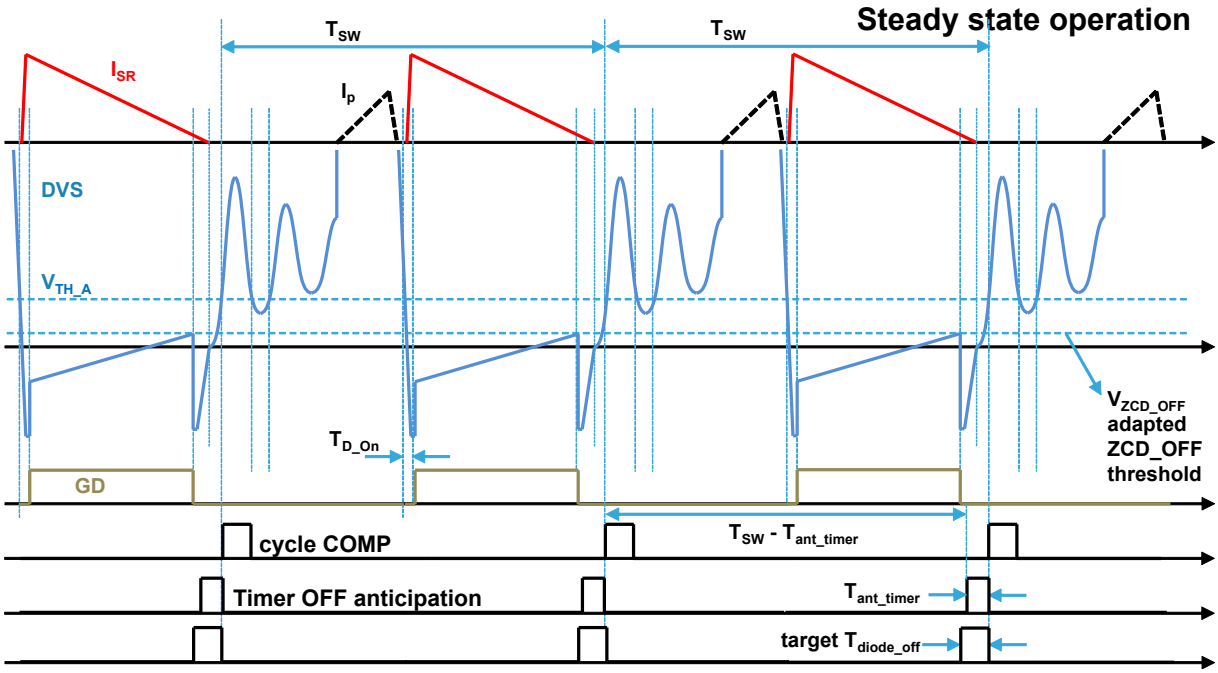
During fixed frequency mixed CCM-DCM operation, the timer is set in such a way that in the current cycle it provides a turn-off with an anticipation T_{ant_timer} with respect to the duration of the complete switching period detected in previous cycles. This is illustrated in Figure 3 and Figure 4 below for CCM and DCM, respectively: in both cases, the switching period start is detected at the first rising edge of the DVS signal above the V_{TH_A} threshold by the cycle comparator (in the case of DCM, the ringing after demagnetization is filtered by the blanking time after turn-off).

Figure 3. **Timer turn-off in FF applications (CCM)**



In full CCM steady state operation, the timer always manages the turn-off; in this condition, the adaptive comparator cannot trigger as the DVS signal is always lower than the $V_{ZCD\_OFF\_MIN}$ minimum (adapting) threshold of the comparator.

Figure 4. **Timer turn-off in FF applications (DCM)**

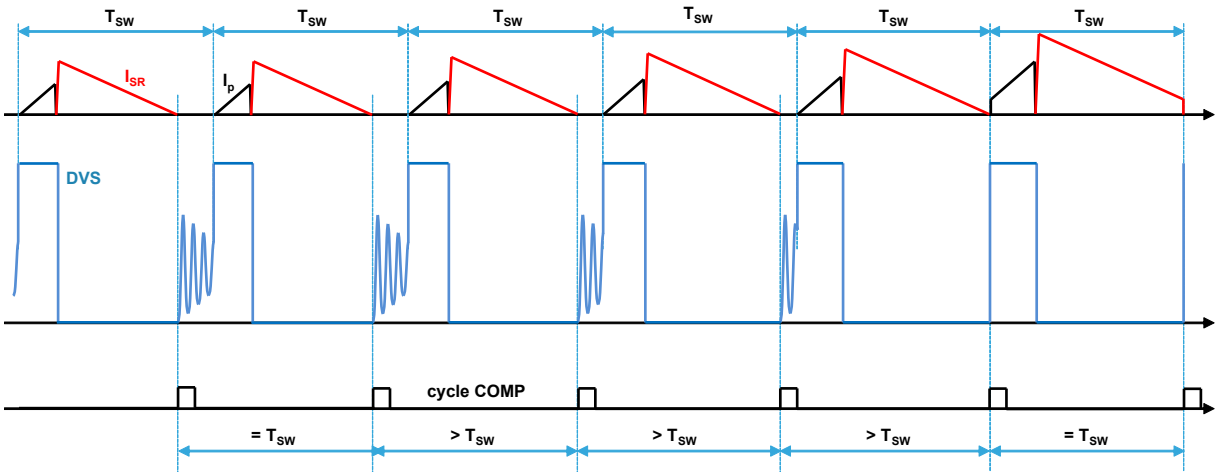


On the other hand, in fixed frequency DCM steady state, the adaptive ZCD comparator triggers the turn-off so that the target residual conduction T_{diode_off} of the body diode is met, while the timer cannot turn off as the target T_{diode_off} is longer than the anticipation time T_{ant_timer} (as in the case of QR operation).

There is a load range where the circuit still operates in CCM, but it is rather close to DCM and the DVS signal can reach the minimum ZCD comparator threshold $V_{ZCD\_OFF\_MIN}$; in this load range, there is some interaction between timer turn-off and adaptive turn-off.

During a load transition low-to-high, where the operation passes from DCM to CCM, the switching period detected by the cycle comparator increases from the current to the next cycle (though the real switching frequency set by the primary controller remains constant). Referring to Figure 5, this happens because the high-impedance period (during the ringing after demagnetization) progressively decreases, while the demagnetization time increases (due to the higher energy request resulting from the load increase). If the period is sensed as increasing cycle by cycle, the timer should update accordingly. After some cycles, however, the transition ends and the sensed period suddenly reduces to the real switching period. Therefore, a current inversion event would have occured if the timer had been progressively updated each cycle. In this phase, the ZCD comparator is also adapting the threshold from the level appropriate for DCM operation to the level for CCM and would therefore not be in time to turn off.

Figure 5. Cycle COMP period detection during low-to-high load transition



To avoid current inversions in these transitions, the SRK1001 does not update the timer every cycle, but once every four cycles in which a period increase is detected; in addition, the turn-off delay increase in the fourth cycle is limited to maximum T_{timer_step}.

There is an impact of this slower adaption of the timer in applications where the switching frequency is modulated for EMI reduction. During the time interval where the modulated switching period increases, the timer update is limited to maximum T_{timer_step} every four cycles. Therefore, the maximum switching period increase from the current to the next cycle must be lower than $\frac{T_{timer\_step}}{4}$ or the timer turn-off will be progressively anticipated and body diode conduction will increase.

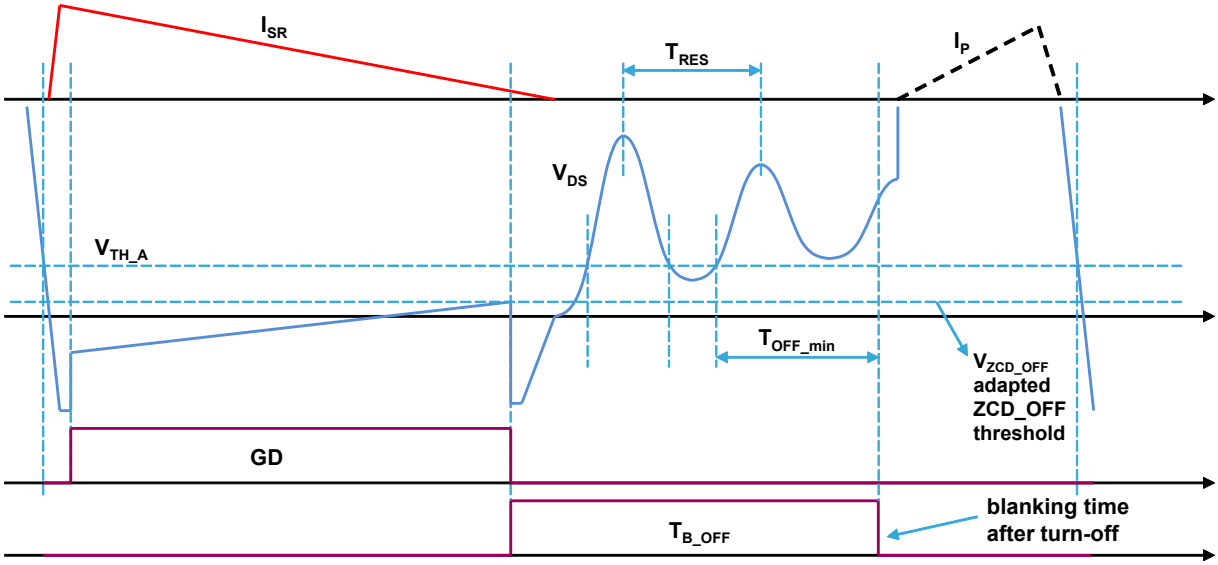
In the time interval during which the switching period begins decreasing (along the modulating frequency cycle), the SRK1001 timer update is not limited as in the previous time interval. The only requirement is that the period decrease from the current to the next cycle must be lower than T_{ant_timer}, otherwise current inversion will occur.

1.2 Blanking after turn-off

The device allows the user to program a blanking time after turn-off by means of a resistor connected from the TOFF pin to ground (refer to datasheet [1.]). The aim of the blanking time is to filter the ringing present on the DVS signal after transformer demagnetization both in QR applications and in FF applications during DCM operation, which might otherwise trigger an unwanted turn-on if the ringing voltage were to decrease below the V_{TH_A} threshold.

The blanking time filtering effect is illustrated in Figure 6, where the dumped ringing after demagnetization can cross the V_{TH_A} threshold.

Figure 6. Blanking time after turn-off

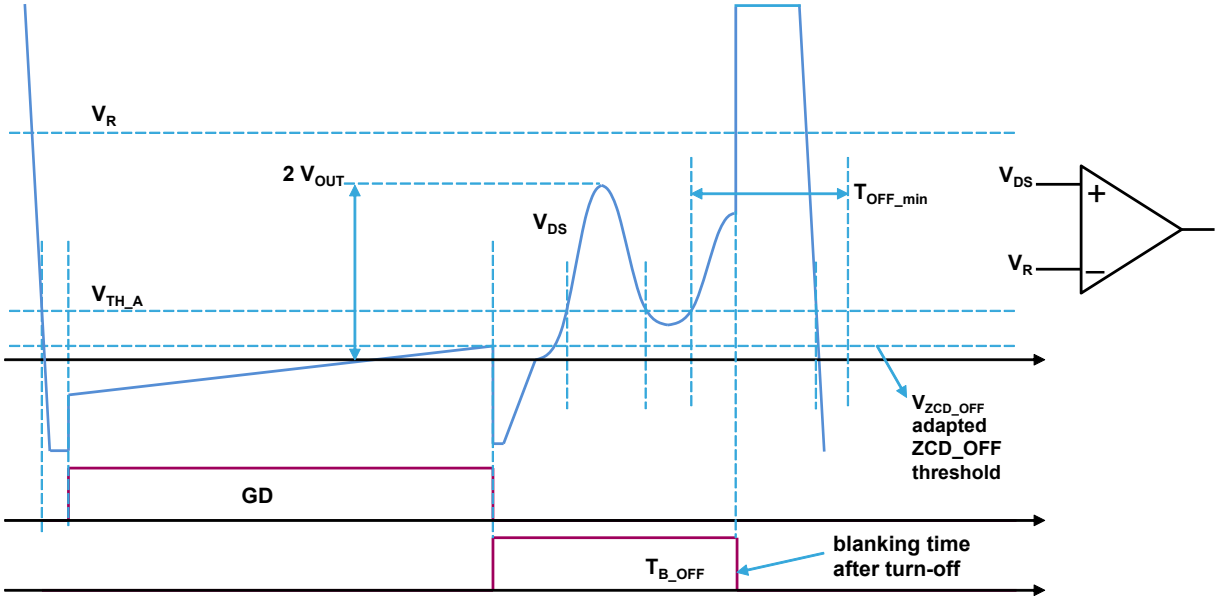


The programmed T_{OFF_min} provides a total blanking time from the SR MOSFET turn-off to the time instant occurring after the DVS ringing voltage remains permanently higher than V_{TH_A} for T_{OFF_min}. Therefore, the user has to program $T_{OFF\_min} > T_{RES}$ (the ringing period).

In some operating conditions (at reduced load and high input voltage, where the primary switch ON time T_{p_ON} is short), it may occur that the programmed T_{OFF_min} is longer than $\frac{T_{RES}}{2} + T_{p\_ON}$. In this case, the total blanking would also filter the DVS falling edge at the beginning of SR MOSFET conduction with a consequent skipping of the driving cycle. To avoid this, the IC is provided with an internal comparator referenced to the voltage $V_R = 2.83V_{out}$ and sensing the DVS signal (The V_R and DVS signals are actually scaled at comparator inputs by resistive dividers for convenience). Referring to Figure 7, when the DVS signal exceeds the threshold V_R, the blanking time after turn-off is terminated (independently of T_{OFF_min}). For correct comparator operation, the V_{out} voltage information has to be available on the VCC pin (or $V_{out} - V_F$ if VAUX functionality is used and a decoupling schottky diode is necessary from V_{out} to the VCC pin). This means that the IC needs to be supplied by the V_{out}.

The ringing after demagnetization on the DVS signal is dumped through the transformer ac resistance. Therefore, if this ringing never crosses V_{TH_A}, the user can program the shortest T_{OFF_min} (using the lowest allowed resistor on TOFF pin); in this case, the internal comparator referenced to V_R for blanking termination would not even be necessary (since T_{OFF_min} blanking will terminate in advance).

Figure 7. **Comparator for blanking time after turn-off termination**

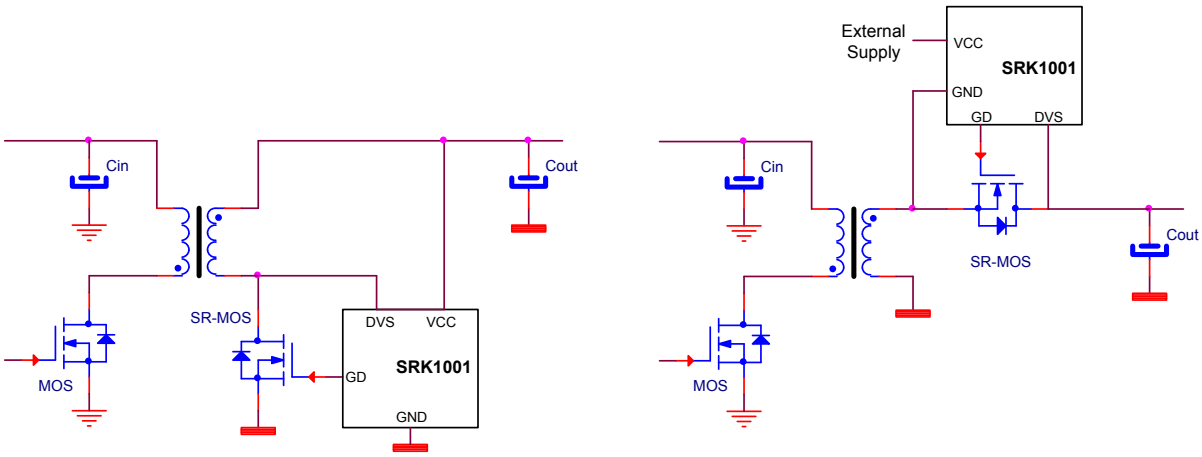


1.3 Low-side and high-side configuration

Normally, the device should be destined for applications where the SR MOSFET is mounted with the source terminal connected to secondary GND (the so called low-side configuration), which allows directly supplying the VCC pin through the output voltage of the circuit (necessary for the reasons discussed above).

In applications where the dumping effect of the transformer is such that the ringing voltage after demagnetization presents a valley voltage that never crosses V_{TH_A}, the SRK1001 with the lowest programmed T_{OFF_min} can be used, in which case a high-side configuration can also be implemented. Figure 8 shows the basic scheme of low-side and high-side configurations.

Figure 8. **Low-side and high-side configurations**



Low-side configuration **High-side configuration**

For the high-side configuration, an external supply is necessary for the SRK1001 VCC pin. This may, for example, come from a further auxiliary winding of the transformer on the secondary side, added on the top of the winding used for the output voltage. Alternatively, a charge pump can be implemented, based on the rectification of the switching waveform across the SR MOSFET drain-source.

Refer to Section 2.1 How to implement the board in the converter for further details on configurations.

1.4 TON pin programming usage

TON pin programming relates to several design aspects of the application:

Filtering

The TON pin is used to filter the noise arising after SR MOSFET turn-on by programming a blanking time (refer to SRK1001 datasheet [1.], Section: "Minimum TON programming") that prevents premature turn-off. This noise mainly depends on driver current path layout and on transformer leakage inductance.

If the driver current path is traced carefully (reducing its stray inductance and loop area), the required blanking time can be shorter. The same also occurs if the transformer leakage inductance effect is minimized through approprate transformer construction and/or by the usage of a clamp circuit across transformer primary winding. Generally, an R2CD clamp is more effective than a standard RCD clamp in these kinds of applications, as it can rapidly dump the ringing after leakage demagnetization as well as reducing EMI noise.

Sleep-mode

The TON pin also allows the user to program a minimum turn-on time to enter sleep-mode when the load is progressively reduced to a level where synchronous rectification is no longer beneficial in the specific application (refer to the SRK1001 datasheet [1.] Section: "Low consumption mode operation: sleep-mode and burst mode"). If the user prefers to use the burst-mode operation of the flyback controller in light load conditions, the minimum TON can be programmed to always be lower than the level at which the system enters burst-mode.

Adaptive gate drive

TON programming also helps reduce driving losses at reduced loads (with consequent efficiency optimization) by modulating the driver voltage high-level (refer to SRK1001 datasheet [1.], Section: "Adaptive gate drive"). This optimization can be achieved in the following way:

1. Select the minimum resistor $R_{TON.min}$ that provides a blanking time suitable to avoid premature turn-off (in all line and load conditions).
2. Check which is the minimum transformer demagnetization time while reducing the load, just before entering burst mode operation of primary controller (should be checked both at minimum and at maximum input voltage).
3. Select the maximum resistor $R_{TON.max}$ that assures SRK1001 never enters automatic sleep-mode before primary burst-mode is detected.
4. Experimentally find the R_{TON} resistor value (between $R_{TON.min}$ and $R_{TON.max}$) that optimizes efficiency at light load level (10% and 25% of load).

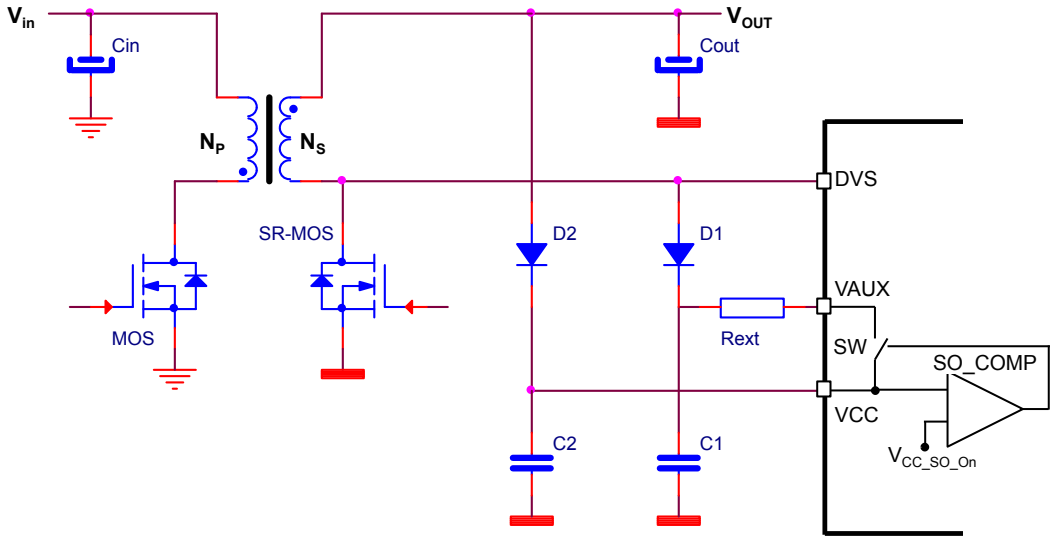
The adaptive gate driver is effective when the circuit is not operating in burst mode. Furthermore, the efficiency improvement is more pronounced in applications that operate at higher switching frequencies and use larger SR MOSFETs (i.e., with greater gate charge).

1.5 VAUX pin operation in CC regulation

In charger applications operating in CC regulation, the output voltage V_{out} (which is also used to supply the SRK1001) may considerably decrease while output current is kept constant at progressively reduced load impedance. For example, a 10 W charger, set at +5 V output in CV regulation, may be required to operate down to 2 V output while it is regulating the output current to somewhat more than 2 A in CC regulation.

In order to guarantee SR MOSFET switching even with low V_{CC} supply voltage, the SRK1001 is provided with the VAUX pin. Referring to the schematic in Figure 9, when the V_{CC} voltage decreases below the threshold $V_{CC\_SO\_On}$ (> V_{CC_Off}), an internal switch is turned on allowing the capacitor C2 placed on VCC pin to be charged up to the turn-on threshold V_{CC_On} by a current drawn through VAUX pin.

Figure 9. **VAUX supply for CC regulation operation (from rectified SR MOSFET drain)**



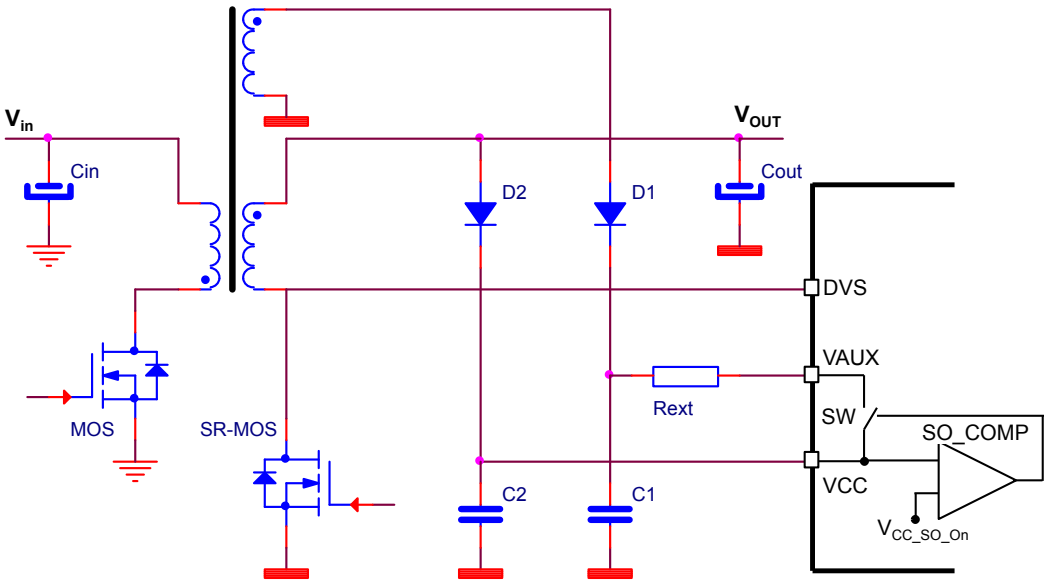
The VAUX pin may be connected, for example, to the rectified SR MOSFET drain voltage, like in Figure 9, or to another auxiliary voltage of the flyback transformer, as shown in Figure 10.

In either case, a (schottky) decoupling diode (D2) is necessary to avoid the VAUX pin charging the output capacitor. An external resistor R_{ext} may be used in series with the VAUX pin in order to externally dissipate some of the power that, without that resistor, would be totally dissipated inside the SRK1001.

1.5.1 Example for parameter calculations

Considering the circuit in Figure 9, the following example is provided to calculate the value of the R_{ext} resistor and power dissipation, in the case of a +5 V charger with operation down to 2 V in CC regulation and transformer secondary-to-primary reflected voltage of 75 V.

Figure 10. **VAUX supply for CC regulation operation from auxiliary winding**



Step 1. Measure or estimate the IC current consumption during CC regulation operation as below:

$$I_{CC} = I_{q\_run} + V_{CC\_avg}{}^{*}C_{iss}{}^{*}F_{sw} = 0.7mA + 4.1V{}^{*}5nF{}^{*}50kHz = 1.725mA$$

where I_q is the IC quiescent current, V_{cc_avg} is the average voltage across VCC pin (mean value between V_{CC_On} and $V_{CC\_SO\_On}$), C_{iss} is the SR MOSFET input capacitance and F_{sw} is the operating frequency.

Step 2. Calculate the maximum and minimum voltage available at VAUX pin:

$$V_{AUX\_min} = V_{o\,.CC} + V_{in\,.min}\left(\frac{N_S}{N_P}\right) - V_F = 2V + 75V\left(\frac{1}{15}\right) - 0.35V = 6.65V$$

$$V_{AUX\_max} = V_{o\,.CC} + V_{in\,.max}\left(\frac{N_S}{N_P}\right) - V_F = 2V + 375V\left(\frac{1}{15}\right) - 0.35V = 26.65V$$

where $V_{o.CC}$ is the output voltage in CC regulation, $V_{in.min}$ / $V_{in.max}$ is the converter minimum/maximum input dc voltage, N_S/N_P is the transformer turn ratio, and V_F is the voltage drop of D1.

Step 3. Calculate the power dissipation of SRK1001, including device consumption and driving:

$$P_{d\_CC} = V_{cc\_avg}{}^{*}I_{CC} = 4.1V{}^{*}1.725mA = 7.072mW$$

where V_{CC_avg} is the mean value between V_{CC_On} and $V_{CC\_SO\_On}$.

Step 4. Calculate the maximum external resistance in series to VAUX pin:

$$R_{ext\_MAX} = \frac{\left(V_{AUX\_min} - V_{CC\_On}\right)}{I_{CC}} - R_{on} = \frac{6.65V - 4.3V}{1.725mA} - 40\Omega = 1.322k\Omega$$

$$R_{tot} = R_{ext} + R_{on} = 1.2k\Omega + 40\Omega = 1.24k\Omega$$

where R_{on} is the resistance of the internal VAUX switch.

Step 5. Calculate the maximum and minimum current from VAUX pin:

$$I_{AUX\_min} = \frac{V_{AUX\_min} - V_{CC\_On}}{R_{tot}} = \frac{6.65V - 4.3V}{1.24k\Omega} = 1.89mA$$

$$I_{AUX\_max} = \frac{V_{AUX\_max} - V_{CC\_On}}{R_{tot}} = \frac{26.65V - 4.3V}{1.24k\Omega} = 18.02mA$$

Step 6. Calculate the maximum power dissipation from VAUX at maximum input voltage ($V_{in.max}$):

$$P_{d\_AUX} = V_{AUX\_max}{}^{*}I_{CC} = 26.65V{}^{*}1.725mA = 45.971mW$$

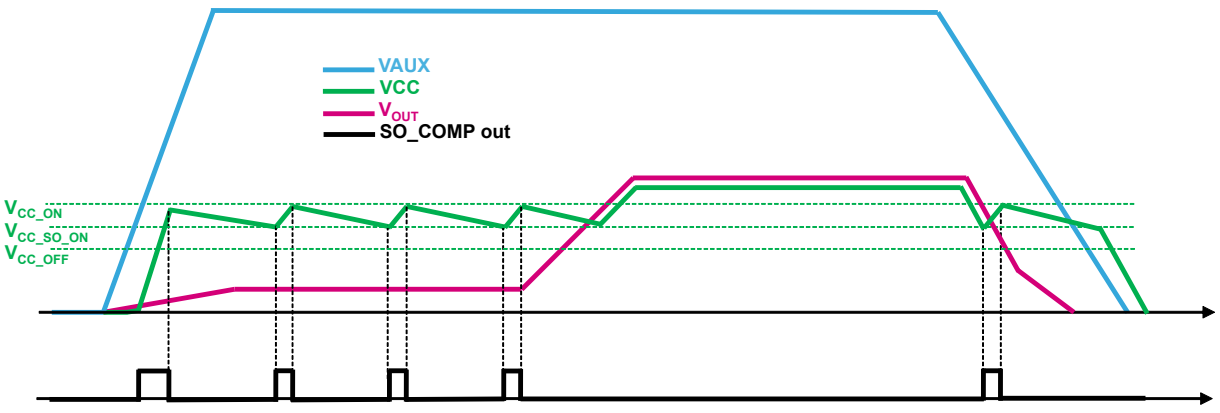
Step 7. Calculate the maximum power dissipation on external resistance and inside SRK1001:

$$P_{d\_Rext} = \frac{\left(P_{d\_AUX} - P_{d_{CC}}\right)^{*}R_{ext}}{R_{tot}} = \frac{(45.971mW - 7.072mW)^{*}1.2k\Omega}{1.24k\Omega} = 37.64mW$$

$$P_{d\_SRK} = P_{d\_AUX} - P_{d\_Rext} = 45.971mW - 37.64mW = 8.33mW$$

The following figure shows VAUX pin operation during the various circuit phases (start-up phase, CC-CV regulation and mains turn-off).

Figure 11. VAUX pin operation



2 Electrical schematic description

The board electrical schematic shown in Figure 12 refers to the generic evaluation board in Table 1. Demonstration board ordering codes (they have similar schematics, only differing in SR MOSFET part number).

The selected SR MOSFETs in the various boards are 150 V-rated devices with standard level gate and are generally intended to operate in applications with output voltage up to 20-24 V, used also to supply the SRK1001 on VCC pin.

Technical positions for an RC snubber across the SR MOSFET are provided on the PCB layout (R11-C5 not mounted) so the user can set the most appropriate values for dumping the ringing across the MOSFET drain-source and reduce its peak voltage in the particular application.

The boards are provided to operate in QR flyback application (no capacitor on TON pin). In a fixed frequency mixed DCM-CCM application, a 100 pF capacitor mounted in the technical position C3 can be used to accommodate this operating mode.

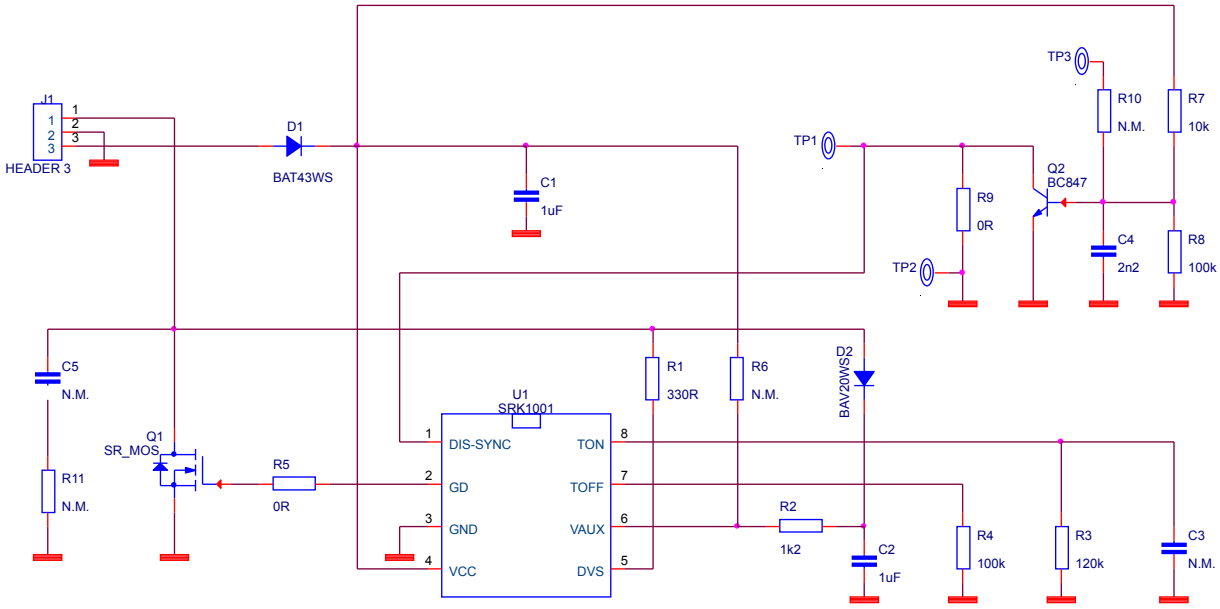
The programmed blanking after turn-on and after turn-off are 1.44 µs (R3=120 kΩ) and 3 µs (R4=100 kΩ), respectively. According to specific application needs, these can be set to appropriate values by selecting different resistor values across the TON and TOFF pins using the following relationships:

- $T_{ON\_MIN} = 12x10^{-12}.R_{TON} \rightarrow$ with R_{TON} ranging between [33 kΩ - 250 kΩ]
- $T_{OFF\_MIN} = 30x10^{-12}.R_{TOFF} \rightarrow$ with R_{TOFF} ranging between [16 kΩ - 200 kΩ]

The resistor R1 (330 Ω) in series to the DVS pin is required to limit dynamic current injections in any condition.

No resistor is required in series between the GD pin and the SR MOSFET gate terminal. The signal on the GD pin is internally used to detect on the falling edge the time instant where the body diode starts conducting (after turn-off) and a series resistor would affect the target residual conduction duration of the body diode T_{diode_off}. In any case, direct connection of the GD pin to the MOSFET gate terminal maximizes efficiency and does not affect EMI. In fact, the SR MOSFET is only turned on after the current starts flowing through the body diode, when the drain-voltage has already dropped to $-V_F$. Therefore, the turn-on just causes a voltage step from $-V_F$ to the drop across the channel resistance ($-R_{ds_{ON}}.I_{SR}$) with negligible impact on EMI. The same considerations are true also after the turn-off, where the current passes through the body diode again.

Figure 12. Board electrical schematic



The boards are provided with the VAUX pin connected to an RCD circuit (which rectifies the SR MOSFET drain-source voltage), suitable in charger applications (in order to allow operation of SRK1001 controller even when the output voltage falls during CC regulation operation).

In an adapter circuit (without CC regulation operation), the RCD circuit (R2, C2, D2) can be removed, diode D1 can be substituted with a jumper, and a zero ohm resistor needs to be added in position R6 (on the rear of the PCB) to connect the VAUX and VCC pins (required when VAUX functionality is not used).

The boards are provided with the DIS/SYNC pin connected to ground through a zero ohm resistor (R9), in order to enable device operation. Resistor R9 must be removed if the user wants to externally drive the DIS/SYNC pin for remote ON/OFF functionality. The PCB was designed to facilitate this by mounting an npn transistor (Q2) connected to the DIS/SYNC pin, which, through resistor R7 (connected to VCC), automatically enables device after start-up (by pulling down Q2). If the user wants to control the device remotely via an external signal, this can be applied to test point TP3 (by removing R7 and adding R10).

If the user needs the synchronization functionality of the DIS/SYNC pin in order to turn off the SR MOSFET in CCM operation based on a signal coming from the primary side through a pulse transformer, this signal can be applied to the DIS/SYNC pin across TP3 and TP2. Refer to the SRK1001 device datasheet [1.] for more details about the DIS/SYNC pin synchronization functionality.

The bill of material of the two EVLSRK1001 boards (in Table 2 below) are identical, differing only in the MOSFET part number.

Table 2. EVLSRK1001 Bill of Material

Ref	Value / PN	Description	Supplier	Case
C1	1µF	50V CERCAP X7R - GENERAL PURPOSE	BC COMP.	SMD 0805
C2	1µF	100V CERCAP X7R - FIEXITERM SERIES	AVX	SMD 1206
C3	N.M.	50V CERCAP X7R - GENERAL PURPOSE	-	SMD 0805
C4	2n2	50V CERCAP X7R - GENERAL PURPOSE	BC COMP.	SMD 0805
C5	N.M.	500V CERCAP COG - GENERAL PURPOSE	-	SMD 1206
D1	BAT43WS	SMALL SIGNAL SCHOTTKY DIODE	VISHAY	SOD323
D2	BAV20WS	SMALL SIGNAL FAST SWITCHING DIODE	VISHAY	SOD323
Q1	SR MOSFET	N-CHANNEL POWER MOSFET	-	-
Q2	BC847	NPN SMALL SIGNAL TRANSISTOR	VISHAY	SOT23
R1	330R	SMD STRD FILM RES - 1/8W - 5% - 250ppm/°C	BC COMP.	SMD 0805
R2	1k2	SMD STRD FILM RES - 1/4W - 5% - 250ppm/°C	BC COMP.	SMD 1206
R3	120k	SMD STRD FILM RES - 1/8W - 1% - 200ppm/°C	BC COMP.	SMD 0805
R4	100k	SMD STRD FILM RES - 1/8W - 1% - 200ppm/°C	BC COMP.	SMD 0805
R5	0R	SMD STRD FILM RES - 1/8W - 5% - 250ppm/°C	BC COMP.	SMD 0805
R6	N.M.	SMD STRD FILM RES - 1/8W - 5% - 250ppm/°C	-	SMD 0805
R7	10k	SMD STRD FILM RES - 1/8W - 5% - 200ppm/°C	BC COMP.	SMD 0805
R8	100k	SMD STRD FILM RES - 1/8W - 5% - 200ppm/°C	BC COMP.	SMD 0805
R9	0R	SMD STRD FILM RES - 1/8W - 5% - 200ppm/°C	BC COMP.	SMD 0805
R10	N.M.	SMD STRD FILM RES - 1/8W - 5% - 250ppm/°C	-	SMD 0805
R11	N.M.	SMD STRD FILM RES - 1/4W - 5% - 250ppm/°C	-	SMD 1206
U1	SRK1001	ADAPTIVE SR FLYBACK CONTROLLER	ST	SO8

2.1 How to implement the board in the converter

The evaluation board is intended to implement synchronous rectification in an existing flyback converter in the low-side configuration (i.e., replacing the output rectifier with the SR MOSFET in the configuration with the anode of its body diode connected to the secondary ground), as indicated in Figure 13. In this case, referring to connector J1 in the board schematic: pin 1 has to be connected to the transformer terminal, pin 2 has to be connected to secondary ground, while pin 3 has to be connected to the output voltage.

The evaluation board can also be used in high-side configuration (see Section 1.3 Low-side and high-side configuration). This is achieved by replacing the output rectifier with the SR MOSFET in the configuration with the cathode of its body diode connected to the output voltage, as indicated in Figure 14: pin 1 of connector J1 has to be connected to the output voltage, and pin 2 to the transformer. The VCC supply to SRK1001 has to be provided externally between pin 3 and pin 2 of connector J1 (for example, through a further transformer winding). The VCC supply can also be provided by adding some components on the evaluation board as shown in Figure 15.

In this last case, the implementation is like in Figure 14: pin 1 and pin 2 of connector J1 are soldered to the board, while pin 3 remains unconnected. The further components required for VCC supply highlighted in Figure 15 have to be added by rework (there is no technical position foreseen on PCB).

Figure 13. Implementing the board on existing flyback converter (low-side configuration)

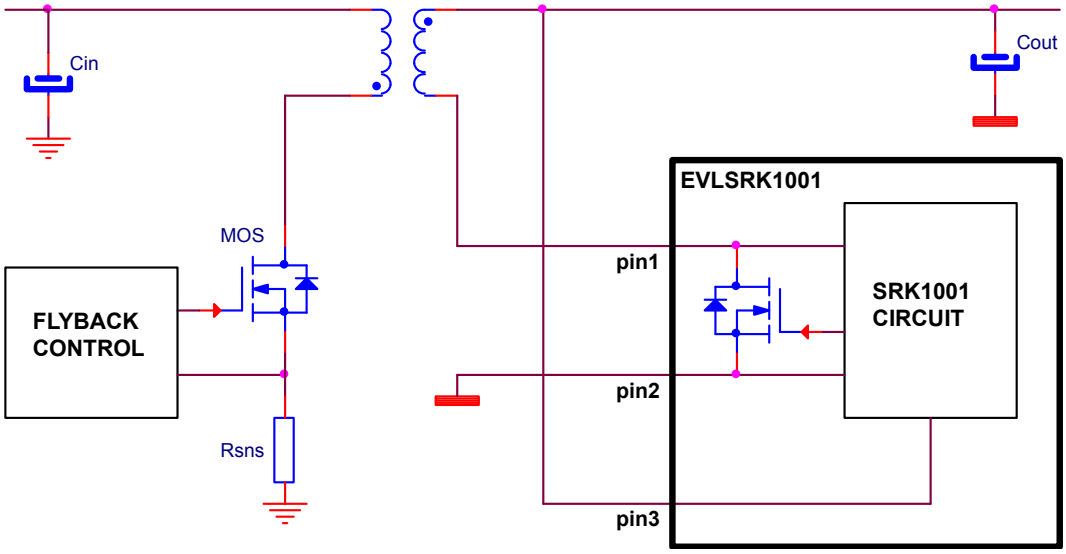


Figure 14. **Implementing the board in high-side configuration**

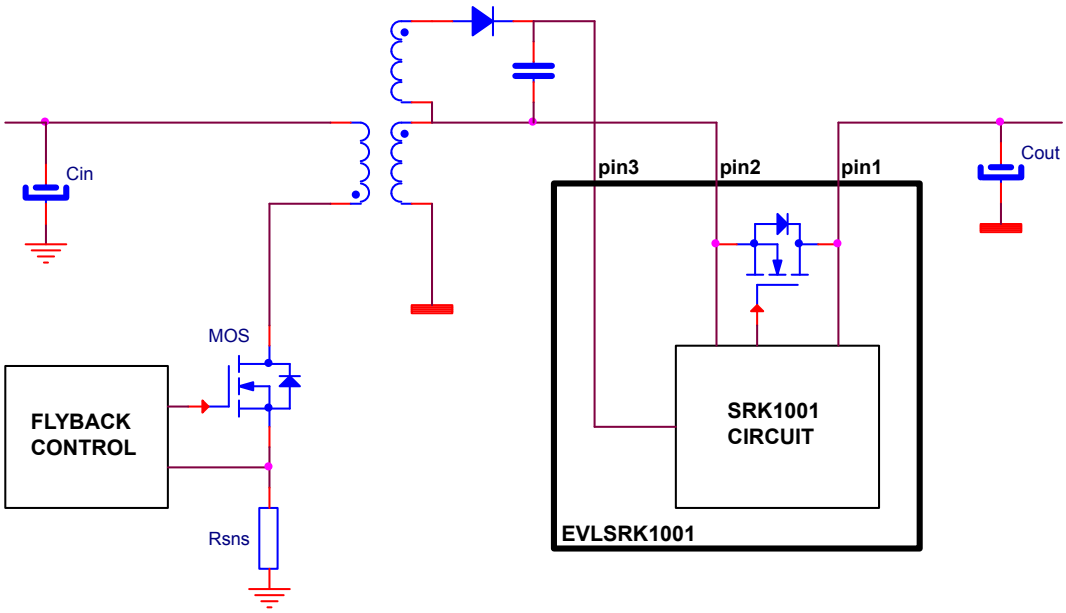
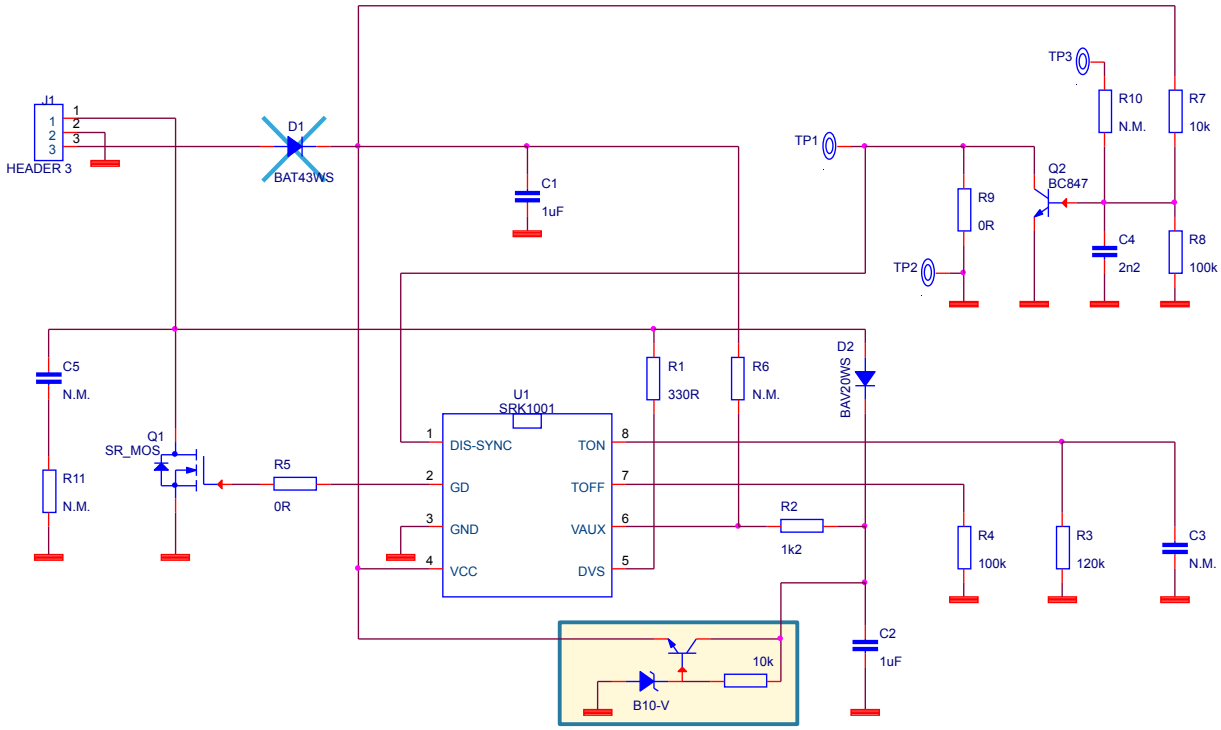


Figure 15. **VCC supply for high-side configuration**



3 Layout suggestions

The GND pin is the return of the bias current of the device and return for gate drive current. It should be routed in the shortest way possible to the common point where the source terminal of the SR MOSFET and output capacitor negative terminal are connected. When laying out the PCB, care must be taken in keeping the source terminal of the SR MOSFET as close to the negative terminal of the output capacitor as possible.

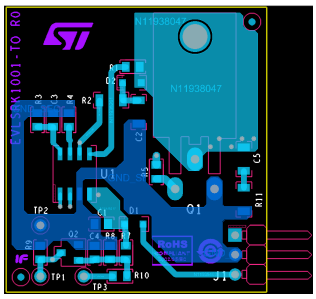
The usage of bypass capacitors between the VCC pin and GND pin is recommended. They should be low-ESR, low-ESL type and located as close to the IC pins as possible. Sometimes, a series resistor (in the order of tens of Ohms) between the converter output voltage and the VCC pin, is useful to form an RC filter along with the bypass capacitor in order to obtain a cleaner V_{CC} voltage.

A larger copper area connected to the GND pin and located below the device package helps heat dissipation generated inside the IC, keeping the junction temperature lower.

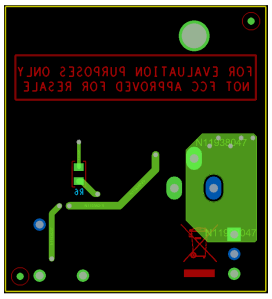
The following recommendations should be taken into account when designing the PCB:

- Connect the device GND pin as close as possible to the SR MOSFET source terminal.
- Reduce the driving current path length and area as much as possible.
- Use a bypass capacitor across VCC and GND as close to the device pins as possible.
- Use a resistor (>300 Ω) in series with the DVS pin.
- The DVS connection to the SR MOSFET drain terminal is not critical (since the adaptive turn-off algorithm automatically compensates for stray inductances in the SR MOSFET current path). Nevertheless, it remains preferable to sense the MOSFET voltage as close to its drain terminal as possible.
- Since the TON and TOFF pin sourced current is relatively low, these pins may be affected by current injections from nearby tracks with high dV/dt (i.e., drain sense signals). The TON and TOFF pins should therefore be kept away from SR MOSFET drain tracks.

Figure 16. Board layout

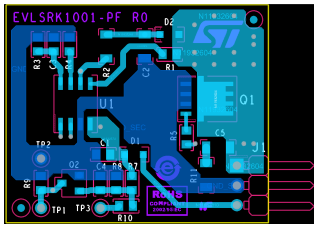


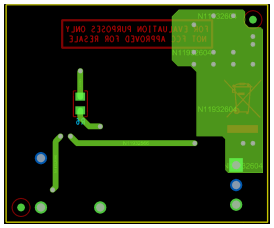
Top



Bottom

Evaluation boards with TO220 MOSFET





Evaluation boards with PowerFLAT MOSFET

4 References

1. SRK1001 datasheet: available at http://www.st.com/

Revision history

Table 3. **Document revision history**

Date	Version	Changes
13-Dec-2019	1	Initial release.

Contents

List of figures

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