AN5355

Application note

Mitigation technique of the SiC MOSFET gate voltage glitches with Miller clamp

Introduction

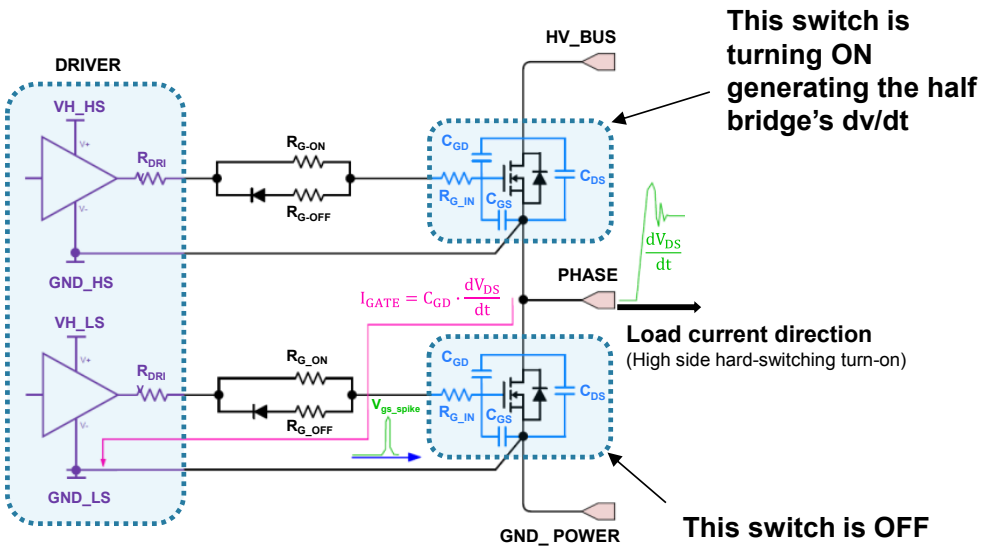
The gate drive requirements of Silicon-Carbide (SiC) MOSFETs are similar to Silicon MOSFETs and IGBTs; however the superior switching capability combined with the specific electrical characteristics of these power devices and parasitic elements requires special attention on the gate drive circuit and layout design to avoid the ringing and overshoot phenomena from becoming an issue. In particular, induced Miller turn-on effects and amplitude voltage glitches across the gate-source terminals may be slightly exacerbated due to the higher target commutation speed and because the negative gate voltage amplitude maximum rating (AMR) is different from the positive one contrary to what is typically expected in silicon devices. It is therefore very important to establish proper driving conditions by preventing these anomalies with appropriate mitigation methods, without overly compromising the device's switching performance. The use of a Miller clamp instead of standard gate driver configurations allows optimal clamping and the best possible gate control under high-speed switching events, to completely eliminate unwanted Miller induced turn-on effects. In order to demonstrate this concept, the 2nd generation 650 V SiC MOSFETs from the STPOWER family in an HiP247 package are employed to investigate these anomalies arising at the gate-source terminals during the switching transients.

1 Miller turn-on and glitch phenomena

1.1 Glitch phenomena generation

In bridge topologies, during the high negative slew rate of V_{DS} voltage of one switch, a current is injected towards the gate by the Miller capacitance of the complementary switch (C_{GD}). A voltage spike appears on the switch gate due to the drop caused by the Miller current across the overall gate path impedance. If the positive V_{GS} spike exceeds the switch $V_{GS(th)}$ during the rapid rise of the V_{DS} transient, a shoot through may occur across the half bridge. Power devices with low threshold voltage such as SiC MOSFETs are more likely to suffer from induced turn-on, which is why certain precautions are required. The negative temperature coefficient of the threshold voltage can also foster this phenomenon and potential risks of capacitive parasitic turn-on can be obviated by reducing the R_{Goff} value.

Figure 1. Miller turn-on phenomenon due to fast rising V_{DS} transient in half bridge topology



In general, the duality of glitch phenomena is generated due to the applied positive or negative dv/dt on the switching node resulting in an instantaneous current I_{GD} flow through the charge of the MOSFET Miller capacitance C_{GD}. Some current through C_{GD} flows out of the gate terminal and back through the drive sink resistance, which produces a spurious voltage spike at the MOSFET. During the negative dv/dt, occurring at turn-off of the complementary switch in half bridge topology, the negative V_{GS} peak has to be kept within the AMR to avoid any possible gate oxide damage.

Figure 2. Miller current generation with positive dv/dt

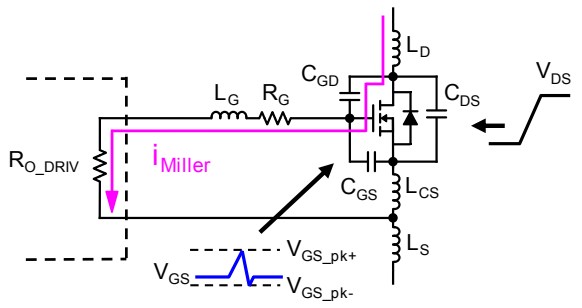


Figure 3. Miller current generation with negative dv/dt

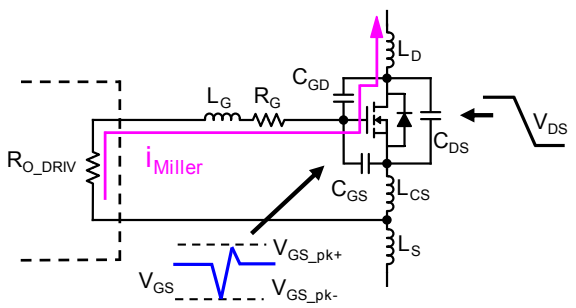
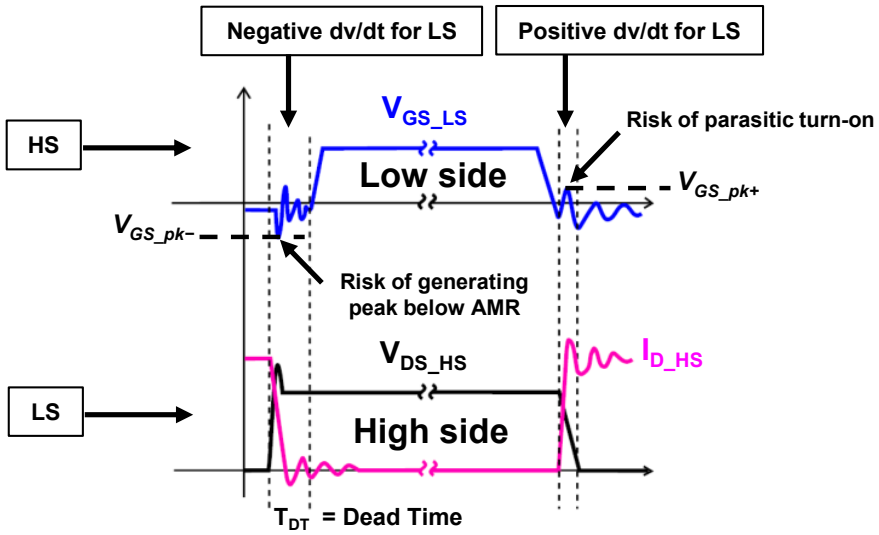


Figure 4. Duality of glitch phenomena



Inductive parasitic turn-on can be also generated during turning off of the load current when a voltage is induced across the emitter stray inductance. In this condition, the decay of the current induces a voltage on source stray inductance that shifts the source potential to the negative level. The inductive parasitic turn-on, however, can be limited by increasing the R_{Goff} value. Useful approaches that help control glitch phenomena include limiting dV/dt rating, minimizing the parasitic gate loop inductance, selecting a driver with low pull down output impedance or implementing negative gate bias. False turn-on phenomenon due to a fast positive dv/dt rating can be also limited by using a separate turn-off gate driving network path or putting a small capacitor between the gate to source at the expense of reducing the efficiency improvement with higher switching losses. More advanced techniques, such as "Active Miller Clamp", can be used to provide a low impedance path without compromising the turn-off slew rate control.

1.2 Mitigation techniques for induced G-S glitches

Driving the switch gate to a negative voltage increases the safety margin between the spike level and the $V_{GS(th)}$ threshold. However, a negative voltage that is too low increases the risk of exceeding the lower AMR limit of V_{GS} due to the negative spikes caused by C_{GD} discharge in the opposite dv/dt transient; the best trade-off is usually a negative voltage between -2 V and -5 V in according to the maximum rating of the involved device. The use of an active Miller clamp to mitigate induced G-S glitches allows to establish a low impedance path without compromising the turn-off slew rate control when the external switch is already off, which helps avoid the induced turn-on phenomenon. Moreover, it also enables the turn-off gate resistor on the basis of turn-off speed requirements only (E_{OFF}), and helps reduce the negative gate spike caused by C_{GD} discharge during the opposite dv/dt transients.

Figure 5. Negative gate driving

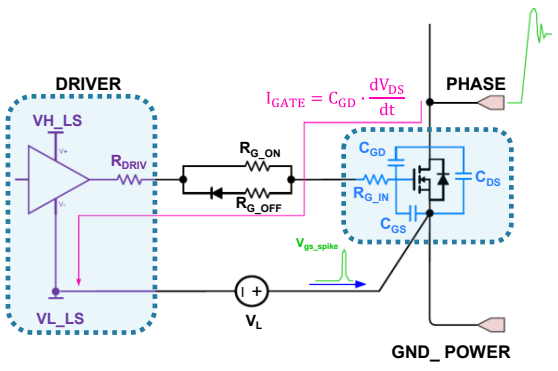
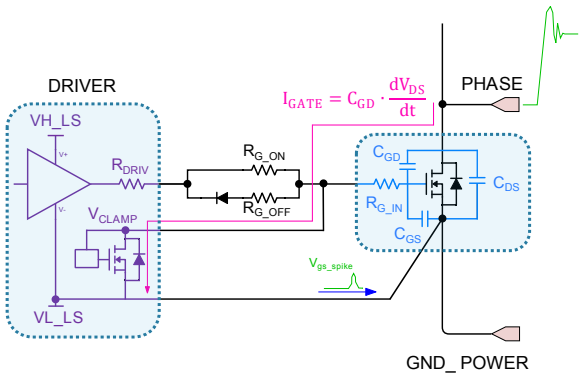


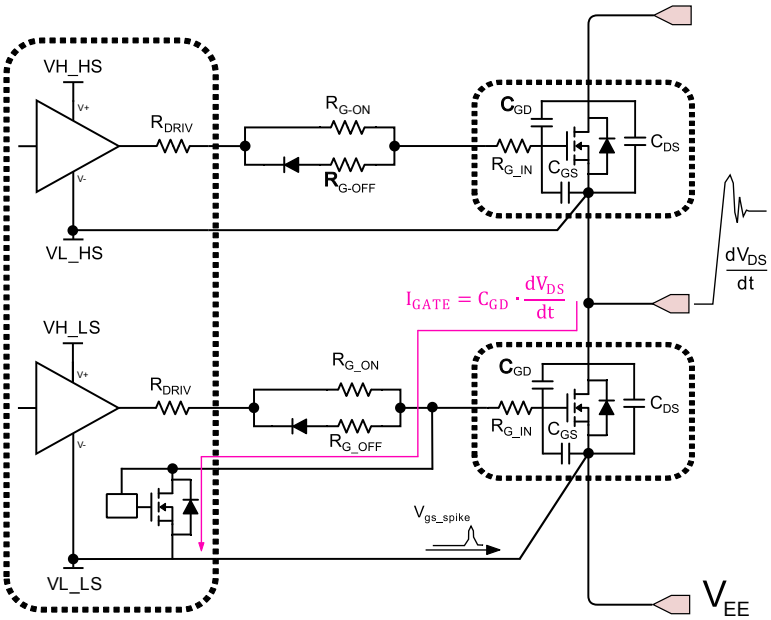
Figure 6. Active Miller CLAMP



1.3 How active Miller clamp works

The additional switch between the gate and source controls the Miller current during a high dV/dt situation and keeps the SiC MOSFET totally off by shorting the gate-to-source path after a voltage level is reached. During turn-off switching, the gate voltage is detected and the clamp is activated when the gate voltage drops below a threshold voltage value relative to V_{EE} (see Figure 6. Active Miller CLAMP). The currents across the Miller capacitance are shunted by the transistor instead of flowing through the output driver V_{OUT}. The Miller clamp function is only effective during SiC MOSFET turn-off and does not affect SiC turn-on. It provides cost saving solution by eliminating the need for a negative supply voltage and additional capacitors that reduce driver efficiency.

Figure 7. **Active Miller clamp technology**

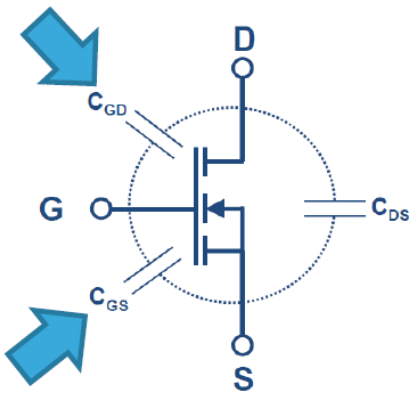


1.4 Voltage coupling through (Miller) capacitance

Another important parameter to be taken in account beside the Miller transfer capacitance in order to minimize the sensitivity to the ringing phenomena is the C_{rss} C_{iss} ratio in terms of maximum amplitude at V_{DS} = 0 V and how its trend decreases over the V_{DS} variation. When a voltage appears across the drain and source of the MOSFET, it couples to the gate and causes the internal gate source capacitor to charge. If the voltage on the gate increases beyond the MOSFETs threshold voltage, it starts to turn back on which can cause cross conduction. The ratio of the capacitances C_{rss} and C_{iss} determines the severity of this effect.

Gen2 SiC MOSFETs also improves on the 1st generation (Gen1) with better C_{GD}/C_{GS} ratio, which determines voltage coupling, and a smaller C_{GD} with bigger C_{GS} minimizes the residual V_{GS} when device is off (capacitive divider).

Figure 8. **SiC MOSFET intrinsic capacitances**

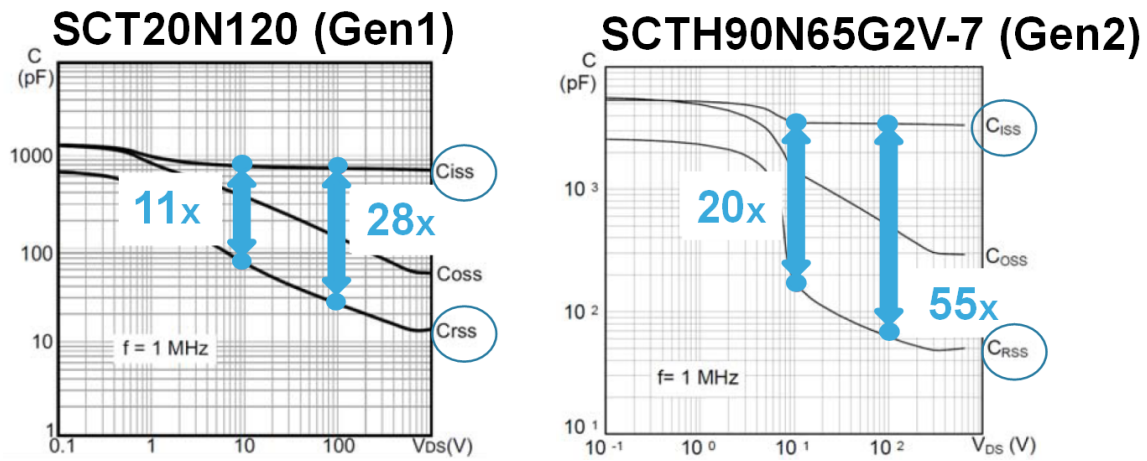


$$C_{RSS} = C_{GD}$$

$$C_{ISS} = C_{GS}//C_{GD} \approx C_{GS} \text{ since } C_{GS} \gg C_{GD}$$

$$C_{OSS} = C_{GD}//C_{DS}$$

Figure 9. Capacitive ratio C_{GD}/C_{GS} Gen1 vs. Gen2 SiC MOSFETs



As visible from the capacitive ratio between Gen1 SiC MOSFET SCT20N120 and Gen2 SiC MOSFET SCTH90N65G2V-7 of the above attached datasheet capacitance variation curves, the reverse transfer capacitance C_{rss} is 11 (Gen1) vs 20 (Gen2) times smaller than the input capacitance C_{iss} at 10 V and 28 (Gen1) vs 55 (Gen2) at 100 V.

2 Voltage glitch suppression with active Miller clamp

The Miller clamp function implemented on the new ST gapLITE driver has been tested for the reduction of both positive and negative glitches: positive glitches could cause thermal stresses on the device due to spurious turn-on effects, while negative glitches could jeopardize the reliability of the gate oxide. The Miller effect has been deeply investigated using two SiC MOSFETs connected in a DC/AC half-bridge configuration at $T_{amb} \approx 25$ °C and driven by gapLITE. The SCTW35N65G2V 2nd generation 650 V / 45 A planar SiC MOSFET by ST in an HiP247 package has been used as the test vehicle. The tested device features extremely low gate charge and input capacitances, very fast and robust intrinsic body diode capacitance, very high operating temperature capability (T_J = 200 °C), and very small $R_{DS(on)}$ variation over temperature.

2.1 Half bridge inverter and setup

The tests and measurements were performed on a half-bridge inverter topology board implemented on a PCB, as shown below.

Figure 10. Half bridge inverter topology

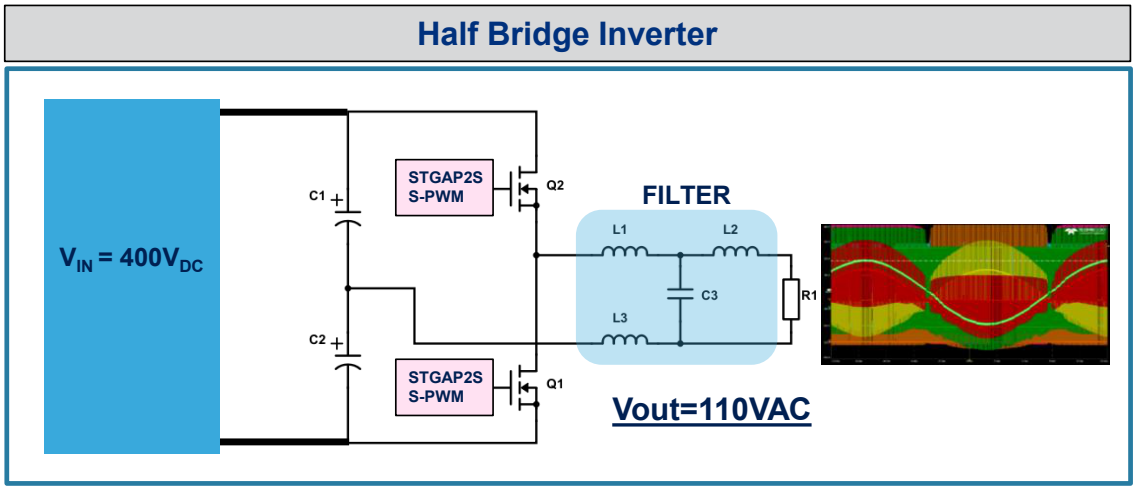


Figure 11. Half bridge inverter prototype

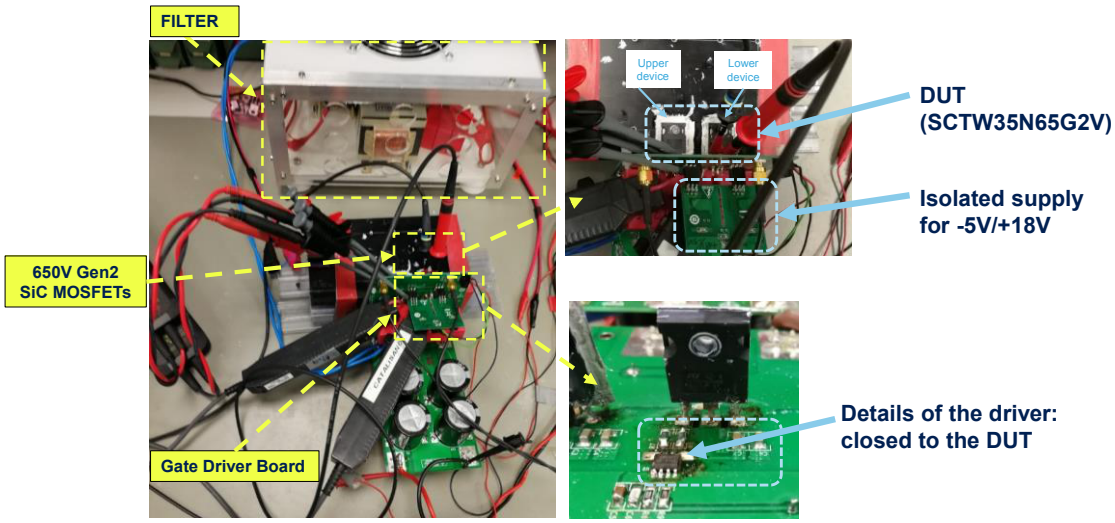
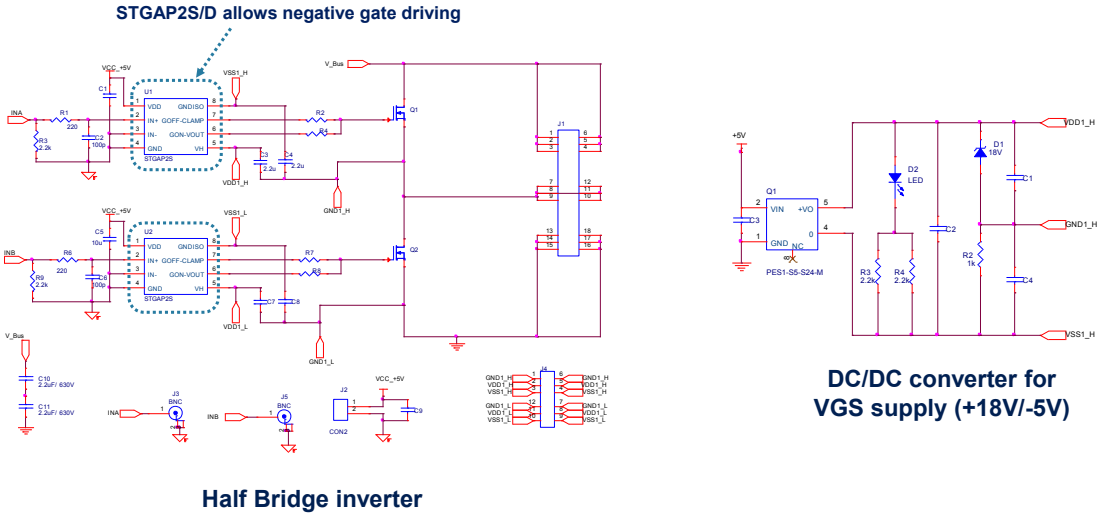


Figure 12. Half bridge inverter wiring diagram



Gate drivers gapLITE single STGAP2S were implemented on the motherboard by allowing negative gate voltage to drive the two SiC MOSFETs. Short paths between gate pin and driver have been enabled and optimized in order to guarantee less impedance to the Miller Clamp. Features and electrical characteristics of the used gapLITE single drive are:

- 3 V 3/5 V logic inputs (1/2, 2/3 of V_{DD} threshold)
- up to 26 V supply voltage
- 4 A sink/source current capability
- short propagation delay: 80 ns
- UVLO function (for each supply)
- temperature shut-down protection
- stand by function
- 100 V/ns CMTI
- high voltage rail up to 1700 V
- active high and active low input pins (for HW interlocking)
- STGAP2C: separated output option for easy gate driving tuning
- STGAP2SC: Miller clamp pin option to avoid induced turn-on
- negative gate drive ability
- SO-8 package

Measurements on lower device were taken with the PP023 passive probe with short loop for GND and 500 MHz of BW. For the upper device, the HVD3106 with twisted terminal and 120 MHz BW. The oscilloscope bandwidth was 500 MHz.

Figure 13. STGAP2C: separated output

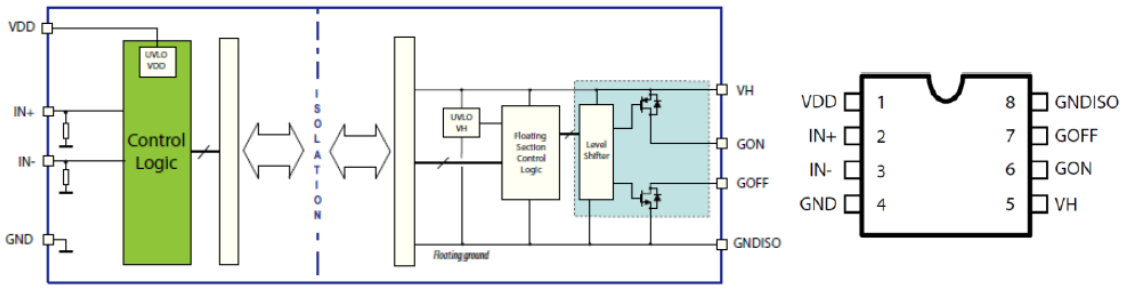
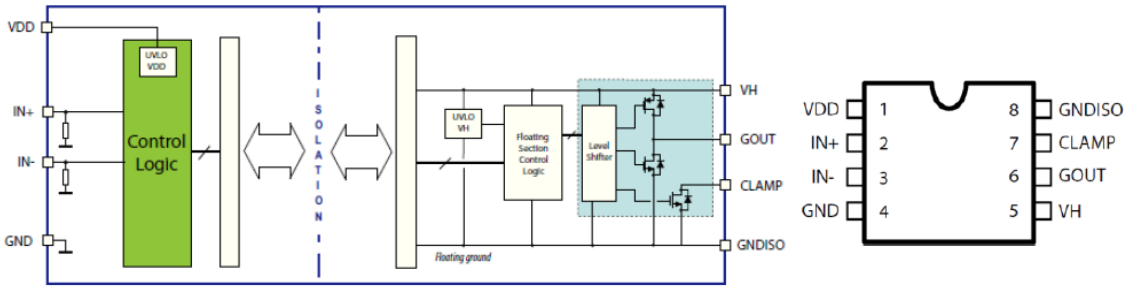


Figure 14. **STGAP2SC: Miller CLAMP pin option to avoid induced turn-on**



2.2 2nd Gen 650 V SiC MOSFET

ST's 2nd generation (Gen2) SiC improves on the 1st generation (Gen1) with better $R_{DS(on)}$, smaller chip size, lower Q_g and optimized JFET geometry. In particular, the new Gen2 features a planar structure with a further elementary pitch reduction that decreases the specific on-resistance $R_{DS(on),SP}$ at 25 ºC (with $R_{DS(on),SP}$ the $R_{DS(on)}$ x active area) by 40% compared with Gen1 MOSFETs. Gen2 SiC MOSFET driving requirements need a gate bias voltage of +18 V to obtain the proper $R_{DS(on)}$ with lower drive loss. It is also possible to reduce this to +15 V, but this increases the $R_{DS(on)}$ by about 80% at 20 A and 25 °C.

Other features are:

- extremely low gate charge and input capacitances
- very fast and robust intrinsic body diode capacitance
- very high operating temperature capability (T_j = 200 °C)
- very small $R_{DS(on)}$ variation overtemperature

Table 1. **Absolute maximum ratings and on/off states**

Parameter	Symbol	Value
SCTW35N65G2V	2nd generation 45 A / 650 V planar SiC MOSFET technology	
Drain current (continuous) at T_c = 25 °C	I_D	45 A
Drain current (continuous) at T_c = 100 °C		35 A
Drain current (pulsed)	I_{DM}	90 A
Gate-source voltage	V_{GS}	-10 to 22 V
Gate-source voltage (recommended operating range)		-5 to 20 V
Operating junction temperature range	T_J	-55 to 200 °C
Gate threshold voltage	$V_{GS(th)}$	3.2 V
Static drain-source on-resistance @ V_{GS} = 18 V, T_J = 25 °C	$R_{DS(on)}$	55 mΩ

Table 2. Dynamic, switching energy and times

Parameter	Symbol	Value
Input capacitance	C_{ies}	1370 pF
Output capacitance	C_{oes}	125 pF
Reverse transfer capacitance	C_{res}	30 pF
Total gate charge	Q_g	73 nC
Turn-on switching energy @ T_J = 25 °C	E_{on}	100 µJ
Turn-off switching energy @ T_J = 25 °C	E_{off}	35 µJ
Fall time @ T_J = 25 °C	t_f	14 ns
Rise time @ T_J = 25 °C	t_r	9 ns

2.3 Gate driver configurations

Two different configurations available for the gate driving networks were implemented: the “Separated Output” option (indicated as SEP OUT) having a different path for the driving networks' turn-on/off, and the “Active Miller clamp” function (indicated as AMC) to mitigate both positive and negative voltage glitches.

Figure 15. Separate output configuration

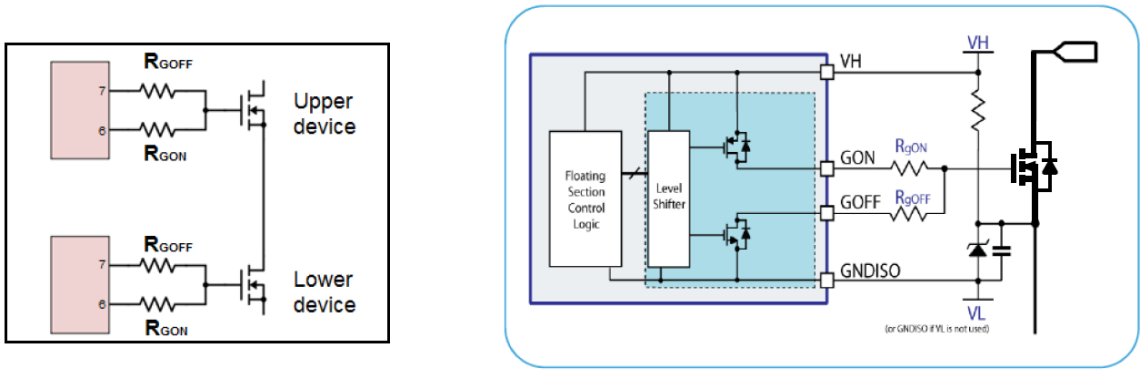
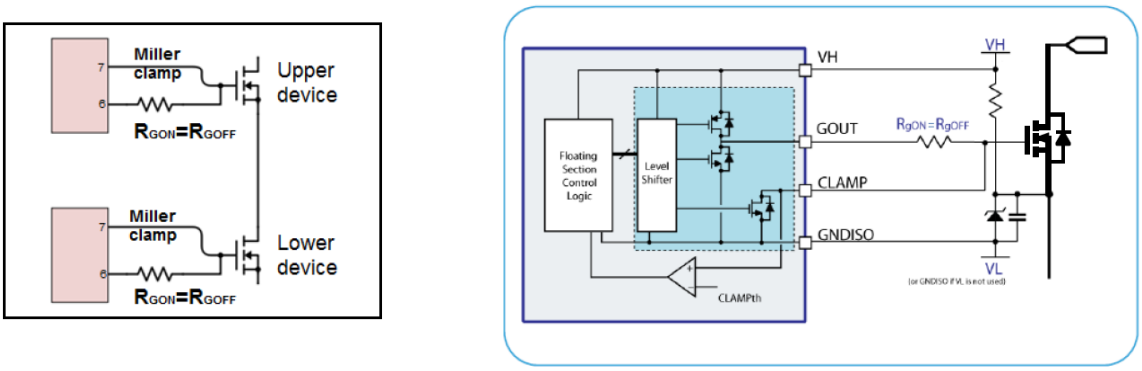


Figure 16. Single output with AMC configuration



3 Test conditions and results

The tests and measurements with SiC MOSFETs and gapLITE were performed on the half-bridge inverter board at the following conditions:

- input voltage V_{IN} = 400 V
- output voltage V_{OUT} = 110 V_{ac}
- output power P_{OUT} = 1600 W
- switching frequency F_{SW} = 50 kHz
- R_{G_ON} = R_{G_OFF} decreased up to 2.2 Ω
- RMS output current IRMS ≈ 14.5 A
- gate-source driving voltage V_{GS_ON} = +18 V and V_{GS_OFF} = -5 V
- death time = 200 ns

The main objectives were:

- To check whether oscillations during commutation are within the reference limits set as $V_{GS(th)_TYP}$ = 3.2 V at 25 ºC and $V_{GS,MIN}$ = -10 V (AMR).
- Compare the two different gate driver configurations in terms of generation and clamping of the gate voltage glitches, by varying the driving settings and slew rate conditions.

The images below show the low side device measurements in the two different driving configurations comparing SEP OUT vs AMC. From the values achieved by the positive and negative voltage glitches on V_{GS} signal vs dv/dt variation, the positive glitches are below the V_{th} value with both tested AMC and SEP OUT driving configurations, both positive and negative dv/dt, and in all the three setting conditions for the gate driving resistances of 22 Ω, 10 Ω and 4.7 Ω, respectively. However, the negative glitches exceed the AMR for both configurations and in all the gate resistance conditions, with the exception of AMC at 22 Ω.

In particular, the positive and negative voltage glitch levels reached by the low side device during the tests were:

+2.4 V and -5.5 V with SEP OUT compared to -3.5 V and -7.5 V with AMC @ R_{G_ON} = R_{G_OFF} = 22 Ω and positive dv/dt up to 40 V/ns;

-3.0 V and -11.6 V with SEP OUT compared to +1.1 V and -8.5 V with AMC @ R_{G_ON} = R_{G_OFF} = 22 Ω and negative dv/dt up to 20 V/ns;

+0.3 V and -6.8 V with SEP OUT compared to -2.3 V and -10.2 V with AMC @ R_{G_ON} = R_{G_OFF} = 10 Ω and positive dv/dt up to 60 V/ns;

-1.5 V and -11.5 V with SEP OUT compared to +2.0 V and -8.9 V with AMC @ R_{G_ON} = R_{G_OFF} = 10 Ω and negative dv/dt up to 30 V/ns;

-1.3 V and -7.5 V with SEP OUT compared to -0.5 V and -11.5 V with AMC @ R_{G_ON} = R_{G_OFF} = 4.7 Ω and positive dv/dt up to 80 V/ns;

-0.2 V and -12.0 V with SEP OUT compared to +2.5 V and -10.6 V with AMC @ R_{G_ON} = R_{G_OFF} = 4.7 Ω and negative dv/dt up to 40 V/ns.

Figure 17. Positive and negative voltage ringing with +dv/dt and -dv/dt @ R_g = 22 Ω

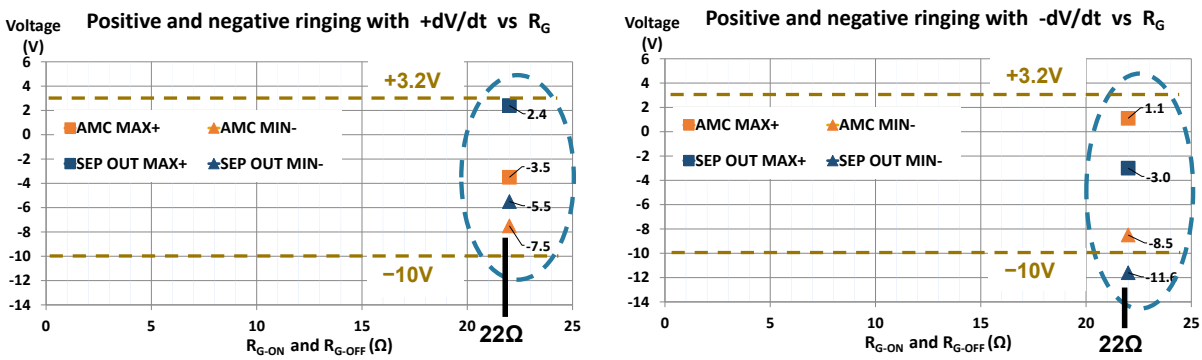


Figure 18. Positive and negative voltage ringing with +dv/dt and -dv/dt @ R_g = 10 Ω

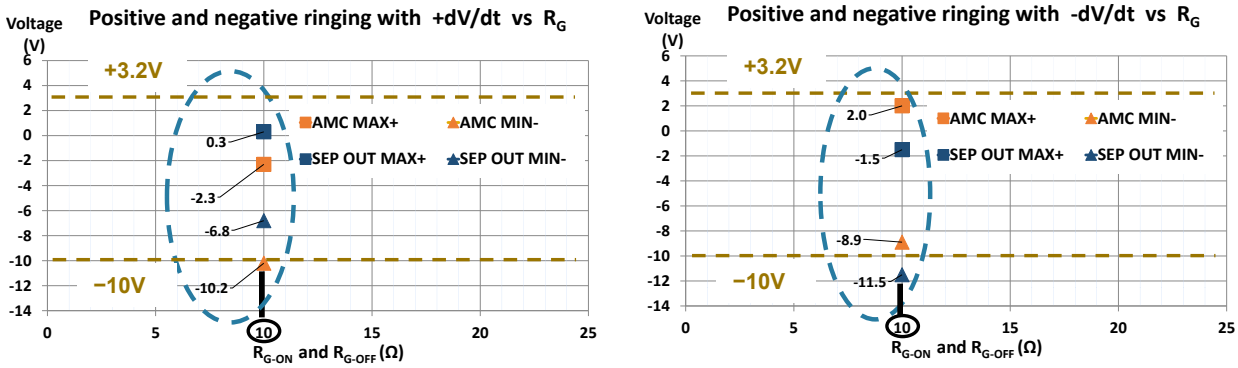


Figure 19. Positive and negative voltage ringing with +dv/dt and -dv/dt @ R_g = 4.7 Ω

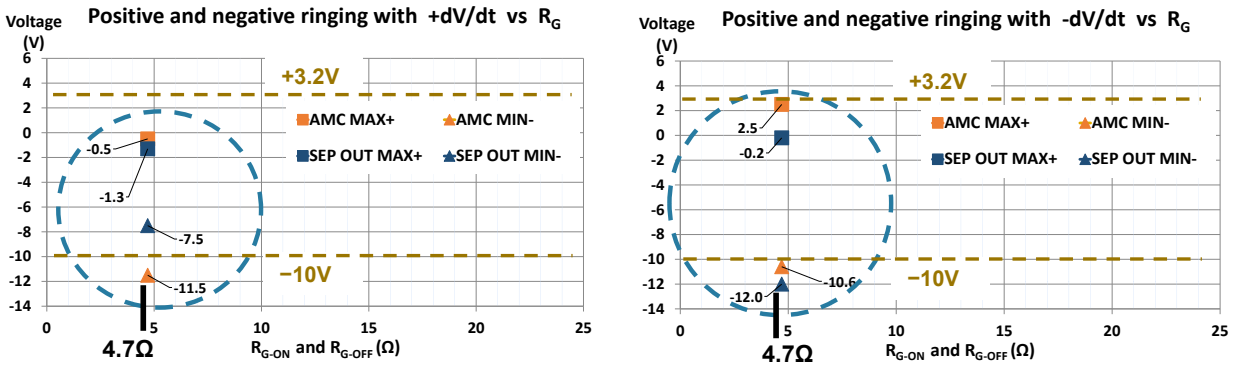


Figure 20. AMC vs SEP OUT with positive and negative dv/dt and R_g = 22 Ω

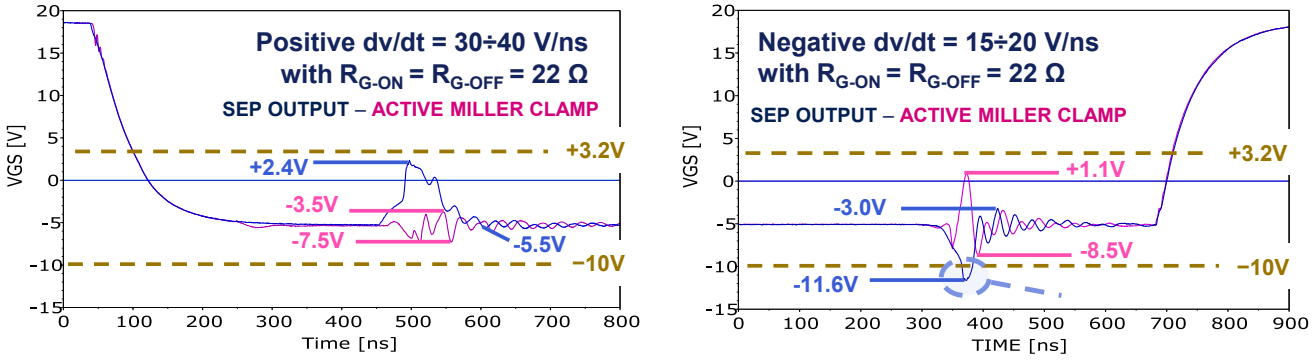


Figure 21. **AMC vs SEP OUT with positive and negative dv/dt and R_g = 10 Ω**

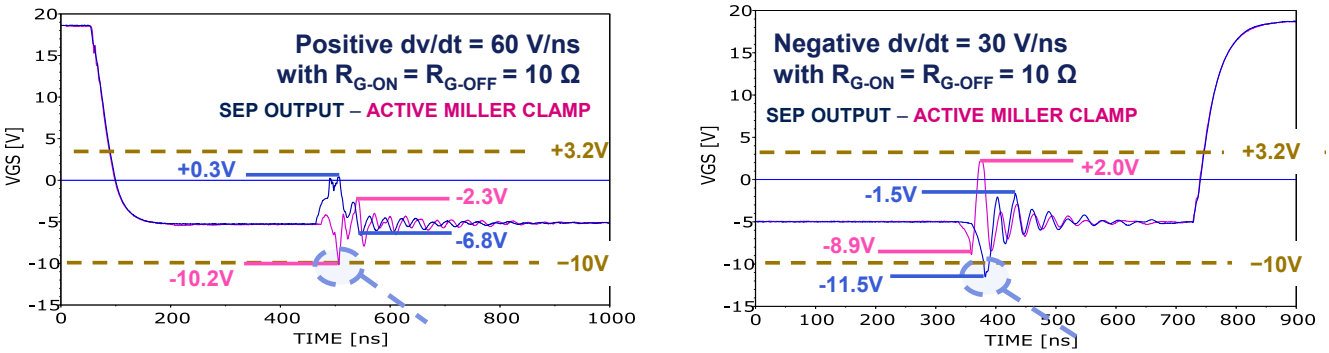
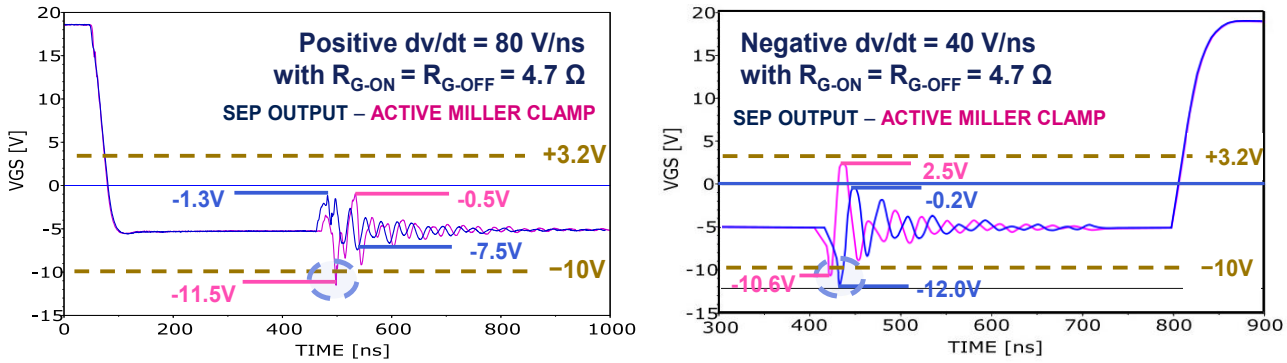


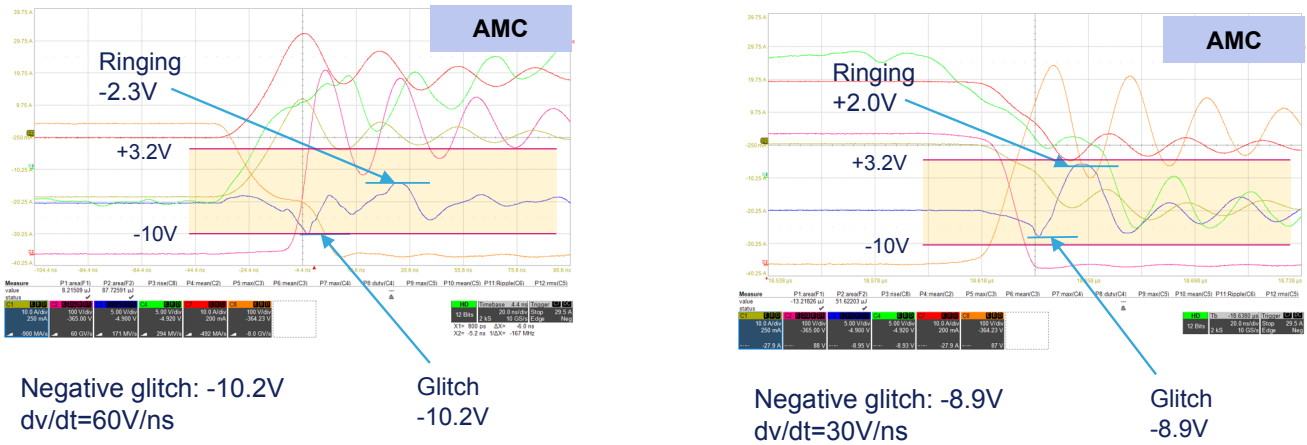
Figure 22. **AMC vs SEP OUT with positive and negative dv/dt and R_g = 4.7 Ω**



The figure below mentions the waveforms acquired in the AMC case with R_g = 10 Ω during positive and negative dv/dt for both low side and high side devices. The color codes used to differentiate the electrical signals are:

- Low side device: drain current in yellow (CH1@10 A/div), drain-source voltage in pink (CH2@100 V/div), gate-source voltage in blue (CH3@5 V/div)
- High side device: drain current in red (CH7@10 A/div), drain-source voltage in orange (CH8@100 V/div), gate-source voltage in green (CH4@5 V/div)

Figure 23. **AMC with positive and negative dv/dt @ R_g = 10 Ω**

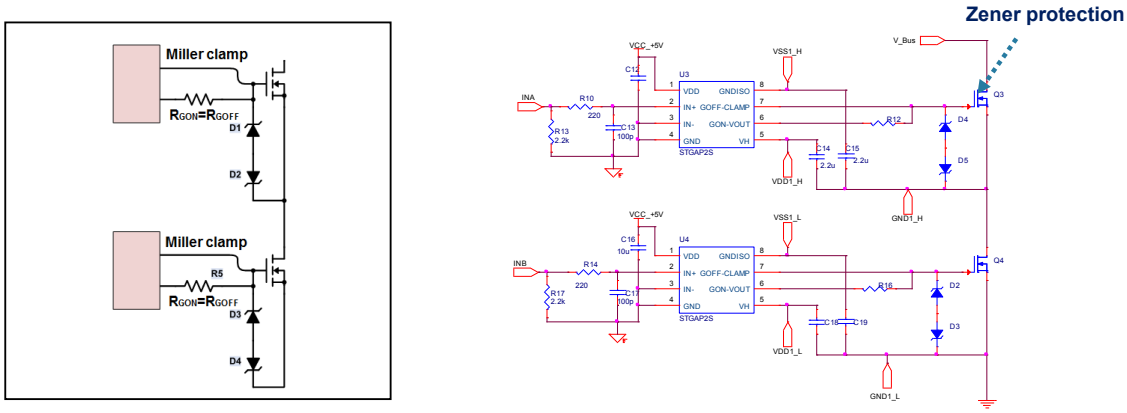


3.1 Zener protection among G-S pins with AMC driver configuration

Further evaluation tests were performed with the AMC driver by inserting zener protection among the G-S pins using two anti-series diodes to investigate the clamping action towards both positive and negative glitches at 2.2 Ω with the AMC driver:

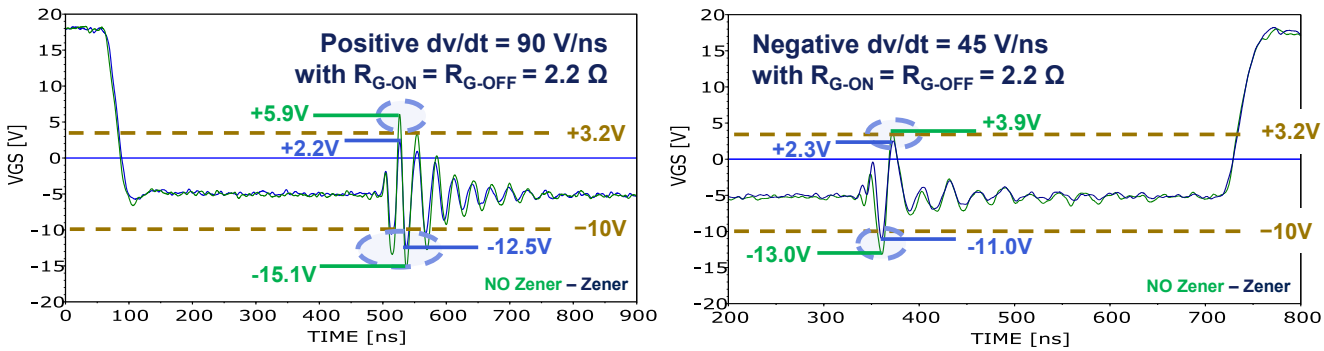
- 20 V Zener diode to clamp positive glitch
- 6 V Zener diode to clamp negative glitch

Figure 24. AMC configuration with zener protection among G-S pins



From the following figures with the Zener protection connected among the G-S pins, the negative glitches always exceed the AMR for configurations with Zener protection and R_g = 2.2 Ω, even if the negative V_{GS}-peak value is smaller than the value without Zener protection. Moreover, in AMC configuration without Zener diodes, the positive glitch is above the V_{th} value, but apparently not long enough to cause parasitic turn-on; while in AMC configuration with Zener diodes, the positive glitches are always below the V_{th} value and exhibit an effective performance improvement.

Figure 25. AMC driver with positive and negative dv/dt @ R_g = 2.2 Ω: comparison with/without Zener protection



4 Conclusion

Fast switching devices such as Silicon-Carbide (SiC) MOSFETs are affected by a common problem related to the induced Miller turn-on effect and the generation of glitch phenomena on the gate-source voltage. To better understand this phenomena, this paper looks at both the negative and positive voltage glitches that occur on the gate-source terminals of SiC MOSFETs during the transients turn-on and off on a typical half-bridge DC-AC power converter topology. A suitable gate driver with a Miller clamp function has been used to mitigate false turn-on behavior under fast switching conditions. The Active Miller Clamp technique shows a significant improvement with dv/dt ratings lower than around 20 V/ns and this case is of primary importance for applications like motor drive where slow switching transients are required. Some limitations are visible at higher dv/dt, especially in terms of negative glitch mitigation, due to the parasitic inductance in the active Miller clamp path that reduces the efficacy in clamping voltage spikes and is responsible for ringing. The use of Zener protection between gate and source provides an improvement in terms of spike reduction at high dv/dt, thus representing a further optimization to be combined with parasitic inductance minimization.

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Revision history

Table 3. Document revision history

Date	Version	Changes
15-Jul-2019	1	First release.

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