

---

## VIPower M0-7 thermal protections

### Introduction

The basic overload protection for Vertical Intelligent smart power (VIPower) drivers is founded on a simple current limit to thermal shutdown algorithm. This type of protection is ideal for driving loads with high inrush currents. However, this type of protection can be very stressful for the devices when driving extremely high inrush loads or faulty loads. So much that a more intelligent means of protection is required while maintaining the same standard of handling inrush currents. ST's M0-7 VIPower high side drivers do this by their advanced protection algorithms. These protection algorithms include:

- Load current limitation
- Active overload management by power limitation
- Over temperature shutdown
- Thermally based two-stage current limitation
- Configurable fault latch-off

## 1 Severe load stresses

While in normal operation, the stresses experienced by VIPower drivers are minimal and do not affect their long term reliability. However, there are times when there may be excessive load inrush current or the load is faulty. During these times, the driver first limits the current. This current limitation causes excessive power dissipation thus overheating the device. This simple current-limit-to-thermal-shutdown protection can generate thermo-mechanical stresses. These stresses can cause early wear-out. Understanding these stresses aids in providing solutions.

### 1.1 Inrush

Incandescent bulbs have an inrush current at turn on that initially mimics that of a shorted load and decays as the filament heats up. Depending on the ambient temperature and the supply voltage, incandescent bulb inrush currents can be as high as 20x that of a normal load. Without a high level of fault mitigation selecting a driver that will not limit the current at this excessive level may be required.

### 1.2 Shorted loads

For a device that is protected by a current-limit-to-thermal-shutdown algorithm a shorted load can be very stressful. This is especially true if the current limit threshold is set high to accommodate for most inrush conditions. Consider a 10 mΩ high side driver, the VN7010AJ. This is a good part for 5 A to 10 A applications. The typical current limit threshold is over 90 A. Shorting this output to ground on a healthy 14 V supply would generate well over 1.2 kW of heat. This extreme power dissipation can generate large thermal gradients across the surface of the die that can cause cumulative inelastic thermo-mechanical stress. That is, every time the driver sees this condition the device gets a little bit worse, eventually failing.

ST's VIPower drivers mitigate these issues by implementing a sophisticated protection algorithm. The multilevel protection algorithm typically steps through these simple phases:

1. Current limit
2. Power limitation
3. Thermal shutdown
4. Reduction of the current limit threshold

There is also an option to latch off the part when encountering either phase 2 or 3 above.

---

## 2 Current limit

---

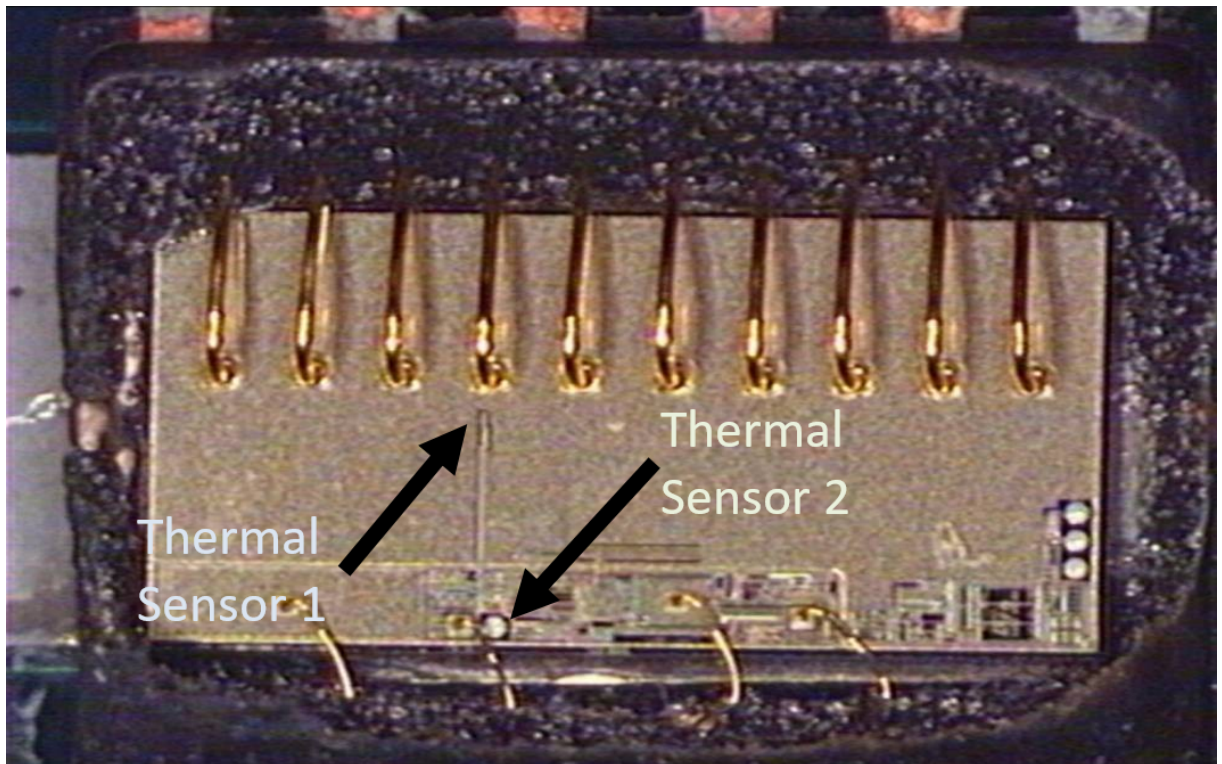
The first line of protection is current limit. For ST VIPower, this limit is set to protect a faulty load from fusing bond wires or melting metallization on the surface of the die. The purpose of current limitation is solely to protect the part from damage due to excessive current. As a result, the current limit is set much higher than the steady state thermal capability of the part. The advantage of doing this is to allow for nominal incandescent bulb inrush without current limitation. This “lights up” an incandescent bulb as quickly as possible and effectively reduces the stress in the driver.

### 3 Power limitation

As previously mentioned, high power dissipation events may cause the die to heat unevenly which can result in inelastic thermo-mechanical stress. The Power Limitation functionality mitigates this issue by slewing the rise in junction temperature. This allows the heat to spread more evenly across the die during the thermal event thus reducing the stress.

There are two Thermal Sensors on the die ([Figure 1](#)). One thermal sensor on the hottest part near the power leads (Thermal Sensor #1) and another one on the coldest part in the control section (Thermal Sensor #2). Thermal Sensor 1 is placed at the hottest part of the die, in the power stages, and Thermal Sensor 2 is placed at the coldest part, in the control section. In a faulty load event, the extreme power dissipation will cause a large thermal gradient between these two sensors. That is, sensor #1 will increase in temperature much faster than sensor #2. When the difference in temperatures between the two sensors exceeds  $\Delta T_{J\_SD}$  (typ. 60 °C), the part will shut off and wait for the temperature to be more evenly distributed across the die.

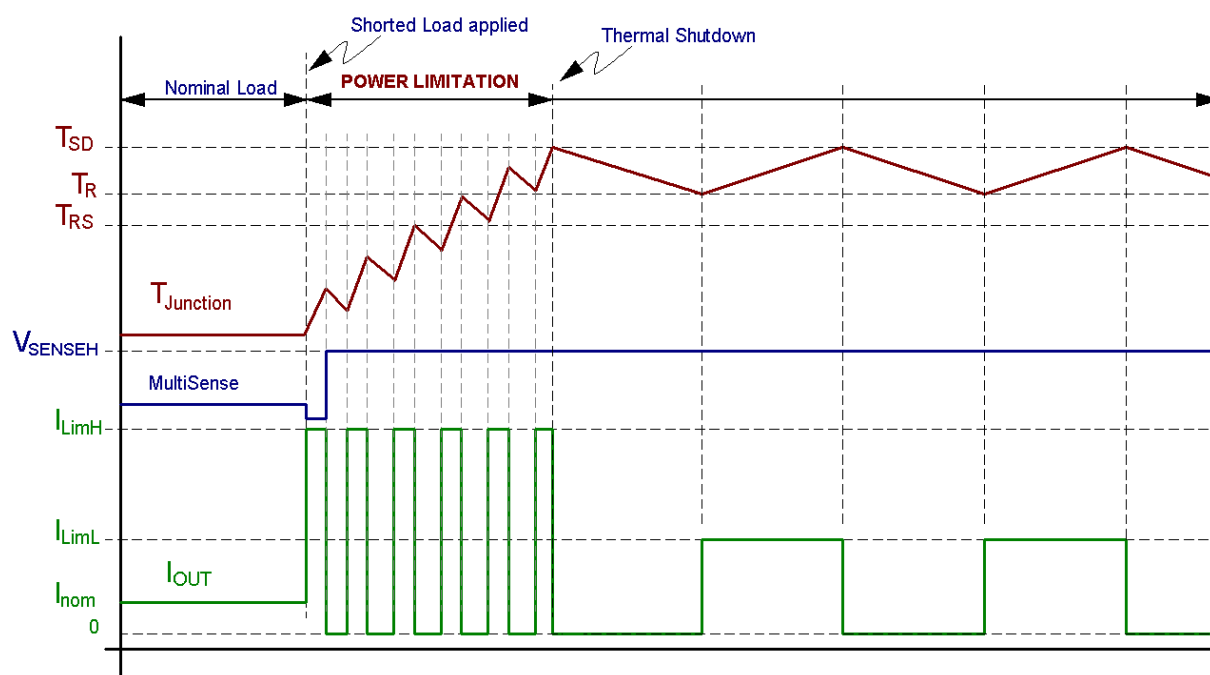
**Figure 1. VN7010AJ Thermal Sensor placement**



At the start of a power limitation event two things occur:

1. The affected output turns off
2. The multisense pin indicates a thermal intervention (see [Section 6](#) )

Figure 2. Power limitation on a shorted load



### 3.1 Why power limitation

As mentioned earlier excessive power dissipation can cause inelastic thermo-mechanical stress on the surface of the silicon. That is, the silicon will expand rapidly and unevenly, heating up faster where the power dissipation is at its highest point. When the device cools, the silicon does not completely return to the original size. This phenomenon can be defined using the Coffin-Manson thermal fatigue model. This model defines the highest thermal gradient across the die without causing inelastic expansion to be approximately 60 °C.

Coffin-Manson thermo-mechanical model:

$$N_f = A_f^{-\alpha} \Delta T^{-\beta} G(T_{MAX})$$

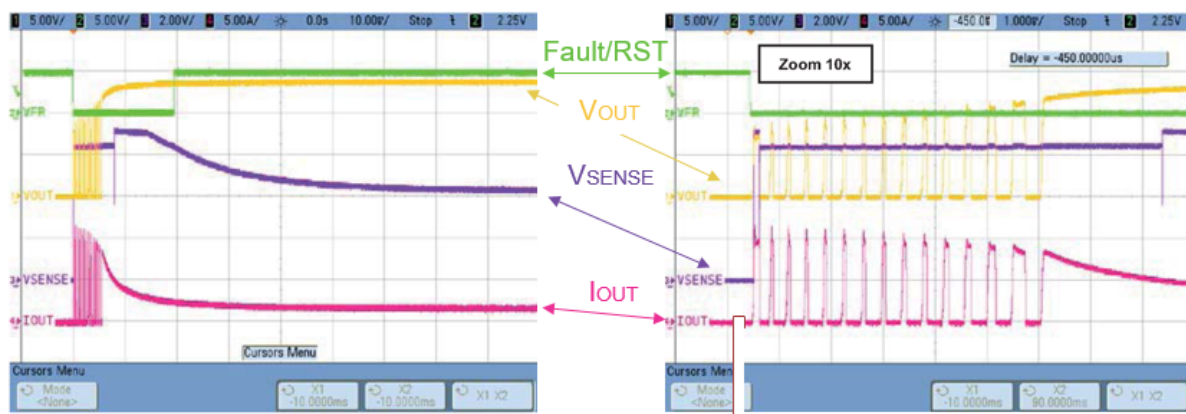
Where:

- $N_f$  = number of cycles to failure
- $f$  = the cycling frequency
- $\Delta T$  = range of temperature during the cycle
- $G(T_{MAX})$  = Arrhenius term evaluated at the max temperature reached during the cycle
- $\alpha = 2$  (typically)
- $\beta = 1/3$  (typically)

### Lamp inrush example

A specific lamp load requires a higher inrush current than the maximum current limit ( $I_{LimH}$ ) of the driver. The driver will limit the current during the inrush period. Power limitation will protect the driver based on the temperature. The Power limitation function will effectively drive the load at turn on as if it were in PWM, based on the dynamic thermal capabilities of the silicon. This allows the highest RMS current possible to heat up the filament as quickly as possible without causing permanent damage to the silicon. Figure 3 illustrates power limitation in action.

Figure 3. Inrush current mitigation



## 4 Thermal shutdown

The most basic of protections is thermal shutdown. ST's high side drivers implement thermal shutdown when the temperature of the thermal sensor near the hottest part of the die (sensor #1 in [Figure 1](#)) exceeds the thermal shutdown threshold ( $T_{SD}$ ). This can occur while operating in Power Limitation or slowly such that the Power Limitation function is not active.

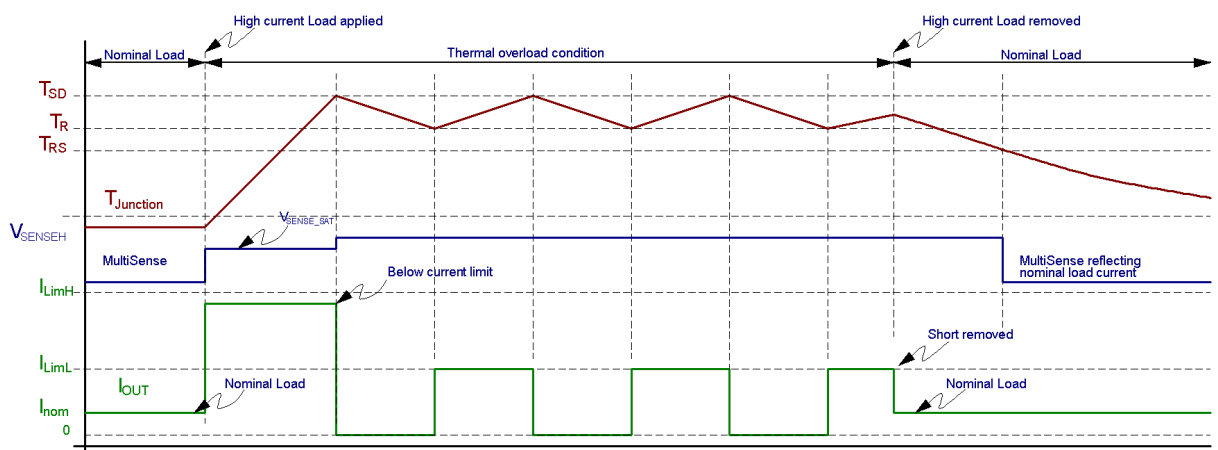
At thermal shutdown three things occur:

1. The affected output is turned off
2. A fault is indicated by the multisense pin if not already active due to power limitation, (see [Section 6](#) )
3. The current limitation threshold is reduced to  $\sim 1/3$  of the initial current limitation threshold

The faulty high side driver output will remain off until sensor 1 cools to the thermal reset value ( $T_R$ ). When the junction temperature falls below the thermal reset value,  $T_R$ , the driver will automatically restart at the reduced current limitation threshold. As long as the faulty load is in place the driver will repeat this process while maintaining a fault indication on the multisense pin (see [Section 6](#) ).

If the fault is removed, the driver will cool down. Only when the temperature of thermal sensor #1 falls below the fault indication reset temperature ( $T_{RS}$ ) will the multisense pin stop reporting a thermal fault.  $T_{RS}$  is lower than  $T_R$  to ensure a stable fault indication during a faulty load.

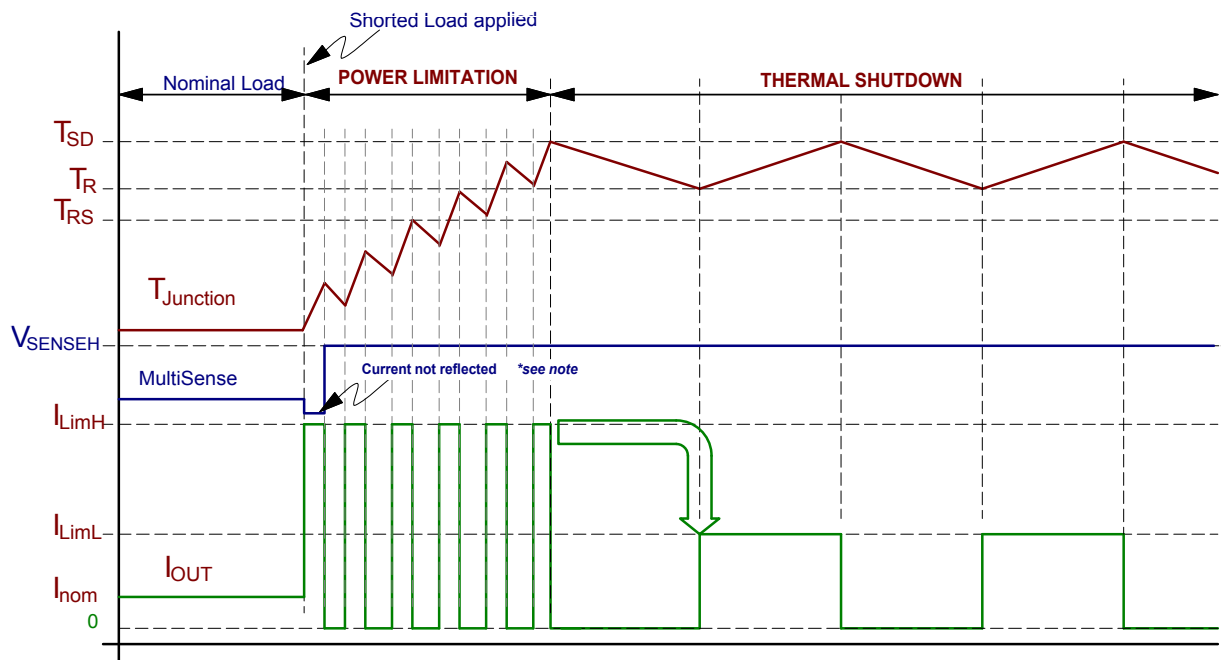
**Figure 4. Thermal shutdown response (no power limitation)**



## 5 Two-Stage current limit

When driving a load that is above the thermal capability of the device, if the FaultRST latch is not enabled (FaultRST = 0), the device will repeat the cycle of power limitation by current limiting to thermal shutdown, cool down and restart. Allowing an extended period of high current and high temperature can cause premature wear-out of the silicon. To mitigate this condition, the current limit after the first thermal shutdown is reduced to  $I_{LIML}$ , approximately  $1/3^{rd}$  of  $I_{LIMH}$  (see Figure 5). Note that power limitation feature did not cause the current limit to shift to the lower value. Only thermal shutdown causes the shift.

Figure 5. Two stage current limit



Note: refer to UM1922, section 7.2.4, for further information

The lower current limit,  $I_{LIML}$ , while being low enough to reduce early wear-out concerns, is still well above the thermal capability of the driver.



## 6 Fault indication

The fault status during a thermal event is communicated to the microcontroller through the Multisense pin. The Multisense pin has multiple functions:

- Current sense feedback of the output(s), ( $I_{SENSE}$ )
- Junction temperature sense feedback, ( $T_{CHIP}$ )
- Battery voltage sense feedback ( $V_{CC}$  Sense)
- Fault indication

The multisense pin function is determined by the Sense Enable (SEn) pin and the Select (SELx) pins. With the SEn pin low the multisense pin is tri-stated. This is so that multiple devices can share the same sense resistor / ADC port. The Select pins determine the multisense pin functionality,  $I_{SENSE}$ ,  $T_{CHIP}$ ,  $V_{CC}$  Sense.

Fault indication is only available when the multisense pin is selected to reflect the output current ( $I_{SENSE}$ ). If the device has more than one output, each individual output current measurement must be selected to see the fault indication for that output.

With the multisense pin set to reflect the output current a thermal event will force the multisense pin to switch from reflecting  $I_{SENSE}$  to a fixed voltage ( $V_{SENSEH}$ ).

**Table 1. Multisense truth table for a dual output device**

SEn	SEL <sub>1</sub>	SEL <sub>0</sub>	MUX channel	Multi Sense output			
				Normal mode	Overload	OFF-state diag.	Negative output
L	X	X					
H	L	L	Channel 0 diagnostic	$I_{SENSE} = 1/K * I_{OUT0}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	H	Channel 1 diagnostic	$I_{SENSE} = 1/K * I_{OUT1}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	H	L	$T_{CHIP}$ Sense	$V_{SENSE} = V_{SENSE\_TC}$			
H	H	H	$V_{CC}$ Sense	$V_{SENSE} = V_{SENSE\_VCC}$			

It should be noted that a fault flag ( $V_{SENSEH}$ ) does not indicate an over current event. It only reflects a thermal event, being either a power limitation or thermal shutdown.

Fault indication can also be off state open load, with the multisense pin set to reflect output current when the input is low.

## 7 Latching function

The M0-7 high side drivers have a configurable latching function which can be activated by the FaultRST pin. When a thermal fault occurs the part will turn off and cool down. If the FaultRST pin is LOW, the part will restart. If FaultRST pin is HIGH, the driver will remain off. A thermal event can be defined as either a power limitation function ( $\Delta T > 60\text{ }^{\circ}\text{C}$ ) or a thermal shutdown ( $T_J > T_{SD}$ ).

To un-latch a faulty output the FaultRST pin is pulled low. The FaultRST pin is global. It applies to all of the outputs in a single device.

*Note: if the latch function is not used then it is strongly recommended that the multisense status be monitored to detect and disable the part in case of a faulty load. Even with the fault mitigation in place staying in a shorted condition may wear the part out prematurely and potentially overheat the circuit board.*

**Figure 6. Latch function**

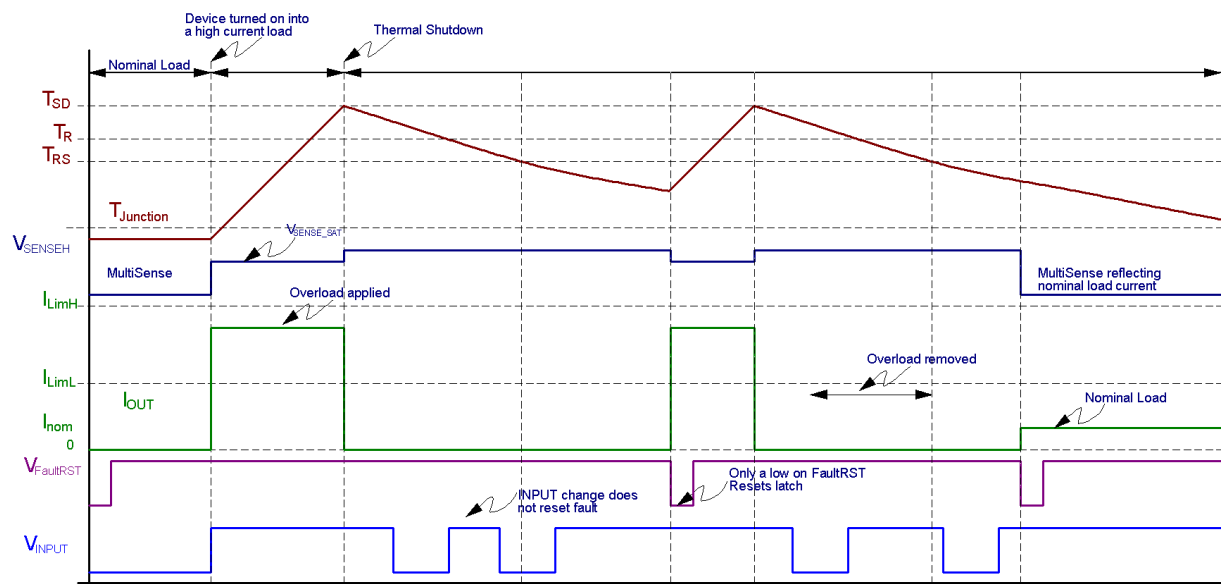
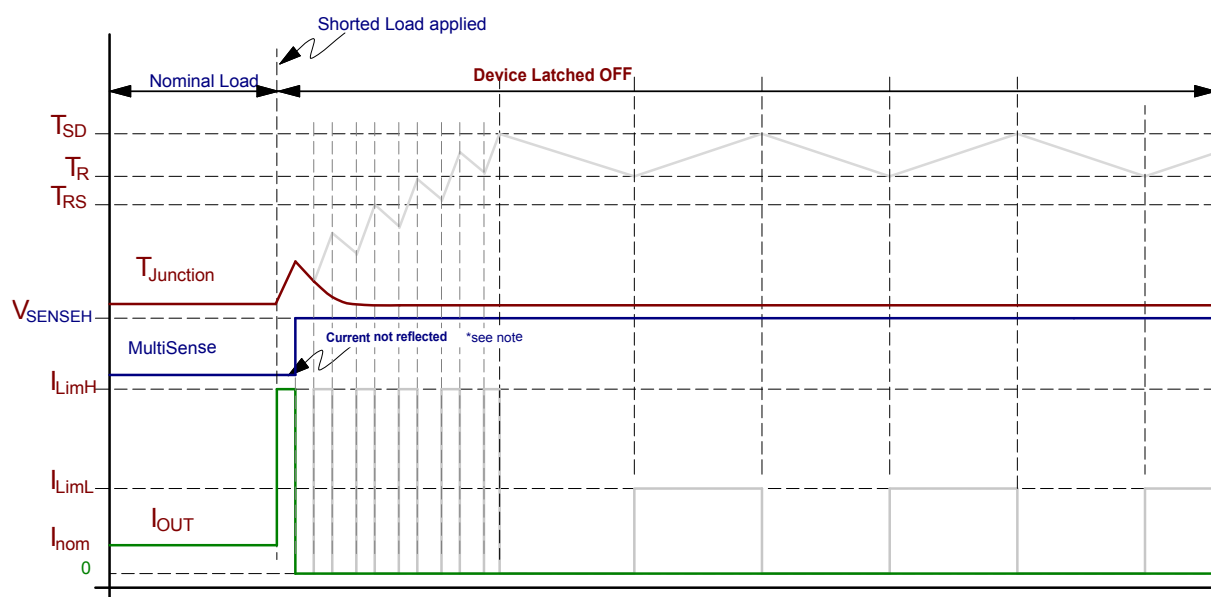


Figure 6 illustrates the conditions for a latch and how to reset it. While the FaultRST pin is high the High Side Driver will latch off at the first indication of a thermal overload (thermal shutdown or power limitation). A change in the input cannot reset the latch. This allows for a PWM control without repeatedly turning on into a faulty load.

Even after the part cools below the thermal reset temperature ( $T_{RS}$ ) the device will remain latched off until the FaultRST pin is lowered. Figure 7 illustrates the latching function at power limitation. This shows that with power limitation and a latch function there is very little stress on the part when driving a shorted load.

**Figure 7. Power limitation with latch**


**Note:** refer to UM1922, section 7.2.4, for further information

## Revision history

**Table 2. Document revision history**

Date	Version	Changes
05-Aug-2019	1	Initial release.

## Contents

<b>1</b>	<b>Severe load stresses</b>	<b>2</b>
1.1	Inrush	2
1.2	Shorted loads.	2
<b>2</b>	<b>Current limit</b>	<b>3</b>
<b>3</b>	<b>Power limitation</b>	<b>4</b>
3.1	Why power limitation	5
<b>4</b>	<b>Thermal shutdown</b>	<b>7</b>
<b>5</b>	<b>Two-Stage current limit</b>	<b>8</b>
<b>6</b>	<b>Fault indication</b>	<b>9</b>
<b>7</b>	<b>Latching function</b>	<b>10</b>
	<b>Revision history</b>	<b>12</b>

## List of tables

<b>Table 1.</b>	Multisense truth table for a dual output device . . . . .	9
<b>Table 2.</b>	Document revision history . . . . .	12

## List of figures

<b>Figure 1.</b>	VN7010AJ Thermal Sensor placement	4
<b>Figure 2.</b>	Power limitation on a shorted load.	5
<b>Figure 3.</b>	Inrush current mitigation	6
<b>Figure 4.</b>	Thermal shutdown response (no power limitation)	7
<b>Figure 5.</b>	Two stage current limit.	8
<b>Figure 6.</b>	Latch function.	10
<b>Figure 7.</b>	Power limitation with latch	11

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved