

## Double output, isolated PSR Flyback converter for Smart Meter and Power Line Communication systems using VIPER267KDTR

### Description

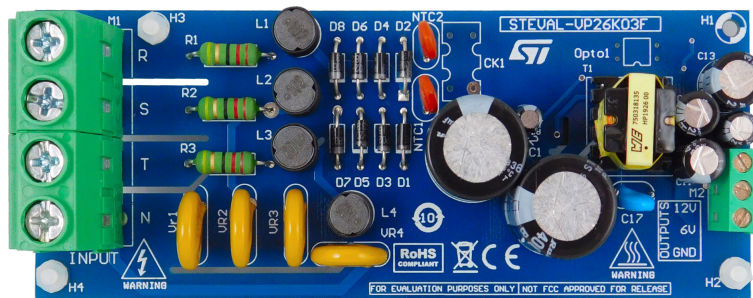
The **STEVAL-VP26K03F** evaluation board implements a double output isolated flyback with primary side regulation (PSR), specifically designed to supply smart meter and PLC systems.

The evaluation board has been developed using the **VIPER267KDTR** offline high-voltage converter, which features a 1050 V avalanche-rugged power section, PWM operation at 60 kHz with frequency jittering for lower EMI, current limiting with 700 mA fixed set point, on-board soft-start, safe auto-restart after fault and low standby power.

The power supply provides 12 V at 700 mA<sub>rms</sub> (1 A peak) to the power line modem (PLM) and the analog circuitry, and 6 V at 200 mA to supply digital circuitry and other low voltage parts.

The power supply is designed to operate across a three-phase input mains from 50 to 290 V<sub>AC</sub>, but can also be connected to a single phase mains from 85 to 500 V<sub>AC</sub>.

Figure 1. STEVAL-VP26K03F evaluation board top



### RELATED LINKS

*The board can also be configured for SSR operation. Refer to STEVAL-VP26K02F*

## 1 Features and specifications

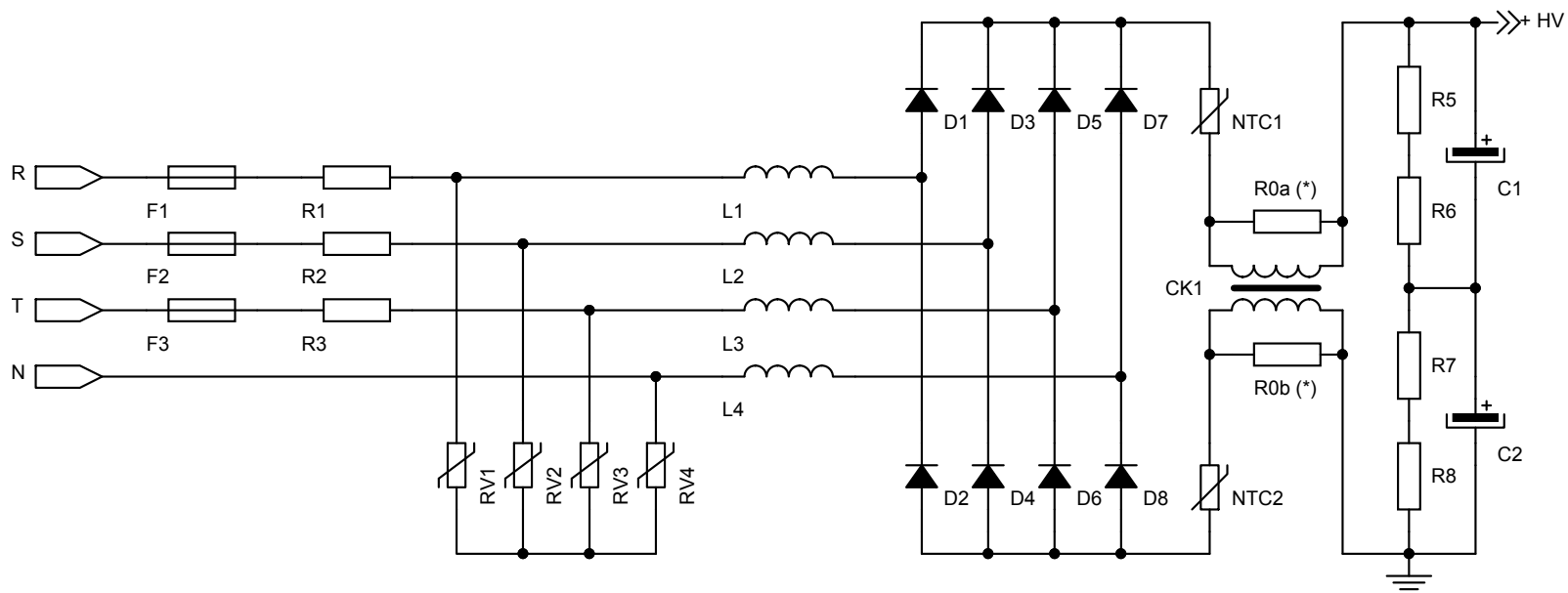
**Table 1. STEVAL-VP26K03F electrical specifications**

Parameter	Min.	Typ.	Max.
Operative AC main input voltage (3-phase connection)	50 V <sub>AC</sub>	-	290 V <sub>AC</sub>
Operative AC main input voltage (2-phase connection)	85 V <sub>AC</sub>	-	498 V <sub>AC</sub>
Mains frequency	47 Hz	-	63 Hz
Output voltage 1 – V <sub>OUT1</sub>	11 V	12 V	16 V
Output current 1 – I <sub>OUT1</sub>	10 mA	-	700 mA (rms)
	-	-	1000 mA (peak)
Output voltage 2 – V <sub>OUT2</sub>	5.5 V	6 V	7 V
Output current 2 – I <sub>OUT2</sub>	10 mA	-	200 mA
Maximum peak power	-	-	13.2 W
Maximum rms power	-	-	9.6 W
Efficiency at full load	-	78%	-
Ambient operating temperature	-40 °C	-	85 °C

## 1.1

## Schematic diagrams

Figure 2. STEVAL-VP26K03F schematic - input section



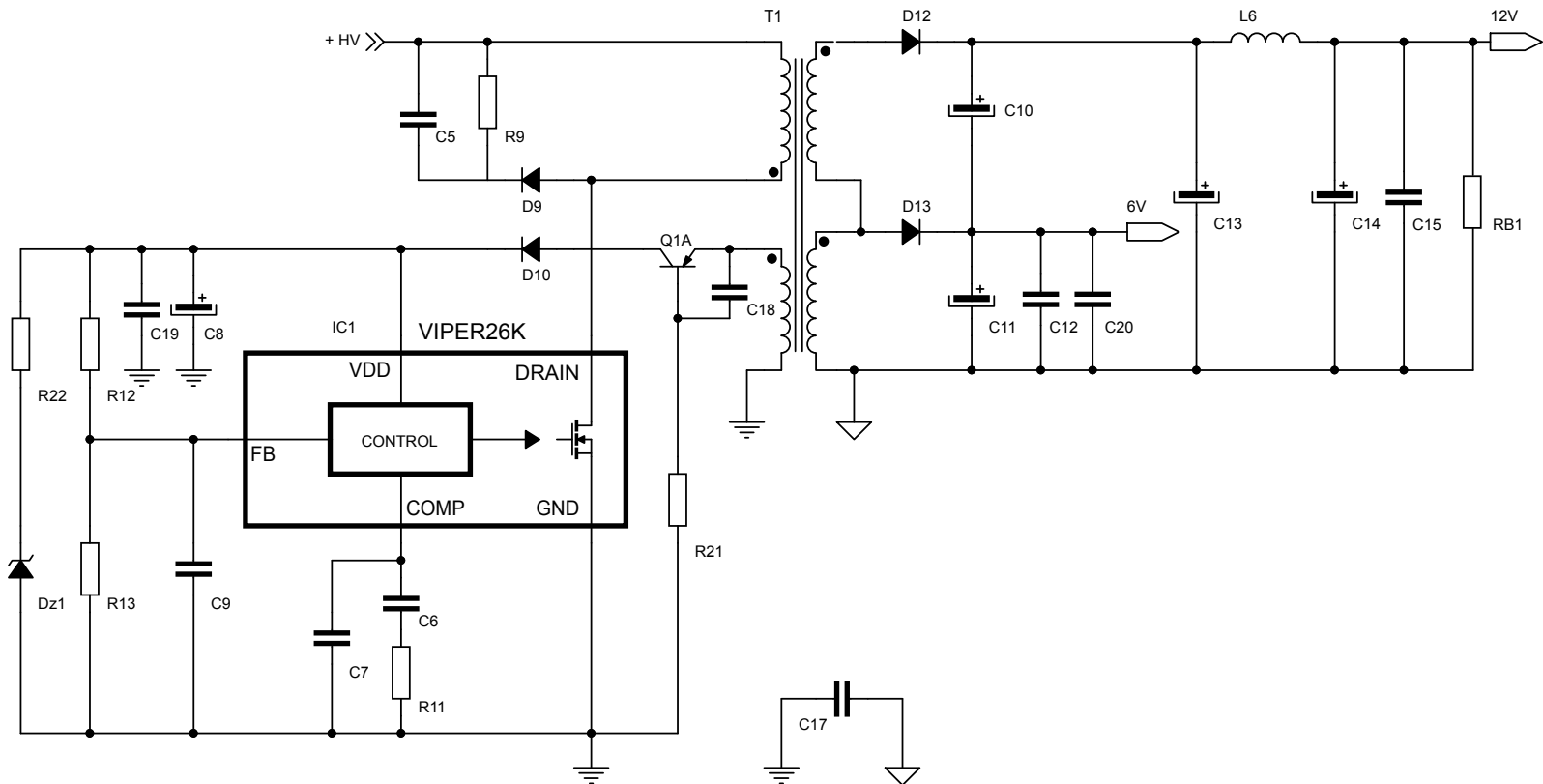


Figure 3. STEVAL-VP26K03F schematic - converter section



## 1.2 Bill of materials

**Table 2. STEVAL-VP26K03F bill of materials**

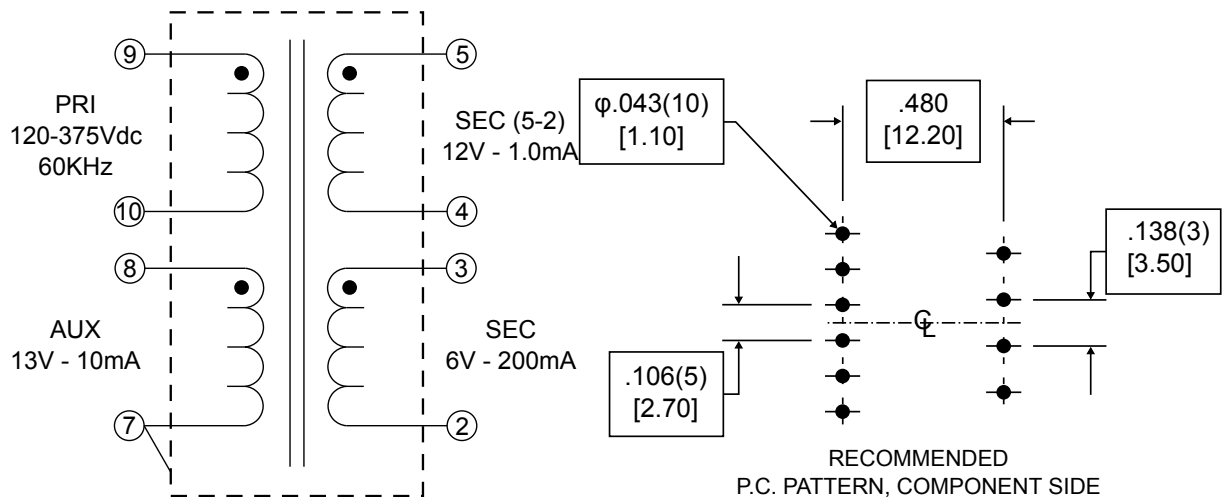
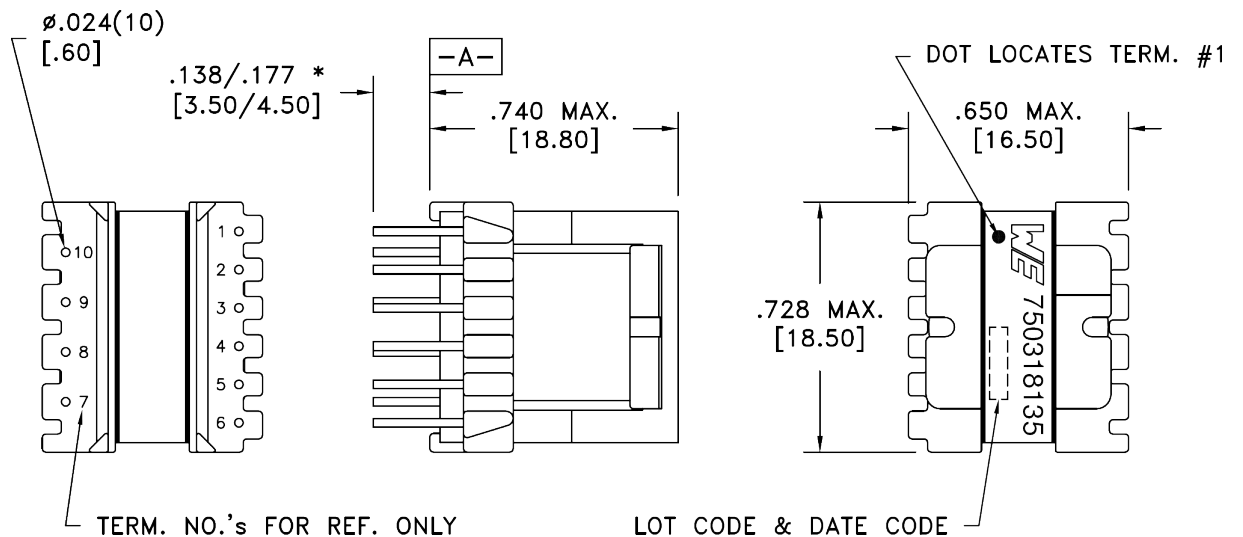
Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	3	R1, R2, R3	22 $\Omega$ , 1W, $\pm 5\%$	Metal Oxide Resistor, TH	TE Connectivity	EP1W22RJ
2	4	R5, R6, R7, R8	1M $\Omega$ , 0.33W, $\pm 5\%$	Resistor, 1206	Panasonic	ERJP08J105V
3	1	R9	220 K $\Omega$ , 0.25W, $\pm 5\%$	Resistor, 1206	Panasonic	ERJT08J224V
4	2	R11, R21	10 K $\Omega$ , $\pm 1\%$	Resistor, 0603	TE Connectivity	CRG0603F10K
5	2	R0a, R0b,	0 $\Omega$ , 0.25W, $\pm 1\%$	Resistor, 0603	Vishay	CRCW06030000Z0EAHP
6	1	R12	150 K $\Omega$ , $\pm 1\%$	Resistor, 0603	Vishay	CRCW0603150KFKEA
7	1	R13	43 K $\Omega$ , $\pm 1\%$	Resistor, 0603	Vishay	CRCW060343K0FKEA
8	1	R22	47 $\Omega$ , 0.125W, $\pm 1\%$	Resistor, 0603	TE Connectivity	CRG0805F47R
9	1	Rb1	8.2 K $\Omega$ , 0.125W, $\pm 1\%$	Resistor, 0603	TE Connectivity	CRG0603F8K2
10	13	R10, R14, R15, R16, R17, R18, R19, R20, C16, C22, OPTO1, IC2, CK1	-	Not mounted	-	-
11	2	C1, C2	68 $\mu$ F, 400 Vcc - 105°C, $\pm 20\%$	Electrolitic Capacitor, TH D=18 mm, H=25 mm, P=7.5 mm	Rubycon	400BXC68MEFC18X25
12	1	C5	1 nF 630 Vdc, 630 Vdc, $\pm 5\%$	Multi layer capacitor, 1206	TDK	C3216C0G2J102J085AA
13	2	C7, C9	1 nf, 200 Vdc, $\pm 5\%$	Multi layer capacitor, 0603	TDK	C3216C0G2J102J085AA
14	1	C8	47 $\mu$ F, 35 Vdc, $\pm 20\%$	Electrolitic Capacitor, H D=4 mm, H=7 mm, P=1.5 mm	Rubycon	-
15	2	C10, C11	220 $\mu$ F, 25 Vcc, +105°C, $\pm 20\%$	Electrolitic Capacitor, TH D=6.3 mm, H=11 mm, P=2.5 mm	Rubycon	35ZLH220MEFC8X11.5
16	3	C6, C12, C15	100nF, 25 Vcc, $\pm 10\%$	Multi layer capacitor, 0603	KEMET	C0603C104K3RACTU
17	1	C13	470 $\mu$ F, 35 Vcc, +105°C, $\pm 20\%$	Electrolitic Capacitor, TH D=10 mm, H=12.5 mm, P=5 mm	Rubycon	25ZLH470MEFC10X12.5
18	1	C14	100 $\mu$ F, 35 Vcc, +105°C, $\pm 20\%$	Electrolitic Capacitor, TH D=6.3 mm, H=11 mm, P=2.5 mm	Rubycon	35ZLH100MEFC6.3X11
19	1	C17	2.2nF, 250 Vac	X1 Y2 Capacitor, TH 8 mm X 5 mm, P 7.5 mm	Murata	DE2E3KY222MA2BM01F

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
20	1	C18	330 pF, 10 Vdc, ±5%	Multi layer capacitor, 0603	Vishay	VJ0603A331JXBAC
21	1	C19	100pF, 250 Vdc, ±5%	Multi layer capacitor, 0603	TDK	CGA3E3C0G2E101J080AA
22	1	C20	1µF, 25 Vdc, ±10%	Multi layer capacitor, 0603	Murata	GRM188C81E105KAADD
23	3	F1, F2, F3	2A	Fuse, 10.1mm X 1.43 mm	Schurter	3403.0169.24
24	1	T1	LP 1.5 mH, out1 12V, out2 6V	WURTH_75031813 5r00 Flyback Transformer	Würth Elektronik	750318135
25	4	L1, L2, L3, L4	1mH	Inductor, TH, D 8mm, P 5mm, H 10mm	Würth Elektronik	7447728102
26	1	L6	3.3 µH / 33 mΩ, 3.23A	Inductor, Lu x La: 0,157 x 0,157" (4,00 x 4,00 mm)	Würth Electronics Inc	74404043033A
27	2	NTC1, NTC2	10 Ω	PTC, TH 9 mm X 4 mm , P 5mm	Murata	NTPA7100LBMB0
28	1	Dz1	22 V, 22, 0.5W	Zener Diode, SOD 123	ON Semiconductor	MMSZ22T1G
29	4	VR1, VR2, VR3, VR4	Vrms=275, VDCmax=350V, ,W max=155J	275 Vac Metal Oxide Varistor, TH series 14, 16.5mm X 4.5mm	Würth Elektronik	820442711E
30	1	Q1	BC807, 45, 0.5, HFE 30	pnp Bipolar Transistor, SOT23	ON Semiconductor	BC807-40LT3G
31	8	D1, D2, D3, D4, D5, D6, D7, D8	RGP02-20E-E3/54, 1800V	High Voltage Rectifier Diode, TH Axial, Body 5.2 x 2.7	Vishay	RGP02-20E-E3/54
32	1	D9	-	Rectifier Diode, SMA	ON Semiconductor	MRA4007T3G
33	1	D10	150 V, 1 A	Schottky Diode, SMA	ST	<a href="#">STPS1150A</a>
34	1	D12	200 V, 10 A	Schottky Diode, SMA	ST	<a href="#">STPS2200UF</a>
35	1	D13	100 V, 1 A	Schottky Diode, SMA	ST	<a href="#">STPS1H100A</a>
36	1	IC1	1050 V	SMPS IC	ST	<a href="#">VIPER267KDTR</a>
37	2	M1	M.4 TH	2-way terminal block	Phoenix Contact	1706785
38	1	M2	M.3 TH	3-way terminal block	Phoenix Contact	1725669
39	4	H1, H2, H3, H4	9.5 mm	Hex spacers	Richco	HS 4 3

### 1.3 Transformer

**Table 3. Transformer characteristics**

Manufacturer	Würth Elektronik
Part number	750318135
Core	E16
Primary Inductance	1.5 mH $\pm 10\%$
Saturation current	950 mA (20% roll-off from initial)
Leakage inductance	100 $\mu$ H typ., 200 $\mu$ H max.
Primary-to-auxiliary turns ratio	5.03 $\pm 1\%$
Primary-to-sec1 turns ratio	10.94 $\pm 1\%$
Primary-to- sec2 turns ratio	10.94 $\pm 1\%$

**Figure 4. Dimensional drawing, pin placement (distances, bottom view) and electrical diagrams**

**Figure 5. Dimensional drawing and pin placement diagram (bottom, side and top view)**


## 2 Circuit description

### 2.1 Input stage and filtering

The input stage is designed for the power supply to sustain operation at up to 500 V<sub>AC</sub>. It consists of three fuses (F1, F2 and F3) implemented to prevent catastrophic failure and two input NTCs to limit the inrush current of the capacitors during startup and to protect the three-phase bridge rectifier (BR). The total required resistance of the NTC is divided into two for safe operation of the NTC components without exceeding the allowed voltage rating across them.

The total bulk capacitance consists of two capacitors in series for a total voltage rating above the maximum operating rectified input voltage (730V<sub>DC</sub> approx.); resistors R5 to R8 ensure equal voltage sharing between the capacitors.

Special care has been placed on filtering conducted converter noise to render powerline communication less sensitive to the switching power supply. Both differential and common mode filters have been implemented.

### 2.2 Snubber network

A low cost RCD (R9-C5-D9) clamp is implemented for the snubber network to limit the leakage inductance voltage spike by dissipating the associated energy during MOSFET turn-off to ensure reliable power supply operation.

The 1050 B<sub>V</sub>DSS voltage of the **VIPER26K** means that further protection against input overvoltage using a parallel transil diode is not required.

The adoption of this low-cost clamp configuration helps to improve EMC performance through smooth drain voltage ringing slopes, and the absence of the transil eliminates a loop that could degrade EMI performance.

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#### RELATED LINKS

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[Appendix B Effect of output LC post filter stage in flyback converters on page 20](#)

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### 2.3 HV converter

The core of the power supply is the **VIPER267KDTR** offline high-voltage converter with 1050 V avalanche-rugged power section with a maximum R<sub>DS(on)</sub> ≤ 8.5 Ω, and a current-mode 60 kHz fixed frequency PWM controller.

The device includes several features which considerably reduce the overall BoM cost and improve system reliability.

Control is achieved by adjusting the voltage on COMP pin, which transfers the output voltage information via the optocoupler. Capacitor C7 connected across the pin is used for appropriate loop compensation.

During normal operation, the V<sub>DD</sub> pin is powered by the output of the auxiliary winding of the transformer, which is rectified by diode D10 and capacitor C8. Resistor R4 is used to filter the auxiliary spikes at turn-off, and limit voltage fluctuation on the pin. Capacitor C19 is used to filter any narrow voltage spikes entering the V<sub>DD</sub> pin. A clamp network consisting of R22 and Dz1 is connected across the V<sub>DD</sub> pin to avoid transient voltages exceeding the absolute maximum rating of the pin.

### 2.4 Output stage

The secondary of the transformer is designed for a two-output option: the secondary windings are wound using a stack arrangement to improve the cross regulation of the non-regulated output.

The first secondary signal is rectified by diode D12 and filtered by output capacitor C13, and is designed to allow sufficient AC ripple capability to avoid component overheating. The L6-C14 post filter is used to further reduce the residual output ripple, while capacitors C15 and C21 further reduce the output switching noise.

The other secondary signal is rectified by diode D13 and capacitor C11.

The output voltage is sensed by voltage divider R12 and R13 and compared with the internal 3.3 V reference of the integrated error amplifier; its output is then converted via the internal OTA into a current control signal for the primary PWM IC.

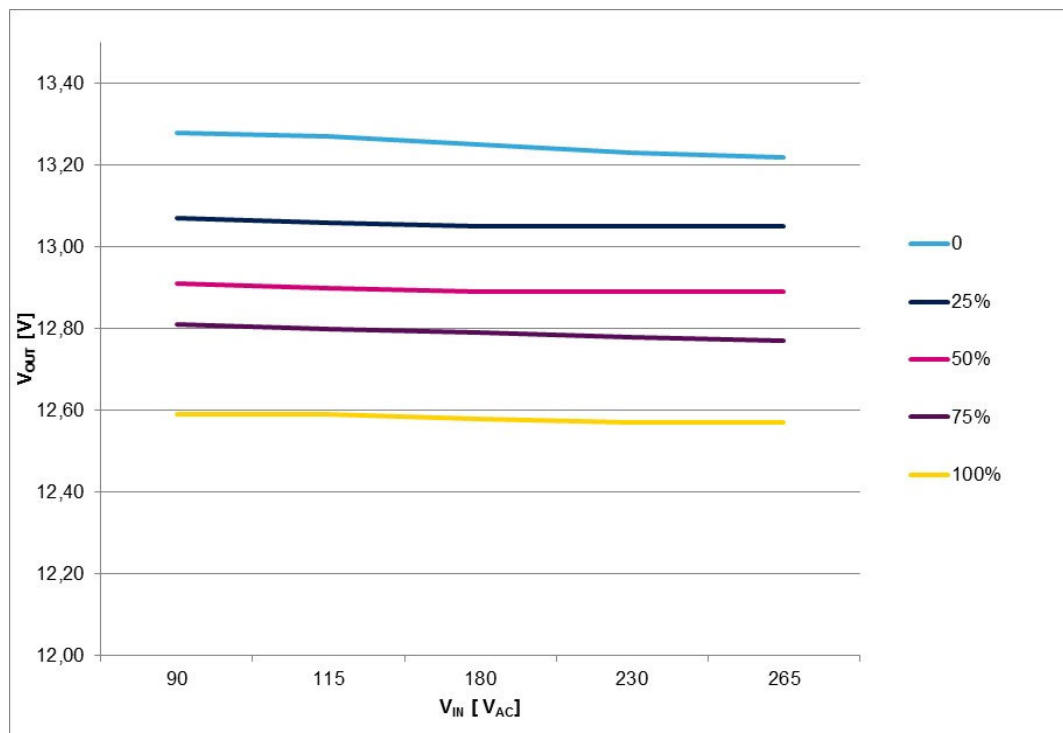


### 3 Performance data

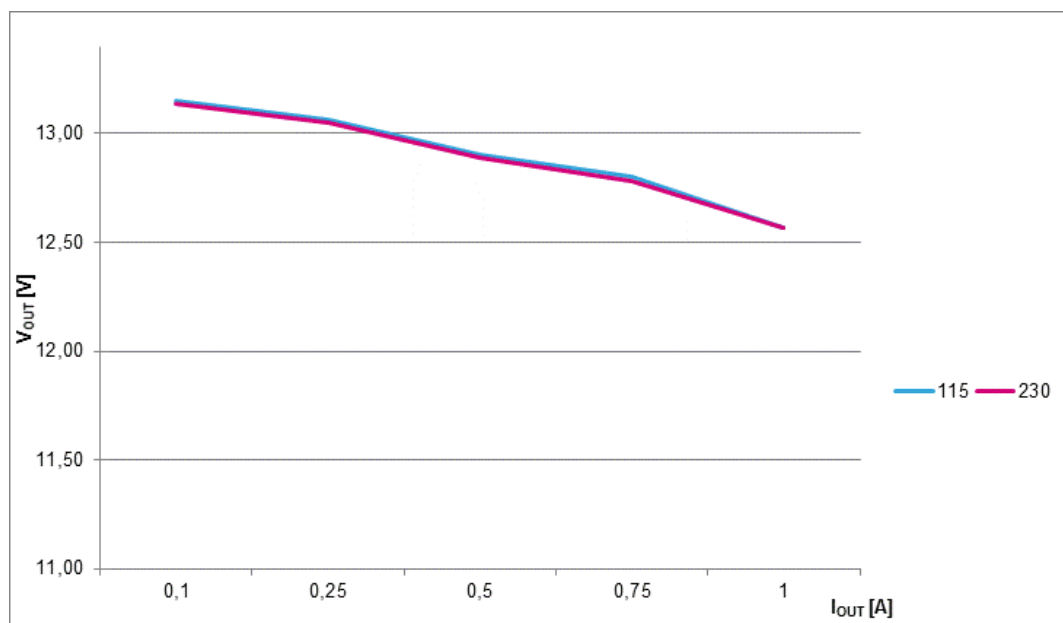
#### 3.1 Output voltage characteristics

The line and load regulation of the board is measured at the PCB output connectors for both 115 V<sub>AC</sub> and 230 V<sub>AC</sub>.

**Figure 6. Line regulation at different loads**



**Figure 7. Load regulation at 115 V<sub>AC</sub> and 230 V<sub>AC</sub>**



## 3.2 Efficiency and light load measurements

The efficiency and the light load consumption of the converter are measured at nominal input voltages (115 V<sub>AC</sub> and 230 V<sub>AC</sub>).

**Table 4. Efficiency at typical and maximum loads**

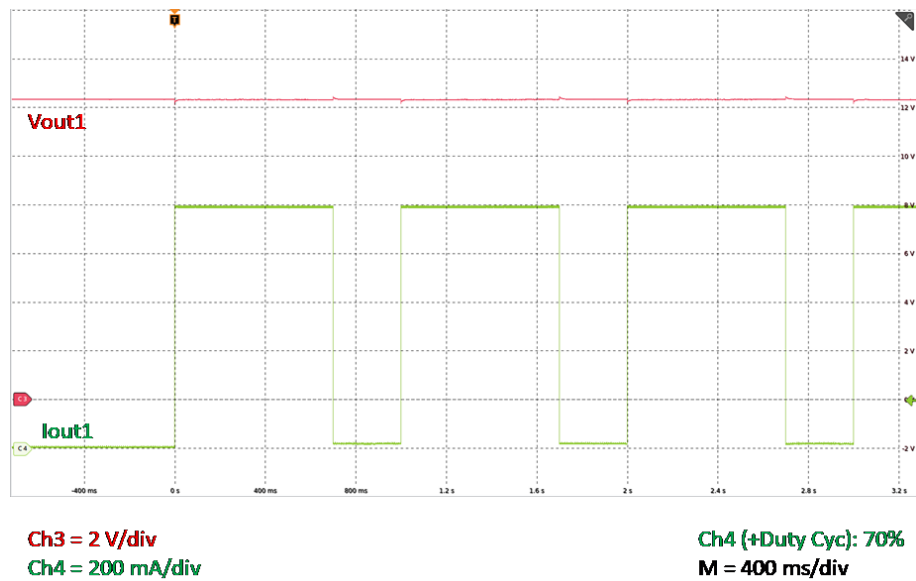
Output condition	Efficiency	
	115 V <sub>AC</sub>	230 V <sub>AC</sub>
12 V at 700 mA / 6 V at 200 mA	77.15%	79.92%
12 V at 1000 mA / 6 V at 200 mA	72.37%	76.45%

## 4 Typical waveforms

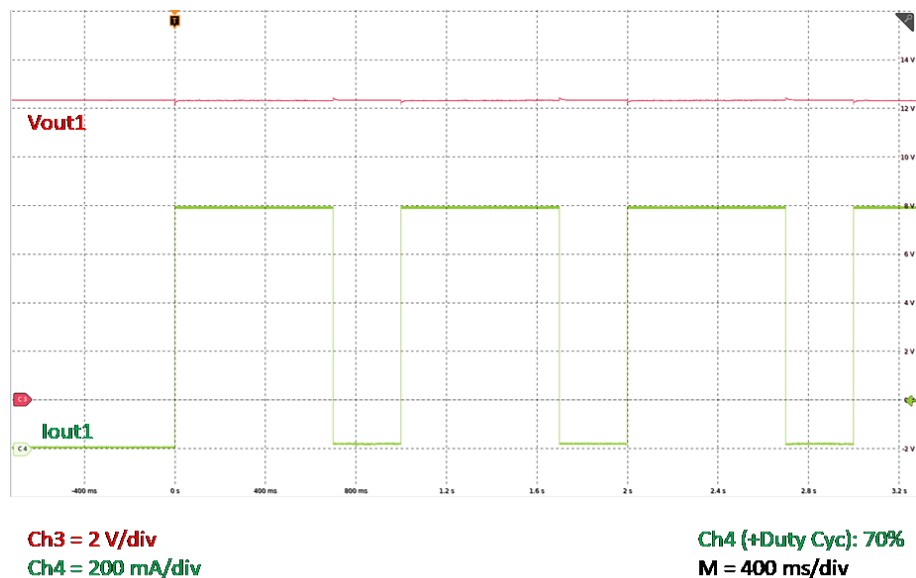
In TX mode, the load on output 1 changes from 10 to 1000 mA with a 1-Hz repetition rate and 70% duty cycle. Output 2 is loaded at typical values (200 mA).

During PLM operation, it is important that the output voltage remains regulated within specification limits to ensure correct operation of the PLM power amplifier (see [Figure 8](#) and [Figure 9](#)). The output voltage is quite stable and clean with no abnormal oscillation during load changes and the steady-state values are within specification by very good margins.

**Figure 8. Output voltage and current at 115 V<sub>AC</sub> (single phase connection)**

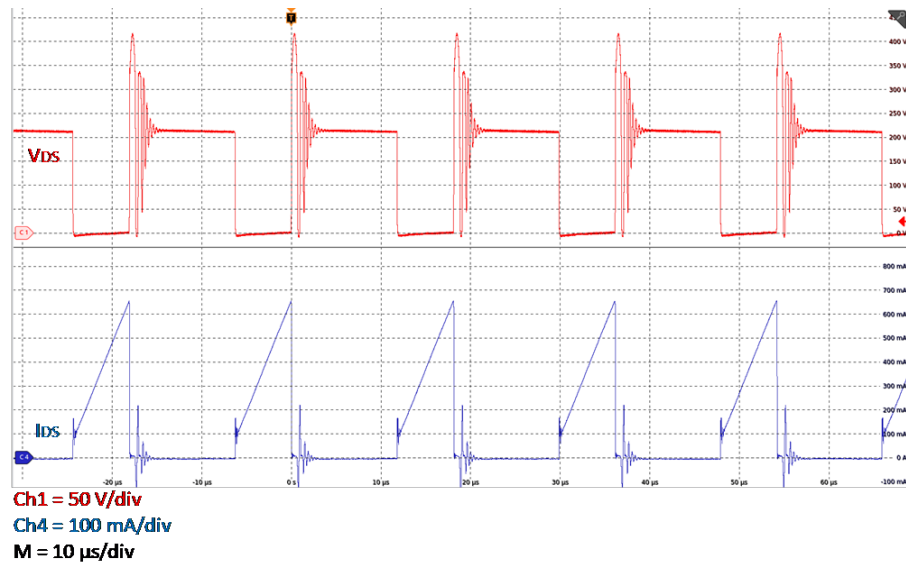


**Figure 9. Output voltage and current at 230 V<sub>AC</sub> (single phase connection)**

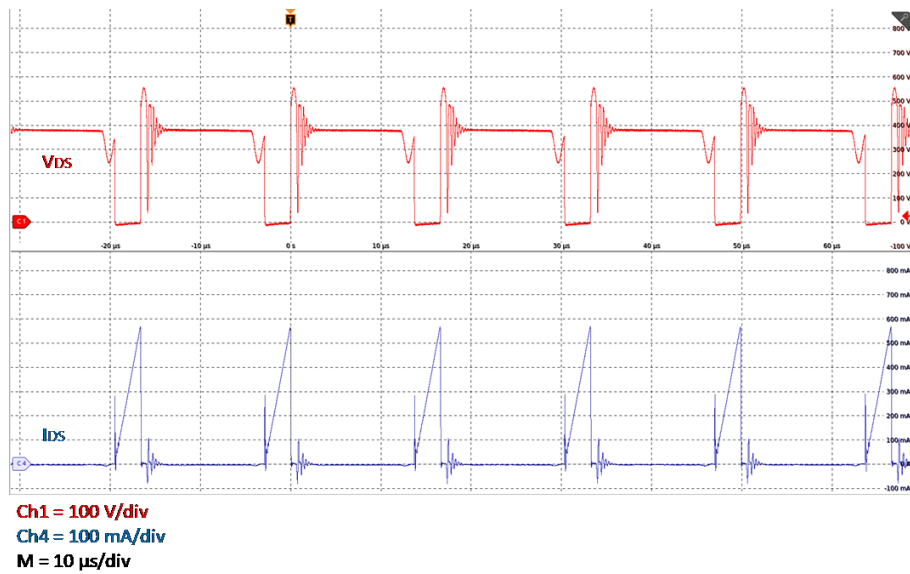


The drain voltage and the drain current waveforms are reported for the two nominal input voltages and for 500V<sub>AC</sub> (see [Figure 10](#) to [Figure 12](#)).

**Figure 10. Drain voltage and drain current at 115 V<sub>AC</sub> (single phase connection)**

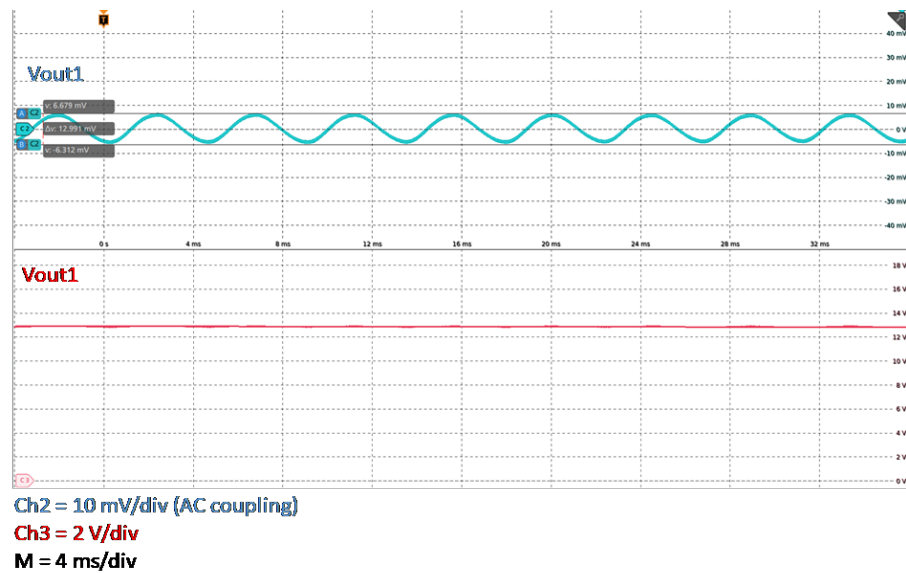


**Figure 11. Drain voltage and drain current at 230 V<sub>AC</sub> (single phase connection)**



**Figure 12. Drain voltage and drain current at 500 V<sub>AC</sub> (single phase connection)**


The output voltage ripple at 12 V output at nominal input voltage and full load is also measured (see Figure 13). It must be very low in order to ensure appropriate sensitivity during PLM operation. The measured value is extremely low at around 0.1% of the nominal output voltage.

**Figure 13. Low frequency ripple at 230 V<sub>AC</sub> (single phase connection)**


## 5 Noise measurements

The pre-compliance tests for conducted noise emissions as per EN55022 (Class B) European normative were performed using a Quasi-Peak detector and an Average detector of the conducted art nominal mains voltage, and compared with the associated limits.

Figure 14 and Figure 15 show that the measured results are well within their respective limits by a very good margin.

Figure 14. LINE conducted disturbance

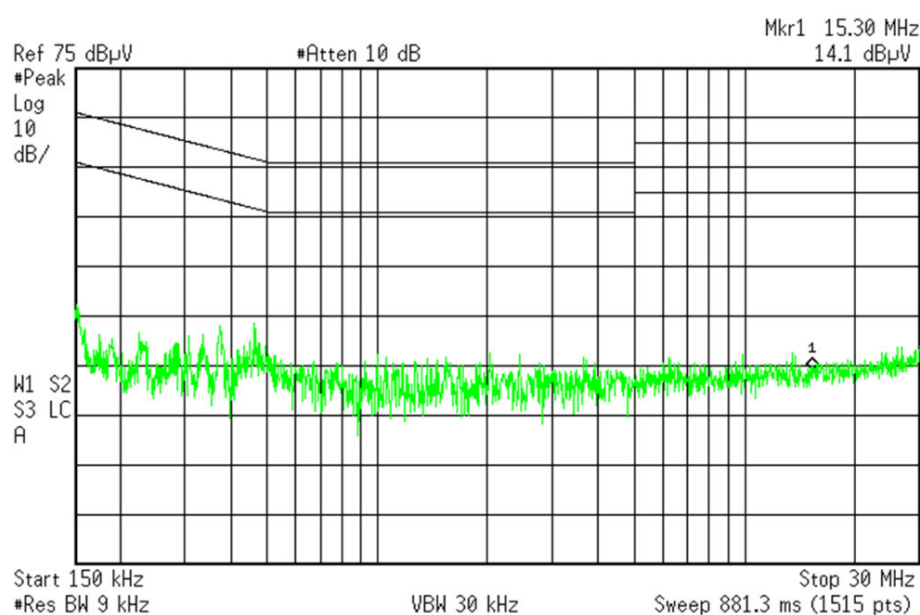
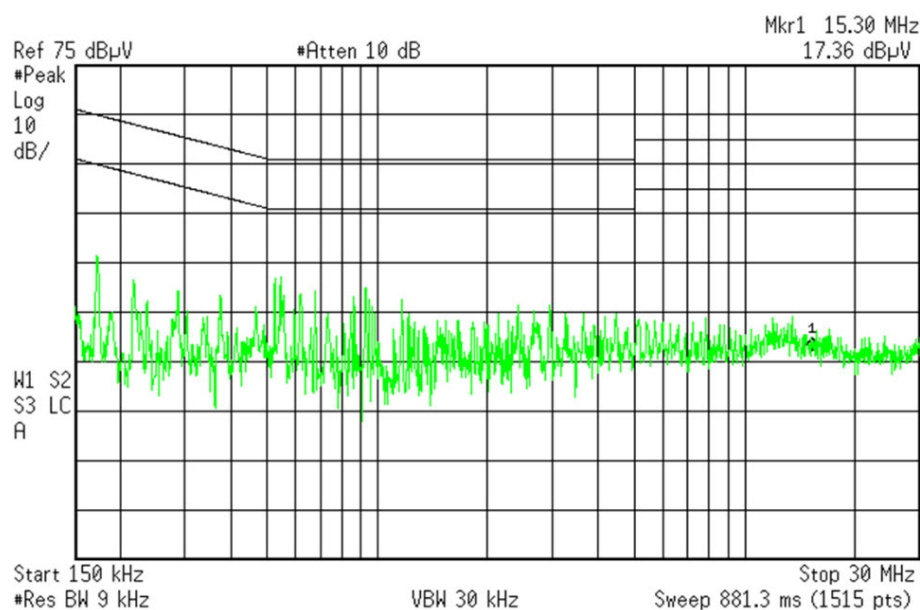


Figure 15. NEUTRAL conducted disturbance



## 6 Conclusion

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We tested our double output isolated PSR flyback converter design based on the [VIPER267KDTR](#), and we demonstrated that the input filter setup, its compliance with the European standards for smart metering and PLC applications, as well as for Electromagnetic compatibility, and the overall performance of the board render it suitable for use in Smart Meter and PLC systems.

## Appendix A CCM flyback converter transfer function

The control-to-output transfer function of the flyback converter in CCM,  $G_{vc}(s)$ , is given by the approximation:

$$G_{vc}(s) \approx H_O \cdot \frac{\left(1 + \frac{s}{\omega_{Z1}}\right) \cdot \left(1 - \frac{s}{\omega_{Z2}}\right)}{1 + \frac{s}{\omega_{P1}}} \quad (1)$$

Gain, poles and zero are defined below:

$$H_O = \frac{n \cdot R_O}{H_{COMP}} \cdot \frac{1-D}{1+D} \quad (2)$$

$$\omega_{Z1} = \frac{1}{R_C \cdot C_O} \quad (3)$$

$$\omega_{Z2} = \frac{n^2 \cdot (1-D)^2 \cdot R_O}{D \cdot L} \quad (4)$$

$$\omega_{P1} = \frac{1+D}{R_O \cdot C_O} \quad (5)$$

### A.1 CCM flyback type-2 compensator design

To compensate the CCM flyback, we use a type-2 compensator featuring the integrator effect that provides high DC gain to minimize static error, as well as a pole-zero pair to boost the phase according to the phase margin target.

The compensator is determined using a manual pole-zero placement technique in which the zero is placed in the vicinity of the power stage dominant pole to cancel its effect and the pole position is adjusted to achieve the required phase margin.

Follow the procedure below to design compensation with a type 2 compensator:

**Step 1.** Select the crossover frequency  $f_C$  and the phase margin  $\phi_m$ :

For CCM flyback, the crossover frequency must be selected as low as possible with respect to the RHP zero  $\omega_{Z2}$  in order to limit the phase degradation that it introduces.

As a general rule, you should set  $f_C$  to below 20% of the RHP zero.

**Step 2.** Evaluate the gain and phase of the plant at crossover frequency:

$$G_{vc}(f_C) = |G_{vc}(2 \cdot \pi \cdot f_C)| \quad (6)$$

$$\Phi_{vc}(f_C) = \arg[G_{vc}(2 \cdot \pi \cdot f_C)] \quad (7)$$

**Step 3.** Design the compensator to have following gain and phase (at  $f_C$ ):

The compensated open-loop gain must attain unit gain at  $f_C$ , with the required phase margin.

$$G_c(f_C) = |G_c(2 \cdot \pi \cdot f_C)| = \frac{1}{G_{vc}(f_C)} \quad (8)$$

$$\Phi_c(f_C) = \arg[G_c(2 \cdot \pi \cdot f_C)] = 90 - 180 + \Phi_m - \Phi_{vc}(f_C) \quad (9)$$

**Step 4.** Cancel the pole of the plant  $f_{P(p)}$  by placing the zero of the compensator  $f_{Z(c)}$  in the neighborhood ( $\alpha = 1$  to 5):

$$f_{Z(c)} = \frac{\omega_{Z(c)}}{2 \cdot \pi} = \alpha \cdot f_{P(p)} \quad (10)$$

**Step 5.** Place the pole of the compensator to boost the phase and to obtain the desired phase margin:

$$f_{P(c)} = \frac{f_C}{\tan\left[\tan^{-1}\left(\frac{f_C}{f_{Z(c)}}\right) - \Phi_c(f_C)\right]} \quad (11)$$



**Step 6.** Calculate the gain  $G_{co}$  :

$$G_{co} = G_c(f_C) \cdot \frac{\omega_C \cdot \sqrt{1 + \left(\frac{f_C}{f_{P(c)}}\right)^2}}{\sqrt{1 + \left(\frac{f_C}{f_{Z(c)}}\right)^2}} \quad (12)$$

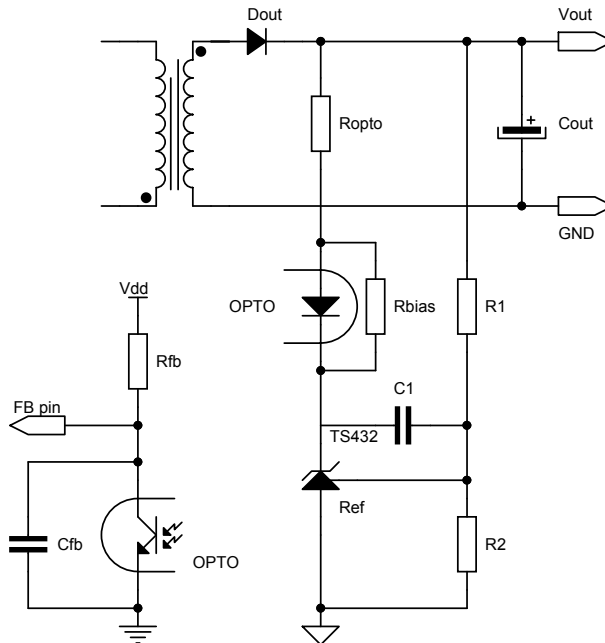
$G_C(s)$  is thus determined.

## A.2

### Compensator implementation

Figure 16 shows the complete schematic arrangement for the type-2 error amplifier in secondary side regulation (SSR). The resistors  $R_1$  and  $R_2$  are used to define the output voltage setpoint. The resistor  $R_{OPTO}$  is used to bias the emitter, while the resistor  $R_{BIAS}$  is used to provide the minimum biasing current to the reference voltage IC. The capacitors  $C_1$  and  $C_{FB}$  are used for the compensation, even if the other components also affect the overall compensator transfer function.

**Figure 16. Secondary feedback implementation using secondary reference voltage and optocoupler**



The transfer function of the compensator can be expressed as:

$$G_C(s) = \frac{CTR \cdot R_{FB}}{R_{OPTO}} \cdot \frac{1 + \frac{1}{s \cdot R_1 \cdot C_1}}{1 + s \cdot R_{FB} \cdot (C_{FB} + C_{OPTO})} \quad (13)$$

In the equation, capacitor  $C_{OPTO}$  is the intrinsic capacitor across the collector that introduces a pole in the transfer function and limits the frequency response. As this pole becomes part of the controller transfer function, specific test measurements are required to determine the correct value as close as possible to the real operating conditions of the selected optocoupler.

Component selection is based on the procedure shown below.

**Step 1.** First calculate the value of the resistor  $R_{BIAS}$  .

The purpose of this resistor is to provide the minimum bias current to the reference IC necessary for correct operation. Considering that the forward voltage of the opto-diode is almost constant (typically  $\approx 1$  V), the value of  $R_{BIAS}$  is simply given by:

$$R_{BIAS} \leq \frac{V_F}{I_{BIAS}} \quad (14)$$

**Step 2.** The next step is the selection of  $R_1$ .

The value must be high enough to minimize the residual losses across the output, but low enough to ensure that the input current of the REF pin of the reference IC is negligible compared with the current across  $R_1$  itself: a general rule is to set the current across  $R_1$  30 to 50 higher than the REF input current.

**Step 3.** Select resistor  $R_2$  to define the output voltage set-point:

$$R_2 = R_1 \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad (15)$$

**Step 4.** Calculate the value of capacitor  $C_1$  to fix the zero  $f_{Z(c)}$ :

$$C_1 = \frac{1}{2\pi \cdot R_1 \cdot f_{Zc}} \quad (16)$$

**Step 5.** Set the value of  $R_{OPTO}$  to fix the mid-band gain  $G_{co}$ :

$$R_{OPTO} = \frac{CTR \cdot R_{FB}}{G_{co}} \quad (17)$$

**Step 6.** Check that  $R_{OPTO}$  satisfies the following equation:

This is to ensure the minimum current through the optodiode to properly drive the FB pin with the current  $I_{FB}$ , ensuring the full dynamic of the pin.

$$R_{OPTO} \leq \frac{V_{OUT} - V_F - V_{REF}}{\frac{I_{FB}}{CTR} + \frac{V_F}{R_{BIAS}}} \quad (18)$$

**Step 7.** Set the value of  $C_{FB}$  to fix the proper phase boost of the compensator:

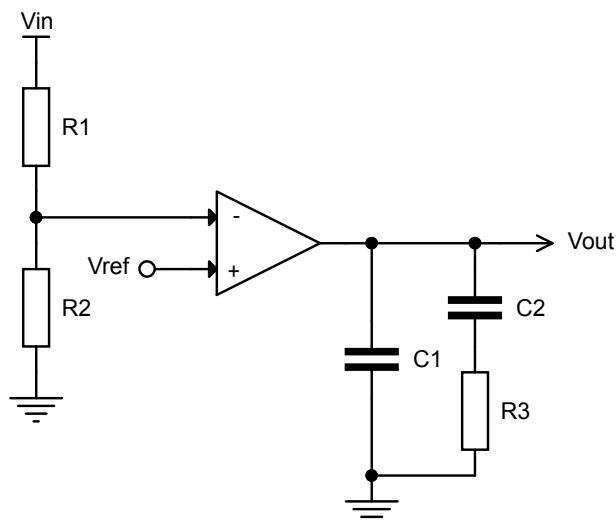
$$C_{FB} = \frac{1}{2\pi \cdot R_{FB} \cdot f_{Pc}} - C_{OPTO} \quad (19)$$

The design of  $G_C(s)$  is now ready.

### A.3 Compensator implementation of PSR

A type-2 compensator with OTA is used for PSR, as shown in the following figure.

**Figure 17. Type 2 compensator with OTA**



The transfer function of the compensator can be expressed as:

$$G_C(s) = \frac{N_{AUX}}{N_{SEC}} \cdot \frac{R_{EA} \cdot R_2 \cdot g_m}{R_1 + R_2} \cdot \frac{1 + s \cdot R_3 \cdot C_2}{(1 + s \cdot R_0 \cdot C_2) \cdot [1 + s \cdot R_3 \cdot (C_1 + C_{EA})]} \quad (20)$$

The terms  $C_{EA}$  and  $R_{EA}$  are the output capacitance and the output resistance of the error amplifier, which are 400 pF and 1.1 MΩ respectively in the Viper26K.

The first component to be chosen is the resistor  $R_1$ , which must be high enough to render the current offset entering the inverting pin negligible, but low enough so that other compensation components are not too large. Resistor  $R_2$  is fixed to set the DC operating point of the loop. Both  $R_1$  and  $R_2$  play a role in the definition of the gain of the compensator.

The remaining components can be calculated.

$$C_1 = \frac{f_{Z1}}{f_{P1}} \cdot \frac{R_2 \cdot g_m}{G_{CO} \cdot (R_1 + R_2)} - C_{EA} \quad (21)$$

$$C_2 = \frac{R_2 \cdot g_m}{G_{CO} \cdot (R_1 + R_2)} - (C_1 + C_{EA}) \quad (22)$$

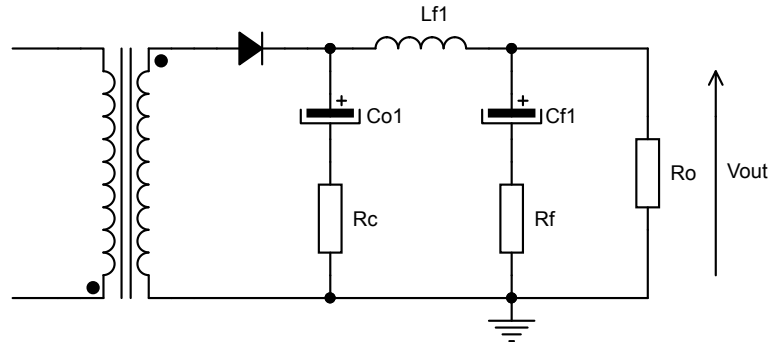
$$R_3 = \frac{1}{2\pi \cdot f_{Z1} \cdot C_2} \quad (23)$$

## Appendix B Effect of output LC post filter stage in flyback converters

Large capacitors are usually used in flyback converters to build the output filter, and it is important to factor in the RMS ripple rating and the parasitic resistance ESR when determining the size of the capacitor to satisfy the output ripple specification.

When the requirement of the ripple is very tight, a simple low cost LC filter can be used to attenuate the ripple to the desired level instead of using a large number of capacitors that increase the cost.

**Figure 18. Output LC post filter for ripple reduction**



Although this solution is very simple and cost effective, it changes the behavior of the plant and extra care must be placed to deal with the compensation design.

Assuming that  $C_O$  is much larger than  $C_F$ , the total transfer function of the plant in presence of the LC filter can be expressed as:

$$G'_{vc}(s) = G_{vc}(s) \cdot \frac{1 + \frac{s}{\omega_{ZF}}}{1 + \frac{s}{\omega_F \cdot Q_F} + \left(\frac{s}{\omega_F}\right)^2} \quad (24)$$

Where:

$$\omega_F = \frac{1}{\sqrt{L_F \cdot C_F}} \quad (25)$$

$$Q_F = \frac{1}{\frac{1}{R_O} \cdot \sqrt{\frac{L_F}{C_F}} + (R_F + R_C) \cdot \sqrt{\frac{C_F}{L_F}}} \quad (26)$$

Where  $G_{vc}(s)$  is the transfer function of the plant without the filter, given in Eq. (1).

The presence of the LC output post filter introduces a further zero and a pair of poles in the transfer function. This causes a peak at frequency  $\omega_F/2\pi$  to appear in the amplitude diagram and a sudden  $180^\circ$  reduction of the phase to occur at the same frequency. Therefore, when you use an LC post filter, it is necessary to design its resonance frequency well above the crossover frequency to keep the resonance peak outside the converter band and to avoid eroding the phase margin or going as far as making the system unstable.

In our board, the LC filter is designed to have the pole pair at frequency  $f_F = 8.76\text{kHz}$ , with a quality factor equal to  $Q_F = 0.801$ , ensuring negligible phase margin erosion at the crossover frequency.

### RELATED LINKS

[2.2 Snubber network on page 8](#)

## Appendix C Layout guidelines and design recommendations

An appropriate PCB layout is essential for the correct operation of any switch-mode converter. It ensures the delivery of clean signals to the IC and higher immunity to external and switching noise, as well as reducing radiated and conducted electromagnetic interference, all of which help a given solution satisfy EMC requirements. Below are some general concepts to keep in mind when designing SMPS circuit layouts.

Separate signal and power tracks:

- Traces carrying signal currents should generally be run at a distance from other tracks carrying pulsed currents or with rapidly changing voltages.
- Signal ground traces should be connected to the IC signal ground, GND, using a single "star point", placed close to the IC.
- Power ground traces should be connected to the IC power ground, GND.
- The compensation network should be connected to the COMP, maintaining the trace to GND as short as possible.
- In two-layer PCBs, it is a good practice to route signal traces on one PCB side and power traces on the other side.

Filter sensitive pins and crucial points on the circuit:

- A small high-frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests.
- A low ESL ceramic capacitor (a few hundred pF up to 0.1  $\mu$ F) should be connected across VCC and GND, placed as close as possible to the IC.
- With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track.

Keep power loops as confined as possible:

- Minimize the area circumscribed by current loops where highly pulsed currents flow in order to reduce its parasitic self-inductance and the radiated electromagnetic field; this will greatly reduce the electromagnetic interferences produced by the power supply during the switching.
- In a flyback converter the most critical loops are:
  - The one with the input bulk capacitor, the power switch and the power transformer
  - the one with the snubber.
  - the one with the secondary winding, the output rectifier and the output capacitor.
- In a buck converter the most critical loop is:
  - The one with the input bulk capacitor, the power switch, the power inductor, the output capacitor and the free-wheeling diode.

Reduce line lengths as any wire will act as an antenna:

- With the very short rise times exhibited by EFT pulses, any antenna has the capability of receiving high voltage spikes. Shorter lines reduce the level of radiated energy received and lower the spikes resulting from electrostatic discharges. This will also keep both resistive and inductive effects to a minimum.
- All traces carrying high currents, especially if pulsed (tracks of the power loops), should be as short and wide as possible.

Optimize track routing:

- as levels of pickup from static discharges are likely to be greater closer to the extremities of the board, it is wise to keep any sensitive lines away from these areas.
- Input and output lines will often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable.
- Since vias are considered inductive elements, they should be kept to a minimum in signal paths and avoided in power paths.

Improve thermal dissipation:

- An adequate copper area must be provided under the DRAIN pins to dissipate heat
- It is not recommended to place large copper areas on the GND.

Finally, in order to improve immunity against fast transient and capacitive noise injection, since pin number 4 is mechanically connected to the controller die pad of the frame, it is highly recommended to connect it to GND.



## Revision history

**Table 5. Document revision history**

Date	Version	Changes
20-Sep-2019	1	Initial release.

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