Application note

L99LD20 and L99LD21 application design guidelines

Introduction

The L99LD20 and L99LD21 are flexible LED driver ICs targeting automotive frontlighting applications.

The L99LD20 integrates two buck converters based on a constant-VLED*toff architecture that control two independent high-power LED strings. In addition to the buck converters, the L99LD21 integrates a boost controller that generates a programmable output voltage up to 60 V that supplies the inputs of the buck converters integrated in the L99LD21 or in external ICs such as the L99LD20.

A variety of spreadsheets and tools is available from ST in order for users to calculate and select external components. Nevertheless, it is important to have a general understanding of the underlying factors that determine the selection of the external components.

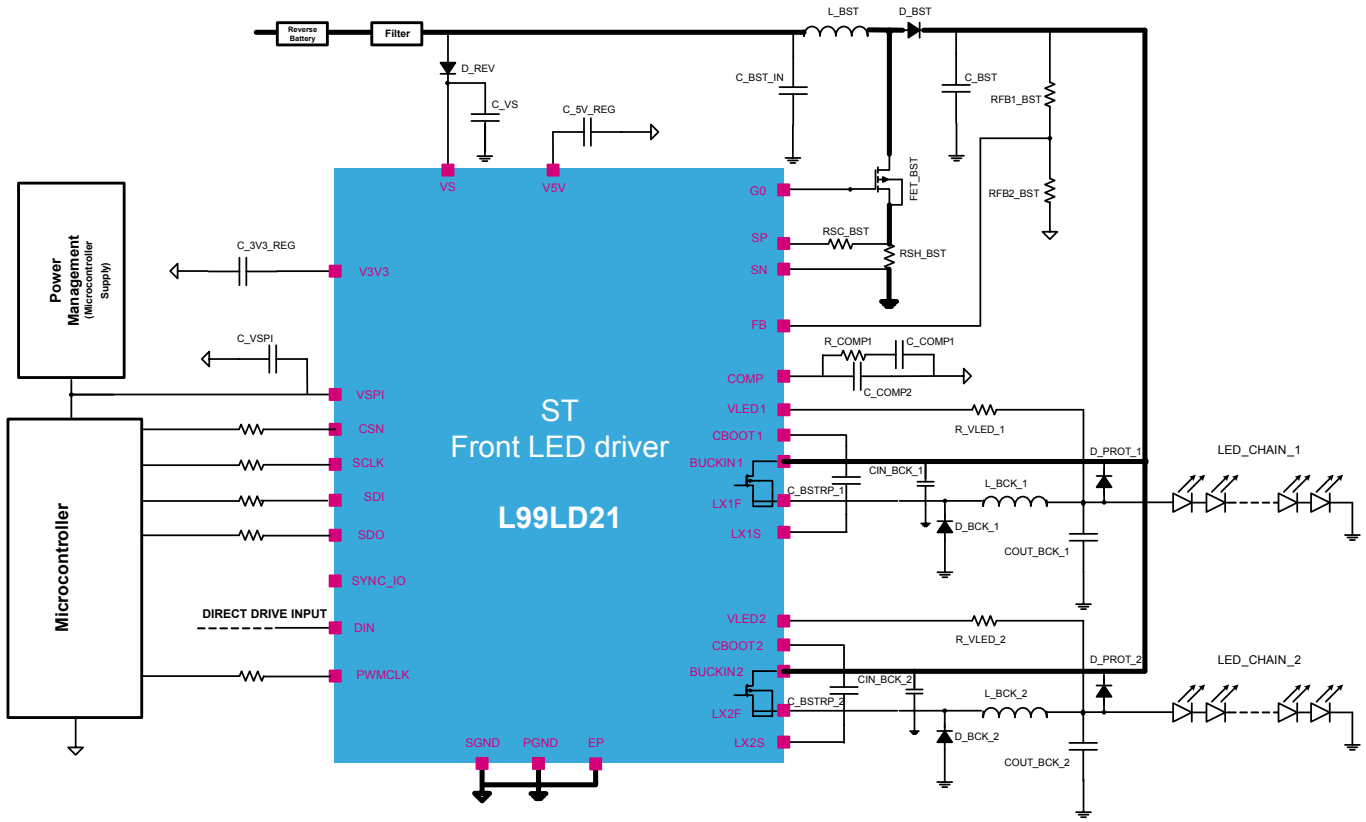
The goal of this application note is to provide some guidelines in the selection of the external components needed for proper operation of the buck converters and the boost controller.

1 The boost controller

With reference to Figure 1, the boost controller implemented in the L99LD21 steps up the input voltage (applied to the VS pin) to generate its output voltage, V_{BOOST}. The user can program this voltage by means of two external resistors and by selecting the desired value for the internal reference voltage V_{FB_REF} via SPI (bits 10 and 11 in Control Register 3), according to the following formula:

$$V_{BOOST} = V_{FB\_REF} \cdot \left(1 + \frac{R_{FB1\_BST}}{R_{FB2\_BST}}\right)$$

Figure 1. L99LD21 application diagram



Note: In the remainder of the section dedicated to the boost controller, the voltage at the VS pin will be indicated as V_{IN} and V_{BOOST} will be indicated as V_{OUT}.

The following paragraphs describe the steps to follow for a proper design of the boost controller.

1.1 Switching frequency

The boost controller operates at a fixed switching frequency f_{SW} that can range between 150 kHz and 450 kHz. The user can select the switching frequency via SPI by means of bits 7, 8 and 9 in Control Register 3. Please refer to the L99LD21 datasheet for the actual values.

In general, higher switching frequencies allow the use of smaller passive components (along with lower costs and less PCB space) and a reduction of current and voltage ripples (and thus lower electromagnetic emissions). On the negative side, higher switching frequencies generate higher power losses and thus a reduction of the overall power efficiency. Therefore, the selection of the switching frequency is a trade-off between conflicting requirements. Moreover, its selection is often dictated by other considerations, such as the avoidance of specific bands of the frequency spectrum.

1.2 Duty cycle

The duty cycle D is the percentage of the switching period during which the converter's MOSFET is commanded on. Ideally, the duty cycle for a boost converter operating in Continuous Conduction Mode (CCM) is equal to

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

If the voltage drop $V_{RDS(ON)}$ across the MOSFET and the diode forward voltage V_F are also taken into account, we have

$$D = \frac{V_{OUT} - V_{IN} + V_F}{V_{OUT} + V_F - V_{RDS(ON)}}$$

The difference between the two formulas is usually very small. $V_{RDS(ON)}$ and V_F will be neglected in the remainder of this document.

The duty cycle of the boost controller has a lower and an upper limit. The lower limit is determined by the minimum ON time (referred to as t_{BOOST_MIN} in the datasheet) and the switching frequency f_{SW} and is equal to

$$D_{BOOST\_MIN} = t_{BOOST\_MIN} \cdot f_{SW}$$

whereas the upper limit is specified in the datasheet as D_{BOOST_MAX} and is equal to 90 %.

Therefore, it must be ensured that the controller operates within these limits (with sufficient margin) over the operating conditions of the application.

1.3 Inductor

Once the switching frequency has been determined, the next step is to select a suitable inductor.

For a boost converter under steady-state conditions, the average inductor current is equal to the average input current. For an ideal lossless converter, this means

$$I_{L,avg} = I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN}}$$

In CCM, the expression above can also be written as

$$I_{L,avg} = I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN}} = \frac{I_{OUT}}{1 - D}$$

In a real converter, power losses cannot be avoided. If we consider the power efficiency of the converter, defined as

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}}$$

then we have

$$I_{L,avg} = I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta}$$

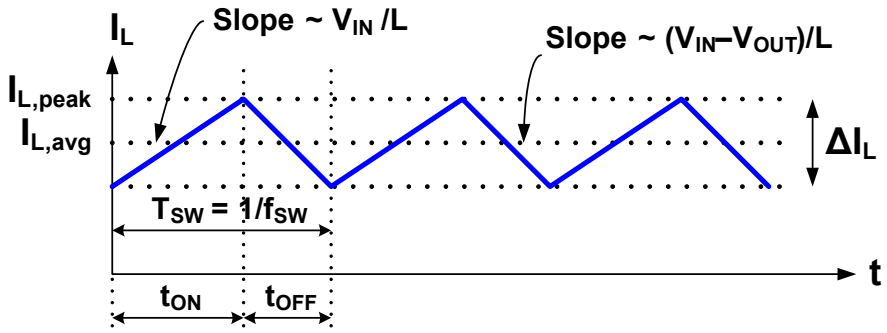
which can be written for CCM operation as

$$I_{L,avg} = I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} = \frac{I_{OUT}}{(1 - D) \cdot \eta}$$

The expression above shows that the inductor current can be significantly higher than the output current and the inductor must be sized accordingly. Moreover, it shows that the highest input current occurs at the minimum operating input voltage $V_{IN,min}$, i.e. at the maximum duty cycle. Although the power efficiency is not known beforehand, an estimate (e.g. 80%-90%, depending on the operating point) can be used for the calculations:

$$I_{L,avg,max} = I_{IN,max} = \frac{V_{OUT} \cdot I_{OUT,max}}{V_{IN,min} \cdot \eta_{estimated}} = \frac{I_{OUT,max}}{(1 - D_{max}) \cdot \eta_{estimated}}$$

Figure 2. **Boost converter inductor current**



As shown in Figure 2, the inductor current varies around $I_{L,avg}$ and the difference between the maximum and minimum value is the peak-to-peak inductor current ripple ΔI_L, which is given by the following formula:

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot f_{SW} \cdot L}$$

It should be noted that the maximum peak-to-peak current ripple $\Delta I_{L,max}$ occurs when $V_{IN} = V_{OUT}/2$ (i.e. at D = 50 %). If $V_{IN} = V_{OUT}/2$ does not fall within the operating range of the converter, $\Delta I_{L,max}$ occurs at the operating input voltage that is closest to this condition. Let's call this voltage V_{IN,max_ripple} .

In order to select the inductance value, an acceptable inductor current ripple must be defined at the application level. A larger inductance results in smaller values of ΔI_L, lower output voltage ripple, higher power efficiency, lower electromagnetic emissions, but it has the disadvantage of slower transient response and larger inductor size. Typically, a good trade-off between these conflicting requirements is to choose $\Delta I_{L,max}$ to be between 20 % and 40 % of the maximum input current. In other words,

$$\frac{\Delta I_{L,max}}{I_{IN,max}} = 0.2 \; to \; 0.4$$

Once $\Delta I_{L,max}$ has been defined, the minimum inductance can be calculated as follows:

$$L = \frac{V_{IN,\max\_ripple} \cdot \left(V_{OUT} - V_{IN,\max\_ripple}\right)}{V_{OUT} \cdot f_{SW} \cdot \Delta I_{L,max}}$$

The maximum peak inductor current under steady-state conditions is therefore

$$I_{L,peak,max} = I_{IN,max} + \frac{\Delta I_{L,VIN\_min}}{2}$$

where Δ_{IL,VIN_min} is the peak-to-peak current ripple at the minimum operating voltage.

Depending on the operating conditions, the converter can operate in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). In CCM, the inductor current never reaches zero, whereas in DCM, the inductor gets fully discharged and its current is zero during a portion of the switching cycle. The minimum output current that keeps the converter in CCM is

$$I_{OUT,min} = \frac{{V_{IN,crit}}^2 \cdot \left(V_{OUT} - V_{IN,crit}\right)}{2 \cdot {V_{OUT}}^2 \cdot f_{SW} \cdot L} = \frac{V_{OUT} \cdot D_{crit} \cdot (1 - D_{crit})^2}{2 \cdot f_{SW} \cdot L}$$

The critical input voltage to calculate $I_{OUT,min}$ is equal to $V_{IN,crit} = (2/3)*V_{OUT}$ (i.e. $D_{crit}=1/3$). If $V_{IN} = (2/3)*V_{OUT}$ does not fall within the operating range of the converter, $V_{IN,crit}$ is the operating input voltage that is closest to this condition.

In general, it is advisable to have the converter operating in CCM in order to avoid ringing on the switch node (i.e. the intersection between inductor, MOSFET and diode) and slow load transient response during the transition between DCM and CCM. In the remainder of this document, operation in CCM will be considered.

With regard to the inductor current ratings, the inductor RMS current is given by

$$I_{L,rms} = \sqrt{{I_{IN,max}}^2 + \frac{{\Delta I_L}^2}{12}} \cong I_{IN,max}$$

Design hints:

- after selecting $\Delta I_{L,max}$ and calculating L, calculate $I_{OUT,min}$, $I_{L,peak,max}$ and $I_{L,rms}$. If $I_{OUT,min}$ is greater than the minimum load in the application and DCM is to be avoided, increase L and recalculate the other quantities;
- the specified saturation current of the inductor (usually indicated as I_{SAT}) should be higher than the maximum current flowing in the converter during current limitation (I_{LIMIT}, which is determined by the R_{SH_BST} resistor connected between the SP pin and the SN pin, see Section 1.4 Current sense resistor);
- the I_{RMS} current rating of the inductor is usually specified in terms of temperature rise due to self-heating. Make sure the inductor does not operate at a temperature higher than its rated range. A good approach is to select an inductor with I_{RMS} greater than $I_{IN,max}$;
- the DCR (DC Resistance) should be as low as possible for better power efficiency;
- the SRF (Self Resonant Frequency) of the inductor must be well above the switching frequency of the converter

1.4 Current sense resistor

As shown in Figure 1, the R_{SH_BST} current sense resistor is connected between the SP pin and SN pin. This resistor has a twofold function:

1. sensing the inductor current to generate a voltage ramp that is used by the control loop of the boost converter;
2. sensing the inductor current for the overcurrent protection of the boost converter.

The overcurrent protection function of the L99LD21 compares the voltage between the SP pin and the SN pin with the internal V_{BOOST_LIM} threshold (typ. 390 mV, as specified in the datasheet). The relationship between the current limitation value I_{LIMIT} that triggers the overcurrent protection and R_{SH_BST} is

$$I_{LIMIT} = \frac{V_{BOOST\_LIM} - \frac{I_{SLOPE} \cdot R_{SC\_BST} \cdot D}{f_{SW}}}{R_{SH\_BST}}$$

where D is the duty cycle in the application, I_{SLOPE} is the slope compensation current ramp injected by the L99LD21 into the SP pin and R_{SC_BST} is the external slope compensation resistor connected to the SP pin. See Section 1.9.2 Slope compensation for details about slope compensation.

As can be evinced from the formula above, the current limitation value is inversely proportional to the duty cycle or, in other words, directly proportional to the input voltage.

Once a current limitation value that is suitable for the application has been defined, R_{SH_BST} can be calculated by rearranging the formula above, which gives

$$R_{SH\_BST} = \frac{V_{BOOST\_LIM} - \frac{I_{SLOPE} \cdot R_{SC\_BST} \cdot D}{f_{SW}}}{I_{LIMIT}}$$

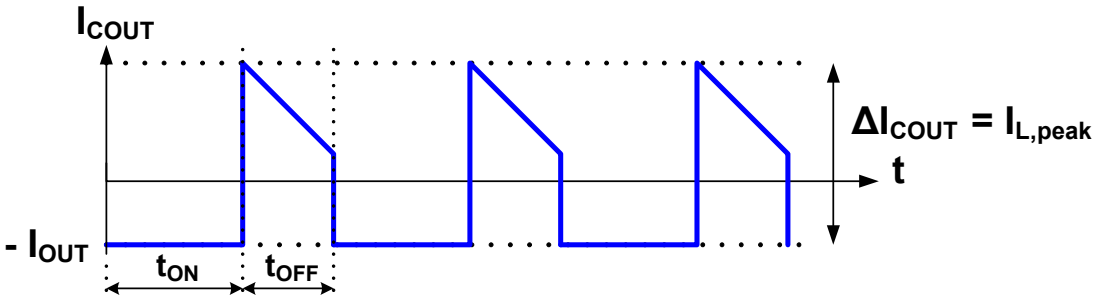
Design hints:

- once the maximum peak inductor current $I_{L,peak\ ,max}$ has been calculated as described in Section 1.3 Inductor, define I_{LIMIT} with sufficient margin (at least 30 % - 50 %) above $I_{L,peak,max}$;
- calculate R_{SH_BST} with the formula above by using the maximum duty cycle ($D = D_{max}$) of the application;
- once R_{SH_BST} has been calculated, calculate I_{LIMIT} at the lowest duty cycle ($D = D_{min}$) of the application and make sure that the inductor has a saturation current above this I_{LIMIT}.

1.5 Output capacitors

The output capacitors have the function of limiting the output voltage ripple to the level required by the application. Capacitance (C), equivalent series resistance (ESR) and equivalent series inductance (ESL) of the output capacitors contribute to the output voltage ripple.

Figure 3. **Boost converter output capacitor current**



Capacitance and ESR can affect the output voltage ripple ΔV_{OUT} in three different ways.

1. Under steady-state operation, the pulsating current flowing in the output capacitors generates a voltage ripple. For CCM, the minimum capacitance needed to reach the required ΔV_{OUT} is

$$C_{OUT} = \frac{I_{OUT,max} \cdot D_{max}}{f_{SW} \cdot \Delta V_{OUT}}$$

whereas the maximum ESR is

$$ESR_{OUT} = \frac{\Delta V_{OUT}}{I_{L,peak,max}}$$

2. In case of output load transients, the converter needs some time to respond to the new load condition due to its finite bandwidth. Before the converter can respond, the increased load demand is supplied by the output capacitors. If f_C is the crossover frequency of the converter's loop gain (see Section 1.9.1 Control loop stability for more details about the crossover frequency) and ΔI_{OUT} is the maximum load step, the minimum capacitance can be estimated as

$$C_{OUT} = \frac{\Delta I_{OUT}}{2\pi \cdot f_C \cdot \Delta V_{OUT}}$$

whereas the maximum ESR is

$$ESR_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

3. In case the full output load is removed from the output, the minimum output capacitance can be estimated as

$$C_{OUT} = \frac{L \cdot {I_{L,peak,max}}^2}{(V_{OUT} + \Delta V_{OUT})^2 - {V_{OUT}}^2}$$

whereas the maximum ESR is

$$ESR_{OUT} = \frac{\Delta V_{OUT}}{I_{L,peak,max}}$$

Based on the three cases above, the most stringent values of capacitance and ESR must be selected.

ESL must be minimized by choosing low-ESL capacitors, designing short PCB traces and placing several output capacitors in parallel.

As can be evinced from Figure 3, the output capacitors of the boost converter are subject to high RMS current. Therefore, the RMS current handling capability of the output capacitors is of primary importance. In CCM, the RMS current in the output capacitors is

$$I_{COUT,rms} = \sqrt{{I_{OUT}}^2 \cdot \frac{D}{1-D} + \frac{{\Delta I_L}^2}{12} \cdot (1-D)} \cong I_{OUT} \cdot \sqrt{\frac{D}{1-D}}$$

The highest value of $I_{COUT,rms}$ occurs when the maximum output current $I_{OUT,max}$ is delivered to the output at the maximum duty cycle D_{max}:

$$I_{COUT,rms,max} \cong I_{OUT,max} \cdot \sqrt{\frac{D_{max}}{1-D_{max}}}$$

Due to the ESR, this RMS current causes power dissipation and a temperature increase of the capacitor, which can negatively impact the reliability and lifetime of the capacitor itself. Therefore, a capacitor with sufficient RMS current rating must be selected. The RMS current handling capability is often the limiting factor and the final ESR often results from this requirement.

Design hints:

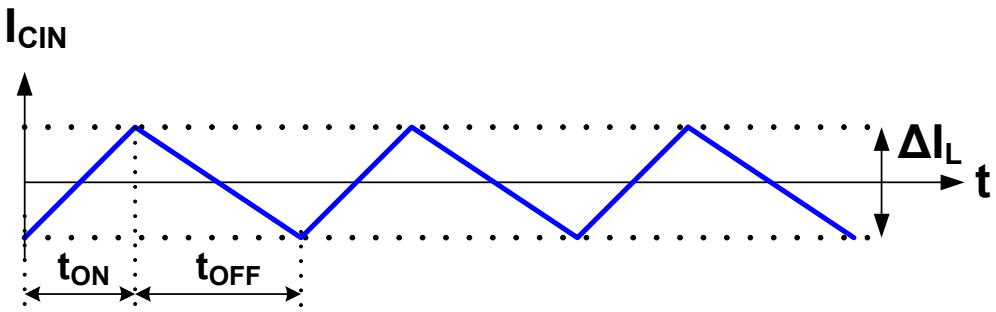
- after determining the requirements for C and ESR, suitable capacitors have to be selected also by taking into account the RMS current ratings;
- electrolytic capacitors have higher capacitance and DC voltage ratings. On the downside, they have higher ESR, which implies lower RMS current handling capabilities;
- ceramic capacitors feature low ESR, which is good for RMS current handling. On the downside, they have limited values of capacitance (especially for higher voltage ratings) and suffer from DC bias effects (i.e. loss of capacitance with applied voltage);
- in order to reach the required value of capacitance, ESR and RMS current handling, several capacitors of different types (electrolytic, ceramic) can be placed in parallel. Special attention should be given to the selection of ceramic capacitors, due to their specific temperature and voltage characteristics, in particular to DC bias effects. Choose ceramic capacitors with voltage ratings at least 1.5 times above the output voltage.

1.6 Input capacitors

The goal of the input capacitors is to limit the input voltage ripple to the desired level.

As shown in Figure 4, the RMS current in the input capacitors is usually low in CCM, since the input current is continuous.

Figure 4. Boost converter input capacitor current



The maximum RMS current flowing in the input capacitance is

$$I_{CIN,rms,max} = \frac{\Delta I_{L,max}}{\sqrt{12}}$$

In order to attain the required input voltage ripple ΔV_{IN}, the minimum capacitance is

$$C_{IN} = \frac{\Delta I_{L,max}}{8 \cdot f_{SW} \cdot \Delta V_{IN}}$$

whereas the maximum ESR is

$$ESR_{IN} = \frac{\Delta V_{IN}}{\Delta I_{L,max}}$$

Similarly to the output capacitors, the ESL must be minimized to prevent voltage spikes due to inductive effects.

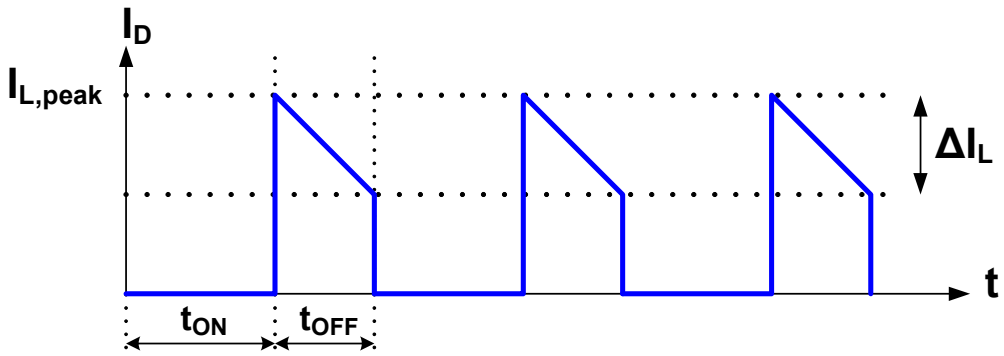
Design hints:

- in terms of RMS current handling, the requirements on the input capacitors are less stringent than those on the output capacitors because the input current of a boost converter in CCM is continuous;
- the considerations listed for the output capacitors also apply to the input capacitors;
- in practice, higher capacitance may be required to prevent potential oscillations caused by inductance present on the PCB.

1.7 Freewheeling diode

The freewheeling diode is placed in series with the output, therefore its average current is the output current I_{OUT}, whereas its peak current is the inductor peak current $I_{L,peak}$.

Figure 5. Boost converter diode current



The maximum power dissipated in the diode is

$$P_{DIODE,max} \cong V_F \cdot I_{OUT,max}$$

The maximum reverse voltage during normal operation is equal to the output voltage V_{OUT}. However, the diode can see a reverse voltage higher than V_{OUT} under light load conditions, as described in the L99LD21 datasheet. In this case, the maximum reverse voltage seen by the diode is the overvoltage protection threshold, which is equal to

$$V_{OUT,OVTH} = V_{FB\_OV\_ON} \cdot \left(1 + \frac{R_{FB1\_BST}}{R_{FB2\_BST}}\right)$$

where $V_{FB\_OV\_ON}$ is typically 3 % to 5 % higher than V_{FB_REF} (output reference voltage), as specified in the datasheet.

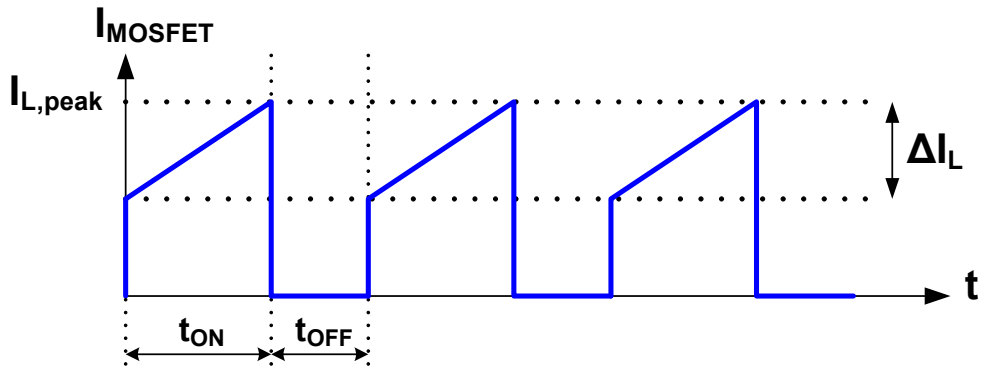
Design hints:

- the average forward current rating of the diode must be higher than the maximum output current;
- the peak repetitive forward current rating of the diode must be higher than the maximum inductor peak current;
- the diode must be able to handle the maximum power dissipated (package and thermal resistance);
- the minimum reverse voltage of the diode must be higher than the output voltage. Adequate margin (at least 20 %) should be taken to account for overvoltages and spikes;
- low forward voltage is important for power efficiency. Schottky diodes are recommended;
- fast switching is important to minimize reverse recovery current and improve efficiency. Schottky diodes are recommended;
- high-temperature leakage current and low forward voltage are usually conflicting parameters for Schottky diodes. A trade-off is usually needed.

1.8 Power MOSFET

The peak current flowing through the MOSFET is the inductor peak current $I_{L,peak}$.

Figure 6. **Boost converter MOSFET current**



The maximum power dissipated in the MOSFET is

$$P_{MOSFET,max} \cong D_{max} \cdot \left(\frac{I_{OUT,max}}{1-D_{max}}\right)^2 \cdot R_{DS(ON),max} + \frac{1}{2} \cdot V_{OUT} \cdot \frac{I_{OUT,max}}{1-D_{max}} \cdot \left(t_{rise} + t_{fall}\right) \cdot f_{sw}$$

where t_{rise} and t_{fall} are respectively the turn-on and turn-off switching time of the MOSFET.

With regard to the drain-source voltage seen by the MOSFET during operation, the same considerations made for the reverse voltage of the diode apply here.

Design hints:

- $R_{DS(ON)}$ and package thermal resistance are usually the limiting factors and are key parameters to handle the required current and reduce power losses;
- the breakdown voltage of the MOSFET must be higher than the output voltage. Adequate margin (at least 20 %) should be taken to account for overvoltages and spikes;
- the n-channel MOSFET must be of a logic-level type in order to be driven properly by the 5 V MOSFET gate driver of the L99LD21;
- the gate charge of the MOSFET should be low in order to reduce switching power losses in the MOSFET and gate charge power losses in the gate driver of the L99LD21.

1.9 Stability

The boost converter of the L99LD21 is based on a peak CMC (Current Mode Control) architecture. When considering CCM operation, this architecture has the advantage of replacing the LC 2nd-order pole usually present in the control-to-output transfer function of a VMC (Voltage Mode Control) architecture with a 1st-order pole. In principle, this simplifies the design of a stable control loop with sufficient phase margin at the crossover frequency f_C (i.e. the frequency at which the loop gain transfer function is equal to 0 dB). However, boost converters have a so-called right-half-plane zero (RHPZ) in the control-to-output transfer function that reduces phase margin and thus makes the control loop more prone to instability.

In addition, when operating in CCM at duty cycles above 50 %, peak CMC converters can be subject to an unstable behavior known as subharmonic oscillation, which causes a significant increase of output ripple and noise. The so-called slope compensation technique aims at preventing the subharmonic oscillation instability.

Control loop stability and slope compensation are analyzed in more detail in the next two sections.

1.9.1 Control loop stability

In order to design a stable control loop, the loop gain transfer function must exhibit sufficient phase margin at the crossover frequency f_C, i.e. at the frequency where the loop gain is equal to 0 dB. The loop gain is the product of the control-to-output transfer function with the error amplifier transfer function.

The simplified control-to-output transfer function of the peak CMC boost converter in CCM is

$$\frac{v_{OUT}}{v_C}(s) \cong \frac{R_{OUT} \cdot (1-D)}{2 \cdot G_{LA} \cdot R_{SH\_BST}} \cdot \frac{\left(1+\frac{s}{\omega_{Z1}}\right) \cdot \left(1-\frac{s}{\omega_{Z2}}\right)}{\left(1+\frac{s}{\omega_P}\right) \cdot \left(1+\frac{s}{Q \cdot \omega_n}+\frac{s^2}{{\omega_n}^2}\right)}$$

$R_{OUT} = \frac{V_{OUT}}{I_{OUT}}\ (output\ load)$

$G_{LA} = 4.25\ (from\ datasheet, linear\ amplifier\ gain\ for\ current\ \ sensing\ across\ R_{SH\_BST})$

$\omega_{Z1} = \frac{1}{R_{ESR} \cdot C_{OUT}}\ (ESR\ zero\ of\ output\ capacitors)$

$\omega_{Z2} = \frac{R_{OUT} \cdot (1-D)^2}{L}\ (RHPZ)$

$\omega_P = \frac{2}{R_{OUT} \cdot C_{OUT}}\ (load\ pole)$

$\omega_n = \pi \cdot f_{SW}\ (complex\ poles\ at\ f_{SW}/2\ due\ to\ subharmonic\ \ oscillation)$

$Q = \frac{1}{\pi \cdot \left[\left(1+\frac{S_e}{S_{on}}\right) \cdot (1-D) - 0.5\right]}\ (quality\ factor\ of\ complex\ poles)$

The pair of complex poles is located at half of the switching frequency and its quality factor is reduced by increasing the slope compensation ramp S_e, which is analyzed in the next paragraph.

The critical element in the transfer function is the RHPZ, as it reduces the phase margin at the crossover frequency, just like a pole does. The results is that the phase margin at the crossover frequency f_C is not sufficient for stability.

Therefore, a suitable compensation network must be added to the feedback loop at the COMP pin in order for the overall loop gain to have sufficient bandwidth and phase margin. The COMP pin is the output of the internal operational transconductance amplifier (OTA). A Type II compensation can be sufficient to stabilize the loop. The overall transfer function of the error amplifier is

$$\frac{v_C}{v_{OUT}}(s) = -\frac{R_{FB2\_BST}}{R_{FB1\_BST}+R_{FB2\_BST}} \cdot G_M \cdot \frac{1+s \cdot R_{COMP1} \cdot C_{COMP1}}{s \cdot (C_{COMP1}+C_{COMP2}) \cdot \left(1+s \cdot R_{COMP1} \cdot \frac{C_{COMP1} \cdot C_{COMP2}}{C_{COMP1}+C_{COMP2}}\right)}$$

where G_M is the transconductance of the OTA integrated in the L99LD21 (570 µS, as specified in the datasheet). If $C_{COMP2} << C_{COMP1}$, then we have

$$\frac{v_C}{v_{OUT}}(s) = -\frac{R_{FB2\_BST}}{R_{FB1\_BST}+R_{FB2\_BST}} \cdot G_M \cdot \frac{1+s \cdot R_{COMP1} \cdot C_{COMP1}}{s \cdot C_{COMP1} \cdot (1+s \cdot R_{COMP1} \cdot C_{COMP2})}$$

The overall loop gain transfer function is the product of the control-to-output transfer function with the error amplifier transfer function:

$$G_{loop}(s) = \frac{v_{OUT}}{v_C}(s) \cdot \frac{v_C}{v_{OUT}}(s)$$

Design hints:

- select the crossover frequency f_C to be at 1/3 of the RHPZ or lower;
- the zero of the error amplifier transfer function generates a phase boost to improve the phase margin, therefore f_C must lie between the zero and the pole of the error amplifier transfer function;
- increasing the distance between the zero and the pole of the error amplifier transfer function will increase the phase margin (more stability), but decrease the DC gain of the overall loop gain (less DC accuracy of the output voltage). Therefore, a trade-off is necessary;
- aim at a phase margin of at least 60°;
- make sure the loop is stable for the entire V_{IN} and I_{OUT} range.

1.9.2 Slope compensation

Even when the loop gain has good phase margin at the crossover frequency, the boost converter can exhibit subharmonic oscillation at duty cycles above 50 %. Slope compensation is the technique used to prevent this form of instability.

Considering the application diagram in Figure 1, the L99LD21 injects a current ramp I_{SLOPE} (20 A/s, as specified in the datasheet) to the SP pin as a countermeasure against subharmonic oscillation. This current flows through resistors R_{SC_BST} and R_{SH_BST} and adds to the inductor current sensed across R_{SH_BST}. If we define S_e as the slope compensation ramp injected and sensed by the L99LD21, S_{on} as the rising slope of the inductor current sensed across R_{SH_BST} and S_{off} as the falling slope of the inductor current sensed across R_{SH_BST}, it is known from the theory that the slope compensation ramp S_e must satisfy the following requirement:

$$S_e > \frac{S_{off}}{2}$$

If we indicate the amount of slope compensation applied with α, we have

$$S_e = \alpha \cdot S_{off}$$

To select the slope compensation resistor R_{SC_BST}, the following formula can be used:

$$R_{SC\_BST} \geq \frac{\alpha \cdot (V_{OUT} - V_{IN,min}) \cdot R_{SH\_BST}}{L \cdot I_{SLOPE}}$$

In order to determine α, let's consider the quality factor of the double complex poles from the previous paragraph:

$$Q = \frac{1}{\pi \cdot \left[\left(1 + \frac{S_e}{S_{on}}\right) \cdot (1 - D) - 0.5\right]}$$

If we substitute S_e and S_{on} in the formula above, we get

$$Q = \frac{1}{\pi \cdot [0.5 - D \cdot (1 - \alpha)]}$$

If too low a value of α is chosen, oscillations can occur due to a high quality factor. Conversely, if too high a value of α is chosen, the dependency of the overcurrent protection limit from R_{SC_BST} becomes stronger (see Section 1.4 Current sense resistor). In order to have good subharmonic oscillations damping, Q must be less than 1 at the maximum duty cycle D_{max}. This means

$$\alpha \geq 1 - \frac{0.5 - \frac{1}{\pi}}{D_{max}}$$

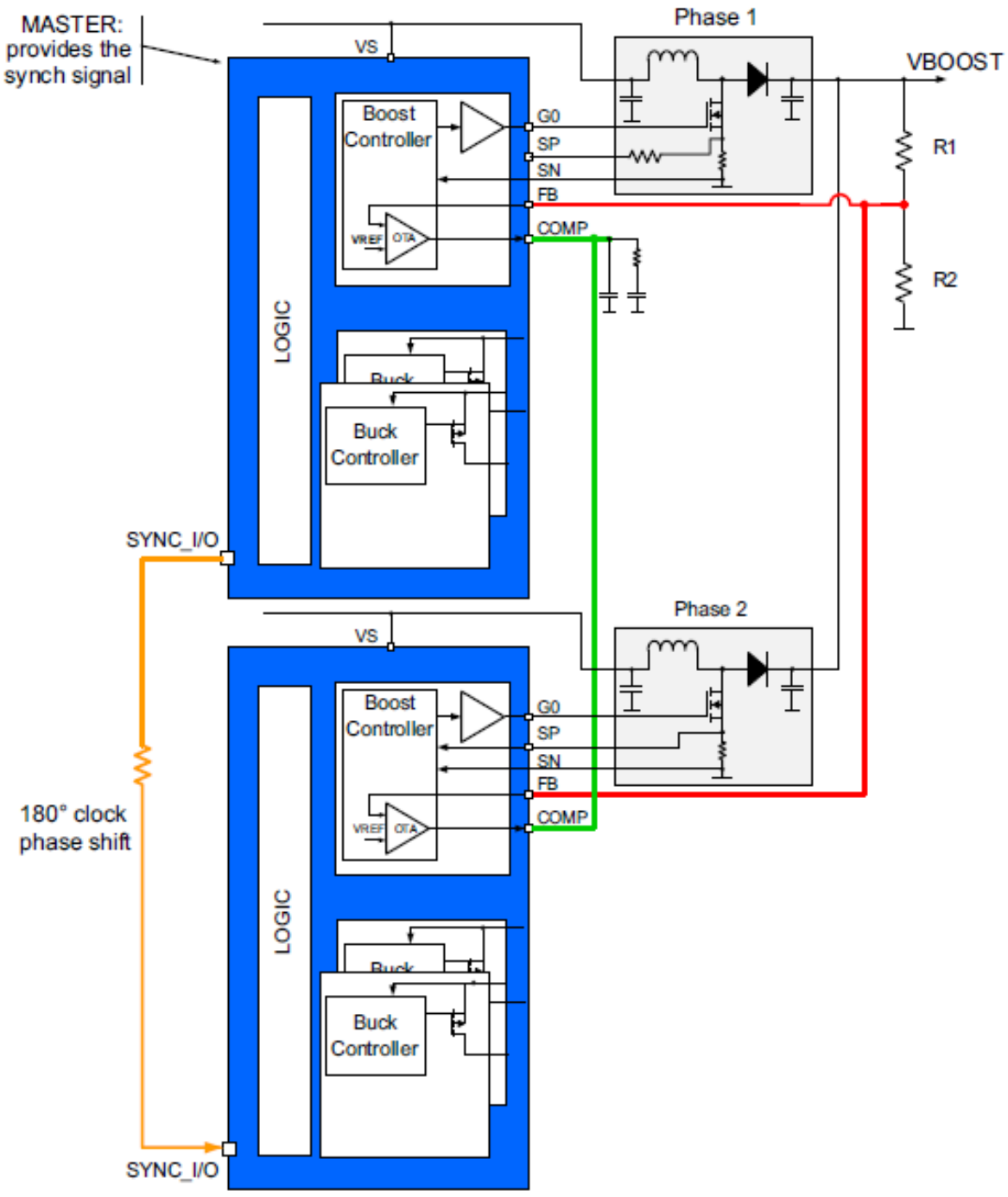
Design hints:

- calculate the minimum α to dampen subharmonic oscillations;
- substitute the calculated value of α into the expression for calculating R_{SC_BST} .

1.10 Interleaving

For high-power applications, it is possible to combine the boost controllers of two L99LD21 units for dual-phase interleaved operation as shown in Figure 7. The FB, COMP and SYNC_I/O pins of the two units must be connected together. One device has to be configured as master and the other as slave. By doing this, the master device provides a 180°-shifted clock to the slave device on the SYNC_I/O pin.

Figure 7. **Pin connections in dual-phase boost controller**



In principle, it is possible to connect N boost controllers in parallel for interleaved operation if all of them are configured as slaves and an external microcontroller provides clocking to the N controllers with proper time shift (360°/N) on the SYNC_I/O pins.

Interleaved operation offers several advantages such as higher efficiency and lower input and output ripple. The following paragraphs explain how to select external components for interleaved operation from a power stage and a stability standpoint for the most generic case of N interleaved boost converters.

1.10.1 Power stage

Inductors, MOSFETs, diodes and current sense resistors must be identical in all of the N boost controllers. Let's indicate the output current of one of the N converters as $I_{OUT,1\_PHASE}$ and the total output current as I_{OUT,N_PHASES}. Then it is

$$I_{OUT,1\_PHASE} = \frac{I_{OUT,N\_PHASES}}{N}$$

Since each boost controller has to conduct a fraction equal to 1/N of the total output current, the above mentioned components must be sized following the rules described in the previous paragraphs for a single-phase converter and considering 1/N of the total output current.

However, the selection of input and output capacitors is different from a single-phase converter.

Input capacitors

The RMS current flowing in the input capacitance is

$$I_{CIN,rms} = \frac{\Delta I_{IN,N\_PHASES}}{\sqrt{12}}$$

where $\Delta I_{IN,N\_PHASES}$ is the peak-to-peak input current ripple of the N-phase boost converter and is equal to

$$\Delta I_{IN,N\_PHASES} = \frac{V_{OUT} \cdot N \cdot \left(\frac{M}{N} - D\right) \cdot \left(D - \frac{M-1}{N}\right)}{L \cdot f_{sw}}$$

with D representing the duty cycle of a single phase. Depending on the duty cycle D, M can vary between 1 and N and represents the number of phases whose MOSFETs are being commanded on at the same time. For example, considering N=3, we would have

$$if\ 0 < D \le \frac{1}{3}, then\ M = 1\ and\ \Delta_{IN,N\_PHASES} = \frac{V_{OUT} \cdot 3 \cdot \left(\frac{1}{3} - D\right) \cdot D}{L \cdot f_{SW}}$$

$$if\ \frac{1}{3} \le D \le \frac{2}{3}, then\ M = 2\ and\ \Delta_{IN,N\_PHASES} = \frac{V_{OUT} \cdot 3 \cdot \left(\frac{2}{3} - D\right) \cdot \left(D - \frac{1}{3}\right)}{L \cdot f_{SW}}$$

$$if\ \frac{2}{3} \le D < 1, then\ M = 3\ and\ \Delta_{IN,N\_PHASES} = \frac{V_{OUT} \cdot 3 \cdot (1 - D) \cdot \left(D - \frac{2}{3}\right)}{L \cdot f_{SW}}$$

$\Delta I_{IN,N\_PHASES}$ is smaller than $\Delta I_{IN,1\_PHASE}$ thanks to the smoothening effect of the N phases operating in parallel. In order to attain the required input voltage ripple ΔV_{IN}, the minimum capacitance is

$$C_{IN} = \frac{\Delta I_{IN,N\_PHASES}}{8 \cdot f_{SW} \cdot \Delta V_{IN}}$$

whereas the maximum ESR is

$$ESR_{IN} = \frac{\Delta V_{IN}}{\Delta I_{IN,N\_PHASES}}$$

Output capacitors

As described in Section 1.5 Output capacitors, the output capacitance and ESR can be determined by considering three different scenarios.

1. Under steady-state conditions, the minimum capacitance is given by

$$C_{OUT} = \frac{I_{OUT,N\_PHASES} \cdot \left(\frac{M}{N} - D\right) \cdot \left(D - \frac{M-1}{N}\right)}{(1 - D) \cdot f_{SW} \cdot \Delta V_{OUT}}$$

The maximum ESR is

$$ESR_{OUT} = \frac{\Delta V_{OUT}}{I_{L\_eq,peak}}$$

where $I_{L\_eq,peak}$ is

$$I_{L\_eq,peak} = \frac{I_{OUT,N\_PHASES}}{(1 - D_{max}) \cdot \eta} + \frac{\Delta I_{IN,N\_PHASES,VIN\_min}}{2}$$

with η being the power efficiency of a single phase and $\Delta I_{IN,N\_PHASES,VIN\_min}$ the peak-to-peak input current ripple at the minimum input voltage.

2. In case of load transients, the minimum capacitance can be estimated as

$$C_{OUT} = \frac{\Delta I_{OUT}}{2\pi \cdot f_C \cdot \Delta V_{OUT}}$$

whereas the maximum ESR is

$$ESR_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

3. In case the full output load is removed from the output, the minimum output capacitance can be estimated as

$$C_{OUT} = \frac{L \cdot {I_{L\_eq,peak}}^2}{{(V_{OUT} + \Delta V_{OUT})}^2 - {V_{OUT}}^2}$$

whereas the maximum ESR is

$$ESR_{OUT} = \frac{\Delta V_{OUT}}{I_{L\_eq,peak}}$$

Based on the three cases above, the most stringent values of capacitance and ESR must be selected.
Finally, the RMS current is given by

$$I_{COUT,rms} \cong \frac{I_{OUT,N\_PHASES}}{(1-D)} \cdot \sqrt{\left(\frac{M}{N} - D\right) \cdot \left(D - \frac{M-1}{N}\right)}$$

which is lower than the RMS current of a single-phase converter thanks to the smoothening effect of the N phases operating in parallel.

1.10.2 Control loop

The compensation of the loop gain in case of N interleaved converters is conceptually similar to the case of a single-phase converter. However, a few adjustments have to be made.
The control-to-output transfer function becomes

$$\frac{v_{OUT}}{v_C}(s) \cong \frac{\boldsymbol{N} \cdot R_{OUT,N\_PHASES} \cdot (1-D)}{2 \cdot G_{LA} \cdot R_{SH\_BST}} \cdot \frac{\left(1 + \frac{s}{\omega_{Z1}}\right) \cdot \left(1 - \frac{s}{\omega_{Z2}}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{Q \cdot \omega_n} + \frac{s^2}{{\omega_n}^2}\right)}$$

$$R_{OUT,N\_PHASES} = \frac{V_{OUT}}{I_{OUT,N\_PHASES}} \ (output\ load)$$

$$G_{LA} = 4.25 \ (from\ datasheet, linear\ amplifier\ gain\ for\ current\ sensing\ across\ R_{SH\_BST})$$

$$\omega_{Z1} = \frac{1}{R_{ESR} \cdot C_{OUT}} \ (ESR\ zero\ of\ output\ capacitors)$$

$$\omega_{Z2} = \frac{\boldsymbol{N} \cdot R_{OUT,N\_PHASES} \cdot (1-D)^2}{L} \ (RHPZ)$$

$$\omega_P = \frac{2}{R_{OUT,N\_PHASES} \cdot C_{OUT}} \ (load\ pole)$$

$$\omega_n = \pi \cdot f_{SW} \ (complex\ poles\ at\ f_{SW}/2\ due\ to\ subharmonic\ oscillation)$$

$$Q = \frac{1}{\pi \cdot \left[\left(1 + \frac{S_e}{S_{on}}\right) \cdot (1-D) - 0.5\right]} \ (quality\ factor\ of\ complex\ poles)$$

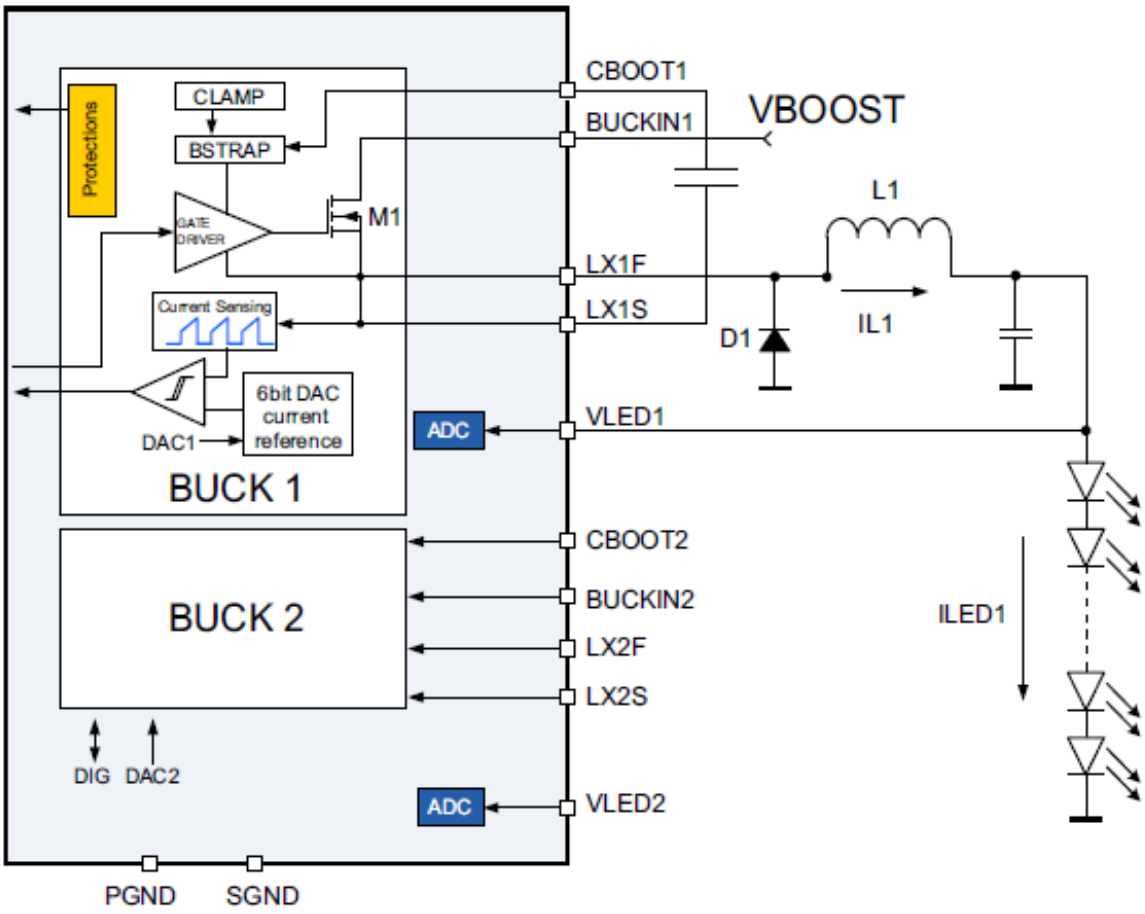
The error amplifier transfer function becomes

$$\frac{v_C}{v_{OUT}}(s) = -\frac{R_{FB2\_BST}}{R_{FB1\_BST} + R_{FB2\_BST}} \cdot \boldsymbol{N} \cdot G_M \cdot \frac{1 + s \cdot R_{COMP1} \cdot C_{COMP1}}{s \cdot C_{COMP1} \cdot (1 + s \cdot R_{COMP1} \cdot C_{COMP2})}$$

2 The buck converters

The two buck converters integrated in the L99LD20 and L99LD21 are based on a peak current control scheme with constant VLED*toff. When the inductor current reaches the inductor peak current threshold programmed by the user by means of the IL1_PEAK and IL2_PEAK bits (6 bits each), the converter adjusts the off-time automatically based on the measured output voltage and on the VLED_TOFF1 and VLED_TOFF2 bits (4 bits each) programmed by the user.

Figure 8. Buck converter circuit



2.1 Switching frequency

Since the buck converter is based on a constant-VLED*toff architecture and not on a fixed-frequency PWM architecture, the switching frequency f_{SW} depends on the operating conditions.

The switching frequency is equal to

$$f_{SW} = \frac{V_{LED} \cdot \left(1 - \frac{V_{LED}}{V_{BUCKIN}}\right)}{VLED\_TOFF}$$

and depends on the input voltage (V_{BUCKIN}), on the LED string voltage (V_{LED}) and on the selected VLED_TOFF value. The maximum switching frequency occurs when $V_{LED} = V_{BUCKIN}/2$.

2.2 Duty cycle

The duty cycle D is the percentage of the switching period during which the converter's MOSFET is commanded on. Ideally, the duty cycle for the buck converter operating in Continuous Conduction Mode (CCM) is equal to

$$D = \frac{V_{LED}}{V_{BUCKIN}}$$

If the voltage drop $V_{RDS(ON)}$ across the integrated MOSFET and the diode forward voltage V_F are also taken into account, we have

$$D = \frac{V_{LED} + V_F}{V_{BUCKIN} + V_F - V_{RDS(ON)}}$$

As described in the datasheet, some constraints exist with regard to the duration of the on-time and the off-time. This translates into specific conditions that the selected VLED_TOFF value must satisfy in order for the buck converter to operate properly:

$$t_{ON\_MIN\_BUCK} < \frac{VLED\_TOFF}{V_{BUCKIN} - V_{LED}} < t_{ON\_MAX\_BUCK}$$

$$t_{OFF\_MIN\_BUCK} < \frac{VLED\_TOFF}{V_{LED}} < t_{OFF\_MAX\_BUCK}$$

2.3 Inductor

Since the inductor of a buck converter is connected directly in series with the output load, the average inductor current is equal to the average LED string current. Therefore

$$I_{L,avg} = I_{LED}$$

The inductor current varies around $I_{L,avg}$ and the peak-to-peak current ripple ΔI_L is

$$\Delta I_L = \frac{VLED\_TOFF \cdot \left(1 + \frac{V_F}{V_{LED}}\right)}{L}$$

If V_F << V_{LED}, then

$$\Delta I_L = \frac{VLED\_TOFF}{L}$$

By imposing ΔI_L to be a given percentage of the LED string current (e.g. 20 %-40 % of I_{LED}), the inductance can be calculated as

$$L = \frac{VLED\_TOFF}{\Delta I_L}$$

If the buck converter operates in CCM, the average LED string current is ideally

$$I_{LED} = I_{L\_PEAK} - \frac{\Delta I_L}{2}$$

This means that the LED string current can be set by adjusting the IL_PEAK and the VLED_TOFF parameters via SPI.

If non-idealities (such as current sense dependencies on the input voltage and comparator delay) are taken into account, the average LED current is given by:

1. for V_{BUCKIN} < 50 V

$$I_{LED} = \frac{I_{L\_PEAK}}{1.036 - 0.04\% \cdot V_{BUCKIN}} + \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK} - \frac{\Delta I_L}{2}$$

2. for V_{BUCKIN} ≥ 50 V

$$I_{LED} = \frac{I_{L\_PEAK}}{1.355 - 0.7\% \cdot V_{BUCKIN}} + \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK} - \frac{\Delta I_L}{2}$$

where $t_{LOOP\_DELAY\_BUCK}$ is the internal comparator delay (as reported in the datasheet).

The peak inductor current is:

1. for V_{BUCKIN} < 50 V

$$I_{L,peak} = \frac{I_{L\_PEAK}}{1.036 - 0.04\% \cdot V_{BUCKIN}} + \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK}$$

2. for $V_{BUCKIN} \geq 50$ V

$$I_{L,peak} = \frac{I_{L\_PEAK}}{1.355 - 0.7\% \cdot V_{BUCKIN}} + \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK}$$

In order for the buck converter to operate in CCM, the following condition must be met:

$$I_{LED} \geq \frac{\Delta I_L}{2}$$

With regard to the inductor current ratings, the inductor RMS current is given by

$$I_{L,rms} = \sqrt{{I_{LED}}^2 + \frac{{\Delta I_L}^2}{12}} \cong I_{LED}$$

Design hints:

- after selecting VLED_TOFF for a given switching frequency and checking for proper operation with the selected VLED_TOFF (no violation of t_{ON} and t_{OFF} times), select the inductance for a given inductor current ripple and finally select IL_PEAK to closely match the required target LED current;
- the specified saturation current of the inductor (usually indicated as I_{SAT}) should be higher than the peak inductor current;
- the I_{RMS} current rating of the inductor is usually specified in terms of temperature rise due to self-heating. Make sure the inductor does not operate at a temperature higher than its rated range. A good approach is to select an inductor with I_{RMS} greater than I_{LED};
- the DCR (DC Resistance) should be as low as possible for better power efficiency;
- the SRF (Self Resonant Frequency) of the inductor must be well above the switching frequency of the converter

2.4 Output capacitors

The output capacitor is placed in parallel to the LED string and helps reduce the LED current ripple, Δi_{LED}.

In order to calculate the requirements on the output capacitor, the LED dynamic resistance has to be determined first. The LED dynamic resistance, r_{LED}, is the inverse slope of the LED's V-I curve. If N is the number of LEDs in the string, the total dynamic resistance of the LED string is

$$r_{LED,string} = N \cdot r_{LED}$$

The minimum capacitance to meet the LED current ripple requirement is

$$C_{OUT} = \frac{\Delta I_L}{8 \cdot f_{SW} \cdot \Delta i_{LED} \cdot r_{LED,string}}$$

whereas the maximum ESR is

$$ESR_{OUT} = \frac{\Delta i_{LED} \cdot r_{LED,string}}{\Delta I_L}$$

The output capacitor has also the function of limiting the output voltage rise ΔV_{OUT} in case the full output load is removed from the output. The minimum output capacitance can be estimated as

$$C_{OUT} = \frac{L \cdot {I_{L,peak}}^2}{(V_{OUT} + \Delta V_{OUT})^2 - {V_{OUT}}^2}$$

whereas the maximum ESR is

$$ESR_{OUT} = \frac{\Delta V_{OUT}}{I_{L,peak}}$$

The most stringent values of C_{OUT} and ESR_{OUT} must be considered.

Finally, the RMS current in the output capacitor is given by

$$I_{COUT,rms} = \frac{\Delta I_L}{\sqrt{12}}$$

Design hints:

- the considerations about electrolytic and ceramic capacitors highlighted in the design hints for the boost output capacitors are also true in this case;
- a single ceramic capacitor should be sufficient in most cases.

2.5 Input capacitors

The input capacitors limit the input voltage ripple to the desired level. They supply current pulses approximately equal to I_{LED} during the MOSFET on-time, whereas they are recharged by the input supply during the MOSFET off-time.

In order to attain the required input voltage ripple ΔV_{IN}, the minimum capacitance is

$$C_{IN} = \frac{I_{LED} \cdot VLED\_TOFF}{(V_{BUCKIN} - V_{LED}) \cdot \Delta V_{IN}}$$

whereas the maximum ESR is

$$ESR_{IN} = \frac{\Delta V_{IN}}{I_{L,peak}}$$

The RMS current flowing in the input capacitance is

$$I_{CIN,rms} = \sqrt{{I_{LED}}^2 \cdot D \cdot (1-D) + \frac{{\Delta I_L}^2}{12} \cdot D} \cong I_{LED} \cdot \sqrt{D \cdot (1-D)}$$

and is maximum for D = 50 % (i.e. for $V_{LED} = V_{BUCKIN}/2$).

The ESL must be minimized to prevent voltage spikes due inductive effects.

Design hints:

- the considerations about electrolytic and ceramic capacitors highlighted in the design hints for the boost output capacitors are also true in this case;
- the input supply of the buck converter is usually the output of a boost converter, so the boost converter output capacitors will serve as input capacitors for the buck converter;
- an additional small ceramic capacitor placed close to the input supply pin is recommended for high-frequency decoupling

2.6 Freewheeling diode

The freewheeling diode conducts the inductor current when the integrated MOSFET is off. Therefore, the diode peak current is equal to the inductor peak current:

$$I_{DIODE,peak} = I_{L,peak}$$

The average diode current is given by

$$I_{DIODE,avg} = I_{LED} \cdot (1-D) = I_{LED} \cdot \left(1 - \frac{V_{LED}}{V_{BUCKIN}}\right)$$

The power dissipated in the diode is

$$P_{DIODE} \cong V_F \cdot I_{LED} \cdot \left(1 - \frac{V_{LED}}{V_{BUCKIN}}\right)$$

The maximum reverse voltage during normal operation is equal to the input voltage V_{BUCKIN}.

Design hints:

- the average forward current rating of the diode must be higher than the calculated average diode current;
- the peak repetitive forward current rating of the diode must be higher than the maximum inductor peak current;
- the diode must be able to handle the maximum power dissipated (package and thermal resistance);
- the minimum reverse voltage of the diode must be higher than the input voltage. Adequate margin (at least 20 %) should be taken to account for overvoltages and spikes;
- low forward voltage is important for power efficiency. Schottky diodes are recommended;
- fast switching is important to minimize reverse recovery current and improve efficiency. Schottky diodes are recommended.
- high-temperature leakage current and low forward voltage are usually conflicting parameters for Schottky diodes. A trade-off is usually needed.

3 Numerical example #1 - boost controller

Let's examine a numerical example for the boost controller based on the following application conditions:

- switching frequency: 400 kHz
- input voltage range: 8 V to 18 V
- V_{OUT}: 60 V
- I_{OUT}: 800 mA

FEEDBACK RESISTORS

The output feedback resistors can be calculated by using the following formula:

$$V_{BOOST} = V_{FB\_REF} \cdot \left(1 + \frac{R_{FB1\_BST}}{R_{FB2\_BST}}\right)$$

If V_{FB_REF} is selected to be 1.496 V (Control Register 3), then we can choose R_{FB1_BST} = 58kΩ and R_{FB2_BST} = 1.5 kΩ.

DUTY CYCLE

Given the application conditions, from Paragraph 2.2 we can calculate the minimum and maximum duty cycle as

$$D_{min} = \frac{V_{OUT} - V_{IN,max}}{V_{OUT}} = \frac{60V - 18V}{60V} = 70\%$$

$$D_{max} = \frac{V_{OUT} - V_{IN,min}}{V_{OUT}} = \frac{60V - 8V}{60V} = 87\%$$

Since $D_{min} > t_{BOOST\_MIN} \times f_{SW}$ and $D_{max} < D_{BOOST\_MAX}$, the boost converter can operate properly under the given operating conditions.

INDUCTOR

Assuming a converter efficiency of 90%, the maximum input current is equal to

$$I_{IN,max} = \frac{I_{OUT,max}}{(1 - D_{max}) \cdot \eta_{estimated}} = \frac{0.8A}{(1 - 0.87) \cdot 0.9} \cong 6.67A$$

The maximum inductor current ripple occurs when the input voltage is equal to 18 V (i.e. at D = 70 %). If we impose the maximum inductor current ripple to be 40 % of $I_{IN,max}$, we can then calculate the inductor as

$$L = \frac{V_{IN,\max\_ripple} \cdot \left(V_{OUT} - V_{IN,\max\_ripple}\right)}{V_{OUT} \cdot f_{SW} \cdot \Delta I_{L,max}} = \frac{18V \cdot (60V - 18V)}{60V \cdot 400kHz \cdot 0.4 \cdot 6.67A} \cong 11.8\mu H$$

If L=12µH is selected, the inductor current ripple at the minimum input voltage is

$$\Delta I_{L,VIN\_min} = \frac{V_{IN,min} \cdot \left(V_{OUT} - V_{IN,min}\right)}{V_{OUT} \cdot f_{SW} \cdot L} = \frac{8V \cdot (60V - 8V)}{60V \cdot 400kHz \cdot 12\mu H} \cong 1.44A$$

and the maximum inductor current is

$$I_{L,peak,max} = I_{IN,max} + \frac{\Delta I_{L,VIN\_min}}{2} = 6.67A + \frac{1.44A}{2} \cong 7.39A$$

The minimum output current that keeps the converter in CCM with the selected inductor is

$$I_{OUT,min} = \frac{V_{IN,crit}^{\,2} \cdot \left(V_{OUT} - V_{IN,crit}\right)}{2 \cdot V_{OUT}^{\,2} \cdot f_{SW} \cdot L} = \frac{(18V)^2 \cdot \left(60V - 18V\right)}{2 \cdot (60V)^2 \cdot 400kHz \cdot 12\mu H} \cong 0.39A$$

OUTPUT CAPACITORS

If we consider now the output capacitors, the conditions to fulfill are those in Section 1.5 Output capacitors.

Under steady-state conditions, let's consider ΔV_{OUT} to be equal to 0.1 V:

$$C_{OUT} > \frac{I_{OUT,max} \cdot D_{max}}{f_{SW} \cdot \Delta V_{OUT}} = \frac{0.8A \cdot 0.87}{400kHz \cdot 0.1V} \cong 17.3\mu F$$

$$ESR_{OUT} < \frac{\Delta V_{OUT}}{I_{L,peak,max}} = \frac{0.1V}{7.39A} \cong 13.5m\Omega$$

In case of output load removal, let's consider ΔV_{OUT} to be equal to 1 V:

$$C_{OUT} > \frac{L \cdot {I_{L,peak,max}}^2}{{(V_{OUT} + \Delta V_{OUT})}^2 - {V_{OUT}}^2} = \frac{12\mu H \cdot {(7.39A)}^2}{{(60V + 1V)}^2 - {(60V)}^2} \cong 5.4\mu F$$

$$ESR_{OUT} < \frac{\Delta V_{OUT}}{I_{L,peak,max}} = \frac{0.5V}{7.39A} \cong 68m\Omega$$

Let's choose for example C_{OUT} = 33 µF and ESR = 8 mΩ.

The maximum RMS current in the output capacitor is

$$I_{COUT,rms,max} \cong I_{OUT,max} \cdot \sqrt{\frac{D_{max}}{1 - D_{max}}} = 0.8A \cdot \sqrt{\frac{0.87}{1 - 0.87}} \cong 2A$$

INPUT CAPACITORS

The conditions to fulfill are those in Section 1.6 Input capacitors. Let's consider ΔV_{IN} to be equal to 0.1 V:

$$I_{CIN,rms,max} = \frac{\Delta I_{L,max}}{\sqrt{12}} = \frac{0.4 \cdot 6.67A}{\sqrt{12}} \cong 0.77A$$

$$C_{IN} > \frac{\Delta I_{L,max}}{8 \cdot f_{SW} \cdot \Delta V_{IN}} = \frac{0.4 \cdot 6.67A}{8 \cdot 400kHz \cdot 0.1V} \cong 8.3\mu F$$

$$ESR_{IN} < \frac{\Delta V_{IN}}{\Delta I_{L,max}} = \frac{0.1V}{0.4 \cdot 6.67A} = 37.5m\Omega$$

FREEWHEELING DIODE

Section 1.7 Freewheeling diode provides the guidelines for selecting the freewheeling diode. The average forward current rating must be higher than 0.8 A (i.e. the maximum output current) and the peak repetitive forward current rating must be higher than 8.41 A (i.e. the maximum inductor peak current). The breakdown voltage must be at least 72 V (i.e. 20 % higher than the output voltage).

POWER MOSFET

Section 1.8 Power MOSFET provides the guidelines for selecting the Power MOSFET. The breakdown voltage must be at least 72 V (i.e. 20% higher than the output voltage). $R_{DS(ON)}$, package thermal resistance and ambient temperature play a key role in the selection of a suitable Power MOSFET.

STABILITY

In order to determine R_{SH_BST} and R_{SC_BST}, we first have to determine the amount of slope compensation needed:

$$\alpha \geq 1 - \frac{0.5 - \frac{1}{\pi}}{D_{max}} \cong 0.79$$

From Section 1.4 Current sense resistor and Section 1.9.2 Slope compensation we have two equations that are a function of R_{SH_BST} and R_{SC_BST}. Solving for R_{SH_BST}, we get

$$R_{SH\_BST} = \frac{V_{BOOST\_LIM} \cdot L \cdot f_{SW}}{L \cdot f_{SW} \cdot I_{LIMIT} + \alpha \cdot (V_{OUT} - V_{IN,min}) \cdot D_{max}} = \frac{390mV \cdot 12\mu H \cdot 400kHz}{12\mu H \cdot 400kHz \cdot 12A + 0.79 \cdot (60V - 8V) \cdot 0.87} = 20m\Omega$$

and therefore

$$R_{SC\_BST} = \frac{\alpha \cdot (V_{OUT} - V_{IN,min}) \cdot R_{SH\_BST}}{L \cdot I_{SLOPE}} = \frac{0.79 \cdot (60V - 8V) \cdot 20m\Omega}{12\mu H \cdot 20A/s} = 3.4k\Omega$$

With regard to loop stability, it is easy to notice that the RHPZ of the control-to-output transfer function has its lowest value when the output current and the duty cycle are maximum. Therefore, we can calculate the compensation network under these conditions and then verify that the feedback loop is also stable under the other operating conditions.

Considering the external components calculated previously, the control-to-output transfer function in the frequency domain is the following (neglecting the complex poles at half of the switching frequency):

$$\frac{v_{OUT}}{v_C}(f) \cong 59 \cdot \frac{\left(1 + j\frac{f}{603kHz}\right) \cdot \left(1 - j\frac{f}{17.7kHz}\right)}{\left(1 + j\frac{f}{129Hz}\right)}$$

If we select the crossover frequency to be f_C = 5 kHz (approximately one third of the RHPZ), the magnitude of the control-to-output transfer function at the crossover frequency is

$$\left|\frac{v_{OUT}}{v_C}(f_C)\right| = 59 \cdot \frac{\left|1 + j\frac{5kHz}{603kHz}\right| \cdot \left|1 - j\frac{5kHz}{17.7kHz}\right|}{\left|1 + j\frac{5kHz}{129Hz}\right|} \cong 1.58$$

and the phase shift is

$$\phi = arctan\left(\frac{5kHz}{603kHz}\right) - arctan\left(\frac{5kHz}{17.7kHz}\right) - arctan\left(\frac{5kHz}{129Hz}\right) \cong -104°$$

We can apply the known K-factor method to determine the placement of the zero and pole of the compensation network. Considering a Type II compensation network and a phase margin of 60° as a target, the phase boost needed is equal to

$$\theta_{boost} = \phi_{margin} - \phi - 90° = 60° + 104° - 90° = 74°$$

and the K-factor is

$$K = tan\left(\frac{\theta_{boost}}{2} + 45°\right) \cong 7$$

Therefore, we can place the zero of the error amplifier at 714 Hz (f_C/K) and the pole at 35 kHz (f_C*K). We can now easily calculate the compensation network. The amplitude of the error amplifier transfer function at the crossover frequency needs to be the reciprocal of the amplitude of the control-to-output transfer function at that frequency. In mathematical terms, it means

$$\left|\frac{v_C}{v_{OUT}}(f_C)\right| \cong \frac{R_{FB2\_BST}}{R_{FB1\_BST} + R_{FB2\_BST}} \cdot G_M \cdot R_{COMP1} = \frac{1}{1.58}$$

from which we obtain R_{COMP1} = 44 kΩ.

Then we must also have that

$$\frac{1}{2 \cdot \pi \cdot R_{COMP1} \cdot C_{COMP1}} = 714Hz$$

and

$$\frac{1}{2 \cdot \pi \cdot R_{COMP1} \cdot C_{COMP2}} = 35kHz$$

from which we obtain C_{COMP1} = 5 nF and C_{COMP2} = 103 pF.

With the calculated compensation network, it is easy to verify that the overall loop is also stable with sufficient phase margin when D = D_{min} = 70 % and I_{OUT} = $I_{OUT,min}$ = 0.4 A.

Finally, now that the crossover frequency f_C is known, we can check the effect of output load transients with the previously calculated values for C_{OUT} and ESR_{OUT}. With reference to Section 1.5 Output capacitors and assuming a maximum load step of ΔI_{OUT} = 0.4 A, then we have

$$\Delta V_{OUT} = \frac{\Delta I_{OUT}}{2\pi \cdot f_C \cdot C_{OUT}} = \frac{0.4A}{2\pi \cdot 5kHz \cdot 33\mu F} = 0.38V$$

and

$$\Delta V_{OUT} = ESR_{OUT} \cdot \Delta I_{OUT} = 8m\Omega \cdot 0.4A = 3.2mV$$

which we can consider acceptable.

4 Numerical example #2 - buck converter

Let's examine a numerical example for the buck converter based on the following application conditions:

- input voltage V_{BUCKIN}: 60 V
- output voltage V_{LED}: 50 V
- LED current I_{LED}: 700 mA
- LED current ripple ΔI_{LED}: ±5 % of I_{LED} (i.e. 10 % peak-to-peak ripple of I_{LED})
- LED string dynamic resistance $r_{LED,string}$: 6 Ω

DUTY CYCLE AND SWITCHING FREQUENCY

Section 2.2 Duty cycle provides two conditions that the selected VLED_TOFF must fulfill in order for the converter to operate properly. In terms of VLED_TOFF, this means

$$4V \cdot \mu s < VLED\_TOFF < 200V \cdot \mu s$$
$$25V \cdot \mu s < VLED\_TOFF < 500V \cdot \mu s$$

If we combine the two conditions above, it must be that

$$25V \cdot \mu s < VLED\_TOFF < 200V \cdot \mu s$$

Let's choose for example 32V*µs. The resulting switching frequency is

$$f_{SW} = \frac{V_{LED} \cdot \left(1 - \frac{V_{LED}}{V_{BUCKIN}}\right)}{VLED\_TOFF} \cong 260kHz$$

and the duty cycle is

$$D = \frac{V_{LED}}{V_{BUCKIN}} = \frac{50V}{60V} \cong 83\%$$

INDUCTOR

In order to calculate the required inductance, we first have to select an inductor current ripple. If we impose the maximum inductor current ripple to be 40 % of I_{LED}, we can then calculate the inductor as

$$L = \frac{VLED\_TOFF}{\Delta I_L} = \frac{32V \cdot \mu s}{0.4 \cdot 0.7A} \cong 114\mu H$$

Let's select for example L = 120 µH.

When non-idealities are taken into account, we know from Section 2.3 Inductor that the LED current is given by the formula below (for V_{BUCKIN} ≥ 50 V)

$$I_{LED} = \frac{I_{L\_PEAK}}{1.355 - 0.7\% \cdot V_{BUCKIN}} + \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK} - \frac{\Delta I_L}{2}$$

We can thus express I_{L_PEAK} (i.e. the value to be programmed via SPI) as

$$I_{L\_PEAK} = (1.355 - 0.7\% \cdot V_{BUCKIN}) \cdot \left(I_{LED} + \frac{\Delta I_L}{2} - \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK}\right) \cong 0.77A$$

Therefore, we can choose I_{L_PEAK} = 0.78 A. The peak inductor current is given by

$$I_{L,peak} = \frac{I_{L\_PEAK}}{1.355 - 0.7\% \cdot V_{BUCKIN}} + \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK} \cong 0.85A$$

OUTPUT CAPACITOR

The minimum capacitance to meet the LED current ripple requirement is

$$C_{OUT} = \frac{\Delta I_L}{8 \cdot f_{SW} \cdot \Delta i_{LED} \cdot r_{LED,string}} = \frac{0.4 \cdot 0.7A}{8 \cdot 260kHz \cdot 10\% \cdot 0.7A \cdot 6\Omega} \cong 321nF$$

The output capacitor has also the function of limiting the output voltage rise ΔV_{OUT} in case the full output load is removed from the output. If we choose ΔV_{OUT} = 5 V, the minimum output capacitance can be estimated as

$$C_{OUT} = \frac{L \cdot {I_{L,peak}}^2}{(V_{OUT} + \Delta V_{OUT})^2 - {V_{OUT}}^2} = \frac{120\mu H \cdot (0.85A)^2}{(50V + 5V)^2 - (50V)^2} \cong 165nF$$

The most stringent requirement is therefore 321 nF.

It is easy to verify that the ESR values resulting from the equations in Section 2.4 Output capacitors are largely met when using standard ceramic capacitors.

The RMS current in the output capacitor is given by

$$I_{COUT,rms} = \frac{\Delta I_L}{\sqrt{12}} = \frac{0.4 \cdot 0.7A}{\sqrt{12}} \cong 81mA$$

INPUT CAPACITOR

The minimum input capacitance can be calculated as

$$C_{IN} = \frac{I_{LED} \cdot VLED\_TOFF}{(V_{BUCKIN} - V_{LED}) \cdot \Delta V_{IN}} = \frac{0.7A \cdot 32V \cdot \mu s}{(60V - 50V) \cdot 0.1V} \cong 22.4\mu F$$

whereas the maximum ESR can be calculated as

$$ESR_{IN} = \frac{\Delta V_{IN}}{I_{L,peak}} = \frac{0.1V}{0.85A} \cong 118m\Omega$$

The RMS current flowing in the input capacitance is

$$I_{CIN,rms} \cong I_{LED} \cdot \sqrt{D \cdot (1 - D)} \cong 0.7A \cdot \sqrt{0.83 \cdot (1 - 0.83)} \cong 0.26A$$

Considering that the input of the buck converter is the output of the boost converter, the requirements on the boost converter output capacitor are usually more stringent than those on the buck converter input capacitor.

FREEWHEELING DIODE

Section 2.6 Freewheeling diode provides the guidelines for selecting the freewheeling diode. The average forward current can be calculated as

$$I_{DIODE,avg} = I_{LED} \cdot (1 - D) = 0.7A \cdot (1 - 0.83) \cong 0.12A$$

Therefore, the average forward current rating must be higher than 0.12 A and the peak repetitive forward current rating must be higher than 0.85 A (i.e. the maximum inductor peak current). The breakdown voltage must be at least 72 V (i.e. 20 % higher than the input voltage).

5 Numerical example #3 - buck converter

Let's examine a numerical example for the buck converter based on the following application conditions:

- input voltage V_{BUCKIN}: 60 V
- output voltage V_{LED}: 20 V
- LED current I_{LED}: 1500 mA
- LED current ripple ΔI_{LED}: ±5 % of I_{LED} (i.e. 10 % peak-to-peak ripple of I_{LED})
- LED string dynamic resistance $r_{LED,string}$: 4 Ω

DUTY CYCLE AND SWITCHING FREQUENCY

Section 2.2 Duty cycle provides two conditions that the selected VLED_TOFF must fulfill in order for the converter to operate properly. In terms of VLED_TOFF, this means

$$16V \cdot \mu s < VLED\_TOFF < 800V \cdot \mu s$$
$$10V \cdot \mu s < VLED\_TOFF < 200V \cdot \mu s$$

If we combine the two conditions above, it must be that

$$16V \cdot \mu s < VLED\_TOFF < 200V \cdot \mu s$$

Let's choose for example 32V*µs. The resulting switching frequency is

$$f_{SW} = \frac{V_{LED} \cdot \left(1 - \frac{V_{LED}}{V_{BUCKIN}}\right)}{VLED\_TOFF} \cong 417kHz$$

and the duty cycle is

$$D = \frac{V_{LED}}{V_{BUCKIN}} = \frac{20V}{60V} \cong 33\%$$

INDUCTOR

In order to calculate the required inductance, we first have to select an inductor current ripple. If we impose the maximum inductor current ripple to be 40 % of I_{LED}, we can then calculate the inductor as

$$L = \frac{VLED\_TOFF}{\Delta I_L} = \frac{32V \cdot \mu s}{0.4 \cdot 1.5A} \cong 53\mu H$$

Let's select for example L = 68 µH.

When non-idealities are taken into account, we know from Section 2.3 Inductor that the LED current is given by the formula below (for V_{BUCKIN} ≥ 50 V)

$$I_{LED} = \frac{I_{L\_PEAK}}{1.355 - 0.7\% \cdot V_{BUCKIN}} + \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK} - \frac{\Delta I_L}{2}$$

We can thus express I_{L_PEAK} (i.e. the value to be programmed via SPI) as

$$I_{L\_PEAK} = (1.355 - 0.7\% \cdot V_{BUCKIN}) \cdot \left(I_{LED} + \frac{\Delta I_L}{2} - \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK}\right) = 1.5785A$$

Therefore, we can choose I_{L_PEAK} = 1.588 A. The peak inductor current is given by

$$I_{L,peak} = \frac{I_{L\_PEAK}}{1.355 - 0.7\% \cdot V_{BUCKIN}} + \frac{V_{BUCKIN} - V_{LED}}{L} \cdot t_{LOOP\_DELAY\_BUCK} \cong 1.81A$$

OUTPUT CAPACITOR

The minimum capacitance to meet the LED current ripple requirement is

$$C_{OUT} = \frac{\Delta I_L}{8 \cdot f_{SW} \cdot \Delta i_{LED} \cdot r_{LED,string}} = \frac{0.4 \cdot 1.5A}{8 \cdot 417kHz \cdot 10\% \cdot 1.5A \cdot 4\Omega} \cong 300nF$$

The output capacitor has also the function of limiting the output voltage rise ΔV_{OUT} in case the full output load is removed from the output. If we choose ΔV_{OUT} = 20 V, the minimum output capacitance can be estimated as

$$C_{OUT} = \frac{L \cdot {I_{L,peak}}^2}{(V_{OUT} + \Delta V_{OUT})^2 - {V_{OUT}}^2} = \frac{68\mu H \cdot (1.81A)^2}{(20V + 20V)^2 - (20V)^2} \cong 186nF$$

The most stringent requirement is therefore 300 nF.

It is easy to verify that the ESR values resulting from the equations in Section 2.4 Output capacitors are largely met when using standard ceramic capacitors.

The RMS current in the output capacitor is given by

$$I_{COUT,rms} = \frac{\Delta I_L}{\sqrt{12}} = \frac{0.4 \cdot 1.5A}{\sqrt{12}} \cong 173mA$$

INPUT CAPACITOR

The minimum input capacitance can be calculated as

$$C_{IN} = \frac{I_{LED} \cdot VLED\_TOFF}{(V_{BUCKIN} - V_{LED}) \cdot \Delta V_{IN}} = \frac{1.5A \cdot 32V \cdot \mu s}{(60V - 20V) \cdot 0.1V} \cong 12\mu F$$

whereas the maximum ESR can be calculated as

$$ESR_{IN} = \frac{\Delta V_{IN}}{I_{L,peak}} = \frac{0.1V}{1.81A} \cong 55m\Omega$$

The RMS current flowing in the input capacitance is

$$I_{CIN,rms} \cong I_{LED} \cdot \sqrt{D \cdot (1 - D)} \cong 1.5A \cdot \sqrt{0.33 \cdot (1 - 0.33)} \cong 0.71A$$

Considering that the input of the buck converter is the output of the boost converter, the requirements on the boost converter output capacitor are usually more stringent than those on the buck converter input capacitor.

FREEWHEELING DIODE

Section 2.6 Freewheeling diode provides the guidelines for selecting the freewheeling diode. The average forward current can be calculated as

$$I_{DIODE,avg} = I_{LED} \cdot (1 - D) = 1.5A \cdot (1 - 0.33) = 1A$$

Therefore, the average forward current rating must be higher than 1 A and the peak repetitive forward current rating must be higher than 1.81 A (i.e. the maximum inductor peak current). The breakdown voltage must be at least 72 V (i.e. 20 % higher than the input voltage).

Revision history

Table 1. **Document revision history**

Date	Version	Changes
21-Nov-2019	1	Initial release.

Contents

List of tables

List of figures