Increasing the ST25DV-I2C series Dynamic NFC Tags ESD robustness on antenna using an external ESD protection

Introduction

For the purposes of this document, the ST25DV-I2C series Dynamic NFC Tags is replaced by ST25DV-I2C

The absolute maximum electrostatic discharge (ESD) ratings for the mounted ST25DV-I2C mounted on an antenna, are specified at 2 kV human body model (HBM).

The ESD robustness of the ST25DV-I2C mounted on the antenna is improved by adding an external ESD protection component.

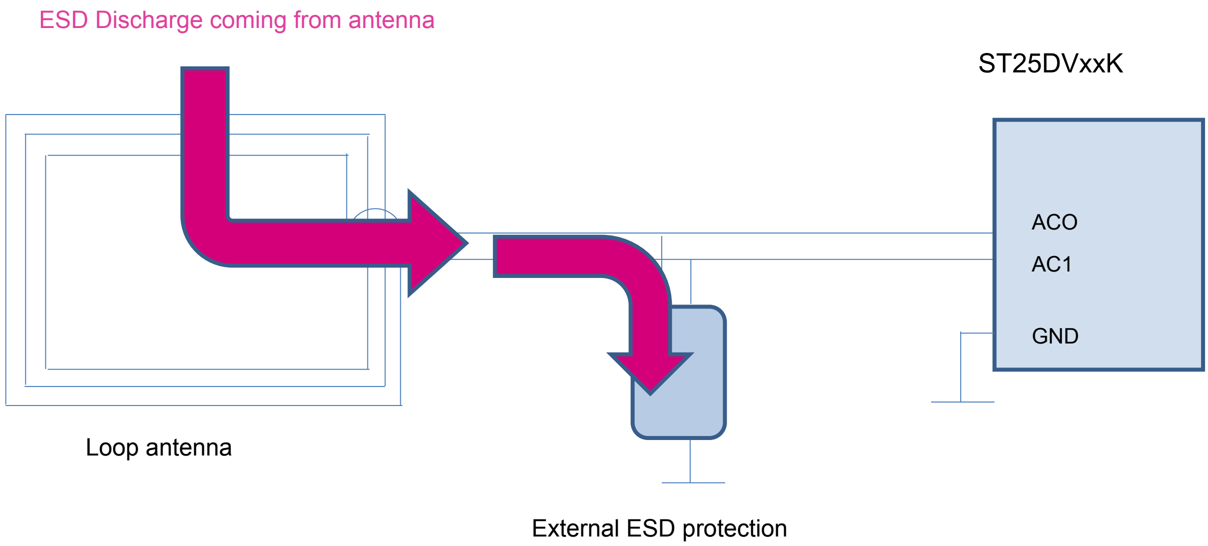
This document describes how to choose a suitable ESD protection, how to implement it. It gives ESD performance measurement results based on the ST25DV-DISCOVERY demonstration antenna embedding the STMicroelectronics USBULC6-2M6 ESD protection.

1 External ESD protection implemented on an ST25DV04K antenna

During the IEC61000-4-2 test process, electrostatic discharges are either applied through the air or by contact using an ESD gun. The test standard is given by *IEC 61000-4-2 standard testing* (AN3353)

Generally speaking, the ESD is picked up by the antenna and dissipated through the AC0 and AC1 pins built-in ESD protections. An external ESD protection is placed between the potential ESD source and the ST25DV-I2C to improve its ESD robustness as illustrated in Figure 1.

Figure 1. External ESD protection on ST25DV-I2C loop antenna



2 Choosing the external ESD protection

The role of an ESD protection is to absorb the high discharge current delivered at a high potential difference to avoid damage to the integrated circuit (IC).

The ESD protection must therefore absorb the discharge current, maintaining an acceptable voltage level for the IC.

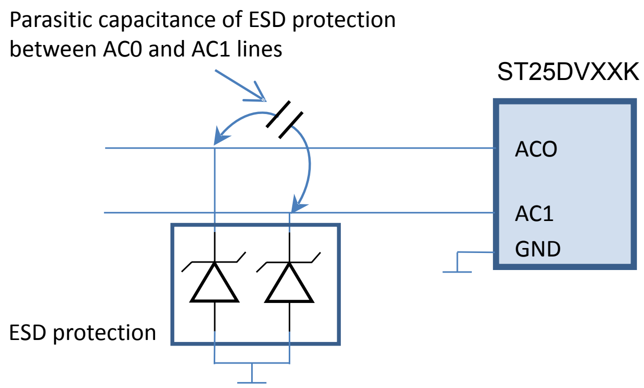
Different parameters must be taken into account when choosing the external ESD protection:

- the break down voltage
- the forward voltage
- the parasitic capacitance of the IC at 13.56 MHz.

Figure 2 describes the equivalent schematic of the ESD protection mounted on the antenna.

Two individual diodes are used to protect AC0 and AC1 RF inputs of the ST25DV-I2C.

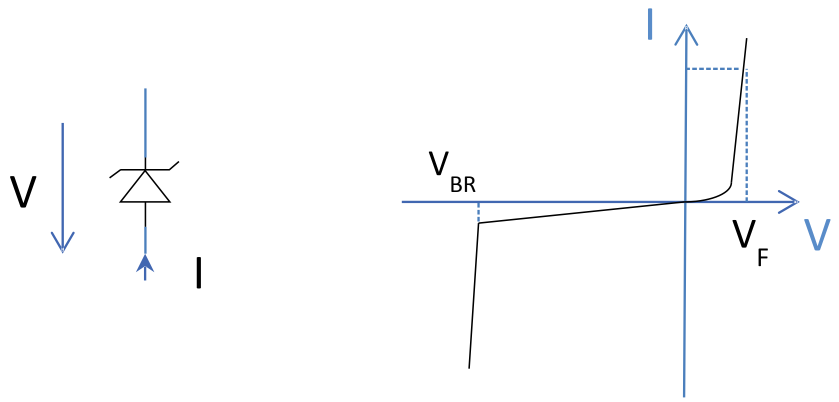
Figure 2. Electrical equivalent schematic of the ESD protection



2.1 Break down voltage and forward voltage of the ESD protection

Figure 3 illustrates the electrical characteristics of an ESD protection.

Figure 3. Electrical characteristics of an ESD protection



The break down voltage (V_{BR}) determines the voltage level at which the ESD protection turns on. To effectively protect the ST25DV-I2C, the V_{BR} must be as low as possible. However, during an RF operation, the RF voltage values present between both: AC0 to GND, and AC1 to GND, are also applied to the external ESD protection. As a consequence, the external ESD protection also clamps the RF voltage on AC0 and AC1 as soon as the RF voltage exceeds V_{BR}. When readers use a low modulation index to communicate with tags, the RF modulation is masked, causing communication holes at short distances. Overcoming this by using a high V_{BR} ESD protection leads to a weak protection of the ST25DV-I2C. To offer the best ESD protection to the ST25DV-I2C (8 kV on contact discharge and 15 kV by air discharge), the external ESD protection voltage levels must be:

- V_{BR} = 6 V
- V_F = 1 V

The voltage level received on either AC0 and AC1 depends on the reader power and antenna, as well as on the tag antenna. The distance at which the communication stops then depends on these parameters but also on the modulation index used by the reader. The RF performance of the ST25DV-I2C tag using an external ESD protection must be validated in the custom system. Since the ESD is affected by the antenna, the ESD robustness must also be validated by the system designer.

2.2 Parasitic capacitance of the ESD protection and tag antenna design

Placing an external ESD protection between the antenna and the ST25DV-I2C causes an additional parasitic capacitance between the AC0 and AC1 lines. If $C_{i/o-i/o}$ is the parasitic capacitance between AC0 and AC1 due to the external ESD protection, and CST25DV-I2C is the ST25DV-I2C built-in tuning capacitance, the total capacitance used to design the tag antenna inductance becomes:

$C_{TOT}= C_{i/o-i/o} + C_{ST25DV-I2C}$

The inductance of the antenna must then satisfy:

$L_{antenna} = 1/(C_{TOT} \times 4 \times \Pi^2 \times F_{tune}^2)$

where F_{tune} is the tuning frequency of the tag.

Note: See the application note How to design an antenna for dynamic NFC tags (AN2972) for more details on antenna design basics.

The read range of the ST25DV-I2C is given by the distance at which the AC0-AC1 AC magnitude voltage roughly reaches 2 V, or the AC0-GND (or AC1-GND) voltage reaches 1.8 V. At this voltage level, the external ESD protection is not active and behaves as a parasitic capacitance. The maximum read range only depends on the reader (power and antenna), the tag antenna (dimension and turns), and the tag antenna tuning frequency. As a consequence, the total capacitance value, including the external ESD protection, is a key parameter for antenna tuning and performance. Its value must be determined before designing the antenna. The low parasitic capacitance ESD protection USBULC6-2M6 is used in next trials: For this part, $C_{I/O-GND}$ is around 1 pF leading to a Cpar between AC0-AC1 around 0.5 pF.

3 Layout rules

The layout and placement of the external ESD protection is an important point in the protection effectiveness: the external ESD protection must be placed in a daisy chain between the ESD source and the ST25DV-I2C (see Figure 4 and Figure 5). The external ESD protection must be placed as close as possible to the ESD source (antenna). Refer to *PCB layout optimization* (AN576) application note for more information.

Figure 4. Efficient ESD protection implementation

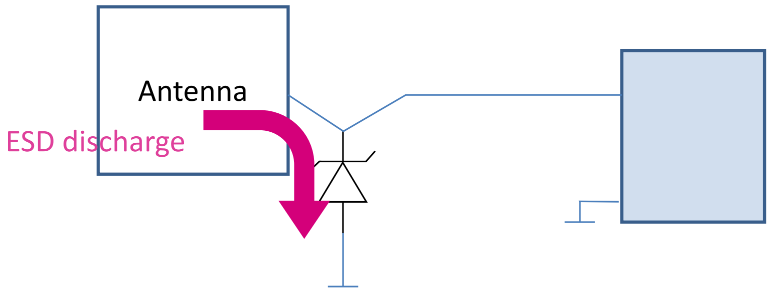
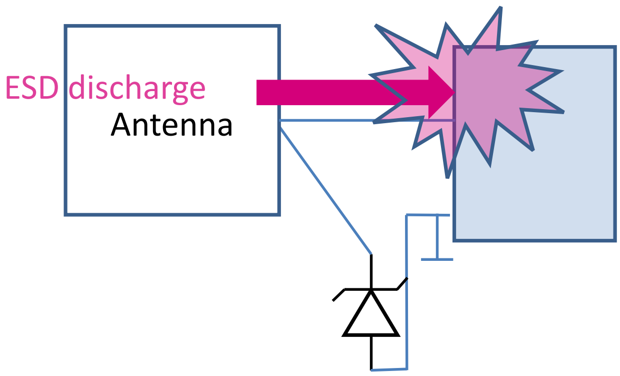


Figure 5. Wrong ESD protection implementation



Note: Use a ground plane instead of ground wires

4 Implementation example

The implementation example uses the USBULC6-2M6 ESD protection and the ST25DV-I2C I²C / ISO15693 Dual Interface EEPROM.

4.1 USBULC6-2M6 connection on the ST25DV-I2C antenna

The pin allocation on ST25DV-I2C is as follows (see Figure 6):

- pins 1 and 6 are connected to the antenna
- pin 2 (GND) is connected to the ground plane
- pin 5 is connected to ST25DV-I2C supply voltage (where V_{CC} is 5V)
- pins 4 and 6 are connected to the antenna.

The overall setup is illustrated in Figure 7

Figure 6. USBULC6-2M6 pinout description

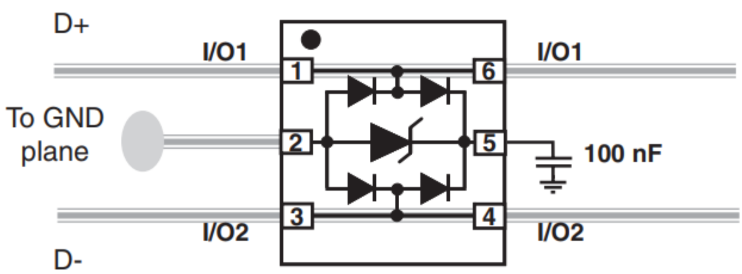
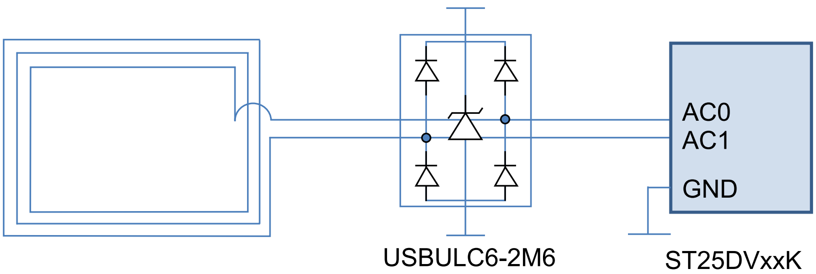


Figure 7. USBULC6-2M6 connection



4.2 ST25DV04K class5 antenna

In the following example, note the GND plane under the ESD protection and the direct connection of the IO pins to the antenna. Ideally, the V_{CC} connection (highlighted in red in Figure 8) should be shorter than the ST25DV40K design. In this case, a jumper for supply source selection on the board is integrated, which extends the VCC line length.

Figure 8. **ST25DV04K class5 antenna layout general view**

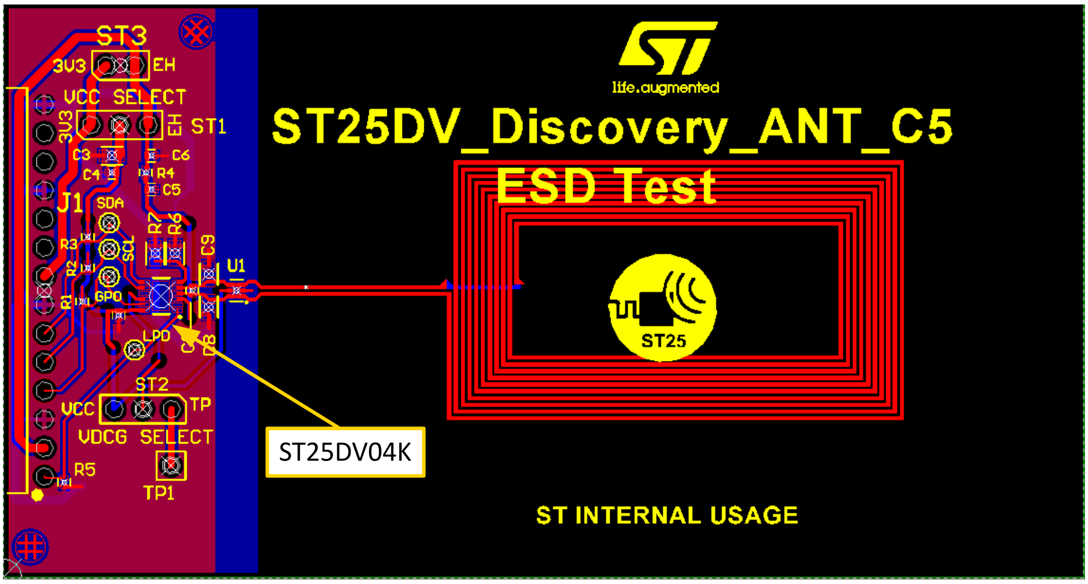
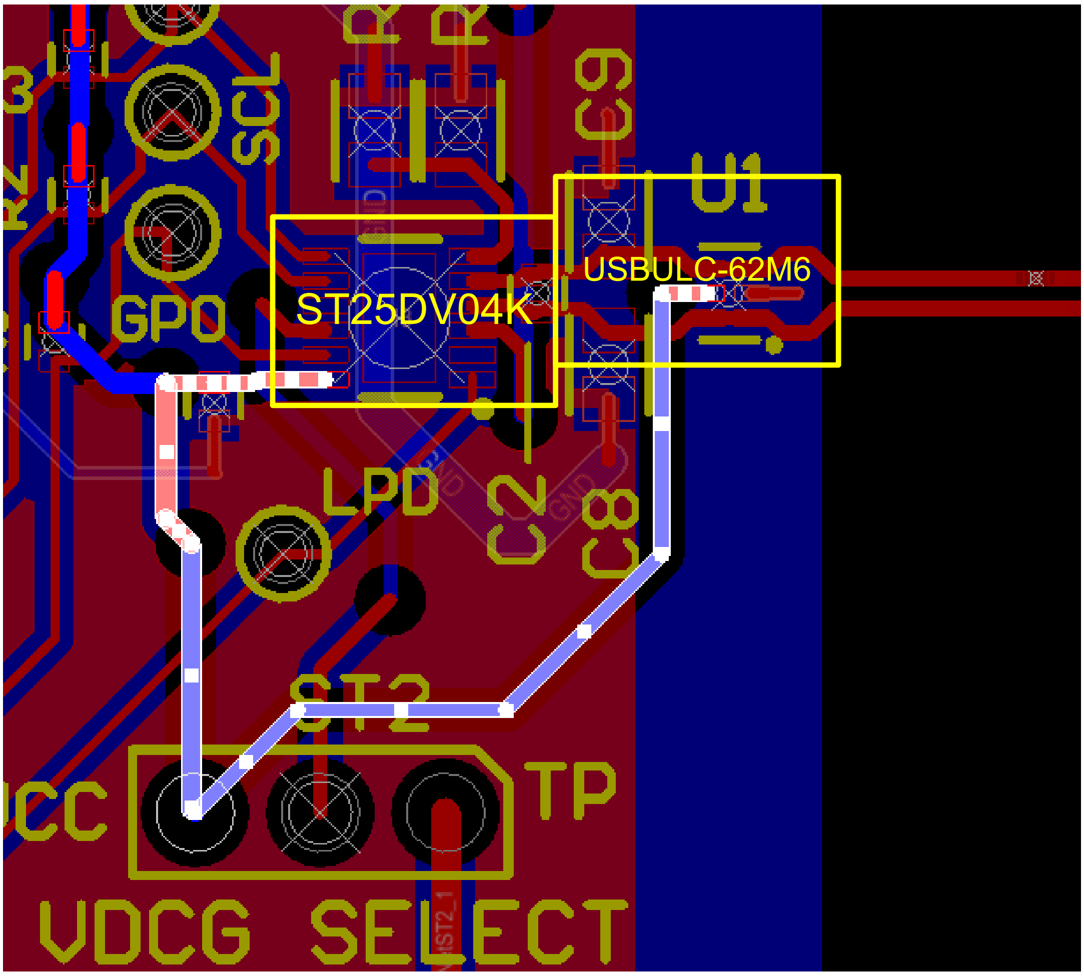


Figure 9. ST25DV04K antenna and USBULC6-2M6



5 ESD test results with USBULC6-2M6 ESD protection and ST25DV04K

ESD tests are performed on the printed circuit board (PCB), with two setups:

- +/-8 kV contact discharge
- +/-15 kV air discharge.

Which corresponds to level 4 in the IEC 61000-4-2 standard.

5.1 IEC 61000-4-2 contact discharge description and results

The contact discharge results are obtained as follows. An ESD discharge is placed at the location identified in Figure 10 and the results are given in Table 1. The experiment is run with and without USBULC6-2M6 ESD protection.

Figure 10. Contact discharge test locations

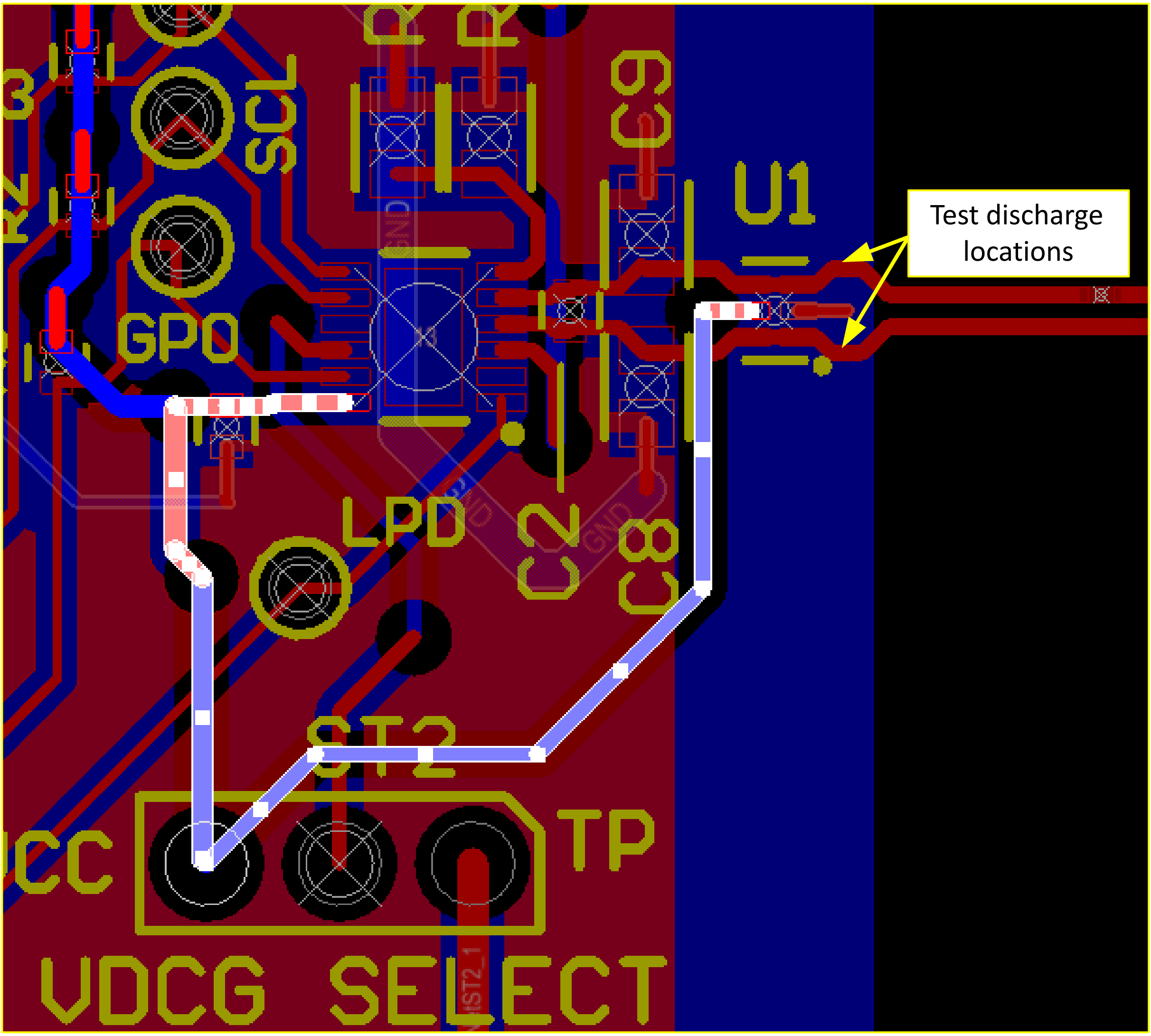


Table 1. **Contact discharge protection level results**

Contact discharge	+/-1 kV	+/-2 kV	+/-3 kV	+/-4 kV	+/-6 kV	+/-8 kV	+/-10 kV	+/-12 kV	+/-15 kV
IEC 61000-4-2	-	Level 1	-	Level 2	Level 3	Level 4	-	-	-
Without USBULC6-2M6	OK	OK	OK	OK	Fail @ 5kV	-	-	-	-
With USBULC6-2M6	-	-	-	-	-	OK	OK	OK	OK

5.2 IEC 61000-4-2 air discharge description and results

The same process is used as in Section 5.1 .

Figure 11 illustrates the discharge points and Table 2 gives the results with and without USBULC6-2M6 ESD protection.

Figure 11. **Air discharge test locations**

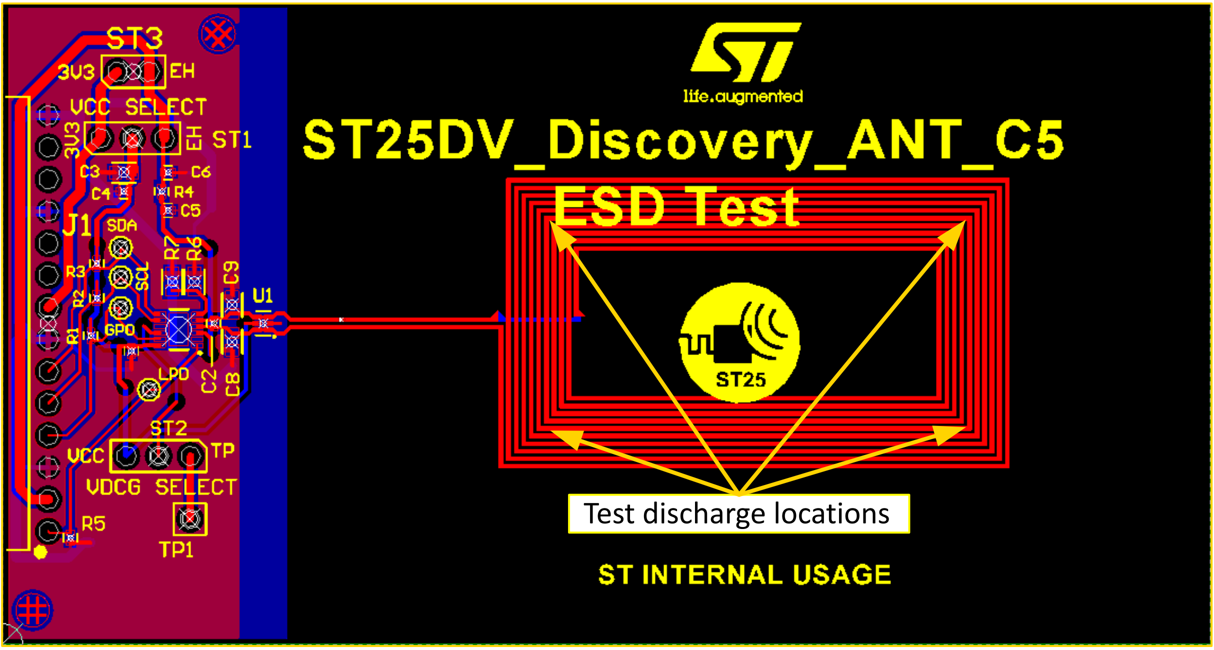


Table 2. **Air discharge protection level results**

Contact discharge	+/-1 kV	+/-2 kV	+/-4 kV	+/-8 kV	+/-10 kV	+/-12 kV	+/-15 kV	+/-17 kV	+/-20 kV
IEC 61000-4-2	-	Level 1	Level 2	Level 3	-	-	Level 4	-	-
Without USBULC6-2M6	-	OK	OK	OK	OK	Fail	-	-	-
With USBULC6-2M6	-	-	-	-	-	OK	OK	OK	OK

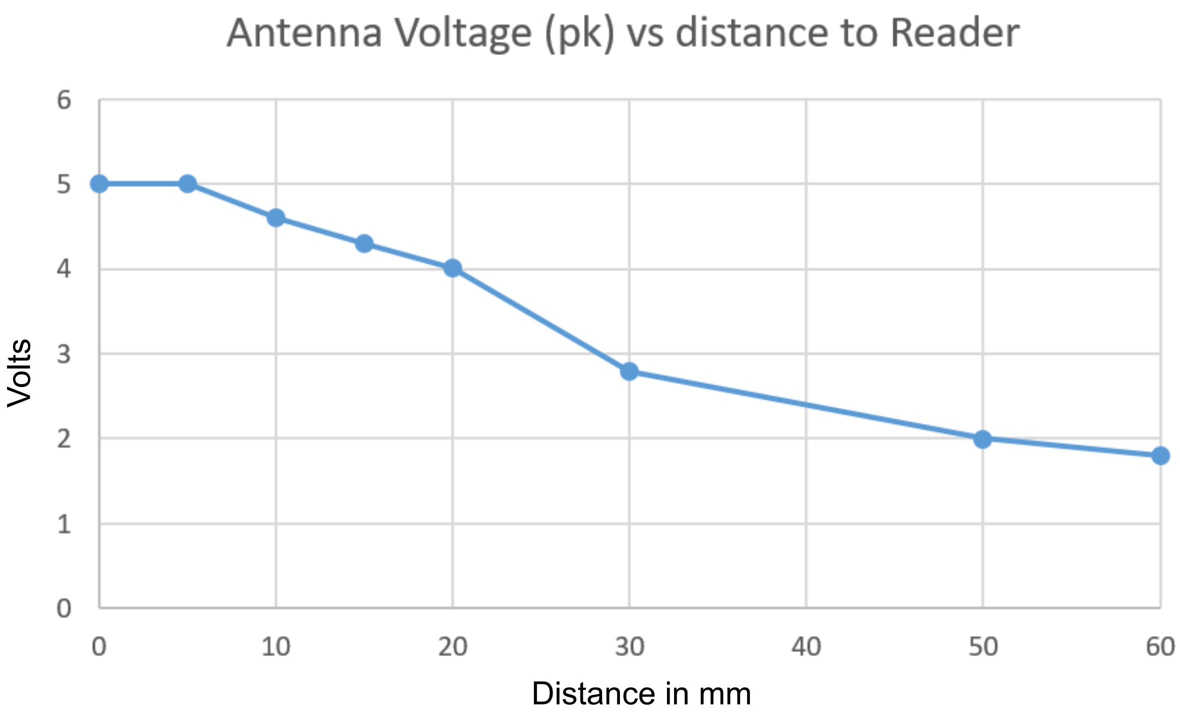
- With USBULC6-2M6: the system passes the IEC 61000-4-2 Level 4
- Without USBULC6-2M6: the system does not pass the IEC 61000-4-2 Level4, only level 2 is achieved

6 RF tests with ST25R95 reader demonstration board

6.1 Antenna voltage

Figure 12 shows an example measurement of the RF voltage amplitude between AC0/1 and GND pins using a ST25R95 reader demonstration board.

Figure 12. Antenna voltage measurement



As expected USBULC6-2M6 is not a clamp antenna voltage which allows the proper operation of the ST25DV-I2C device.

6.2 Frequency tuning

As stated above, $C_{I/O\text{-}GND}$ is 1 pF which results in a $C_{i/o\text{-}i/o}$ of 0.5 pF because the capacitance between AC0 and AC1 are in series.

$C_{ST25DV\text{-}I2C}$ is 28.5 pF with 2 pF tolerance. Influence of USBULC6-2M6 is negligible.

The measurements performed on one board show that without the USBULC6-2M6, F_{tune} is 13.41 MHz; while with USBULC6-2M6, F_{tune} is 13.35 MHz. The system is only slightly affected by the ESD protection parasitic capacitance.

Therefore, the USBULC6-2M6 can be used without any specific antenna design.

Revision history

Table 3. Document revision history

Date	Version	Changes
16-Jan-2020	1	Initial release.

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