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Application note

MDmesh DM6: the last ST super-junction technology with fast recovery diode

Introduction

Each power application has its own requirements and optimization criteria which are reflected in the available technologies paired with innovative package solutions.

It is very difficult, if not even impossible, to fulfill at the same time driving factors like efficiency, power density, EMI, layout parasitic elements, commutation behavior and cost so it is necessary to lead different technologies and solutions.

But the advantages of introducing a new technology may not emerge if you do not adopt both circuitry and layout design criteria that take into account the peculiarity of the new devices. Particular attention must be paid when increasing switching speeds because intrinsic differences between capacities and how they interact with parasitic components of the circuit can lead to undesired results.

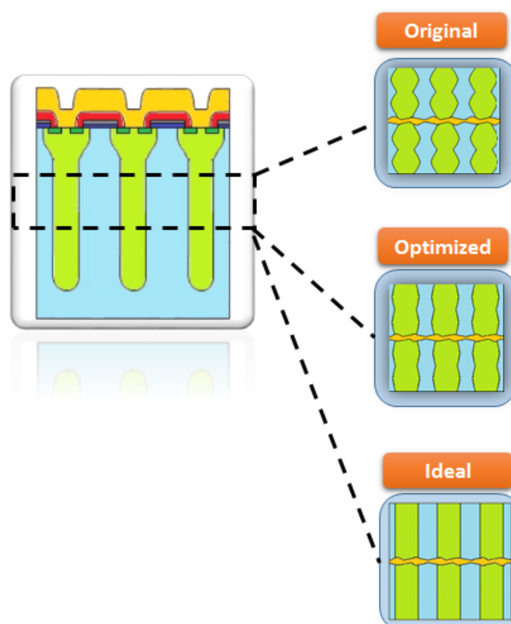
In the following are analyzed some aspect of the MDmesh DM6 series that make this devices suitable for both soft and hard switching applications. This is due not only to very low total gate charge, already an advantage of the previous DM2 series, but also due to turn-off switching losses reduction, especially in the low current range, that is of essence to boost the efficiency in light load conditions where certification rules are more and more stringent. This new technology offers very low reverse recovery charge (Q_{rr}) improving performances in resonant switching topologies where hard switching on a conducting body diode can occur.

An optimization of both the shape and the absolute value of the output capacitance completes the features that make the MDmesh DM6 series well suited to address the target applications.

1 Super-junction (SJ) principle

The basic idea [1][2] of the almost well-known super-junction principle is quite simple: in the on-state the electrons flow through a very low resistive n-area while in the blocking state no electron flow is allowed due to space-charge expansion between the p-doped columns. The practical implementation of this very attractive idea however requires a very sophisticated manufacturing capability due to the mandatory requirement of a perfect compensation of the additional n-charge between adjacent p-columns. Figure below shows the evolution of the column shape towards the ideal one.

Figure 1. Schematic cross section of a vertical super-junction MOSFET: the evolution of the column shape towards the ideal one



The adoption of several optimization starting from the revolutionary principle introduced with super-junction (SJ) devices, has led to different SJ technologies of which the MDmesh DM6 is the last ST’s generation. The resulting technology provides high performance both in hard and soft switching topologies (e.g. PFC, LLC) while not sacrificing the ease of use.

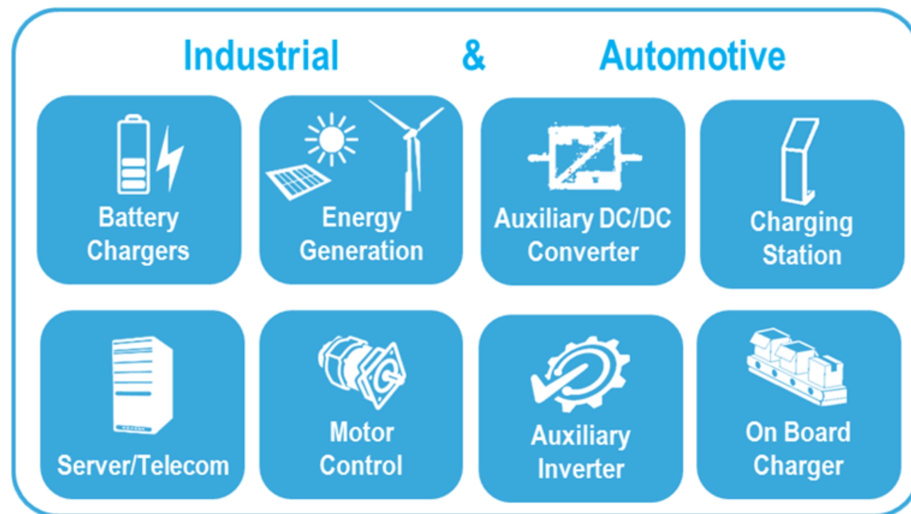
The new MDmesh DM6 series is a step forward in this direction allowing to achieve extremely low switching losses, especially in light load condition, thus enabling switching applications to reach more easily the target certification level and to be designed more compact and lighter. Moreover the improved advantages of the reverse recovery of the body diode lead to much lower power dissipation when hard switching on a conducting body diode occurs.

2 Overview and positioning of DM6 devices

2.1 Target applications

The MDmesh DM6 is the last ST super-junction technology with integrated fast recovery diode and it has been developed to address mainly the high power SMPS for server and telecom applications and the HEV market including OBC (off-board chargers) and charging stations. The following pictogram, in the following figure, summarize the target applications.

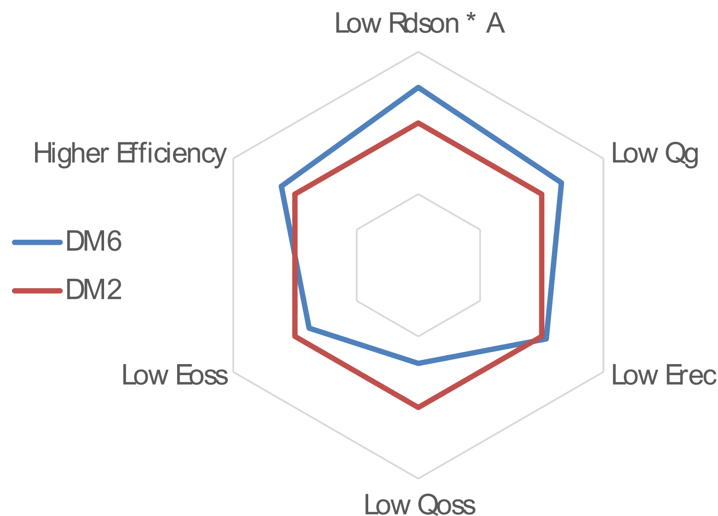
Figure 2. Target applications in industrial and automotive fields



2.2 Predecessors comparison

In the radar chart of the following figure a comparison with the previous super-junction fast diode technology is reported. The obtained improvements in both static and dynamic characteristics lead to higher efficiency in target applications. In particular, comparing device having the same on-resistance, the DM6 one has reduced both power losses during the diode recovery and turn-off of the MOSFET. More detailed results will be reported in the following with focused attention in LLC HB and ZVS PSFB applications

Figure 3. Positioning of the MDmesh DM6 against MDmesh DM2 predecessor



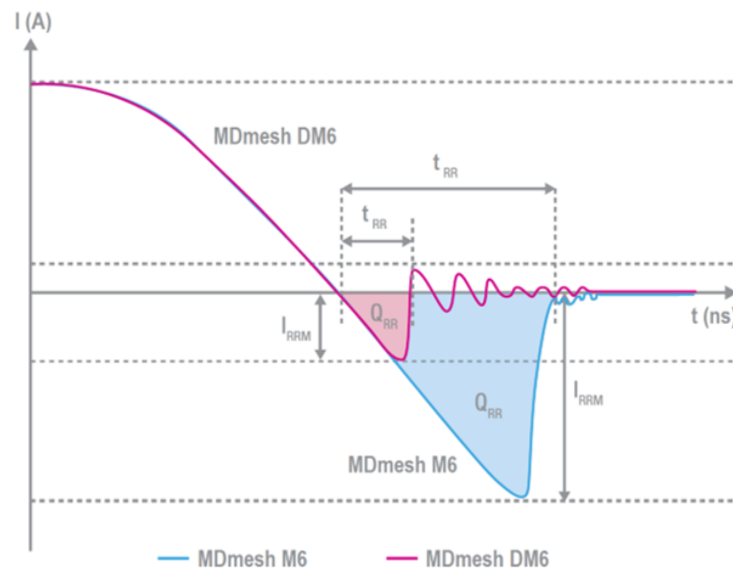
3 Technology main characteristics

A short recap of the characteristic required to a power switch for working well in power converters is given in the following together with a comparison of the main improvements that the new DM6 technology sets out against the DM2 one.

3.1 Body diode characteristics

The following figure shows a qualitative comparison of the recovery current of devices with a fast recovery diode, as the DM6 ones, with respect to a M6 one. The main parameters (Q_{rr}, t_{rr}, I_{rrm}) required for a quantitative comparison are also shown.

Figure 4. **Diode current comparison during recovery**



The DM6 technology offers a very low reverse recovery charge that allows a reduction in power losses and a more safe switching behavior that is required especially in resonant switching topologies where hard commutation on a conducting body diode can occur. In developing the DM6 technology, particular attention was paid to the LLC HB and ZVS PSFB applications. The need to use a fast recovery diode, to ensure reliable operation of ZVT PSFB converters (Figure 5. ZVS PSFB schematic), has long be established. The very fast commutation time from forward conduction of the body diode to forward conduction of MOSFET channel coupled with a very short period to where the device is required to block voltage could not allow enough time for the body diode to clear of minority carriers, Figure 6. Possible dangerous condition in ZVS PSFB circuit if diode recovery is not fast enough. In this case it is mandatory to minimize both the power losses due to the Q_{rr} and have a device rugged enough to sustain the very high dv/dt and dI/dt during diode recovery. The DM6 devices are a step forward in this direction because of their lowest Q_{rr} and higher ruggedness.

Figure 5. ZVS PSFB schematic

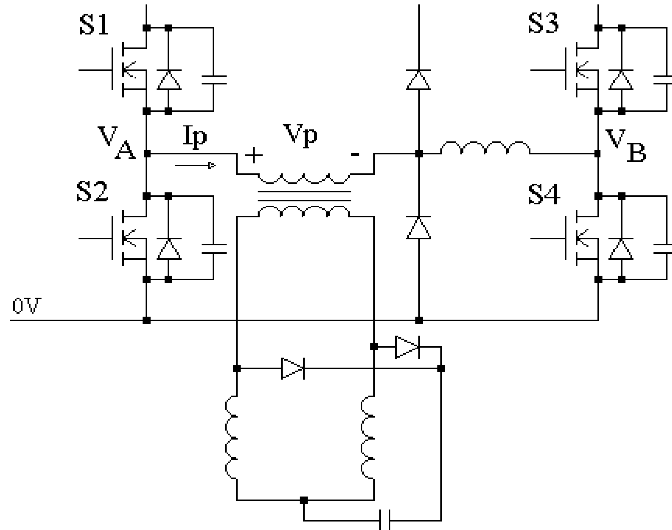
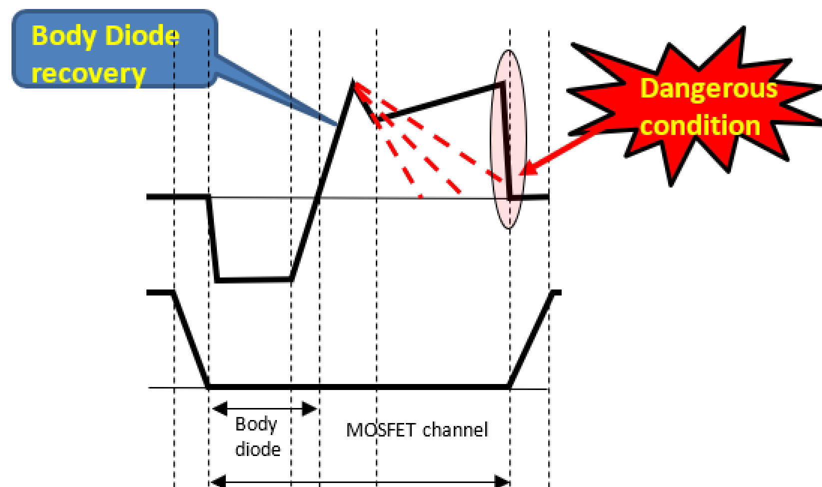


Figure 6. Possible dangerous condition in ZVS PSFB circuit if diode recovery is not fast enough



3.2 Device electrical characteristic comparison

The following table reports a summary of the typical main static and dynamic electrical characteristics of both a DM2 and a DM6 device. In the next sections a deeper analysis of some key parameters will show and explain the technological improvement realized by the DM6 devices.

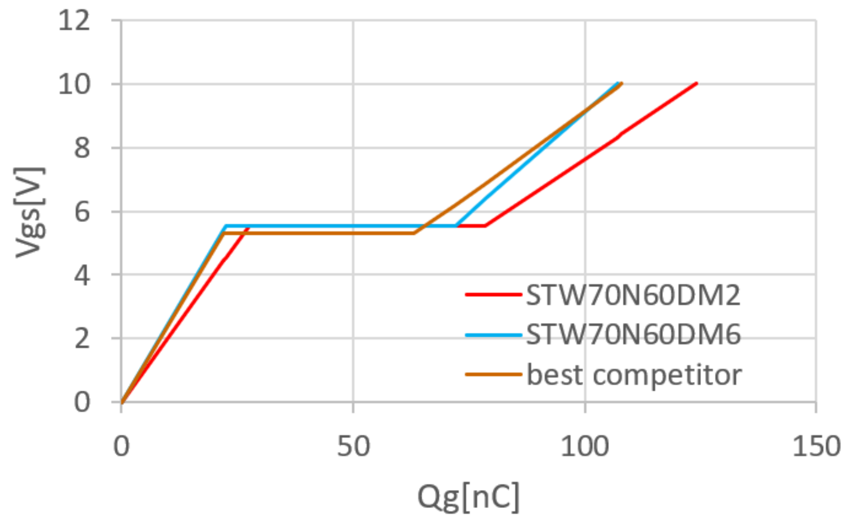
Table 1. DM6 and DM2 device comparison

Symbol	Parameter	Test Condition	STW70N60DM2	STW70N60DM6	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=1mA	600	600	V
I_D	Drain current		66	62	A
$R_{DS(on)}$	Static Drain-source on-resistance	V_{GS}=10V, I_D=32A	37	36	mΩ
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250 mA	4	4	V
R_G	Intrinsic gate resistance		2	1.5	Ω
Q_G	Total gate-charge	V_{DD}=480V, I_D=62A, V_{GD}=10V	121	99	nC
Q_{GS}	Gate-Source charge		26	28	nC
Q_{GD}	Gate-Drain charge		61	44	nC
C_{iss}	Input capacitance	V_{DS}=100V, V_{GS}=0V, f=1MHz	5508	4360	pF
C_{oss}	Output capacitance		241	235	pF
C_{rss}	Reverse capacitance		2.8	13	pF
t_{rr}	Reverse recovery time	I_{SD} = 62A, di/dt = 100 A/µs, V_{DD} = 60 V	150	140	ns
Q_{rr}	Reverse recovery charge		0.75	0.7	µC
I_{RRM}	Reverse recovery current		10.5	10	A

3.2.1 Gate-charge improvements

The gate-charge curve is the main tool for comparing at a glance the on-field behavior that different devices will have in terms of gate driving energy requirements and switching losses. The graph in the following figure show the improved gate-charge curve of DM6 against the DM2 and the best competitor one. Besides very low Q_g, typical of both series, DM6 features a valuable E_{off} reduction, more detail in the next Section 3.2.3 Charge (Qoss) and energy (Eoss) stored in output capacitance, thus reducing the turn-off switching losses in hard switching converters. The driving losses are also reduced leading both to higher switching frequencies.

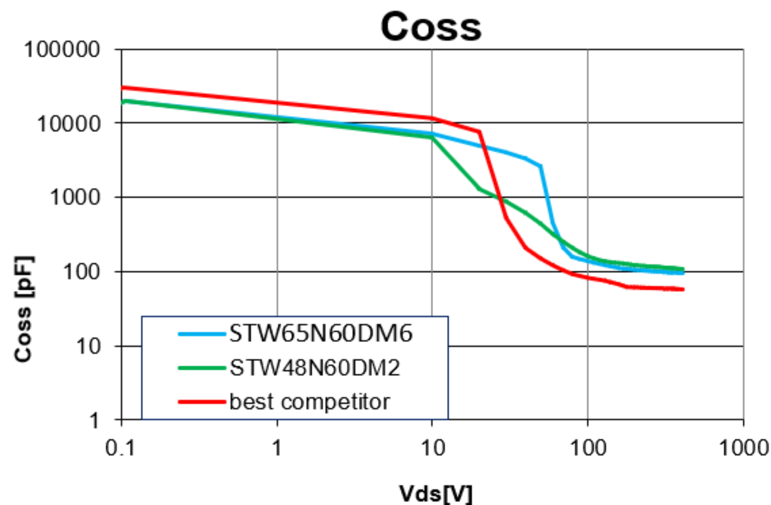
Figure 7. **DM6, DM2 and best competitor gate charge comparison**



3.2.2 Output capacitance profile improvement

The SJ principle, overcoming the intrinsic silicon limit, allows a smaller chip size compared to a conventional Power MOSFET having the same $R_{DS(on)}$. As a consequence all the surface area related characteristics decrease directly with the chip size. Some parameters, however, are also strongly linked to technology characteristics. An evidence of this aspect, not present in standard Power MOSFET, is in the sudden decrease of output capacitance from low to high drain voltage. This is related to the structure of the output capacitance which change from a thin very large surface capacitor, due to the space surface layer at low voltage drain, to orders of magnitude smaller capacitance, due to the fully depletion of the space charge layer, leading to surface capacitor decrease and width increase. The next figure compares the C_{oss} of DM6 and DM2 series. The obtained results are due to both an optimization of the overall column aspect (even if the ratio height to width has been maintained quite constant) and to the modification of the horizontal structure. A sharper capacitance transition from low to high Vds voltage has been obtained. The emphasis of non-linearity of the capacitance characteristic, typical of the SJ structure, helps in achieving lower switching losses. The entity of the achieved improvement will be analyzed in the next sections and some real example of obtainable efficiency improvements will be reported.

Figure 8. **DM6, DM2 and best competitor C_{oss} comparison**



3.2.3 Charge (Q_{oss}) and energy (E_{oss}) stored in output capacitance

The performance improvements introduced by the charge balancing structures include both $R_{DS(on)}$ and all the junction capacitances valuable reduction even if makes the latter much more nonlinear. The effective stored charge and energy in the super-junction MOSFET are significantly reduced but calculating these parameters for comparing different MOSFETs to choose the one that best match our application needs has become not so straightforward. The traditional approach to understanding MOSFET parameters such as C_{oss} and C_{rss} is no longer valid due to the high non linearity they exhibit. Until now, super junction transistors have been used most effectively in hard-switching topologies, where the device is forced to switch even under high current and voltage conditions. The necessity of increasing frequency to achieve higher power density and efficiency has led to resonant converters and to the use of ZVS techniques. The LLC resonant converters, in particular, are widely adopted due to the advantages such as high efficiency, high power density, and low electromagnetic interference in power supply applications among the various power converter designs. In addition to the basic criteria required for power MOSFET selection, the keeping of Zero Voltage Switching (ZVS) operation of the power MOSFET is required together with the avoidance of system reliability issues due to incomplete body diode reverse recovery in the power MOSFET. The minimum inductor current required for ZVS, necessary to charge/discharge the effective capacitance appearing in parallel with drain-sources of the power switches in half-bridge LLC, is related to the capacitance itself. The lower the output capacitance value, the lower the charge to be removed the lower the need for magnetizing current and less dead time. For further details, refer to [3] [4] [5]. Figure 9. Q_{oss}: charge stored in the output capacitance and Figure 10. E_{oss}: energy stored in the output capacitance show that ZVS operation is easier to be achieved with DM2 devices thanks to lower C_{oss} value. Nevertheless this drawback of DM6 against DM2 is not a big issue: the additional losses due to capacitance charge and discharge are generally negligible compared to the overall switching losses. In addition, designing the application to achieve the device turn-on when Vds is around 20 V results in the reduction the recirculating current needed to discharge the output capacitance and being E_{oss} losses quite similar it is possible to benefit of the lower E_{off} losses of DM6.

Figure 9. Q_{oss}: charge stored in the output capacitance

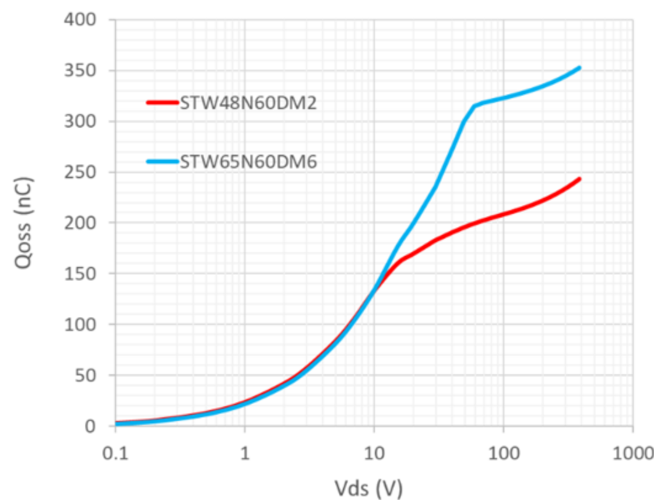
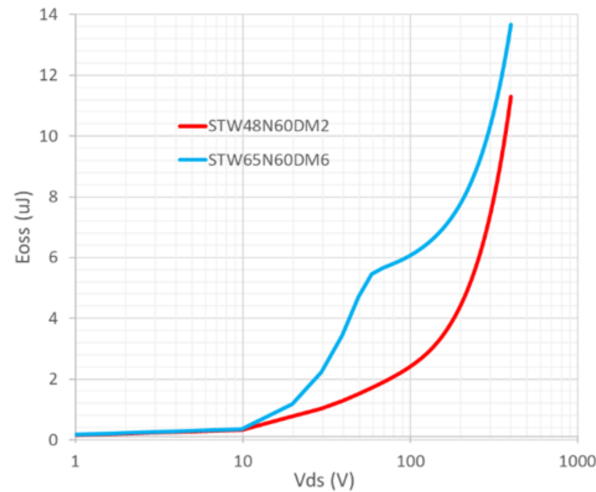


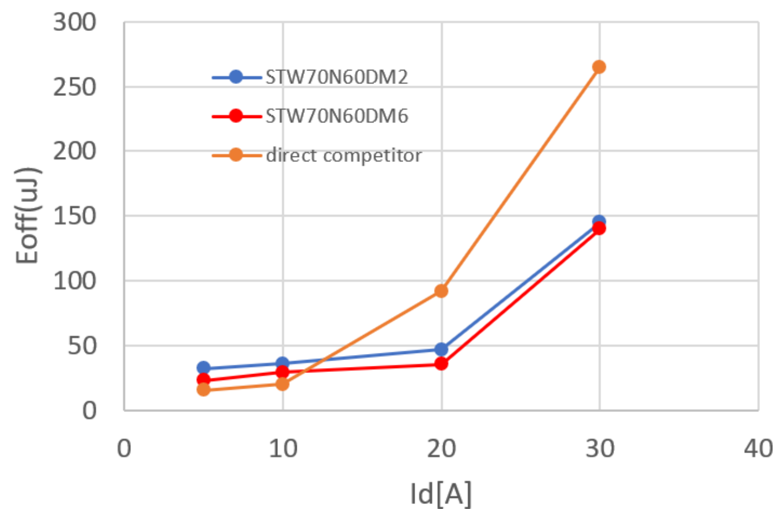
Figure 10. E_{oss}: energy stored in the output capacitance



3.2.4 Switching losses comparison

In the next figure the comparison of switching losses is reported for hard switching at turn off. The DM6 technology exhibits lower losses respect to the previous technology due to both the gate charge and output capacitance profile optimization. So, being almost equivalent from both turn-on and on losses the better choice from efficiency point of view are the DM6 devices. But, being DM6 an even more sophisticated technology respect to the DM2 one, cost implication could arise. So the best tradeoff have to be investigated, mainly in terms of efficiency and cost, being the two technologies equivalent from other aspects as ruggedness, reliability and so on. In Section 4 Measurement results some real example of obtainable efficiency improvements will be reported.

Figure 11. Hard switch E_{off} comparison



4 Measurement results

In the following are reported a comparison of the new DM6 with DM2 standard and direct competitors in some typical application.

4.1 Aux DC-DC converter

In this section the device STW47N60DM6 [6], STW48N60DM2 [7], whose main characteristic are resumed in the next table are compared. As test vehicle has been used the ZVS PSFB section on the primary side of an auxiliary DC-DC converter.

The test condition are:

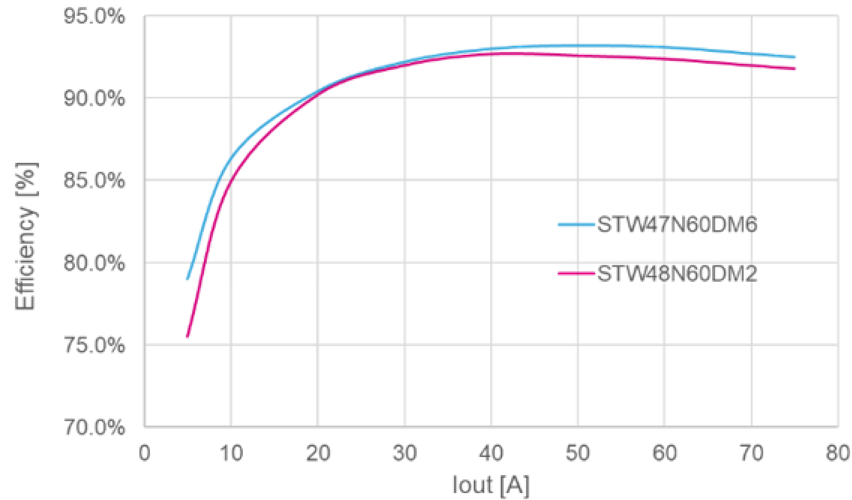
- V_{in} = 350 V
- V_{OUT} = 12 V
- P_{OUT} = 0W to 900W
- f_{SW} = 70 kHz

Table 2. Electrical characteristics of compared devices (STW47N60DM6, STW48N60DM2)

Symbol	Parameter	Test Condition	STW48N60DM2	STW47N60DM6	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	V_{GS}=0V, I_D=1mA	600	600	V
I_D	Drain current		40	36	A
$R_{DS(on)}$	Static Drain-Source on-resistance	V_{GS}=10V, I_D=20A	65	70	mW
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250 mA	4	4	V
R_G	Intrinsic gate resistance		4	1.6	Ω
Q_G	Total gate-charge	V_{DD}=480V, I_D=40A, V_{GD}=10V	70	55	nC
Q_{rr}	Reverse recovery charge	I_{SD} = 40A, di/dt = 100 A/μs,V_{DD} = 60 V	0.7	0.54	μC
I_{RRM}	Reverse recovery current		10	9.50	A

The efficiency measurement reported in the following figure show the advantage of using DM6 devices in comparison with the DM2 ones. In light load condition the measured efficiency improvement is more evident.

Figure 12. **Efficiency comparison between DM2 and DM6 solution**



4.2 Efficiency measurement in LLC HB 700 W

In this section the device STW65N60DM6 [8], STW48N60DM2 [9], whose main characteristic are resumed in the following table, are compared. As test vehicle has been used a 700 W Open Loop LLC system.

The test condition are:

- V_{in} = 400 V
- V_{OUT} = 12 V
- P_{OUT} = 0W to 600W
- f_{SW} = 80 kHz up to 120kHz

The efficiency measurement reported in Figure 13. Efficiency comparison between DM2 and DM6 solution, a direct competitor is also included and Figure 14. Δefficiency referred to DM6 solution shows a higher efficiency of DM6 devices on the whole load range in comparison with the DM2 ones and the direct competition. The best competitor performances however are very close to the DM6 ones.

Table 3. **Electrical characteristics of compared devices (STW65N60DM6, STW48N60DM2)**

Symbol	Parameter	Test Condition	STW48N60DM2	STW65N60DM6	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	V_{GS}=0V, I_D=1mA	600	600	V
I_D	Drain current		40	38	A
$R_{DS(on)}$	Static Drain-Source on-resistance	V_{GS}=10V, I_D=20A	65	62	mW
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250 mA	4	4	V
R_G	Intrinsic gate resistance		4	2	Ω
Q_G	Total gate-charge	V_{DD}=480V, I_D=40A, V_{GD}=10V	70	61	nC
Q_{rr}	Reverse recovery charge	I_{SD} = 40A, di/dt = 100 A/µs,V_{DD} = 60 V	0.7	0.54	µC
I_{RRM}	Reverse recovery current		10	9.50	A

Figure 13. **Efficiency comparison between DM2 and DM6 solution, a direct competitor is also included**

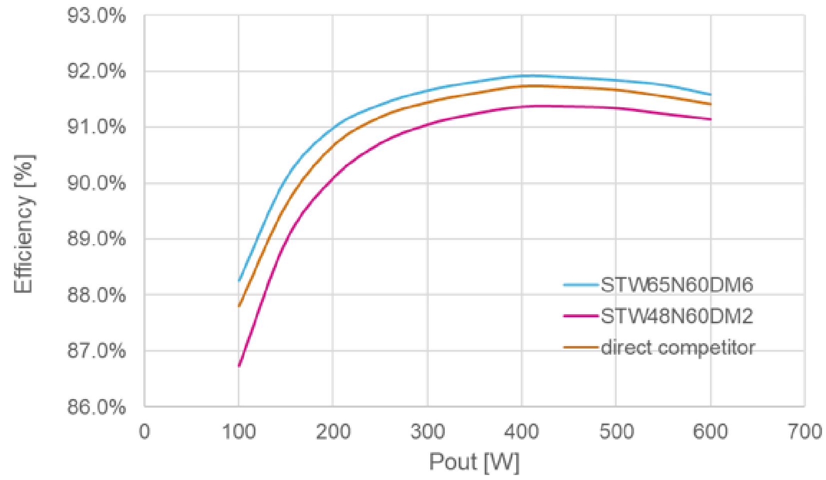
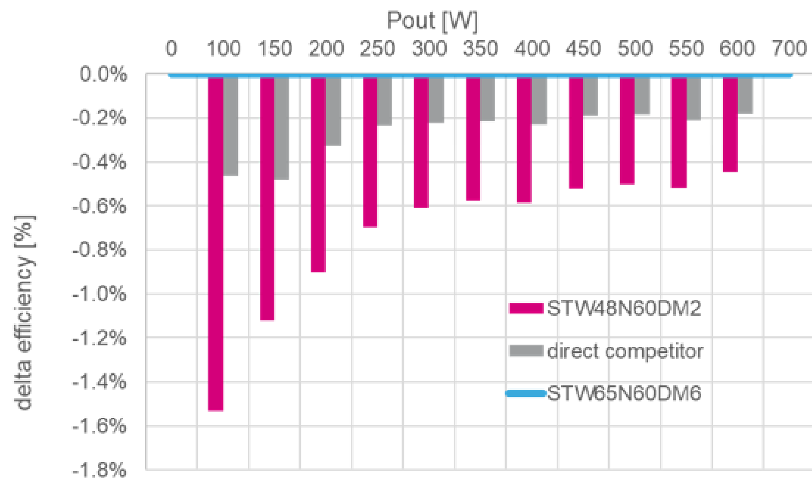


Figure 14. **∆efficiency referred to DM6 solution**



5 Conclusion

This application note presents the new STMicroelectronics super-junction technology called DM6 compared to both the previous DM2 and to competitor ones. This technology is an evolution of the previous DM2 one obtained by some optimization regarding the overall column aspect, thus leading to gate charge and output capacitance improvement and leading to efficiency increase both in hard and soft switching applications.

Tests were performed on several application board comparing devices performance. The results have shown that the output capacitance profile influences the switching operation and determines the total efficiency of the system. The optimization of this aspect in MDmesh DM6 devices offers higher efficiency, especially when the system operates in light load condition. In addition the improved performances of the intrinsic fast recovery diode give a more safe switching behavior that is required especially in resonant switching topologies where hard commutation on a conducting body diode can occur.

6 References

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[6] "STF47N60DM6 data sheet," [Online].

[7] "STF48N60M2 data sheet," [Online].

[8] "STW65N60DM6 data sheet," [Online].

[9] "STW48N60DM2 data sheet," [Online].

Revision history

Table 4. **Document revision history**

Date	Version	Changes
11-Dec-2019	1	Initial release.

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