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Application note

Migration between SPC584Bx and SPC584Cx/SPC58ECx

Introduction

SPC584Bx is an optimized derivative of SPC584Cx/SPC58ECx, as such it features less memory, cores, peripheral and I/O.

During SPC584Bx specification and development, focus has been put to keep both devices HW and SW compatible, but some features had to be adjusted with respect to the optimized architecture, such as the flash module with a single 2 MB code flash partition as well as a single data partition shared by the main core and the HSM core.

This document describes the differences between the two devices to help designers to develop an application compatible with both devices or migrating from one device to another.

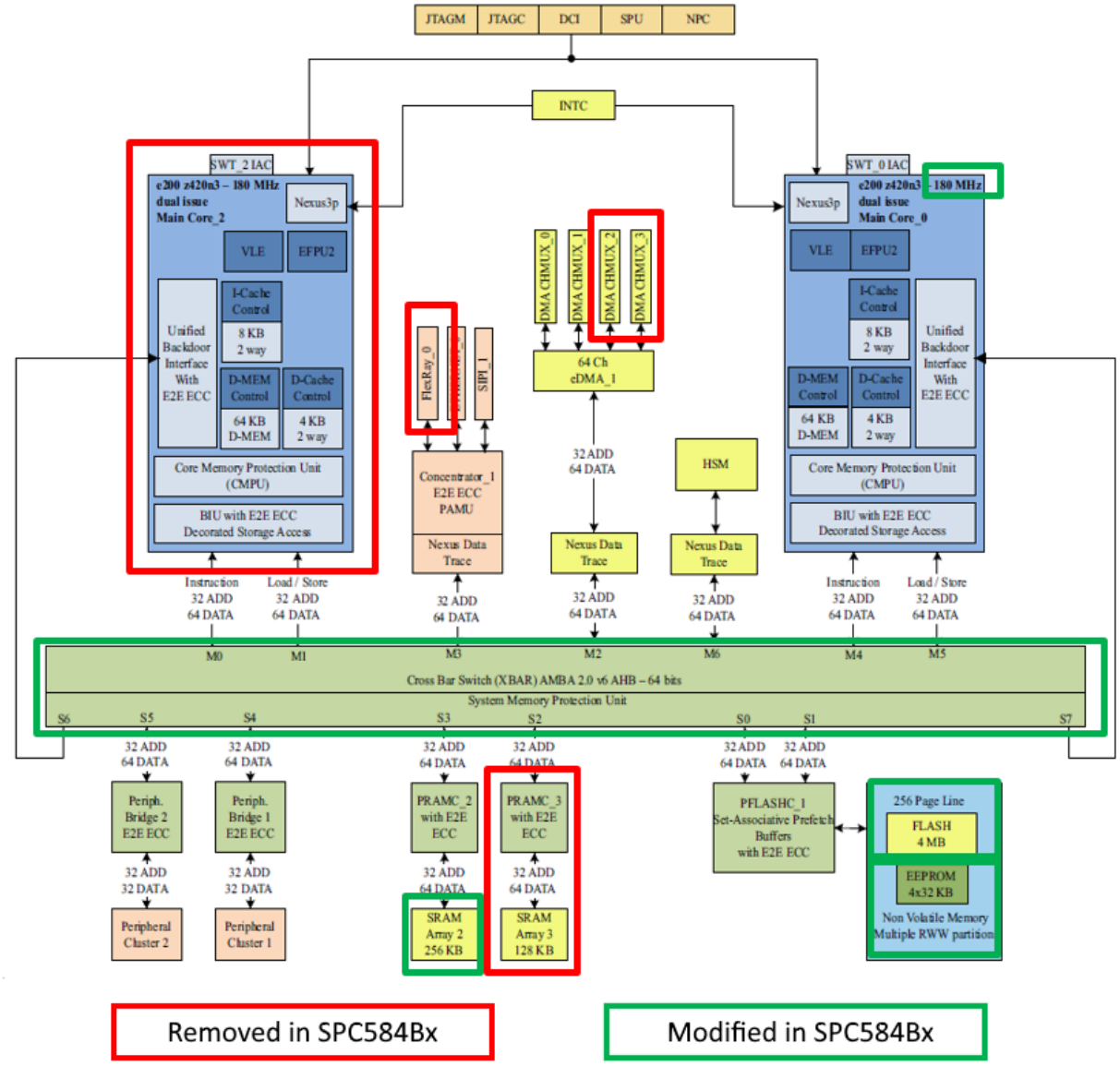
The following features are covered in this document:

- Architecture
- Cores/Platform
- SRAM
- Flash
- Peripherals
- Pinout
- Power Supply
- Power Consumption

1 Architecture

1.1 SPC584Cx/SPC58ECx architecture

Figure 1. **SPC584Cx/SPC58ECx architecture**



Removed in SPC584Bx:

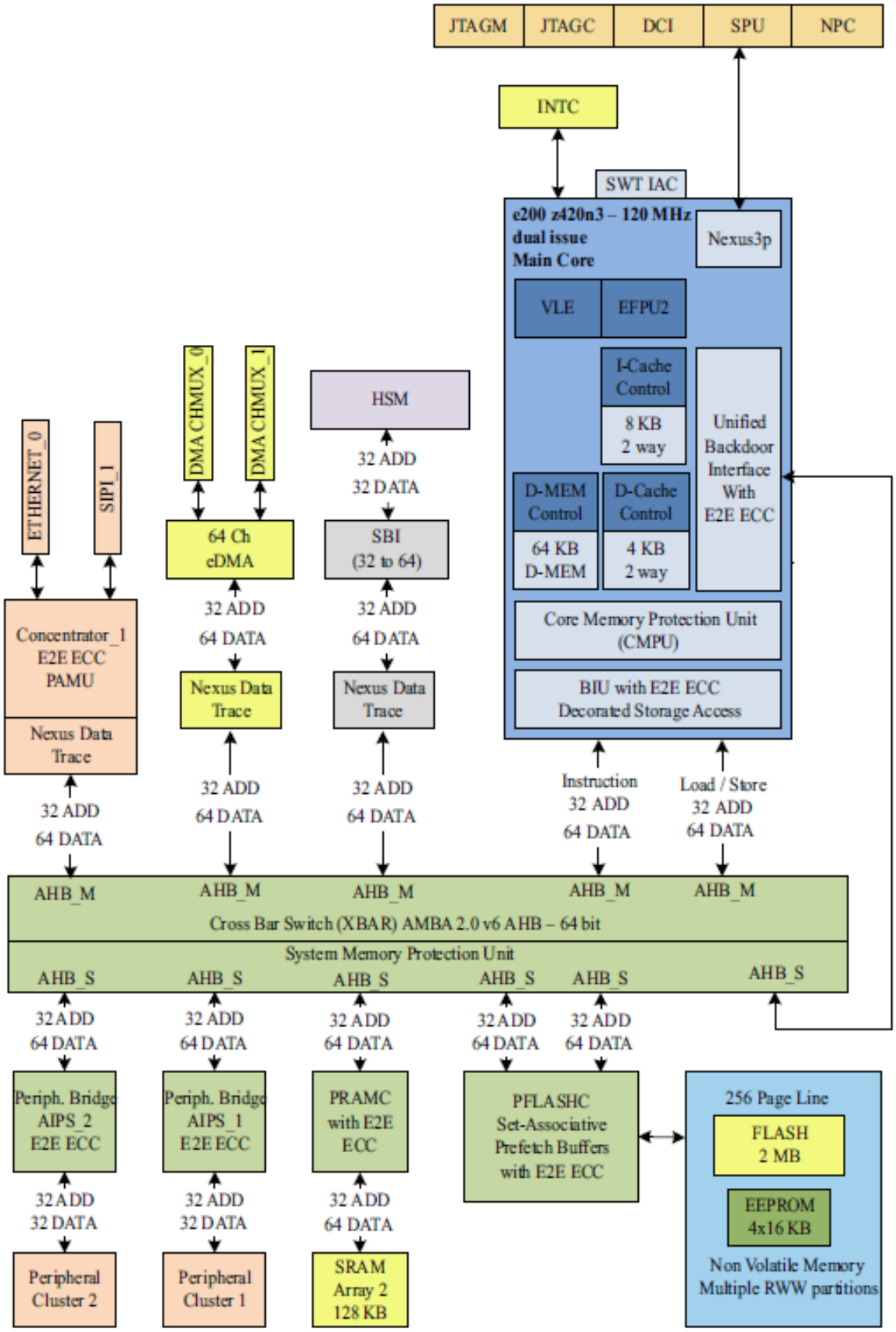
- Main Core2
- FlexRay_0
- DMA CHMUX_2/3
- SRAM
  - PRAMC_3
  - SRAM Array 3 (128K)

Modified in SPC584Bx:

- Main Core 0 max freq (180 MHz vs 120 MHz)
- XBAR/SMPU
- SRAM Array 2 size (256K vs 128K)
- CFLASH size (4M vs 2M)
- DFLASH size (4 x 32K vs 4 x 16K)
- C/DFLASH different sectorization
- different RWW partitions (4 vs 2)

1.2 SPC584Bx architecture

Figure 2. **SPC584Bx architecture**



2 Platform

2.1 Cores and SMPU

Figure 3. **Cores and SMPU**

	Commercial Code	SPC584Cx / SPC58ECx		SPC584Bx
		Reference device		Comparison vs CHO4M
	Item	Feature		Feature
Core / Platform	Core Number	2x z4		1x z4
	Core 0	z420		z420
	I$/D$ - I_Mem/D_Mem	8K/4K -/64K		8K/4K -/64K
	Core 1	-		-
	I$/D$ - I_Mem/D_Mem	-		-
	Core 2	z420		N/A
	I$/D$ - I_Mem/D_Mem	8K/4K - /64K		N/A
	Core MPU	24 regions / core		24 regions / core
	System MPU	24 regions		16 regions

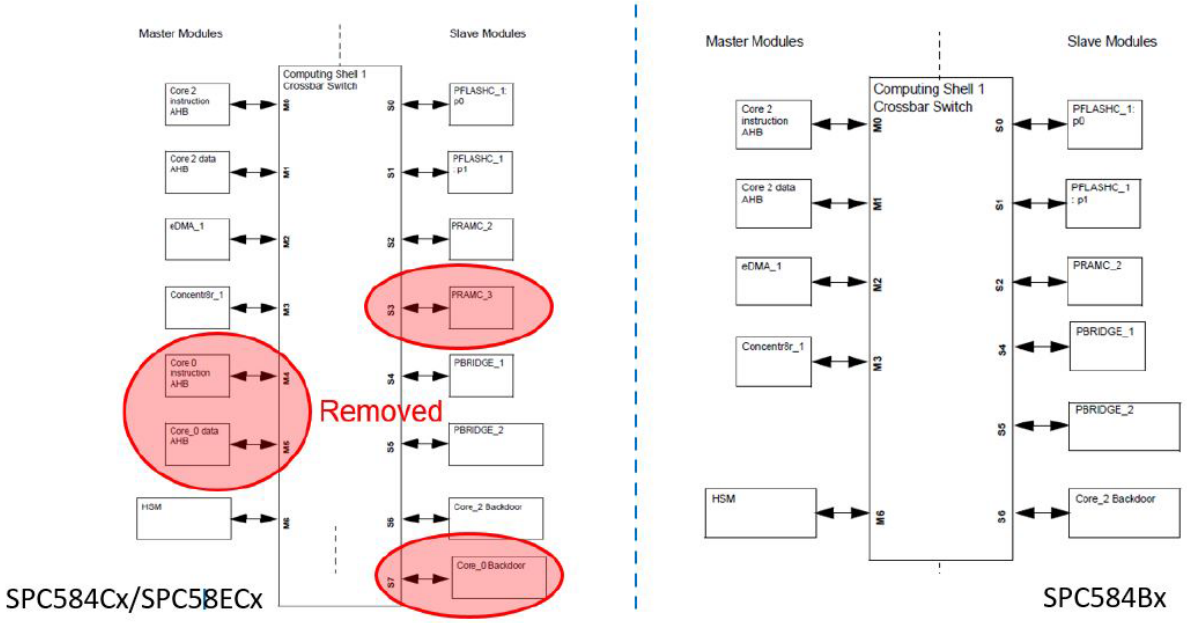
Below are the main differences between the two devices:

- on SPC584Bx the 2nd z4 core has been removed
- SMPU regions reduced from 24 to 16

2.2 XBAR

On SPC584Bx the ports related to the second core (Core0) have been obviously removed but compatibility is maintained on the other Masters and Slaves port numbers.

Figure 4. **XBAR**



3 SRAM

SPC584Cx/SPC58ECx:

Table 1. SPC584Cx/SPC58ECx RAM options

SPC58EC80	SPC584C80	SPC58EC74	SPC584C74	SPC58EC70	SPC584C70	Type	Start address	End address
512[1]	384[1]	416[1]	320[1]	320[1]	256[1]			
8	8	8	8	8	8	PRMAC_2 (STBY)	0x400A8000	0x400A9FFF
24	24	24	24	24	24	PRMAC_2 (STBY)	0x400AA000	0x400AFFFF
160	160	160	160	160	160	PRMAC_2 (STBY)	0x400B0000	0x400D7FFF
64	64	64	64	NA	NA	PRMAC_2 (STBY)	0x400D0000	0x400E7FFF
32	32	32	NA	NA	NA	PRMAC_3	0x400E0000	0x400EFFFF
32	32	NA	NA	NA	NA	PRMAC_3	0x400F0000	0x400F7FFF
63,75	NA	NA	NA	NA	NA	PRMAC_3	0x400F0000	0x40107EFF
0,25	0,25	0,25	0,25	0,25	0,25	PRMAC_3	0x40107F00	0x40107FFF
64	NA	64	64	64	NA	D-MEM CPU_0	0x50800000	0x5080FFFF
64	64	64	64	64	64	D-MEM CPU_2	0x52800000	0x5280FFFF

1. *RAM size is the sum of TCM and SRAM*

SPC584Bx:

Table 2. SPC584Bx RAM options

SPC584B70	SPC584B64	SPC584B60	Type	Start address	End address
192[1]	160[1]	128[1]			
8	8	8	PRMAC_2 (STBY)	0x400A8000	0x400A9FFF
24	24	24	PRMAC_2 (STBY)	0x400AA000	0x400AFFFF
32	32	32	PRMAC_2 (STBY)	0x400B0000	0x400B7FFF
32	32	NA	PRMAC_2 (STBY)	0x400B8000	0x400BFFFF
32	NA	NA	PRMAC_2 (STBY)	0x400C0000	0x400CFFFF
64	64	64	D-MEM CPU_2	0x52800000	0x5280FFFF

1. *RAM size is the sum of TCM and SRAM*

With STBY RAM (max):

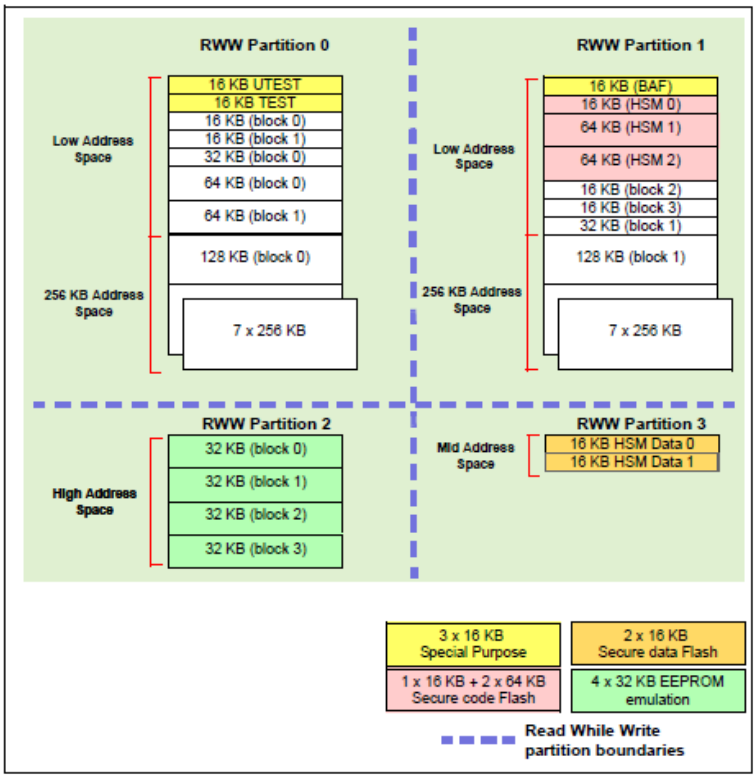
- 192Kbyte – 256Kbyte (on SPC584Cx/SPC58ECx)
- 64Kbyte – 128Kbyte (on SPC584Bx)

4 Flash

4.1 Segmentation and RWW partitioning

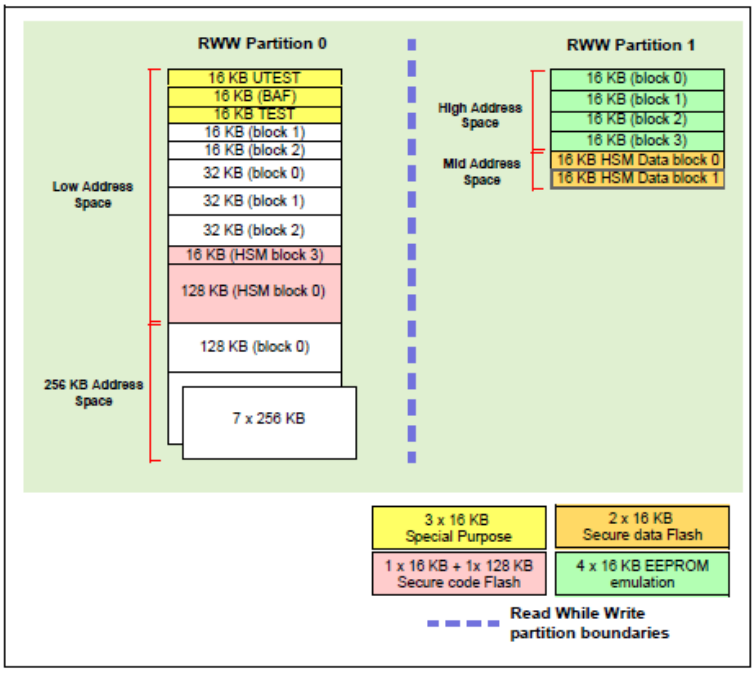
SPC584Cx/SPC58ECx:

Figure 5. Flash memory segmentation and read-while-write partitioning



SPC584Bx:

Figure 6. **Flash memory segmentation and read-while-write partitioning**

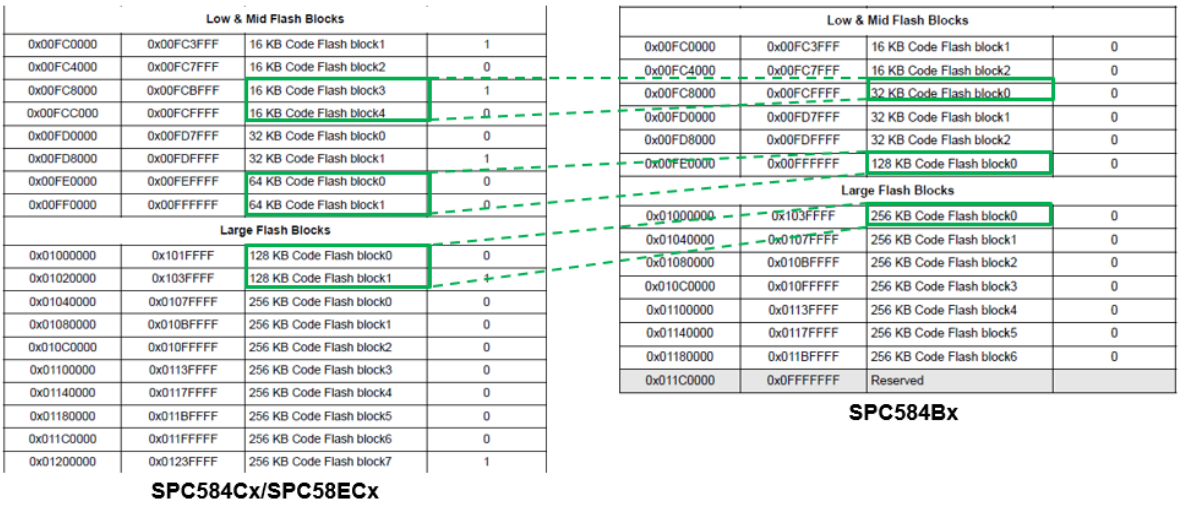


4.2 Code flash sectorization

On SPC584Bx, few sectors have been merged to cope with the maximum number of sectors supported in a flash partition:

- @0x00FC8000 → one block of 32 KB instead of the two 16 KB implemented on SPC584Cx/SPC58ECx
- @0x00FE0000 → one block of 128 KB instead of the two 64 KB implemented on SPC584Cx/SPC58ECx
- @0x01000000 → one block of 256 KB instead of the two 128 KB implemented on SPC584Cx/SPC58ECx

Figure 7. Flash partition



Low & Mid Flash Blocks			
0x00FC0000	0x00FC3FFF	16 KB Code Flash block1	1
0x00FC4000	0x00FC7FFF	16 KB Code Flash block2	0
0x00FC8000	0x00FCBFFF	16 KB Code Flash block3	1
0x00FCC000	0x00FCFFFF	16 KB Code Flash block4	0
0x00FD0000	0x00FD7FFF	32 KB Code Flash block0	0
0x00FD8000	0x00FDFFFF	32 KB Code Flash block1	1
0x00FE0000	0x00FEFFFF	64 KB Code Flash block0	0
0x00FF0000	0x00FFFFFF	64 KB Code Flash block1	0
Large Flash Blocks			
0x01000000	0x101FFFF	128 KB Code Flash block0	0
0x01020000	0x103FFFF	128 KB Code Flash block1	0
0x01040000	0x0107FFFF	256 KB Code Flash block0	0
0x01080000	0x010BFFFF	256 KB Code Flash block1	0
0x010C0000	0x010FFFFF	256 KB Code Flash block2	0
0x01100000	0x0113FFFF	256 KB Code Flash block3	0
0x01140000	0x0117FFFF	256 KB Code Flash block4	0
0x01180000	0x011BFFFF	256 KB Code Flash block5	0
0x011C0000	0x011FFFFF	256 KB Code Flash block6	0
0x01200000	0x0123FFFF	256 KB Code Flash block7	1

SPC584Cx/SPC58ECx

Low & Mid Flash Blocks			
0x00FC0000	0x00FC3FFF	16 KB Code Flash block1	0
0x00FC4000	0x00FC7FFF	16 KB Code Flash block2	0
0x00FC8000	0x00FCFFFF	32 KB Code Flash block0	0
0x00FD0000	0x00FD7FFF	32 KB Code Flash block1	0
0x00FD8000	0x00FDFFFF	32 KB Code Flash block2	0
0x00FE0000	0x00FFFFFF	128 KB Code Flash block0	0
Large Flash Blocks			
0x01000000	0x103FFFF	256 KB Code Flash block0	0
0x01040000	0x0107FFFF	256 KB Code Flash block1	0
0x01080000	0x010BFFFF	256 KB Code Flash block2	0
0x010C0000	0x010FFFFF	256 KB Code Flash block3	0
0x01100000	0x0113FFFF	256 KB Code Flash block4	0
0x01140000	0x0117FFFF	256 KB Code Flash block5	0
0x01180000	0x011BFFFF	256 KB Code Flash block6	0
0x011C0000	0x0FFFFFFF	Reserved	

SPC584Bx

4.3 HSM code flash sectorization

On SPC584Bx, HSM code sectors have been merged to cope with the maximum number of sectors supported in a flash partition:

- @0x00610000 → one block of 128 KB instead of the two 64KB implemented on SPC584Cx/SPC58ECx

Figure 8. Flash sectorization

Security Code Flash Blocks			
0x0060C000	0x0060FFFF	16 KB HSM Code block5	1
0x00610000	0x0061FFFF	64 KB HSM Code block2	1
0x00620000	0x0062FFFF	64 KB HSM Code block3	1
0x00630000	0x0067FFFF	Reserved	

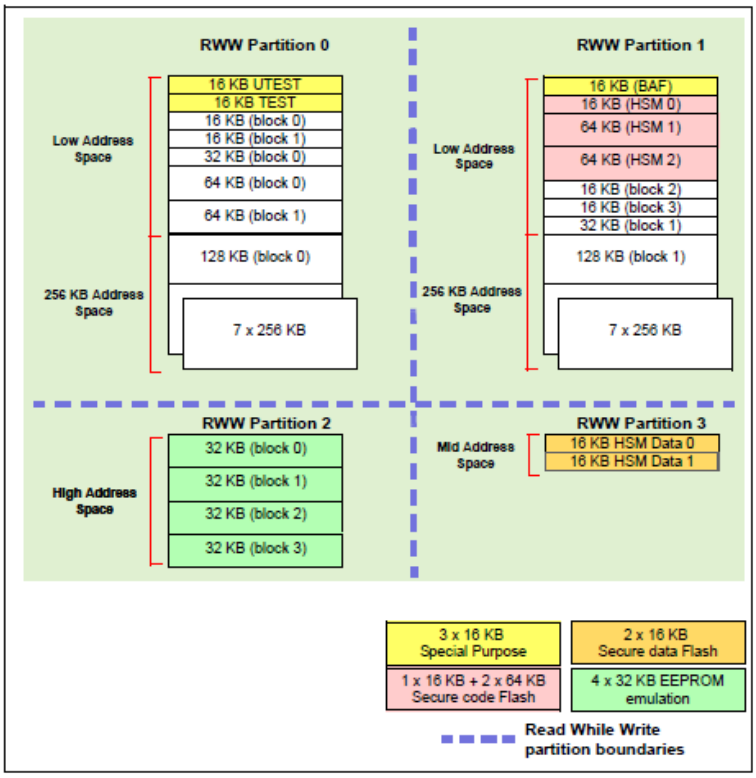
SPC584Cx/SPC58ECx

Security Code Flash Blocks			
0x0060C000	0x0060FFFF	16 KB HSM Code block3	0
0x00610000	0x0062FFFF	128 KB HSM Code block0	0
0x00630000	0x0067FFFF	Reserved	

SPC584Bx

4.4 SPC584Cx/SPC58ECx: RWW partitions

Figure 9. **Flash memory segmentation and read-while-write partitioning**



Four RWW partitions are implemented, where:

- Partition 0 contains Host Code blocks
- Partition 1 contains HSM Code (and Host Code) blocks
- Partition 2 contains Host Data blocks
- Partition 3 contains HSM Data blocks

This partitioning allows following RWW accesses among Host (cores) and HSM:

Figure 10. **RWW accesses**

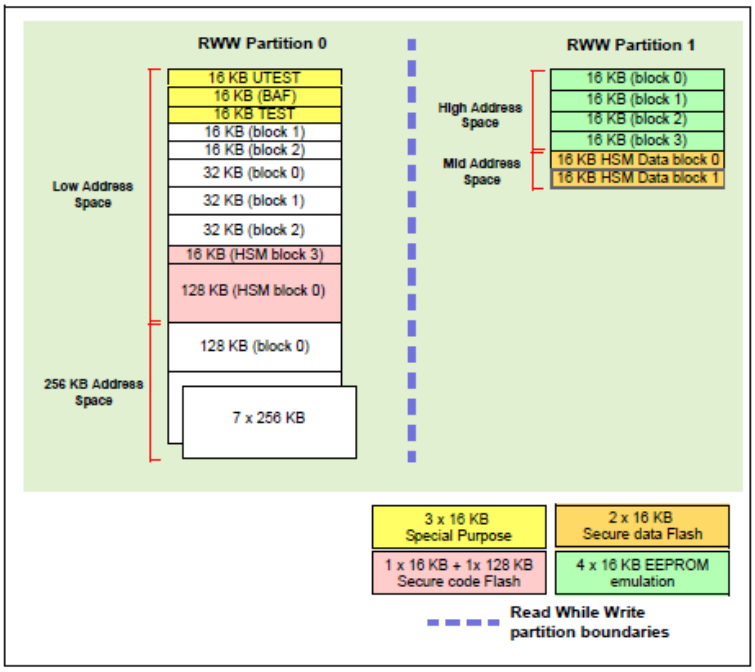
HSM \ Host		Data Flash		Program Flash	
		Read	Write	Read	Write
Data Flash	Read	Permitted	Permitted	Permitted	Permitted
	Write	Permitted	Permitted (*)	Permitted	Permitted
Program Flash	Read	Permitted	Permitted	Permitted	Permitted (**)
	Write	Permitted	Permitted	Permitted (**)	Permitted (*)

Where:

- (*) in parallel the HSM can write its code/data sectors and the HOST can write its code/data sectors. The hardware - however - serializes the operations;
- (**) permitted only in case of different Partitions (0 and 1).

4.5 SPC584Bx: RWW partitions

Figure 11. Flash memory segmentatiion and read-while-write partitioning



Only two RWW partitions are implemented on SPC584Bx, where:

- Partition 0 contains Host Code and HSM blocks
- Partition 1 contains Host Data and HSM data blocks

This partitioning allows following RWW accesses among Host (core) and HSM:

Figure 12. RWW accesses

HSM \ Host		Data Flash		Program Flash	
		Read	Write	Read	Write
Data Flash	Read	Permitted	Forbidden	Permitted	Permitted
	Write	Forbidden	Permitted (*)	Permitted	Permitted
Program Flash	Read	Permitted	Permitted	Permitted	Forbidden
	Write	Permitted	Permitted	Forbidden	Permitted (*)

Where:

- (*) in parallel the HSM can write its code/data sectors and the HOST can write its code/data sectors. The hardware - however - serializes the operations.

4.6 SPC584Cx/SPC58ECx vs SPC584Bx: RWW partitions

Migrating from SPC584Cx/SPC58ECx to SPC584Bx, the following accesses become forbidden:

- HSM and HOST accesses in RWW to their CFLASH blocks
- HSM and HOST accesses in RWW to their DFLASH blocks

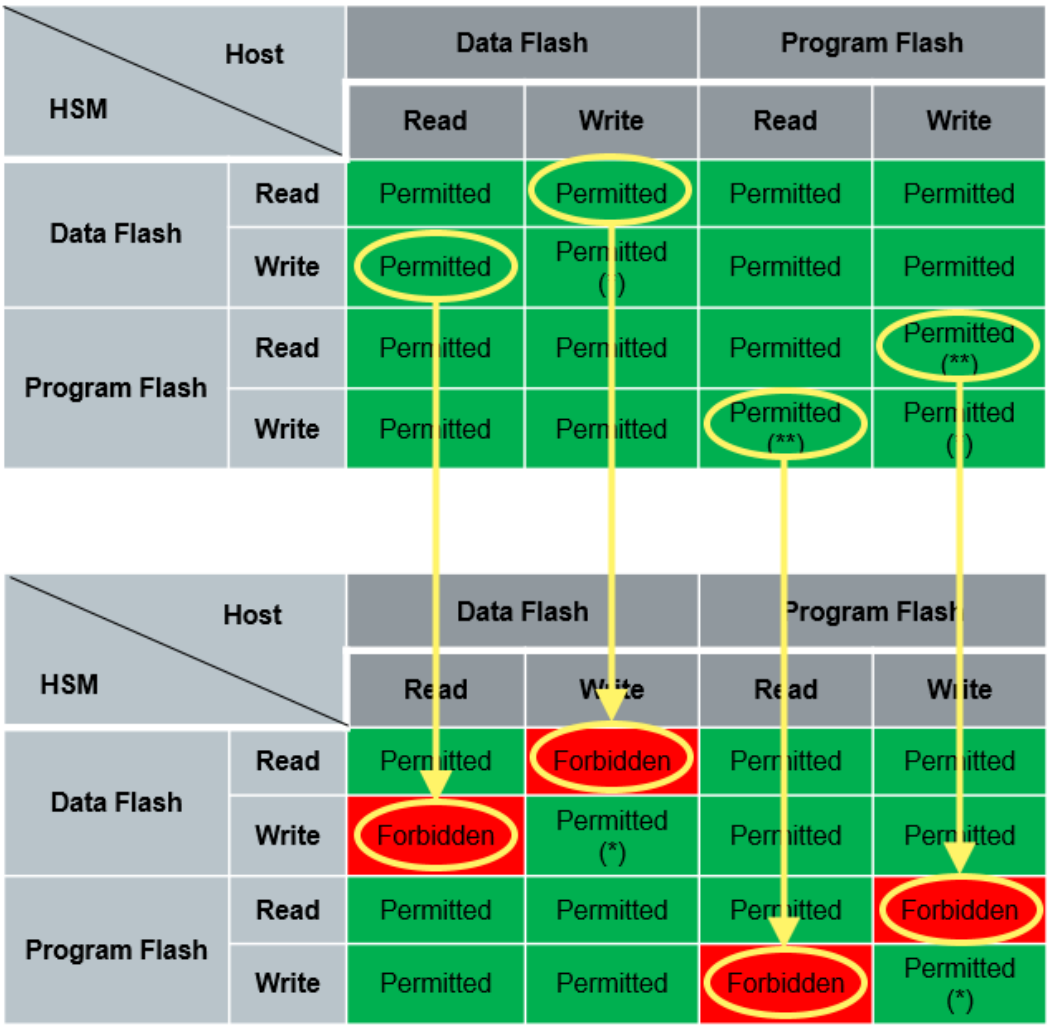
Concurrent access to the Data sectors triggers an exception:

- HOST program its Data Sector
- HSM reads its Data sector (or vice versa)
  - The HSM software jump to an exception

Concurrent access to the Code sectors triggers an exception:

- HOST program its Code Sector
- HSM reads its Code sector (or vice versa)
  - The HSM software jump to an exception

Figure 13. RWW partitions



On SPC584Bx, these limitations request a specific SW handling to manage C-DFlash access in RWW.

4.7 SPC584Bx: RWW partitions – sw proposal

The requirement is that HSM shall recover from a flash high voltage operation: this means that HSM has to execute the same instruction before the RWW event.

The Idea is that:

- exception handlers in RAM
- HSM waits until the high voltage operation in flash ends in the exception handler
- Afterwards, HSM jumps to the instruction that triggered the exception

With the following limitations:

- HSM can’t access the main interface of the flash
- No register to invalidate the Mini-cache of the flash
- IVOR1 is not recoverable

Current status is that ST SHE FW implements the workaround for the HSM code sector.

Also, in order to avoid eventual RWW exceptions generation a handshake protocol could be implemented between HSM side and HOST side.

The ST HSM Bootloader code has been designed implementing an handshake protocol using the HSM to Host interface register to avoid RWW exception between HSM and HOST/BAF code.

For further details, please contact an ST representative.

5 Peripherals

In the following table the main differences in terms of IPs are reported: most of them are identical and some have different number of instances.

Figure 14. IPs differences

	Commercial Code	SPC584Cx / SPC58ECx		SPC584Bx
		Reference device	Comparison vs CHO4M	
	Item	Feature		Feature
System	DMA	1x 64ch		1x 32ch
	STM	2x STM		1x STM
Communication I/F	LIN	18x LINFLex		14x LINFLex
	FlexRay	Dual ch (10MB/s, 64buffers)		-
	DSPI	8x DSPI		7x DSPI
ADC	SAR-ADC (12bit)	96ch (3x 12-bit /1x 12-bit supervisor / 1x 10-bit STBY)		63ch (2x 12-bit /1x 12-bit supervisor / 1x 10-bit STBY)

Regarding the ADC, one instance (SARADC_12bit_3) has been removed and the number of channels reduced:

Figure 15. ADC comparison

Converter Type	12-bit SAR ADC				10-bit SAR ADC
Special Function	Supervisor SAR ADC	Fast SAR ADC			STDBY & Fast Comparator
Name	SAR_ADC_12bit_SUPERVISOR (SAR_ADC_B)	SAR_ADC_12bit_0	SAR_ADC_12bit_1	SAR_ADC_12bit_3	SAR_ADC_10bit_STDBY
Number of internal channels(1)	95	16	16	16	24

ADC removed

SPC584Cx/SPC58ECx

1. This is the maximum number of available channels per dedicated silicon but the available number of channels per package might be different (refer to the IO_Definition document)

Converter Type	12-bit SAR ADC			10-bit SAR ADC
Special Function	Supervisor SAR ADC	Fast SAR ADC		STDBY & Fast Comparator
Name	SAR_ADC_12bit_SUPERVISOR (SAR_ADC_B)	SAR_ADC_12bit_0	SAR_ADC_12bit_1	SAR_ADC_10bit_STDBY
Number of internal channels(1)	63	11	11	9

SPC584Bx

1. This is the maximum number of available channels per dedicated silicon but the available number of channels per package might be different (see the IO_Definition document)

Number of channels reduced

Then, consider that following SPC584Cx/SPC58ECx IPs are not implemented on SPC584Bx:

- SEMA42
- FLEXRAY_0

5.1 IPs instances

The following table shows which SPC584Cx/SPC58ECx instances are missing on SPC584Bx.

Figure 16. IPs instances

	SPC584Cx / SPC58ECx	SPC584Bx
IPs	**Instances**	**Missing Instances**
LINFlexD_x	0-17	13, 14, 16, 17
DSPI_x	0-7	7
SAR_ADC_x	12bit_0,1,3, B0 10bit_STDBY	12bit_3
DMAMUX_x	0-3	2,3
SWT_x	0-2	0
STM_x	0-1	0

6 Clocking

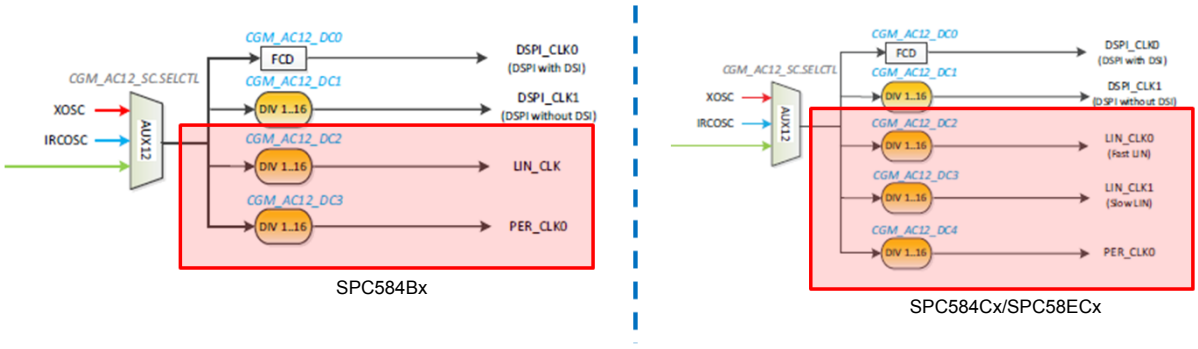
Clocking tree is common among SPC584Bx and SPC584Cx/SPC58ECx in terms of branches and registers except for the following two points:

1. On SPC584Cx/SPC58ECx there are two kinds of LINFLexD instances: fast (25Mbaud for 0/1/2/3/4/5/6/14/15/16/17) and slow (20Mbaud for 7/8/9/10/11/12/13).

   While, on SPC584Bx, only the slow ones are implemented.

   So, there are two clock branches (one for each type) on SPC584Cx/SPC58ECx and just one for SPC584Bx.
2. As a consequence, PER_CLK0 will change its branch (from AC12_DC3 to AC12_DC4) on SPC584Cx/SPC58ECx.

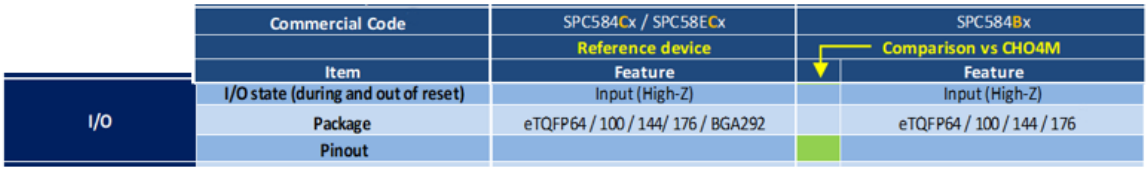
Figure 17. Clocking



7 Pinout

7.1 Pinout comparison

Figure 18. **I/O comparison**



SPC584Bx pinout is a direct subset of SPC584Cx/SPC58ECx pinout.

The pinout comparison between SPC584Bx and SPC584Cx/SPC58ECx is provided in the Excel file attached to this document.

This excel file shows:

- how the pads are mapped in both devices

Figure 19. **I/O mapping**

PIN	PAD SPC584Bx QFP100	PAD SPC58xCx QFP100	PORT SPC584Bx QFP100	PORT SPC58xCx QFP100
1	PAD[62]	PAD[62]	PD[14]	PD[14]
2	PAD[63]	PAD[63]	PD[15]	PD[15]
3	PAD[41]	PAD[41]	PC[9]	PC[9]
4	PAD[40]	PAD[40]	PC[8]	PC[8]

- the common alternate functions, the ones only available on SPC584Bx and the ones only available on SPC584Cx/SPC58ECx

Figure 20. **AF comparison**

PIN			PORT SPC584Bx QFP144	PORT SPC58xCx QFP144		COMMON AF	AF ONLY ON SPC584Bx QFP144	AF ONLY ON SPC58xCx QFP144
1			PD[14]	PD[14]		SIUL GPIO62 (i/o) DSPI 3 CS1 (o) DSPI 6 SOUT (o) LIN 6 TXD (o) DSPI 6 SIN (i) Ethernet 0 ETH_RDATA0 (i)	 CAN 0 sys0 TX (o) eMIOS 1 UC0 (i/o) eMIOS 1 UC0 (i)	CAN 0 sys0 TX (o) LIN 2 TXD (o) eMIOS 1 UC0 (i/o) LIN 2 RXD (i) DSPI 3 SIN (i) DSPI 5 SIN (i) eMIOS 1 UC0 (i)

- the Common Internal Source and the ones only available on SPC584Cx/SPC58ECx

Figure 21. **Internal source comparison**

DESTINATION PORT	COMMON INTERNAL SOURCES	SPC584Bx ONLY INTERNAL SOURCES	SPC584Cx/SPC58ECx ONLY INTERNAL SOURCES
	PIT 0 PIT_TRIGGER0		
Ethernet 0 ETH_TS_TRIG1	STM 0 STM2_INT0		STM 0 INT0

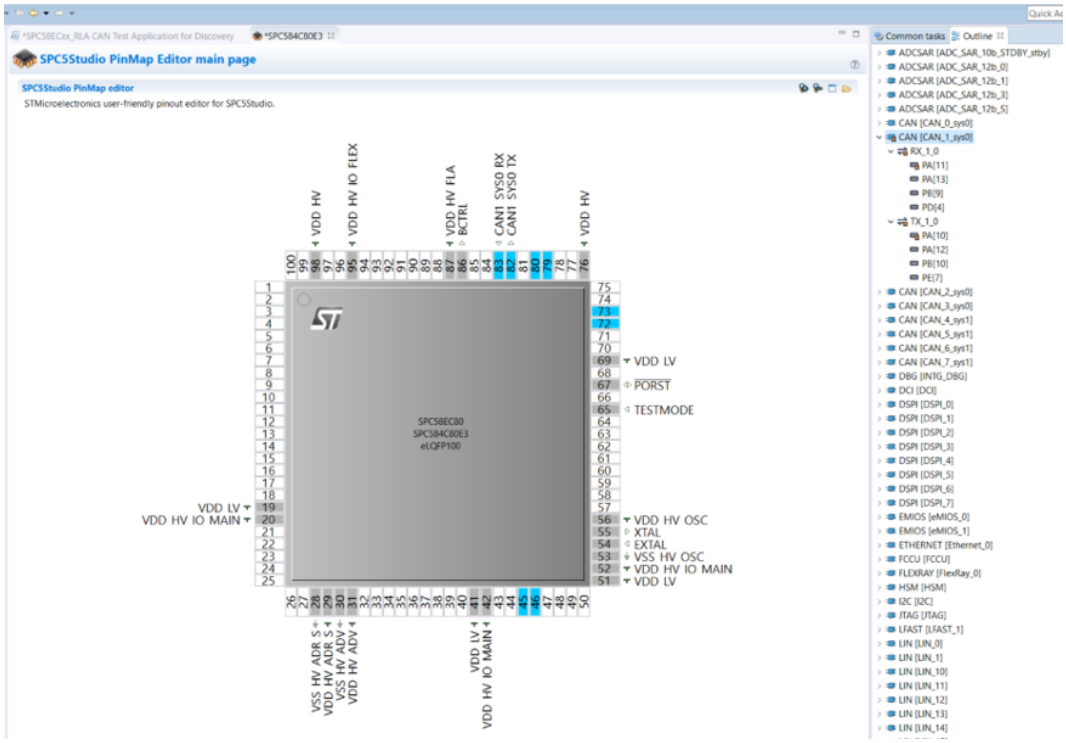
7.2 Pinout configuration

SPC5Studio tool provides a graphical user-friendly method for pin configuration.

As showed in the following picture, it is possible to check the pads related to a specific peripheral.

Selecting, for instance, the CAN1_sys0 on the right column, it will be showed in the package the related RX and TX pads.

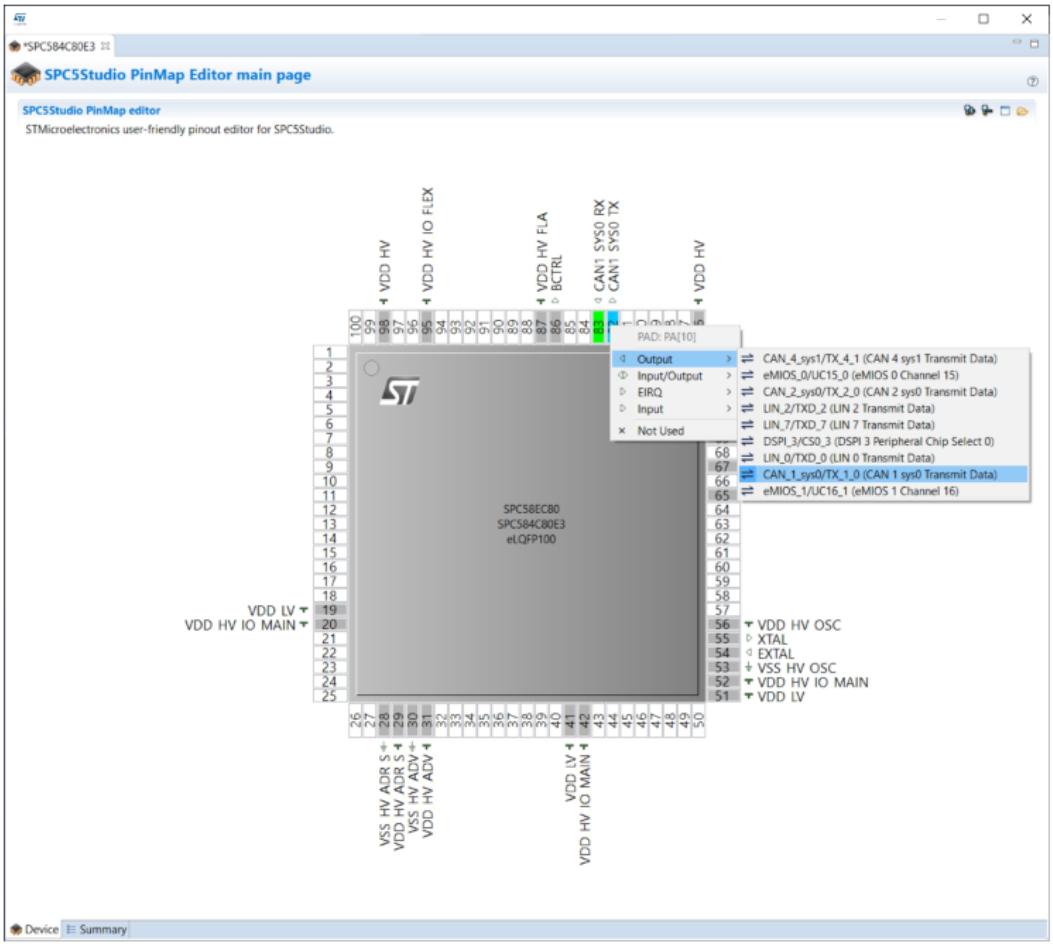
Figure 22. PinMap editor - IPs



On the other hand, SPC5Studio tool allows also to configure an alternate function for a specific pad.

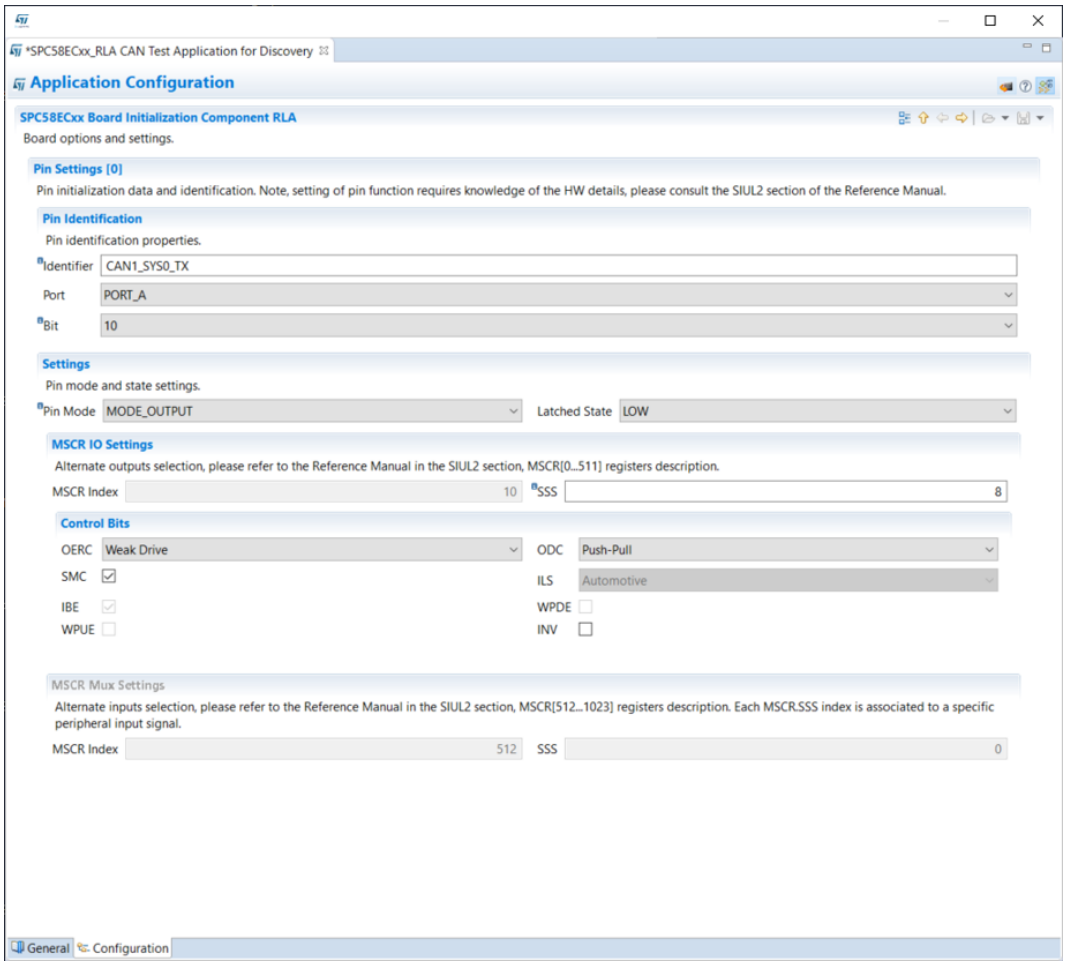
In the following picture, selecting the pin 82, user can choose among all the output features (CAN1_sys0/TX_1_0, sMIOS1/UC16_1, …)

Figure 23. **PinMap editor - pins**



In this case, the pin can be fully configured through the following window where all the SIUL2_MSCRx fields (OERC,SMC,IBE,…) could be specified.

Figure 24. **Pads configuration**



7.3 Features over packages

The following table shows an overview of the device features over all the packages.

Figure 25. Features packages

Line	Line Code	Core PowerPC	Clock freq. (MHz)	FLASH (KB)		RAM (KB) system& local + instruction	Package	GPIOs	Connectivity								Timers eMIOS 16bit	ADC		Security	Safety
				Code	Data				SPI	LIN	CAN-FD	I2C	FlexRay	Ethernet	SD/SDIO/e MMC	OSPI		Channels	Resolution		
C Line	SPC58EC SPC584C	2 x z4	180/ 160/ 120	4096	128 (4 x 32)	512	FPBGA292	215	8	16	8	1	1	1	-	-	64	95	1 x 10 bit 4 x 12 bit	HSM Evita Medium	ASIL-B
		1 x z4				384	eLQFP176	138	8	16	8	1	1	1	-	-	64	63			
		2 x z4		3072		416	eTQFP144	108	8	16	8	1	1	1	-	-	64	49			
		1 x z4				320	eTQFP100	68	8	14	8	1	1	1	-	-	61	32			
		2 x z4		2048		320	eTQFP64	35	5	10	8	1	-	-	-	-	35	18			
		1 x z4				256															
4B Line	SPC584B	1 x z4	120/ 80/ 64	2048	64 (4 x 16)	192	eLQFP176	151	7	14	8	1	-	1	-	-	64	63	1 x 10 bit 3 x 12 bit	HSM Evita Medium	ASIL-B
				1536		160	eTQFP144	119	7	14	8	1	-	1	-	-	63	49			
							eTQFP100	75	7	13	8	1	-	1	-	-	58	32			
				1024		128	eTQFP64	40	5	8	8	1	-	-	-	-	35	18			

7.4 Pad-keeper configurability

LP (Low Power) pads are the only ones active during STANDBY. When Standby mode is entered, the Pad-Keeper feature is activated for them, than means: if the pad status is high, the weak pull-up resistor is automatically enabled; if the pad status is low, the weak pull-down resistor is automatically enabled.

Unlike the device SPC584Cx/SPC58ECx cut1.1 where this feature cannot be disabled, in the SPC584Bx cut1.2 devices,Pad-Keeper can be disabled on the following 6 WKUP pads: PC1, PD5, PA2, PA11, PE10, PF3.

Please, refer to AN5484 "SPC58x - Configurable PAD - Keeper feature" for more details.

8 Power supply

8.1 Power management regulators

Figure 26. **Power management comparison**

Device	External regulator	Internal SMPS regulator	Internal linear regulator external ballast	Internal linear regulator internal ballast	Auxiliary regulator	Clamp regulator	Internal standby regulator(1)
SPC584Cx SPC58ECx	—	—	X	X(2)	X	X	X
SPC584Bx	—	—	X (3)	X	X	X	X

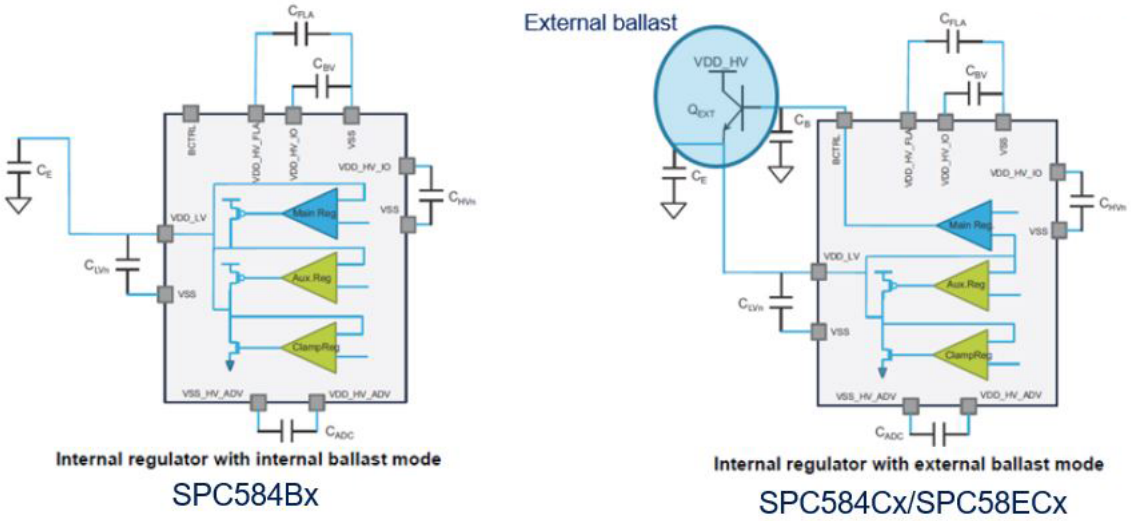
1. Standby regulator is automatically activated when the device enters standby mode.
2. The operability of the device with internal ballast can be limited by the maximum thermal dissipation of the device in the application. The internal ballast option is available only on specific devices, please contact the local sales.
3. For compatibility purpose with SPC584Cx/SPC58ECx, or for the optimization of the power dissipation, the operability of the device with external ballast can be used. The external ballast option is available only on specific devices, contact the local sales.

Where:

- SPC584Cx/SPC58ECx needs an external NPN bipolar as the ballast device (used to reduce the power that device should dissipate);
- SPC584Bx uses internal ballast transistor;
- Different configuration (2,3) available only through agreements with ST sales.

8.2 Power management configurations

Figure 27. **Power management configurations**



In case of migration from SPC584Cx/SPC58ECx to SPC584Bx, current consumption and thermal dissipation should be well evaluated.

Regarding Base Control (BCTRL), it is bonded on all SPC584Bx packages and its pinout compatibility is maintained vs SPC584Cx/SPC58ECx packages, as showed here below:

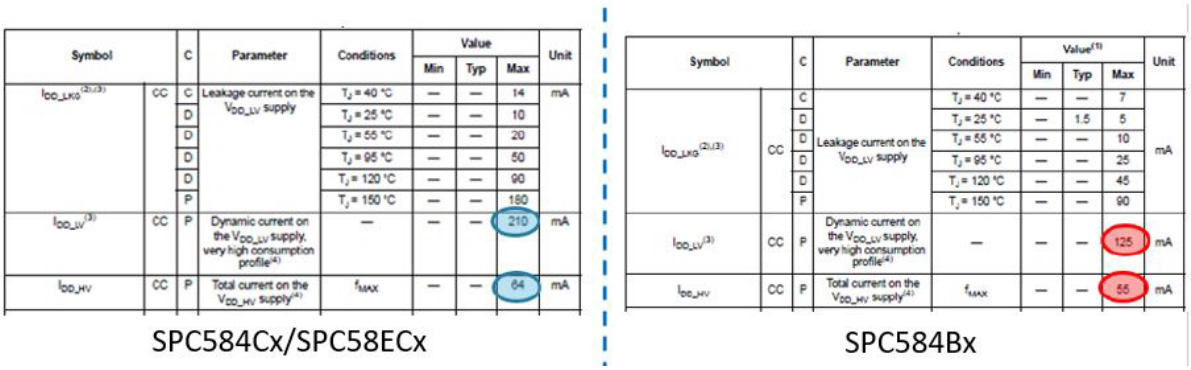
Figure 28. **BCTRL mapping**

PIN		PAD SPC584Bx QFP100	PAD SPC584Cx/SPC58ECx QFP100
86		BCTRL	BCTRL

9 Power consumption

9.1 Running mode consumption

Figure 29. Running consumption comparison



Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{DD_LKG}[2][3]	CC	C	Leakage current on the V_{DD_LV} supply	T_J = 40 °C	—	—	14	mA
		D		T_J = 25 °C	—	—	10	
		D		T_J = 55 °C	—	—	20	
		D		T_J = 95 °C	—	—	50	
		D		T_J = 120 °C	—	—	90	
		P		T_J = 150 °C	—	—	180	
I_{DD_LV}[3]	CC	P	Dynamic current on the V_{DD_LV} supply, very high consumption profile[4]	—	—	—	210	mA
I_{DD_HV}	CC	P	Total current on the V_{DD_HV} supply[4]	f_{MAX}	—	—	64	mA

SPC584Cx/SPC58ECx

Symbol		C	Parameter	Conditions	Value[1]			Unit
					Min	Typ	Max	
I_{DD_LKG}[2][3]	CC	C	Leakage current on the V_{DD_LV} supply	T_J = 40 °C	—	—	7	mA
		D		T_J = 25 °C	—	1.5	5	
		D		T_J = 55 °C	—	—	10	
		D		T_J = 95 °C	—	—	25	
		D		T_J = 120 °C	—	—	45	
		P		T_J = 150 °C	—	—	90	
I_{DD_LV}[3]	CC	P	Dynamic current on the V_{DD_LV} supply, very high consumption profile[4]	—	—	—	125	mA
I_{DD_HV}	CC	P	Total current on the V_{DD_HV} supply[4]	f_{MAX}	—	—	55	mA

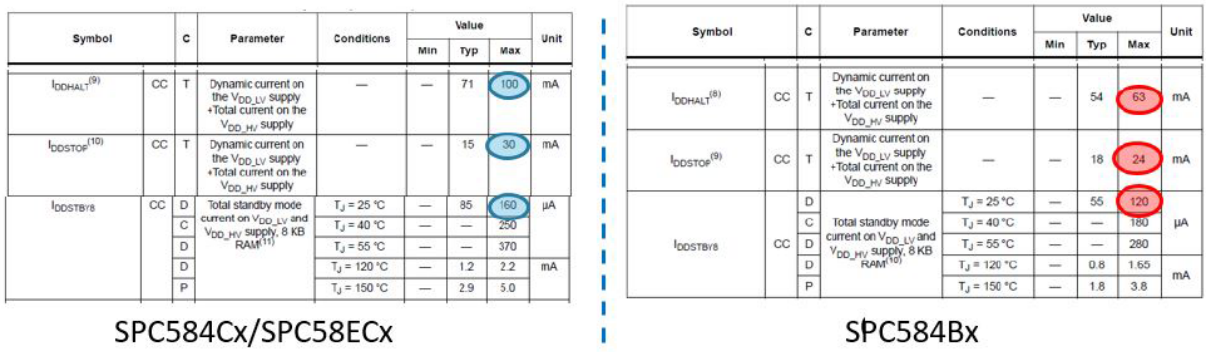
SPC584Bx

The picture (taken from respective DSs) is related to worst case consumption for both devices that have the following consumptions/configurations:

- SPC584Cx/SPC58ECx:
  - Consumption: IDD_LV=210mA, IDD_HV=64mA
  - Configuration: 2 x e200Z4 @ 180 MHz, HSM @ 90 MHz, all IPs clock enabled, Flash access with prefetch disabled, Flash consumption includes parallel read and program/erase, all SARADC in continuous conversion, DMA continuously triggered by ADC conversion, 4 DSPI / 8 CAN / 2 LINFlex and 2 DSPI transmitting, 2 x EMIOS running (8 channels in OPWMT mode), FIRC, SIRC, FXOSC, PLL0-1 running. The switching activity estimated for dynamic consumption does not include I/O toggling, which is highly dependent on the application.
- SPC584Bx:
  - Consumption: IDD_LV=125mA, IDD_HV=55mA
  - Configuration: 1 x e200Z4 @ 120 MHz, HSM @ 60 MHz, all IPs clock enabled, Flash access with prefetch disabled, Flash consumption includes parallel read and program/erase, all SARADC in continuous conversion, DMA continuously triggered by ADC conversion, 2 DSPI / 8 CAN / 2 LINFlex transmitting, RTC and STM running, 1 x EMIOS running (4 channels in OPWMT mode), FIRC, SIRC, FXOSC, PLL0-1 running.

9.2 Low power mode consumption

Figure 30. Low power consumption comparison



Symbol	C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
I_{DDHALT}[9]	CC T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	71	100	mA
I_{DDSTOP}[10]	CC T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	15	30	mA
$I_{DDSTBY8}$	CC D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 8 KB RAM[11]	T_J = 25 °C	—	85	160	µA
	C		T_J = 40 °C	—	—	250	
	D		T_J = 55 °C	—	—	370	
	D		T_J = 120 °C	—	1.2	2.2	mA
	P		T_J = 150 °C	—	2.9	5.0	

SPC584Cx/SPC58ECx

Symbol	C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
I_{DDHALT}[8]	CC T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	54	63	mA
I_{DDSTOP}[9]	CC T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	18	24	mA
$I_{DDSTBY8}$	CC D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 8 KB RAM[10]	T_J = 25 °C	—	55	120	µA
	C		T_J = 40 °C	—	—	180	
	D		T_J = 55 °C	—	—	280	
	D		T_J = 120 °C	—	0.8	1.65	mA
	P		T_J = 150 °C	—	1.8	3.8	

SPC584Bx

The picture (taken from respective DSs) is related to Low Power Modes (HALT/STOP/STANDBY) max consumption for both devices that have the following consumptions:

- IDD_HALT → SPC584Cx/SPC58ECx: 100 mA, SPC584Bx: 63 mA
- IDD_STOP → SPC584Cx/SPC58ECx: 30 mA, SPC584Bx: 24 mA
- IDD_STANDBY → SPC584Cx/SPC58ECx: 160 µA, SPC584Bx: 120 µA

Appendix A Reference documents

Table 3. **Reference documents**

Doc Name	ID	Title
AN5484	034218	SPC58x - Configurable PAD - Keeper feature

Revision history

Table 4. **Document revision history**

Date	Version	Changes
17-Dec-2019	1	Initial release.
01-Dec-2020	2	Added: • Section 5.1 IPs instances • Section 6 Clocking • Section 7.1 Pinout comparison • Section 7.2 Pinout configuration • Section 7.3 Features over packages • Section 7.4 Pad-keeper configurability • Section Appendix A Reference documents Minor text changes in Minor text changes in Section 5 Peripherals.
31-Mar-2021	3	Confidentiality level changed from Restricted to Public. Minor text changes.
19-May-2022	4	Add a new file excel in attach. Updated Section 7.1 Pinout comparison

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