Getting started with STM32MP23/25xx MPUs hardware development

Introduction

This application note shows how to use the STM32MP23/25xx lines (MPUs). It describes the minimum hardware resources required to develop an application based on these products.

This document provides an overview of the hardware implementation of the development board, with focus on features like:

- Power supply
- Package selection
- Clock management
- Reset control
- Boot mode settings
- Debug management

Reference design schematics are also included in this application note. They show a description of the main components, interfaces, and modes.

Table 1. Applicable products

Type	Products
Microprocessor	STM32MP257F, STM32MP257D, STM32MP257C, STM32MP257A STM32MP255F, STM32MP255D, STM32MP255C, STM32MP255A STM32MP253F, STM32MP253D, STM32MP253C, STM32MP253A STM32MP251F, STM32MP251D,STM32MP251C, STM32MP251A STM32MP235F, STM32MP235D, STM32MP235C, STM32MP235A STM32MP233F, STM32MP233D, STM32MP233C, STM32MP233A STM32MP231F, STM32MP231D, STM32MP231C, STM32MP231A

1 General information

This document applies to the STM32MP23/25xx lines, Arm®-based MPUs.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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Table 2. Reference documents

N°	Reference	Title
[1]	AN2867	Oscillator design guide for STMicroelectronics microcontrollers
[2]	AN1709	EMC design guide for STMicroelectronics microcontrollers
[3]	AN5275	USB DFU/USART protocols used in STM32MP1 series bootloaders
[4]	AN5723	Guidelines for DDR configuration on STM32MP2 MPUs
[5]	AN5725	How to use STPMIC2x for hardware and software integration on STM32MP2 MPUs
[6]	AN5724	Guidelines for DDR memory routing on STM32MP2 MPUs
[7]	AN5727	How to use STPMIC2x for a wall adapter powered application on STM32MP25 MPUs
[8]	UM3359	Evaluation board with STM32MP257F MPU
[9]	UM3385	Discovery kit with STM32MP257F MPU
[10]	RM0457	STM32MP23/25xx advanced Arm®-based 64/32-bit MPUs
[11]	DS14285	STM32MP25xA/D datasheet
[12]	DS14284	STM32MP25xC/F datasheet
[13]	DS14634	STM32MP23xC/F datasheet
[14]	DS14635	STM32MP23xA/D datasheet
[15]	AN4879	Introduction to USB hardware and PCB guidelines using STM32 MCUs
[16]	AN5728	How to use STPMIC2x for a battery powered application on STM32MP25 MPUs

Table 3. Glossary

Term	Meaning
ADC	Analog-to-digital converter
AHB	Advanced high-performance bus
AXI	Advanced extensible interface bus. By extension, the interconnect matrix based on AXI
AXIM	AXI matrix. AXI based interconnect
BKPSRAM	Backup SRAM
BSEC	Boot and security controller. OTP interface
CA35	Cortex-A35
CM33	Cortex-M33
CNT	Generic timer (inside Cortex-A)
CRYP	Cryptographic IP. Supporting DES, Triple-DES and AES
CSI	Camera serial interface
CTI	Cross-trigger interface
DAP	Debug access port
DCMI	Digital camera interface. Parallel interface
DDRCTRL	Double data rate SDRAM controller

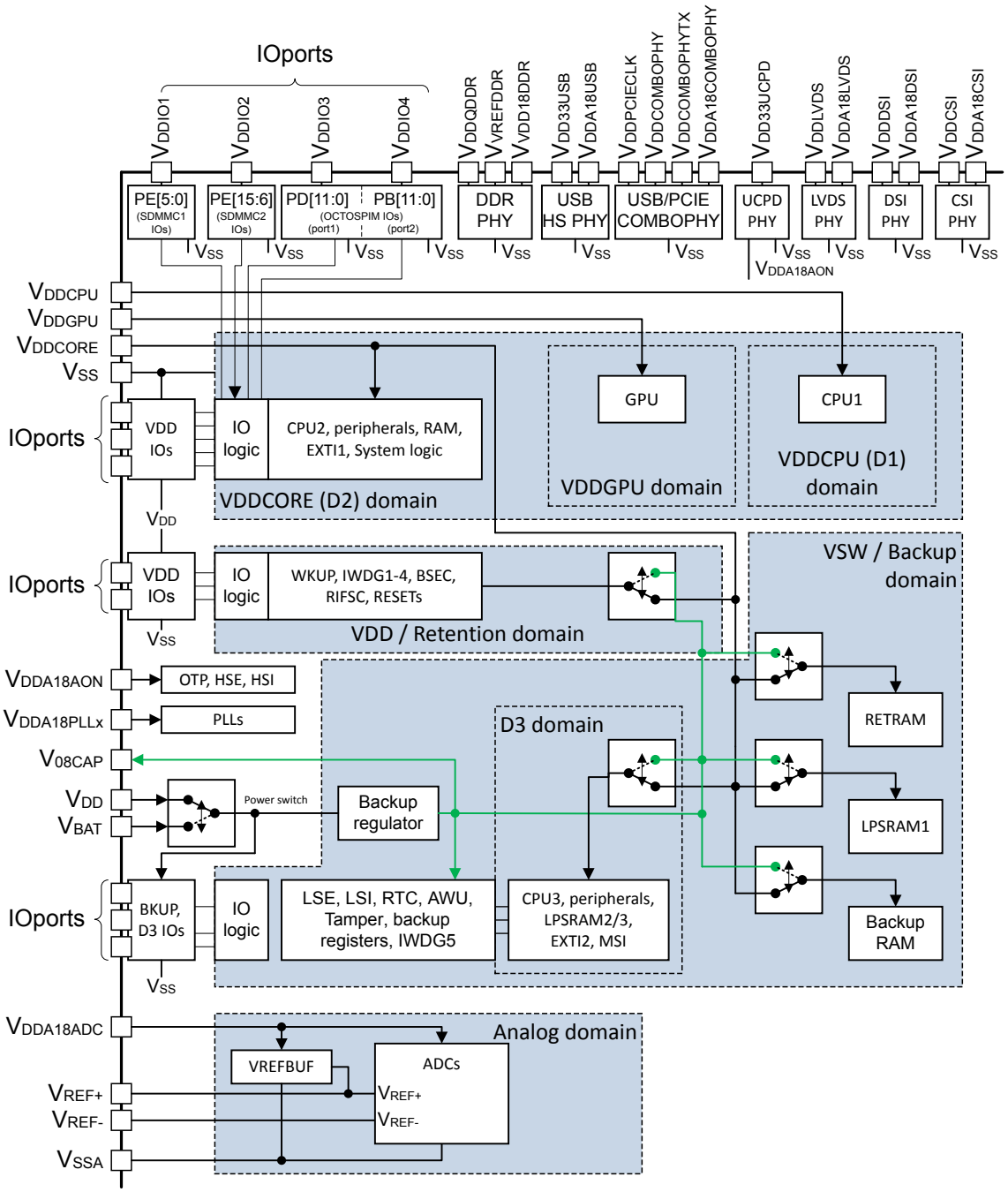
Term	Meaning
DDRPERFM	DDR performance monitor, linked to DDRCTRL
DLYBQS	Delay block for QUASDPI. Compensate external signals timings to reach highest data rates
DLYBSD	Delay block for SDMMC. Compensate external signals timings to reach highest data rates
DMA	Direct memory access. Bus master able to autonomously transfer data between peripheral and memory or between memories
DMAMUX	DMA request multiplexor
DSI	Display serial interface master
ETH	Ethernet controller
ETM	Embedded trace module
EXTI	Extended interrupt and event controller
FDCAN	Controller area network with flexible data-rate. Could also support time triggered CAN (TT)
FMC	Flexible memory controller
GIC	Generic interrupt controller
GMAC	Gigabit Ethernet media access controller
GPIO	General-purpose input/output
GPU	Graphic processing unit
HASH	Cryptographic hash block. Supporting secure hash algorithm (SHA),
HDMI	High definition multimedia interface
HDP	Hardware debug port
HSE	High-speed external crystal oscillator
HSEM	Hardware semaphore. Helps multiprocessor resources sharing
HSI	High-speed internal oscillator
I²C	Inter IC bus
I3C	Improved I²C
I2S	Inter IC sound
IPCC	Inter-processor communication controller
IWDG	Independent watchdog
JTAG	Joint test action group. A debug interface
LCD	Liquid crystal display
LPTIM	Low-power timer
LSE	Low-speed external crystal oscillator
LSI	Low-speed internal oscillator
LVDS	Low voltage differential signaling, by extension a display interface based on this.
MSI	Multispeed internal oscillator
OCTOSPI	Octal data serial peripheral interface
OCTOSPIM	OCTOSPI IO manager
LTDC	LDC TFT display controller
MDMA	Master direct memory access
MLAHB	Multilayer AHB. AHB based interconnect
NVIC	Nested vectored interrupt controller (inside Cortex-M4)
OTP	One time program memory
PCB	Printed circuit board

Term	Meaning
PCIE	Peripheral component interconnect express
PHY	A mixed-signal physical interface. Generally, it enables adapting the internal logical level to a specific interface standard
PMB	Process monitor block
PMIC	Power management integrated circuit. It is an external circuit that provides various platform power supplies with large controllability through signals and serial interface
PTH	Plated through hole. It is a drilled hole with conductive wall using, for example, a layer of deposited copper.
PWR	Power control
RCC	Reset and clock control
RETRAM	Retention SRAM
RNG	Random number generator
ROM	Read only memory
RTC	Real-time clock
SAI	Serial audio interface
SDMMC	Secure digital and multimedia card interface. Supports SD, MMC, eMMC, and SDIO protocols
SMPS	Switched-mode power supply
SPDIF	Sony/Philips digital interface format
SPI	Serial peripheral interface
SRAM	Static random access memory
STGEN	System timing generation. Used for Cortex-A7 timers
STGENC	STGEN control. Secure part of STGEN
STGENR	STGEN read. Read-only part of STGEN
STM	System trace macrocell
SW	Software
SWD	Serial wire debug
SWO	Single wire output. A trace port
SYSCFG	System configuration
SYSRAM	System SRAM
SYSTICK	System tick timer (inside Cortex-M4)
TAMP	Tamper detection IP
TFT	Thin film transistor. An LCD technology process
TIM	Timer
TSGEN	Debug time stamp generator. Used to ensure multiple core trace synchronizations
UART	Universal asynchronous receiver transmitter
UCPD	USB Type-C® power delivery controller
USART	Universal synchronous/asynchronous receiver/transmitter
USB	Universal serial bus
USB3DR	USB 3.0 dual role controller
USBH	USB host controller
USB hi-speed	USB 2.0 at 480 Mbit/s half-duplex
USB SuperSpeed	USB 3.0 at 5 Gbit/s full-duplex

Term	Meaning
USBPHYC	USB physical interface control
VREFBUF	ADC voltage reference buffer
WWDG	Window watchDog

2 Power supplies

Figure 1. **Power supply scheme**



DT68353V3

2.1 Overview

Note: See details and guaranteed operating points in the product datasheets.
Values in this section are for information only.

- The main I/Os voltage supply (V_{DD}) range is either 1.8 V or 3.3 V typ. There are as well dedicated independent I/Os supplies for some interfaces (V_{DDIO1}, V_{DDIO2}, VDDIO3, and V_{DDIO4}).
- There are multiple analog and digital logic voltage supplies, see Section 2.2: Power supply schemes for details.
- The real-time clock (RTC) and backup registers can be powered from the V_{BAT} voltage when the main V_{DD} supply is powered off. This internal supply with automatic switch between V_{BAT} and V_{DD} is named V_{SW} domain and is also used to supply PI8, PC13, PZ0 to PZ5 pins, and, only for TAMP_IN usage, the PC3, PC4, PC5, PF6, PF7, PG1, PG3, and PZ6 pins.
  V_{BAT} voltage is typically 3 V when used with a coin-cell battery.

2.1.1 Independent ADC supply and reference voltage

To make sure that the conversion of signals is more accurate and can cover a wider range of values, the ADC (analog-to-digital converter) and reference have their own power supply that can be filtered separately. This helps to protect them from any interference or noise that may be present on the printed circuit board (PCB).

The analog operating voltage supply ($V_{DDA18ADC}$) is 1.8 V typ.

- The ADC/VREFBUF voltage supply input is available on a separate VDDA18ADC pin.
- An isolated supply ground connection is provided on the VSSA pin.
  In all cases, the VSSA pin must be externally connected to the same supply ground as the V_{SS}.

Warning: *The ADC_INx I/Os must not exceed VDDA18ADC + 0.3 V as specified in the product datasheet.*

External VREF

The user can connect a separate external reference voltage ADC input on VREF+. The voltage on VREF+ may range from 1.10 V to $V_{DDA18ADC}$.

Internal VREF

The user can enable in the VREFBUF block an internal reference voltage on VREF+.

The voltage on VREF+ can be either 1.21 V or 1.5 V.

The VREF+ pin has an internal reference voltage (VREF) that can be used externally, such as for an analog comparator reference. However, it is important to make sure that the amount of electrical current being used stays within the values specified in the datasheet.

Caution: *When available (depending on package), VREF- must be externally tied to V_{SSA}.*

2.1.2 Battery backup

To retain the content of the backup registers, BKPSRAM and RETRAM, when V_{DD} is turned off, the VBAT pin can be connected to an optional standby voltage supplied by a battery or another source.

The VBAT pin also powers the RTC unit, allowing the RTC to operate even when the main digital supply (V_{DD}) is turned off. The switch to the V_{BAT} supply is controlled by the power down reset (PDR) circuitry embedded in the PWR.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.

2.2 Power supply schemes

Note: See details and guaranteed operating points in product datasheets. Values in this section are for information only.

The circuit is powered by multiple power supplies. Those supplies must be connected to external decoupling capacitors (see Table 4).

I/Os supplies

- The V_{DD} is the main supply for I/Os and an internal part, kept powered during the standby mode.
  - The voltage range is either 1.8 V or 3.3 V typ.
  - V_{DD} should be present whenever other I/Os supplies are present (except V_{BAT}, which is independent and $V_{DDA18AON}$, which is always present).
- V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, and V_{DDIO4} are separate/dedicated I/Os supplies.
  - Voltage ranges are either 1.8 V, 3.0 V, or 3.3 V typ.
  - Each of those supply could have different voltage or be shut down independently.
- The VBAT pin can be connected to the external battery.
  - The voltage range is 2.3 V to 3.6 V (except when connected to V_{DD}).
  - If the application does not support backup battery, it is recommended to connect this pin to V_{DD}.
  - If the application is supporting a backup battery, it is required to add a 2.2 µF capacitor and a resistor (to limit the voltage slew rate when a backup battery is plugged, as explain in Table 4 note 2).
- V_{DDQDDR} is the DDR I/O supply.
  - The voltage range is 1.283 V to 1.45 V for interfacing DDR3L memories (1.35 V typ.).
  - The voltage range is 1.14 V to 1.26 V for interfacing DDR4 memories (1.2 V typ.).
  - The voltage range is 1.06 V to 1.17 V for interfacing LPDDR4 memories (1.1 V typ.).

Digital logic supplies

- V_{DDCPU} digital CPU domain supply (Cortex-A35)
  - Could be shut down during the Run2, Stop2, LP-Stop2, LPLV-Stop2, Standby1, or Standby2 mode (using a PWR_CPU_ON signal).
  - The voltage range during run mode is 0.8 V typ. (0.91 V typ. in overdrive(1))
  - Dependent on V_{DD} supply, V_{DD} shall be present before V_{DDCPU}.
  - V_{DDCPU} could be reduced further in specific stop modes (LP-Stop1 or LPLV-Stop1). This involves either PWR_ON (for example with STPMIC25, external power management IC) or PWR_LP signal.
- The V_{DDCORE} is the main digital voltage.
  - V_{DDCSI}, V_{DDDSI}, V_{DDLVDS}, $V_{DDCOMBOPHY}$, $V_{DDCOMBOPHYTX}$, and $V_{DDPCIECLK}$ should usually be connected to V_{DDCORE}.
  - Could be shut down during the Standby1 or Standby2 mode (using a PWR_ON signal).
  - The voltage range during run mode is 0.82 V typical.
  - Dependent on V_{DD} supply. V_{DD} shall be present before V_{DDCORE}.
  - V_{DDCORE} could be reduced further in a specific stop mode (LPLV-Stop1 or LPLV-Stop2). This involves either PWR_ON (for example with STPMIC25, external power management IC) or PWR_LP signal.
- V_{DDGPU} digital GPU domain supply:
  - Could be shut down or reduced when a GPU is not used during run mode (for example, under SW control using I²C message to STPMIC25 or any other ways) or shutdown during any low power mode (for example, using PWR_ON signal to follow V_{DDCPU} control).
  - The voltage range during run mode is 0.8 V typ. (0.9 V typ. in overdrive(1)).
  - Dependent on V_{DD} supply, V_{DD} shall be present before V_{DDGPU}.

1. *Overdrive is only available on some part references. Overdrive affects maximum Tj and reliability data.*

1.8 V analog supplies

- $V_{DDA18AON}$ power supply input for system analog such as reset, power management, oscillators, and OTP, kept powered during the standby mode
  - The voltage range is 1.8 V typ.
- The $V_{DDA18ADC}$ pin is the analog (ADC/VREFBUF) supply.
  - The voltage range is 1.8 V typ.
  - Additional precautions can be taken to filter analog noise. $V_{DDA18ADC}$ could be connected to a shared 1.8 V supply through an inductor based filter.
  - The VREF+ pin can be connected to the $V_{DDA18ADC}$ external power supply. If a separate, internal, or external, reference voltage is applied on VREF+, a decoupling capacitor must be connected between this pin and VREF- (see Table 4).
    Refer to Section 2.1.1: Independent ADC supply and reference voltage.

Following supplies could be connected on a same source with independent decoupling whenever possible.

- The voltage range is 1.8 V typ.
- The VDDA18PLL1, VDDA18PLL2, and VDDA18PLL3 pins are the analog supply for PLLs.
- The VDDA18DDR pin is the analog supply for DDR PHY.
- The VDDA18DSI pin is the analog supply for DSI.
- The VDDA18CSI pin is the analog supply for CSI.
- The VDDA18LVDS pin is the analog supply for LVDS.
- The VDDA18COMBOPHY pin is the analog supply for COMBOPHY.
- The VDDA18USB pin is the analog supply for USB HS PHY.

3.3 V USB supplies

Should be connected on a same source with independent decoupling whenever possible.

- The voltage range is 3.3 V typ.
- $V_{DD33USB}$ is the USB high-speed PHY supply.
- $V_{DD33UCPD}$ is the USB Type-C® power delivery Common Criteria lines PHY supply.

Caution: *All supply grounds (V_{SS}, V_{SSA}, V_{SSAON}, and V_{REF-}) should be all connected to power planes.*

The following table must be used as a guideline only. Real count and values of capacitors could be adapted depending on various parameters: such as capacitor size and dielectric, PCB technology, product power integrity simulations.

Information in this table does not include capacitors on supplies sources (such as LDO or SMPS) or external devices (such as DDR memory, SD-Card, e.MMC, flash memories.)

Table 4. Amount of decoupling recommendation by package(1)(2)

Supplies pins	Decoupling point(3)	Value	VFBGA361 TFBGA361	VFBGA424	TFBGA436	Comments
VBAT	VSS	2.2 µF(4)(5)	1	1	1	Decoupling could be skipped if VBAT = VDD
V08CAP	VSS	4.7 µF(4)	1	1	1	Internal backup regulator decoupling
VDDCORE	VSS	1 µF(4)	6	8	6	-
VDDDSI, VDDLVDS, VDDCSI, VDDCOMBOPHY, VDDCOMBOPHYTX, VDDPCIECLK	VSS	100 nF	6	6	6	Supplies must be connected altogether and as well to VDDCORE.
VDDCPU	VSS	1 µF(4)	7	8	7	-
VDDGPU	VSS	1 µF(4)	7	8	6	-

Supplies pins	Decoupling point[3]	Value	VFBGA361 TFBGA361	VFBGA424	TFBGA436	Comments
VDDQDDR	VSS	1 µF[4]	5	5	8	-
VDDA18AON	VSSAON	100 nF	1	1	1	-
VDDA18PLL1/2/3, VDDA18DDR, VDDA18USB, VDDA18DSI, VDDA18LVDS, VDDA18CSI, VDDA18COMBOPHY	VSS	100 nF	7	7	7	Supplies must be connected altogether.
VDD	VSS	1 µF[4]	5	5	5	-
VDDIO1[6]	VSS	100 nF	1	1	1	Usually for SD-Card
VDDIO2[6]	VSS	100 nF	1	1	1	Usually for e.MMC
VDDIO3[6]	VSS	100 nF	1	1	1	usually for OCTOSPIM_P1
VDDIO4[6]	VSS	100 nF	1	1	1	usually for OCTOSPIM_P2
VDD33USB, VDD33UCPD	VSS	100 nF	1	1	1	Supplies must be connected altogether.
VDDA18ADC	VSSA	2.2 µF[4]	1	1	1	VSSA must be connected to VSS plane
		100 nF	1	1	1	
VREF+	VREF- & VSSA	1 µF[4]	1	1	1	VREF- must be connected to VSSA then VSS plane (chained connection)
		100 nF	1	1	1	

1. *This table should be used as a guideline only. Real count and values of capacitors could be adapted depending on various parameters: capacitor size and dielectric, PCB technology, product power integrity simulations, and so on.*
2. *Information in this table does not include capacitors on supplies sources (such as LDO or SMPS) or external devices (such as DDR memory, SD-Card, e.MMC, flash memories, and so on.)*
3. *All VSSx and VSSA must be connected to a common VSS plane.*
4. *Multilayer ceramic capacitor type (MLCC)*
5. *Fulfilling a minimum rise time defined in a datasheet might require a few ohms to be inserted in series. Total RC should be at least equal to Tr * battery voltage (for example, RC = 60µs for Tr = 20µs/V and 3V battery, which could be ensured by a 20 ohms series for a CR2032 battery type having 8-9 ohms minimum internal resistance). Rise time limitation could be as well ensured by a ferrite bead and a capacitor.*
6. *Must be connected to VDD if not used for dedicated interface supply.*

Note: See package feature details in Section 3.1: Package selection. Not all I/Os are supplied by VDD. See below the summary of related supplies.

Table 5. I/O power domains

Supply pin	Pin names
VDD	NRSTC1MS, PA0, PA1, PA10, PA11, PA12, PA13, PA14, PA15, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PB12, PB13, PB14, PB15, PC0, PC1, PC10, PC11, PC12, PC2, PC6, PC7, PC8, PC9, PD12, PD13, PD14, PD15, PF0, PF1, PF10, PF11, PF12, PF13, PF14, PF15, PF2, PF3, PF4, PF5, PF8, PF9, PG0, PG10, PG11, PG12, PG13, PG14, PG15, PG2, PG4, PG5, PG6, PG7, PG8, PG9, PH10, PH11, PH12, PH13, PH2, PH3, PH4, PH5, PH6, PH7, PH8, PH9, PI0, PI1, PI10, PI11, PI12, PI13, PI14, PI15, PI2, PI3, PI4, PI5, PI6, PI7, PI9, PJ0, PJ1, PJ10, PJ11, PJ12, PJ13, PJ14, PJ15, PJ2, PJ3, PJ4, PJ5, PJ6, PJ7, PJ8, PJ9, PK0, PK1, PK2, PK3, PK4, PK5, PK6, PK7, PWR_CPU_ON, PWR_LP, PWR_ON, PZ7, PZ8, PZ9
VDDIO1(1)	PE0, PE1, PE2, PE3, PE4, PE5
VDDIO2(2)	PE10, PE11, PE12, PE13, PE14, PE15, PE6, PE7, PE8, PE9
VDDIO3 (3)	PD0, PD1, PD10, PD11, PD2, PD3, PD4, PD5, PD6, PD7, PD8, PD9
VDDIO4(4)	PB0, PB1, PB10, PB11, PB2, PB3, PB4, PB5, PB6, PB7, PB8, PB9
VDDA18AON	OSC_IN, OSC_OUT, PDR_ON
VSW (5)	OSC32_IN, OSC32_OUT, PC13, PI8, PZ0, PZ1, PZ2, PZ3, PZ4, PZ5, PZ6
VDD/VSW(5) (6)	PC3, PC4, PC5, PF6, PF7, PG1, PG3

1. *Usually used for SD-Card using SDMMC1*
2. *Usually used for eMMC or SD-Card using SDMMC2*
3. *Usually used for OCTOSPIM_P1*
4. *Usually used for OCTOSPIM_P2*
5. *VSW is supplied by VBAT in the absence of VDD.*
6. *Pins with two supplies; VSW supply for enabled TAMP_INx additional function, VDD supply for GPIO and other alternate function*

Note: I/O power domain table does not include analog cells, which have one or more dedicated supplies (such as PHYs).

Table 6. Supply usage for unused features

Supply pin	Usual connection	Supply option if not used(1)	Pins or functions	Signals connection if not used	Related block
VDDDSI	VDDCORE	VSS	DSI_xxx pins	All open or all VSS	DSI
VDDA18DSI	Global 1.8V analog supply	VSS			
VDDLVDS	VDDCORE	VSS	LVDS_xxx pins	All open	LVDS
VDDA18LVDS	Global 1.8V analog supply	VSS			
VDDCSI	VDDCORE	VSS	CSI_xxx pins	All open or all VSS	CSI
VDDA18CSI	Global 1.8V analog supply	VSS			
VDDCOMBOPHY, VDDCOMBOPHYTX	VDDCORE	VSS	COMBOPHY_xx pins	COMBOPHY_RXxP/N to VSS. COMBOPHY_TXxP/N and COMBOPHY_REXT open	USB3DR SuperSpeed or PCIE
VDDA18COMBOPHY	Global 1.8V analog supply	VSS			
VDDPCIECLK	VDDCORE	VSS	PCIE_CLKxx pins	PCIE_CLKINP/N to VSS. PCIE_CLKOUTP/N open	PCIE
VDDGPU	Dedicated supply	VSS	GPU/NPU usage	-	GPU or NPU
VDDA18USB	Global 1.8V analog supply	VSS	USBH_HS_DP/DM pins and USB3DR_DP/DM pins	All DP/DM to VSS. All TXRTUNE open	USBH or USB3DR
VDD33USB	Dedicated 3.3V supply	VSS			
VDD33UCPD	Dedicated 3.3V supply	VSS	UCPD_CC1/CC2 pins	UCPD_CC1/CC2 open	UCPD
VDDA18ADC	Dedicated 1.8V supply or filtered global 1.8V analog supply	VSSA	ADC (internal and external channels)	-	ADC1 or ADC2 or ADC3
	-	-	ANA0/ANA1	VSSA	-
			VREF+ pin	VSSA	
			VREFBUF usage	-	VREFBUF

1. *Possible connection only when all related pins/functions are not used.*

2.3 Specific I/O constrains related to voltage settings

V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, and V_{DDIO4} have specific register settings and control sequences to be respected when used at 3 V/3.3 V or 1.8 V typ. Refer to the PWR section in the product reference manual for details.

See also Section 7.5: I/O speed settings for constrains on I/O speed settings for V_{DD}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, and V_{DDIO4} domains.

2.4 Reset and power supply supervisor

2.4.1 Power-on reset (POR)/power-down reset (PDR)

The device has an integrated POR/PDR circuitry that allows proper operation starting from 1.71 V.

The device remains in the Reset mode as long as V_{DD} and $V_{DD18AON}$ are below a specified threshold, and $V_{POR/PDR}$ is without the need for an external reset circuit. For more details concerning the power on/power down reset threshold, refer to the electrical characteristics in the product datasheets.

2.4.2 vddcore_ok reset

The system has an integrated circuitry that allows proper startup operation of the V_{DDCORE} (D2) domain.

The V_{DDCORE} domain remains in Reset mode when V_{DDCORE} is below the operation threshold vddcore_ok. Once the V_{DDCORE} supply level is above the operation threshold vddcore_ok, the V_{DDCORE} domain is taken out of reset. When the LVDS_D2 bit is set, the V_{DDCORE} supply level can be lowered in LPLV-Stop1 or LPLV-Stop2 modes.

For more details concerning the vddcore_ok reset threshold, refer to the electrical characteristics of the datasheet.

2.4.3 VDDCORE monitoring

The system has a detection circuitry, which detects if the V_{DDCORE} supply voltage is below or above the operating range. Detection is done by comparing the V_{DDCORE} with two thresholds (high and low thresholds).

VCOREH and VCOREL flags are available in the PWR control register 5 (PWR_CR5) to indicate if VDDCORE is higher or lower than the thresholds. The VCOREH and VCOREL are available on tamper signals but also connected to the EXTI2 and can generate an interrupt if enabled through the EXTI2 registers.

The detection is enabled by setting the VCOREMONEN bit in PWR control register 5 (PWR_CR5).

The VDDCORE voltage thresholds, when enabled, are not available in LPLV-Stop1, LPLV-Stop2, Standby1, Standby2, and V_{BAT} modes.

For more details concerning the vcore_thr_high and vcore_thr_low threshold, refer to the electrical characteristics of the datasheet.

2.4.4 vddcpu_ok reset

The system has an integrated circuitry that allows proper startup operation of the V_{DDCPU} (D1) domain.

The V_{DDCPU} domain remains in Reset mode when V_{DDCPU} is below the operation threshold vddcpu_ok. Once the V_{DDCPU} supply level is above the operation threshold vddcpu_ok, the V_{DDCPU} domain is taken out of reset. When the LVDS_D1 bit is set, the V_{DDCPU} supply level can be lowered in LPLV-Stop1 or LPLV-Stop2 mode. For more details concerning the vddcpu_ok reset threshold, refer to the electrical characteristics of the datasheet.

2.4.5 VDDCPU monitoring

The system has a detection circuitry, which detects if the V_{DDCPU} supply voltage is below or above the operating range. Detection is done by comparing the V_{DDCPU} with two thresholds (high and low thresholds). The level of the low threshold can be selected by the VCPULS bits in the PWR control Register 6 (PWR_CR6). The high level is fixed.

VCPUH and VCPUL flags are available, in the PWR control register 6 (PWR_CR6), to indicate if V_{DDCPU} is higher or lower than the thresholds. The VCPUH and VCPUL are available on tamper signals but also connected to the EXTI2 and can generate an interrupt if enabled through the EXTI2 registers.

The detection is enabled by setting the VCPUMONEN bit in PWR control register 6 (PWR_CR6). The VDDCPU voltage thresholds, when enabled, are not available in Run2, LPLV-Stop1, LPLV-Stop2, Standby1, Standby2, and V_{BAT} modes.

For more details concerning the vcpu_thr_high and vcpu_thr_low threshold, refer to the electrical characteristics of the datasheet.

2.4.6 VDDGPU monitoring (GPUVM)

The system has an integrated circuitry (GPUVM) that enables monitoring the independent GPU supply V_{DDGPU}. VDDGPURDY indicates if the V_{DDGPU} independent power supply is higher or lower than the VDDGPUVM threshold.

The independent V_{DDGPU} supply is not considered as present by default, and logical and electrical isolation is applied to ignore any information coming from the V_{DDGPU} domain. The voltage monitor is disabled by default.

The output of the VDDGPU monitor is connected to an EXTI line and can generate an interrupt if enabled through the EXTI registers. The GPUVMO output interrupt is generated when the independent power supply drops below the VDDGPUVM threshold and/or when it rises above the VDDGPUVM threshold, depending on the EXTI line rising/falling edge configuration.

When the GPU is not used (V_{DDGPU} OFF) or on hold (V_{DDGPU} voltage reduced), a specific sequence should be used. Refer to the PWR section in the reference manual for details.

2.4.7 Programmable voltage detector (PVD)

The user can monitor the voltage level of the PVD_IN pin using the PVD (Programmable voltage detector). This can be achieved by comparing the voltage of the PVD_IN pin to the internal V_{REFINT} (Internal voltage reference) level.

The PVD is enabled by setting the PVDE bit in the PWR_CR3 register.

A PVDO flag is available to indicate whether the PVD_IN pin is higher or lower than the threshold. This event is internally connected to EXTI1 and can generate an interrupt if enabled through the EXTI1 registers. The PVD output interrupt can be generated when PVD_IN drops below the PVD threshold. It can also happen when PVD_IN rises above the PVD threshold depending on the EXTI line rising or falling edge configuration. As an example, the service routine can perform emergency shutdown tasks.

2.4.8 Peripheral voltage monitoring (PVM)

Only VDD and VDDA18AON are monitored by default, as it is the only supplies required for all system-related functions. The other I/O supplies (V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, $V_{DD33UCPD}$, $V_{DD33USB}$, and $V_{DDA18ADC}$) can be independent from VDD and can be monitored with peripheral voltage monitoring (PVM).

A GPVMO flag is available, in the PWR control register 1 (PWR_CR1), to indicate if all enabled independent power supplies are higher or lower than the PVM threshold. This event is internally connected to the EXTI1 and can generate an interrupt if enabled through the EXTI1 registers. The GPVMO interrupt can be generated when all enabled independent power supplies rise above the PVM threshold or when at least one enabled independent power supply drops below the PVM threshold, depending on the EXTI1 line rising/falling edge configuration. The PVM is not available in Standby1 and Standby2 mode.

The independent supplies (V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, $V_{DD33UCPD}$, $V_{DD33USB}$, and $V_{DDA18ADC}$) are not considered as present by default, and logical and electrical isolation is applied to ignore any information coming from the peripherals supplied by these dedicated supplies.

- If these supplies are shorted externally to VDD, the application should assume they are available without enabling any peripheral voltage monitoring and the power isolation can be removed by setting the corresponding supply valid bits.
- If these supplies are independent from VDD, the peripheral voltage monitoring (PVM) can be enabled to confirm whether the supply is present or not.

2.4.9 Backup regulator voltage thresholds

The backup regulator voltage (V08CAP) can be monitored by comparing it with two threshold levels.

Two flags are available in the PWR control register 2 (PWR_CR2), to indicate if V08CAP is higher or lower than the threshold. The monitoring can be enabled/disabled with a MONEN bit in PWR control register 2 (PWR_CR2). As an example, the levels could be used to trigger a routine to perform emergency saving tasks. The monitoring, when enabled, is also available in Standby1, Standby2, and V_{BAT} modes. The flags are available on tamper signals.

2.4.10 Application and system resets

An application reset (app_rst) is generated from one of the following sources:

- A reset from NRST pad
- A reset from POR/PDR signal (generally called power-on reset)
- A reset from BOR signal (generally called brownout)
- A reset from one of the independent watchdogs (IWDG)
- A software reset from the RCC
- A failure on HSE, when the clock security system feature is activated
- A RETRAM CRC error reset
- A RETRAM ECC failure reset

A system reset (sys_rstn) is generated from one of the following sources:

- A reset from app_rstn signal (application reset)
- A reset from vcore_rstn signal
- A reset from vcpu_rstn signal when the D1 domain does not exit from Standby1/2

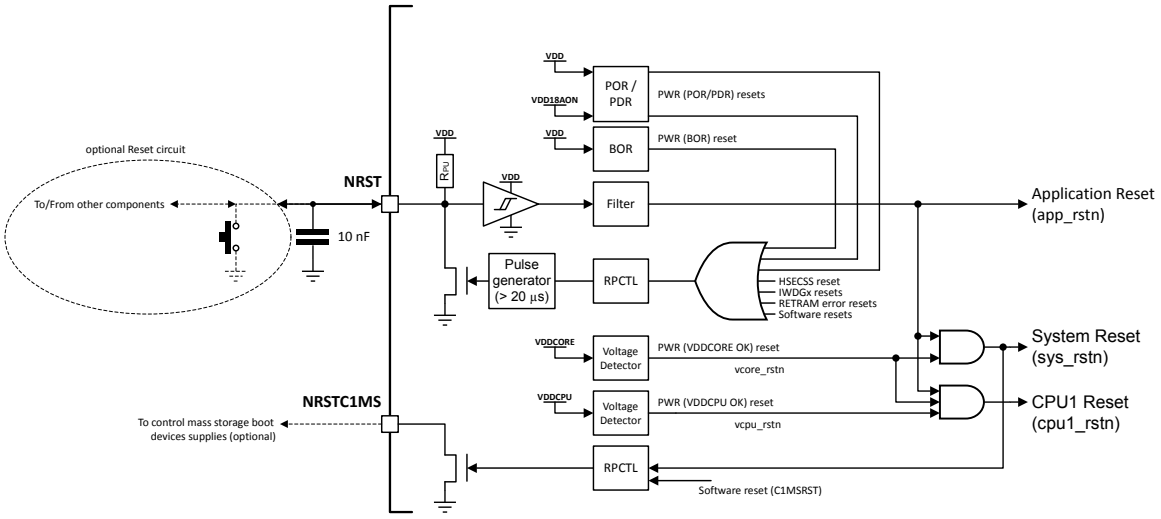
Note: When the system is in Standby1 or Standby2, the V_{DDCORE} and V_{DDCPU} are switched off, but V_{DD} and $V_{DD18AON}$ are still present. So when the system exits from Standby1 or Standby2, the vcore_rst signal is activated, generating a nreset reset.

NRST pin is also activated when app_rstn is internally generated and low level duration could be adapted using RPCTL.

NRSTC1MS pin is activated when sys_rstn is generated. NRSTC1MS pin could be used to control supplies of external flash memory required for the first level boot of CPU1 and which need a power cycle to ensure a platform reboot (for example, SD-Card). Low level duration could be adapted using RPCTL.

Refer to the RCC section in the product reference manual for more details on reset coverage and configuration.

Figure 2. Simplified reset pin circuit



1. *This is a very simplified view, only to give an overview of resets flows, it does not include all details. Details and specific behaviors are described in the product reference manual.*

3 Packages

3.1 Package selection

The package must be selected by considering the constraints that are strongly dependent upon the application.

The list below summarizes the more frequent constraints:

- Number of interfaces required
  Some interfaces might not be available on some packages.
  Some interfaces combinations might not be possible on some packages.
  Refer to product datasheets for details.
- PCB technology constraints
  Small pitch and high ball density could require more PCB layers and higher PCB class requiring stack-up with microvia (laser via) technology.
- Package height
- PCB available area
- Thermal constraints
  Larger packages have better thermal dissipation capabilities.

Table 7. Package availability summary

Size (mm)(1)	16 x 16	10 x 10	14 x 14	18 x 18
Pitch (mm)	0.8	0.5	0.5	0.8
Thickness (mm)	1.2	1	1	1.2
Sales number	TFBGA361	VFBGA361	VFBGA424	TFBGA436
STM32MP231x	AJ	AL	AK	-
STM32MP233x	AJ	AL	AK	-
STM32MP235x	AJ	AL	AK	-
STM32MP251x	AJ	AL	AK	AI
STM32MP253x	AJ	AL	AK	AI
STM32MP255x	AJ	AL	AK	AI
STM32MP257x	AJ	AL	AK	AI

1. *Typical body size*

Note: Refer to the product datasheets on www.st.com for up-to-date reference availability.

Table 8. STM32MP25xx differences per package

Features			STM32MP25xxAJ	STM32MP25xxAL	STM32MP25xxAK	STM32MP25xxAI
			TFBGA361	VFBGA361	VFBGA424	TFBGA436
Package		Body size (mm)	16 x 16	10 x 10	14 x 14	18 x 18
		Pitch (mm)	0.8	0.5	0.5	0.8
		Thickness (mm)	1.2	1	1	1.2
		Ball count	361	361	424	436
SDRAM	-		Up to 2 x 4.8 Gbytes internal buses. AES-128 Encryption/Decryption			
	DDR3L	16 bits, 1066MHz	Up to 1 Gbyte, single rank			
		32 bits, 1066MHz	-		Up to 2 Gbytes, single rank	
	DDR4	16 bits, 1200MHz	Up to 4 Gbytes, single rank			
		32 bits, 1200MHz	-		Up to 4 Gbytes, single rank	
	LPDDR4	16 bits, 1200MHz	Up to 2 Gbytes, single rank			
		32 bits, 1200MHz	-		Up to 4 Gbytes, single rank, two channels in parallel (lockstep)	
LVDS display interface (LVDS)			Single-link of 4 x data lanes 1.1 Gbps each (up to 1050p60)(1)		Dual-link of 4 x data lanes 1.1 Gbps each (up to 1536p60)(1)	
GPIO	**with interrupt (total** count)		144	144	144	172
	Wake-up pins		6	6	6	6
	Tamper input/active output pins		8 + 8	8 + 8	8 + 8	8 + 8
ADC	ADC channels in total (differential)		23 (11)(2)	23 (11)(2)	21 (10)	23 (11)(2)

1. *Availability depends on the device.*
2. *Including two (or one differential) low noise inputs on dedicated ANA0/ANA1 pins.*

Table 9. STM32MP23xx differences per package

Features			STM32MP23xxAJ	STM32MP23xxAL	STM32MP23xxAK
			TFBGA361	VFBGA361	VFBGA424
Package		Body size (mm)	16 x 16	10 x 10	14 x 14
		Pitch (mm)	0.8	0.5	0.5
		Thickness (mm)	1.2	1	1
		Ball count	361	361	424
SDRAM	-		Up to 2 x 4.8 Gbytes internal buses. AES-128 Encryption/Decryption		
	DDR3L	16 bits, 1066MHz	Up to 1 Gbyte, single rank		
	DDR4	16 bits, 1200MHz	Up to 4 Gbytes, single rank		
	LPDDR4	16 bits, 1200MHz	Up to 2 Gbytes, single rank		
LVDS display interface (LVDS)			4 x data lanes 1.1 Gbps each (up to 1050p60)(1)		
GPIO	**with interrupt (total** count)		144	144	144
	Wake-up pins		6	6	6
	Tamper input/active output pins		8 + 8	8 + 8	8 + 8
ADC	ADC channels in total (differential)		23 (11)(2)	23 (11)(2)	21 (10)

1. *Availability depends on the device.*
2. *Including two (or one differential) low noise inputs on dedicated ANA0/ANA1 pins.*

3.2 Alternate function mapping to pins

As a general rule, for each used interface, it is recommended to keep ball choices together as close as possible to ease PCB routing and to avoid potential timing issues.

In addition, to fulfill timings, I3C signals like SDA/SCL pairs must be chosen thanks to Table 10. I3C pins possible combinations.

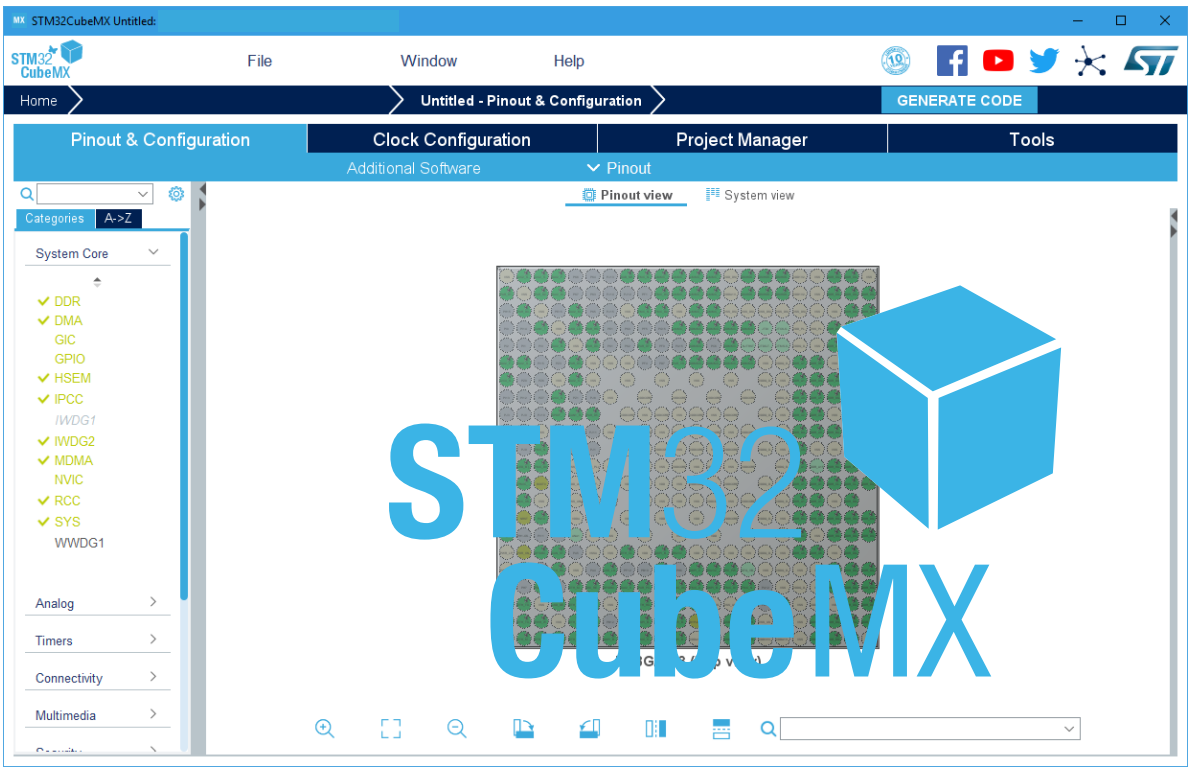
Table 10. I3C pins possible combinations

SCL signals	SDA signals		
I3C1			
-	PJ10	PI1	PA2
PJ1	Yes	-	-
PG13	-	Yes	-
PA3	-	-	Yes
I3C2			
-	PF0	PB4	PJ13
PF2	Yes	-	-
PB5	-	Yes	-
PJ12	-	-	Yes
I3C3			
-	PH2	PG0	PG2
PH6	Yes	-	-
PC12	-	Yes	Yes
PG1	-	Yes	Yes
I3C4			
-	PZ0	PZ3	PZ9
PZ1	Yes	Yes	Yes
PZ2	Yes	Yes	Yes
PZ4	Yes	Yes	Yes

In order to explore easily peripheral alternate functions mapping to pins, it is recommended to use the STM32CubeMX tool available on www.st.com.

Note: STM32CubeMX might not support all features or options that are described in the product reference manual or datasheet. This is usually due to reduced features in software deliveries such as OpenSTLinux or STM32CubeMP2. This can evolve in future releases of the ecosystem.

Figure 3. STM32CubeMX example screenshot



1. *This is a screenshot example. It is not specific to STM32MP25xx lines. The appearance can also differ with future STM32CubeMX versions.*

4 Clocks

Different clock sources can be used to drive the subsystems clocks:

- HSI oscillator clock (high-speed internal clock signal): 64 MHz typical
- MSI oscillator clock (multispeed internal clock signal): 16 or 4 MHz typical
- HSE oscillator clock (high-speed external clock signal): 40 MHz typical
- PLL1 dedicated to Cortex-A35 core
- PLL2 dedicated to DDR subsystem
- PLL3 dedicated to GPU(1)
- PLL4/5/6/7/8 clocks
- PLL_DSI to generate the DSI clock (up to 2.5 GHz) (1)
- PLL_USB to generate the USB clock (480 MHz)
- PLL_COMBOPHY to generate the USB3DR (for SuperSpeed) or PCIE clocks (up to 5GHz)(1)
- PLL_LVDS to generate the LVDS clock (up to 1.1 GHz)(1)

1. *Availability depends on the STM32MP23/25xx lines devices.*

The devices have two secondary clock sources:

- 32 kHz low-speed internal RC (LSI RC) that drives the independent watchdog and, optionally, the RTC used for automatic wake-up from the Stop/Standby modes.
- 32.768 kHz low-speed external crystal (LSE crystal) that optionally drives the real-time clock (RTCCLK)

Each clock source can be switched on or off independently when it is not used, to optimize the power consumption.

Refer to the reference manual and datasheet for the description of the clock tree, and for details of the possible clock frequencies.

4.1 HSE oscillator clock

The high-speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE user external clock (see Figure 4).
- HSE external crystal (see Figure 5).

See also Section 8.1: Clock for recommended implementation.

Figure 4. HSE external clock

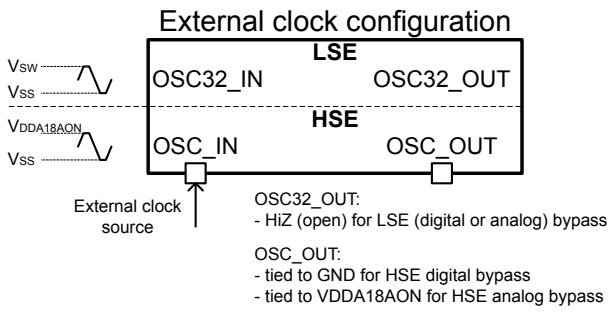
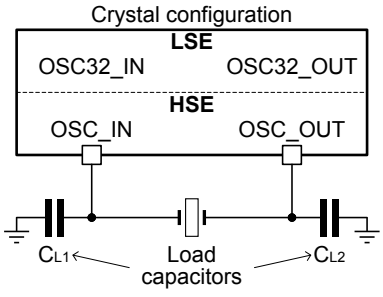


Figure 5. HSE crystal



1. Refer to the application note .

4.1.1 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency from 16 to 48 MHz (refer to the corresponding datasheets for actual max value).

The external digital (V_{IL}/V_{IH}) or analog (amplitude of 200 mV pk-pk minimum) clock signal with a duty cycle of about 50%, has to drive the OSC_IN pin.

Note: To allow USB boot, the boot ROM automatically selects the HSE mode by checking the OSC_OUT connection during the startup phase (that is on the NRST rising edge):

- OSC_OUT is tied to GND (max 1 kΩ): HSE digital bypass
- OSC_OUT is tied to $V_{DDA18AON}$ (max 1 kΩ): HSE analog bypass
- OSC_OUT high-Z or connected to a crystal: HSE crystal mode.

When utilizing a bypass, the activation of the external clock generator can be achieved through the PWR_ON feature for the purpose of power conservation (that is to say deactivated during Standby). In that case, the OSC_IN clock input must be stable within 10 ms after the PWR_ON rising edge occurs.

4.1.2 External crystal (HSE crystal)

The external oscillator frequency ranges from 16 to 48 MHz.

The external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in Figure 5. Using a 40 MHz crystal frequency is a good choice to get accurate USB high-speed clocks.

The crystal and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected crystal.

For C_{L1} and C_{L2} it is recommended to use NP0/C0G capacitors selected to meet the load requirements of the crystal. C_{L1} and C_{L2}, have usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. The PCB and pin capacitances must be included when sizing C_{L1} and C_{L2}.

Refer to the application note [1] and electrical characteristics sections in the product datasheet for more details.

4.2 LSE OSC clock

The LSE can be generated from two possible clock sources (see Figure 6 and Figure 7 below):

- LSE user external clock, see Figure 6
- LSE external crystal, see Figure 7

Figure 6. LSE external clock

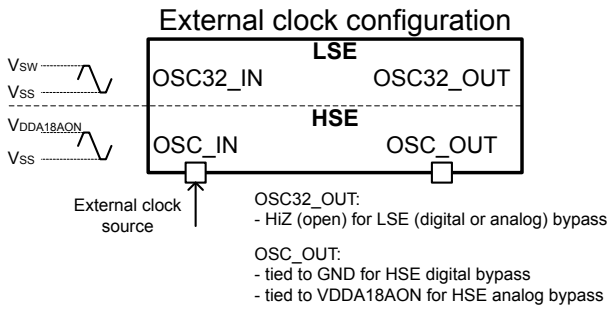
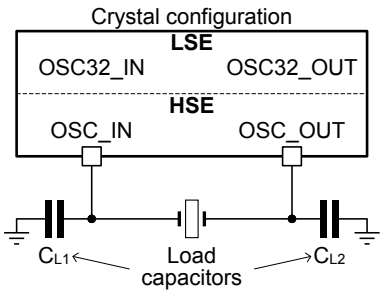


Figure 7. LSE crystal resonators



1. LSE crystal resonators: It is strongly recommended to use a crystal with a load capacitance CL≤12.5 pF.

4.2.1 External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. The external digital (VIL/VIH) or analog (amplitude of 200 mV pk-pk minimum) clock signal with a duty cycle of about 50% has to drive the OSC32_IN pin while the OSC32_OUT pin must be left high-Z (see Figure 6). The configuration of the bypass mode as well as the selection between the digital and analog is done within the RCC registers.

4.2.2 External crystal (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal. It has the advantage of providing a low-power, but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins. The goal is to minimize output distortion and startup stabilization time. The load capacitance values C_{L1} and C_{L2} must be adjusted according to the selected oscillator. It is recommended to use medium-high or high drive on the LSE oscillator.

Refer to the application note [1] and the electrical characteristics sections in the product datasheet for more details.

4.3 Clock security system (CSS)

Details can be found in the product reference manual (See Table 2. Reference documents).

4.3.1 CSS on HSE

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped. If a failure is detected on the HSE oscillator clock, an application reset can be generated.

4.3.2 CSS on LSE

The clock security system can be turned on using software. When this happens, the clock detector is turned on after a delay in the LSE oscillator startup. The detector is turned off when the oscillator stops. If there is a problem with the LSE oscillator clock, the RTC/TAMP clock source is stopped and the TAMP block is notified for security protection and system wake-up.

5 Boot configuration

5.1 Boot mode selection

In the STM32MP23/25xx lines, different boot modes can be selected by means of the BOOT[3:0] pins and OTP settings.

Table 11. Boot sources

BOOT[3:0] pins	Alternate boot pins OTP value							
	0b00 (default)				0b01	0b10	0b11	
	Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)		Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)	
			Cortex-A35	Cortex-M33			Cortex-A35	Cortex-M33
0	UART and USB(2) (3)							
1	SD-Card	-	-	-	SD-Card	SD-Card	Serial NAND	Serial NOR
2	e•MMC	-	-	-	e•MMC	e•MMC	e•MMC	Serial NOR
3	Development boot(2)							
4	Serial NOR	-			Serial NOR	Serial NOR	SLC NAND	Serial NOR
5	Serial NAND	-					e•MMC(4)	Serial NOR
6	SLC NAND	-					e•MMC(4)	HyperFlash™
7	-	SD-Card	-	-	HyperFlash™	HyperFlash™	Serial NAND	HyperFlash™
8	-	e•MMC	-	-	Serial NAND	Serial NAND	e•MMC	HyperFlash™
9	-		Serial NAND	Serial NOR	-		SD-Card(5)	Serial NOR
10	-		SLC NAND	Serial NOR	-		SD-Card(5)	HyperFlash™
11	-	Serial NOR	-	-	SLC NAND	SLC NAND	SLC NAND(6)	HyperFlash™
12	Development boot(2)							
13	-	-	e•MMC	Serial NOR	SD-Card(5)	SD-Card(5)	SD-Card	Serial NOR
14	-	-	SD-Card	Serial NOR	e•MMC(4)	e•MMC(4)	SD-Card	HyperFlash™
15	UART and USB(3)							

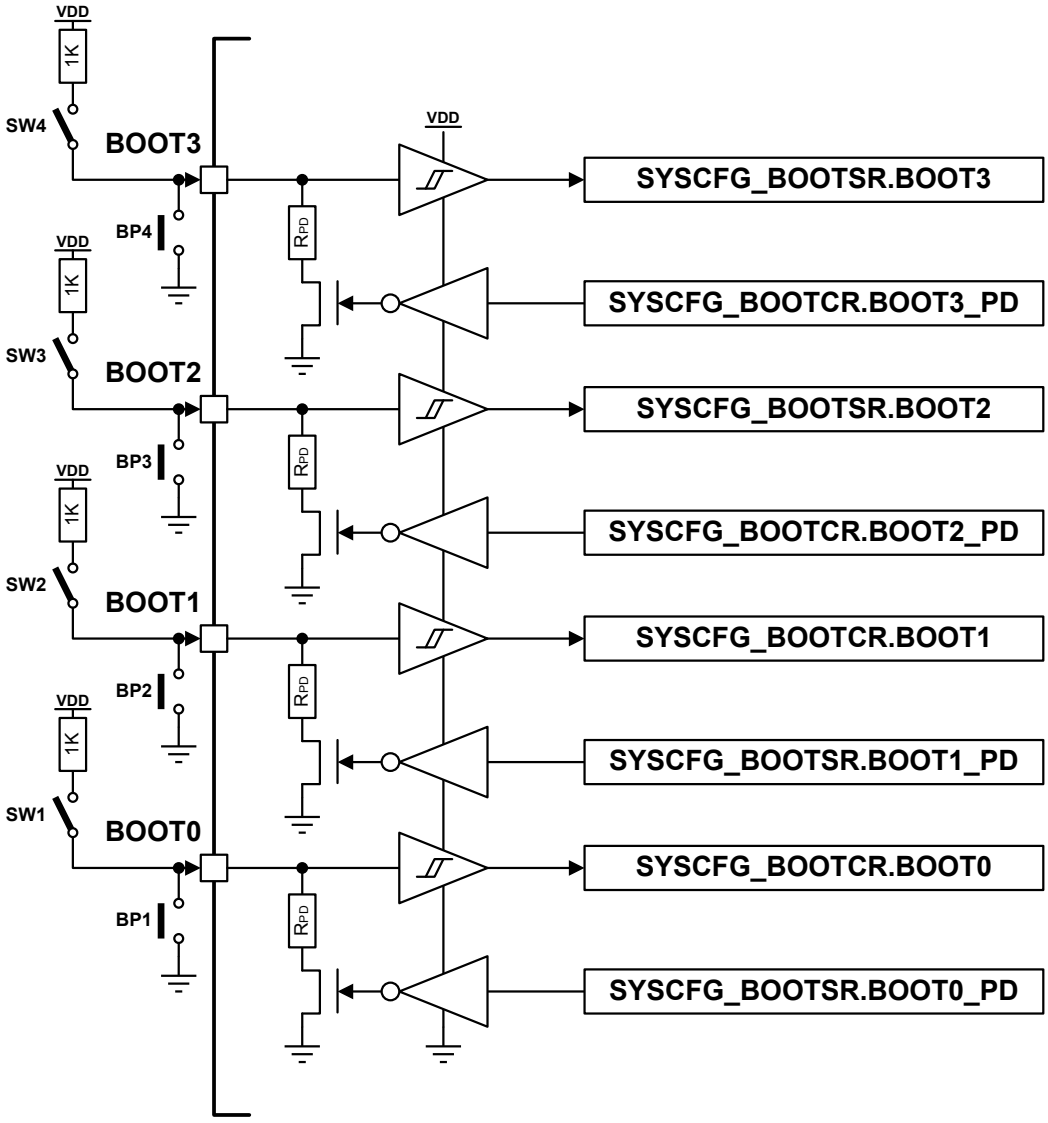
1. *Two flash memory config. Indirect Cortex-A35 boot (from Cortex-M33) or used during Cortex-A35 D1Standby exit*
2. *Cannot be override by OTP.*
3. *Wait incoming connection on USART2/6 or UART5/8/9 on default pins and USB high-speed device on USB3DR_DP/DM.*
4. *e•MMC on SDMMC1*
5. *SD-Card on SDMMC2*
6. *Only 8-bit memory is supported as some FMC and OCTOSPIM port2 pins are shared (usage of FMC in 16-bit mode is exclusive of usage of OCTOSPIM port2).*

The values on the BOOT pins are sampled by boot ROM after a reset. It is up to the user to set the BOOT[3:0] pins before reset exit to select the required boot mode. The BOOT pins could also be resampled later by software (for example by reading SYSCFG_BOOTCR.BOOT[3:0] field) or by the boot ROM when exiting the Standby mode. Consequently, they must be kept in the required boot mode configuration all the time.

5.2 Boot pin connection

Figure 8 shows an example of the external connection required to select the boot memory of the STM32MP23/25xx lines devices.

Figure 8. Boot mode selection example



Despite all the recovery cases in software, there is a risk that with wrong or corrupted flash memory content (such as: user mistake, bad flash memory content programmed, power lost), the system might not start (also known as ‘bricked’).

Note that on empty flash memory, the boot code automatically switches to UART/USB connection.

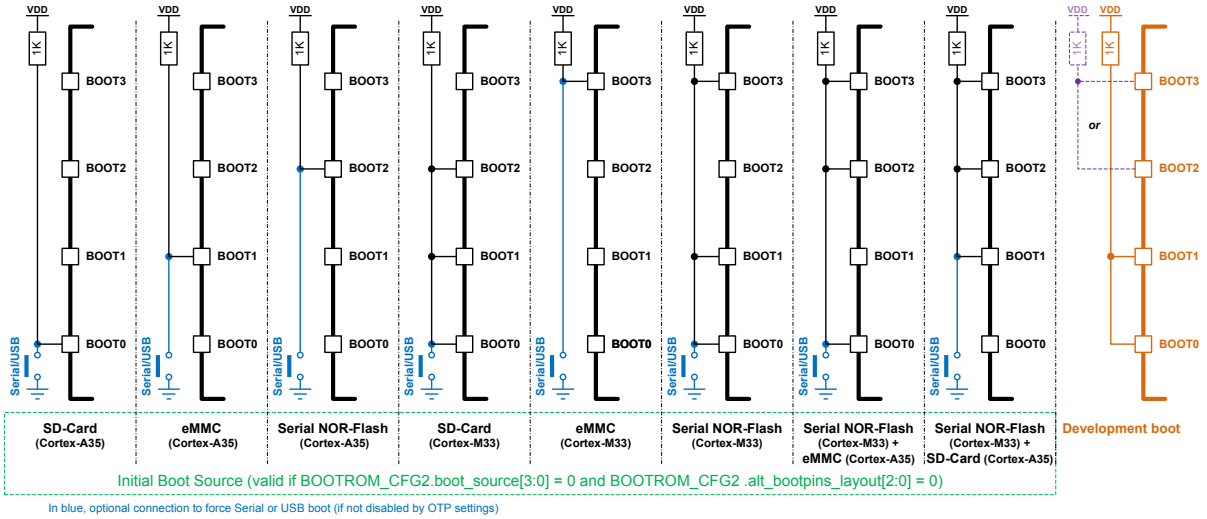
It might be required to have a way to force use of UART/USB connection in order to enable board flash memory reprogramming (for example: after sale services, firmware update).

There are also cases of where initial boot is done on a different flash memory than regular boot (for example the initial boot from SD-Card, which copies binary data in another flash memory like serial NOR, serial NAND, eMMC, or SLC NAND). This is possible as the initial boot code could set relevant OTP bits to force future boot from the programmed flash memory (see Figure 10). This allows a simplified and flexible mass production without intervention on BOOT pins. The typical connections examples for a final board are described in Figure 9.

The switches could be done by various ways: pushbutton, solder bridges, connector contacts, test points, and so on, but assumed ‘open’ by default during normal product boot to avoid current flow in external resistors.

Note that OTP configuration could force or forbid any of the boot sources in order to satisfy product security requirements.

Figure 9. BOOT pins typical connection schematics



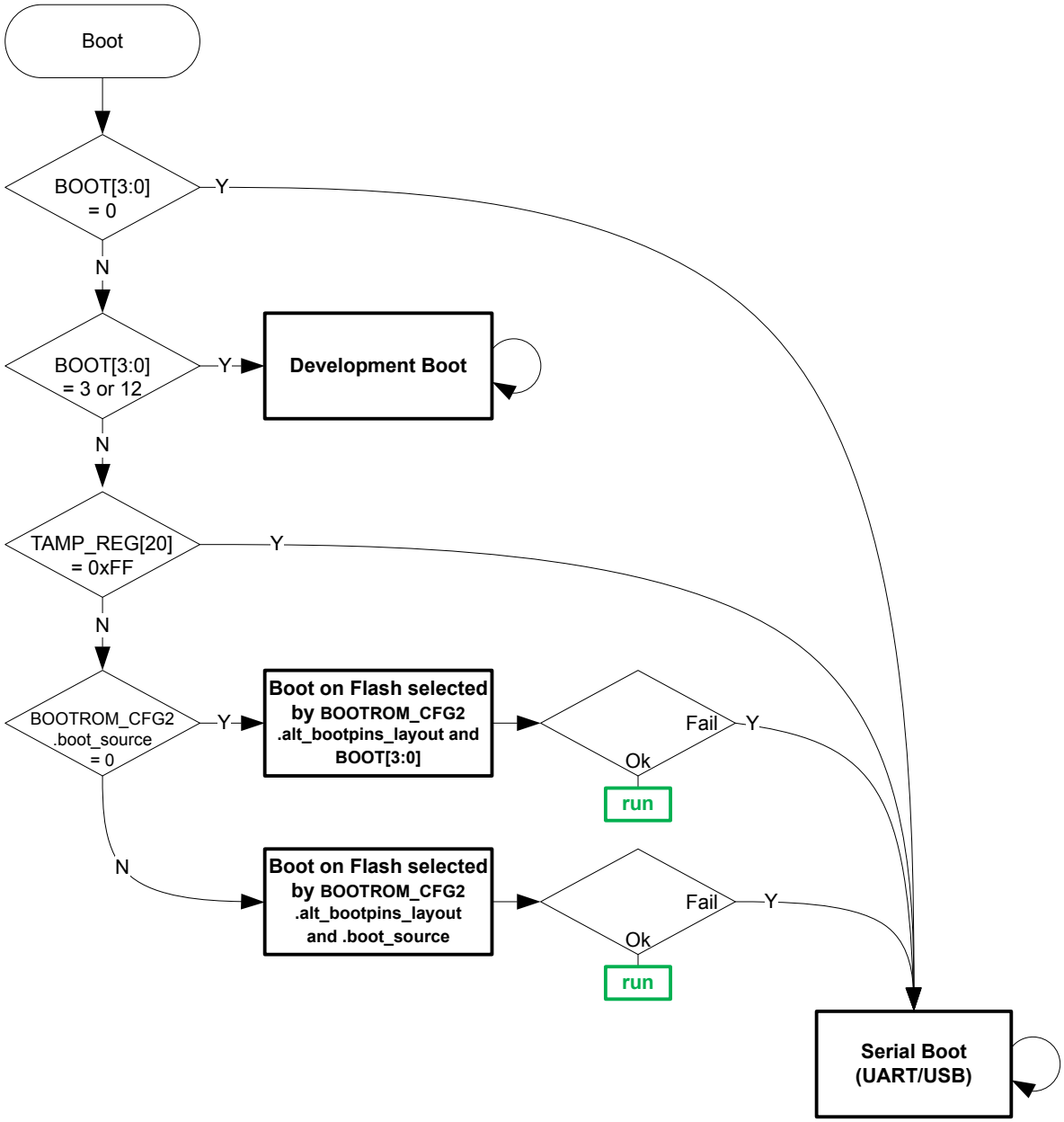
5.3 Embedded bootloader mode

This embedded bootloader is located in the boot ROM memory. During boot, the OCTOSPI, FMC, SDMMC, and USART peripherals operate with the internal 64 MHz oscillator (HSI).

The USB3DR high-speed device, however, can function only if an external clock (HSE) is present with a recommended frequency of 40 MHz (alternatively, 16, 19.2, 20, 24, 25, 26, 28, 32, 36, 40 or 48 MHz could be used with OTP settings and/or automatic frequency detection).

For additional information, refer to the USB DFU/USART protocols used in STM32MP1 series bootloaders [3].

Figure 10. Simplified boot flow



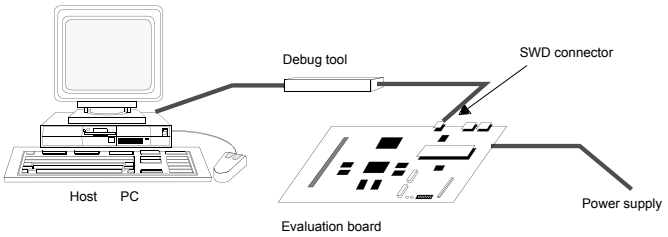
6 Debug management

6.1 Introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG, or SWD connector and a cable connecting the host to the debug tool.

Figure 11 shows the connection of the host to the evaluation board.

Figure 11. Host-to-board connection



6.2 SWJ debug port (serial wire and JTAG)

The STM32MP25xx lines core integrates the serial Wire/JTAG debug port (SWJ-DP). It is an Arm® standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and an SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHB-AP port

The two pins of the SW-DP are multiplexed with two of the five JTAG pins of the JTAG-DP.

6.3 Pinout and debug port pins

6.3.1 Internal pull-up and pull-down resistors on JTAG pins

To avoid any uncontrolled I/O levels, the STM32MP25xx lines embed internal pull-up and pull-down resistors on JTAG pins:

- NJTRST: Internal pull-up
- JTDI: Internal pull-up
- JTDO-TRACESWO: Internal pull-up
- JTMS-SWDIO: Internal pull-up
- JTCK-SWCLK: Internal pull-down

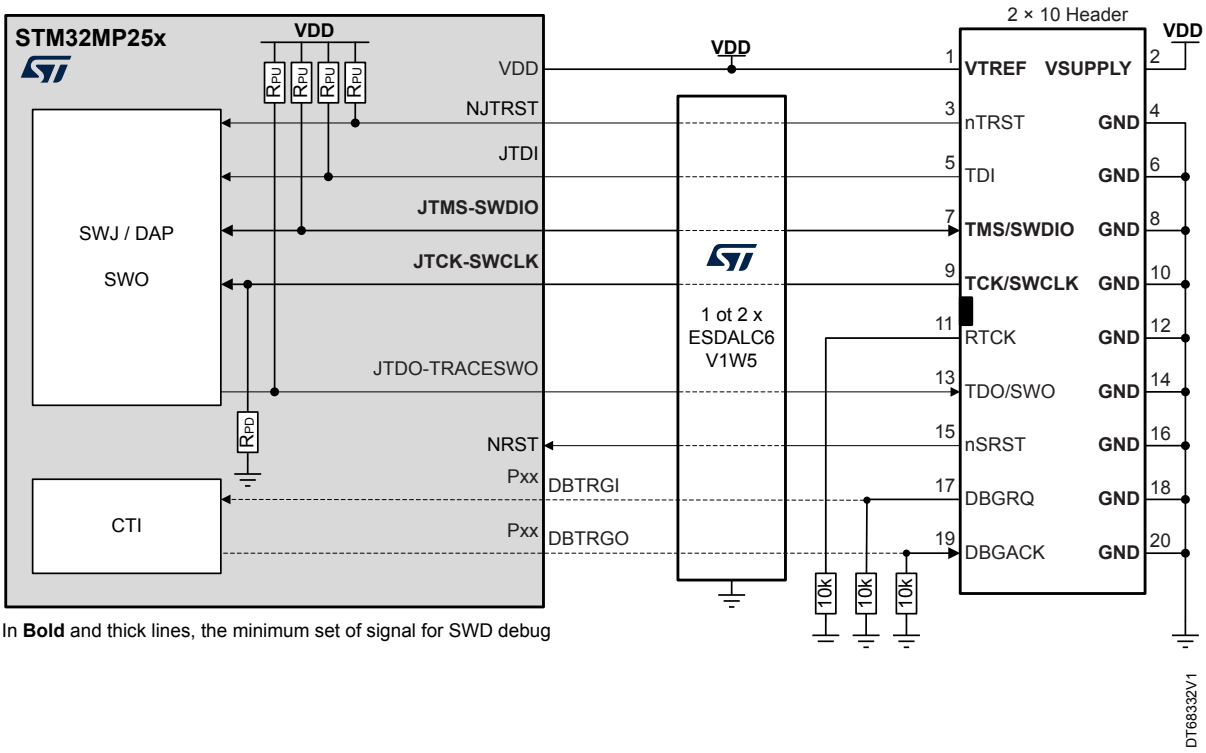
Note:

- *The JTAG IEEE standard recommends adding pull-up resistors on TDI, TMS, and nTRST but there is no special recommendation for TCK. However, for the STM32MP25xx lines, an integrated pull-down resistor is used for JTCK.*
- *Having embedded pull-up and pull-down resistors removes the need to add external resistors.*
- *In order to use the RMA (return material acceptance), the JTAG pins (JTDI, JTCK, JTMS) must be accessible. The JTDO pin might be needed too, depending on the tool that is used.*

6.3.2 Debug port connection with standard JTAG connector

Figure 12 shows the connection between the STM32MP23/25xx lines and a standard JTAG/SWD connector.

Figure 12. JTAG/SWD using Arm® JTAG 20 connector implementation example



In **Bold** and thick lines, the minimum set of signal for SWD debug

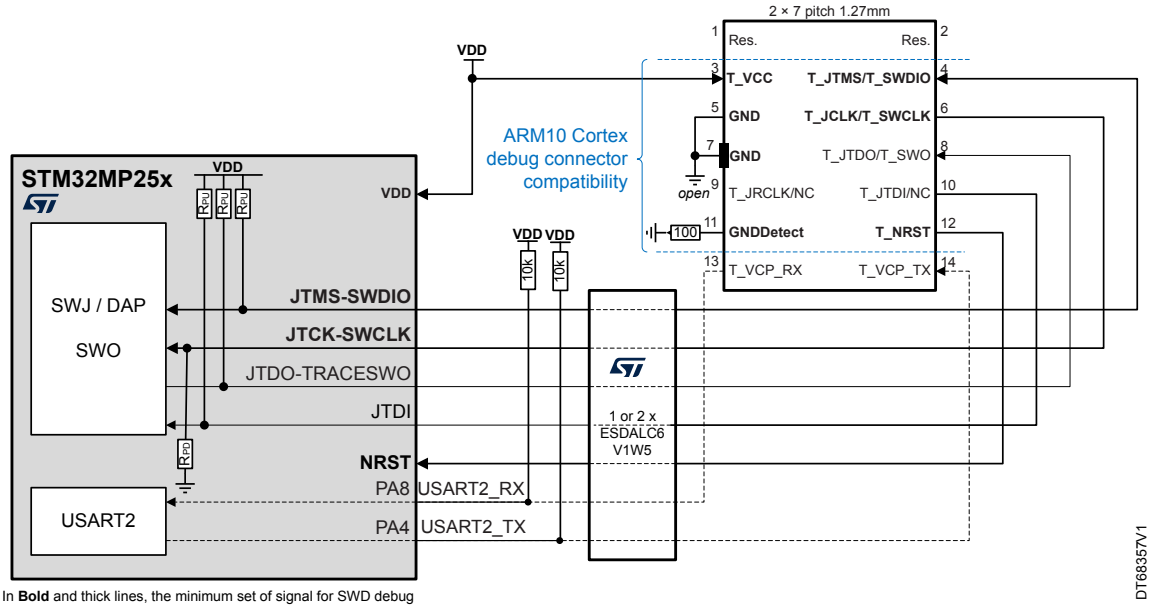
Note: The single wire trace on the TRACESWO pin is only available for Cortex®-M core. To trace all cores activity, a parallel trace port must be used (see Section 6.3.4: Parallel trace and HDP).

6.3.3 Debug port and UART connection with STDC14 connector

Figure 13 shows the connection between the STM32MP23/25xx lines and an STDC14 connector including UART virtual com port connection.

Reference example for the STDC14 header is FTSH-107-01-L-DV-K-A.

Figure 13. JTAG/SWD/UART VCP using STDC14 connector implementation example



Note:

- *The single wire trace on the TRACESWO pin is only available for Cortex®-M33 core. To trace all core activities, a parallel trace port must be used (see Section 6.3.4: Parallel trace and HDP).*
- *STDC14 connector is respecting (from pin 3 to pin 12) the Arm10 pinout (Arm® Cortex® debug connector).*

6.3.4 Parallel trace and HDP

Parallel trace

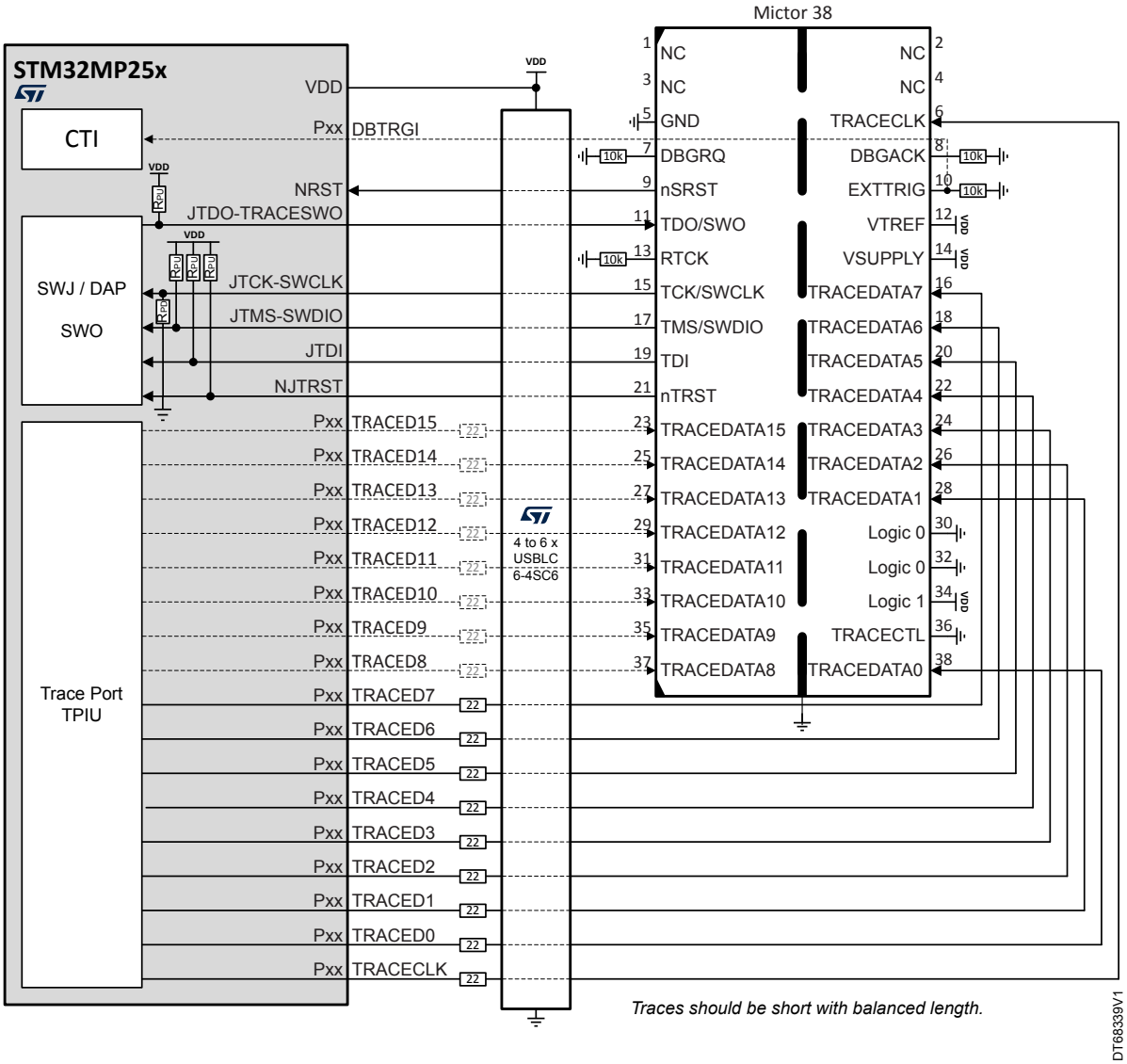
TRACED[15:0] and TRACECLK signals are available as alternate functions on I/Os pins. The user could select the number of trace data N = 1, 2, 4, 8 or 16 pins. Less trace data mean lower available trace bandwidth, so less information could be traced (such as the number of trace sources, code and/or data tracing) without trace overrun. For each product, a trade-off between available features and the trace bus could lead to have reduced feature while using trace during product development.

The trace is compliant to Arm® CoreSight™ trace. It needs a dedicated tracing tool in order to be interpreted and correlated with debugging done through SWD or JTAG.

For more information on the Trace Port interface CoreSight™ component, refer to the product reference manual and the Arm® CoreSight™ technical reference manual.

Note that for efficient tracing bandwidth, TRACECLK should run as fast as possible while maintaining good signal integrity on all parallel trace signals. This is dependent on board and connector choices, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

Figure 14. **Parallel trace port with JTAG/SWD on Mictor-38 implementation example**



Hardware debug port (HDP)

Some internal signals are available for deep debugging. Internal knowledge and an oscilloscope or logic analyzer are needed. For more information, refer to the product reference manual and datasheet.

6.3.5 Debug triggers and LEDs

The CoreSight™ cross-trigger interface (CTI) is available on pins as DBTRGI and DBTRGO.

DBTRGI could be generated by the external user signal. It could be programmed also inside CoreSight™ components to start/stop traces or enter specific cores in debug mode (break).

DBTRGO could be generated by CTI to see externally that a trigger condition is reached by one of the CoreSight™ components (core break, trace started, and so on.).

DBTRGO could be made available on PZ3, PZ4, and PZ6.

DBTRGI could be made available on PZ3, PZ4, and PZ6.

6.3.6 Debug LED

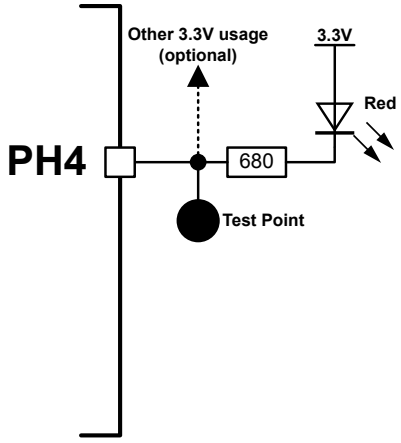
The PH4 pin has a specific BOOTFAILN behavior (see boot documentation for details):

- During the boot phase, in case of boot failure, the PH4 pin is set to low open-drain. The debug LED lights bright. Note that in most cases, without secure boot enabled, this fail is not visible as it immediately falls back to an UART/USB boot.
- During UART/USB boot, the PH4 pin toggles open-drain at a rate of few Hz until a connection is started. The debug LED blinks fast.
- With BOOT[3:0] = 0b0011 (development boot), PH4 is set to low open-drain. The debug LED lights bright.
- In all other cases, like normal boot, the PH4 pin is kept in its reset value. It means in high-Z until further software setting.

It is a good idea to put a red LED on PH4 as shown in Figure 15. In case of VDD= 1.8V, additional circuitry might be needed.

LEDs are useful for quick visual signaling of system activity. So, it is a good choice to use at least PH4 for quick low level boot error signaling. In most cases, the LED circuitry does not conflict with usage for other purposes (such as USBH_HS_OVRCUR, USB3DR_OVRCUR).

Figure 15. PH4 LED connection (valid for VDD = 3.3V)



7 Recommendations

7.1 PCB

For technical reasons, it is mandatory to use a multilayer PCB with a separate layer dedicated to the ground (VSS), and another layer dedicated to power supplies like V_{DD}, V_{DDCPU}, and V_{DDCORE}. This provides good decoupling and a good shielding effect.

7.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution. The aim is to reduce cross-coupling on the PCB that is noisy high-current circuits, low-voltage circuits, and digital components.

7.3 Ground and power supplies (V_{SSx},V_{DDx})

Due to a large power and high frequencies involved in the STM32MP25xx devices, it is mandatory to use PCB with at least four layers and with dedicated power planes for V_{SSx} and V_{DDx}.

7.4 GPIO advance configuration

To utilize ETH RGMII, DCMIPP parallel inputs, LTDC parallel outputs, or parallel TRACE outputs (TPIU), it is necessary to configure certain settings within the GPIOx_ADVCFG and GPIOx_DELAY registers. Refer to Table 12. GPIO advance configuration recommended settings below for recommended values.

Table 12. GPIO advance configuration recommended settings

Interface	Mode	Signals	GPIOx_ADVCFGR bits				GPIOx_DELAY field
			RET	INVCLK	DE	DLYPATH	DLY[3:0]
ETH1, ETH2, ETH3(2)	RGMII	ETHx_RGMII_RX_CTL	1	0	1	0	0b0000
		ETHx_RGMII_RXD[3:0]					
		ETHx_RGMII_TX_CTL					
		ETHx_RGMII_TXD[3:0]					
		others ETHx_	0	0	0	0	0b0000
	RGMII_ID (GMAC side internal delays) (1)	ETHx_RGMII_RX_CLK	0	0	0	1	0b1101
		ETH1_RGMII_GTX_CLK	0	0	0	0	0b1100
		ETH2_RGMII_GTX_CLK	0	0	0	0	0b1011
		ETH3_RGMII_GTX_CLK	0	0	0	0	0b1011 or 0b1100
		ETHx_RGMII_RX_CTL	1	0	1	0	0b0000
		ETHx_RGMII_RXD[3:0]					
		ETHx_RGMII_TX_CTL					
		ETHx_RGMII_TXD[3:0]					
		others ETHx_	0	0	0	0	0b0000
DCMIPP parallel	PIXCLK rising edge sampling	DCMIPP_PIXCLK	0	1	0	0	0b0000
		others DCMIPP_	1	1	0	0	0b0000
	PIXCLK falling edge sampling	DCMIPP_PIXCLK	0	0	0	0	0b0000
		others DCMIPP_	1	1	0	0	0b0000
LTDC parallel	Signals change on CLK rising edge	LCD_CLK	0	0	0	0	0b0000

Interface	Mode	Signals	GPIOx_ADVCFGR bits				GPIOx_DELAY field
			RET	INVCLK	DE	DLYPATH	DLY[3:0]
LTDC parallel	Signals change on CLK rising edge	others LCD_	1	0	0	0	0b0000
	Signals change on CLK falling edge	LCD_CLK	0	1	0	0	0b0000
		others LCD_	1	0	0	0	0b0000
TRACE (TPIU) parallel	Edge align data	TRACECLK	1	0	0	0	0b0000
		others TRACEx	1	0	0	0	0b0000
	Center align data	TRACECLK	1	0	0	0	0b0000
		others TRACEx	1	1	0	0	0b0000

1. *Use these settings only if 2ns internal delay is needed for RGMII timings. Delay values could be slightly tuned if required.*
2. *ETH3 could use same settings than ETH1 or ETH2, except that values are specified by design and not evaluated by characterization nor tested in production.*

7.5 I/O speed settings

It is important to set the right output drive on I/Os to have sufficient rise and fall time. Moreover, it helps avoid any additional ringing and noise.

When there are no specific requirements for I/O speed, it is mandatory to set OSPEEDR to 0.

As a first approximation, the following drawing and tables could be used to choose quickly the right setting to apply according to signal frequency and capacitive load. This setting might need to be tailored in case of signal integrity issue.

Whenever one OSPEEDR value of two or three is used, related I/O compensation needs to be enabled in SYSCFG. There are five independent I/O compensations for each of the five independent I/O supplies: V_{DD}, V_{DDIO1}, V_{DDIO2}, VDDIO3, and V_{DDIO4}. Refer to the product datasheet and reference manual for more details.

Note that there are five independent I/Os voltage sections (V_{DD}, V_{DDIO1}, V_{DDIO2}, VDDIO3, or V_{DDIO3}), which, in some AFMUX settings cases, could be shared between different interfaces.

When V_{DD}, V_{DDIO1}, V_{DDIO2}, VDDIO3, or V_{DDIO4} are working at 1.8 V, settings must be done in PWR_CR1.VDDIOxVRSEL (for VDD, VDDIO3 and VDDIO4) or PWR_CR7.VDDIO2VRSEL (for VDDIO2) or PWR_CR8.VDDIO1VRSEL (for VDDIO1). Without these settings, the I/Os are working in degraded mode.

Note: To avoid I/O damage due to mis-settings, in addition to PWR settings, there are OTP bits (HSLV_VDDIOx) which must be programmed when a specific domain (V_{DD}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, or V_{DDIO4}) may be used below 2.5 V on a product. See related sections in the product reference manual for details.

Note: In case of asynchronous or single edge clocked data lanes (such as SDR), the maximum data frequency toggle is effectively half the data rate.

For example, an SPI running at 10 Mbit/s/s has a maximum frequency of 5 MHz on the data signal, like output serial data 01010101..., but 10 MHz on the clock signal.

On dual-edge clocked data lanes (such as DDR), the clock, and data have the same maximum toggling frequency.

Figure 16. I/O speed summary with various loads and voltages

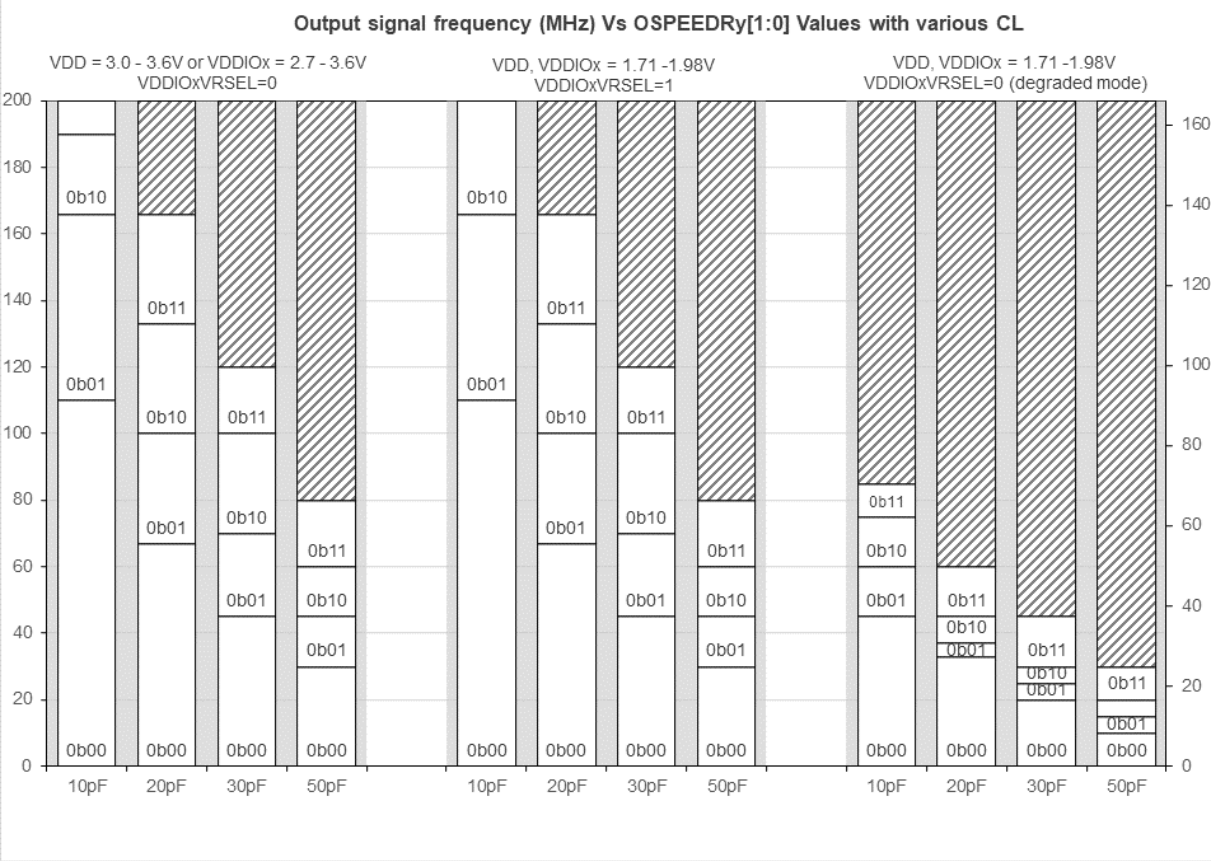


Table 13. OSPEEDR setting example for VDD = 3.3 V typ.[1]

Peripheral	Signals	Toggling rate (MHz)	OSPEEDR CL=30 pF		OSPEEDR CL=10 pF	
FMC async	Data/Controls	-	1	Medium speed	0	Low speed
FMC sync	CLK	66	3	Very high speed [2]	3	Very high speed [2]
	Data/Controls	33	1	Medium speed	0	Low speed
OCTOSPIM (SDR)	CLK	133	2[3]	High speed	1	Medium speed
	Data/Controls	66.5	1	Medium speed	0	Low speed
OCTOSPIM (DDR)	All	66.5	1	Medium speed	0	Low speed
LTDC	CLK	150	3 [3]	Very high speed	1	Medium speed
	Data/Controls	75	2	High speed	0	Low speed
LTDC	CLK	83	2	High speed	0	Low speed
	Data/Controls	41.5	0	Low speed	0	Low speed
TIM/LPTIM	All	5	0	Low speed	0	Low speed
I2C	All	1	0	Low speed	0	Low speed
USART	All	5	0	Low speed	0	Low speed
SPI	CLK	50	1	Medium speed	0	Low speed
	Data/Controls	25	0	Low speed	0	Low speed
SAI	MCLK	15	0	Low speed	0	Low speed
	CLK	1	0	Low speed	0	Low speed
	Data/Controls	0.5	0	Low speed	0	Low speed
SDMMC (SDR)	CLK	120	3 [3]	Very high speed	2	High speed
	Data/Controls	60	2	High speed	1	Medium speed
SDMMC (DDR)	All	52	1	Medium speed	0	Low speed
FDCAN	All	5	0	Low speed	0	Low speed
ETH (MII)	CLK	25	0	Low speed	0	Low speed
	Data/Controls	12.5	0	Low speed	0	Low speed
ETH (RMII)	All	50	1	Medium speed	0	Low speed
	Data/Controls	25	0	Low speed	0	Low speed
ETH (RGMII)	All	125	2 [3]	High speed	1	Medium speed
ETH (MDIO)	MDIO	2.5	0	Low speed	0	Low speed
TRACE	All	133	2 [3]	High speed	1	Medium speed
		100	2	High speed	0	Low speed

1. *VDDIOxVRSEL = 0*
2. *Required to reduce I/O delay for internal feedback clock. A serie resistor of 22-33 Ω close to FMC_CLK pin might be useful to improve signal integrity at memory side.*
3. *Value for 20 pF load*

Table 14. OSPEEDR setting example for VDD = 1.8 V typ.[1]

Peripheral	Signals	Toggling rate (MHz)	OSPEEDR CL=30 pF		OSPEEDR CL=10 pF	
FMC async	Data/Controls	-	1	Medium speed	0	Low speed
FMC sync	CLK	66	3	Very high speed[2]	3	Very high speed [2]
	Data/Controls	33	1	Medium speed	0	Low speed
OCTOSPIM (SDR)	CLK	133	2 [3]	High speed	1	Medium speed
	Data/Controls	66.5	1	Medium speed	0	Low speed
OCTOSPIM (DDR)	All	66.5	1	Medium speed	0	Low speed
LTDC	CLK	150	3 [3]	Very high speed	1	Medium speed
	Data/Controls	75	2	High speed	0	Low speed
LTDC	CLK	83	2	High speed	0	Low speed
	Data/Controls	41.5	0	Low speed	0	Low speed
TIM/LPTIM	All	5	0	Low speed	0	Low speed
I2C	All	1	0	Low speed	0	Low speed
USART	All	5	0	Low speed	0	Low speed
SPI	CLK	50	1	Medium speed	0	Low speed
	Data/Controls	25	0	Low speed	0	Low speed
SAI	MCLK	15	0	Low speed	0	Low speed
	CLK	1	0	Low speed	0	Low speed
	Data/Controls	0.5	0	Low speed	0	Low speed
SDMMC (SDR)	CLK	166	3 [3]	Very high speed	2	High speed
	Data/Controls	83	2	High speed	1	Medium speed
SDMMC (DDR)	All	52	1	Medium speed	0	Low speed
FDCAN	All	5	0	Low speed	0	Low speed
ETH (MII)	CLK	25	0	Low speed	0	Low speed
	Data/Controls	12.5	0	Low speed	0	Low speed
ETH (RMII)	All	50	1	Medium speed	0	Low speed
	Data/Controls	25	0	Low speed	0	Low speed
ETH (RGMII)	All	125	2 [3]	High speed	1	Medium speed
ETH (MDIO)	MDIO	2.5	0	Low speed	0	Low speed
TRACE	All	133	2 [3]	High speed	1	Medium speed
		100	2	High speed	0	Low speed

1. *VDDIOxVRSEL = 1*
2. *Required to reduce IO delay for internal feedback clock. A serie resistor of 22-33 ohms close to FMC_CLK pin might be useful to improve signal integrity at memory side.*
3. *Value for 20 pF load*

7.6 PCB stack and technology

A trade-off between the PCB cost and easy electrical connections has to be made. Below, examples are, either for four or six layers PCB with only PTH (suited for 0.8mm pitch package), or for six layers PCB with both PTH and laser drilled vias (suited for 0.5mm pitch package).

Note that some STM32MP25xx lines packages with an outer ball pitch of 0.5 mm provide power improved center ball matrix with depopulated matrix. It enables large PTH via in between balls.

This ensures better supply connection as well as optimized thermal conductivity than small buried laser drilled vias.

Figure 17. **6-layer PTH PCB stack example**

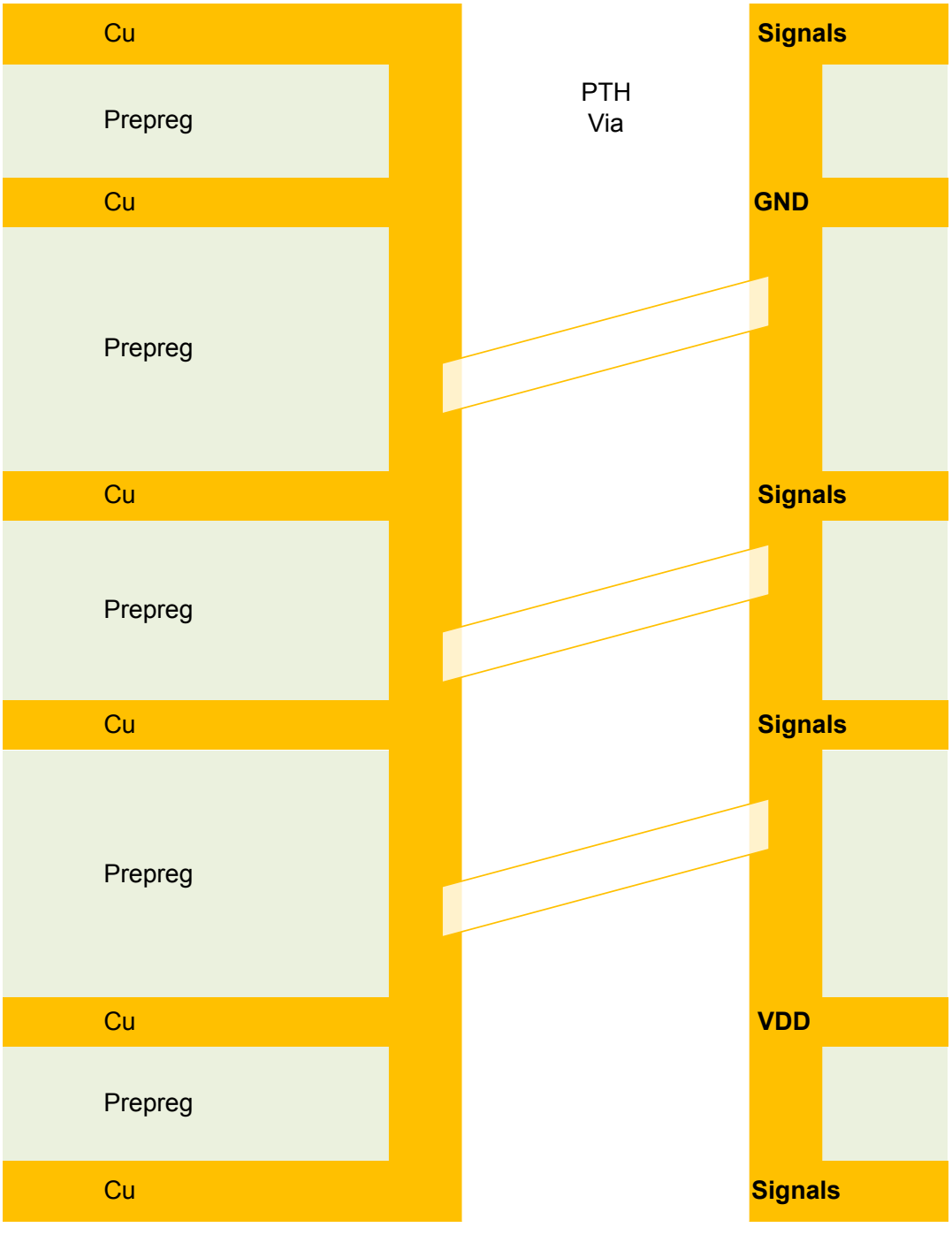


Figure 18. **6-layer PTH + laser vias PCB stack example**

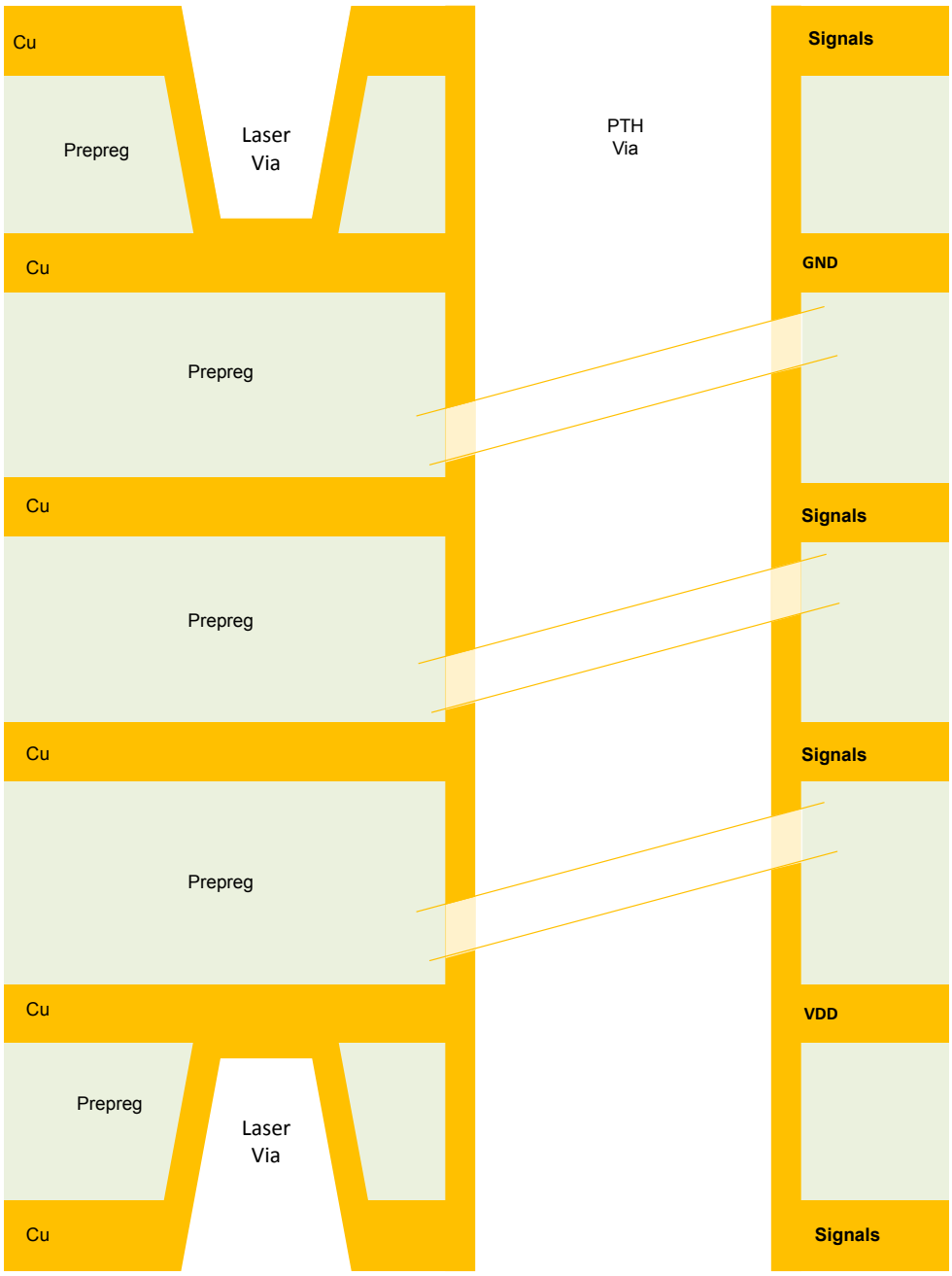


Figure 19. **PCB rule for 0.8 mm pitch package (with PTH)**

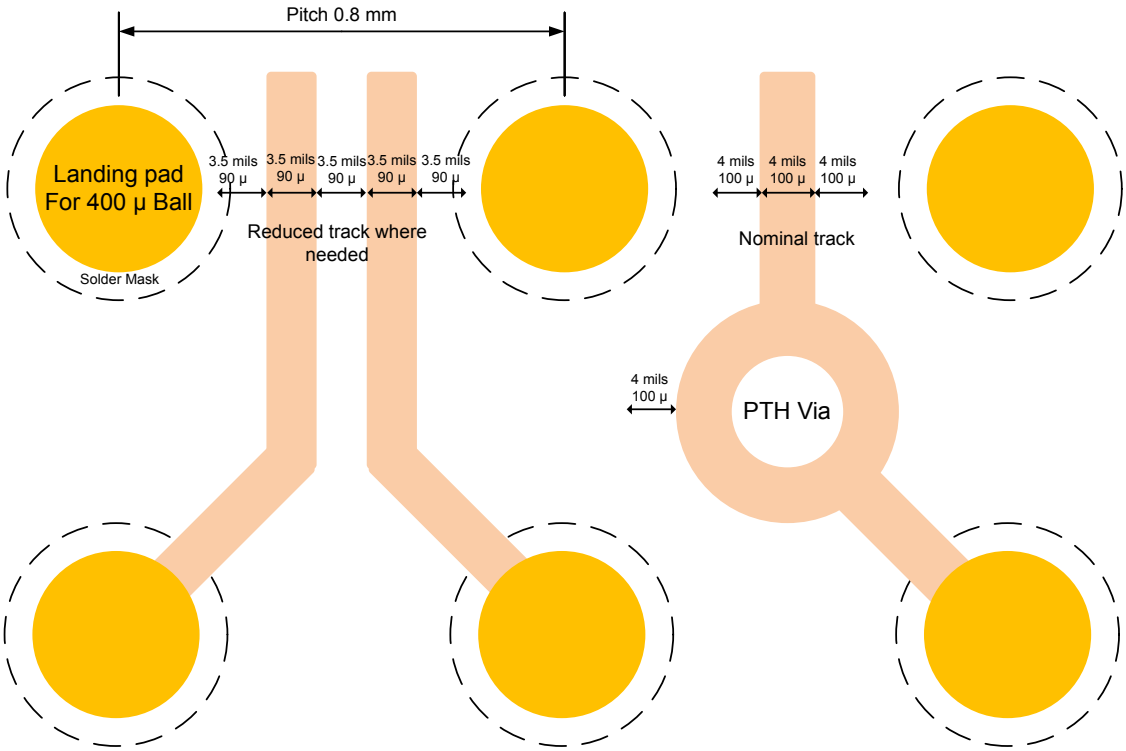
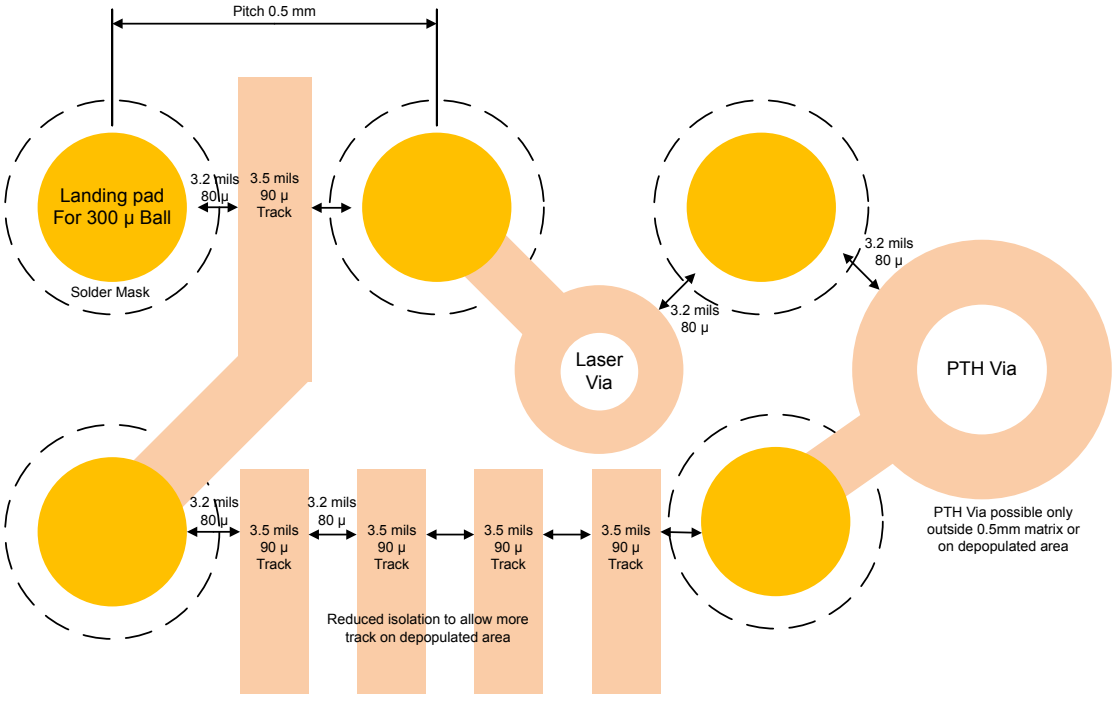


Figure 20. **PCB rule for 0.5 mm pitch package (with laser via and PTH)**

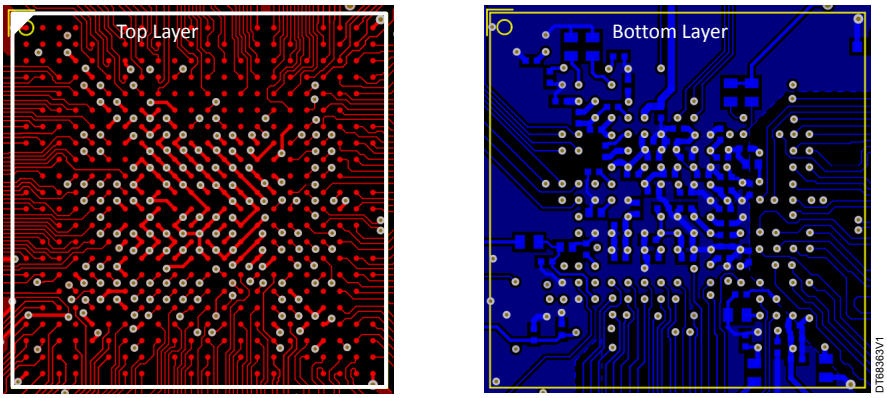


7.7 Decoupling

All the power supply and ground pins must be properly connected to the power supplies. These connections, including pins, tracks, and vias must have as low impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair must be decoupled with ceramic capacitors (most of the time 100 nF or 1 µF, see Table 4. Amount of decoupling recommendation by package[23]). These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Exact values might depend on the application. Figure 21 shows the typical layout of such a decoupling placement.

Figure 21. Example of decoupling layout



7.8 ESD/EMI protections

ElectroStatic discharge (ESD) and electromagnetic interference (EMI) should be taken into account from the beginning of a product development as it could be very complex and expensive to add them later.

ESD and EMI are driven by global standards (such as IEC 61000, JESD 22) which in most countries require a certification to allow mandatory marking to be applied on a product (such as CE, FCC).

ESD and EMI are also driven by standardized interface certification or requirements (for example USB).

Although the STM32MP23/25xx lines embed device level ESD protection, the final product protection should be done by external components, more especially on interfaces having external user access in the final product (such as Ethernet, USB, SD-card). Some components provide ESD protection as well as EMI common-mode filtering (for example ECMF02-2AMX6 used on USB). Some examples of ESD/EMI protections are provided in Section 8: STM32MP25x reference design examples.

For more details, refer to the application note [2] about the EMC design guide.

7.9 Sensitive signals

When designing an application, the EMC (electromagnetic compatibility) performance can be improved by closely studying the following points:

- Signals for which a temporary disturbance affects the running process permanently (such as interrupts and handshaking strobe signals) are not the case for LED commands.
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy or sensitive traces nearby (the crosstalk effect) improve the EMC performance. For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (such as clock)
- Sensitive signals (such as high-Z ones)

Signals that do not allow negative injection, such as input/output signals on VSW supply, need to be handled with care to prevent undershoots. To avoid this, a series resistor (usually 22 Ω) can be added close to the signal source to match impedance, or a small capacitor (suited to the impedance and frequency of the signal) can be added near the input/output to reduce ringing. Refer to the product datasheet for more information.

For more details, refer to the application note [2] about the EMC design guide.

7.10 Unused I/Os and features

The STM32MP25xx lines are designed for a wide range of applications and often a particular application does not use 100% of the resources.

To increase the EMC performance, unused clocks, counters, or I/Os should not be left free. For example, I/Os should be set to “0” or “1” (external or internal pull-up or pull-down to the unused I/O pins), and unused features should be “frozen” or disabled.

8 STM32MP25x reference design examples

This section provides examples to help the user to connect major and critical interfaces to the devices. Examples apply also to the STM32MP23x lines whenever the feature is available.

8.1 Clock

Two clock sources are used for STM32MP25xx lines, with the following choices:

- LSE: 32.768 kHz crystal for the embedded RTC
- HSE: 40 MHz crystal or external oscillator as STM32MP25xx lines main clock

Refer to Section 4: Clocks.

Figure 22. HSE recommended schematics for both oscillator/crystal options

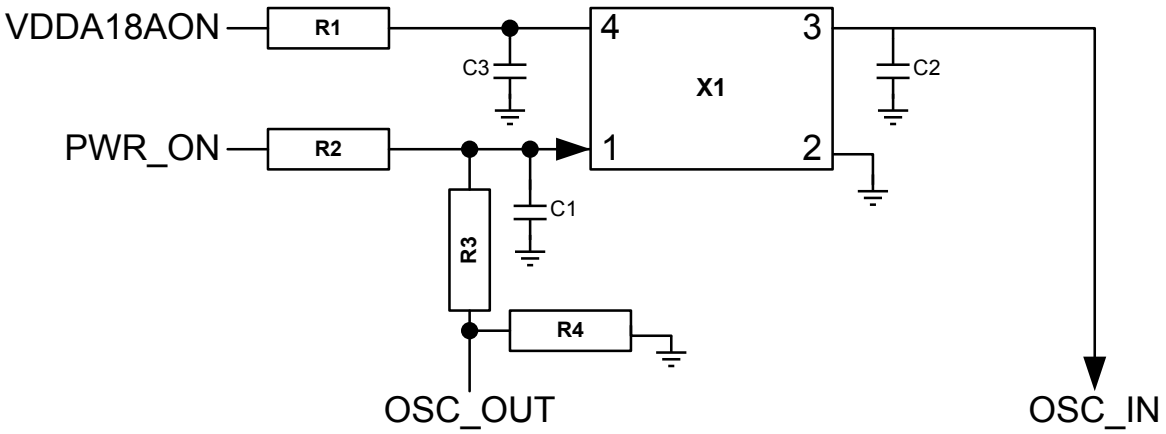


Table 15. HSE BOM for oscillator or crystal

Components	Oscillator (OSC_OUT = logic 0)	Crystal (OSC_OUT = crystal pin)
X1	NZ2016SH 40 MHz	NX2016SA 40 MHz
R1	10 Ω	- (open)
R2	10 KΩ / 30 KΩ(1)	- (open)
R3	- (open) / 33 KΩ(1)	0 Ω
R4	1 KΩ	- (open)
C1	- (open)	6.8 pF
C2	- (open)	6.8 pF
C3	10 nF	- (open)

1. *For respectively VDD = 1.8 V and VDD = 3.3 V. In case of VDD = 3.3 V, a resistor divider formed by R2/(R3+R4) is required as the oscillator pin 1 (Enable) must be limited to a VDDA18AON (1.8 V) voltage, which supplies the external oscillator.*

8.2 Reset

The NRST reset signal in Figure 2. Simplified reset pin circuit is active low. The reset sources include:

- Reset button
- Debugging tools via the JTAG connector

Refer to Section 2.4: Reset and power supply supervisor.

8.3 Boot mode

The boot option is configured by setting permanent wires or switches: SW4 (BOOT3), SW3 (BOOT2), SW2 (BOOT1) and SW1 (BOOT0) and internal OTP. Refer to Section 5: Boot configuration.

In case of the UART boot using one of the possible U(S)ARTx_RX pins (see Table 16) to avoid a floating signal sent to the host until the initialization character is received and decoded by the boot ROM, it is required to have a 10 kΩ V_{DD} pull-up on the respective U(S)ARTx_TX pin.

The U(S)ART_RX pin used for boot or system console should not be left floating to avoid dummy serial characters decoding. This could be ensured either by defining an internal pull-up in a uBoot/Linux device tree, or using a 10 kΩ VDD pull-up on the board.

The table below shows the default pins used for each boot interface.

Table 16. Minimum set of default pins used during boot ROM phase

Interface	type		Signal	Pin	IO supply domain
FMC	SLC NAND 8-bits	SLC NAND 16-bits	FMC_NOE	PE15	VDDIO2(1)
			FMC_RNB	PE13	
			FMC_NWE	PE14	
			FMC_NCE1	PE12	
			FMC_ALE	PE8	
			FMC_CLE	PE11	
			FMC_D0	PE9	
			FMC_D1	PE6	
			FMC_D2	PE7	
			FMC_D3	PD15	VDD
			FMC_D4	PD14	
			FMC_D5	PB13	
			FMC_D6	PD12	
			FMC_D7	PB14	
	-		FMC_D8	PB5	VDDIO4(2)
			FMC_D9	PB6	
			FMC_D10	PB7	
			FMC_D11	PD13	VDD
			FMC_D12	PB8	VDDIO4(2)
			FMC_D13	PB9	
			FMC_D14	PB11	
			FMC_D15	PB10	
OCTOSPIM Port1	Serial NOR, Serial NAND	HyperFlash™	OCTOSPIM_P1_CLK	PD0	VDDIO3
			OCTOSPIM_P1_NCS1	PD3	
			OCTOSPIM_P1_IO0	PD4	
			OCTOSPIM_P1_IO1	PD5	
	-		OCTOSPIM_P1_IO2	PD6	
			OCTOSPIM_P1_IO3	PD7	
			OCTOSPIM_P1_IO4	PD8	
			OCTOSPIM_P1_IO5	PD9	
			OCTOSPIM_P1_IO6	PD10	

Interface	type			Signal	Pin	IO supply domain
OCTOSPIM Port1	-		HyperFlash™	OCTOSPIM_P1_IO7	PD11	VDDIO3
				OCTOSPIM_P1_NCLK	PD1	
				OCTOSPIM_P1_DQS	PD2	
OCTOSPIM Port2	Serial NOR, Serial NAND		HyperFlash™	OCTOSPIM_P2_CLK	PB10	VDDIO4[2]
				OCTOSPIM_P2_NCS1	PB8	
				OCTOSPIM_P2_IO0	PB0	
				OCTOSPIM_P2_IO1	PB1	
	-			OCTOSPIM_P2_IO2	PB2	
				OCTOSPIM_P2_IO3	PB3	
				OCTOSPIM_P2_IO4	PB4	
				OCTOSPIM_P2_IO5	PB5	
				OCTOSPIM_P2_IO6	PB6	
				OCTOSPIM_P2_IO7	PB7	
				OCTOSPIM_P2_NCLK	PB11	
				OCTOSPIM_P2_DQS	PB9	
SDMMC1	SD-Card or eMMC			SDMMC1_CK	PE3	VDDIO1
				SDMMC1_CMD	PE2	
				SDMMC1_D0 [3]	PE4	
SDMMC2	SD-Card or eMMC			SDMMC2_CK	PE14	VDDIO2[1]
				SDMMC2_CMD	PE15	
				SDMMC2_D0[3]	PE13	
USART2				USART2_RX	PA8	VDD
				USART2_TX	PA4	
UART5				UART5_RX	PB15	VDD
				UART5_TX	PA0	
USART6				USART6_RX	PF4	VDD
				USART6_TX	PF5	
UART8				UART8_RX	PF3	VDD
				UART8_TX	PG3	
UART9				UART9_RX	PB14	VDD
				UART9_TX	PD13	
USB3DR	USB device			USB3DR_DP	USB3DR_DP	VDD33USB/ VDDA18USB
				USB3DR_DM	USB3DR_DM	
				USB3DR_TXRTUNE	USB3DR_TXRTUNE	

1. *Some FMC and SDMMC2 pins are shared, this means that usage of FMC is exclusive of usage of SDMMC2.*
2. *Some FMC and OCTOSPIM port2 pins are shared, this means that usage of FMC in 16-bit mode is exclusive of usage of OCTOSPIM Port2.*
3. *Only used as input by boot ROM*

8.4 SWD/JTAG interface

The reference design shows the connections between the STM32MP25xx devices and some standard connector (refer to Section 6: Debug management).

Note: If available, it is recommended to connect the debugger probe system reset pin to NRST. This action permits resetting the application from the debugger.

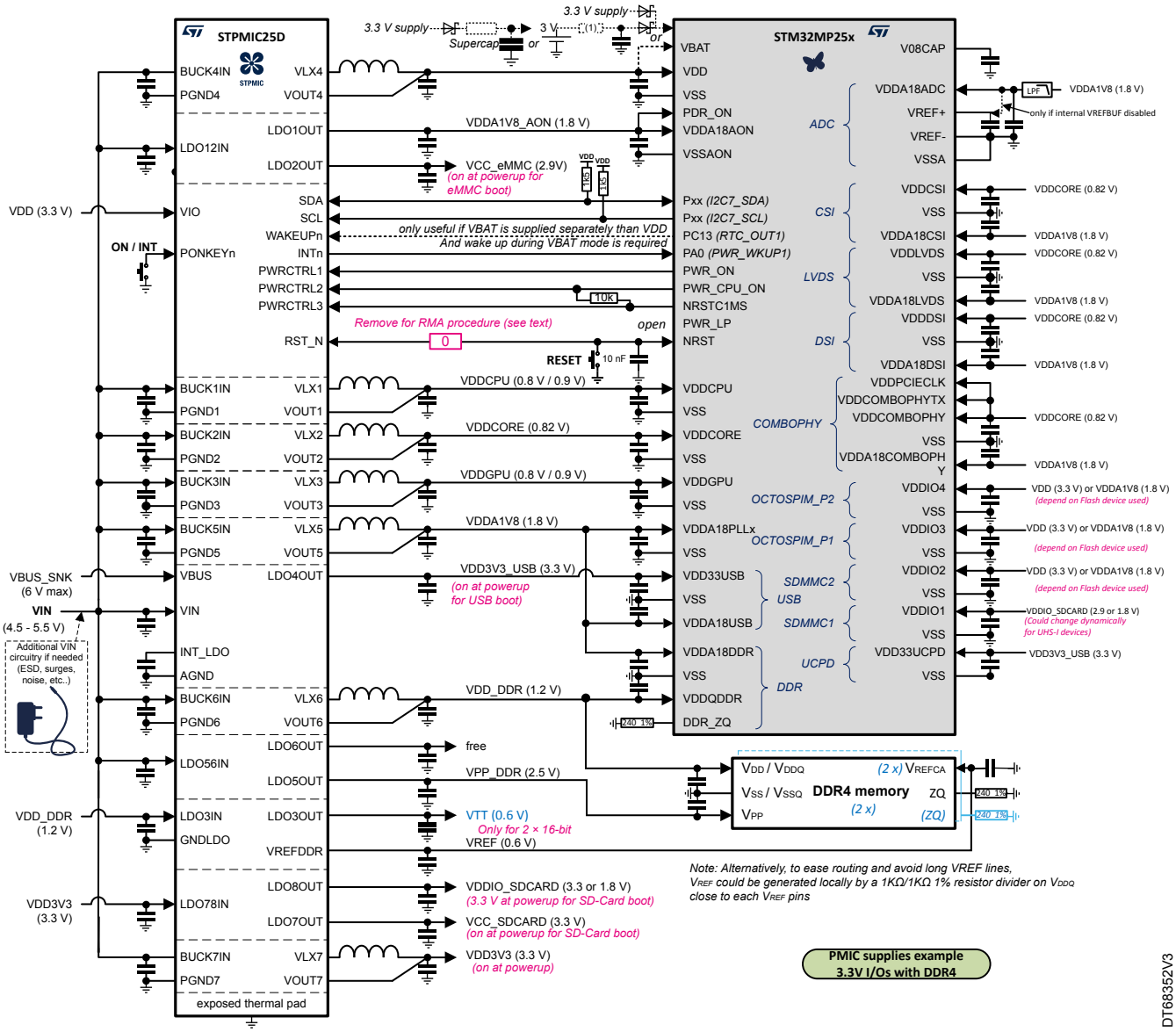
8.5 Power supply

The STPMIC25 automatically applies power cycling when its RST_N pin is activated (for example, button, system reset). However, in the case of entering an RMA state, the power cycling should not be done. A 0 Ω resistance between NRST and STPMIC25 RST_n pins could be provided and removed when using the procedure to enter an RMA state. Refer to Section 2: Power supplies.

8.5.1 Example of PMIC supplies for 3.3 V I/Os and DDR4

This reference design example targets a complex 3.3 V I/Os platform with DDR4 and high integration PMIC. Usually, all platform components can be powered by the PMIC. Full power supply control is supported thanks to PMIC I²C and side band signals. The Sleep mode, the Stop mode, and the Standby mode are supported. See PMIC documentation for details of PMIC components.

Figure 23. Example of PMIC supplies for 3.3 V I/Os and DDR4



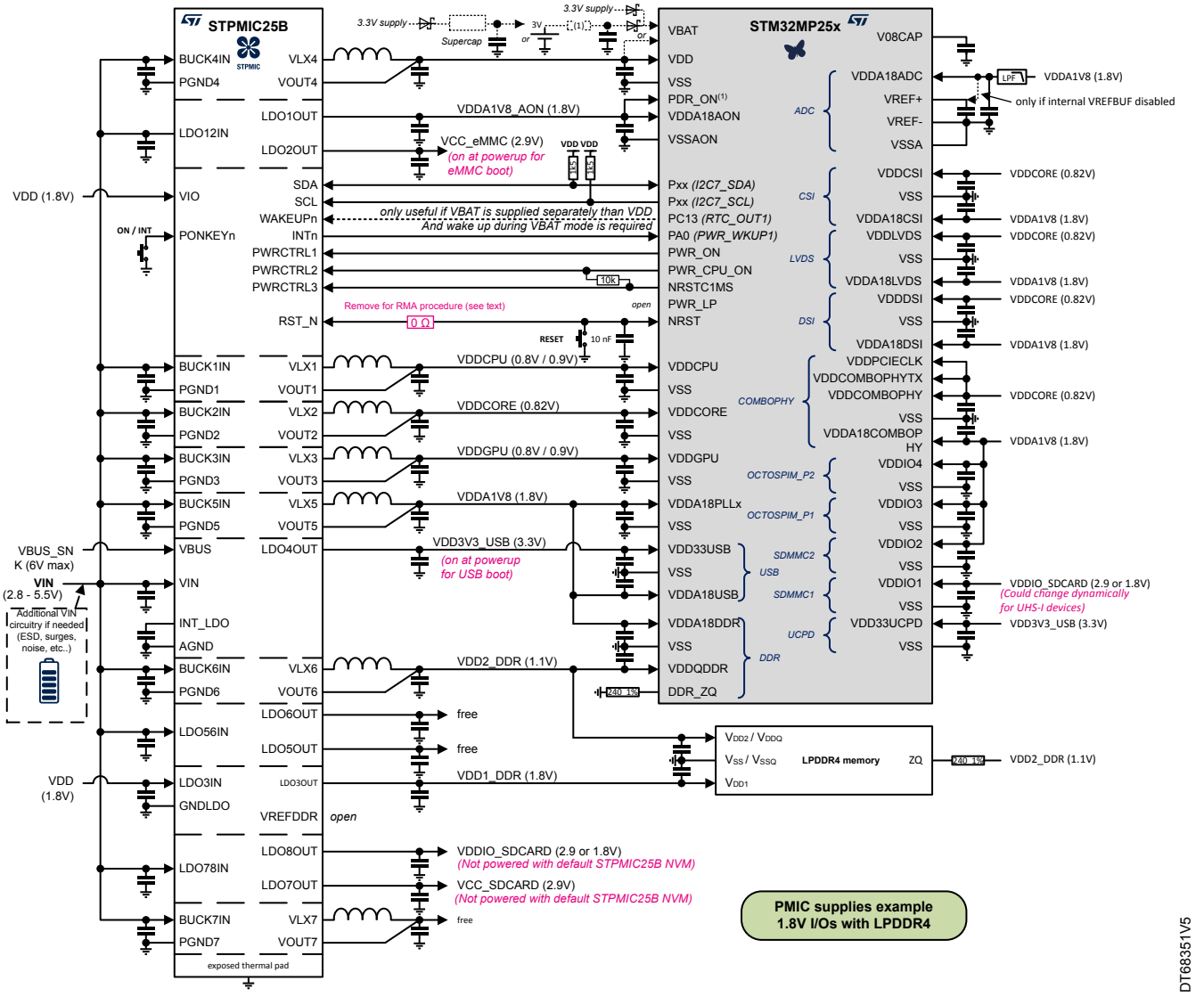
See Table 4. Amount of decoupling recommendation by package[23].

Note: On a same I²C bus, it is not possible to share I²C devices controlled from both secure and nonsecure software. For example: a secure software controls STPMIC2x in our standard deliveries and that STPMIC2x belongs to a distinct and secured I²C controller.

8.5.2 Example of PMIC supplies for 1.8 V I/Os with LPDDR4

This reference design example targets a complex 1.8 V I/Os platform with low power LPDDR4 and high integration PMIC. Usually, all platform components can be powered by the PMIC. The full power supply control is supported thanks to PMIC I²C and side band signals. The Sleep mode, the Stop mode, and the Standby mode are supported as well as very-low power standby with LPDDR4 retention. See PMIC documentation for details of PMIC components.

Figure 24. Example of PMIC supplies for 1.8 V I/Os with LPDDR4



1. *PDR_ON must always be connected to VDDA18AON.*

Note: SD card supplies are not enabled in the STPMIC25A and STPMIC25B default NVM after shipment. They need to be specifically programmed in the customer production flow (using USB or UART boot) to allow SD card boot. Alternatively, if no SD card UHS-I is required, instead of using LDO7 and LDO8, the SD card supplies (VDDIO_SDCARD and VCC_SDCARD) could be both connected to a 2.7-3.6 V supply enabled with default the STPMIC25x NVM (for example, BUCK7 or LDO2).

See Table 4. Amount of decoupling recommendation by package[23].

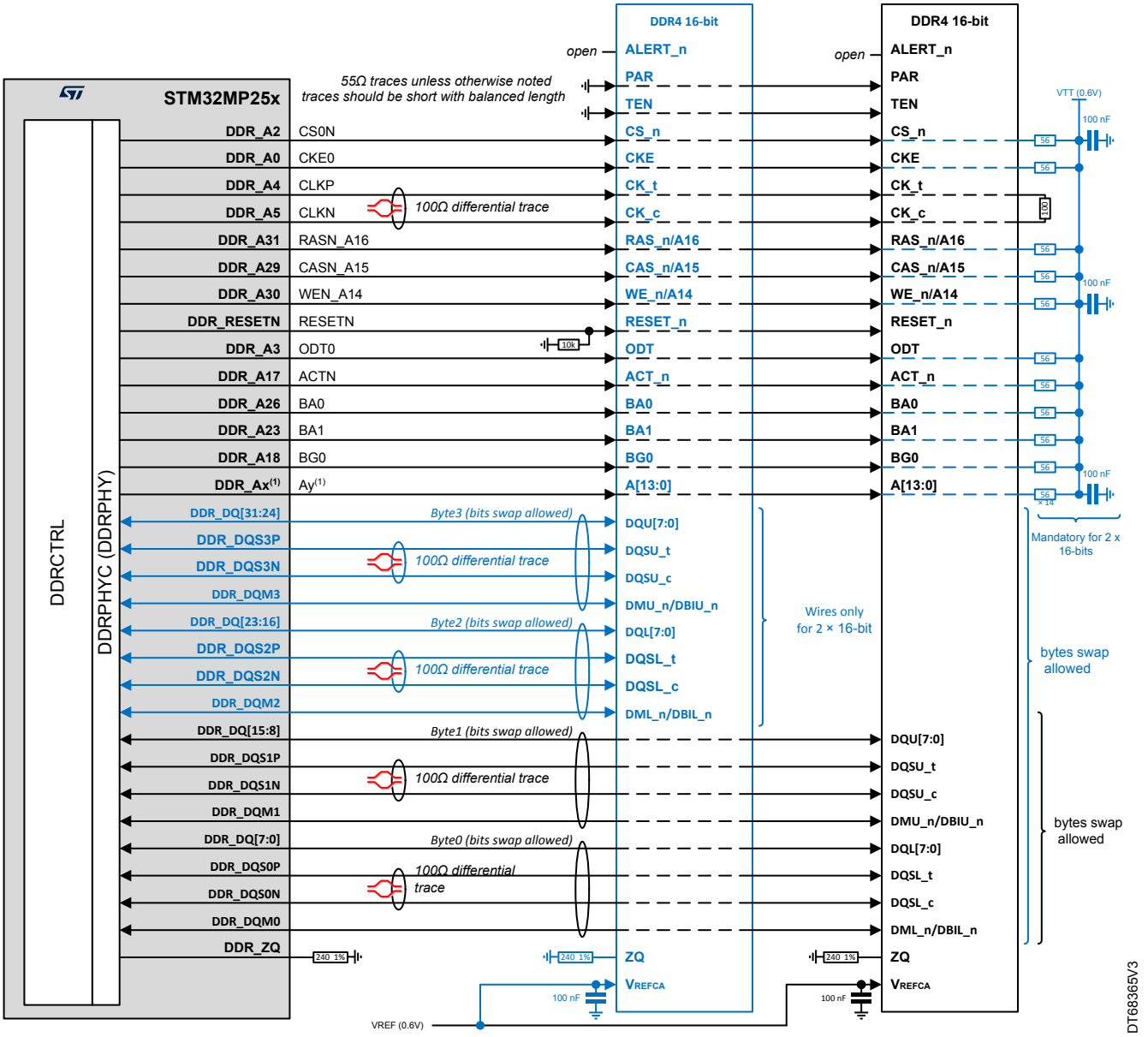
Note: On a given I²C bus, it is not possible to share I²C devices controlled from both secure and nonsecure software. For example, secure software controls the PMIC in our standard deliveries and that PMIC belongs to a distinct and secured I²C .

8.6 DDR4 SDRAM

A 240 Ω 1% resistor should be connected between DDR_ZQ and V_{SS}. This resistor must not be shared with the ZQ resistors required on each DDR4 component.

In case of a 2x16-bit device, the impedance matching resistor network connected on the termination voltage (VTT) supply must be placed as close as possible to the last device. 'Fly-by' routing techniques must be used to avoid any impedance discontinuities. Values in the example below should work in most cases, but could be tailored to each side I/O drive strengths and PCB impedance.

Figure 25. DDR4 16/32 bits connection example



Note:

1. *See the table below.*
2. *Alternatively, to ease routing and avoid long V_{REF} lines, V_{REF} can be generated locally by a 1 kΩ or 1 kΩ 1% resistor divider on V_{DDQ} close to each VREF pin.*
3. *Supplies and decoupling capacitors are not shown.*
4. *Detailed routing examples are described in the corresponding application note [6].*

Table 17. DDR4 2x16-bit default pin mapping(1)

DDRCTRL pin	Signal name	DDR4 x16 #1	DDR4 x16 #2 (2)	Comments
DDR_RESETN	RESETN	RESET_n	RESET_n	10k pull-down to memory VSS
DDR_ZQ	-	-	-	240 Ω 1% to VSS
-	-	ZQ	-	240 Ω 1% to memory VSS
-	-	-	ZQ	240 Ω 1% to memory VSS
DDR_VREF	-	-	-	Not used, it should be left open.
-	VREF	VREFCA	VREFCA	0.6 V reference voltage
-	-	PAR	PAR	Not used, it should be connected to memory VSS.
-	-	TEN	TEN	
-	-	ALERT_n	ALERT_n	Not used, it should be left open.
DDR_A0	CKE0	CKE	CKE	-
DDR_A1	-	-	-	Not used, it should be left open.
DDR_A2	CS0N	CS_n	CS_n	-
DDR_A3	ODT0	ODT	ODT	-
DDR_A4	CLKP	CK_t	CK_t	-
DDR_A5	CLKN	CK_c	CK_c	-
DDR_A6	-	-	-	Not used, it should be left open.
DDR_A7	-	-	-	Not used, it should be left open.
DDR_A8	A9	A9	A9	-
DDR_A9	A12_BCN	A12/BC_n	A12/BC_n	-
DDR_A10	A11	A11	A11	-
DDR_A11	A7	A7	A7	-
DDR_A12	A8	A8	A8	-
DDR_A13	A6	A6	A6	-
DDR_A14	A5	A5	A5	-
DDR_A15	A4	A4	A4	-
DDR_A16	BG1	-	-	BG1 is not used on DDR4 x16 or DDR4 x32, but DDR_A16 pin could be selected for another DDR4 signal than the default one. See note (1).
DDR_A17	ACTN	ACT_n	ACT_n	-
DDR_A18	BG0	BG0	BG0	-
DDR_A19	not used	-	-	Not used, it should be left open.
DDR_A20	A3	A3	A3	-
DDR_A21	A2	A2	A2	-
DDR_A22	A1	A1	A1	-
DDR_A23	BA1	BA1	BA1	-
DDR_A24	does not exist	-	-	-
DDR_A25	A13	A13	A13	-
DDR_A26	BA0	BA0	BA0	-
DDR_A27	A10_AP	A10/AP	A10/AP	-
DDR_A28	A0	A0	A0	-
DDR_A29	CASN_A15	CAS_n/A15	CAS_n/A15	-

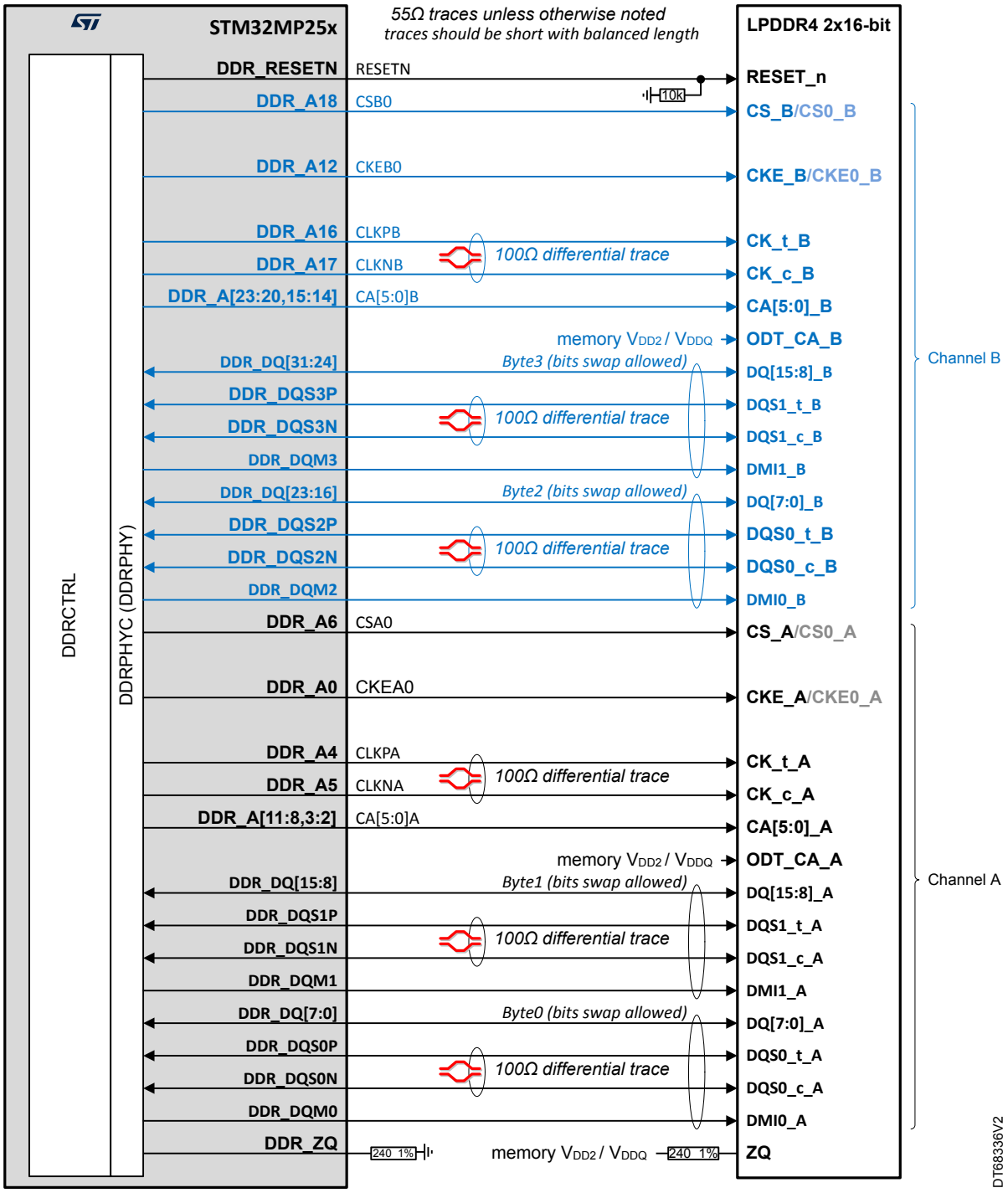
DDRCTRL pin	Signal name	DDR4 x16 #1	DDR4 x16 #2 (2)	Comments	
DDR_A30	WEN_A14	WE_n/A14	WE_n/A14	-	
DDR_A31	RASN_A16	RAS_n/A16	RAS_n/A16	-	
DDR_DQ[31:24]	DQ[31:24]	-	DQU[7:0]	Data bits could be swapped within a same byte	Byte3 could be swapped with other bytes (3)
DDR_DQM3	DQM3	-	DMU_n/DBIU_n		
DDR_DQS3P	DQS3P	-	DQSU_t		
DDR_DQS3N	DQS3N	-	DQSU_c		
DDR_DQ[23:16]	DQ[23:16]	-	DQL[7:0]	Data bits could be swapped within a same byte	Byte2 could be swapped with other bytes (3)
DDR_DQM2	DQM2_DBIL2	-	DML_n/DBIL_n		
DDR_DQS2P	DQS2P	-	DQSL_t		
DDR_DQS2N	DQS2N	-	DQSL_c		
DDR_DQ[16:8]	DQ[15:8]	DQU[7:0]	-	Data bits could be swapped within a same byte	Byte1 could be swapped with other bytes (3)
DDR_DQM1	DQM1	DMU_n/DBIU_n	-		
DDR_DQS1P	DQS1P	DQSU_t	-		
DDR_DQS1N	DQS1N	DQSU_c	-		
DDR_DQ[7:0]	DQ[7:0]	DQL[7:0]	-	Data bits could be swapped within a same byte	Byte0 could be swapped with other bytes (3)
DDR_DQM0	DQM0	DML_n/DBIL_n	-		
DDR_DQS0P	DQS0P	DQSL_t	-		
DDR_DQS0N	DQS0N	DQSL_c	-		

1. *DDR_A8 to DDR_A31 pin mapping can be tailored by software. See the application note Guidelines for the DDR configuration on STM32MP2 MPUs (AN5723).*
2. *Only for 2x 16 bits*
3. *For a given 32-bit platform with two memory devices, if an option is foreseen for BOM reduction to a single 16-bit memory device, then Byte0 and Byte1 must be connected to this device.*

8.7 LPDDR4 SDRAM

A 240 Ω 1% resistor should be connected between DDR_ZQ and V_{SS}. This resistor must not be shared with one or more ZQ resistors required on the LPDDR4 component.

Figure 26. LPDDR4 connection example



Note: 1. *Supplies and decoupling capacitors are not shown.*
2. *Detailed routing examples are described in the corresponding application note [6].*

Table 18. **LPDDR4 pin mapping**[1]

DDRCTRL pin	Signal name	LPDDR4	Comments
DDR_RESETN	RESETN	RESET_n	10k pull-down to memory VSS
DDR_ZQ	-	-	240 ohms 1% to VSS
-	-	ZQ0	240 ohms 1% to memory VDD2/VDDQ
-	-	ODT_CA_A	Should be connected to memory VDD2/VDDQ (CA terminations enabled by default, could be disabled later inside memory settings)
-	-	ODT_CA_B	
DDR_VREF	-	-	-[2]
DDR_A0	CKEA0	CKE0_A	-
DDR_A1	-	-	-[2]
DDR_A2	CA0A	CA0_A	-[3]
DDR_A3	CA1A	CA1_A	
DDR_A4	CLKPA	CK_t_A	-
DDR_A5	CLKNA	CK_c_A	-
DDR_A6	CSA0	CS0_A	-
DDR_A7	-	-	-[2]
DDR_A8	CA2A	CA2_A	-[3]
DDR_A9	CA3A	CA3_A	
DDR_A10	CA4A	CA4_A	
DDR_A11	CA5A	CA5_A	
DDR_A12	CKEB0	CKE0_B	-
DDR_A13	-	-	-[2]
DDR_A14	CA0B	CA0_B	-[4]
DDR_A15	CA1B	CA1_B	
DDR_A16	CLKPB	CK_t_B	-
DDR_A17	CLKNB	CK_c_B	-
DDR_A18	CSB0	CS0_B	-
DDR_A19	-	-	-[2]
DDR_A20	CA2B	CA2_B	-[4]
DDR_A21	CA3B	CA3_B	
DDR_A22	CA4B	CA4_B	
DDR_A23	CA5B	CA5_B	
DDR_A24	does not exist	-	-[2]
DDR_A25	-	-	
DDR_A26	-	-	
DDR_A27	-	-	
DDR_A28	-	-	
DDR_A29	-	-	
DDR_A30	-	-	
DDR_A31	-	-	

DDRCTRL pin	Signal name	LPDDR4	Comments
DDR_DQ[31:24]	DQ[31:24]	DQ[15:8]_B	Data bits could be swapped within a same byte with adequate DDRPHYC_DBYTE[3:0]_DQ[7:0]LNSEL setting inside DDRPHYC. Byte lanes within a channel (0 and 1 or 2 and 3) can be swapped on PCB with adequate programming of DDRCTRL_REGS_DERATEEN.DERATE_BYTE used for MR4 polling by DDRCTRL for temperature derating refresh. The default setting is 0 for MR4 read using DDR_DQ[7:0]. Swapping byte lanes between channels is not allowed.
DDR_DQM3	DQM3	DMI1_B	
DDR_DQS3P	DQS3P	DQS1_t_B	
DDR_DQS3N	DQS3N	DQS1_c_B	
DDR_DQ[23:16]	DQ[23:16]	DQ[7:0]_B	
DDR_DQM2	DQM2_DBIL2	DMI0_B	
DDR_DQS2P	DQS2P	DQS0_t_B	
DDR_DQS2N	DQS2N	DQS0_c_B	
DDR_DQ[16:8]	DQ[15:8]	DQ[15:8]_A	
DDR_DQM1	DQM1	DMI1_A	
DDR_DQS1P	DQS1P	DQS1_t_A	
DDR_DQS1N	DQS1N	DQS1_c_A	
DDR_DQ[7:0]	DQ[7:0]	DQ[7:0]_A	
DDR_DQM0	DQM0	DMI0_A	
DDR_DQS0P	DQS0P	DQS0_t_A	
DDR_DQS0N	DQS0N	DQS0_c_A	

1. *Some DDR_Ax pin mapping can be tailored by software. See the application note Guidelines for the DDR configuration on STM32MP2 MPUs (AN5723).*
2. *Not used, it must be left open.*
3. *Address/Command lines can be swapped with other CAx_A using MapCAA[0to5]toDfi setting inside DDRPHYC.*
4. *Address/Command lines could be swapped with other CAx_B using MapCAB[0to5]toDfi setting inside DDRPHYC.*

8.8 SD card

Note: As boot is always done in 'Standard' mode (3 V IOs), if the card is used by the application in UHS-I, a power cycle on the card supply is required after a Reset mode or Standby mode. NRSTC1MS could be used for that purpose.

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers) and V_{DD} voltage.

When using V_{DDIO1} = 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on pins used on SDMMC1 outputs.

If needed, the impedance matching resistor should be placed as close as possible of the output driver pin. Values in the example below should work in most cases, but could be tailored to IO drive strengths and PCB impedance.

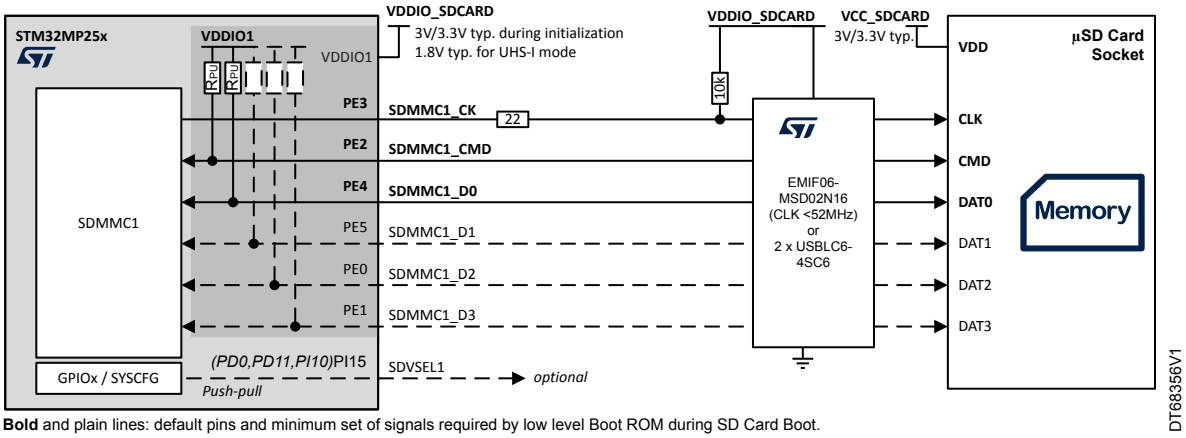
Before the V_{CC_SDCARD} shutdown (for example before a Standby mode), all signals going to the card must be set to 0 or high-Z by the SDMMC1 driver.

The example is independent from MPU I/O voltage V_{DD} and relies on variable VDDIO1 that could be set, either to 3.0 V/3.3 V, or 1.8 V typ. using one of the followings:

- SDVSEL1 ('0' or high-Z = 3 V/3.3 V (default), '1' = 1.8 V) connected to an external regulator or other component managing the V_{DDIO1} voltage.
- A regular GPIO output connected to an external regulator or other component managing the V_{DDIO1} voltage.
- An I²C bus in case of use with PMIC.

If a programmable V_{DDIO_SDCARD} is not available in the platform, V_{DDIO1} could be connected to V_{CC_SDCARD}. In that case, UHS-I is not supported.

Figure 27. SD-Card with embedded level shifter connection



Bold and plain lines: default pins and minimum set of signals required by low level Boot ROM during SD Card Boot.

Note: When switching to UHS-I mode (V_{DDIO1} = 1.8V), VDDIOxVRSEL should be set only when V_{DDIO1} is within the 1.8V allowed range. In case of reset of the SD-Card to the legacy 3V/3.3V range, to avoid damage on the I/Os, VDDIOxVRSEL should be cleared before the voltage is outside the 1.8V allowed range.

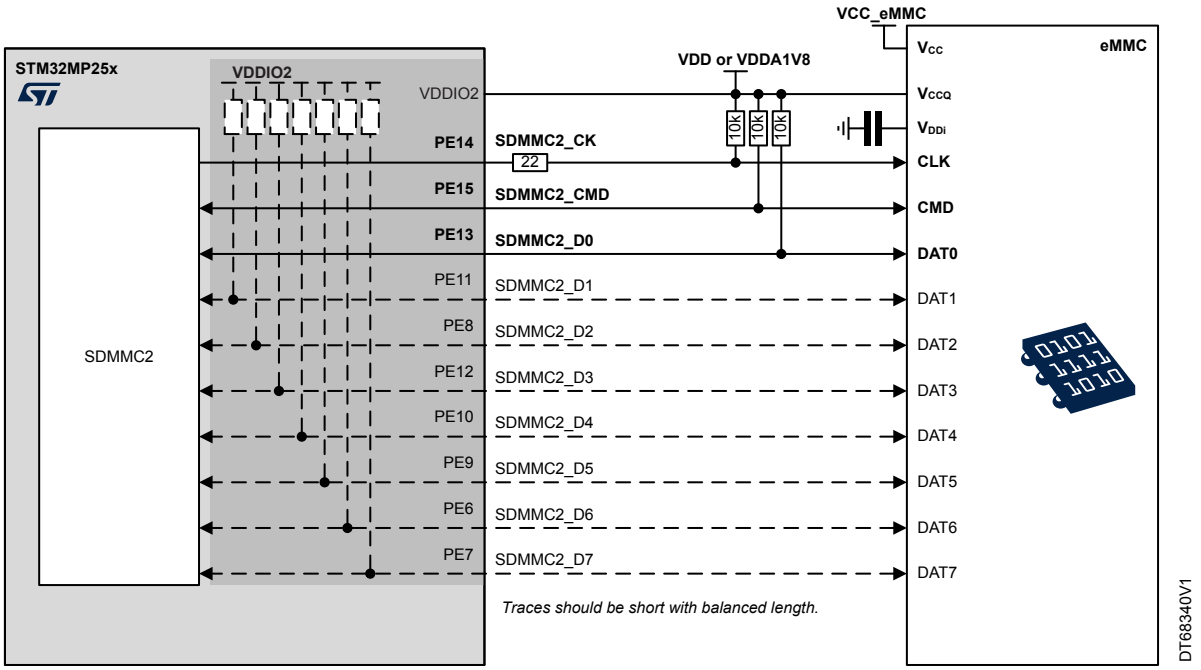
8.9 eMMC™ flash

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DDIO2} voltage.

When using V_{DDIO2} = 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on pins used on SDMMC2 outputs.

If needed, the impedance matching resistor should be placed as close as possible of the output driver pin. Values in the example below should work in most cases, but could be tailored to IO drive strengths and PCB impedance.

Figure 28. eMMC™ connection example



Note:

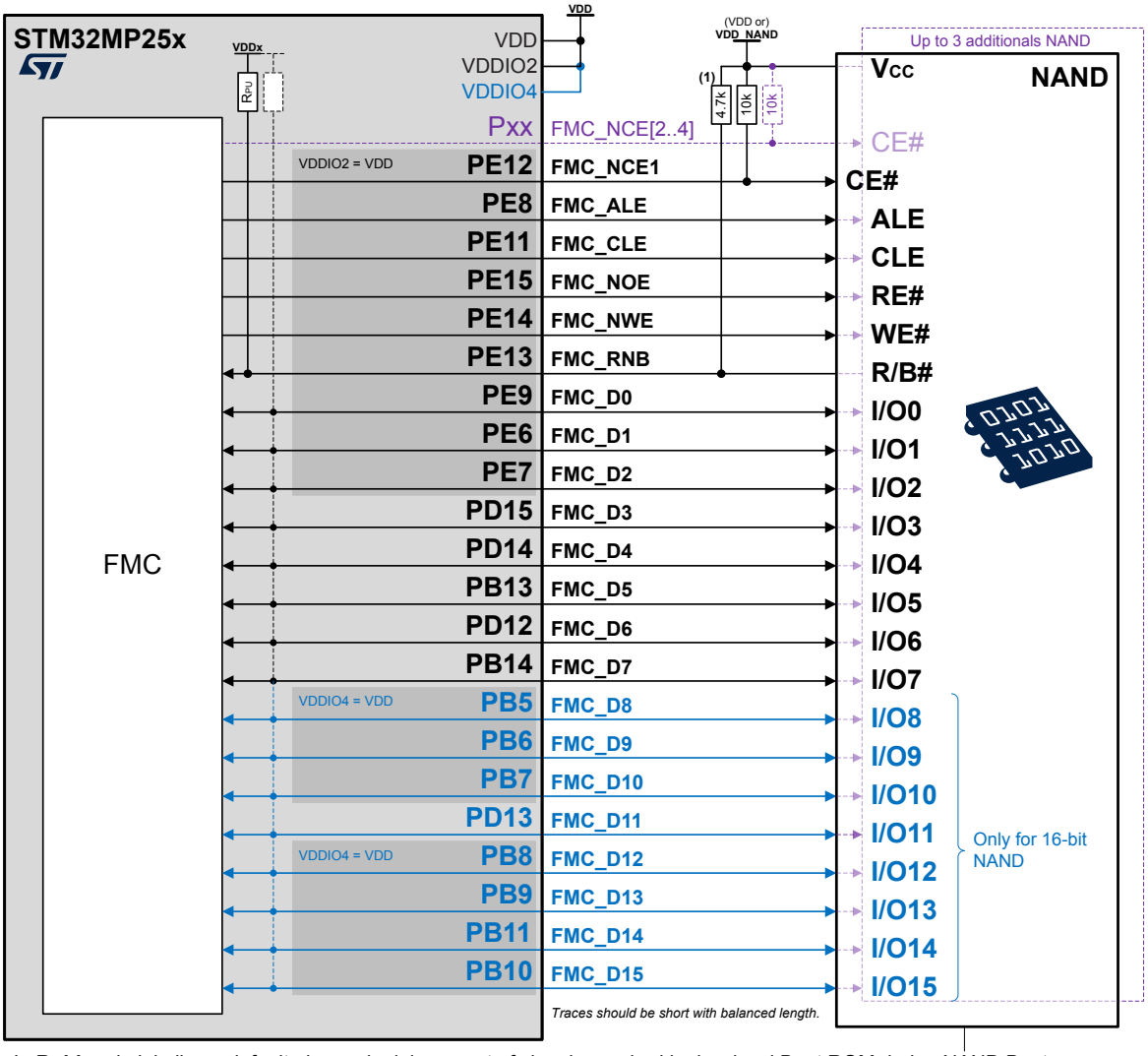
1. *In bold and plain lines, default pins and minimum set of signals required by low level boot ROM during eMMC boot.*
2. *Decoupling capacitors are not shown.*

8.10 SLC NAND flash memory

Up to four 8 or 16-bit SLC NAND memory devices (CE# = FMC_NCE1, FMC_NCE2, FMC_NCE3 or FMC_NCE4) are supported.

Note that boot is only done on the SLC NAND memory device connected to FMC_NCE1.

Figure 29. SLC NAND flash memory connection



In **Bold** and plain lines, default pins and minimum set of signals required by low level Boot ROM during NAND Boot.

Note:

1. *Pull-up on FMC_RNB is optional. The 4.7kΩ value (lower than internal R_{PU}) could give better signal rise time that could reduce the wait time seen by FMC.*
2. *NAND flash memory V_{CC} supply (V_{DD_NAND}) must be cut for >1ms in order to allow reboot (on Reset or Standby mode exit). See NAND flash memory device for details.*
3. *Decoupling capacitors are not shown.*
4. *Only single level cell (SLC) NAND flash memory is supported, with either hamming, BCH4 or BCH8 error correction algorithms.*

8.11 Serial NOR/NAND flash

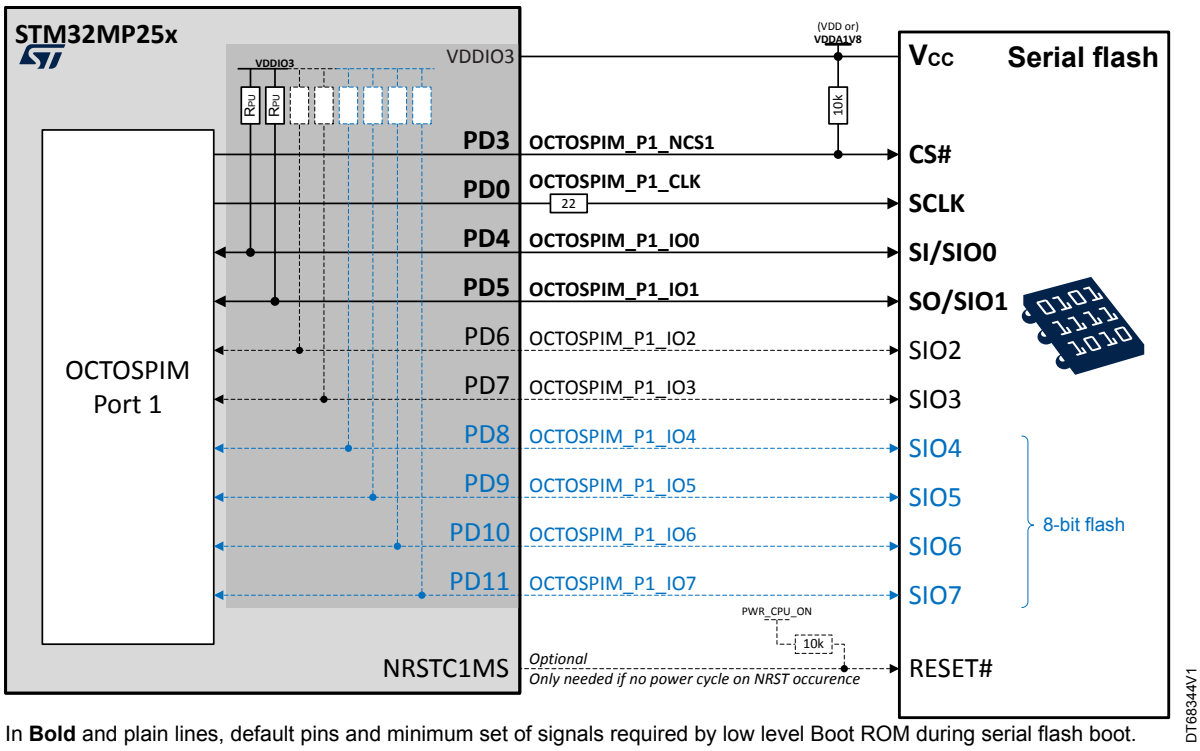
As boot is always done in SPI mode, if the serial flash memory is set by the application in multiple data lines, or if the sector addressing has been changed, a power cycle on a serial flash memory supply is required after Reset or Standby mode exit.

Note: A good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DDIO3} (or V_{DDIO4}) voltage.

When using V_{DDIO3} (or V_{DDIO4})= 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on pins used on OCTOSPIM outputs.

If needed, the impedance matching resistor must be placed as close as possible of the output driver pin. Values in the example below work in most cases, but can be tailored to I/O drive strengths and PCB impedance.

Figure 30. Serial flash memory connection example



In **Bold** and plain lines, default pins and minimum set of signals required by low level Boot ROM during serial flash boot.

Note:

1. *If RESET# is not connected, the serial flash memory supply (VCC) must be cut for >1ms in order to allow reboot (on reset or standby exit). See serial flash memory device documentation for details.*
2. *Decoupling capacitors are not shown.*
3. *During SPI mode boot using SI/SO, some serial memories could use I/O2 and I/O3 pins as an additional feature like HOLD. In order to make this device boot, it might be necessary to set those pins to an inactive level by adding external pull-ups.*

In case the memory I/O power supply VCC could be shut down independently than VDD, and NRSTC1MS is used for other purposes or other voltages on the platform, NRSTC1MS must not be directly connected to the memory reset pin and the following options could be used:

- Memory reset pin left open (assuming the memory has an internal power on reset and the NRSTC1MS is used to generate a power cycle on the memory)
- Connected through a Schottky diode with the cathode on the NRSTC1MS side

Otherwise, the NRSTC1MS might be pulled low by memory internal protections when memory I/O supply is not present (which could cause some unwanted reset of other platform devices using the NRSTC1MS pin).

Refer to memory documentation to verify the memory reset pin requirements: especially the presence of internal power on reset and/or internal pull-up on the reset pin).

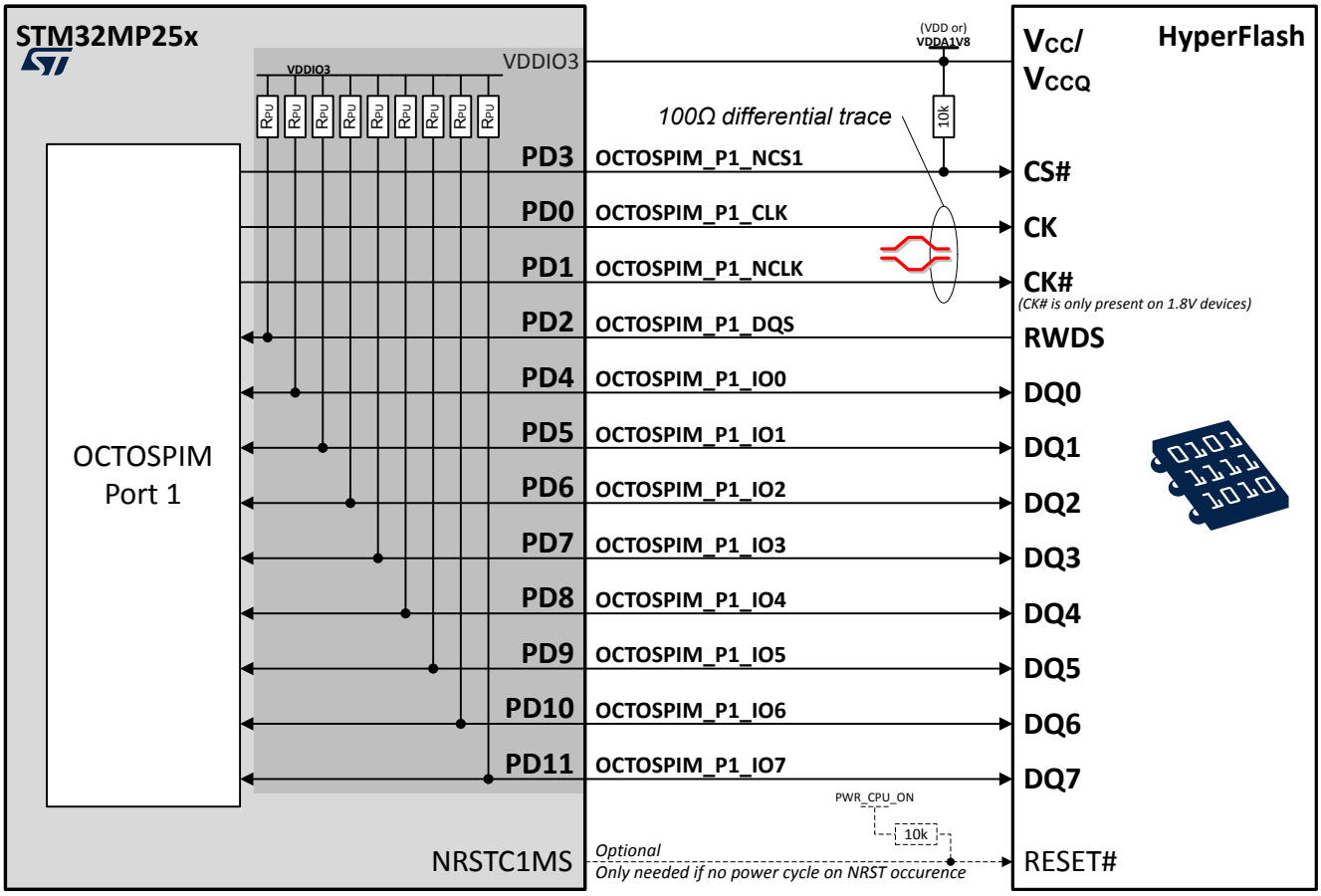
8.12 HyperFlash™

Note: If the serial flash memory mode set by the application is not compatible with the expected mode by the boot ROM, a power cycle on the serial flash memory supply is required after Reset or Standby mode exit. NRSTC1MS could be used for that purpose.

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DDIO3} (or V_{DDIO4}) voltage.

When using V_{DDIO3} (or V_{DDIO4}) = 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on pins used on OCTOSPIM outputs.

Figure 31. HyperFlash™ connection example



In **Bold** and plain lines, default pins and minimum set of signals required by low level Boot ROM during serial flash boot.

Note:

1. *If RESET# is not connected, HyperFlash™ supply (V_{CC}/V_{CCQ}) must be cut for >1ms in order to allow reboot (on Reset or Standby mode exit). See HyperFlash™ device documentation for details.*
2. *Decoupling capacitors are not shown.*

8.13 USB

Multiple USB options are possible. Examples are listed below:

- 1 × hi-speed USB device (Figure 32 or Figure 33)
- 1 × hi-speed USB device (Figure 32 or Figure 33) + 1 × USB hi-speed host (Figure 34)
- 1 × SuperSpeed USB host (Figure 35), see note below
- 1 × SuperSpeed USB dual-role (Figure 36)
- 1 × SuperSpeed USB dual-role (Figure 36) + 1 × USB hi-speed host (Figure 34)

Multiple hi-speed USB hosts using an external USB hub component is not described here.

Note: In case of on-board flash memory programming using the STM32CubeProgrammer, at least one USB with device capabilities is required. This is achieved with Figure 32, Figure 33, or Figure 36 and with some constrains, Figure 35. See also Section 8.13.4: USB high-speed/SuperSpeed dual role with Type-C connector (USB3DR).

Table 19. USB high-speed PCB routing recommendations

Recommendation	Min	Typ	Max	Unit
Differential impedance	76.5	90	103.5	Ω
Single-ended impedance	38.25	45	51.75	Ω
Length matching within a pair (including package(1))	-50	-	+50	mils
	-1.27	-	+1.27	mm
Max traces length (up to connector or first active component)	-	-	8	inches
	-	-	203	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		-(2)
Do no route over power plane split. No stubs (point to point only). No right angles				

1. *See Section 8.19 for PCB track length matching details.*
2. *Definition could be found, for instance, in the DDR memory routing guidelines ([6]).*

For USB SuperSpeed COMBOPHY PCB routing recommendations, see Section 8.14: PCI Express (PCIE).

8.13.1 USB hi-speed device (USB3DR)

A 200 Ω 1% resistor should be connected between USB3DR_TXRTUNE and V_{SS}.

Refer to the application note [15] for details on VBUS detection with GPIO.

Figure 32. USB hi-speed device with Micro-B connector example

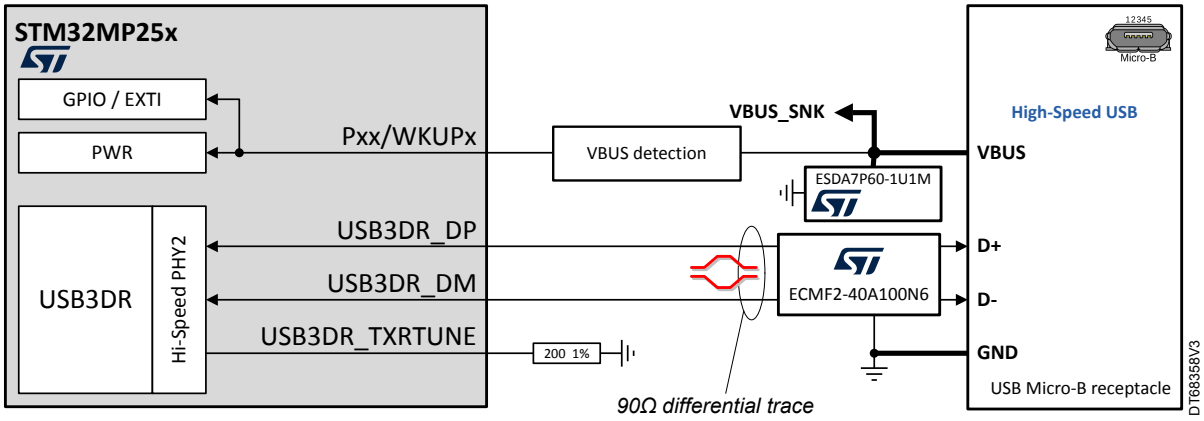
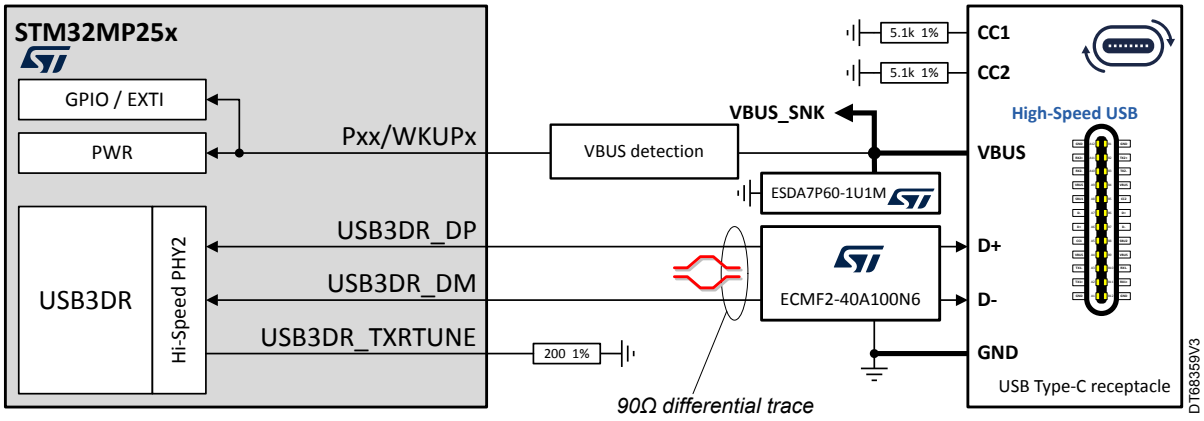


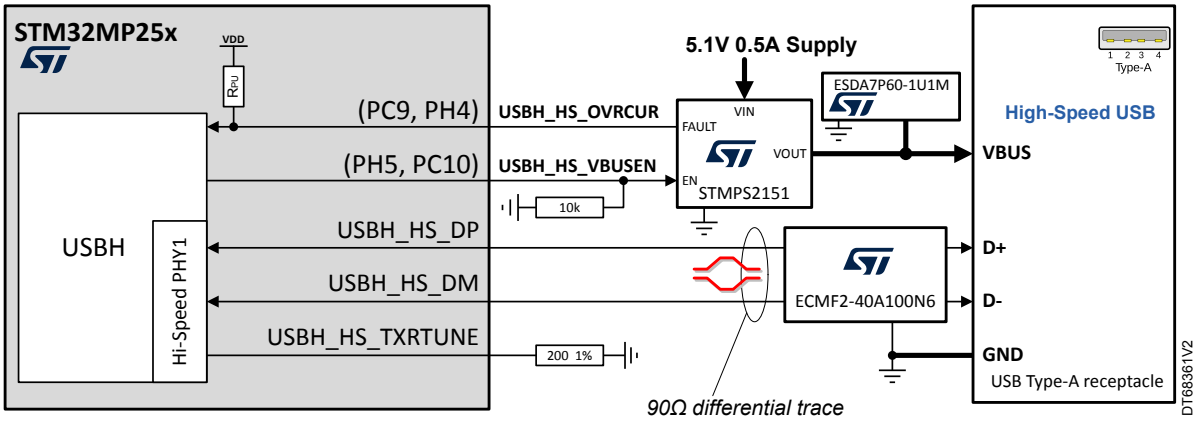
Figure 33. USB hi-speed device with Type-C connector example



8.13.2 USB hi-speed host with Type-A connector (USBH)

A 200 Ω 1% resistor should be connected between USBH_HS_TXRTUNE and V_{SS}.

Figure 34. USB hi-speed host example



Note: VBUS 1A is also possible using STMPS2171 instead of STMPS2151.

8.13.3 USB SuperSpeed host with Type-A connector (USB3DR)

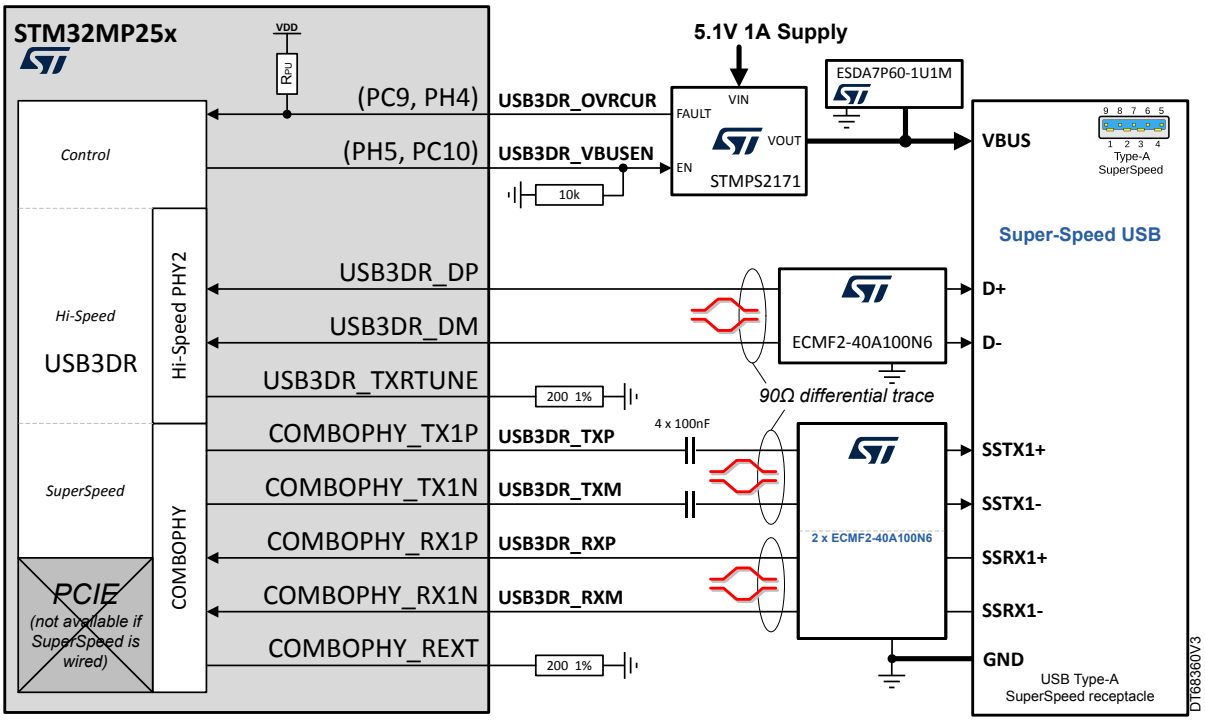
A 200 Ω 1% resistor should be connected between USB3DR_TXRTUNE and V_{SS}.

A 200 Ω 1% resistor should be connected between COMBOPHY_REXT and V_{SS}.

Note: As PCI-Express (PCIE) and USB SuperSpeed (USB3DR SuperSpeed link) share the same I/Os (COMBOPHY pins), their usage is exclusive and defined during user product definition.

Note: USB3DR hi-speed device is required by boot ROM when connected to a PC computer running a STM32CubeProgrammer in USB mode, for example, to program board flash memory devices. This is still possible with this USB SuperSpeed host use-case by using a nonstandard Type-A/Type-A USB hi-speed cable. It is possible only during STM32CubeProgrammer usage, and might need specific uBoot settings to allow this nonstandard usage.

Figure 35. USB SuperSpeed host connection example



8.13.4 USB high-speed/SuperSpeed dual role with Type-C connector (USB3DR)

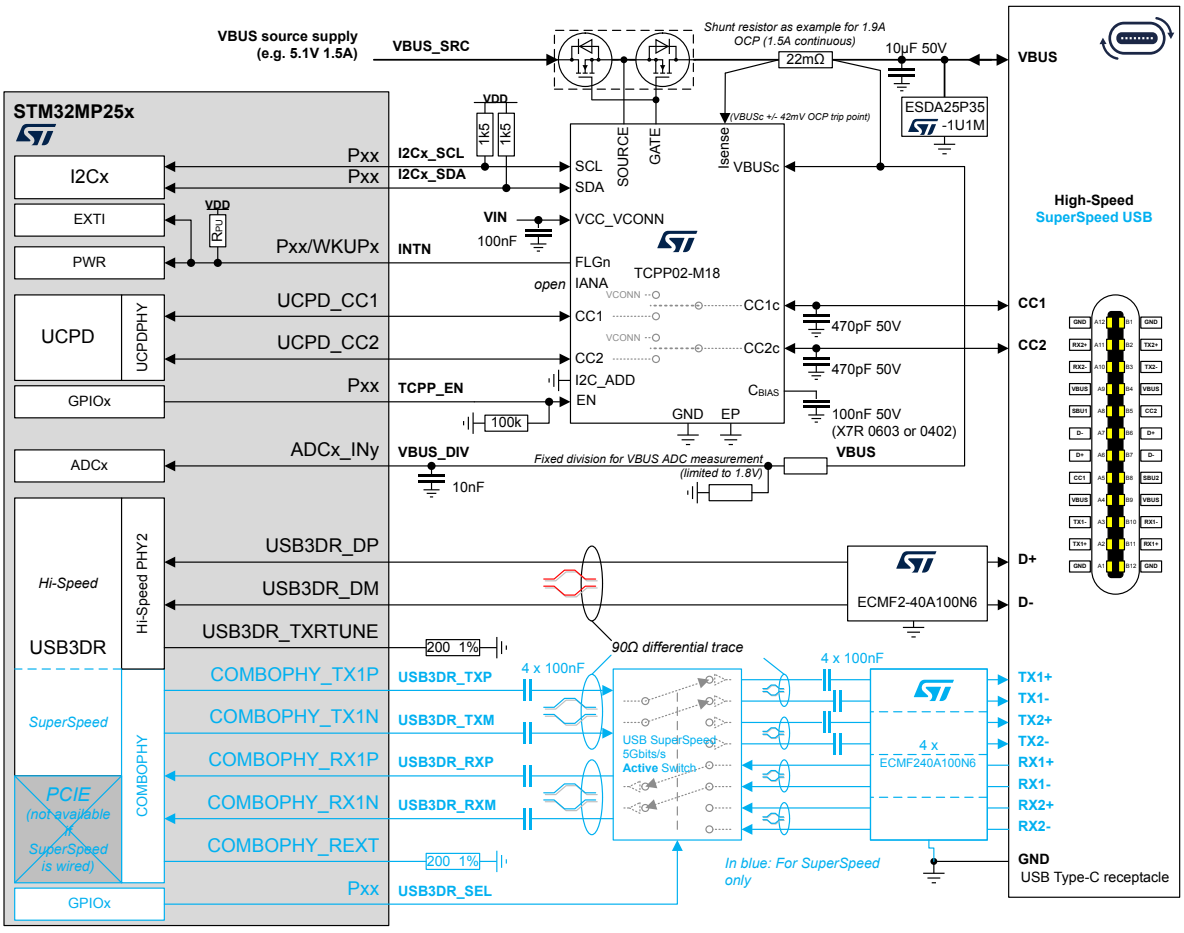
This example supports dual role data (host or device) as well as a USB Power Delivery protocol on Common Criteria lines using UCPD.

A 200 Ω 1% resistor should be connected between USB3DR_TXRTUNE and V_{SS}.

A 200 Ω 1% resistor should be connected between COMBOPHY_REXT and V_{SS} (if SuperSpeed is used).

Note: As PCI-Express (PCIE) and USB SuperSpeed (USB3DR SuperSpeed link) share the same I/Os (COMBOPHY pins), their usages are exclusive and defined during user product definition.

Figure 36. USB hi-speed/SuperSpeed dual role connection example



VBUS fixed divider should be tailored from the expected VBUS voltage to keep the ADC input voltage below 1.8V. Typical value of the divider is 1/15 (for VBUS up to 20V) or 1/30 (for VBUS up to 48V).

The maximum limit for VCONN in TCPP02 is 100mW. However, this reference cannot be used in complete compliance with USB SuperSpeed because the USB specification requires VCONN to provide at least 1W. Contact STMicroelectronics for latest recommended parts.

After power-up, TCPP02 does not advertise itself on CC1/CC2 lines as a Type-C UFP. A Type-A to Type-C cable might be necessary for flash memory programming sequence to ensure the host computer to act as a DFP and initiate the enumeration process required for boot ROM USB boot.

Note:

1. *See TCPP02-M18 documentation for more details.*
2. *On a same I²C bus, it is not possible to share I²C devices controlled from both secure and nonsecure software. For example, a secure software controls STPMIC25 in our standard deliveries and that STPMIC25 belongs to a distinct and secured I²C master.*

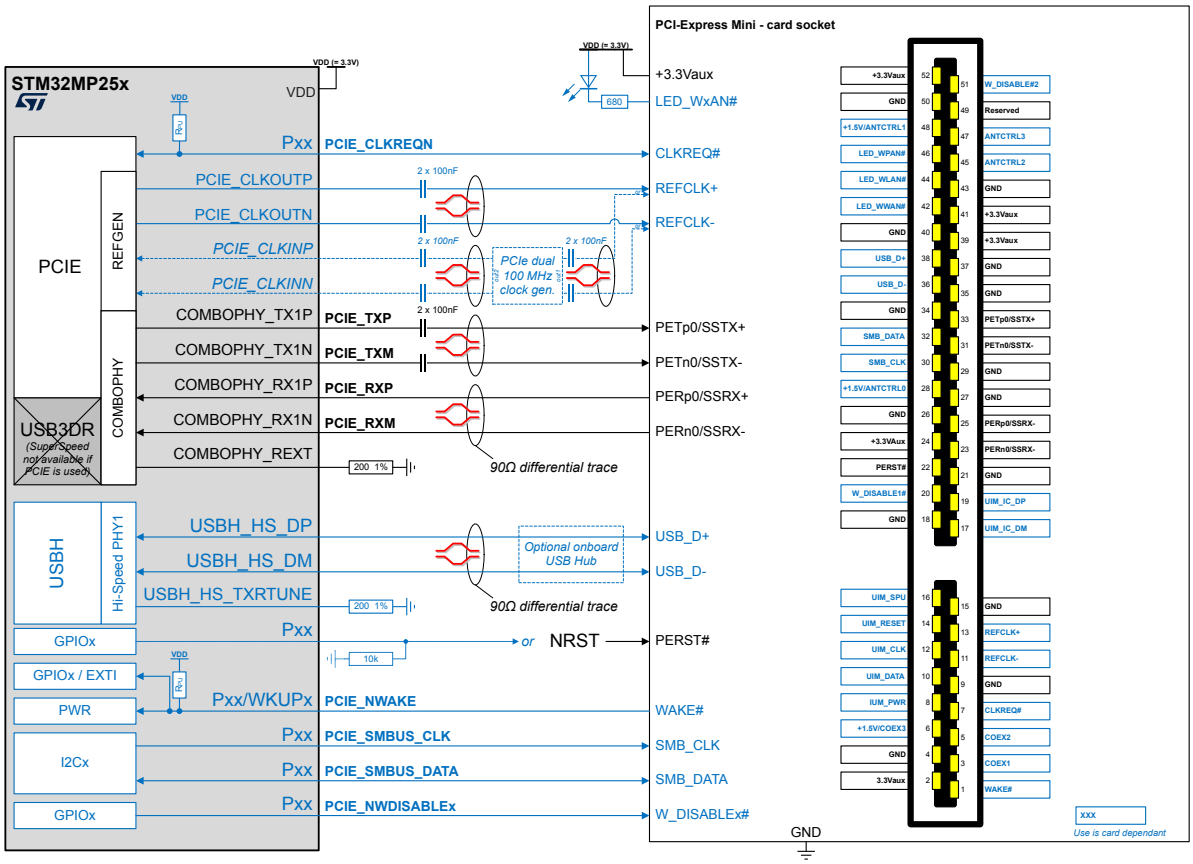
8.14 PCI Express (PCIE)

A 200 Ω 1% resistor should be connected between COMBOPHY_REXT and V_{SS}.

Note: If the USBH hi-speed host is also used to connect a specific PCI-Express device, a 200 Ω 1% resistor should be connected between USBH_HS_TXRTUNE and V_{SS}.

Note: As PCI-Express (PCIE) and USB SuperSpeed (USB3DR SuperSpeed link) share the same I/Os (COMBOPHY pins), their usages are exclusive and defined during user product definition.

Figure 37. PCIE example with connection to a PCI-Express mini



Note:

1. *Decoupling capacitors not shown.*
2. *In case PCIE_CLKINP/N inputs are used as PCIE clock source, and in order to complete internal PCIE initialization, the PCIE_CLKREQN pin should be temporarily driven at 0. This is done by the application software using related PCIE_CLKREQN GPIO in open-drain with output low.*

Table 20. COMBOPHY PCB routing recommendations

Recommendation	Min	Typ	Max	Unit
Differential impedance	85	90	95	Ω
Single-ended impedance	42	45	48	Ω
Length matching within a pair (including package)(1)	-5	-	+5	mils
	-0.127	-	+0.127	mm
Max traces length (up to connector or first active component)	-	-	8	inches
	-	-	203	mm
AC coupling capacitor (including capacitor tolerances)	74	100	200	nF
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		-(2)
Do no route over power plane split. No stubs (point to point only). No right angles				

1. *See Section 8.19 for PCB track length matching details.*
2. *Definition could be found, for instance, in the DDR memory routing guidelines ([6]).*

8.15 Ethernet

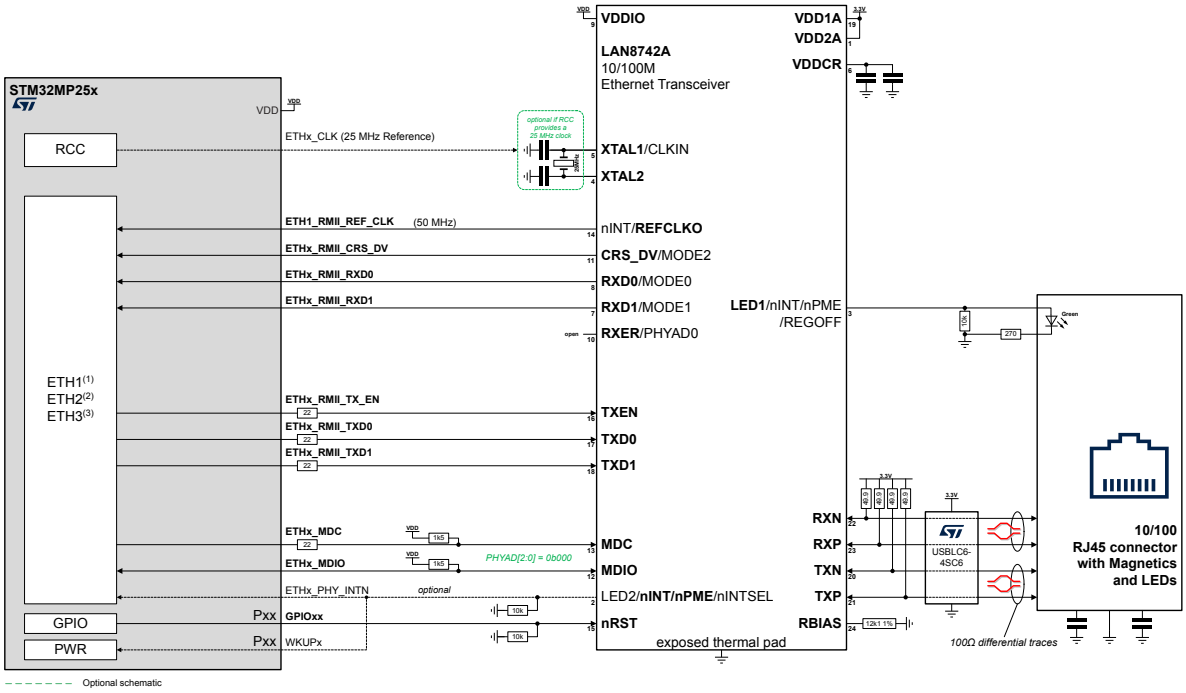
8.15.1 10/100M Ethernet

Note: A good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers) and V_{DD} voltage.

When using VDD = 1.8 V, a setting of VDDIOxVRSEL could be required to ensure the adequate speed on the pins used on the ETHx outputs.

If needed, the impedance matching resistors must be placed as close as possible of the output driver pin. Values in the example below works in most cases, but can be tailored to each side I/O drive strengths and PCB impedance.

Figure 38. 10/100M Ethernet PHY connection example



Note:

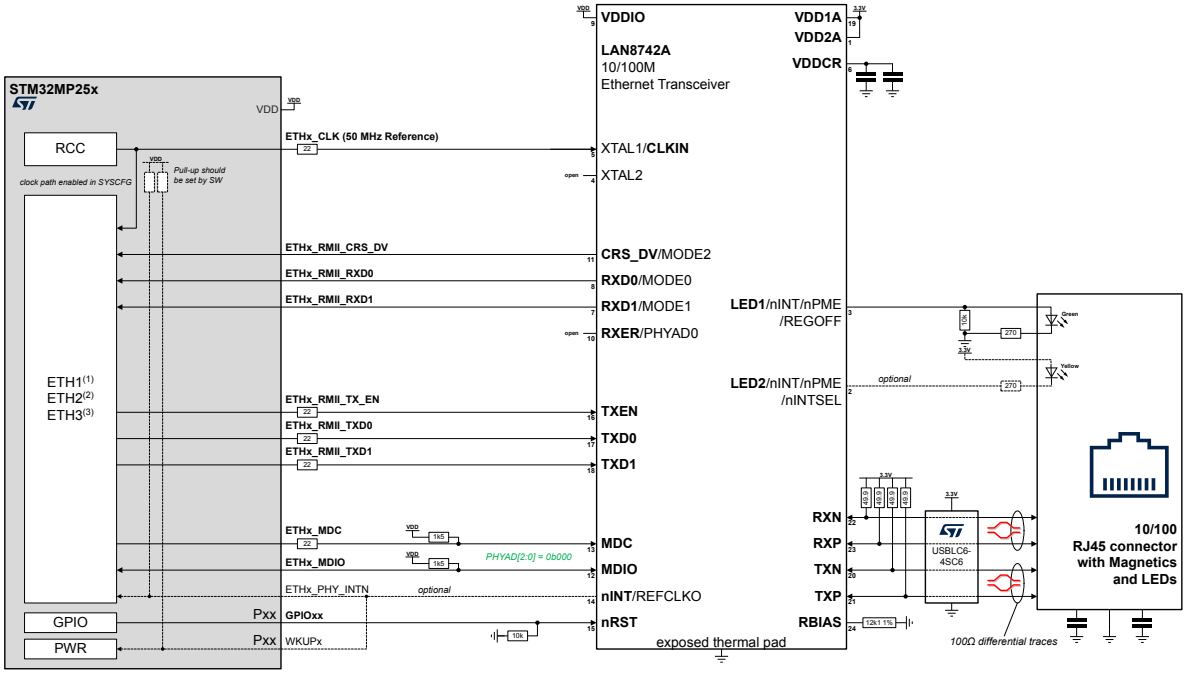
1. *ETH1 is either ETH1 direct or ETHSW port2 (ETHSW is not available on some part numbers).*
2. *ETH2 is not available on some part numbers.*
3. *ETH3 is ETHSW port1. ETHSW is not available on some part numbers.*
4. *Decoupling capacitors not shown.*

Note:

- *As RCC cannot provide the 25 MHz reference clock to the PHY during low power modes, the dedicated 25 MHz crystal is required on the PHY in case a Wake-Up On LAN (WOL) is needed for the platform.*
- *Setting RCC PLLs to get 25 MHz output for PHY clocking could constrain other RCC frequencies. In that case it is more flexible to put a dedicated 25 MHz crystal on the PHY.*

Alternatively, if PHY allows it and if the RCC can provide a precise 50 MHz clock (to be checked with respect to HSE quartz frequency and RCC other peripheral/core clocks frequency settings), a 50 MHz ETH_CLK can be provided by the STM32MP23/25xx devices to the PHY, and REF_CLK is left unconnected on both sides. This saves BOM and area, as well as some power on some PHYs.

Figure 39. 10/100M Ethernet PHY connection (with REFCLK from RCC)



Note:

1. *ETH1 is either ETH1 direct or ETHSW port2 (ETHSW is not available on some part numbers).*
2. *ETH2 is not available on some part numbers.*
3. *ETH3 is ETHSW port1. ETHSW is not available on some part numbers.*
4. *Decoupling capacitors are not shown.*

Note:

- *As the RCC cannot provide the 50 MHz reference clock to the PHY during Low-power modes, this option is not possible in case a Wake-Up On LAN (WOL) is needed for the platform. Setting the RCC PLLs to get 50 MHz output for PHY clocking could constrain other RCC frequencies. In that case, this option is not possible.*
- *Setting RCC PLLs to get 50 MHz output for PHY clocking could constrain other RCC frequencies. In that case, this option is not possible.*

Table 21. ETH RMII pins

Pin name	(1)	ETH1(2)	ETH2(3)	ETH3(4)(3)	Comments
ETHx_CLK	→	PF3, PF5, PF8	PF4, PG3	-(5)	Optional 25 MHz or 50 MHz reference(6)
ETHx_RMII_REF_CLK	←	PA14	PC0, PF6	PA5	Optional if 50 MHz provided by ETHx_CLK
ETHx_RMII_CRS_DV	←	PA11	PC3, PF8	PA2	-
ETHx_RMII_RXD0	←	PF1	PG0	PA9	-
ETHx_RMII_RXD1	←	PC2	PC12	PA10	-
ETHx_RMII_TX_EN	→	PA13	PC4	PA3	-
ETHx_RMII_TXD0	→	PA15	PC7	PA6	-
ETHx_RMII_TXD1	→	PC1	PC8	PA7	-
ETHx_MDC	→	PA9, PF0, PF4	PC6, PG4, PH10	-(7)	-
ETHx_MDIO	→ ←	PA10, PF2, PF5	PC5, PF9, PH11	-(7)	-
ETHx_PHY_INTN	←	PA12, PC6, PF5	PF5, PG3	PA1	Optional

1. *Signal direction: → MPU to PHY, ← PHY to MPU*
2. *Could be also used as ETHSW port2. ETHSW is not available on some part numbers.*
3. *Not available on some part numbers*
4. *Equivalent to ETHSW port1*
5. *If needed, ETH1_CLK should be used.*
6. *As RCC cannot provide the reference clock to the PHY during low power modes, a dedicated 25MHz crystal is required on the PHY if Wake-Up On LAN (WOL) is needed for the platform.*
7. *ETH3 PHY share THE same MDC/MDIO pins than ETH1 PHY (need to use different address for the PHY).*

8.15.2 Gigabit Ethernet

Note that a good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

When using V_{DD} = 1.8 V, a setting of VDDIOxRSEL could be required to ensure the adequate speed on pins used on ETHx outputs.

If needed, the impedance matching resistors should be placed as close as possible of the output driver pin. Values in the example below should work in most cases, but could be tailored to each side I/O drive strengths and PCB impedance.

Figure 40. Gigabit Ethernet PHY connection with VDD = 3.3 V (RTL8211F)

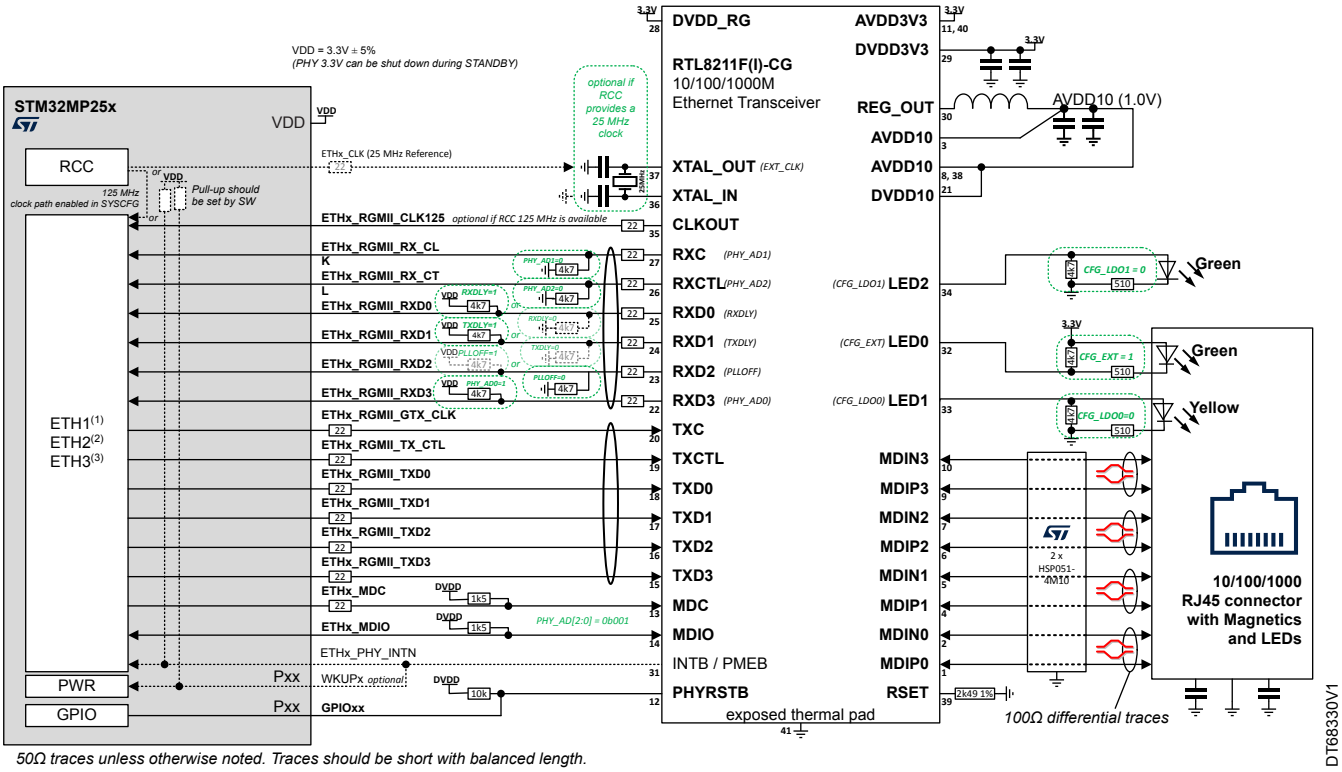
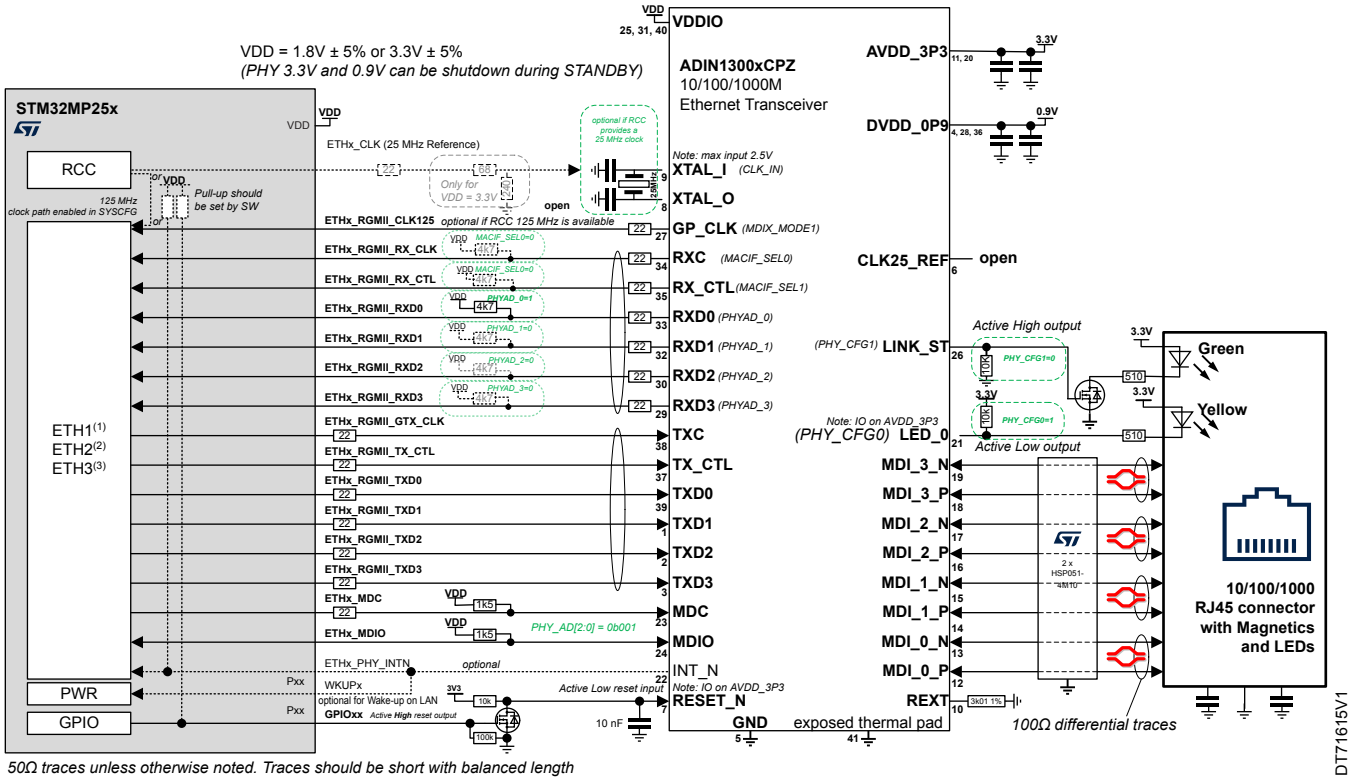


Figure 41. Gigabit Ethernet PHY connection (ADIN1300xCPZ)



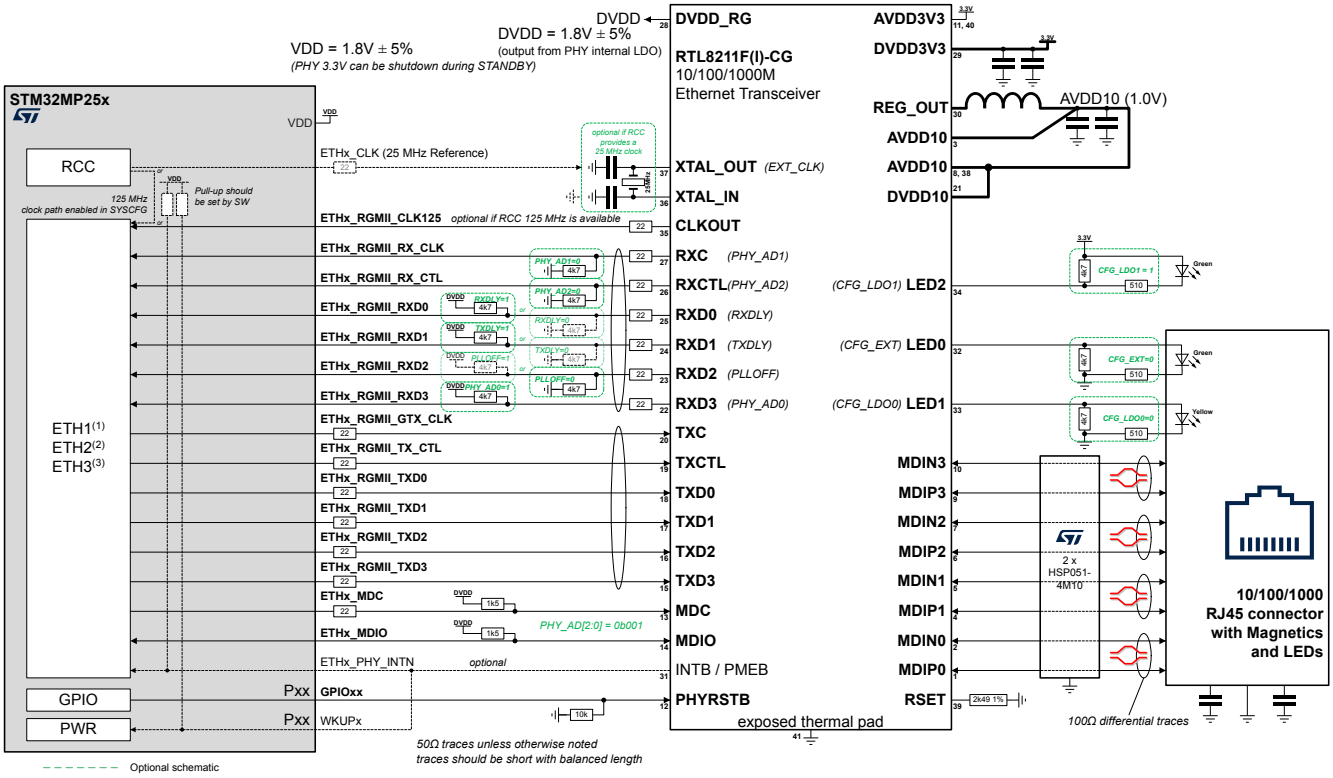
Note:

1. *ETH1 is either ETH1 direct or ETHSW port2 (ETHSW is not available on some part numbers).*
2. *ETH2 is not available on some part numbers.*
3. *ETH3 is ETHSW port1. ETHSW is not available on some part numbers.*
4. *Decoupling capacitors are not shown.*

Note:

- *As RCC cannot provide the 25 MHz reference clock to the PHY during low power modes, the dedicated 25 MHz crystal is required on the PHY in case Wake-Up On LAN (WOL) is needed for the platform.*
- *Setting RCC PLLs to get 25 MHz output for PHY could constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.*

Figure 42. Gigabit Ethernet PHY connection with V_{DD} = 1.8 V (RTL8211F)



Note:
1. *ETH1 is either ETH1 direct or ETHSW port2 (ETHSW is not available on some part numbers).*
2. *ETH2 is not available on some part numbers.*
3. *ETH3 is ETHSW port1. ETHSW is not available on some part numbers.*
4. *Decoupling capacitors are not shown.*

Note:
- *As RCC cannot provide the 25MHz reference clock to the PHY during low power modes, the dedicated 25MHz crystal is required on the PHY in case Wake-Up On LAN (WOL) is needed for the platform.*
- *Setting RCC PLLs to get 25MHz output for PHY could constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25MHz crystal on the PHY.*

Table 22. ETH RGMII pins

Pin name	(1)	ETH1(2)	ETH2(3)	ETH3(4)(3)	Comments
ETHx_CLK	→	PF3, PF5, PF8	PF4, PG3	-(5)	Optional 25 MHz reference(6)
ETHx_RGMII_CLK125	←	PC4, PH9	PF8, PG2	-(7)	Optional if 125 MHz is fed internally from RCC to ETH IP
ETHx_RGMII_RX_CLK	←	PA14	PF6	PA5	See also Table 12. GPIO advance configuration recommended settings
ETHx_RGMII_RX_CTL	←	PA11	PC3	PA2	
ETHx_RGMII_RXD0	←	PF1	PG0	PA9	
ETHx_RGMII_RXD1	←	PC2	PC12	PA10	
ETHx_RGMII_RXD2	←	PH12	PF9	PH7	
ETHx_RGMII_RXD3	←	PH13	PC11	PH8	
ETHx_RGMII_GTX_CLK	→	PC0	PF7	PH2	
ETHx_RGMII_TX_CTL	→	PA13	PC4	PA3	
ETHx_RGMII_TXD0	→	PA15	PC7	PA6	
ETHx_RGMII_TXD1	→	PC1	PC8	PA7	
ETHx_RGMII_TXD2	→	PH10	PC9	PH6	
ETHx_RGMII_TXD3	→	PH11	PC10	PH3	
ETHx_MDC	→	PA9, PF0, PF4	PC6, PG4, PH10	-(8)	-
ETHx_MDIO	→ ←	PA10, PF2, PF5	PC5, PF9, PH11	-(8)	-
ETHx_PHY_INTN	←	PA12, PC6, PF5	PF5, PG3	PA1	Optional

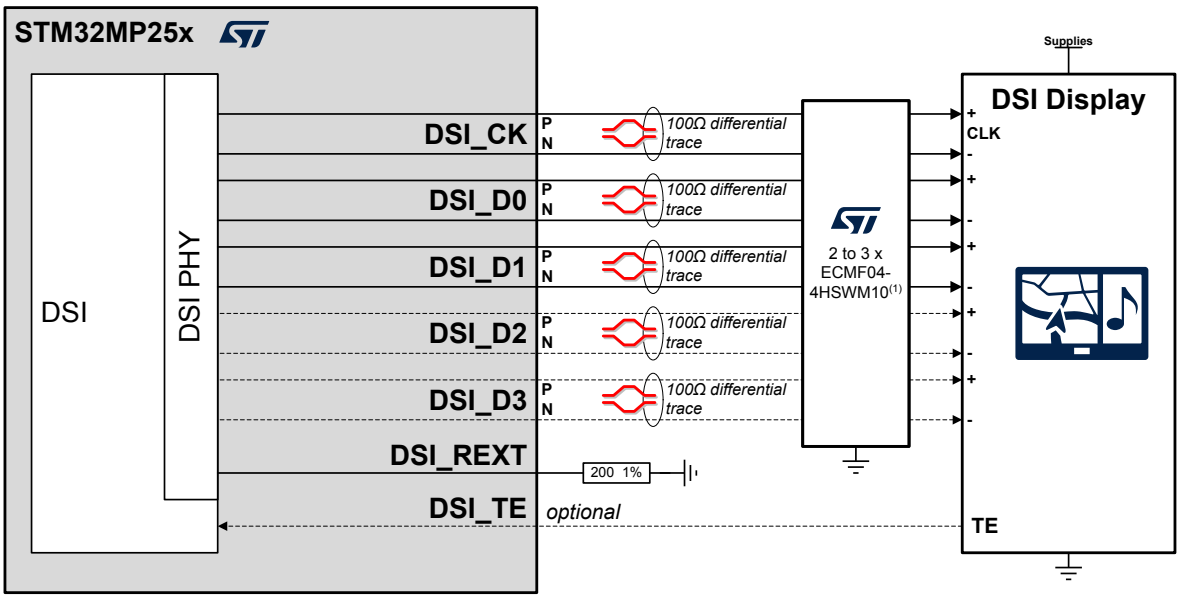
1. *Signal direction: → MPU to PHY, ← PHY to MPU*
2. *Could be also used as ETHSW port2. ETHSW is not available on some part numbers.*
3. *Not available on some part numbers*
4. *Equivalent to ETHSW port1*
5. *If needed, ETH1_CLK should be used.*
6. *As RCC cannot provide the reference clock to the PHY during low power modes, a dedicated 25MHz crystal is required on the PHY if Wake-Up On LAN (WOL) is needed for the platform.*
7. *If needed, ETH1_RGMII_CLK125 should be used.*
8. *ETH3 PHY share the same MDC/MDIO pins than ETH1 PHY (need to use different address for the PHY).*

8.16 Display serial interface (DSI)

Note: As pixel data sent over DSI are provided by LTDC, same image and same picture timing is possible at a time over the whole set of possible interface (LTDC parallel output, DSI, or LVDS). See reference manual for details.

A 200 Ω 1% resistor should be connected between DSI_REXT and V_{SS}.

Figure 43. Display connection example with DSI



Note:
1. *ECMF04-4HSWM10 includes common-mode filter for WLAN/BT bands. For ESD protection only, HSP051-4M10 could be used instead (similar but not same footprint).*
2. *Decoupling capacitors are not shown.*

Table 23. DSI PCB routing recommendations

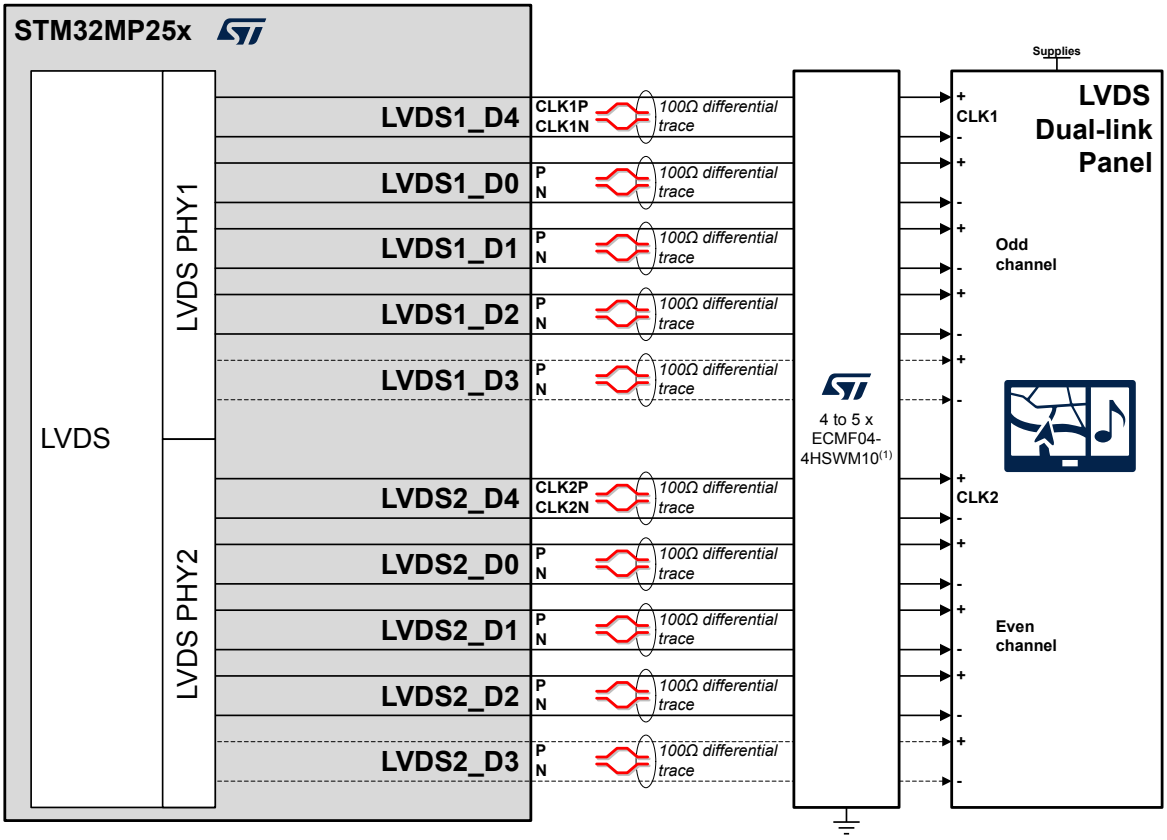
Recommendation	Min	Typ	Max	Unit
Differential impedance	90	100	110	Ω
Single-ended impedance	45	50	55	Ω
Length matching within a pair (including package)(1)	-5	-	+5	mils
	-0.127	-	+0.127	mm
Length matching between clock and data pairs	-100	-	+100	mils
	-2.54	-	+2.54	mm
Max link length (including display cables)	-	-	8	inches
	-	-	203	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		-(2)
Do no route over power plane split. No stubs (point to point only). No right angles				

1. *See Section 8.19 for PCB track length matching details.*
2. *Definition could be found, for instance, in the DDR memory routing guidelines ([6]).*

8.17 Display serial interface using LVDS signaling (LVDS)

Note: As pixel data sent over LVDS are provided by LTDC, same image and same picture timing is possible at a time over the whole set of possible interface (LTDC parallel output, DSI, or LVDS single-link or dual-link). See reference manual for details.

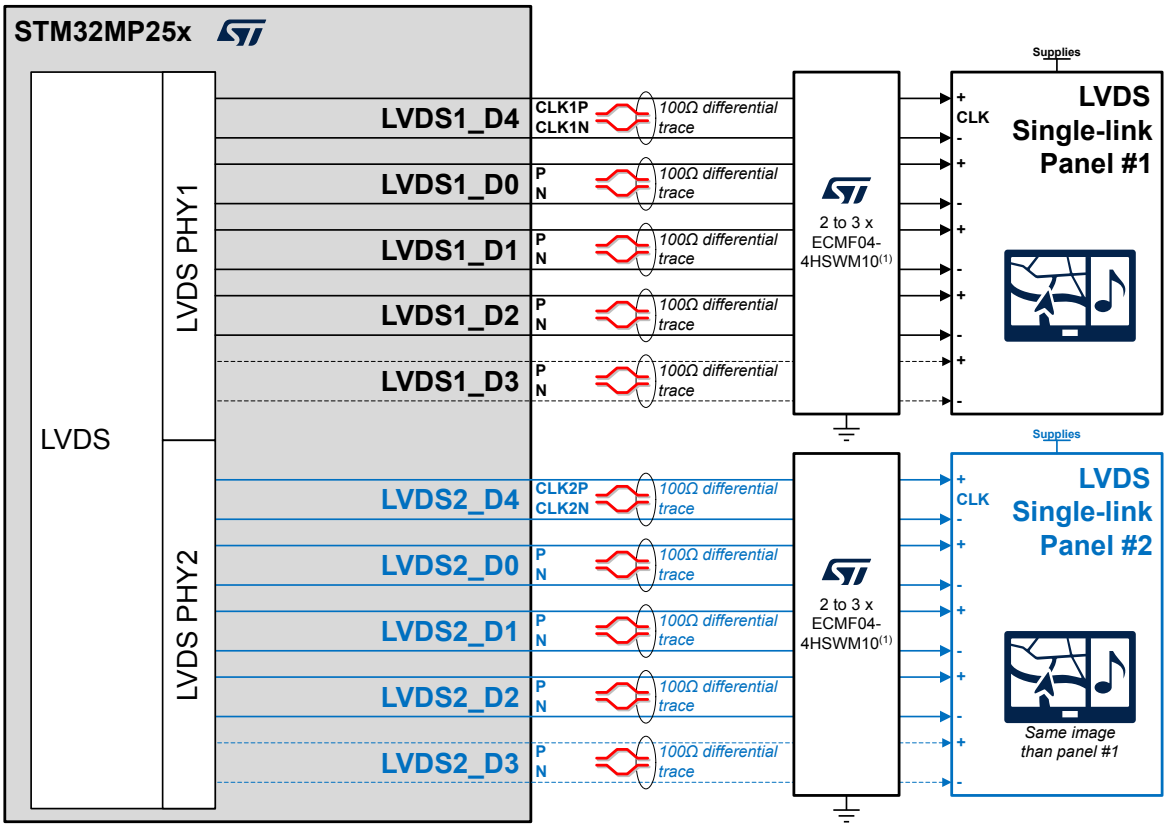
Figure 44. Dual-link panel connection with LVDS



Note:

1. *ECMF04-4HSWM10 includes common-mode filter for WLAN/BT bands. For ESD protection only, HSP051-4M10 could be used instead (similar but not same footprint).*
2. *Decoupling capacitors are not shown.*
3. *Availability of LVDS depends on the STM32MP23/25xx lines devices.*

Figure 45. **Single-link panel connection with LVDS**



Note:

1. *ECMF04-4HSWM10 includes common-mode filter for WLAN/BT bands. For ESD protection only, HSP051-4M10 could be used instead (similar but not same footprint).*
2. *Supplies and decoupling capacitors are not shown.*
3. *Availability of LVDS depends on the STM32MP23/25xx lines devices.*

Notice that when using two single-link displays (Figure 44), it is only possible to have the same image (clone) with the requirement to have exactly the same display configuration (that is to say both displays must have the same timings requirements). It is not possible to output different images on each display.

Table 24. LVDS PCB routing recommendations

Recommendation	Min	Typ	Max	Unit
Differential impedance	90	100	110	Ω
Single-ended impedance	45	50	55	Ω
Length matching within a pair (including package)(1)	-5	-	+5	mils
	-0.127	-	+0.127	mm
Length matching between clock and data pairs	-200	-	+200	mils
	-5.08	-	+5.08	mm
Max link length (including display cables)	-	-	20	inches
	-	-	508	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		-(2)
Do no route over power plane split. No stubs (point to point only). No right angles				

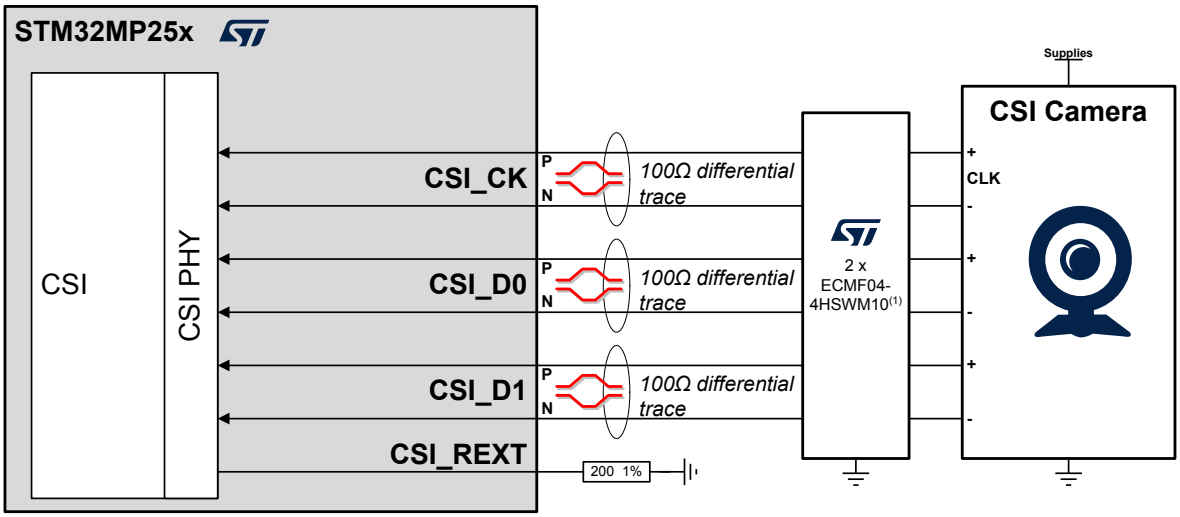
1. *See Section 8.19 for PCB track length matching details.*
2. *Definition could be found, for instance, in the DDR memory routing guidelines [6].*

8.18 Camera serial interface (CSI)

Note: As pixel data received by CSI are processed by DCMIPP, the parallel high-resolution sensor interface is not available when CSI is used. In that case, a second parallel low-performance sensor is still possible using DCMI. See reference manual for details.

A 200 Ω 1% resistor should be connected between CSI_REXT and V_{SS}.

Figure 46. CSI example



Note: 1. Supplies and decoupling capacitors are not shown.
2. Image sensor controls are not shown (I2C for control, autofocus, and so on.)

Table 25. CSI PCB routing recommendations

Recommendation	Min	Typ	Max	Unit
Differential impedance	90	100	110	Ω
Single-ended impedance	45	50	55	Ω
Length matching within a pair (including package)(1)	-5	-	+5	mils
	-0.127	-	+0.127	mm
Length matching between clock and data pairs	-100	-	+100	mils
	-2.54	-	+2.54	mm
Max link length (including camera module cables)	-	-	8	inches
	-	-	203	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		-(2)
Do no route over power plane split. No stubs (point to point only). No right angles				

1. *See Section 8.19 for PCB track length matching details.*
2. *Definition could be found, for instance, in the DDR memory routing guidelines [6].*

8.19 High-speed differential lane PCB track length matching

When possible, each package has been optimized to provide easier length matching when differential balls pair signals are not directly on adjacent balls. Table 26 shows internal package track length difference xP minus xN/xM at ball level to be taken into account by the PCB tool. Ideal length matching is achieved when : PCB track length of xP - PCB track length of xN/xM - internal package track length difference (table below) = 0 .

Figure 47. Example of PCB differential track for 0.8 and 0.5 mm ball pitch package

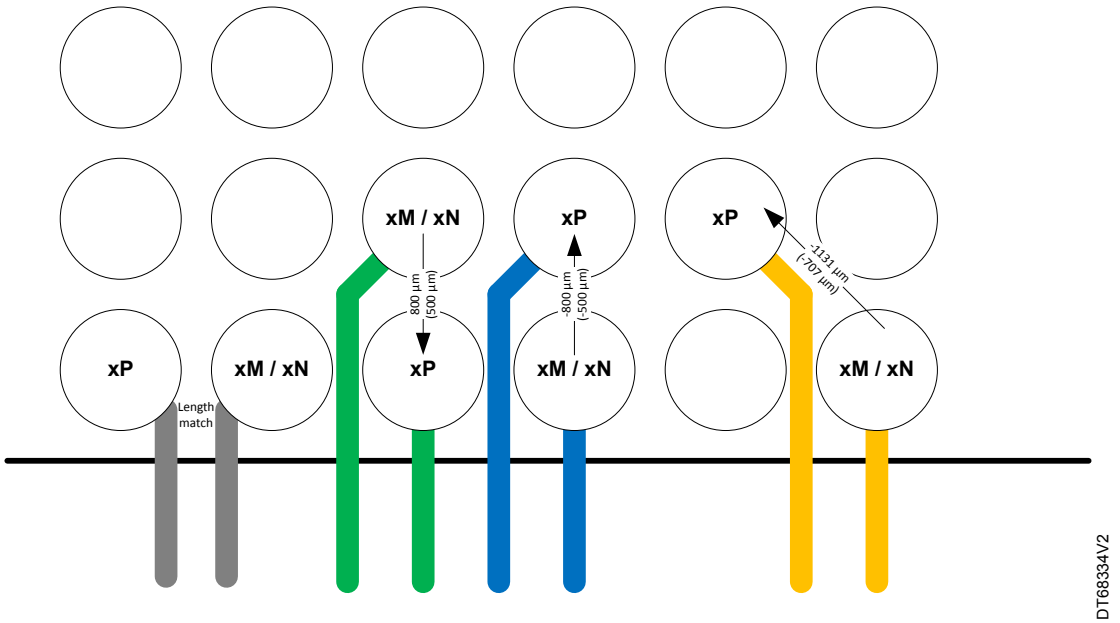


Table 26. Package length matching values

Pin name	TFBGA361 (16 x 16 pitch 0.8 mm)		VFBGA361 (10 x 10 pitch 0.5 mm)		VFBGA424 (14 x 14 pitch 0.5 mm)		TFBGA436 (18 x 18 pitch 0.8 mm)	
	Ball	Δlength (µm)	Ball	Δlength (µm)	Ball	Δlength (µm)	Ball	Δlength (µm)
DSI								
DSI_CKP	A4	337	B4	207	C7	283	A8	404
DSI_CKN	B4		A4		C8		B8	
DSI_D0P	B6	-457	B5	57	B9	-192	C9	-478
DSI_D0N	A6		A5		C9		B9	
DSI_D1P	B5	-389	B6	-366	B10	-332	D9	138
DSI_D1N	A5		A6		A10		E9	
DSI_D2P	B3	-313	A3	-177	B7	-311	C8	30
DSI_D2N	A3		B3		A7		D8	
DSI_D3P	B2	85	A2	-135	A6	379	A7	449
DSI_D3N	A2		B2		B6		B7	
CSI								

Pin name	TFBGA361 (16 x 16 pitch 0.8 mm)		VFBGA361 (10 x 10 pitch 0.5 mm)		VFBGA424 (14 x 14 pitch 0.5 mm)		TFBGA436 (18 x 18 pitch 0.8 mm)	
	Ball	Δlength (µm)	Ball	Δlength (µm)	Ball	Δlength (µm)	Ball	Δlength (µm)
CSI_CKP	C1	262	C1	147	C4	389	C6	323
CSI_CKN	C2		C2		D4		D6	
CSI_D0P	E2	-463	E2	-450	B3	-335	C5	-365
CSI_D0N	E1		E1		A3		B5	
CSI_D1P	D1	228	D1	162	B5	273	D7	526
CSI_D1N	D2		D2		C5		E7	
USB								
USBH_HS_DP	W15	39	W11	-11	AF21	-224	AA16	-300
USBH_HS_DM	V15		V11		AG21		AB16	
USB3DR_DP	W16	3	W12	27	AF22	-246	W17	-212
USB3DR_DM	V16		V12		AG22		Y17	
LVDS								
LVDS1_D0P	F1	334	F2	75	G2	253	D4	-24
LVDS1_D0N	F2		F1		G3		D3	
LVDS1_D1P	G1	296	F4	125	H3	345	D2	164
LVDS1_D1N	G2		F3		H4		D1	
LVDS1_D2P	H1	351	G4	83	J1	323	E3	471
LVDS1_D2N	H2		G3		J2		E4	
LVDS1_D3P	K1	-72	J3	68	L2	309	F2	292
LVDS1_D3N	K2		J2		L3		F3	
LVDS1_D4P	J1	328	H4	562	K1	288	F4	386
LVDS1_D4N	J2		H3		K2		F5	
LVDS2_D0P	-		-		B1	159	A4	50
LVDS2_D0N					B2		B4	
LVDS2_D1P	-		-		C2	326	A2	707
LVDS2_D1N					C3		A3	
LVDS2_D2P	-		-		E3	-33	C3	-47
LVDS2_D2N					D3		B3	
LVDS2_D3P	-		-		E1	241	C1	231
LVDS2_D3N					E2		C2	
LVDS2_D4P	-		-		F1	253	B1	286
LVDS2_D4N					F2		B2	
COMBOPHY								
COMBOPHY_TX1P	V11	536	U15	336	AE24	-185	AA19	-168
COMBOPHY_TX1N	W11		V15		AD24		AB19	
COMBOPHY_RX1P	V12	-312	U16	-191	AG25	155	AA20	-259
COMBOPHY_RX1N	W12		V16		AF25		AB20	

Revision history

Table 27. **Document revision history**

Date	Version	Changes
21-Mar-2024	1	Initial release
22-Mar-2024	2	Updated document specific properties Added Table 1. Applicable products
26-Jun-2024	3	Updated: • Table 2. Reference documents • Table 4. Amount of decoupling recommendation by package[23] • Table 7. Package availability summary • Table 8. STM32MP25xx differences per package • Section 4.1.2: External crystal (HSE crystal) • Table 11. Boot sources • Section 7.4: GPIO advance configuration • Figure 23. Example of PMIC supplies for 3.3 V I/Os and DDR4 • Section 8.5.2: Example of PMIC supplies for 1.8 V I/Os with LPDDR4 • Figure 24. Example of PMIC supplies for 1.8 V I/Os with LPDDR4 • Table 17. DDR4 2x16-bit default pin mapping[1] • Figure 26. LPDDR4 connection example • Table 18. LPDDR4 pin mapping[1]
13-Nov-2024	4	Updated: • Document references • Table 1. Applicable products • Table 2. Reference documents • Section 2.1.1: Independent ADC supply and reference voltage • Figure 2. Simplified reset pin circuit • Table 7. Package availability summary • Table 8. STM32MP25xx differences per package • Table 9. STM32MP23xx differences per package • Table 13. OSPEEDR setting example for VDD = 3.3 V typ.[1] • Table 14. OSPEEDR setting example for VDD = 1.8 V typ.[4] • Section 8: STM32MP25x reference design examples • Figure 23. Example of PMIC supplies for 3.3 V I/Os and DDR4 • Figure 24. Example of PMIC supplies for 1.8 V I/Os with LPDDR4 • Table 17. DDR4 2x16-bit default pin mapping[1] • Table 18. LPDDR4 pin mapping[1] • Table 26. Package length matching values • Table 4. Amount of decoupling recommendation by package[23]
1-Apr-2025	5	Updated: • Section 7.4: GPIO advance configuration • Section 8.6: DDR4 SDRAM • Section 8.13.1: USB hi-speed device (USB3DR) • Section 8.19: High-speed differential lane PCB track length matching

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