ST8500 power line communication system-on-chip G3-PLC characterization

Introduction

This document is aimed at describing the electrical characteristics and communication performance of a Power Line Communication (PLC) node based on the EVALKITST8500-1 hardware and G3-PLC firmware operating in the CENELEC A, CENELEC B and FCC frequency band.

The EVALKITST8500-1 is an evaluation kit for the ST8500 platform, exploiting the performance capability of the ST8500 device and STLD1 line driver.

The ST8500 is a fully programmable power line communication (PLC) modem system-on-chip (SoC), able to run any PLC protocol in the frequency band up to 500 kHz.

Please check for the EVALKITST8500-1 hardware documentation, evaluation software and firmware libraries at st.com/powerline. For specific software or firmware releases, you may need to contact the STMicroelectronics sales office directly

Figure 1. EVALKITST8500-1 - ST8500 evaluation kit

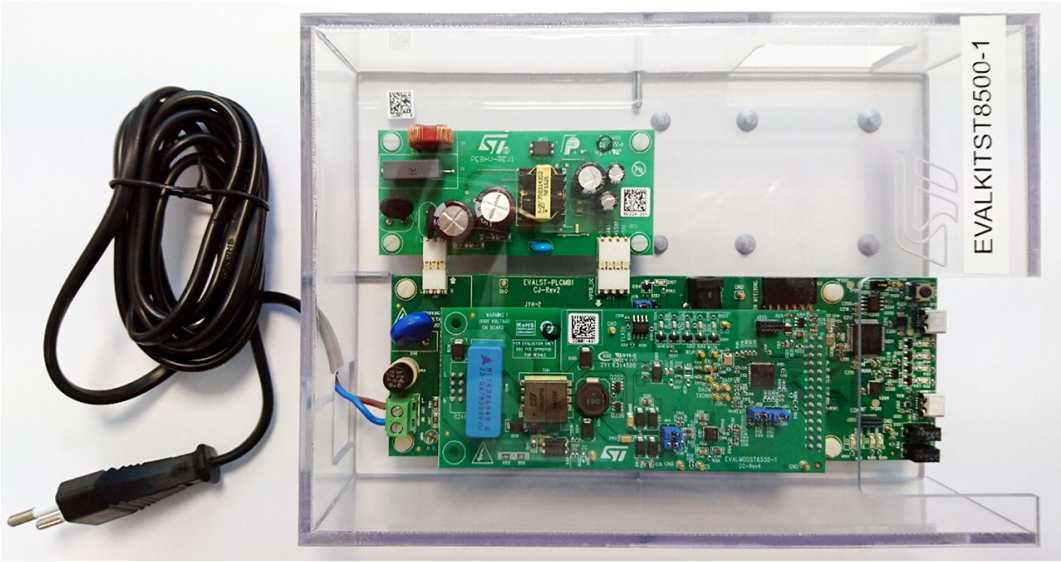
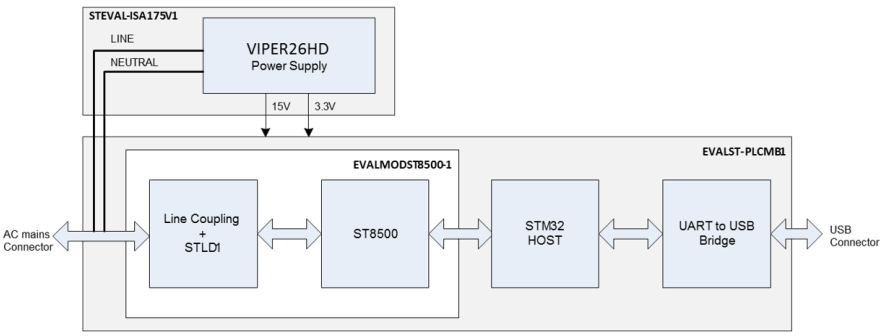


Figure 2. EVALKITST8500-1 – functional block diagram



1 Safety recommendations

The ST8500 evaluation kit must be used by expert technicians only. Due to the high voltage (85 - 265 Vac) present on the non-isolated parts, special care must be taken in order to avoid electrical risks for user safety.

There are no protections against high voltage accidental human contact.

After disconnection of the board from the mains all the live part must not be touched immediately because of the energized capacitors.

It is mandatory to use a mains insulation transformer to perform any tests on the high voltage sections, using test instruments like, for instance, spectrum analyzers or oscilloscopes.

Do not connect any probe to high voltage sections if the board is not isolated from the mains supply, in order to avoid damaging instruments and demonstration tools.

STMicroelectronics assumes no responsibility for the consequences of any improper use of this development tool.

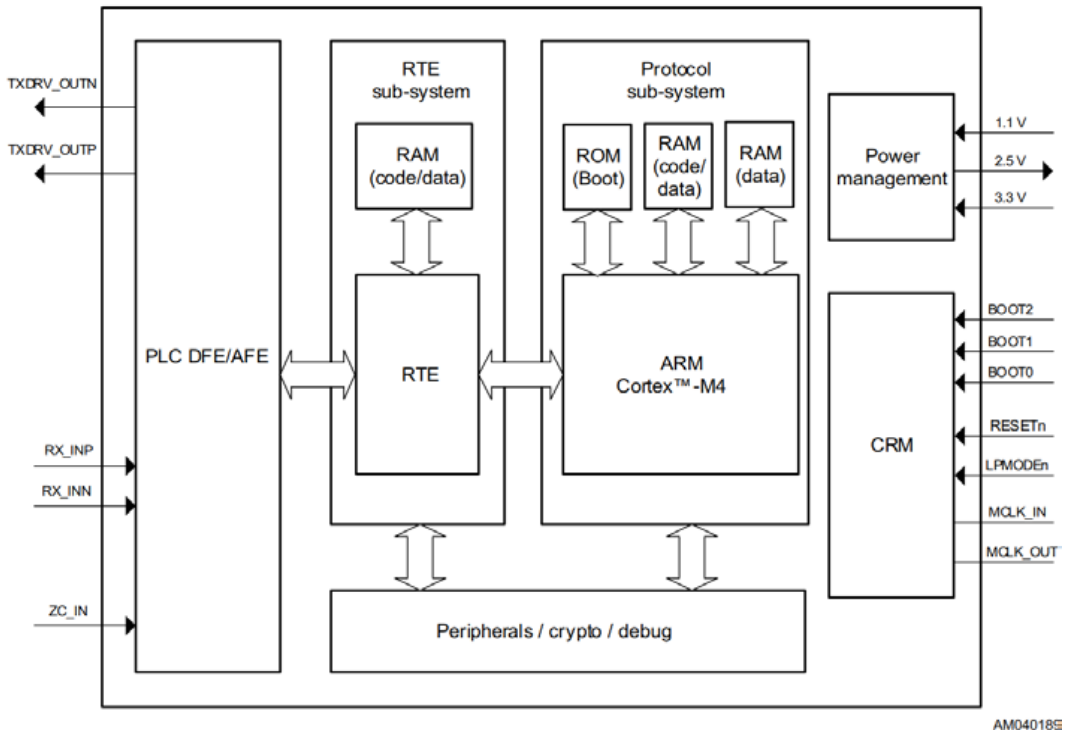
2 ST8500 programmable power line communication modem system on chip description

The ST8500 is a fully programmable power line communication (PLC) modem System-on-Chip (SoC), able to run any PLC protocol in the frequency band up to 500 kHz.

The device architecture has been designed to target CENELEC EN50065, FCC and ARIB compliant applications supporting all major PLC protocol standards such as ITU G.9904 (PRIME), ITU G.9903 (G3-PLC) and many other possible PLC protocol specifications and evolutions.

The ST8500 basic block diagram is shown in Figure 3.

Figure 3. ST8500 block diagram



3 Scope of the performance tests

In this document, we focus on G3-PLC Physical layer communication performance for the 3 bands:

- G3 CENELEC A: 35.9375 to 90.625 kHz
- G3 CENELEC B: 98.4375 to 121.875 kHz
- G3 FCC: 154.6875 to 487.5 kHz

Note: ***Values of the performance parameters reported in this document may be subject to variations due to updates to the G3-PLC firmware library.***

4 Test equipment

The measurement results reported in this document have been obtained using the following instruments:

Table 1. Electrical instruments used for testing

Equipment designation	Equipment reference	Purpose
Spectrum analyzer	Rohde & Schwarz FSU	TX and RX signal power measurement
Spectrum analyzer	Agilent E4443A	RX Input noise power measurement
Differential active probe	Agilent 1141A	Differential, high impedance, low level signal measurements
Probe control and power module	Agilent 1142A	Agilent 1141A probe supply and control
Two-line V-network LISN (x2)	Rohde & Schwarz ENV216	Connecting DUT (ST8500 development kit) to AC mains – Reference line impedance
50 Ω attenuator	Trilithic 2010926004-R	Transmitted signal attenuation
EMC-EMI filter (x3)	Schaffner FN2080-6-06	Mains noise filtering
DC power analyzer	Agilent N6705A	Power supply and current consumption measurement

5 Power supply characteristics

The VIPer26H PSU board is used to power the full EVALKITST8500-1, with:

- VCC = 15 V DC voltage to power the STLD1 line driver section
- 3.3 V DC voltage to power the ST8500 device but also the STM32 host controller and auxiliary functions

In the table below, we discriminate the power consumption of the ST8500 module (measured on ST8500 module input) from the power consumption of the STM32 host controller and auxiliary functions.

The test set-up for the measurements performed in this section is described in Figure 5.

Table 2. Electrical characteristics - power supply

Parameter	Band	Value				Conditions
		Min.	Typ.	Max.	Unit	
VCC power supply voltage		8	15	18	V	
VCC power supply current RX mode (*)		-	1.5	2	mA	Current into STLD1 and external bias network
VCC power supply current TX mode (*)	CEN-A (Class 134)	33.8	44.2	48.8	mA	No load
		101	109	112	mA	CISPR16-1-2 LISN
		550	600	602	mA	2 Ω
	CEN-B (Class 122)	30.6	41	45.9	mA	No load
		38.3	47.5	52	mA	CISPR16-1-2 LISN
		293	300	302	mA	2 Ω
	FCC	36	44.9	49.3	mA	No load
		49.5	57.5	61.8	mA	CISPR16-1-2 LISN
		580	615	620	mA	2 Ω
3V3 supply voltage		3	3.3	3.6	V	
3V3 power supply current RX mode (**)	CEN-A	39.1	37	35.5	mA	
	CEN-B	38.9	36.8	35.3	mA	
	FCC	44.7	42.1	40.1	mA	
3V3 power supply current TX mode (**)	CEN-A	46.2	45	42.9	mA	
	CEN-B	47.7	45.6	44	mA	
	FCC	53	50.4	48.3	mA	
3V3 power supply current - STM32 host & peripheral functions		9	9.2	9.4	mA	
1V1 ST8500 core supply voltage		1.05	1.1	1.21	V	1V1 is generated by a DCDC from 3V3
1V1 ST8500 core power supply current RX mode (***)	CEN-A		65		mA	
	CEN-B		63		mA	
	FCC		78.8		mA	
1V1 ST8500 core power supply current TX mode (***)	CEN-A		63.3		mA	
	CEN-B		64		mA	
	FCC		77.1		mA	

(*) VCC powers only the STLD1 Line Driver section (3V3/2V5/1V1 power consumption not included)

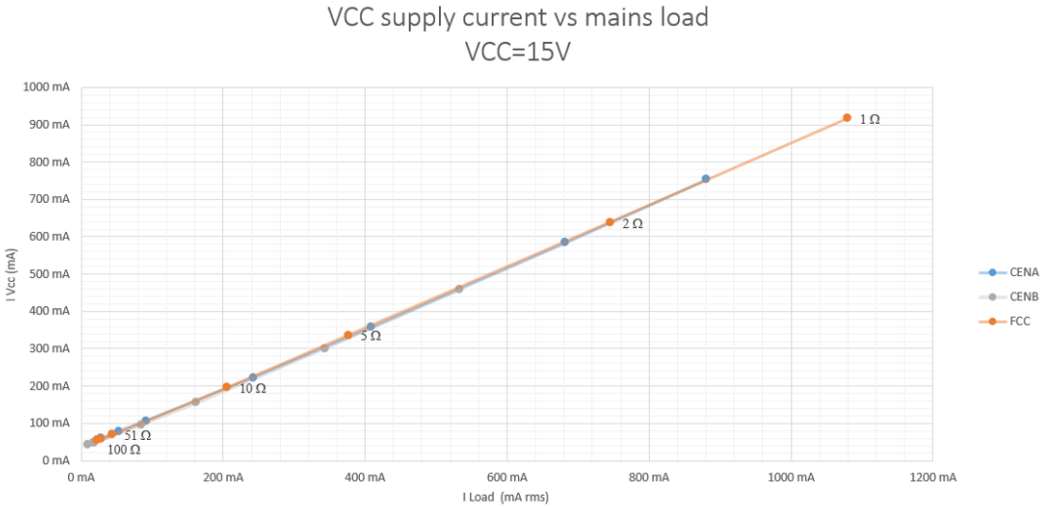
(**) 3V3 power consumption of the ST8500 only (no LED), including 1V1 DC-DC and 2V5 internal ST8500 LDO regulators

(***) 1V1 current already included in the 3V3 power consumption through the 1V1 DC-DC regulator

6 VCC supply current vs. load impedance

The current to be supplied by VCC in TX mode is linked to the load connected to J107 at mains level. This relation is illustrated in Figure 4.

Figure 4. VCC supply current vs. main load



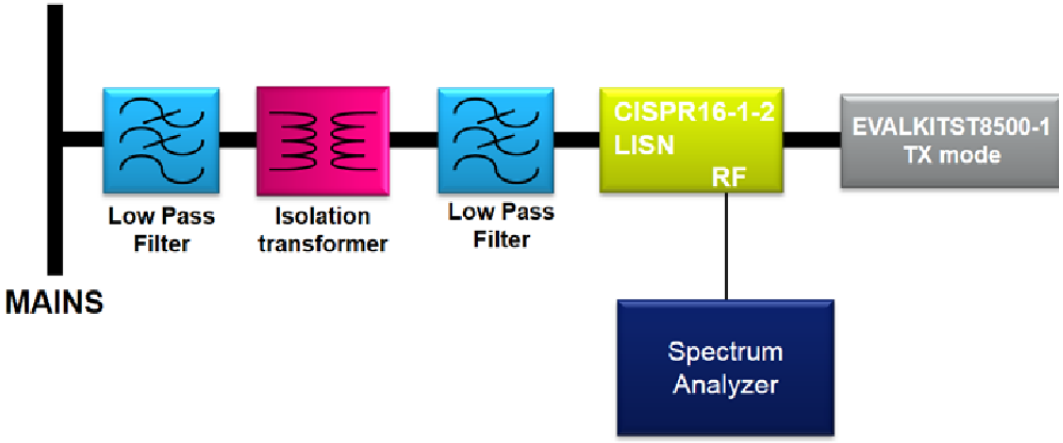
7 Transmitter characteristics

The voltages and currents in the transmission chain (line driver output, line coupling circuit and line load) depend on the load connected at mains level (J107). This section is illustrating graphically the behavior of those parameters.

7.1 Test setup

Transmitter characterization has been performed using the set-up illustrated in Figure 5 .

Figure 5. Bench set-up for transmission measurements



Instruments references are described in Section 4

Low Pass Filters (Schaffner FN2080-6-06) attenuate noise from mains in PLC bands.

It is recommended to configure the spectrum analyzer input coupling to DC, otherwise the power measurement for frequency below 50 kHz may be wrong.

A DC Power analyzer is used to supply the EVALKITST8500-1 while measuring current consumption.

The EVALKITST8500-1 mains output J107 is either connected to the LISN for spectrum analysis or to a variable load for power consumption measurement

7.2 Transmitter output voltage

7.2.1 VCC = 15 V

The output voltage delivered at STLD1 line driver output (PA1_OUT - PA2_OUT) and at the EVALKITST8500-1 output (J107) is given in the following figures, according to the load applied at J107 connector, and with VCC = 15 V (typical value).

For CEN-A and FCC, the TX power is at the maximum value (compliant to class 134).

For CEN-B, the TX power is set to be compliant to class 122.

Figure 6. Transmitter output voltage (V rms) vs. load current

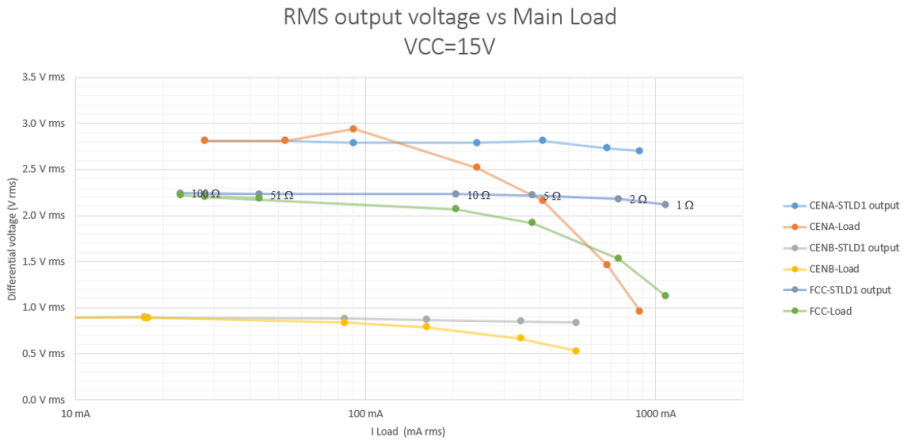


Figure 7. Transmitter output voltage (V p-p) vs. load current

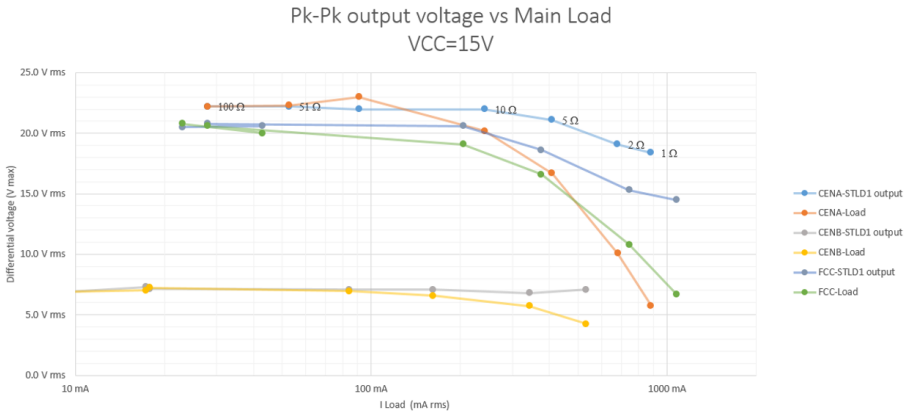


Figure 8. Coupling circuit on EVALKITST8500-1 (STLD1 transmitting between N_PLC_ISO and L_PLC_ISO)

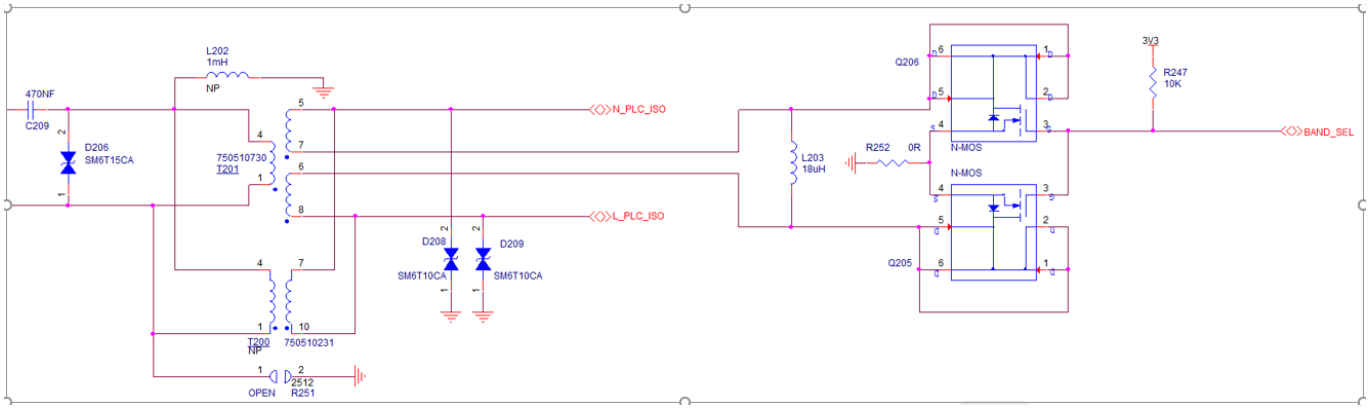
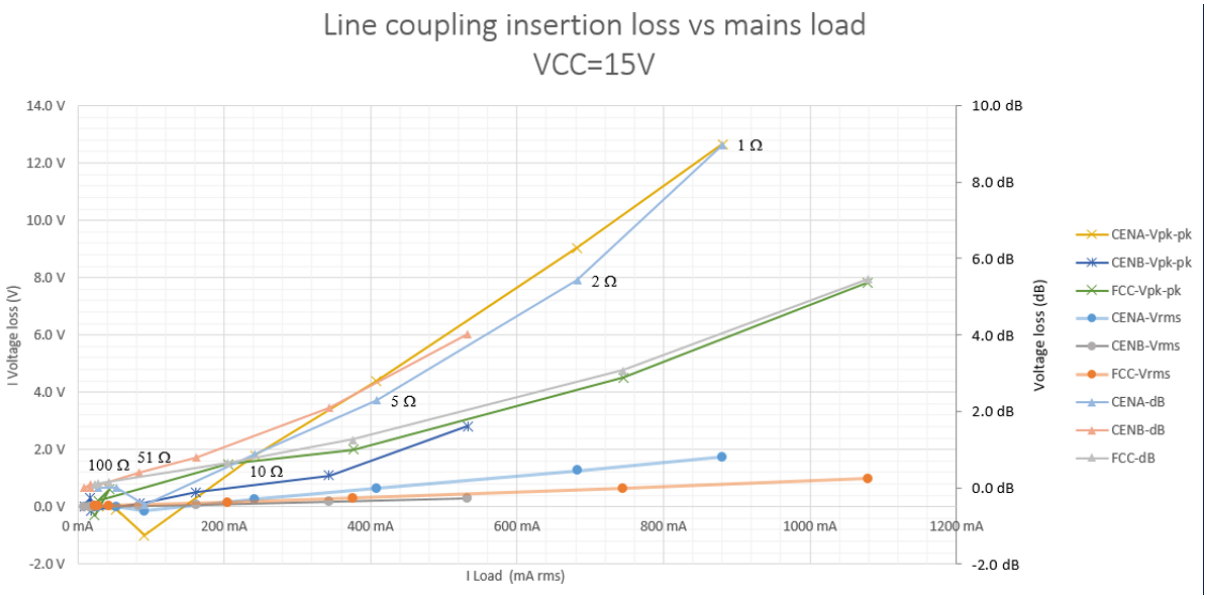


Figure 9 illustrates the difference between the voltage generated by STLD1 and the voltage applied on the load. Those insertion losses are due to the coupling circuit non-negligible impedance.

Figure 9. Line coupling loss vs. mains load



7.2.2 8 V ≤ VCC ≤ 18 V

In order to maximize the TX power, minimize the quantization errors of the DAC and avoid the saturation of the TX chain, the *phyLDVCC* FW parameter can be configured, depending on the VCC voltage provided to the platform:

- *phyLDVCC* = 0x0A for VCC <=10 V
- *phyLDVCC* = 0x0C for VCC <=12 V
- *phyLDVCC* = 0x0F for VCC <=15 V

Table 3 and Table 4 report the RMS and peak-to-peak measurements of the transmitted signal at various stages of the TX chain (DAC, PreDriver, STLD1 and mains) with EVALKITST8500-1 output (J107) connected to CISPR16-1-2 LISN or to 2 Ω load.

For the CENELEC A and FCC bands, we consider different *phyLDVCC* settings and TXPower = 0x20 (maximum configurable value).

For the CENELEC B band, we consider only class 122, so *phyLDVCC* = 0x0A and TXPower = 0x1B.

All results are reported as differential output voltage. The maximum operating values are:

- 1 V pp differential for DAC output
- 6.2 V pp differential for PreDriver output
- 2* (0.8*VCC) V pp differential for STLD1 output

Table 3. TX Power levels (typ) on TX chain vs *phyLDVCC* with CISPR16-1-2 LISN load

Band	*phyLDVCC*	VCC	DAC output		PreDriver output		STLD1 output		Mains (J107)	
			V RMS	V pp	V RMS	V pp	V RMS	V pp	V RMS	V pp
CEN-A	0x0A	10 V	0.10	0.83	0.45	3.69	1.98	16.30	1.99	16.60
	0x0C	12 V	0.11	0.84	0.50	4.25	2.21	18.40	2.23	18.40
	0x0F	15 V	0.11	0.85	0.63	5.13	2.78	22.50	2.79	22.80
CEN-B	0x0A	10 V	0.09	0.78	0.21	1.70	0.89	7.13	0.89	7.25
FCC	0x0A	10 V	0.08	0.78	0.38	3.50	1.59	14.40	1.55	14.70
	0x0C	12 V	0.09	0.79	0.43	3.88	1.79	16.60	1.77	16.90
	0x0F	15 V	0.09	0.80	0.53	4.78	2.23	21.40	2.20	21.30

Table 4. TX Power levels (typ) on TX chain vs *phyLDVCC* with 2 Ω load

Band	*phyLDVCC*	VCC	STLD1 output		Mains (J107)	
			V RMS	V pp	V RMS	V pp
CEN-A	0x0A	10 V	1.94	14.50	1.02	7.30
	0x0C	12 V	2.18	16.30	1.14	8.40
	0x0F	15 V	2.73	18.90	1.42	9.70
CEN-B	0x0A	10 V	0.85	6.80	0.67	5.72
FCC	0x0A	10 V	1.55	10.60	1.12	8.00
	0x0C	12 V	1.74	12.50	1.25	9.10
	0x0F	15 V	2.17	15.30	1.57	11.10

7.3 Output power

Figure 10 illustrates the relationship between the current into the load connected at J107 and:

- the power absorbed from the VCC supply (right Y-axis)
- the power delivered by the STLD1 line driver (left Y-axis)
- the power delivered to the load (left Y-axis)

For CEN-A and FCC, the TX power is at the maximum value (compliant to class 134).
For CEN-B, the TX power is set to be compliant to class 122.

Figure 10. TX power vs. load current

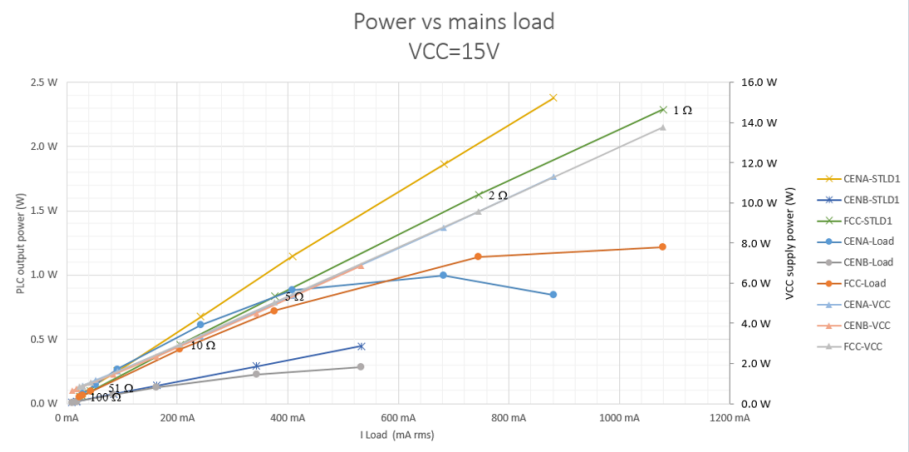
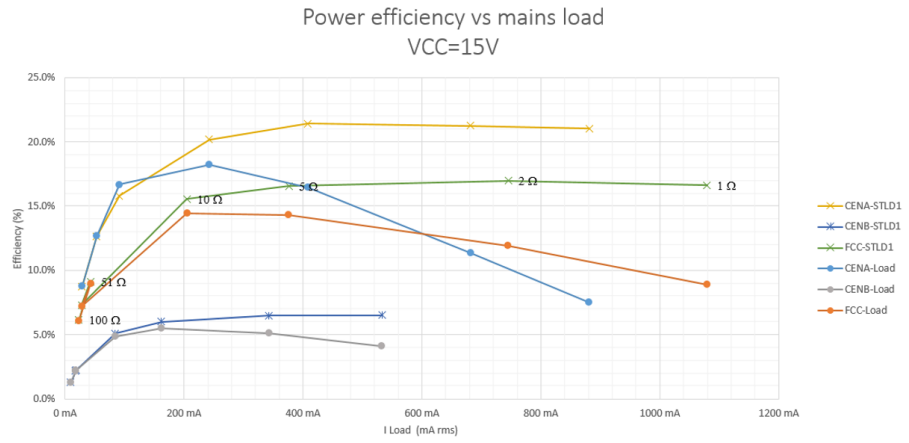


Figure 11 illustrates the efficiency of the STLD1 line driver and the full TX chain (including the losses in the coupling circuit) according to the load connected at J107.

Figure 11. Power efficiency vs. load current

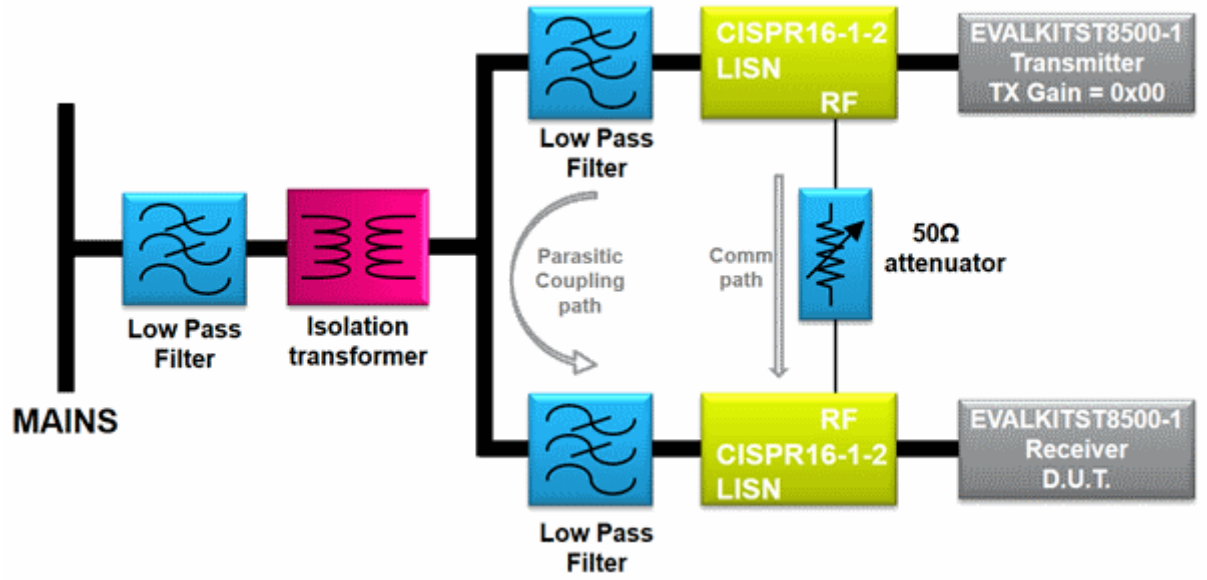


8 Receiver characteristics

8.1 Receiver sensitivity test setup

Because of the very low amplitude of the signals measured in this section, the bench setup of Figure 12 has been used in order to perform reliable measurements.

Figure 12. Bench setup for receiver sensitivity measurement



Instrument references are described in Table 1

One EVALKITST8500-1 is used as a transmitter for sensitivity vs. PER (Packet Error Rate) measurements. Its TX digital gain is set to minimum value in order to keep its output signal as low as possible and minimize the effect of the parasitic coupling paths through LISN and power supply connections.

Measurements of sensitivity vs. modulation are done according to the following procedure:

- Set attenuation = 0 dB
- Measure transmitted signal at receiver D.U.T. input (J107) = $L_{IN(0dB)}$
- Increase attenuation until PER reaches 5% maximum = $Att_{5\%}$
- Calculate RX sensitivity = $L_{IN(0dB)}$ - $Att_{5\%}$

8.2 Input noise level

To reach a good RX sensitivity level, the overall system (AC-DC, DC-DC, PCB layout…) is designed to minimize the noise floor on various bands.

Table 5 gives the noise power measured at ST8500 RX_IN inputs, using an R&S FSU26 spectrum analyzer with integrated Low Noise amplifier and 1141A high impedance differential probe. Also the noise power measured thru a CISPR 16-1-2 LISN is reported.

The measured power is integrated into each band.

Table 5. Input noise level

Parameter	Band	EVALKITST8500-1 noise level	Unit
RX_IN input noise power (Differential)	CEN-A	23	dBµV pk
	CEN-B	15	dBµV pk
	FCC	27	dBµV pk
Noise power measured at CISPR 16-1-2 LISN port	CEN-A	29	dBµV pk
	CEN-B	22	dBµV pk
	FCC	34	dBµV pk

Figure 13. CEN-A RX input noise level

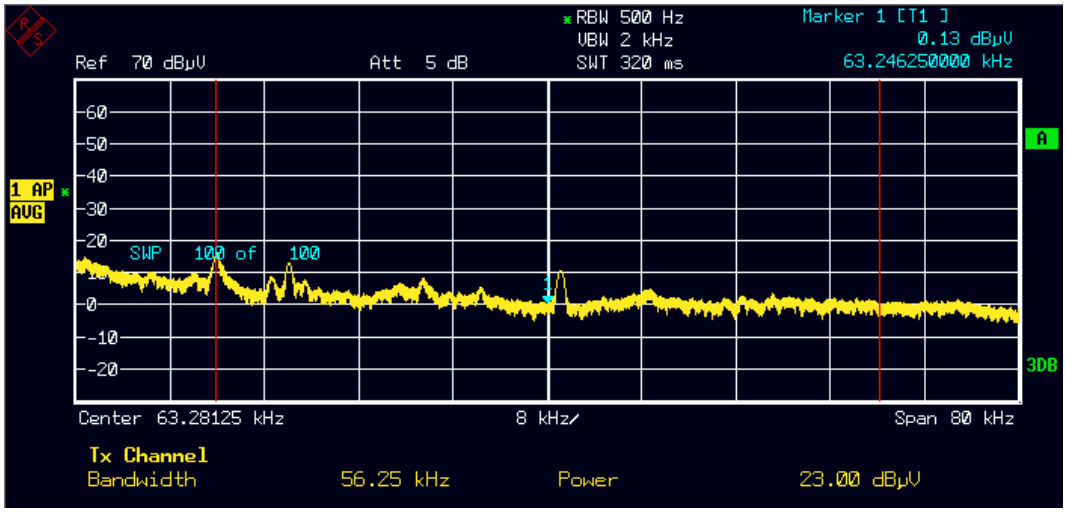


Figure 14. **CEN-B RX input noise level**

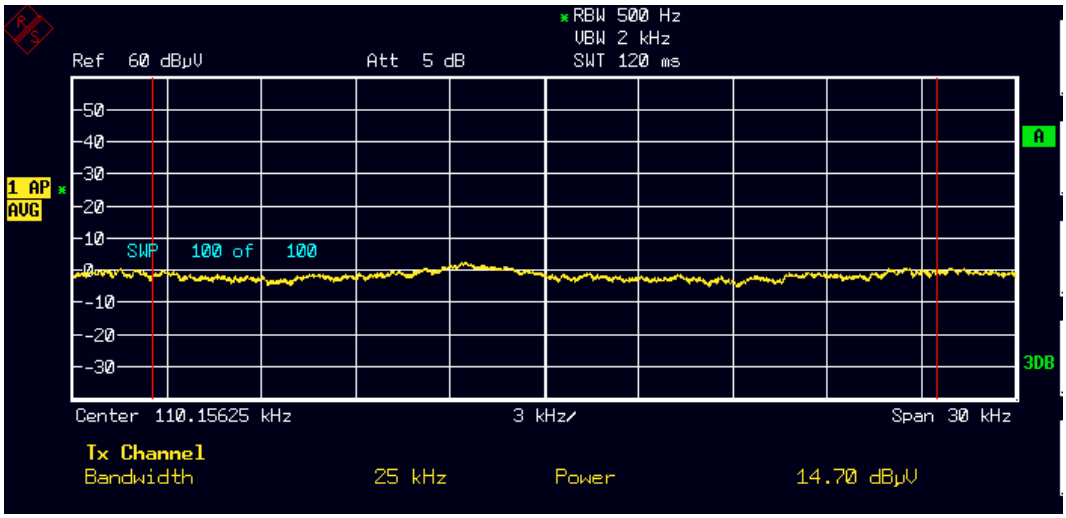
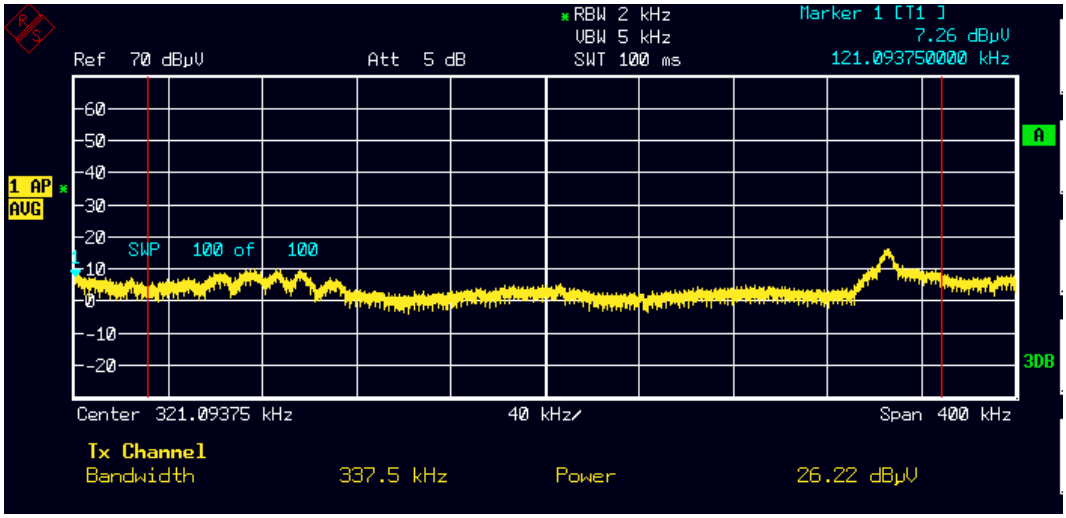


Figure 15. **FCC RX input noise level**



8.3 RX sensitivity level

Table 6 reports the minimum input signal level that can be applied to EVALKITST8500-1 mains connector J107, while guaranteeing a maximum PER of 5% at PHY level.

Table 6. ST8500 development kit sensitivity vs. modul

Parameter	Condition	CEN-A	CEN-B	FCC	Unit
RX sensitivity	ROBO - Coherent - PER < 5%	24	20	30	dBµV
	ROBO - Differential - PER < 5%	25	21	33	dBµV
	BPSK - Coherent - PER < 5%	27	23	35	dBµV
	BPSK - Differential - PER < 5%	30	26	38	dBµV
	QPSK - Coherent - PER < 5%	30	26	38	dBµV
	QPSK - Differential - PER < 5%	33	30	42	dBµV
	8PSK - Coherent - PER < 5%	34	31	42	dBµV
	8PSK - Differential - PER < 5%	40	34	45	dBµV

9 CENELEC and FCC compliance tests

Depending on the frequency band used (CEN-A, CEN-B or FCC), the PLC communication system designed with the ST8500 has to comply with various standards.

Some standards are common to all bands whereas some are specifics to CENELEC or FCC bands.

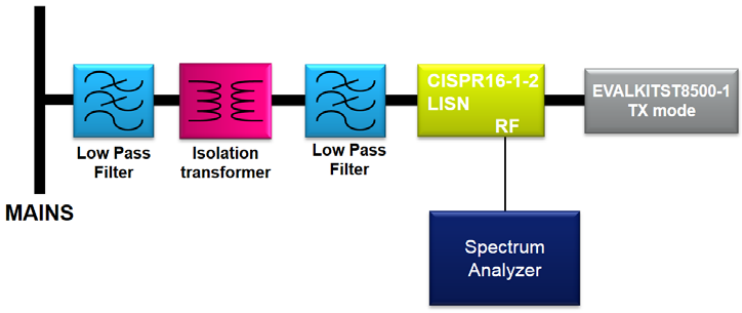
Table 7. List of standard tests required for EMC compliance – subset related to G3-PLC implementation

Type	Reference standard	Test	Applicability	Result
PLC transmission: Conducted measurement	EN 50065-1	Bandwidth measurements	CEN-A, CEN-B	PASS
	EN 50065-1, ITU G.9901	Maximum output levels	ALL	PASS
Conducted disturbance measurements	EN 50065-1, ITU G.9901	Conducted emissions (9 kHz – 30 MHz)	ALL	PASS
Radiated disturbance measurement	EN 50065-1	Radiated emissions (30 MHz – 1 GHz)	ALL	PASS
Conducted immunity	EN 50065-2-3, IEC 61000-4-6	RF conducted signals immunity test (150 kHz – 80 MHz, 10 V rms)	ALL	PASS
	EN 50065-2-3, IEC 61000-4-4	Fast Transients Immunity test (2 kV, 5 kHz)	ALL	PASS
	EN 50065-2-3, IEC 61000-4-5	Surge Immunity test (4 kV, common mode and differential mode)	ALL	PASS
Radiated immunity	EN 50065-2-3, IEC 61000-4-3	RF radiated signals immunity test (80-1000 MHz – 10 V/m)	ALL	PASS
	EN 50065-2-3, IEC 61000-4-2	Electrostatic discharge immunity test (ESD) (+/-8 kV contact, +/-15 kV air discharge)	ALL	PASS
	EN 50065-2-3, IEC 61000-4-8	Power frequency magnetic field immunity test (50 Hz – 100/300 A/m)	ALL	PASS
Input impedance measurement	EN50065-7	RX impedance	CEN-A, CEN-B	PASS
		TX impedance		PASS

9.1 TX conducted emission

The TX conducted emission tests have been performed using the following setup:

Figure 16. Bench setup for TX conducted emission tests



Instrument references are described in Table 1

For all measurement results related to Conducted emission in CEN-A, CEN-B and FCC, refer to the reports available in the ANNEX.

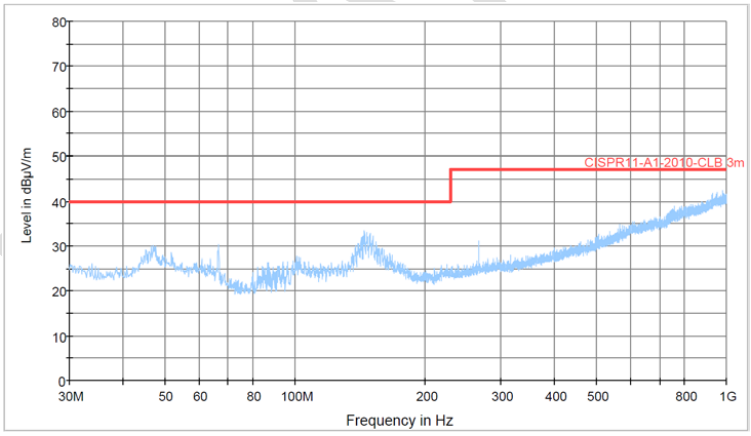
9.2 Radiated disturbance field strength

Figure 17 below illustrates the radiated disturbances generated by the EVALKITST8500-1.

Figure 17. Radiated disturbance (EN50065-1 §7.3)

TEST REQUIREMENT	
Reference standard	EN 50065-1
IMQ operational instruction	IO-80-P10 + IO-80-P11
Test set-up details and procedure	EN 50065-1, sub-clause 7.3
Deviation to test procedure	None
EUT operating condition	# 1 - 2

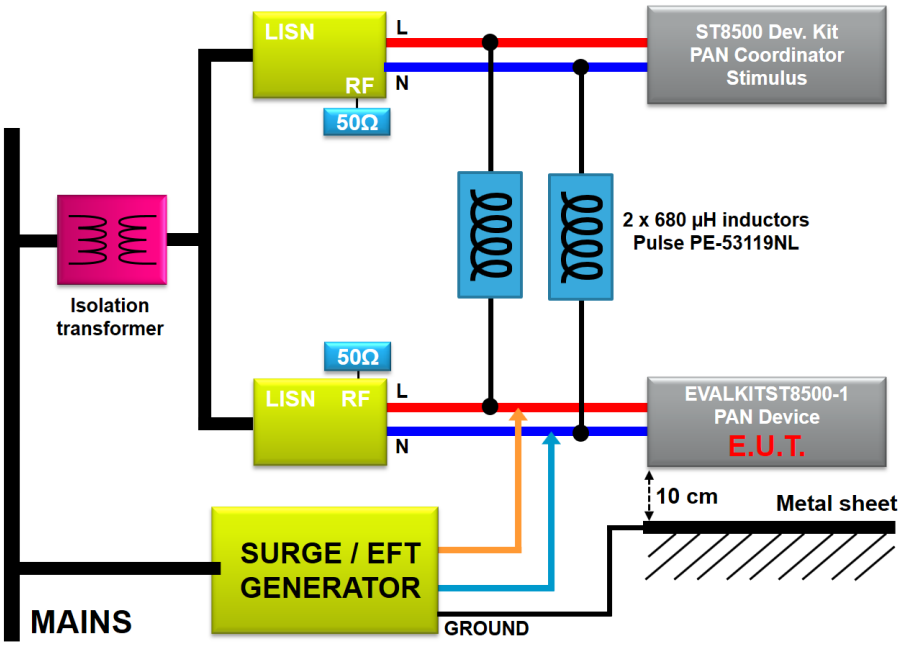
Port	Frequency (MHz)	Limit dB(µV/m)	Comments	Annex	Results
Enclosure	30 ÷ 230	40.5 Quasi-Peak	Since the measurement distance is reduced at 3 meter, the limits are increased by a factor of 10.5 dB.	A	PASS
	230 ÷ 1000	47.5 Quasi-Peak		A	PASS



9.3 Conducted immunity

9.3.1 Electrical fast transients (EFT) and surge immunity

Figure 18. **EFT and surge immunity test setup**



During the EFT and Surge immunity tests, a communication is established between the E.U.T (EVALKITST8500-1) and the stimulus generator (ST8500 Development kit with LCD).

The stimulus acts as a PAN coordinator, and the E.U.T. acts as a PAN device. The coordinator is sending frames to the E.U.T. and expects to receive a frame answer in the reverse direction (“ping”).

The coordinator is displaying on the LCD the total number of transmitted frames and the number of error frames.

9.3.2 Conducted RF signals immunity

Table 8. **Conducted RF signals immunity - test requirements**

TEST REQUIREMENT	
Reference standard	EN 61000-4-6
Test set-up	§ 7
Test specification and procedure	EN 61000-4-6 § 8 and EN 50065-2-3 table
IMQ operational instruction	IO-80-P24 + IO-80-P25
Test supply voltage	230V/50Hz
EUT operating condition	# 1 - 2

Port under test	Test voltage (V(rms)) (unmodulated)	Modulation during the test	Coupling mode	Performance criteria	Results
AC mains	10	AM, 80 %, 1 kHz sinewave	☒ CDN ☐ Inductive clamp	A	PASS

Frequency step: 1%
Actuation time: 3 seconds

9.4 Radiated immunity

9.4.1 Power frequency magnetic field immunity

Table 9. **Power frequency magnetic field immunity**

TEST REQUIREMENT	
Reference standard	EN 61000-4-8
Test set-up	§ 7
Test specification and procedure	EN 61000-4-8 § 8 and EN 50065-2-3 table 1
IMQ operational instruction	IO-80-P31
Test supply voltage	230V/50Hz
EUT operating condition	# 1 - 2

Frequency (Hz)	Test magnetic field (A/m (rms))	Performance criteria	Results
50	100	A	PASS
50	300	B	PASS

9.4.2 Radiated RF electromagnetic field immunity

Table 10. **Radiated RF electromagnetic field immunity**

TEST REQUIREMENT	
Reference standard	EN 61000-4-3
Test set-up	§ 7
Test specification and procedure	EN 61000-4-3 § 8 and EN 50065-2-3 table 1
IMQ operational instruction	IO-80-P21 + IO-80-P22
Test supply voltage	230V/50Hz
EUT operating condition	# 1 - 2

Frequency (MHz)	Test field strength (V/m (rms)) (unmodulated)	Modulation during the test	Performance criteria	Results
80 ÷ 1000	10	AM, 80 %, 1 kHz sinewave	A	PASS

Frequency (MHz)	Test field strength (V/m (rms)) (unmodulated)	Modulation during the test	Performance criteria	Results
900 ± 5	10	50 %, 200 Hz modulated	A	PASS

Frequency step: 1%
Actuation time: 3 seconds

REMARKS
Observed performance criterion: A The apparatus continue to operate during and after the test. No degradation of performance are observed

9.5 Equipment impedance

For a PLC node, particular attention must be paid to the impedance of the line coupling circuit. Specifically:

• In receiving (idle) mode, the coupling impedance must be high enough to make the power line source impedance negligible and to minimize the mutual interference between different PLC nodes connected to the same network

• In transmitting mode, the coupling impedance must be very low inside the signal bandwidth but high enough for out-of-band frequencies.

According to such requirements, the EN50065-7 standard document fixes the limits for the PLC node operating in the CENELEC band:

- In Table 11 are the limits and in Figure 19 the measurement results for the CEN-A band
- In Table 12 are the limits and in Figure 20 the measurement results for the CEN-B band

Please note that there are no specific limits defined for FCC, but Figure 21 presents the impedance measurement results for FCC as well.

Those measurements have been performed using the voltage ratio method, as described in Annex D of EN50065-7 standard.

Table 11. Minimum impedance for CEN_A band (35.9375 kHz to 90.625 kHz) equipment

Frequency range	3-9 kHz	9-35.9375 kHz	35.9375-90.625 kHz	90.625-95 kHz	95-148.5 kHz
Out BW	Out BW	In BW	Out BW	Out BW	
Rx mode	10 Ω	Free (10 Ω recommended)	50 Ω	Free (10 Ω recommended)	5 Ω
Tx mode	Free	Free	Free	Free	3 Ω

Figure 19. EVALKITST8500 Rx/Tx impedance measurement – CEN-A

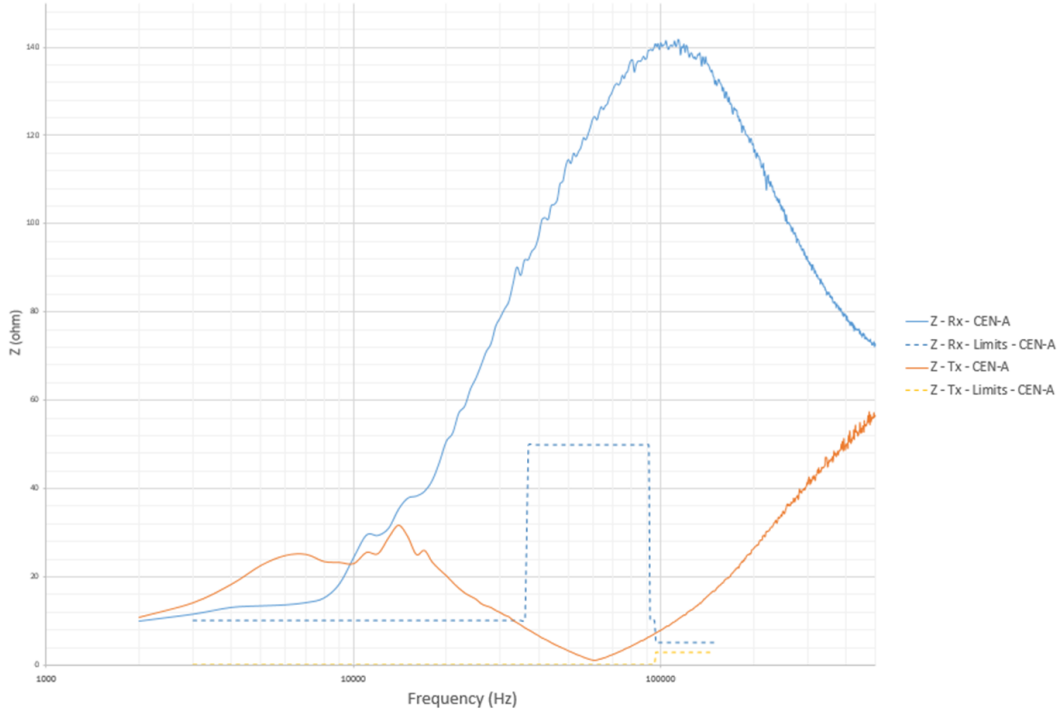


Table 12. Minimum impedance for CEN-B band (98.4375 kHz to 121.875 kHz) equipment

Frequency range	3-9 kHz	9-95 kHz	95-148.5 kHz
Rx mode	10 Ω	5 Ω	5 Ω
Tx mode	10 Ω	5 Ω	Free

Figure 20. **EVALKITST8500 Rx/Tx impedance measurement – CEN-B**

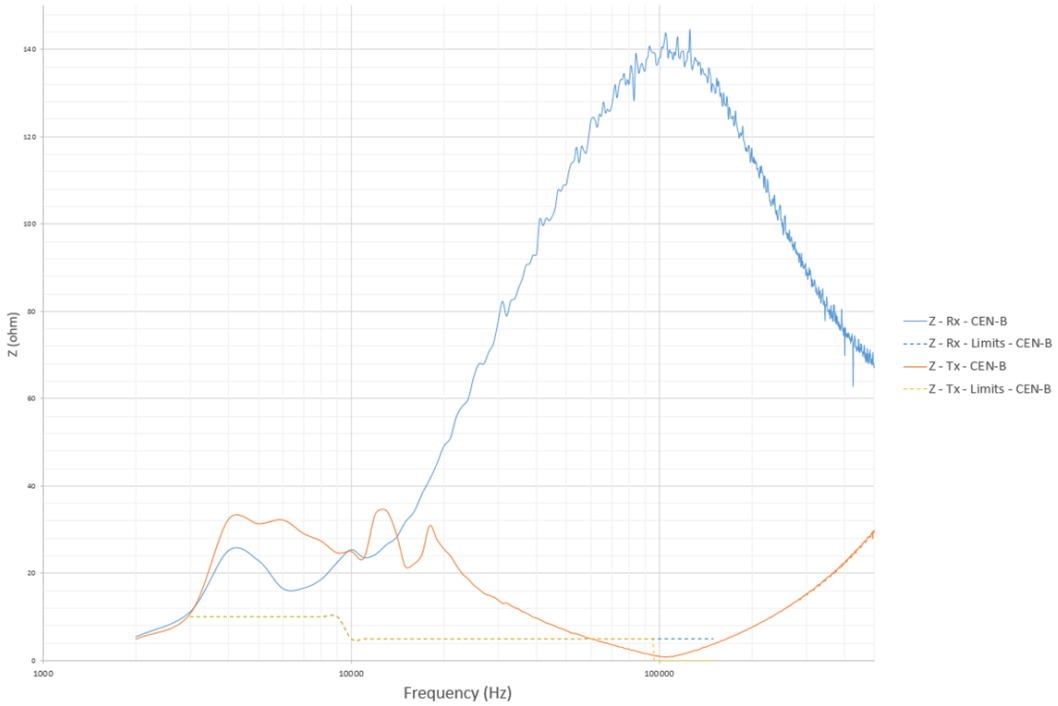
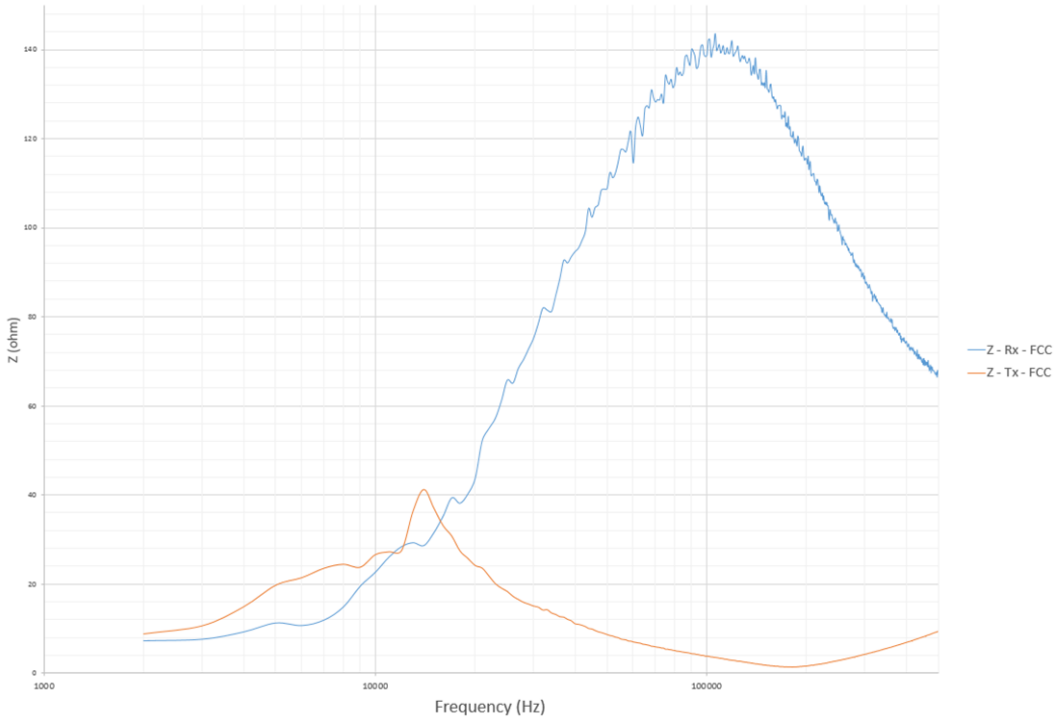


Figure 21 shows that the input impedance magnitude vs. frequency measured in reception and transmission mode, for CEN-B band, is compliant with the EN50065-7 limits.

Figure 21. **EVALKITST8500 Rx/Tx impedance measurement – FCC**



10 Other PLC standard requirements

Depending on the country of PLC deployment, and on the frequency band, the systems may need to fulfill other standard requirements.

Those standards may specify more tests to check the PLC performance against various load, attenuation and noise conditions.

The EVALKITST8500-1 is also internally tested to comply with the requirements listed hereafter.

10.1 G3 Performance tests

The G3 Alliance defines the performance test suite used for certification of G3-PLC devices.

It covers various PLC performance tests to check that the G3 products comply with requirements such as:

- TX performance on low impedance conditions
- RX performance in various conditions (no noise, white noise, narrow-band noise, impulsive broadband noise, etc.)
- Timing and data rate performance

For further information, please refer to the official G3 Alliance website http://www.g3-plc.com/home/

10.2 ETSI TS 103 909

This Technical Specification [4] ETSI TS 103 909 defines some test methods to check the performance of PLC equipment operating in the range from 9 to 500 kHz.

Link Budget (LB) and Data Rate (DR) are assessed against several types of impairments, such as:

- Periodic impulse noise
- Random impulse noise
- Tonal noise

For further information, please refer to the ETSI website www.etsi.org .

11 References

[1] ST8500 datasheet on www.st.com
[2] ST8500 Application Note AN5120 on www.st.com
[3] EVALKITST8500-1 user manual, schematics, PCB layout on www.st.com
[4] ETSI TS 103 909

12 Normative references

EN50065: Signaling on low voltage electrical installations in the frequency range 3 kHz to 148.5 kHz.

- Part 1 : General requirements, frequency bands and electromagnetic disturbances
- Part 2-3 : Immunity requirements
- Part 4-2 : Low voltage decoupling filters - Safety requirements
- Part 7 : Equipment impedance

IEC 61000-4 : Electromagnetic compatibility (EMC)

- Part 4-2 : 2 Radiated, radio-frequency, electromagnetic field immunity test
- Part 4-3 : 3 Radiated, radio-frequency, electromagnetic field immunity test
- Part 4-4 : Electrical fast transient/burst immunity test
- Part 4-5 : Surge immunity test
- Part 4-6 : Immunity to conducted disturbances, induced by radio-frequency fields

13 Annex A - CEN-A TX conducted emission test report

Figure 22. **ANNEX A - CEN-A TX conducted emission test report**

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EN50065-1 PHY compliancy - §6.2 & §6.3

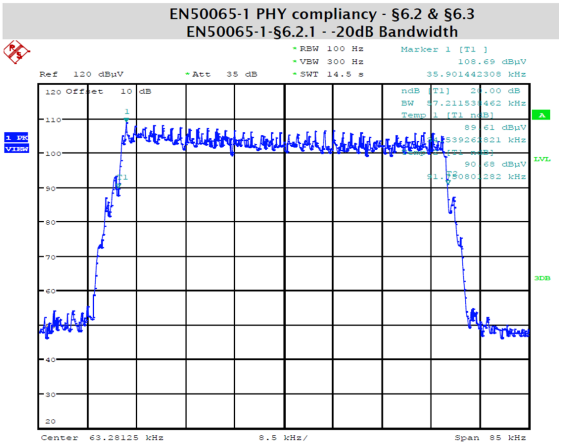
PASS

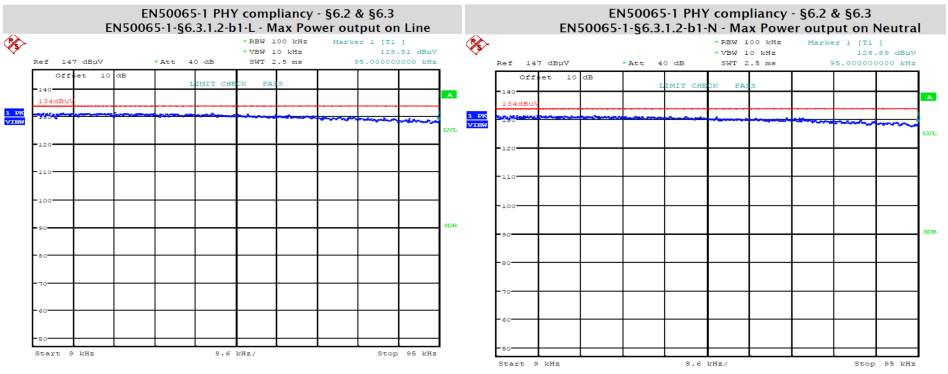
Test Parameters		
Band	CENA	
IFS	4	ms
Modulation	DROBO	
Class	134	

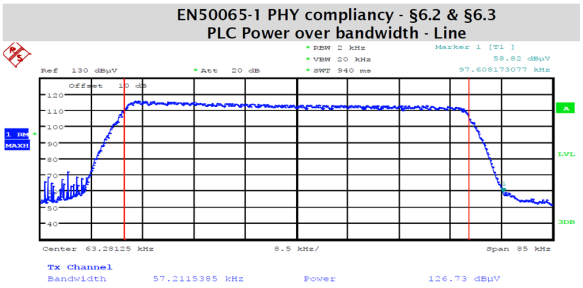
Started	2018/02/02 11:09:20
Ended	2018/02/02 11:19:24
Duration	00:10:0

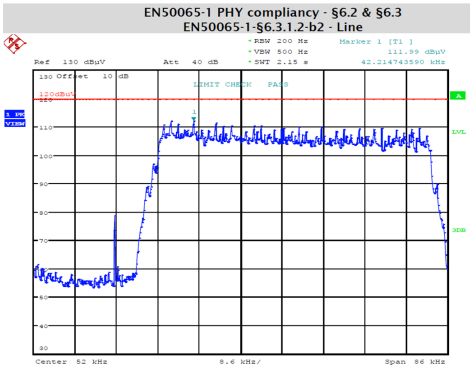
Test Description
Goal of the test is to check the DUT is compliant to the EN50065-1 standard : §6.2 and §6.3

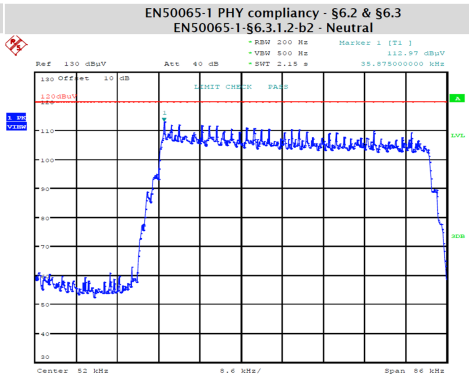
Time	Test	Spec Item	AC wire	Result	Unit	EN50065-1 Limit (from spec sheet)	Limit PASS	Picture	PLC command	Verdict
11:12:59	PLC PHY signal -20dB Bandwidth	EN50065-1_6.2.1	Line	57211.5	Hz	60000		Pic1	plc perf 0 65535 4 133 0x0000 32 0x3f	PASS
11:14:04	Max output power - L	EN50065-1_6.3.1.2-b1-134	Line			134	True	Pic2	plc perf 0 65535 4 133 0x0000 32 0x3f	PASS
11:15:07	Max output power - N	EN50065-1_6.3.1.2-b1-134	Neutral			134	True	Pic3	plc perf 0 65535 4 133 0x0000 32 0x3f	PASS
11:16:12	PLC PHY signal power integrated over bandwidth - L	EN50065-1_6.3.1.2-b1-134	Line	126.7	dBµV	134		Pic4	plc perf 0 65535 4 133 0x0000 32 0x3f	PASS
11:17:14	PLC PHY signal power integrated over bandwidth - N	EN50065-1_6.3.1.2-b1-134	Neutral	126.8	dBµV	134		Pic5	plc perf 0 65535 4 133 0x0000 32 0x3f	PASS
11:18:20	Max output power - RBW=200Hz - L	EN50065-1_6.3.1.2-b2	Line			120	True	Pic6	plc perf 0 65535 4 133 0x0000 32 0x3f	PASS
11:19:23	Max output power - RBW=200Hz - N	EN50065-1_6.3.1.2-b2	Neutral			120	True	Pic7	plc perf 0 65535 4 133 0x0000 32 0x3f	PASS

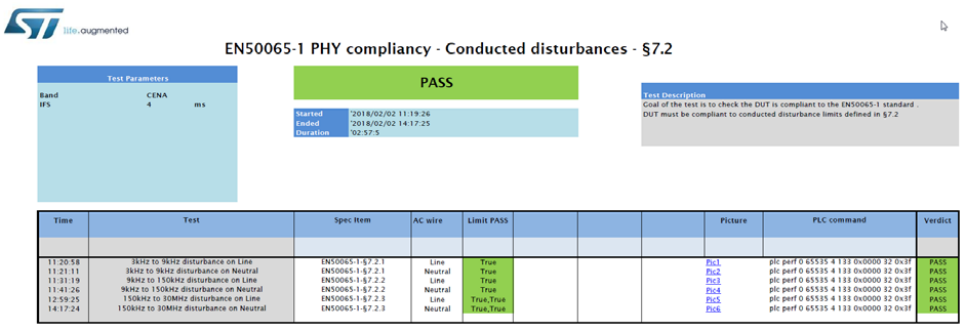


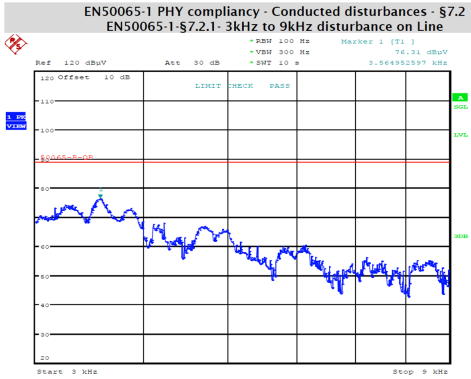


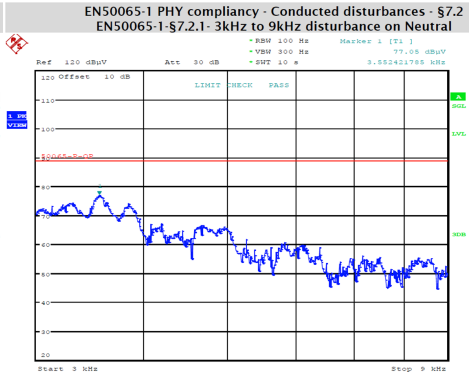

EN50065-1 PHY compliancy - §6.2 & §6.3
PLC Power over bandwidth - Line
Tx Channel
Bandwidth 57.2115385 kHz
Power 126.73 dBuV

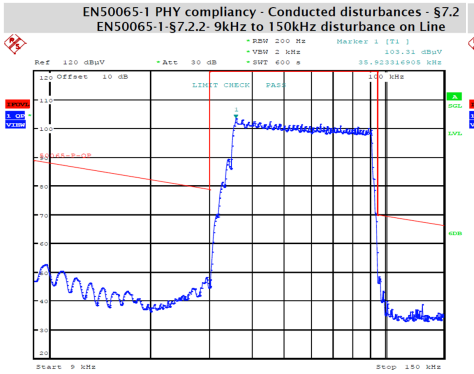

EN50065-1 PHY compliancy - §6.2 & §6.3
EN50065-1-§6.3.1.2-b2 - Line

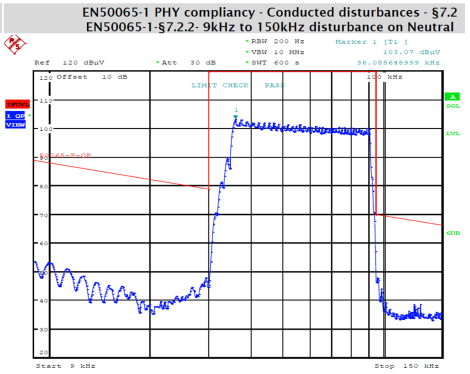

EN50065-1 PHY compliancy - §6.2 & §6.3
EN50065-1-§6.3.1.2-b2 - Neutral

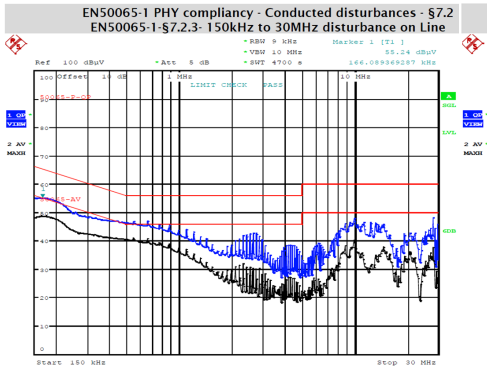

EN50065-1 PHY compliancy - Conducted disturbances - §7.2
Test Parameters
Band CENA
IFS 4 ms
PASS
Started 2018/02/02 11:19:26
Ended 2018/02/02 14:17:25
Duration 02:57:5
Test Description
Goal of the test is to check the DUT is compliant to the EN50065-1 standard .
DUT must be compliant to conducted disturbance limits defined in §7.2
Time
Test
Spec Item
AC wire
Limit PASS
Picture
PLC command
Verdict
11:20:58 3kHz to 9kHz disturbance on Line EN50065-1-§7.2.1 Line True Pic1 plc perf 0 65535 4 133 0x0000 32 0x3f PASS
11:21:11 3kHz to 9kHz disturbance on Neutral EN50065-1-§7.2.1 Neutral True Pic2 plc perf 0 65535 4 133 0x0000 32 0x3f PASS
11:31:19 9kHz to 150kHz disturbance on Line EN50065-1-§7.2.2 Line True Pic3 plc perf 0 65535 4 133 0x0000 32 0x3f PASS
11:41:26 9kHz to 150kHz disturbance on Neutral EN50065-1-§7.2.2 Neutral True Pic4 plc perf 0 65535 4 133 0x0000 32 0x3f PASS
12:59:25 150kHz to 30MHz disturbance on Line EN50065-1-§7.2.3 Line True,True Pic5 plc perf 0 65535 4 133 0x0000 32 0x3f PASS
14:17:24 150kHz to 30MHz disturbance on Neutral EN50065-1-§7.2.3 Neutral True,True Pic6 plc perf 0 65535 4 133 0x0000 32 0x3f PASS

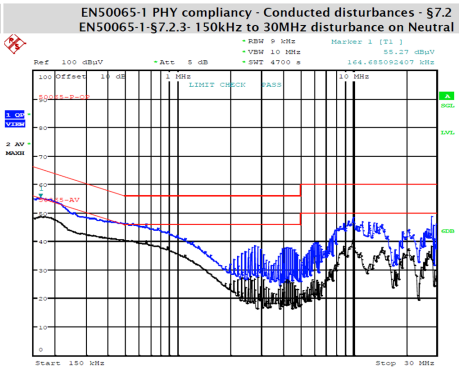

EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.1- 3kHz to 9kHz disturbance on Line


EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.1- 3kHz to 9kHz disturbance on Neutral


EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.2- 9kHz to 150kHz disturbance on Line
LIMIT CHECK PASS
Start 9 kHz
Stop 150 kHz


EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.2- 9kHz to 150kHz disturbance on Neutral
LIMIT CHECK PASS
Start 9 kHz
Stop 150 kHz


EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.3- 150kHz to 30MHz disturbance on Line
LIMIT CHECK PASS
Start 150 kHz
Stop 30 MHz


EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.3- 150kHz to 30MHz disturbance on Neutral
LIMIT CHECK PASS
Start 150 kHz
Stop 30 MHz

14 Annex B - CEN-B TX conducted emission test report

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EN50065-1 PHY compliancy - §6.2 & §6.3

Test Parameters		
Band	CENB	
IFS	4	ms
Modulation	DROBO	
Class	122	

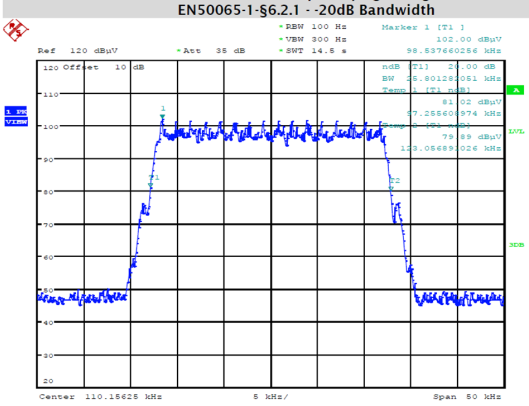
PASS

Started	'2017/10/20 14:02:07
Ended	'2017/10/20 14:11:03
Duration	'00:08:5

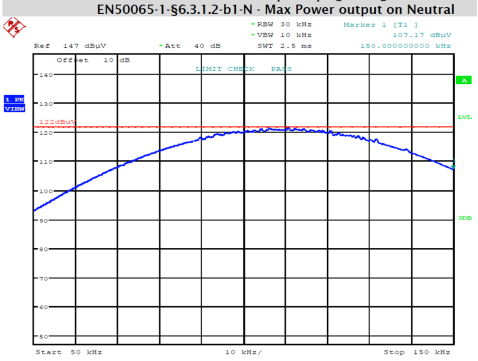
Test Description
Goal of the test is to check the DUT is compliant to the EN50065-1 standard : §6.2 and §6.3

Time	Test	Spec Item	AC wire	Result	Unit	EN50065-1 Limit	Limit PASS	Picture	PLC command	Verdict
						from spec sheet				
14:06:10	PLC PHY signal -20dB Bandwidth	EN50065-1_6.2.1	Line	25801.3	Hz	60000		Pic1	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
14:07:51	Max output power - L	EN50065-1_6.3.1.2-b1-122	Line			122	True	Pic2	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
14:08:54	Max output power - N	EN50065-1_6.3.1.2-b1-122	Neutral			122	True	Pic3	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
14:09:59	PLC PHY signal power integrated over bandwidth - L	EN50065-1_6.3.1.2-b1	Line	117.7	dBµV	122		Pic4	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
14:11:02	PLC PHY signal power integrated over bandwidth - N	EN50065-1_6.3.1.2-b1	Neutral	117.8	dBµV	122		Pic5	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS

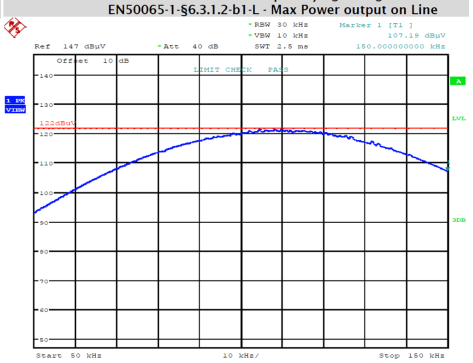
EN50065-1 PHY compliancy - §6.2 & §6.3
EN50065-1-§6.2.1 - -20dB Bandwidth

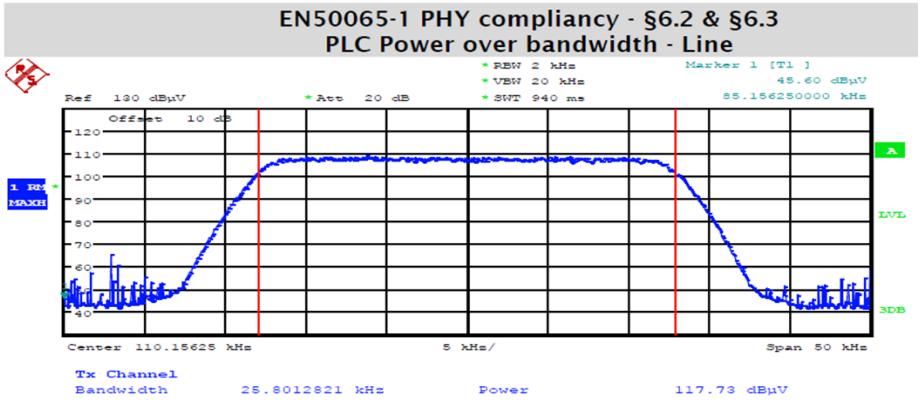


EN50065-1 PHY compliancy - §6.2 & §6.3
EN50065-1-§6.3.1.2-b1-N - Max Power output on Neutral



EN50065-1 PHY compliancy - §6.2 & §6.3
EN50065-1-§6.3.1.2-b1-L - Max Power output on Line





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EN50065-1 PHY compliancy - Conducted disturbances - §7.2

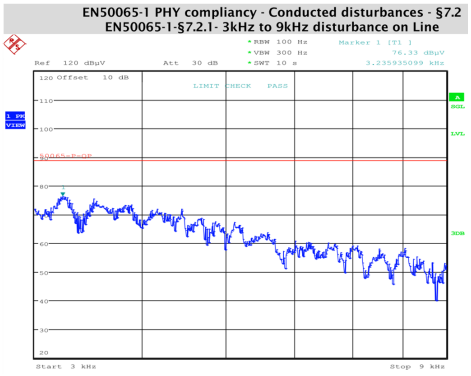
Test Parameters		
Band	CENB	
IFS	4	ms

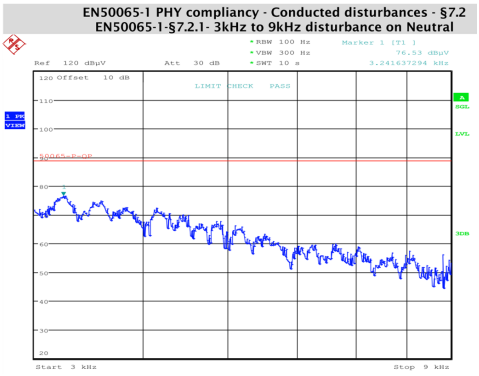
PASS

Started	'2017/10/19 18:34:03
Ended	'2017/10/19 21:32:27
Duration	'02:58:2

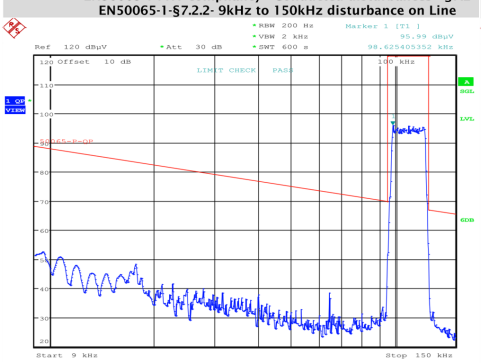
Test Description
Goal of the test is to check the DUT is compliant to the EN50065-1 standard .
DUT must be compliant to conducted disturbance limits defined in §7.2

Time	Test	Spec Item	AC wire	Limit PASS				Picture	PLC command	Verdict
18:35:58	3kHz to 9kHz disturbance on Line	EN50065-1-§7.2.1	Line	True				Pic1	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
18:36:12	3kHz to 9kHz disturbance on Neutral	EN50065-1-§7.2.1	Neutral	True				Pic2	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
18:46:20	9kHz to 150kHz disturbance on Line	EN50065-1-§7.2.2	Line	True				Pic3	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
18:56:27	9kHz to 150kHz disturbance on Neutral	EN50065-1-§7.2.2	Neutral	True				Pic4	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
20:14:27	150kHz to 30MHz disturbance on Line	EN50065-1-§7.2.3	Line	True,True				Pic5	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS
21:32:26	150kHz to 30MHz disturbance on Neutral	EN50065-1-§7.2.3	Neutral	True,True				Pic6	plc perf 0 65535 4 54 0x0000 28 0x0f	PASS

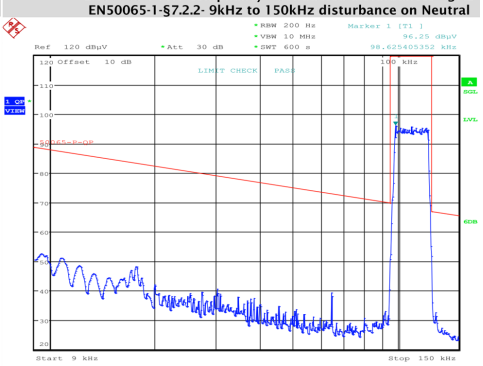




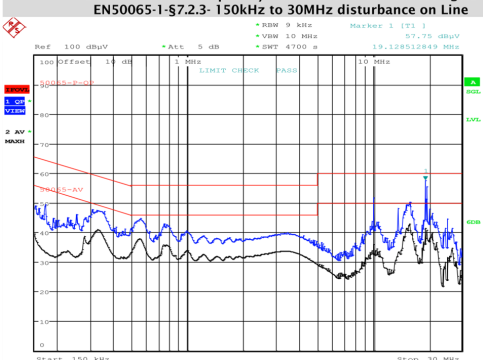
EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.2- 9kHz to 150kHz disturbance on Line



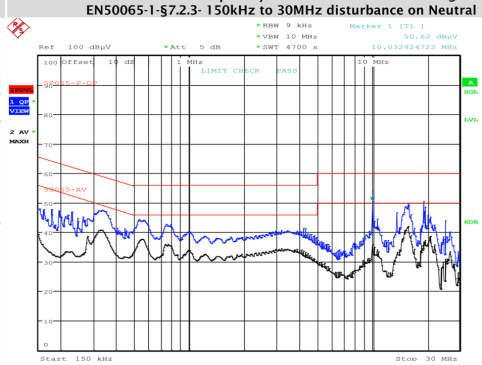
EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.2- 9kHz to 150kHz disturbance on Neutral



EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.3- 150kHz to 30MHz disturbance on Line



EN50065-1 PHY compliancy - Conducted disturbances - §7.2
EN50065-1-§7.2.3- 150kHz to 30MHz disturbance on Neutral



15 Annex C - FCC TX conducted emission test report

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G.9901 FCC PHY compliancy - Conducted disturbances - §6 and 7

Test Parameters		
Band	FCC	
IFS	4	ms

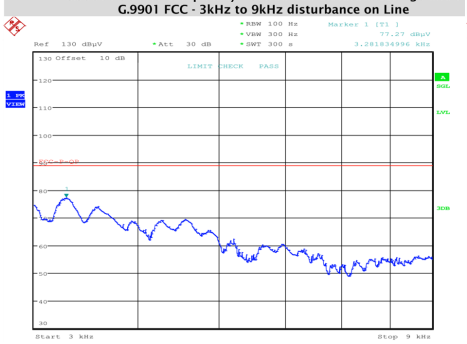
PASS

Started	'2018/02/02 15:43:20
Ended	'2018/02/02 19:04:22
Duration	'03:21:0

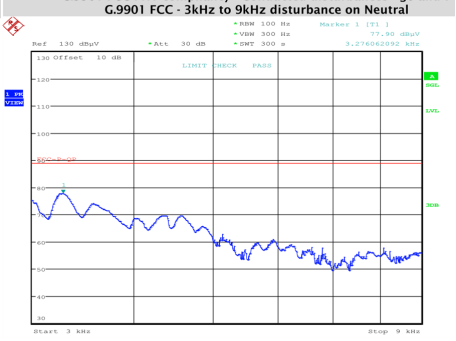
Test Description
Goal of the test is to check the DUT is compliant to the G9901 standard .
DUT must be compliant to conducted disturbance limits defined in §6 and 7

Time	Test	Spec Item	AC wire	Limit PASS				Picture	PLC command	Verdict
15:49:46	3kHz to 9kHz disturbance on Line	G.9901 §6	Line	True				Pic1	plc perf 0 65535 4 460 0x0000 32 0xffffffff	PASS
15:54:53	3kHz to 9kHz disturbance on Neutral	G.9901 §6	Neutral	True				Pic2	plc perf 0 65535 4 460 0x0000 32 0xffffffff	PASS
16:11:40	9kHz to 535kHz disturbance on Line	G.9901 §6-7	Line	True				Pic3	plc perf 0 65535 4 460 0x0000 32 0xffffffff	PASS
16:28:25	9kHz to 535kHz disturbance on Neutral	G.9901 §6-7	Neutral	True				Pic4	plc perf 0 65535 4 460 0x0000 32 0xffffffff	PASS
17:46:24	150kHz to 30MHz disturbance on Line	G.9901 §7	Line	True,True				Pic5	plc perf 0 65535 4 460 0x0000 32 0xffffffff	PASS
19:04:21	150kHz to 30MHz disturbance on Neutral	G.9901 §7	Neutral	True,True				Pic6	plc perf 0 65535 4 460 0x0000 32 0xffffffff	PASS

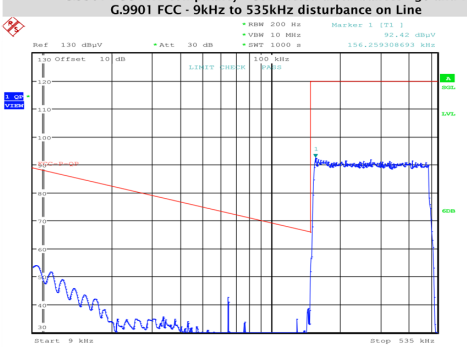
G.9901 FCC PHY compliancy - Conducted disturbances - §6 and 7
G.9901 FCC - 3kHz to 9kHz disturbance on Line



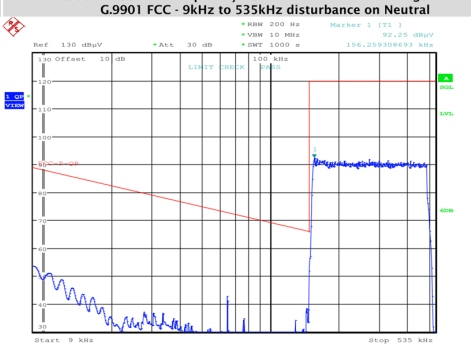
G.9901 FCC PHY compliancy - Conducted disturbances - §6 and 7
G.9901 FCC - 3kHz to 9kHz disturbance on Neutral



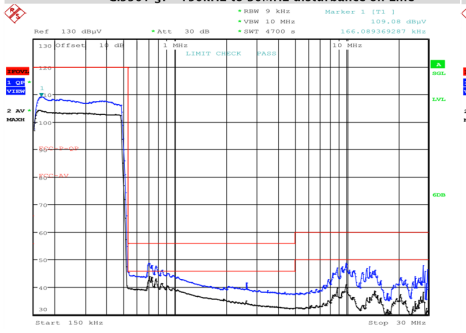
G.9901 FCC PHY compliancy - Conducted disturbances - §6 and 7
G.9901 FCC - 9kHz to 535kHz disturbance on Line



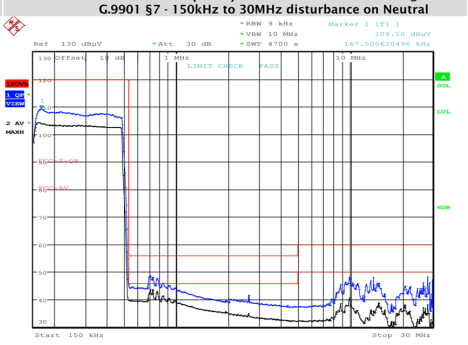
G.9901 FCC PHY compliancy - Conducted disturbances - §6 and 7
G.9901 FCC - 9kHz to 535kHz disturbance on Neutral



G.9901 FCC PHY compliancy - Conducted disturbances - §6 and 7
G.9901 §7 - 150kHz to 30MHz disturbance on Line



G.9901 FCC PHY compliancy - Conducted disturbances - §6 and 7
G.9901 §7 - 150kHz to 30MHz disturbance on Neutral



Revision history

Table 13. **Document revision history**

Date	Version	Changes
14-Jan-2021	1	Initial release.

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