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Application note

Designing digital outputs for factory automation

Introduction

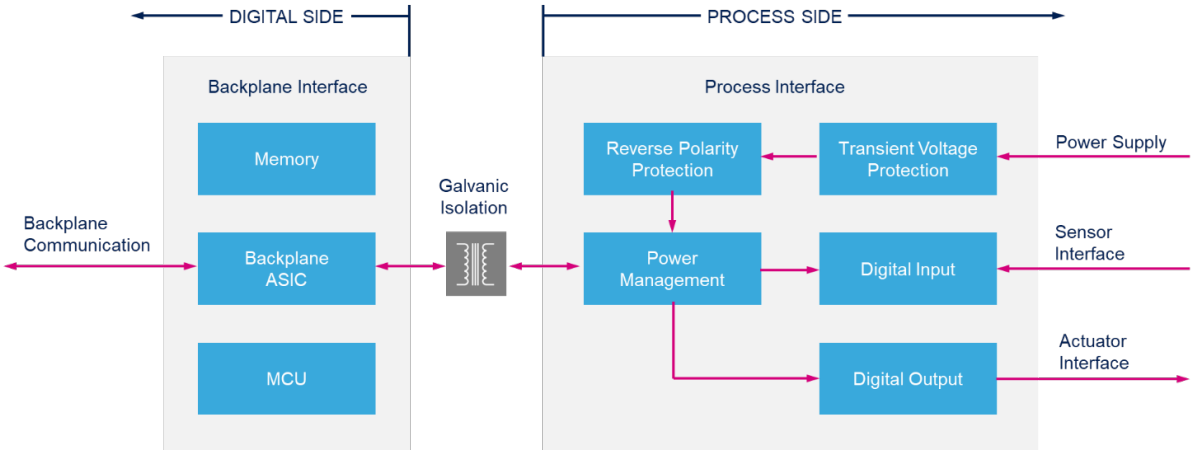
Factory automation systems are raising the technical and functional complexity of front-line elements like sensors and actuators, and the digital I/O modules that control them must balance performance, diagnostics and reliability aspects with power consumption, form factor and cost.

It is important to appreciate certain aspects of digital I/O module architecture in Programmable Logic Controllers (PLC) and how appropriate semiconductor power component selection can help build viable applications that meet stringent industrial standards requirements.

1 Digital I/O module architecture

The functional, electrical and technical requirements surrounding digital I/O modules are defined in the industrial standard IEC 61131-2 (Programmable Controllers).

Figure 1. Digital I/O module architecture



The above diagram shows the common functional blocks found in most digital I/O modules, even if real implementations vary in terms of integration and certain application-specific features.

For instance, the galvanic isolation necessary for protecting sensitive high-speed digital circuits on the Digital side from the electrical transients in the power components on the Process side can be either implemented using separate circuitry with optocouplers or digital isolators, or may be embedded in integrated I/O chips.

Furthermore, the configuration of digital inputs (DI) and outputs (DO) typically varies in balance and granularity.

1.1 Process side and Digital side design

Any discussion regarding Digital side design will generally revolve around application-specific considerations, while the design of robust digital output modules on the Process side are largely always relevant as these sections are often heavily exposed to electrical overstress.

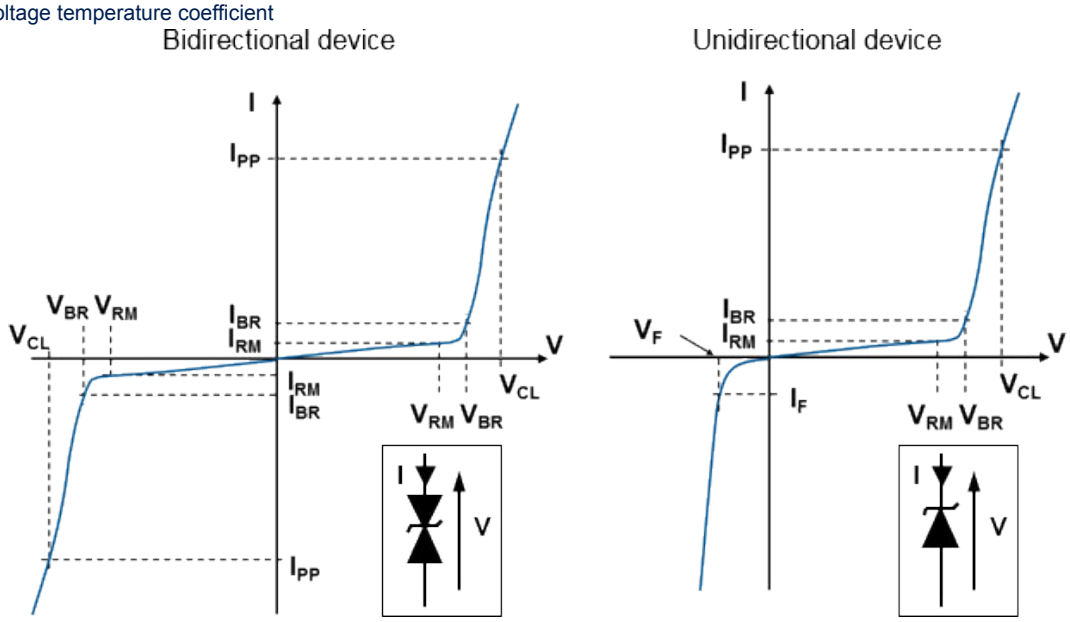
2 Transient voltage protection

The Process side often involves various forms of electrical overstress deriving from switching high currents in installations with long wiring that drive valves and heavy servodrives.

A Transil or Transient Voltage Suppressor (TVS), is typically used to protect the application against transient overvoltage caused by electrostatic discharge (ESD), electrical fast transients (EFT) and high-power surge pulses. This device is specifically designed to sustain high peak current I_{PP} during the transient pulse and to clamp the voltage at a certain limiting level V_{CL} . When the power limit of a TVS is exceeded, Transil electrodes are designed to short-circuit in order to protect the application circuitry and prevent further overvoltage.

Figure 2. TVS characteristic parameters

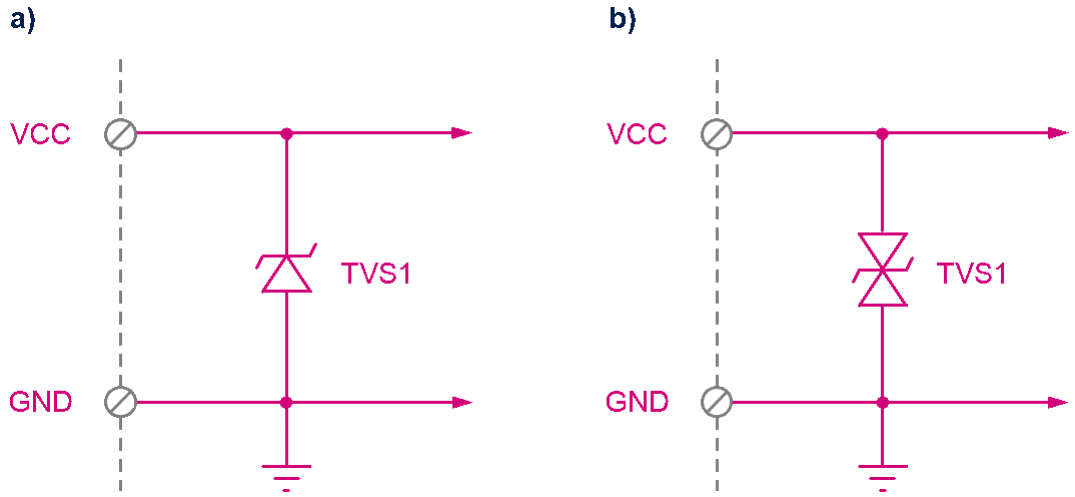
V_{RM} = maximum stand-off voltage
I_{RM} = maximum leakage current at V_{RM}
I_{BR} = breakdown current
V_{BR} = breakdown voltage at I_{BR}
I_{PP} = peak pulse current
V_{CL} = clamping voltage at I_{PP}
R_D = dynamic resistance
I_F = forward current
V_F = forward voltage drop at I_F
αT = voltage temperature coefficient



A TVS in a power supply circuitry can be either unidirectional or bidirectional.

Figure 3. **Unidirectional and bidirectional TVS**

a) unidirectional TVS
b) bidirectional TVS

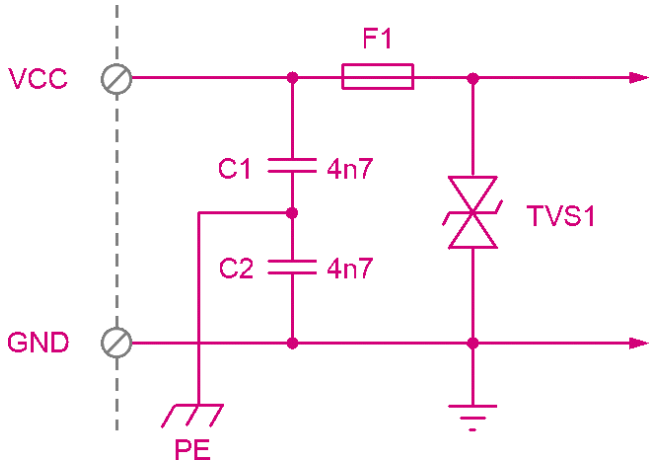


The voltage in unidirectional TVS is clamped at V_{CL} when the Transil is exposed to a positive pulse (i.e., TVS is reverse-biased), while it produces a voltage drop V_F when exposed to a negative overstress, like a diode. The unidirectional TVS clamps negative surges at a lower voltage and provides better overstress protection for surrounding ICs, but it does not provide immunity to reverse polarity voltage on power supply terminals when, for example, the system is wired incorrectly.

A bidirectional Transil with symmetrical V/I characteristics should instead be used in applications that do not include failsafe mechanisms against reverse connection like modules with backplane power supply. Such applications must, however, implement reverse polarity protection against negative transients.

The following figure shows a complete transient voltage protection scheme with additional capacitors C1 and C2 providing a defined coupling with the protective earth terminal (PE) of the application as well as a common mode (CM) noise filter.

Figure 4. **Transient voltage protection scheme**



To prevent damage in the event of TVS breakdown, an appropriate fuse F1 with respect to the nominal and peak current characteristics may be inserted on the VCC path to disconnect the circuit from power supply once the TVS is shorted.

TVS selection is based on application supply voltage VCC and type and level of disturbance signals to be suppressed. The protection device behaves as an open circuit under normal operating conditions and carries the disturbance current away in the event of electrical overstress.

The supply voltage range for Programmable Controllers is given as follows:

$$V_{CC} = 24V - 15\%/ + 20\% = \ < 20.4V, 28.8V >$$

Therefore, for the TVS:

$$V_{BR} > V_{CC,\,max}$$

where V_{BR} is voltage level at which TVS starts to conduct (~1mA).

Depending on application requirements, the stand-off voltage value V_{RM} can be used instead, which guarantees a TVS current of only 1 µA.

The ST TVS product families suitable for surge protection in digital I/O modules are SM15T ($P_{P,8/20µs}$ = 10kW) and SMC30J ($P_{P,8/20µs}$ = 36kW), where $P_{P,8/20µs}$ indicates the power limits for 8/20µs surge pulses.

Note: IEC, IEC 61000-4-5:2014, Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test.

For $V_{CC,max}$ = 28.8V, the devices SM15T33CA and SMC30J30CA may be considered.

Table 1. TVS clamping parameters

Type	$P_{P,8/20µs}$ [kW]	V_{BR} [V]	V_{CL}@I_{PP} [V]	I_{PP} [A]	R_D [mΩ]
SM15T33CA	10	31.4	59	169	140
SMC30J30CA	36	33.3	64.3	569	48

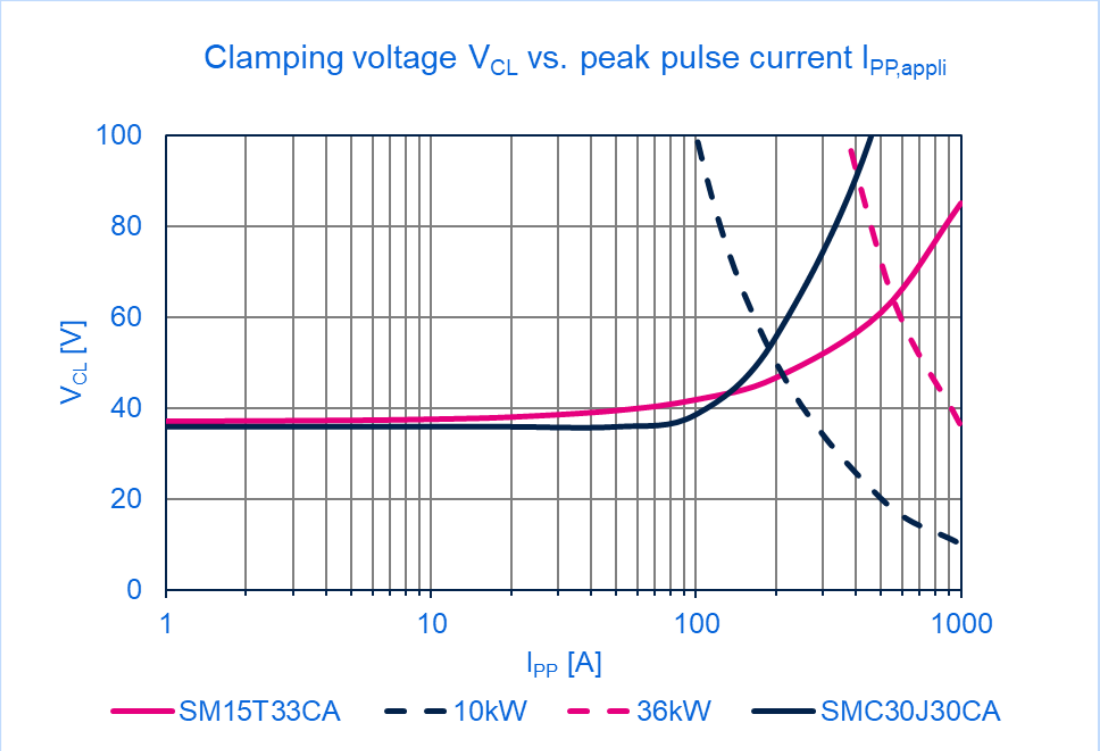
Using the R_D dynamic resistance parameter, the clamping voltage can be derived for other levels of 8/20µs surge current:

$$V_{CL,\,max} = V_{CL} - R_D \times \left(I_{PP} - I_{PP,\,appli}\right)$$

where $I_{PP,appli}$ is the surge current in the application (as specified in TVS datasheets).

The following figure shows the clamping voltage vs. TVS current for both devices, together with corresponding power boundaries.

Figure 5. Clamping voltage vs. peak pulse current



The maximum admissible surge amplitude can be derived from peak pulse current I_{PP} and the coupling method to be used:

$$V_{SURGE,\,max} = I_{PP} \times Z_{SURGE} + V_{CL} \cong I_{PP} \times R_{SURGE} + V_{CL}$$

If we consider common mode coupling impedance of a surge pulse generator R_{SURGE} = 12Ω (neglecting the coupling capacitance C_{SURGE} = 9µF), then the limit surge voltage can be determined as follows:

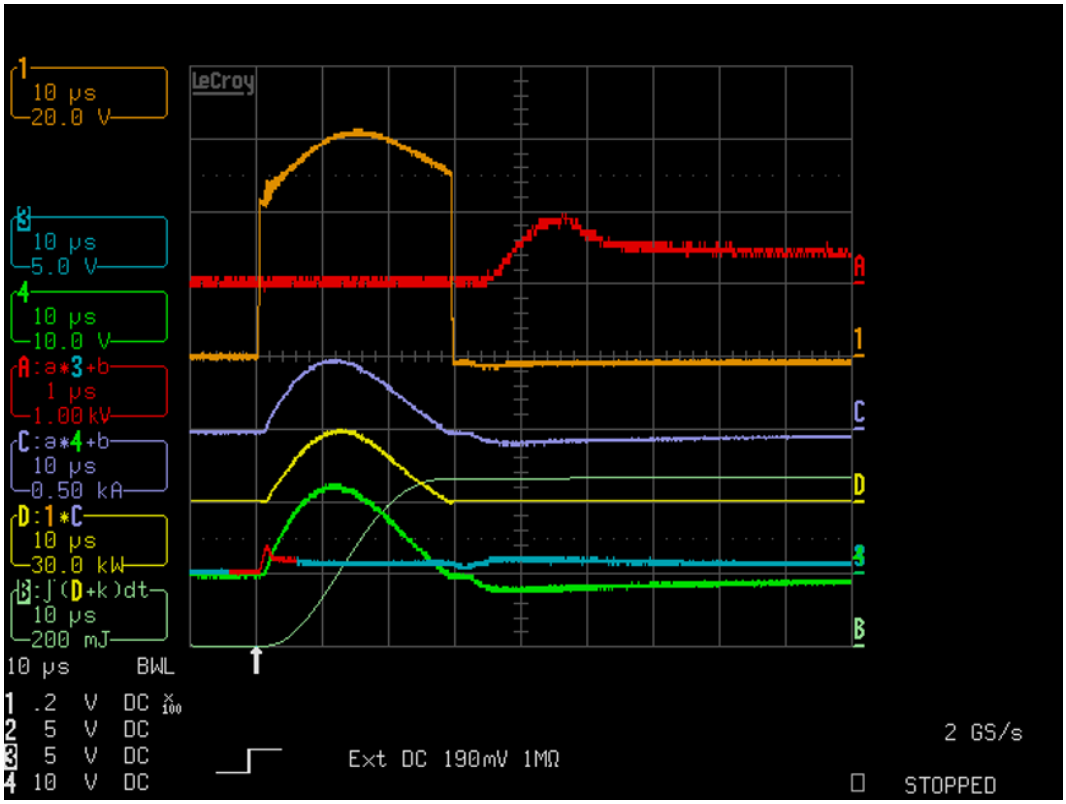
$$\text{SMC15T33CA} \rightarrow V_{SURGE,\,max} \cong 169 \times 12 + 59 = 2087V$$

$$\text{SMC30J30CA} \rightarrow V_{SURGE,\,max} \cong 569 \times 12 + 64.3 = 6892.3V$$

The SMC30J30CA provides robust protection with good clamping characteristics thanks to its low dynamic resistance.

The figure below shows the scope readout of the clamping behavior of the SMC30J30CA when tested for a 1 kV surge.

Figure 6. SMC30J30CA 1 kV surge clamping



The waveforms show that voltage over the TVS during the surge event is clamped at approximately $V_{TVS,CL}$ = 60 V and peak power dissipation is $P_{TVS,P}$ = 30kW. The clamping behavior of the SMC30J30CA is in line with above parameters and the TVS can therefore withstand 1 kV surges.

RELATED LINKS

For more information on the 1500 W TVS, view datasheet DS0683

For more information on the 3000 W TVS, view datasheet DS8598

6.6 EMC immunity on page 27

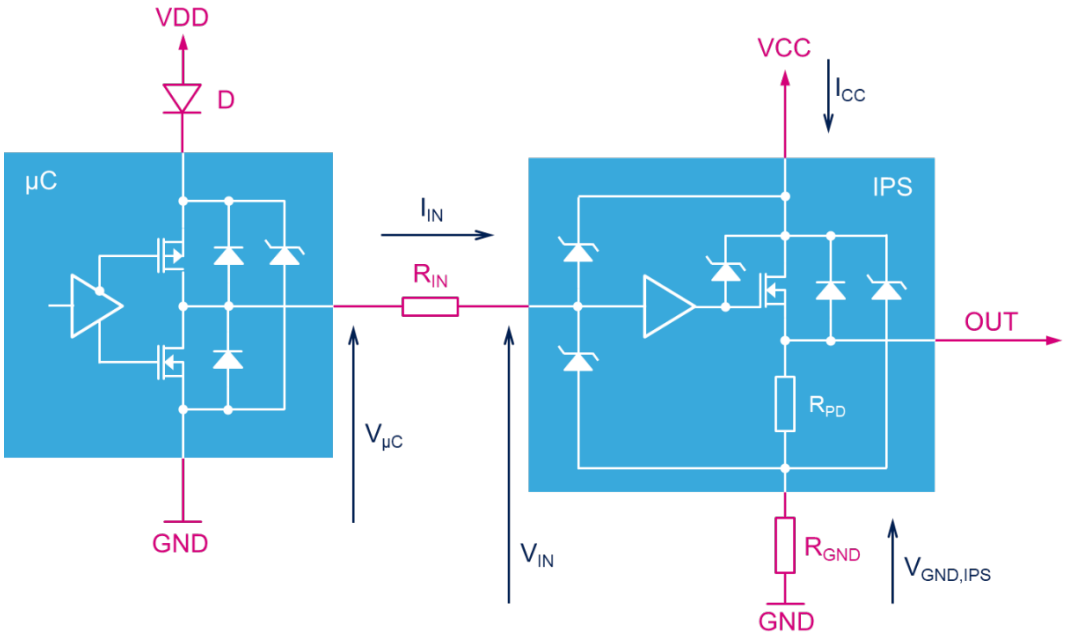
3 Reverse polarity protection

A Digital Output IC (Intelligent Power Switch, IPS) is driven by a digital device (microcontroller or an ASIC) which can be either galvanically coupled or there can be a galvanic isolation (optocoupler, digital isolator) in between.

3.1 Resistor in ground path

An example of basic protection scheme is shown below with a simplified internal structure of the integrated circuits.

Figure 7. Digital Output IC connection



The reverse polarity protection in the above figure is implemented with a diode D protecting the reverse current in the V_{DD} path and a resistor R_{GND} limiting the reverse current in the power path of the IPS.

We will use an STM32 ARM Cortex-M3 microcontroller and the IPS160H intelligent power switch for the following calculations, with reference values taken from the relevant IC datasheets.

Consider the microcontroller supply voltage V_{DD} = 3.3V and output voltage in logic H state $V_{\mu C,H} = V_{DD}$.

The lowest possible R_{GND} resistance is used to minimize the GND voltage drop $V_{GND,IPS}$:

$$R_{GND} \geq \left(\left|-V_{CC,\max}\right| - V_F\right) \div I_{CC,\text{reverse},\max} = (28.8 - 0.3) \div 0.250 = 114\Omega \cong 120\Omega$$

For R_{GND} = 120Ω, the ground shift $V_{GND,IPS}$ may rise up to:

$$V_{GND,IPS,\max} = R_{GND} \times I_{S,\max} = 120 \times 2.1 = 252\text{mV}$$

3.2 Resistor between Digital Output MCU and IPS

It is good practice to decouple the microcontroller and IPS ICs using series resistors to limit parasitic currents in case of faults and to limit EMC disturbance signals from the Process side affecting the microcontroller.

The value of the resistor must ensure proper operation in the full operating range and prevent damage in case of fault events such as reverse polarity.

Under normal operating conditions, we calculate the resistance as:

$$V_{IN,H} = V_{\mu C,H} - R_{IN} \times I_{IN} - V_{GND,IPS,\max} \geq V_{IN,H,\min} = 2.2\text{V}$$

$$R_{IN} \times I_{IN} \leq V_{\mu C,H} - V_{GND,IPS,\max} - V_{IN,H,\min}$$

$$R_{IN} \times I_{IN} \leq 3.3 - 0.252 - 2.2 = 0.848\text{V}$$

$$R_{IN} \leq \frac{V_{RIN}}{I_{IN}} = \frac{0.848}{0.2mA} = 4.24k\Omega$$

For current limitation in case of reverse polarity:

$$R_{IN} \geq \frac{|-V_{CC,max}| - 2 \times V_F}{I_{IN,max}} = \frac{28.8 - 0.6}{10mA} = 2.82k\Omega$$

Therefore:

$$2.82k\Omega \leq R_{IN} \leq 4.24k\Omega$$

We use the highest resistance value is selected for maximum protection: $R_{IN} = 4.2k\Omega$

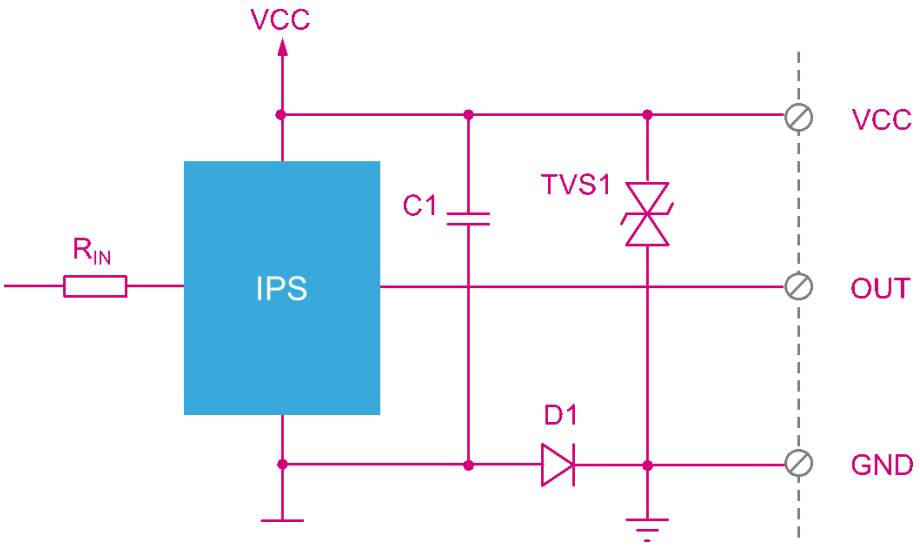
Note: The reverse polarity condition has the greatest impact on R_{IN} dimensioning, so other common fault scenarios where V_{CC} supply is disconnected or shorted to GND while V_{DD} is present do not need to be analyzed.

Several options are available to protect the application against damage under the reverse polarity condition.

3.3 Diode in ground path

A common solution for reverse polarity protection can be obtained when we replace the ground path resistor with a Schottky diode.

Figure 8. Protection diode in GND path



In this case the reverse current is limited to the leakage current of the diode D1, which is in the order of a few µA using the ST Schottky rectifier family STPS1H diodes. Capacitor C1 is used to block the supply voltage of the IPS and filter the noise. In real applications, it is usually represented by a 100nF ceramic capacitor in parallel with an electrolytic capacitor of a few µF.

Since the forward current in operating conditions is low (I_S ≈ 10mA), the diode is mainly selected on the basis of the required reverse voltage V_{RRM}. If we consider the above-mentioned application conditions then the reverse-biased diode can be exposed up to voltage $V_{CC,max}$ = 28.8V.

Higher level of overvoltage occurs when a negative surge pulse is applied to the power supply terminals during operation. Negative surge voltage is clamped by the TVS1 on the power supply connector and is in series with voltage on the blocking capacitor C1.

The reverse-biased diode is therefore exposed to voltage:

$$V_R = |-V_{CC} - V_{CL}| = |-28.8 - 64.3| = 93.1V$$

This requirement is fully satisfied by the STPS1H100 power Schottky rectifier.

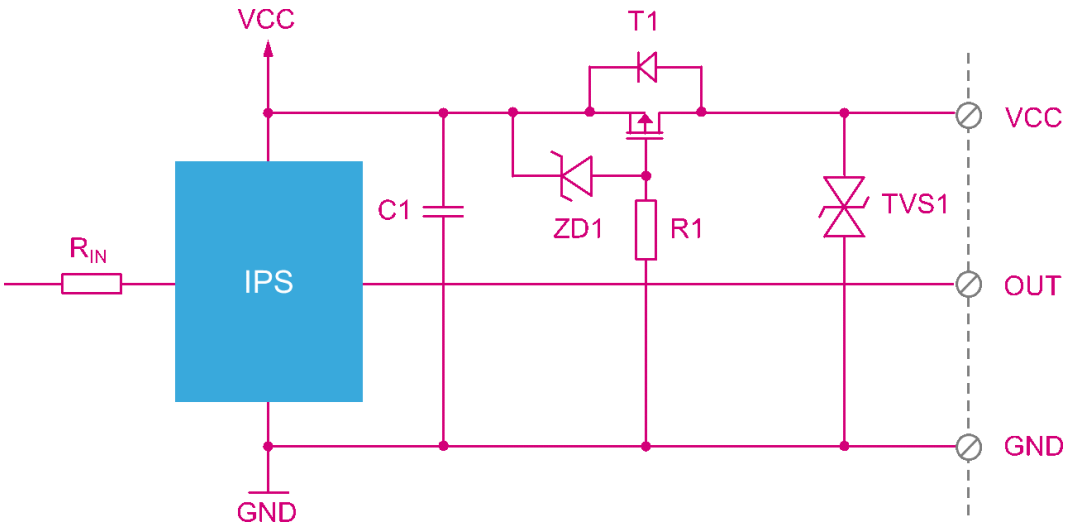
RELATED LINKS

For more information on the STPS1H100 Schottky rectifier, view datasheet DS1228

3.4 MOSFET switch in VCC path

Placing a MOSFET in the VCC path addresses the problem of the potential shift between the application and digital ground, which other reverse polarity protection strategies do not solve.

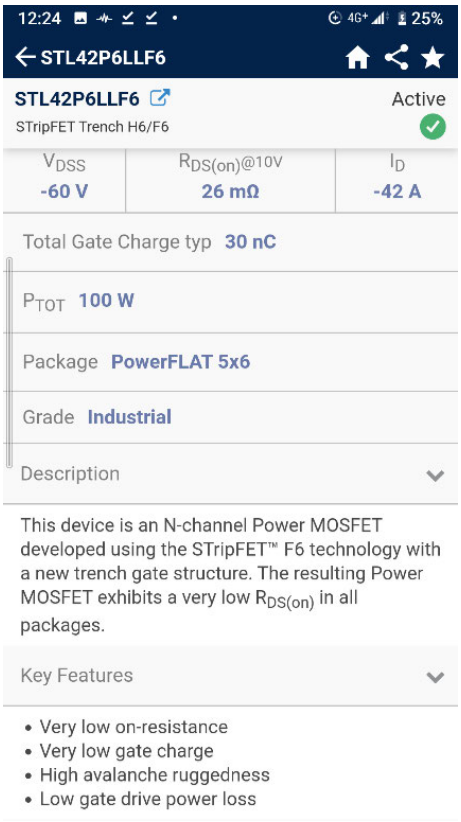
Figure 9. Reverse polarity protection with P-Channel MOSFET



The protection circuit consists of a P-channel MOSFET which is biased by Zener diode ZD1 and resistor R1. Unlike the GND path, which carries only low currents (IPS self-consumption), the V_{CC} path supplies current to all loads connected to its channels. Therefore, the total current I_{CC} can reach up to several Amps and the $R_{DS(\ on)}$ is the key parameter in the selection of the MOSFET switch.

We used the STPOWER MOSFET Finder app to quickly identify an appropriate P-channel Power MOSFET, STL42P6LLF6, developed using the STripFET F6 technology. This small form-factor device can withstand voltage up to 60 V and $R_{DS(\ on)}$ = 26mΩ.

Figure 10. STPOWER MOSFET Finder



Diode ZD1 is rated to 10 V in order to ensure optimal MOSFET behavior. If we set the diode current I_{ZD} = 0.4 mA, then the value of the resistor R1 = 36 kΩ.

RELATED LINKS

For more information on the STL42P6LLF6 Power MOSFET, view datasheet DS10014

4 Digital output section

As the Digital Output section drives various electric loads such as actuators in an automation system, it must ensure reliable operation in harsh environments.

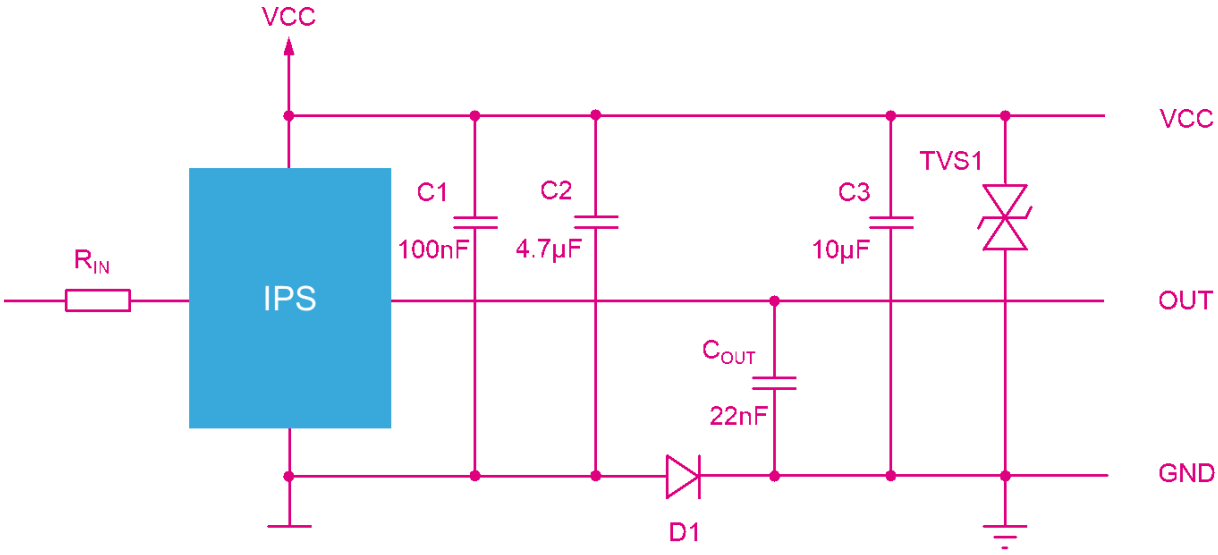
The STMicroelectronics portfolio of high-side driving solutions called Intelligent Power Switches (IPS) ranges in several parameters, including one to eight integrated channels, per-channel current ratings, serial or parallel digital side interfaces, and special features such as integrated galvanic isolation.

The following fundamental characteristics are common to all ST IPS products:

- High level of robustness including the full set of protections
  - Current limitation and short-circuit protection
  - Thermal shutdown protection
- Fast turn-off of inductive loads (fast demagnetization)
- ESD, EFT and Surge immunity on the process side pins
- Undervoltage lockout and loss of ground protection
- Diagnostics

The following figure shows a digital output section application circuit.

Figure 11. IPS application schematic



Besides the protection components for overvoltage and reverse polarity protection, it is very important to block the power supply voltage of an IPS and to filter its outputs properly in order to ensure stable operation under various application conditions.

A filtering capacitor C1 = 100 nF in combination with capacitor C2 = 4.7 µF should be placed as close as possible to the IPS to provide a bypass path for noise and ensure stable power supply for the IC.

The module power supply connector voltage is blocked by an additional capacitor C3 with higher capacitance (10 µF or 22 µF), which helps balance load current transients.

Each output channel should be filtered by an output capacitor C_{OUT} around 22 nF to provide the primary application protection against ESD, EFT and Surge overstress. Ceramic and low ESR capacitors should be used, with appropriate 50 V or 100 V rated voltage according to the application requirements.

Note: Applicable standards:

IEC, IEC 61000-4-2:2008, Electromagnetic compatibility (EMC): Part 4-2 - Testing and measurement techniques - Electrostatic discharge immunity test

IEC, IEC 61000-4-4:2012, Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test.

IEC, IEC 61000-4-5:2014, Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test.

5 IPS160H and IPS161H intelligent power switches

Figure 12. **IPS160H in PSSO12 package**

5.1 IPS16xH characteristics

This single-channel high-side driver is designed for Functional Safety and high-ruggedness applications like maritime and railway transportation.

Key parameters:

- V_{CC} range from 8 V to 60 V
- Output current:
  - IPS160H - 2.5 A
  - IPS161H - 0.7 A
- $R_{DS(\ on)}$ = 60 mΩ
- Open-load detection
- Programmable cut-off delay
- PSSO12 package

The extended voltage range up to 60 V helps module designers build Functional Safety applications and systems with strong EMC disturbance ruggedness, and reduce time-to-market and development costs.

The IC also features open load detection and cut-off limitation to significantly reduce power consumption in overload conditions.

RELATED LINKS

For more information on the IPS160H IPS, view datasheet DS10907

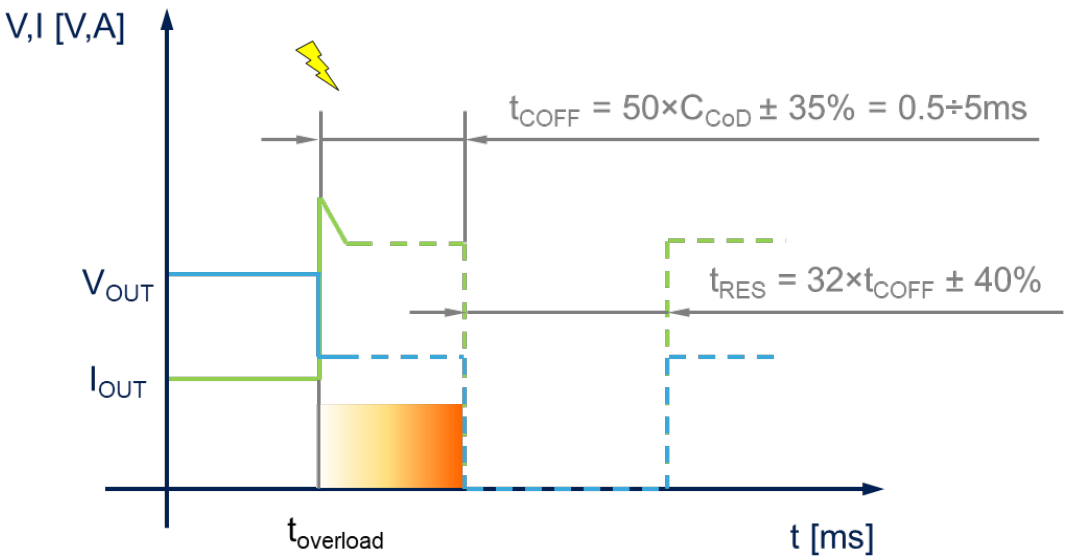
For more information on the IPS161H IPS, view datasheet DS11698

5.2 Cut-off limitation

When the IPS16xH Overload Mode is triggered by an event such as load degradation or a short-circuit failure, the output current is actively limited by the integrated power switch operating in linear mode. As a result, the IC power dissipation rapidly increases in proportion to the power supply voltage V_{CC}.

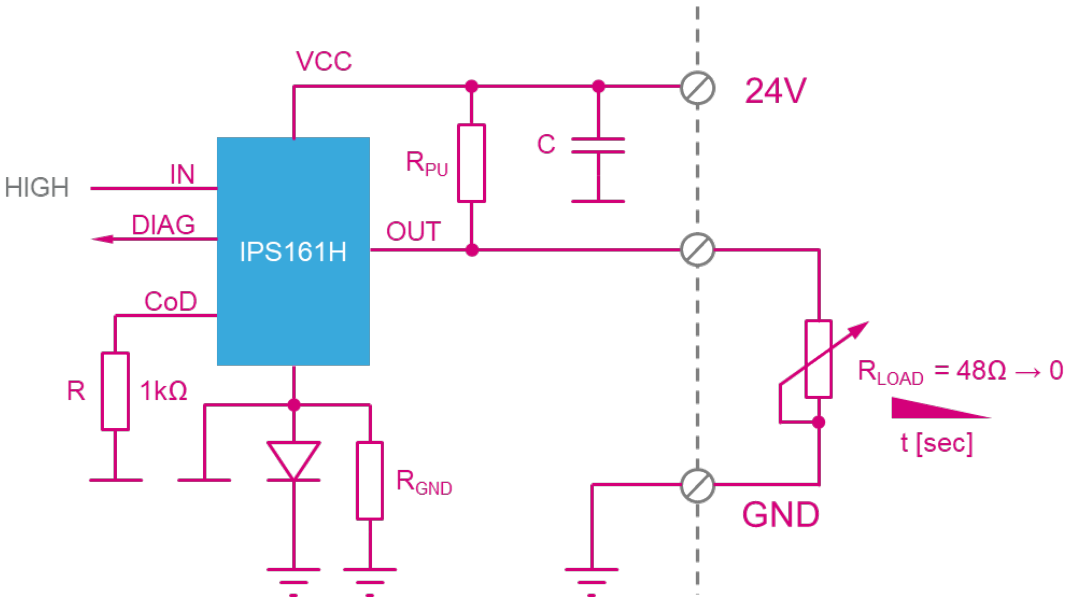
To keep the PCB and system housing temperature inside safe limits, the programmable cut-off limitation feature can be implemented, which helps reduce power dissipation inside the module by 97%. This is achieved by automatic turn-off of the switch after a certain current limitation interval (0.5 ms ≤ t_{COFF} ≤ 5ms), which is set by an external capacitor connected to the CoD pin of the IC.

Figure 13. **Cut-off limitation**



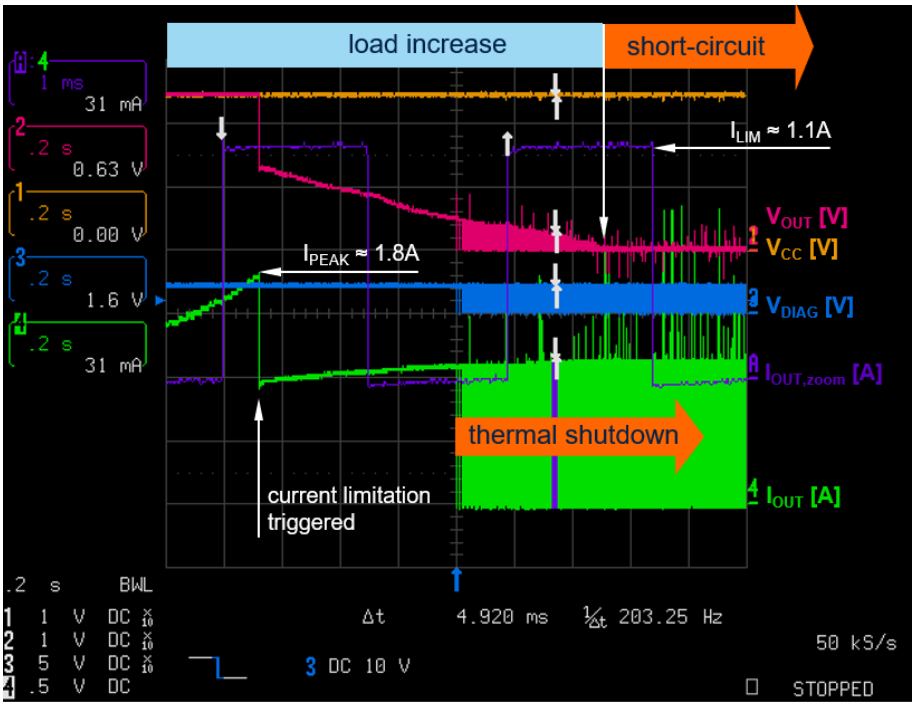
The cut-off limitation feature can be deactivated when the CoD pin is connected to ground through a 1 kΩ resistor, in which case the IPS is protected against overload and short-circuit conditions by current limitation and thermal shutdown mechanisms, as illustrated in the application schematic below.

Figure 14. **Overcurrent operation, cut-off disabled**



This scenario was measured using the STEVAL-IFP034V1 evaluation board. Its output was loaded with a 48 Ω potentiometer resistance progressively decaying to zero. The transition from nominal load to short-circuit was captured on a scope as shown in the following figure.

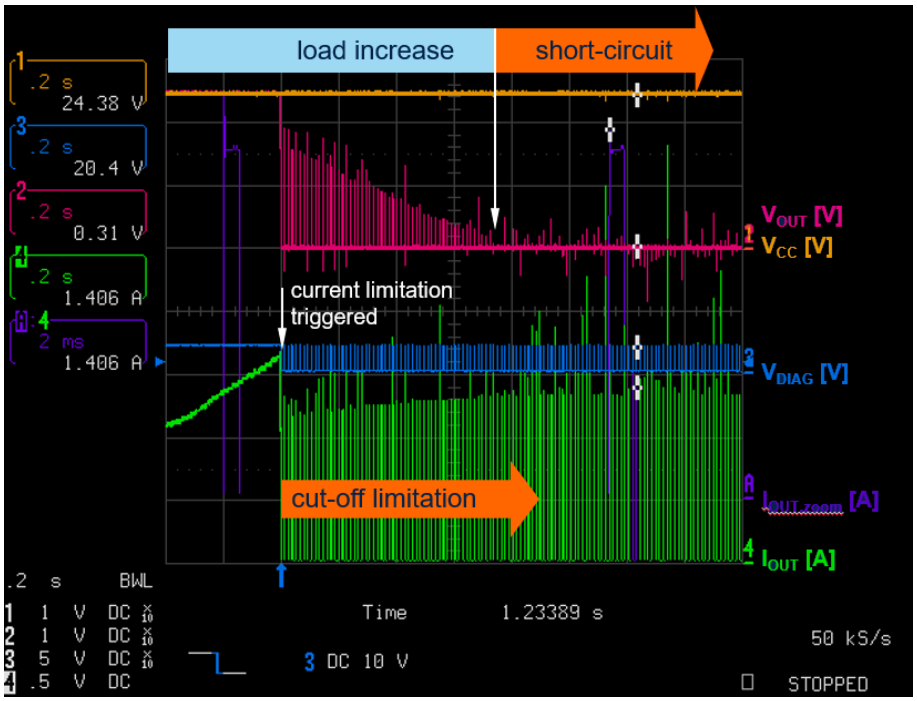
Figure 15. **Short-circuit transition waveforms (cut-off disabled)**



The green output current waveform shows that when the current limitation is triggered, the output current is limited to a constant I_{LIM} = 1.1A. Power dissipation of the IPS rises significantly as a result of increased voltage drop V_{DS} produced on an integrated power MOSFET operating in linear mode. This eventually results in eventual thermal shutdown when the temperature of the power switch reaches the junction temperature shutdown threshold $T_{JSD,typ}$ = 170°C, after which the power switch is periodically commutated in order to limit the junction temperature.

When cut-off limitation is activated by connecting a 10 nF capacitor to the CoD pin, the overload management behavior changes as shown in the following figure.

Figure 16. **Short-circuit transition waveforms, cut-off enabled**



The output current commutations are much less frequent compared to the previous case. The cut-off timing frequency is defined by the capacitor value, and for 0 nF, the delay duration (ON phase) $t_{coff} \approx 500$ µs and the restart delay time $t_{res} \approx 13$ ms, as shown by the purple waveform.

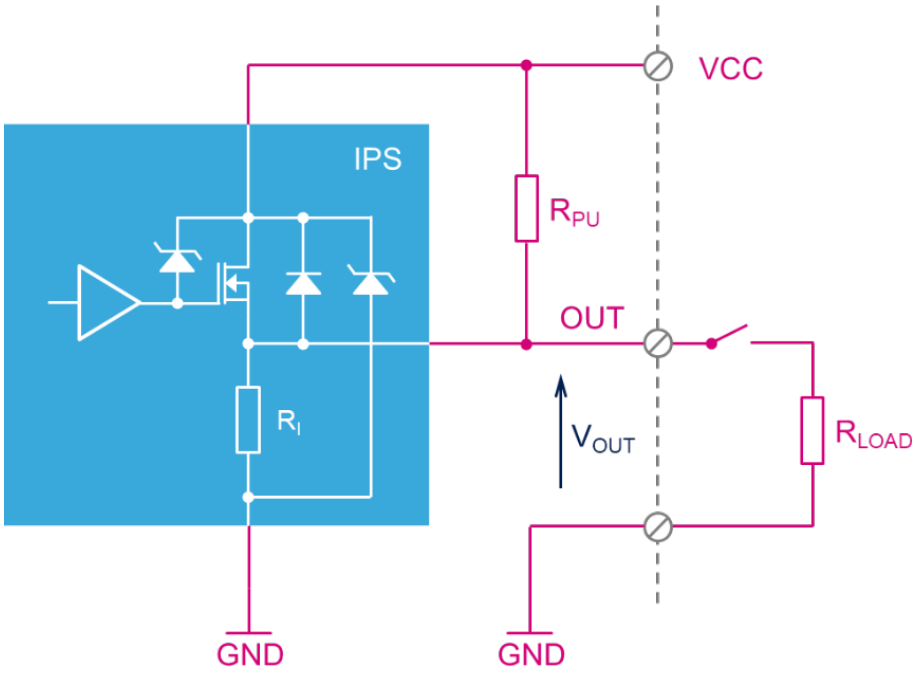
The cut-off limitation helps minimize power dissipation in overload conditions and therefore prevents excessive heat in a digital output module if an actuator in the system fails.

5.3 Open load detection

The IPS16xH open load detection feature continuously monitors the system for actuation failures such as cut wires and burnt out lamps on the factory floor. This allows load failures to be localized quickly to minimize production down-time.

The IC monitors load connection when its channel is in the OFF-state by means of an external pull-up resistor R_{PU} (e.g. 68 kΩ) connected to the output, as shown in the following figure.

Figure 17. **Open load detection circuit**



Under normal conditions with a properly connected load, the output voltage is pulled-down to GND through a low-ohmic resistance of the connected actuator (R_{LOAD}). In this case, the output voltage is given by the following formula:

$$V_{OUT} = V_{CC} \times \frac{R_{LOAD} \| R_I}{R_{PU} + (R_{LOAD} \| R_I)}$$

The R_I output impedance of the IC is connected in parallel to R_{LOAD} and its value is typically between 130 kΩ and 360 kΩ. The purpose of R_I is to pull down the output voltage to the OFF-state when there is no load connected. As the resistance of the connected load is much lower than both R_I and $R_{PU,}$ the OFF-state output voltage in normal conditions is close to 0 V.

When a load is disconnected, perhaps due to a failure, the resistance ratio in the circuit instantly changes and the output voltage is now pulled-up as R_I comes into effect:

$$V_{OUT} = V_{CC} \times \frac{R_I}{R_{PU} + R_I}$$

The output voltage is monitored by the IPS16xH and a fault is triggered when it exceeds the open load detection threshold $V_{OLoff,max}$ = 4V in OFF-state.

Open load detection can be used to quickly localize and repair failures in the wiring installation or failed lamps and actuators in the production line.

RELATED LINKS

To calculate the external resistor for the IPS160H IPS, view datasheet DS10907

To calculate the external resistor for the IPS161H IPS, view datasheet DS11698

5.3.1 Open load detection blanking

In many applications, the load impedance has a certain capacitive component that might be introduced by the capacitance of wiring to the load.

When such loads are switched OFF, the output voltage decreases until the load capacitance is discharged. The duration of this voltage transient depends on the pull-down impedance. In order to avoid spurious open load diagnostic triggering, the IPS16xH integrates a blanking time t_{BKT} = 200 µs to mask detection immediately after turn-OFF.

In high capacitance loads, the t_{BKT} might be insufficient to filter open-load flickering, so open load filtering should be implemented in the controller software.

5.4 EMC immunity

In factory floor environments, the high-power electrical systems and machines such as switched-mode power supplies, turbines, robotics and drives produce a lot of electrical noise in the wiring structure and through electromagnetic fields. Therefore, strong immunity and robustness is the key requirement for semiconductor devices in automation systems.

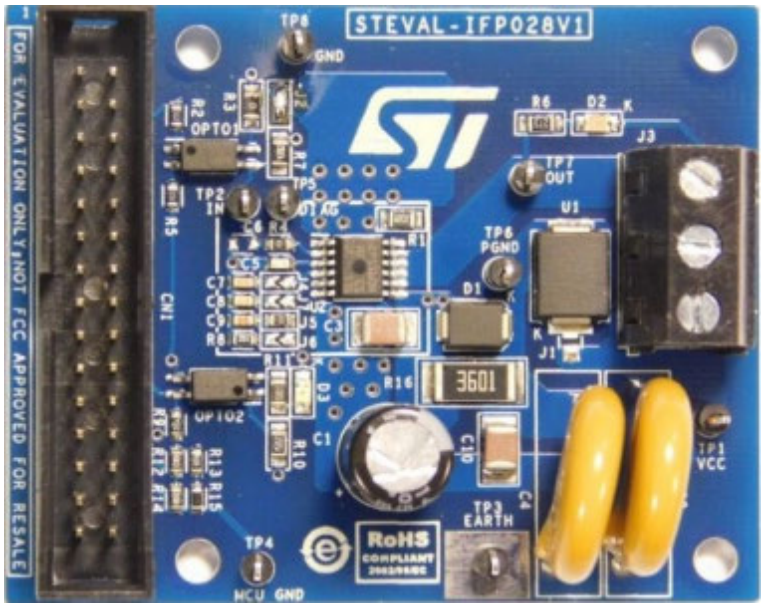
Electronic systems used in factory automation must comply with the electromagnetic compatibility (EMC) requirements for industrial applications in the IEC 61000-4 international standard.

The electrical immunity of digital I/O systems is assessed in terms of the following disturbance signal types:

1. Electrostatic discharge (IEC 61000-4-2)
2. Electrical Fast Transient (IEC 61000-4-4)
3. High-energy surge (IEC 61000-4-5)
4. Immunity to conducted disturbances (IEC 61000-4-6)

To test immunity of IPS16xH, we used the STEVAL-IFP028V1 and STEVAL-IFP034V1 evaluation boards.

Figure 18. IPS160H evaluation board

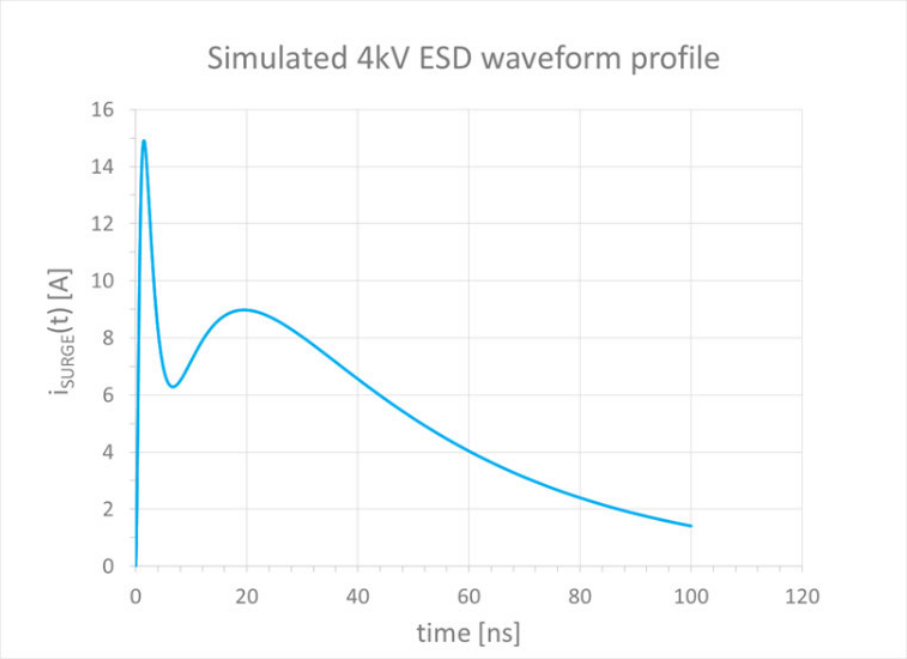


The application and immunity tests performed in ST labs to verify reliability and robustness of the IPS160H and IPS161H single-channel drivers demonstrate compliance with all industrial EMC immunity requirements and can therefore operate reliably in harsh industrial environments.

5.4.1 Electrostatic discharge (IEC 61000-4-2)

Electrostatic discharge (ESD) occurs when two objects with different electrical charge come into contact, such as when a human operator touches terminals of a module during maintenance. ESD is characterized by a very fast dynamics with a pulse rising time of 0.8 ns.

Figure 19. **ESD pulse waveform**



The results of ESD tests performed on the IPS160H are listed in the following table.

Table 2. **IPS160H/ IPS161H ESD immunity (IEC 61000-4-2)**

test level		coupling		
		VCC	GND	OUT
Contact				
1	2kV	B/B	B/B	B/B
2	4kV	B/B	B/B	B/B
3	6kV	B/B	B/B	B/B
4	8kV	B/B	B/B	B/B
Air				
1	2kV	B/B	B/B	B/B
2	4kV	B/B	B/B	B/B
3	8kV	B/B	B/B	B/B
4	15kV	B/B	B/B	B/B

The evaluation boards were tested in the EMC laboratory using a Teseq NSG 435 ESD simulator under the following application conditions:

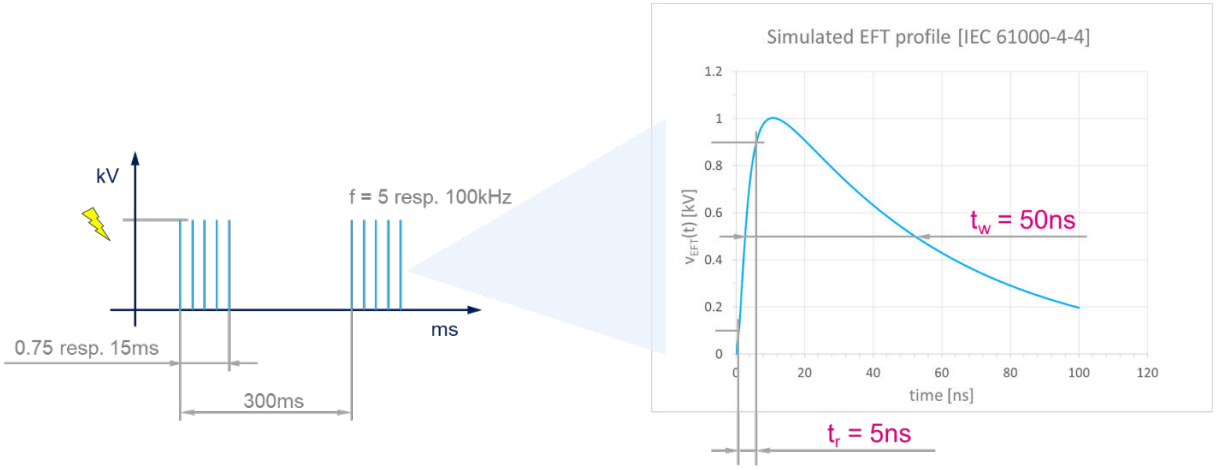
- Normal ambient temperature T_{AMB} = 24°C
- Power supply voltage VCC = 25.5V provided by two 12 V acid-lead cells in series
- Output in OFF-state with test startup procedure
- ESD applied to VCC, GND and Output terminals
- Each test case consists of 10 pulses applied to the tested point in each polarity

Test results show that IPS160H and IPS161H passed all the test levels up to 8 kV for contact discharge and 15 kV for air discharge, in line with requirements for industrial applications.

5.4.2 Electrical fast transient (IEC 61000-4-4)

Electrical Fast Transients (EFT) are repetitive signals that occur in wiring as a result of switched mode power supply operation or electric motor commutation. These signals are bursts of overvoltage pulses carrying relatively low amounts of energy.

Figure 20. EFT pulse



EFT immunity was verified using the EMTEST Compact NX5 test generator under the following application conditions:

- Normal ambient temperature T_{AMB} = 24°C
- Power supply voltage VCC = 25.5V
- Disturbance applied to power supply wires and output using capacitive coupling clamp (equivalent capacitance 150 pF)
- Each test case consists of continuous disturbance application for 1 min in each polarity

Table 3. IPS160H/ IPS161H EFT immunity (IEC 61000-4-4)

test level		disturbance signal	
		5kHz	100kHz
		15/300ms, 60s	0.75/300ms, 60s
1	0.5kV	A/A	A/A
2	1kV	A/A	A/A
3	2kV	A/A	A/A
4	4kV	A/A	A/A

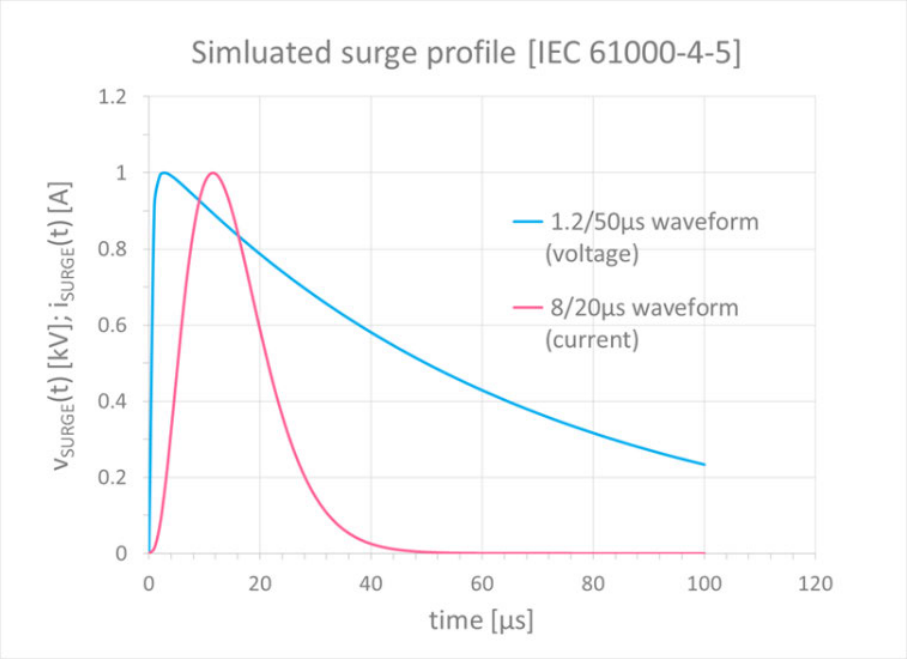
The test results in the above table demonstrate that the IC can tolerate up to 4 kV EFT overstress.

Note: The application was tested up to 5.5 kV and the IC continued operation without suffering any damage.

5.4.3 High-energy surge (IEC 61000-4-5)

A surge test introduces single pulse overstress with high energy to simulate disturbance from events such as lightning strikes and switching high inductances. The surge pulse in the IEC 61000-4-5 standard is defined by the shape of voltage curve when surge generator output is open (rising time 1.2 µs and 50 µs duration) and current waveform when the output is shorted (rise time 8 µs and 20 µs duration).

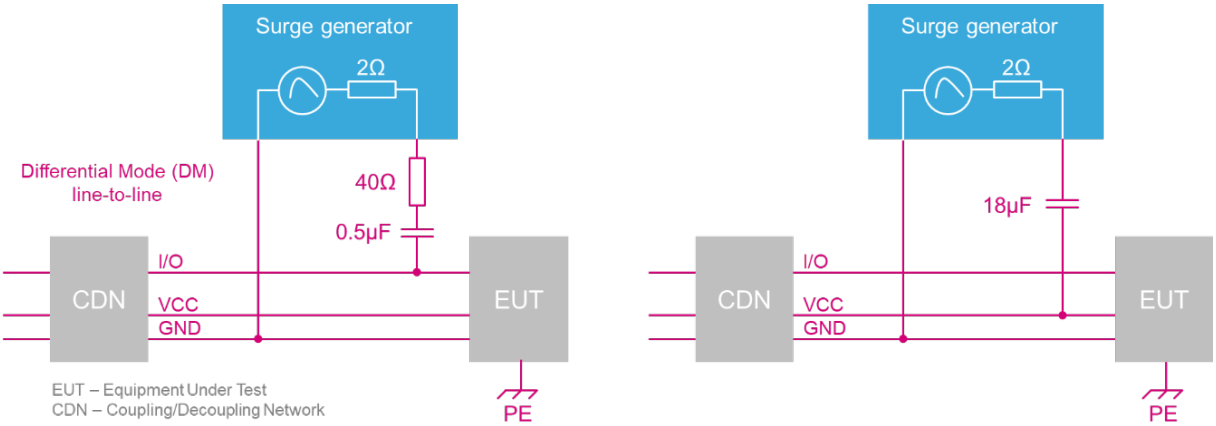
Figure 21. Surge pulse waveforms



Surge pulse tests are generally applied in Differential Mode (DM) and Common Mode (CM) to the process side I/O and power supply connectors of a digital I/O module. The two modes differ in the way the surge pulse overstress is coupled to the application.

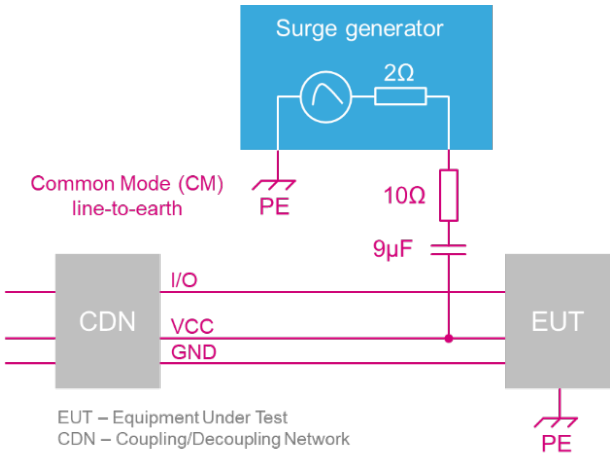
In Differential Mode surge pulse is referenced to the ground reference terminal and is applied either to digital I/O lines through 42 Ω/0.5 µF serial coupling impedance or to power supply terminals through 2 Ω/18 µF.

Figure 22. Surge pulse test setup - Differential Mode (DM)



In Common Mode, the test pulse is referenced to protective earth terminal (PE) and is coupled to power supply terminals through serial impedance of 12 Ω/9 µF.

Figure 23. **Surge pulse test setup - Common Mode (CM)**



The surge pulse immunity test results are provided in the following table.

Table 4. **IPS160H/161H Surge immunity (IEC 61000-4-5)**

Test level		Coupling			
		OUT-GND (DM)	L-PE (CM)	N-PE (CM)	L-N (DM)
		42Ω / 0.5µF	12Ω / 9µF	12Ω / 9µF	2Ω / 18µF
1	0.5kV	B/B	B/B	A/A	B/B
2	1kV	B/B	B/B	A/A	- / -
3	2kV	B/B	B/A	B/A	- / -

6 8-channel ISO8200AQ and ISO8200BQ galvanic isolated drivers

Figure 24. **ISO8200AQ in QFN 9x11mm package**

6.1 Key characteristics

ISO8200xQ is an octal high-side driver with integrated galvanic isolation, designed for applications requiring high integration.

Key parameters:

- 8-channel IPS
- Output current 0.7 A/channel
- 4 kV galvanic isolation
- Low RDS(on) = 110 mΩ
- SPI or parallel interface
- Short-circuit and thermal protection
- Small form factor

The ICs is housed in a very small form factor QFN package 9×11 mm and is available in the following product communication options:

- 20MHz SPI to communicate with a microcontroller (ISO8200AQ)
- Parallel digital interface (ISO8200BQ)

Both ICs are equivalent in terms of power-stage structure, including built-in short-circuit protection, current limitation and thermal shut-down. Each channel is rated for currents up to 0.7 A and it can drive any kind of resistive, capacitive or inductive load with opposite terminal connected to ground.

RELATED LINKS

For more information on the 8-ch ISO8200AQ galvanic isolated driver, view datasheet DS12812

For more information on the 8-ch ISO8200BQ galvanic isolated driver, view datasheet DS10781

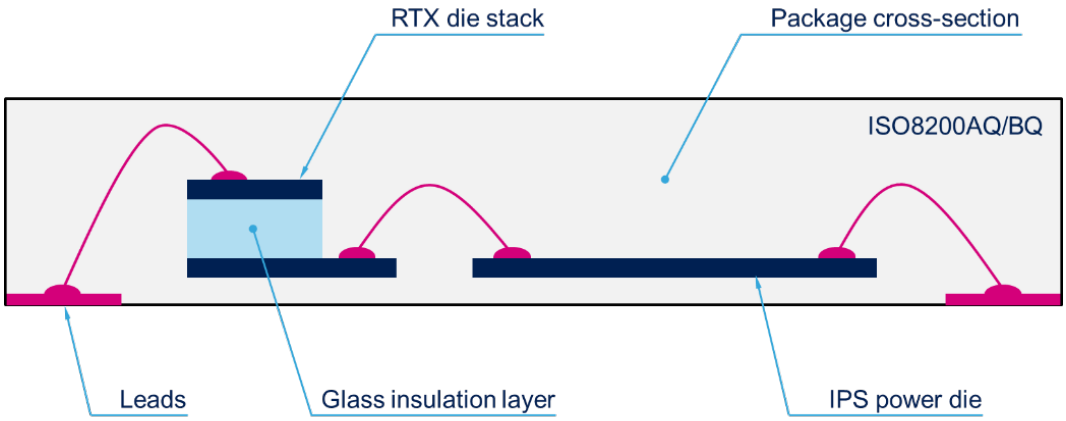
6.2 Galvanic isolation

Strong electrical disturbance may occur on factory floors with high-powered machinery. Ground loops and other parasitic effects caused by large wiring installations together with strong EMC disturbance may heavily disturb or even completely disrupt operation of sensitive digital components such as microprocessors and bus ASICs, which operate at low voltage and high speed.

Galvanic isolation is therefore essential for limiting disturbance in digital I/O modules which interface with production line sensors and actuators.

The ISO8200AQ and ISO8200BQ smart power switches integrate galvanic isolation in the IPS, which helps simplify the design, reduce PCB size and optimize costs since external isolation components such as optocouplers or digital isolators can be omitted.

Figure 25. **Simplified internal structure of an isolated IPS**



A glass isolation layer lies between the digital and the process side, which communicate using an RF modulated signal over an electro-magnetic antenna structure to ensure robust and reliable data transfer while minimizing EMI disturbance.

The insulation withstand voltage of the IC is 2.5kV$_{RMS}$.

The ISO8200xQ isolation technology is certified according to UL1577 and UL508 standards and is compliant to safety limits defined by VDE0884-11.

RELATED LINKS

For more information on the 8-ch ISO8200AQ galvanic isolated driver, view datasheet DS12812

For more information on the 8-ch ISO8200BQ galvanic isolated driver, view datasheet DS10781

6.3 Diagnostics

The ISO8200xQ provides an open-drain diagnostic output /FAULT that is activated when any output channel enters thermal shutdown due to overload (channel temperature above T_{JSD} = 170°C) or when a communication error occurs between the two isolated sides.

The ISO8200AQ can also identify which channel has overloaded thanks to the channel-specific overtemperature flag vectors transferred via SPI. Serial communication integrity is monitored, as well as the voltage level on the power supply, which is activated when power supply falls below $V_{CC(PGON),\ typ}$ = 17.5V. This feature allows to prevent undefined system behavior and data losses in case of a blackout by applying emergency and system shutdown procedures before the supply drops to undervoltage region.

RELATED LINKS

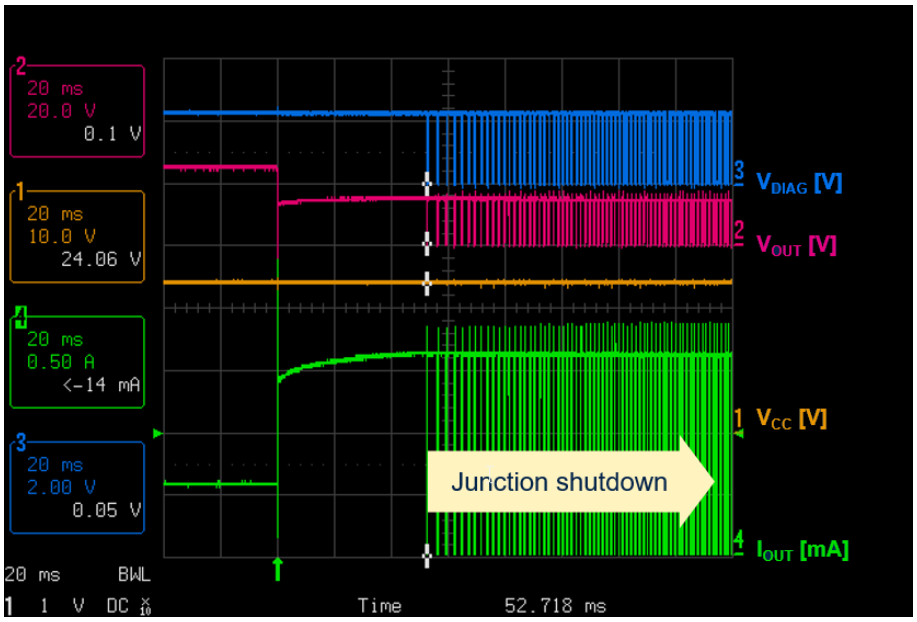
For more information on the 8-ch ISO8200AQ galvanic isolated driver, view datasheet DS12812

For more information on the 8-ch ISO8200BQ galvanic isolated driver, view datasheet DS10781

6.4 Thermal shutdown protection

The ISO8200xQ has a sophisticated thermal protection scheme ensuring full inter-channel independence in case of overload. To protect the IC against short-circuits, the ISO8200xQ integrates current limitation in which the power MOSFET of the overloaded channel is driven in linear mode to limit the output current below $I_{LIM,max}$ = 1.9 A.

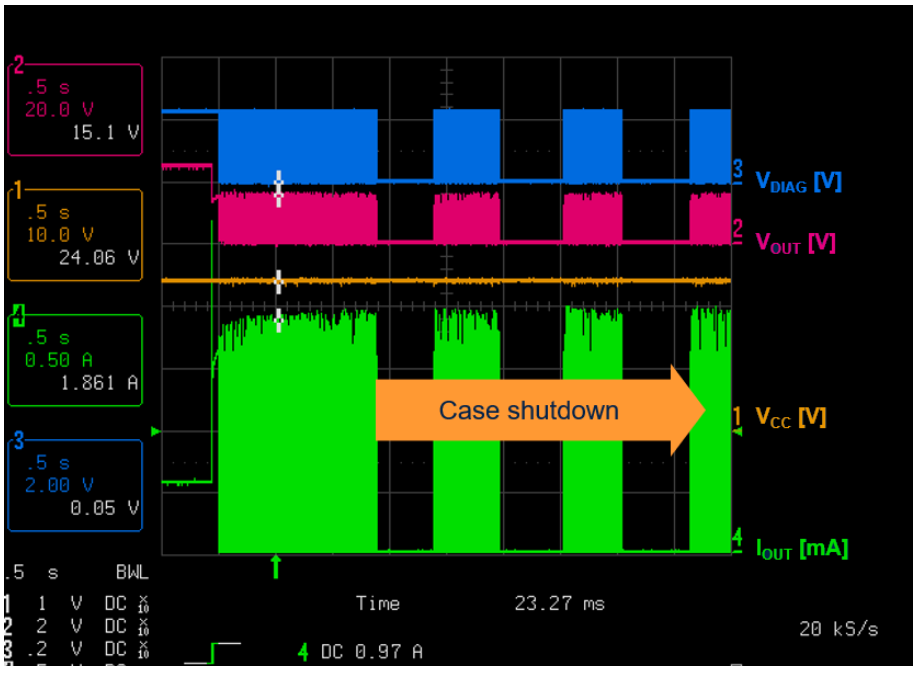
Figure 26. **ISO8200xQ current limitation and junction thermal shutdown**



As soon as the junction temperature reaches the junction threshold T_{JSD} = 170°C, the thermal shutdown protection starts to periodically switch-OFF an overloaded channel.

To protect the IC when overload conditions persist or appear on multiple channels simultaneously, an additional Case thermal shutdown is implemented. When the IC case reaches the T_{CSD} = 130°C threshold, all overloaded channels are switched-OFF until case temperature decreases (case thermal hysteresis is T_{CHYST} = 20°C), as shown in the following figure.

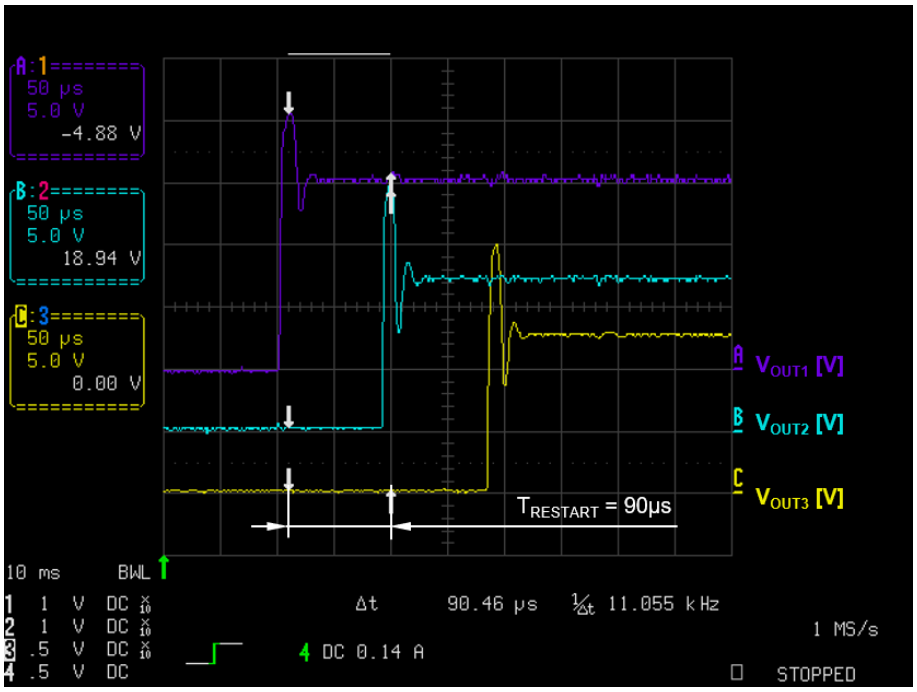
Figure 27. **ISO8200xQ Case thermal shutdown**



Note: Even when one or more channels are deactivated due to thermal shutdown, the unaffected channels will continue to be driven normally.

The recovery of the system from overload implements staggered channel activation as the simultaneous re-activation of up to eight channels with loads after thermal shutdown could produce a significant current transient in the V_{CC} path.

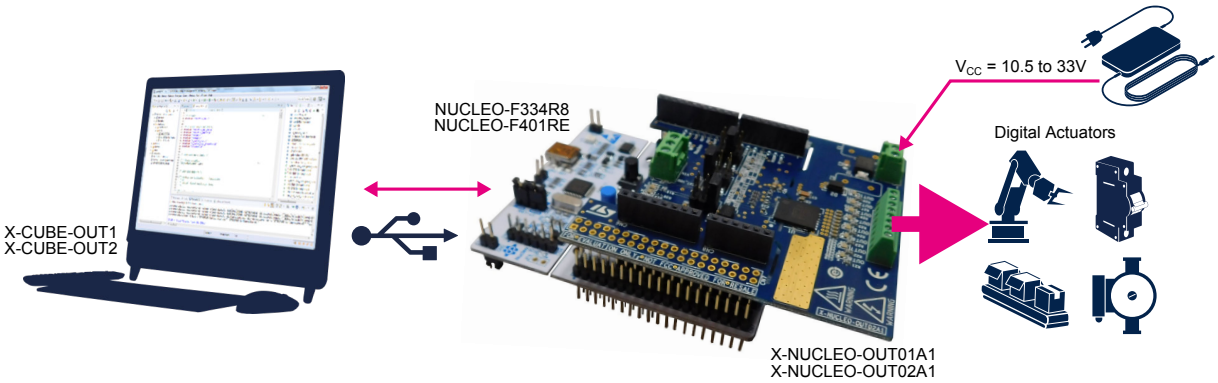
Figure 28. ISO8200xQ Case shutdown recovery



6.5 Evaluation tools

The ISO8200AQ and ISO8200BQ is accompanied by a complete evaluation toolset based on STM32 ODE, with STM32 NUCLEO development and expansion boards and X-CUBE firmware package supporting various development environments.

Figure 29. ISO8200xQ Evaluation ecosystem



The X-NUCLEO expansion boards can either be used with custom controller PCBs.

RELATED LINKS

Visit the ST website for complete documentation and the related STM32 firmware libraries

6.6 EMC immunity

The immunity of ISO8200xQ ICs was verified using relevant STM32 NUCLEO development and expansion boards. Below are the EMC immunity test results for the ISO8200AQ.

EMC tests were carried out in the ST EMC Laboratory with the following common test conditions and setup:

- Normal ambient temperature T_{AMB} = 24°C
- Process side power supply voltage VCC = 25.5V provided by two 12V acid-lead cells in series
- Digital side power supply VDD = 3.3V
- Test board: NUCLEO-F401RE development board + X-NUCLEO-OUT02A1 expansion board

6.6.1 Electrostatic discharge (IEC 61000-4-2)

The ESD immunity of the ISO8200AQ was verified using the Teseq NSG 435 ESD simulator under the following specific application conditions:

- Output state commutating (C0h ↔ F0h) at 1Hz
- ESD applied to VCC, GND and OUT2 in OFF-state

Each test case consists of 10 pulses applied to the tested point in each polarity.

Table 5. ISO8200AQ ESD immunity

Test level		Coupling		
		VCC	GND	OUT2
Contact				
1	2kV	A/A	A/A	A/A
2	4kV	A/A	A/A	A/A
3	6kV	A/A	B/B	B/A
4	8kV	B/A	B/A	B/B
-	9kV	B/A	B/B	B/B
Air				
1	2kV	A/A	A/A	A/A
2	4kV	A/A	A/A	A/A
3	8kV	A/A	B/A	B/A
4	15kV	A/A	A/A	A/A
-	16.5kV	A/A	A/A	A/A

The table shows that the IC can withstand overstress levels above the peak 8 kV/15 kV ESD values specified by the standard.

6.6.2 Electrical Fast Transient (IEC 61000-4-4)

EFT immunity was verified using the EMTEST Compact NX5 test generator under the following specific application conditions:

- Output state commutating (C0h ↔ F0h) at 1 Hz
- Disturbance applied to power supply wires and output using capacitive coupling clamp (equivalent capacitance 150 pF)
- Each test level verified both for 5 kHz and 100 kHz EFT
- Single polarity test duration 1 min

Table 6. **ISO8200AQ EFT immunity**

Test level		Disturbance signal	
		5kHz	100kHz
		15/300ms, 60s	0.75/300ms, 60s
1	0.5kV	A/A	A/A
2	1kV	A/A	A/A
3	2kV	A/A	A/A
4	4kV	A/A	A/A
-	5.5kV	A/A	A/A

Immunity to Electrical Fast Transients was verified up to 5.5 kV, demonstrating full ISO8200AQ compliance with the industrial requirement for digital output ICs.

6.6.3 High-energy surge (IEC 61000-4-5)

Surge immunity was verified using the EMTEST Compact NX5 test generator under the following specific application conditions:

- Output state commutating (C0h ↔ F0h) at 1 Hz
- Surges applied in differential mode (DM, surge referenced to application ground):
  - OUT2 in OFF-state; coupling impedance: 42 Ω + 0.5 µF
  - VCC terminal; coupling impedance: 2 Ω + 18 µF
- Surges applied in common mode (CM, referenced to protective earth):
  - VCC terminal; coupling impedance: 12 Ω + 9 µF
  - GND terminal; coupling impedance: 12 Ω + 9 µF

Table 7. **ISO820AQ Surge immunity**

test level		Coupling			
		OUT2 OFF (DM)	L-PE (CM)	N-PE (CM)	L-N (DM)
		42Ω / 0.5µF	12Ω / 9µF	12Ω / 9µF	2Ω / 18µF
1	0.5kV	A/A	A/A	A/A	A/A
2	1kV	A/A	A/A	A/A	- / -
3	2kV	A/A	A/A	A/A	- / -

The surge immunity of the ISO8200AQ was verified up to 2 kV on the outputs. Power supply terminals sustain surges up to 2 kV in Common Mode and 500 V in differential coupling. Immunity levels achieved are fully in line with industrial requirements.

7 Summary

It is important to understand the architectural characteristics of a digital output module and how its internal components are designed and dimensioned for robust and reliable operation.

STMicroelectronics has extensive experience in developing innovative industrial grade products for Smart Factories, including the IPS160H and IPS161H single-channel drivers and the small form factor ISO8200AQ and ISO8200BQ eight-channel IPS family of drivers with integrated galvanic isolation.

These recent devices offer full EMC immunity compliance with relevant standards, as well as monitoring, diagnostic and protection capabilities that can help improve reliability and reduce downtime in critical production systems.

Revision history

Table 8. **Document revision history**

Date	Version	Changes
03-Aug-2020	1	Initial release.

Contents

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