15V/18W isolated SSR Flyback with VIPER318LDTR

Introduction

The STEVAL-VP318L1F implements a 15 V/18 W power supply with a wide (90 to 265 V_{AC}) input voltage range, set in isolated Flyback topology with secondary side regulation (SSR).

The power supply has the following characteristics:

- 4-point average active mode efficiency at full load: >85% (compliant with European CoC ver. 5)
- 4-point average active mode efficiency at 10% full load: >76% (compliant with European CoC ver. 5)
- input power consumption in no load condition: < 50 mW (at 230 V_{AC})
- input power consumption at P_{OUT} = 250mW: < 400 mW (at 230 V_{AC})
- Compliant with IEC55022 Class B conducted EMI, even with reduced EMI filter
- Independently settable input undervoltage/overvoltage protections
- RoHS compliant

The evaluation board is based on the VIPER318LDTR off-line high voltage converter with the following features:

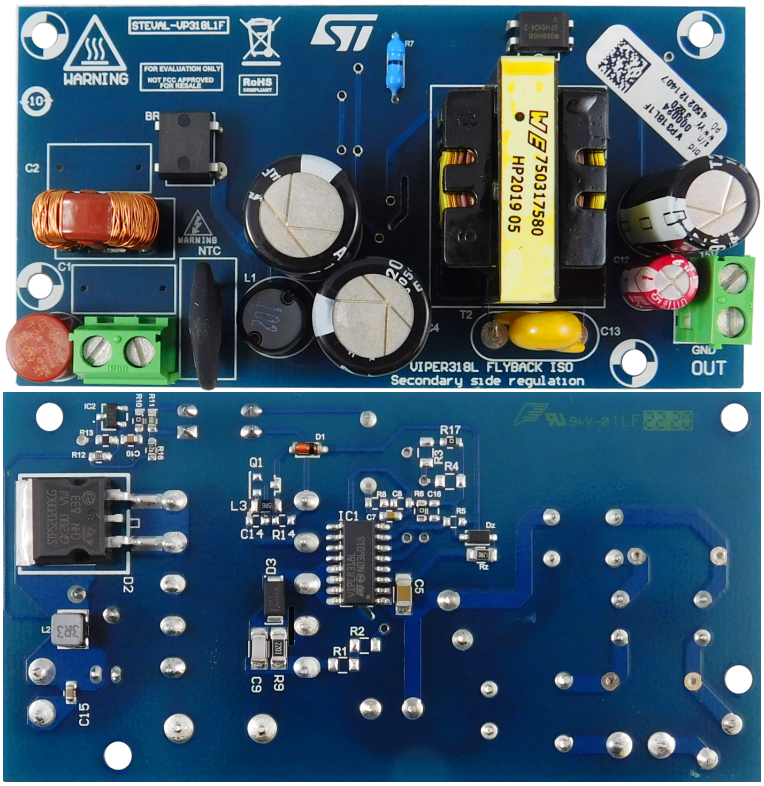
- 800V avalanche rugged Power MOSFET
- Embedded HV start-up
- On-board trans-conductance error amplifier internally referenced to 1.2 V ±2%
- Current mode PWM controller with drain current limit protection for easy compensation
- Pulse frequency modulation (PFM) and ultra-low stand-by consumption of the internal circuitry under light load condition
- 60 kHz fixed switching frequency with jittering

Enhanced system reliability through built-in soft start function and the following set of protections:

- pulse skip mode to avoid flux-runaway
- delayed overload protection (OLP)
- input overvoltage protection
- input undervoltage protection
- thermal shutdown protection

Excluding pulse-skip mode, all protections are auto restart mode.

Figure 1. **STEVAL-VP318L1F evaluation board top and bottom**



1 Circuit description

The PCB is designed to accommodate primary side regulation (PSR) or secondary side regulation (SSR), which is determined by specific BOM component choices. The STEVAL-VP318L1F specifically implements SSR operation.

FB is connected to GND pin (which disables the internal error amplifier), the output voltage value is set by the TS3431 placed on the secondary side through the R12 and R13 voltage divider. An opto-coupler carries the TS3431 error signal to the primary side, where it adjusts the COMP pin voltage level (and thus the DRAIN peak current) to the value required by the control loop for output voltage regulation.

Resistors R1, R2, R3 and R4 form a voltage divider from the rectified input mains to implement input undervoltage and overvoltage protection. By default, these resistors are disconnected and a 0 Ω R17 is mounted to minimize board consumption in no-load and light-load conditions. In this way, the OVP pin is connected to GND and UVP pin is left floating to disable their functions.

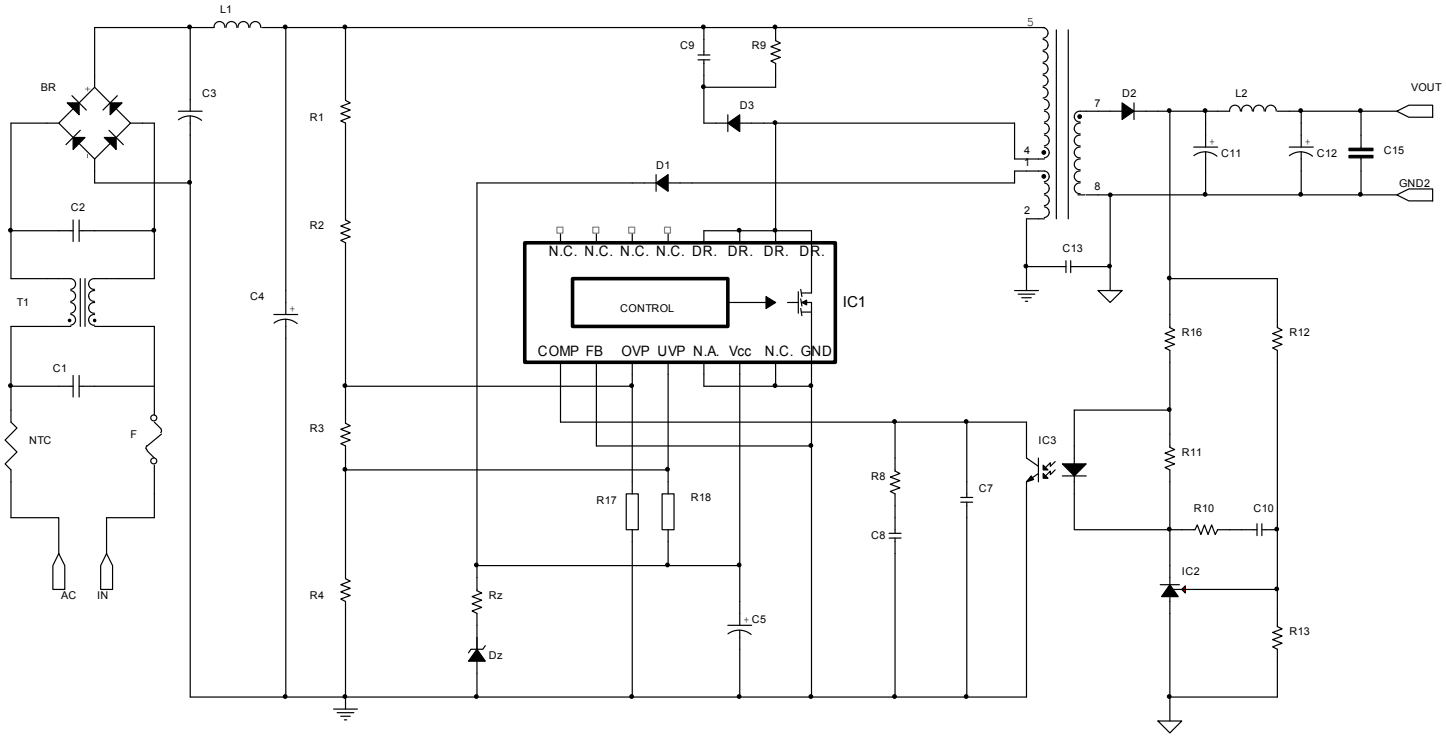
1.1 Specifications

Table 1. Electrical specs

Parameter	Symbol	Value
Input voltage range	V_{IN}	90 - 265 V_{AC}
Output voltage	V_{OUT}	15 V
Max. output current	I_{OUT}	1.2 A
Max. output power	P_{OUT}	18 W
Precision of output regulation	ΔV_{OUT}	±5%
High frequency output voltage ripple	ΔV_{OUT}	50 mV
Max. ambient operating temperature	T_{AMB}	65 °C
Switching frequency	F_{OSC}	60 kHz

1.2 Schematic diagram

Figure 2. **STEVAL-VP318L1F board schematic**



1.3 Bill of materials

Table 2. **STEVAL-VP318L1F bill of materials**

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	1	BR	DF06M DF-M 600 V 1 A	Diode bridge	Vishay	DF06M-E3/45
2	1	D1	1N4148 SOD-123 100 V 0.3 A	Small signal diode	Diodes Zetex	1N4148W-7-F
3	1	D2	STPS20200CG, D^2PAK, 200 V 20 A	Dual power Schottky diode	ST	STPS20200CG-TR
4	1	D3	MRA4007T3G DO-214AC 1000V 1A	General purpose diode	ON Semiconductor	MRA4007T3G
5	1	Dz	BZT52C22 SOD-123 22V 0.5W	Zener diode	Diodes Zetex	BZT52C22-7-F
6	0	C1	Not connected, through hole	X2 capacitor		
7	0	C2	Not connected, through hole	X2 capacitor		
8	1	C3	22 µF, 450 V, through hole	Electrolytic capacitor - BXF series	Rubycon	450BXF22M12.5X20
9	1	C4	22 µF, 450 V, through hole	Electrolytic capacitor - BXF series	Rubycon	450BXF22M12.5X20
10	1	C5	4.7 µF 1206 50 V ±10%	Multi-layer ceramic capacitor	KEMET	C1206C475K5PACTU
11	1	C7	0.68 nF 0603 50 V ±5%	Multi-layer ceramic capacitor	KEMET	C0603C681J5GACTU
12	0	C8	Not connected	Multi-layer ceramic capacitor		
13	1	C9	1 nF 1206 630 V ±5%	Multi-layer ceramic capacitor	TDK	C3216C0G2J102J085AA
14	1	C10	68 nF 0603 50 V ±10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012206094
15	1	C11	680 µF, 25 V, ultra-low ESR, through hole	Electrolytic capacitor - ZL series	Rubycon	25ZL680MEFC10X20
16	1	C12	100 µF, 35 V, through hole	Electrolytic capacitor	Wurth Elektronik	860020573008
17	1	C13	2.2 nF through hole	Y1 capacitor	Vishay	VY1222M37Y5VQ63V0
18	0	C14	Not connected, 0603	Multi-layer ceramic capacitor		
19	1	C15	100 nF 0603 25 V ±10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012206071
20	0	C16	Not connected, 0603	Multi-layer ceramic capacitor		
21	1	L1	1 mH through hole, 0.5 A ±10%	Power inductor - RFB series	Coilcraft	RFB0810-102L

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
22	1	L2	3.3 µH SMD 3.23 A	Shielded power inductor	Wurth Elektronik	74404043033A
23	1	L3	5.6 µH 0805 0.16 A	Small signal inductance	Wurth Elektronik	744760356A
24	1	T1	20 mH through hole, 0.5 A ±30%	Common mode choke	Wurth Elektronik	744821120
25	1	T2	750317580 rev05, through hole	Flyback transformer	Wurth Elektronik	750317580
26	1	NTC	10 Ohm through hole, ±20%	Thermistor	EPCOS	B57237S0100M000
27	1	F	2 A/250 V through hole	Fuse	Wickmann	3821200041
28	0	R1	Not connected, 0805	UVP-OVP resistor		
29	0	R2	Not connected, 0805	UVP-OVP resistor		
30	0	R3	Not connected, 0805	UVP-OVP resistor		
31	0	R4	Not connected, 0805	UVP-OVP resistor		
32	0	R5	Not connected, 0603	Resistor		
33	1	R6	0 Ohm 0603	Resistor	Any	
34	1	R7	0 Ohm through hole	Resistor	Any	
35	0	R8	Not connected, 0603	Resistor		
36	1	R9	220 k Ohm 1206 0.6 W ±5%	Snubber resistor	TE Connectivity	CRGS1206J220K
37	1	R10	0 Ohm 0603	Resistor	Any	
38	1	R11	1.5 k Ohm 0603 0.1 W ±1%	Resistor	Vishay	CRCW06031K50FKEA
39	1	R12	100 k Ohm 0603 0.2 W ±1%	Resistor	Panasonic	ERJP03F1003V
40	1	R13	9.1 k Ohm 0603 0.1 W ±1%	Resistor	Panasonic	ERJU03F9101V
41	0	R14	Not connected, 0603	Resistor		
42	1	R16	820 Ohm 0603 0.25 W ±1%		Vishay	CRCW0603820RFKEA
43	1	R17	0 Ohm 0603	OVP disable resistor	Any	
44	1	Rz	12 Ohm 0805 0.5 W ±5%	Resistor	TE Connectivity	CRGS0805J12R
45	1	IC1	VIPer318LD, SO-16N	Energy saving off-line high voltage converter	ST	VIPER318LDTR
46	1	IC2	TS3431 SOT-23	1.24 V adjustable shunt voltage reference	ST	TS3431BILT

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
47	1	IC3	SFH610-A through hole, PDIP	Optocoupler	Vishay	SFH610A-2
48	1	IN	282837-2 through hole, 250 Vac 13.5 A	Two-way input connector	TE Connectivity	282837-2
49	1	OUT	282837-2 through hole, 250 Vac 13.5 A	Two-way output connector	TE Connectivity	282837-2

1.4 Transformer

Table 3. Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Wurth Elektonik	-
Part number	750317580 rev05	-
Primary inductance (pins 3 - 5)	1.5mH ±10%	10kHz, 100mV, Ls
Leakage inductance	30uH typ, 45uH max	tie(1+2, 6+7+9+10),100kHz, 100mV, Ls
Primary to sec turn ratio	5:1, ± 1%	(3-5):(10-6), tie(6+7, 9+10)
Primary to aux turn ratio	9.38 ± 1%	(3-5):(2-1)
Reflected voltage	78V	
Saturation current	1.5A max	20% roll-off from initial
Operating current	0.7A max	
DC-DC resistance 3-5	3.45 Ω ±10%	20°C
DC-DC resistance 2-1	0.475 Ω ±10%	20°C
DC-DC resistance 10-6	0.115 Ω ±10%	20°C, tie(6+7, 9+10)

Figure 3. **Electrical and pin diagrams**

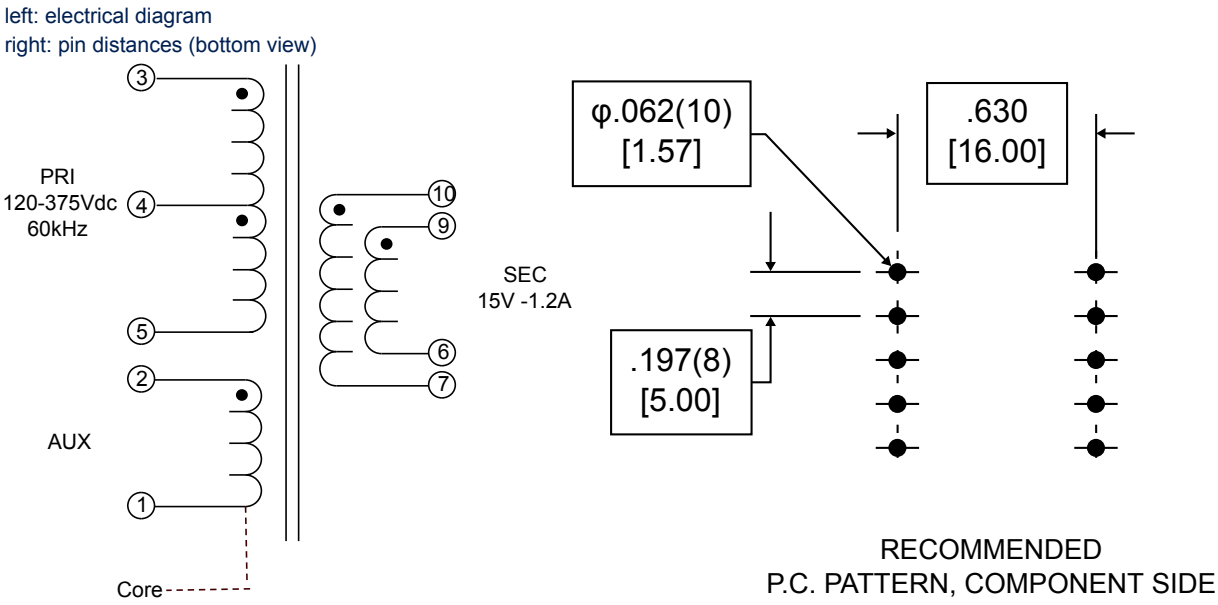
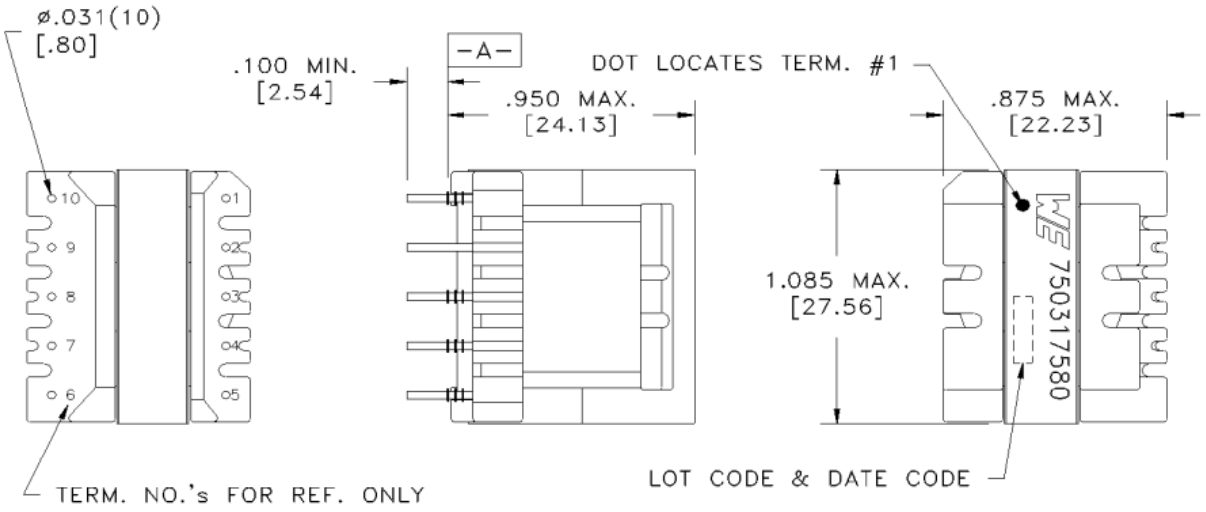


Figure 4. **Transformer dimensions (bottom, side and top view)**



2 Performance

2.1 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies contained in a separate housing from the devices they are powering need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion. It states that an SMPS with power throughput of 18 W should have an active mode efficiency higher than 85.45%.

Another applicable standard Department of Energy (DOE) recommendation, whose active mode efficiency requirement for the same power throughput is 85.00%.

The values in the following table show that the SMPS is compliant with both standards.

Table 4. Active mode efficiency

Regulation requirements at P_{OUTnom}=18W		Efficiency
CoC5 req.	DOE req.	
85.45%	85.00%	85.67% (at V_{IN}=115V_{AC})
		86.28% (atV_{IN}=230VAC)

2.2 Light load performance

CoC5 has also efficiency requirements when the output load is 10% of the nominal output power. The values in the following table demonstrate the compliance of the power supply with this requirement.

Table 5. Performance at 10% output load

CoC5 eff. Req. at P_{OUTnom}/10 (P_{OUTnom} = 18 W)	Efficiency
75.45%	83.55% (at V_{IN}=115V_{AC})
	76.78% (at V_{IN}=230V_{AC})

In version 5 of the Code of Conduct, the power consumption of the power supply when it is not loaded is also considered. The compliance criteria for EPS converters with nominal output power below 49 W and the STEVAL-VP318L1F no-load input power consumption measurements at 115 V_{AC} and 230 V_{AC} nominal input voltages are given in the following table. The board is also compliant with these requirements.

Table 6. Performance at no load

Max no load consumption (0.3W < Pno < 49W)	Board no load consumption
75mW	42.6 mW (at V_{IN}=115V_{AC})
	44.5 mW (at V_{IN}=230V_{AC})

Another requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The values in the following table verify the compliance of the board with this requirement, as well as showing efficiency measurements in certain other light load conditions (P_{OUT} = 25mW, P_{OUT} = 50mW).

Table 7. Performance and efficiency at light load

V_{IN} [V_{AC}]	Efficiency [%]		
	P_{OUT}=25mW	P_{OUT}=50mW	P_{OUT}=250mW
115	77	115	359
230	81	121	374

Another criterion is the output power (or the efficiency) when the input power is equal to one watt, the values for which are provided in the following table.

Table 8. Performance at P_{IN} = 1 W

V_{IN} [V_{AC}]	Efficiency at P_{IN}=1W [%]
115	78.3
230	70.8

2.3 Typical waveforms

The following figures show the drain voltage and current waveforms in full load condition for the two nominal input voltages.

Figure 5. Drain voltage and current at 115 V_{AC}, max. load

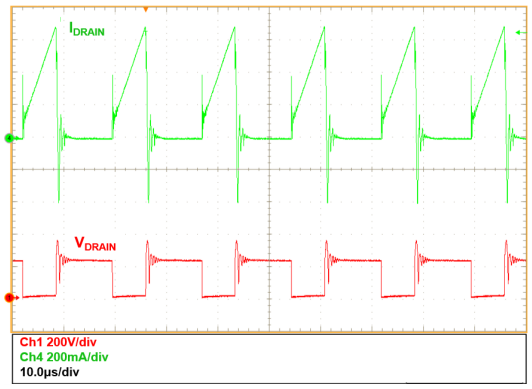
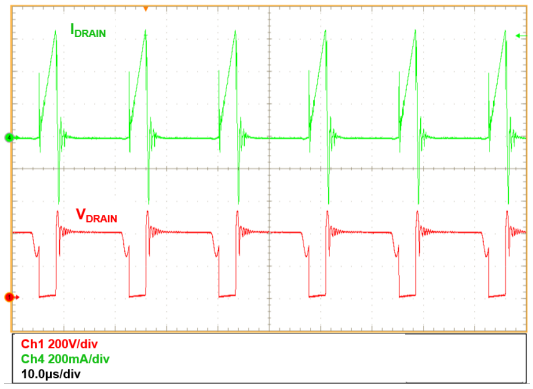


Figure 6. Drain voltage and current at 230 V_{AC}, max. load



The following figures show the drain voltage and current waveforms in full load condition for the minimum and maximum input voltages.

Figure 7. Drain voltage and current at 90 V_{AC}, max. load

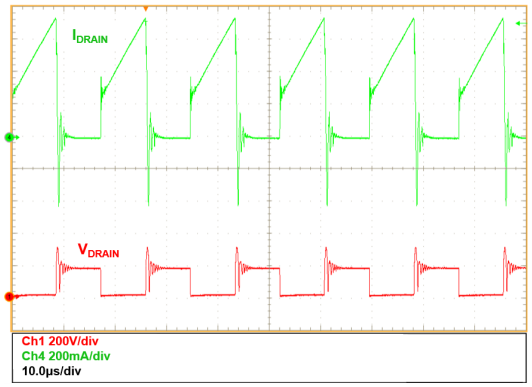
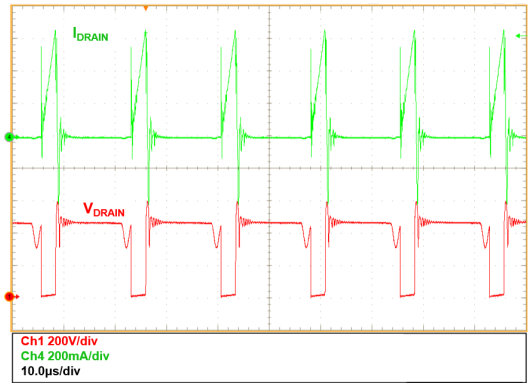


Figure 8. Drain voltage and current at 265 V_{AC}, max. load



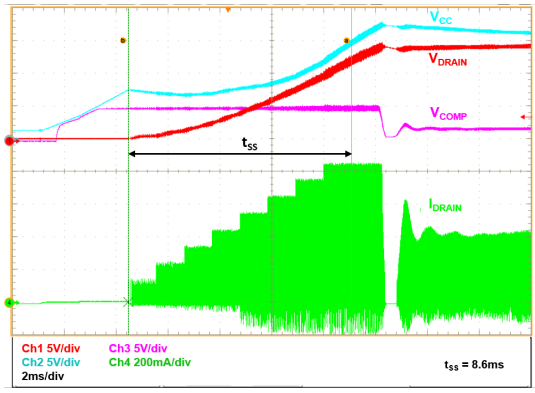
3 Functional check

3.1 Soft start

As V_{DRAIN} exceeds $V_{HVSTART}$ at power-up, the internal HV current generator charges the V_{CC} capacitor C5 to V_{CCon}, the Power MOSFET starts switching, the current generator is turned off, and the IC is powered by the energy stored in C5.

An internal soft-start function progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in 8 steps. In this way, the DRAIN current is limited during output voltage increase, thus reducing the stress on the secondary diode. The soft-start time t_{SS} needed for the current limitation set-point to reach its final value is internally fixed at 8 ms. This function is activated on any converter start-up attempt and after a fault event. The soft start phase is shown in the following figure.

Figure 9. Soft start



3.2 Overload protection

In an overload or short-circuit event, the drain current value reaches I_{DLIM}. Every cycle this condition is met, an internal OCP counter is incremented, and if the overload is maintained continuously for time t_{OVL} (50 ms typical, internally fixed), the counter reaches its end-of-count and the protection is tripped (Figure 10). The power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 s typical, Figure 11). After this time has elapsed, the device resumes switching and, if the fault is still present, the protection continues triggering indefinitely. This lowers the repetition rate of converter restart attempts so that it works safely with extremely low power throughput and avoids IC overheating in case of repeated overload events.

Figure 10. OLP fault applied during steady state operation t_{OVL}

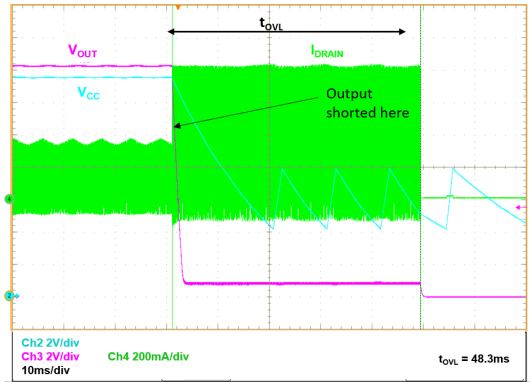
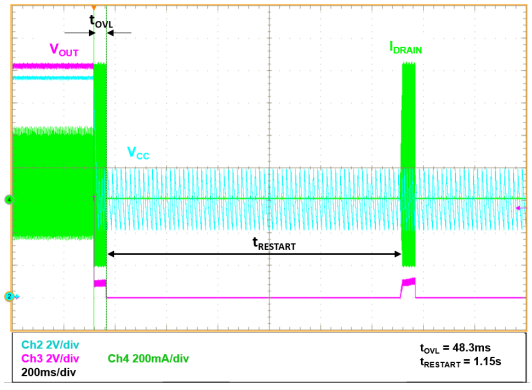


Figure 11. OLP fault applied during steady state operation $t_{RESTART}$



Furthermore, at startup after any protection tripping, the internal soft start-up function is invoked (Figure 12), in order to reduce the stress on the secondary diode.

After fault removal, the IC resumes working normally. If the fault is removed during t_{SS} or t_{OVL} (i.e., before protection tripping), the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short circuit is removed during $t_{RESTART}$, the IC has to wait for $t_{RESTART}$ to elapse before switching resumes (Figure 13).

Figure 12. OLP fault maintained t_{SS} and t_{OVL}

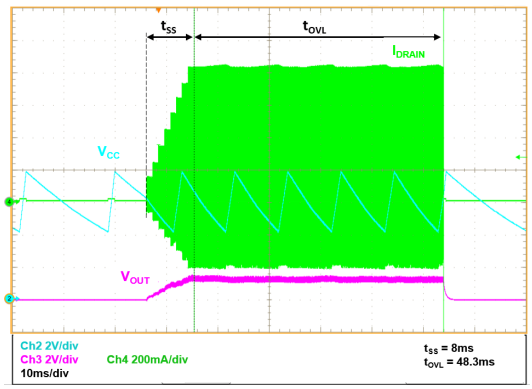
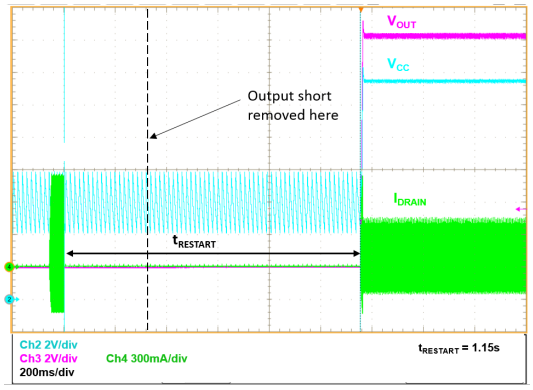


Figure 13. OLP fault removed and autorestart



3.3 Pulse skip mode

Any time the I_{DRAIN} drain peak current exceeds I_{DLIM} within the t_{ON_MIN} minimum on-time, one switching cycle is skipped. The check is made on a cycle-by-cycle basis and the cycles can be skipped until the F_{OSC_MIN} minimum switching frequency (15 kHz, typ.) is reached.

If the above condition persists and the internal OCP counter reaches its end-of-count, the IC is stopped for $t_{RESTART}$ (1 s, typ.) and activated again through a soft-start.

Any time I_{DRAIN} does not exceed I_{DLIM} within t_{ON_MIN}, one switching cycle is restored. The check is made on a cycle-by-cycle basis and the cycles can be restored until the nominal switching frequency F_{OSC} is reached.

This protection provides, when required, more time for inductor discharge than what allowed at nominal switching frequency, thus helping limiting the "flux runaway" effect, often occurring at converter startup and consisting in a net increase of the average inductor current when the primary MOSFET, charged during the minimum on-time through the input voltage, cannot discharge the same amount during the off-time, due to a very low output voltage. This current has to be limited as it could reach dangerously high values for the power components during the startup first cycles , until the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance.

We captured a startup sequence at 250 V_{DC} to test the protection. Figure 14 shows the initial phase with switching cycles at reduced frequency. F_{OSC_MIN} = 15 kHz is reached during the very first cycles (Figure 15). The 30 kHz and 60kHz switching cycles then alternate for a certain period until the nominal 60 kHz F_{OSC} is restored (Figure 16).

Figure 14. **Short-circuit at 250 V_{DC} – pulse skipping**

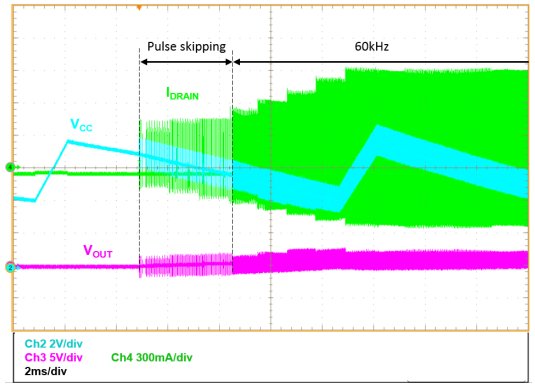


Figure 15. **Short-circuit at 250 V_{DC} – pulse skipping (zoom 1)**

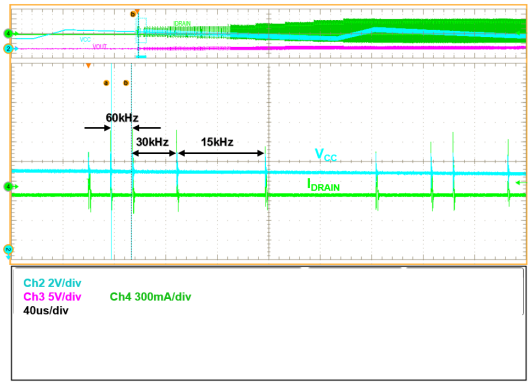
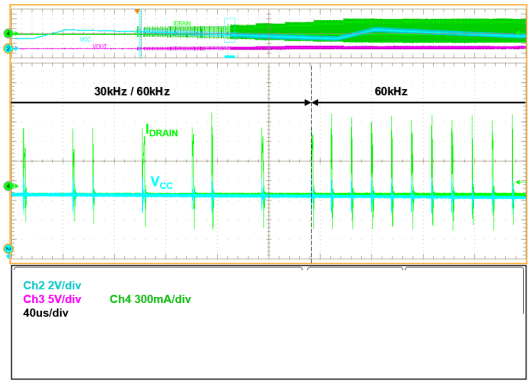


Figure 16. **Short-circuit at 250 V_{DC} – pulse skipping (zoom 2)**



3.4 Input undervoltage/overvoltage

Input undervoltage and overvoltage protections are available on the respective UVP and OVP pins and can be enabled or disabled independently. by default, the protections are both disabled, but the voltage divider R1, R2, R3 and R4 is available to allow UVP and OVP implementation.

The input voltage divider high-side resistor selection should be a high value in order to limit the power consumption from the mains and should be divided in two to withstand high input voltage values. in our example, 3 MΩ values are selected for R1 and R2.

The medium-side and low-side resistors, R3 and R4, are selected through the following formulas:

$$R4 = \frac{V_{in\_UVP} + I_{UVP\_pull-up} \cdot RH - \sqrt{\left(V_{in\_UVP} + I_{UVP\_pull-up} \cdot RH\right)^2 - 4 \cdot V_{UVP\_th} \cdot I_{UVP\_pull-up} \cdot RH}}{2 \cdot I_{UVP\_pull-up}} \quad (1)$$

$$R3 = \left(V_{OVP\_th} - R4 \cdot I_{UVP\_pull-up}\right) \cdot \frac{RH}{V_{in\_OVP}} - R4 \quad (2)$$

where RH = R1 + R2; V_{UVP_th} and V_{OVP_th} are the UVP and OVP pin thresholds reported in the VIPer31 datasheet (0.4V and 4V typical respectively); V_{in_UVP} and V_{in_OVP} are the required input UVP and OVP thresholds (i.e., the input voltage values corresponding to V_{UVP_th} on UVP pin; and V_{OVP_th} on OVP pin, respectively); $I_{UVP\_pull-up}$ is the internal pull-up current on the UVP pin.

As an example, if we select V_{IN_UVP} = 50 V_{DC} and V_{IN_OVP} = 380 V_{DC} in equations (1) and (2), then we obtain: R3 = 20 kΩ and R4 = 43 kΩ.

Input undervoltage protection behaves in the following way:

- When the input voltage drops below V_{IN_UVP}, the UVP pin voltage falls below V_{UVP_th} and an internal counter is activated.
- If V_{UVP} remains lower than V_{UVP_th} for more than t_{UVP_DEB} (30 ms typ.), the IC is stopped with no restart attempts.
- This is shown in Figure 17, where V_{IN_UVP} measures about 51 V as expected.
- As long as V_{UVP} remains below V_{UVP_th}, most of the internal blocks are disabled and the internal consumption is reduced to ultra-low values, while V_{CC} is maintained between V_{CSon} and V_{CCon} by the periodical activation of the internal HV-current source, as shown in Figure 18.

Figure 17. V_{IN} from 60 to 50 V_{DC}: UVP triggering

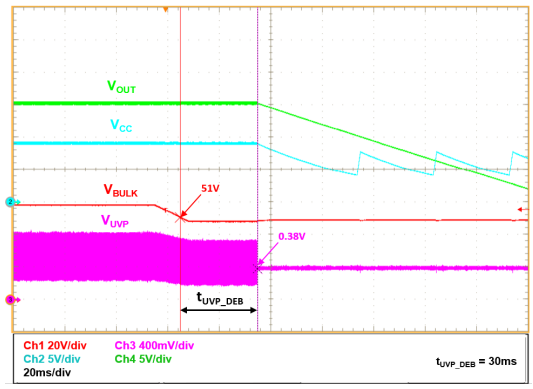
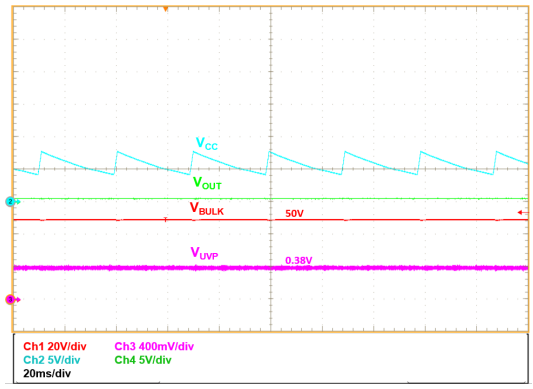


Figure 18. V_{IN} 50 V_{DC}: UVP steady-state



When V_{IN} exceeds V_{IN_UVP}, the UVP pin voltage exceeds V_{UVP_th}. If this condition is maintained for more than t_{UVP_REST} (30 ms, typ.), normal operation is restored (Figure 19).

Input overvoltage protection behaves in the following way:

- When the input voltage rises above V_{IN_OVP}, the OVP pin voltage exceeds V_{OVP_th} and an internal counter is activated.
- If V_{OVP} remains higher than V_{OVP_th} for more than t_{OVP_DEB} (250 µs typ.), the IC is stopped.
- This is shown in Figure 20, where V_{IN_OVP} measures about 381 V as expected.

Figure 19. V_{IN} from 60 to 50 V_{DC}: resuming from UVP

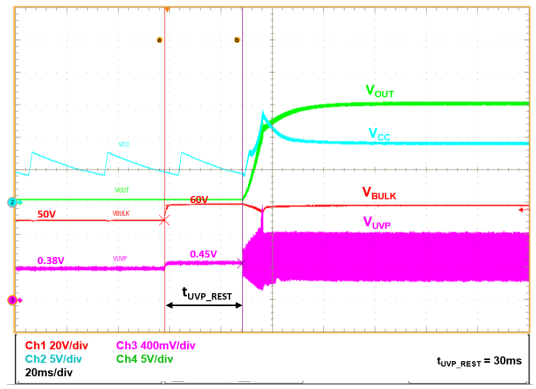
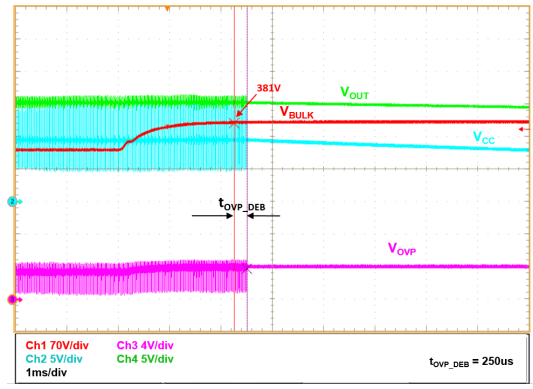


Figure 20. V_{IN} from 325 to 385 V_{DC}: OVP triggering



- OVP stops the device in auto-restart for t_{OVP_REST} (500 ms, typ.), the duration of restart attempts is t_{OVP_DEB}, as shown in Figure 21 and Figure 22.

Figure 21. V_{IN} 385 V_{DC}: OVP steady state

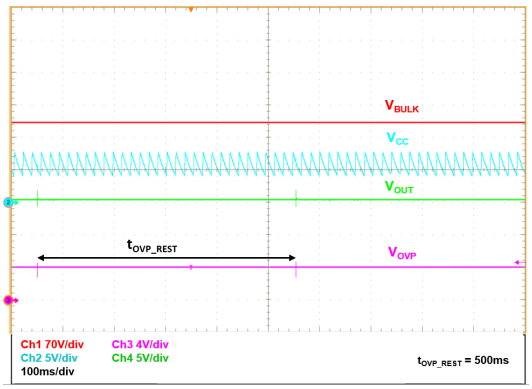
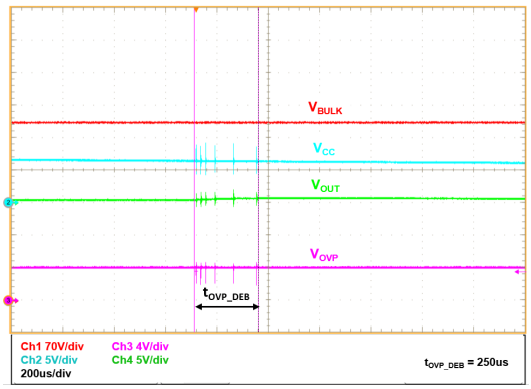


Figure 22. V_{IN} 385 V_{DC}: OVP steady state (zoom)



- When V_{IN} falls below V_{IN_OVP}, the OVP pin voltage goes below V_{OVP_th}.
- If this condition is maintained for more than t_{OVP_DEB}, the VIPer31 restarts switching with soft-start phase and normal operation is restored (Figure 23 and Figure 24).

Figure 23. V_{IN} from 385 to 320 V_{DC}: resuming from OVP

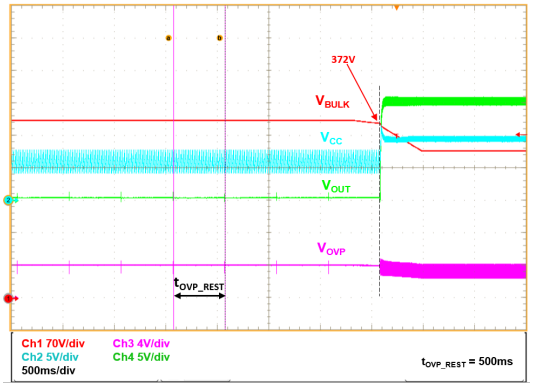
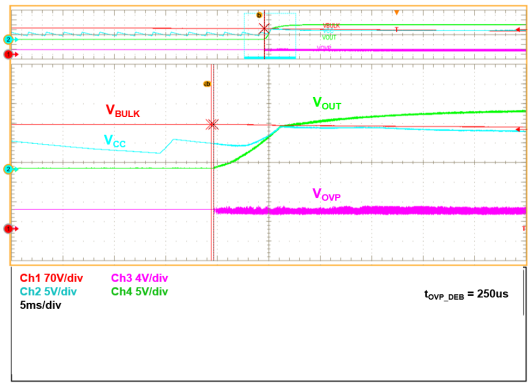


Figure 24. V_{IN} from 385 to 320 V_{DC}: resuming from OVP (zoom)



The power consumption of the input undervoltage/overvoltage network can be calculated as:

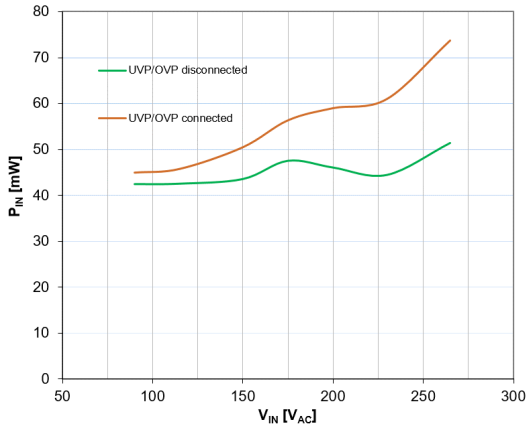
$$P_{IN_{UVP\_UVP}}\left(V_{IN}\right) = \frac{V_{IN}^2}{(R1 + R2 + R3 + R4)} \quad (3)$$

This results in less than 18 mW consumption at 230 V_{AC} (~325 V_{DC})

If the undervoltage and overvoltage protections are not required, the OVP pin should be connected to GND pin (selecting R17 = 0 Ω), the UVP pin should be left floating, and the R1, R2, R3, R4 voltage divider should be disconnected.

The following figure shows the no-load consumption curves vs V_{IN} for a connected and disconnected protection network. When the OVP/UVP network is connected, the power supply no load consumption at 230 V_{AC} is about 60 mW.

Figure 25. **No load consumption vs V_{IN} with and without UVP/OVP network**



3.5 Overtemperature protection

The Power MOSFET junction temperature is sensed during the on time through a diode integrated in the HV section of the chip. If a junction temperature higher than T_{SD} (160 °C, typ.) is measured, the PWM is disabled for $t_{RESTART}$.

In order to increase robustness against electromagnetic noise, the protection is ONLY triggered if the condition is met for n_{th} = 3 consecutive switching cycles. After $t_{RESTART}$, the IC resumes switching with soft start phase and if a junction temperature above T_{SD} is still measured for three consecutive switching cycles, the protection is triggered and PWM is disabled again for $t_{RESTART}$; otherwise, normal operation is restored.

During $t_{RESTART}$, the V_{CC} pin voltage is maintained between V_{CSon} and V_{CCon} by the HV current source periodical activation.

A 1nF/1000V capacitor has been soldered between DRAIN and GND in order to increase device temperature with increased switching losses. In this way, the protection is tripped at 230 V_{DC}/ 300 mA at a measured case temperature of 165 °C.

Figure 26. **Thermal shutdown at T_{SD} = 165 °C**

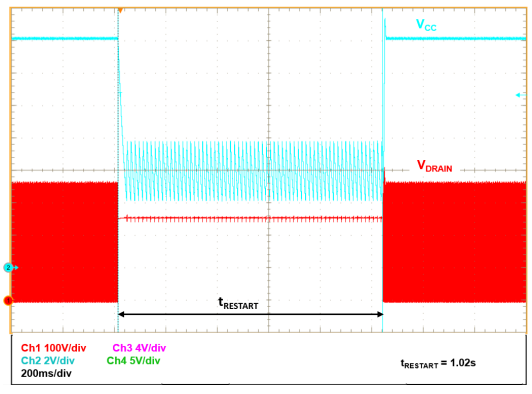
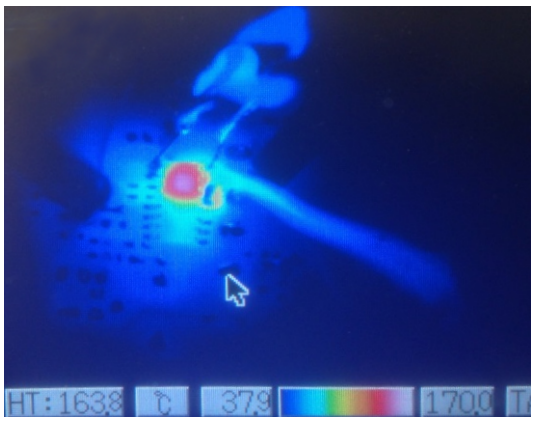


Figure 27. **Thermal shutdown at T_{SD} = 165 °C (thermal image)**



4 Thermal measurements

A thermal analysis of the board was performed using an IR camera for 85 V_{AC}, 115 V_{AC}, 230 V_{AC} and 265 V_{AC} mains input at full load condition. The results are shown in the following figures.

Figure 28. Thermal image at 90 V_{AC}, full load, T_{AMB} = 25 °C

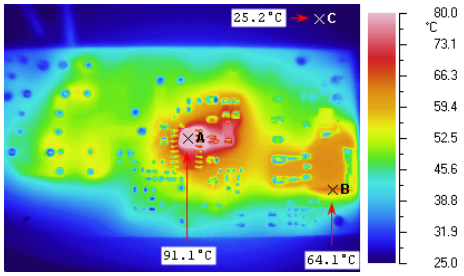


Figure 29. Thermal image at 115 V_{AC}, full load, T_{AMB} = 25 °C

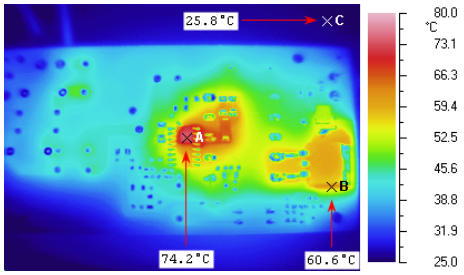


Figure 30. Thermal image at 230 V_{AC}, full load, T_{AMB} = 25 °C

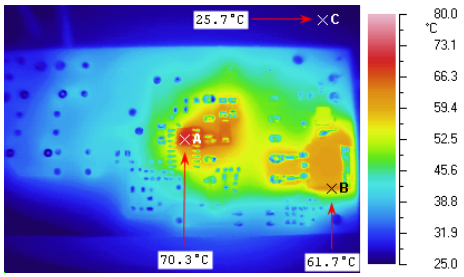
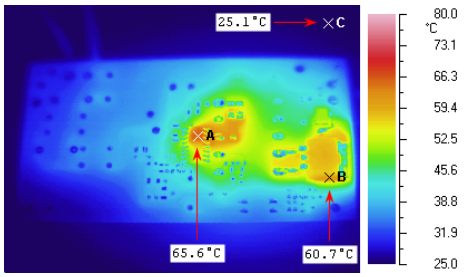


Figure 31. Thermal image at 265 V_{AC}, full load, T_{AMB} = 25 °C



5 EMI measurements

Pre-compliance tests regarding EN55022 (Class B) European normative with average detector were performed using an EMC analyzer and a LISN. The results are shown in the following figures.

Figure 32. Average measurements at 115 V_{AC}, full load, T_{AMB} = 25 °C

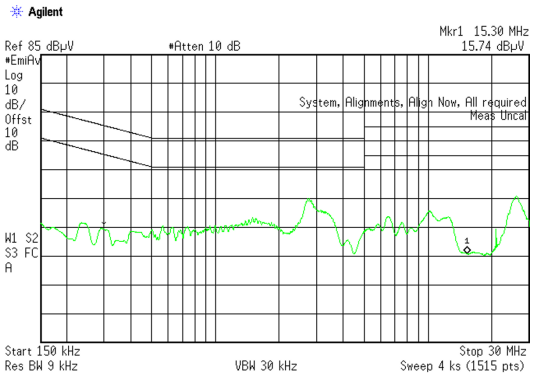
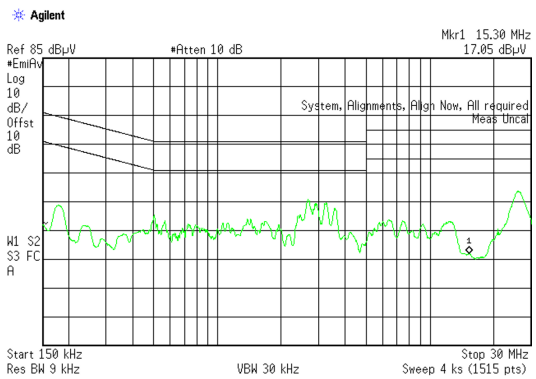


Figure 33. Average measurements at 230 V_{AC}, full load, T_{AMB} = 25 °C



6 Board layout

Figure 34. **Board layout - top layer**

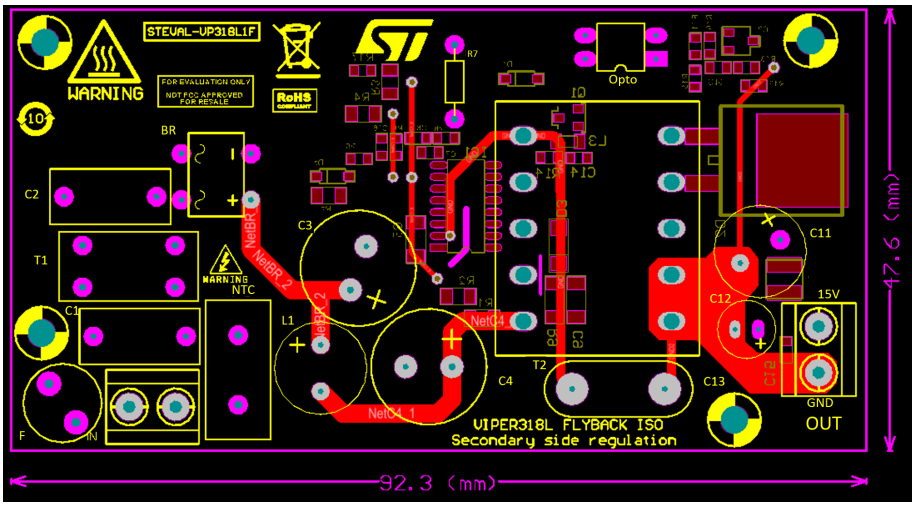
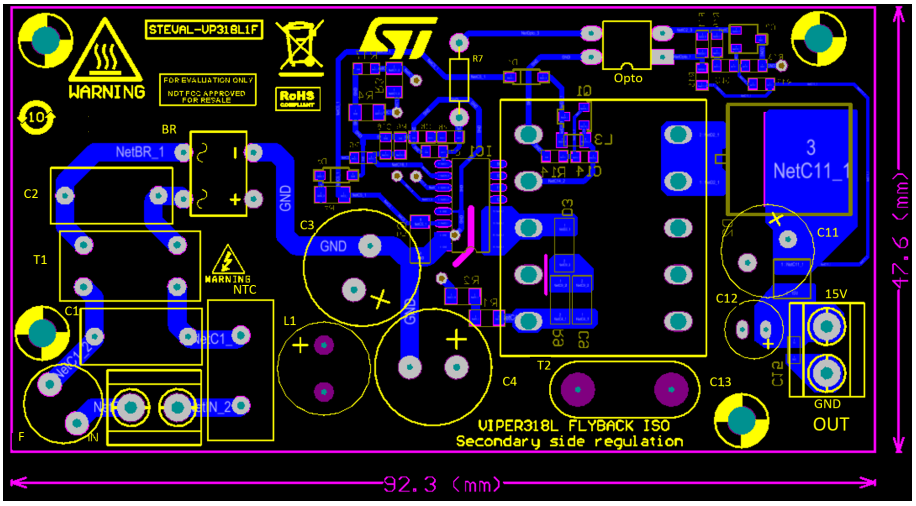


Figure 35. **Board layout - bottom layer**



7 Conclusion

We tested the STEVAL-VP318L1F single-output 15V/18W evaluation board in Flyback isolated topology using the VIPer318L, and demonstrated how the VIPER31 can support SMPS converter designs that comply with the most stringent energy regulations, and reduce size, complexity and BoM requirements.

STEVAL-VP318L1F consumes less than 50 mW at 230 V_{AC} mains in no load condition and can satisfy both CoC 5 and DOE requirements for active mode and light load efficiency for External Power Supplies.

The 800 V, avalanche rugged Power MOSFET and the embedded protections render the VIPer31 ideal for applications requiring robust, reliable and energy efficient performance.

Appendix A CCM flyback converter transfer function

The control-to-output transfer function of the flyback converter in CCM, $G_{vc}(s)$, is given by the approximation:

$$G_{vc}(s) \approx H_O \cdot \frac{\left(1+\frac{s}{\omega_{Z1}}\right)\cdot\left(1-\frac{s}{\omega_{Z2}}\right)}{1+\frac{s}{\omega_{P1}}} \quad (4)$$

Gain, poles and zero are defined below:

$$H_O = \frac{n \cdot R_O}{H_{COMP}} \cdot \frac{1-D}{1+D} \quad (5)$$

$$\omega_{Z1} = \frac{1}{R_C \cdot C_O} \quad (6)$$

$$\omega_{Z2} = \frac{-\left[n^2 \cdot (1-D)^2 \cdot R_O\right]}{D \cdot L} \quad (7)$$

$$\omega_{P1} = \frac{1+D}{R_O \cdot C_O} \quad (8)$$

Where:

- n = primary to secondary turns ratio
- $R_0 = V_{OUT}/I_{OUT}$ = nominal output resistance
- C_0 = capacitance of the output capacitor
- R_C = ESR of the output capacitor
- D = converter duty cycle
- L = primary inductance
- $H_{COMP} = \Delta V_{COMP}/\Delta I_{DRAIN}$ (from device datasheet)

A.1 CCM flyback type-2 compensator design

To compensate the CCM flyback, we use a type-2 compensator featuring the integrator effect that provides high DC gain to minimize static error, as well as a pole-zero pair to boost the phase according to the phase margin target.

$$G_{c(s)} = G_{co} \cdot \frac{1+\frac{s}{\omega_{zc}}}{s \cdot \left(1+\frac{s}{\omega_{pc}}\right)} \quad (9)$$

The compensator is determined using a manual pole-zero placement technique in which the zero is placed in the vicinity of the power stage dominant pole to cancel its effect and the pole position is adjusted to achieve the required phase margin.

Follow the procedure below to design compensation with a type 2 compensator:

Step 1. Select the crossover frequency f_C and the phase margin Φ_m :

For CCM flyback, the crossover frequency must be selected as low as possible with respect to the RHP zero ω_{Z2} in order to limit the phase degradation that it introduces.

As a general rule, you should set f_C to below 20% of the RHP zero.

Step 2. Evaluate the gain and phase of the plant at crossover frequency:

$$G_{vc}(f_C) = \left|G_{vc}(2 \cdot \pi \cdot f_C)\right| \quad (10)$$

$$\Phi_{vc}(f_C) = arg\left[G_{vc}(2 \cdot \pi \cdot f_C)\right] \quad (11)$$

Step 3. The compensated open-loop gain must attain the unit gain at f_C , with the required phase margin, therefore the compensator must have following gain and phase at f_C :

$$G_c(f_C) = |G_c(2 \cdot \pi \cdot f_C)| = \frac{1}{G_{vc}(f_C)} \quad (12)$$

$$\Phi_c(f_C) = arg[G_c(2 \cdot \pi \cdot f_C)] = 90 - 180 + \Phi_m - \Phi_{vc}(f_C) \quad (13)$$

Step 4. Cancel the pole of the plant f_{P1} by placing the zero of the compensator f_{zc} in the neighborhood ($\alpha =$ 1 to 5):

$$f_{zc} = \frac{\omega_{zc}}{2 \cdot \pi} = \alpha \cdot f_{P1} \quad (14)$$

Step 5. Place the pole of the compensator to boost the phase and to obtain the desired phase margin:

$$f_{pc} = \frac{f_C}{tan\left[tan^{-1}\left(\frac{f_C}{f_{zc}}\right) - \Phi_c(f_C)\right]} \quad (15)$$

Step 6. Calculate the gain G_{co} :

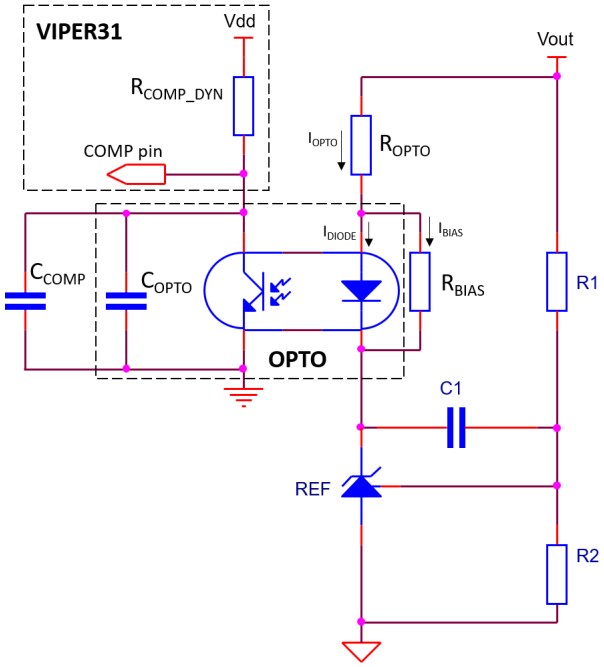
$$G_{co} = G_c(f_C) \cdot \frac{\omega_C \cdot \sqrt{1 + \left(\frac{f_C}{f_{pc}}\right)^2}}{\sqrt{1 + \left(\frac{f_C}{f_{zc}}\right)^2}} \quad (16)$$

$G_C(s)$ is thus determined.

A.2 Compensator network implementation

The figure below shows the complete schematic arrangement for the type-2 error amplifier in secondary side regulation (SSR). The resistors R_1 and R_2 are used to define the output voltage set point. The resistor R_{OPTO} is used to bias the emitter, while the resistor R_{BIAS} is used to provide the minimum biasing current to the reference voltage, REF. The capacitors C_1 and C_{COMP} are used for the compensation, even if the other components also affect the overall compensator transfer function.

Figure 36. Secondary feedback implementation using secondary reference voltage and optocoupler



With reference to the implementation of the figure above, the general expression of the compensator transfer function given in Equation 9 takes this particular form:

$$G_C(s) = \frac{CTR \cdot R_{COMP\_DYN}}{R_{OPTO} \cdot R1 \cdot C1} \cdot \frac{1 + s \cdot R_1 \cdot C_1}{s \cdot \left[1 + s \cdot R_{COMP\_DYN} \cdot (C_{COMP} + C_{OPTO})\right]} \quad (17)$$

In the equation, capacitor C_{OPTO} is the intrinsic capacitor across the collector that introduces a pole in the transfer function and limits the frequency response. As this pole becomes part of the controller transfer function, specific test measurements are required to determine the correct value as close as possible to the real operating conditions of the selected optocoupler.

Component selection is based on the procedure shown below.

Step 1. Calculate the value of the resistor R_{BIAS} .

The purpose of this resistor is to provide the minimum bias current to the reference REF necessary for correct operation. Considering that the forward voltage of the opto-diode is almost constant (typically ≈ 1 V), the value of R_{BIAS} is simply given by:

$$R_{BIAS} \leq \frac{V_F}{I_{BIAS}} \quad (18)$$

Where I_{BIAS} is the minimum cathode current for regulation of the reference (500 µA for TS3431).

Step 2. The next step is the selection of I_{R1} .

The value must be high enough to minimize the residual losses across the output, but low enough to ensure that the input current of the reference pin of REF is negligible compared with the current across R_1 itself. A general rule is $I_{R1} \geq 50 \cdot I_{REF}$.

Step 3. Select resistor R_2 to define the output voltage set-point:

$$R_2 = R_1 \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad (19)$$

Where V_{REF} is the REF reference voltage (1.24 V for TS3431)

Step 4. Calculate the value of capacitor C_1 to cancel the pole of the plant :

$$C_1 = \frac{1}{2 \cdot \pi \cdot R_1 \cdot f_{zc}} \quad (20)$$

Step 5. Set the value of R_{OPTO} to ensure the minimum current through the opto-diode to properly drive the COMP pin with the current I_{COMP}, ensuring the full dynamic of the pin.

If I_{OPTO} is the current flowing through R_{OPTO}, the current through the optodiode, I_{DIODE}, is given by:

$$I_{DIODE} = I_{OPTO} - I_{BIAS} = \frac{V_{OUT} - V_F - V_{REF}}{R_{OPTO}} - \frac{V_F}{R_{BIAS}} \quad (21)$$

Step 6. Check that the following condition is satisfied:

$$I_{DIODE} \cdot CTR \geq I_{COMP} \quad (22)$$

Step 7. The maximum value of R_{OPTO} can now be derived:

$$R_{OPTO} \leq \frac{V_{OUT} - V_F - V_{REF}}{\frac{I_{COMP}}{CTR} + \frac{V_F}{R_{BIAS}}} \quad (23)$$

Step 8. The value of I_{COMP} is the maximum source current provided by the pin (usually during burst mode condition) and is provided by the controller datasheet, whereas the value of CTR is achieved by characterization.

The final value of R_{OPTO} is selected to fulfill the compensator gain requirement:

$$R_{OPTO} = \frac{CTR \cdot R_{COMP\_DYN}}{R_1 \cdot C_1 \cdot G_{co}} \quad (24)$$

Step 9. Finally, the value of C_{COMP} is calculated from the compensator pole placement

$$C_{COMP} = \frac{1}{2 \cdot \pi \cdot f_{pc} \cdot R_{COMP\_DYN}} - C_{OPTO} \quad (25)$$

Table 9. Summary of compensator component calculations and results

Part	Ref. equation	Theoretical value	Selected value
R_{BIAS}	$\leq \frac{V_F}{I_{BIAS}}$	2 kΩ	1.5 kΩ
R_1	$\frac{V_{OUT} - V_{REF}}{50 \cdot I_{REF}}$	306 kΩ	100 kΩ
R_2	$R_1 \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}$	9 kΩ	9.1 kΩ
C_1	$\frac{1}{2 \cdot \pi \cdot R_1 \cdot f_{zc}}$	65 nF	68 nF
R_{OPTO}	$\frac{CTR \cdot R_{COMP\_DYN}}{R_1 \cdot C_1 \cdot G_{co}} \leq \frac{V_{OUT} - V_F - V_{REF}}{\frac{I_{COMP}}{CTR} + \frac{V_F}{R_{BIAS}}}$	0.752 kΩ ≤ 10.18 kΩ	0.82 kΩ
C_{COMP}	$\frac{1}{2 \cdot \pi \cdot f_{pc} \cdot R_{COMP\_DYN}} - C_{OPTO}$	0.662 nF	0.68 nF

The resulting crossover frequency f_C and phase margin Φ_m are:

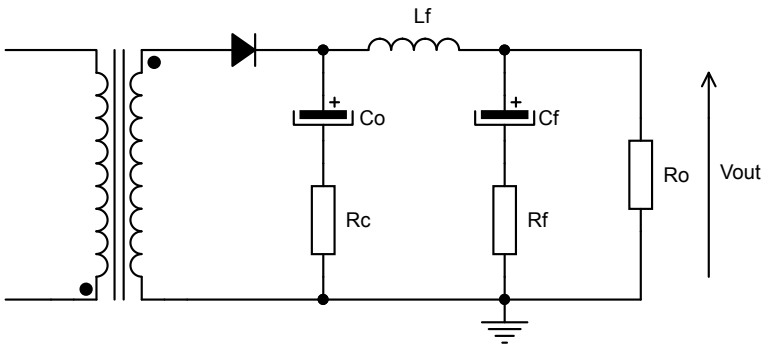
$$f_C \approx 1.15kHz$$
$$\Phi_m \approx 76°$$

Appendix B Effect of output LC post filter stage in flyback converters

Large capacitors are usually used in flyback converters to build the output filter, and it is important to factor in the RMS ripple rating and the parasitic resistance ESR when determining the size of the capacitor to satisfy the output ripple specification.

When the requirement of the ripple is very tight, a simple low cost LC filter can be used to attenuate the ripple to the desired level instead of using a large number of capacitors that increase the cost.

Figure 37. Output LC post filter for ripple reduction



Although this solution is very simple and cost effective, it changes the behavior of the plant and extra care must be placed to deal with the compensation design.

Assuming that C_O is much larger than C_f , the total transfer function of the plant in presence of the LC filter can be expressed as:

$$G'_{vc}(s) = G_{vc}(s) \cdot \frac{1 + \frac{s}{\omega_f}}{1 + \frac{s}{\omega_f \cdot Q_f} + \left(\frac{s}{\omega_f}\right)^2} \quad (26)$$

Where:

$$\omega_f = \frac{1}{\sqrt{L_f \cdot C_f}} \quad (27)$$

$$Q_f = \frac{1}{\frac{1}{R_O} \cdot \sqrt{\frac{L_f}{C_f}} + \left(R_f + R_c\right) \cdot \sqrt{\frac{C_f}{L_f}}} \quad (28)$$

Where $G_{vc}(s)$ is the transfer function of the plant without the filter.

The presence of the LC output post filter introduces a further zero and a pair of poles in the transfer function. This causes a peak at frequency $\omega_f/(2\pi)$ to appear in the amplitude diagram and a sudden 180° reduction of the phase to occur at the same frequency. Therefore, when you use an LC post filter, it is necessary to design its resonance frequency well above the crossover frequency to keep the resonance peak outside the converter band and to avoid eroding the phase margin or going as far as making the system unstable.

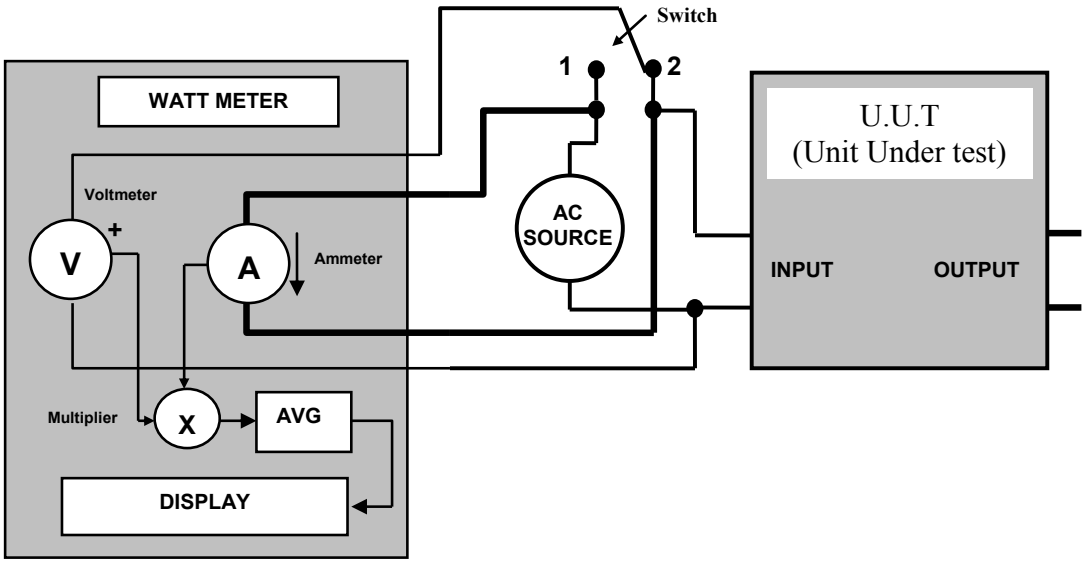
In our board, the LC filter in designed to have the pole pair at frequency $f_f = 8.76kHz$, with a quality factor equal to $Q_f = 0.801$, ensuring negligible phase margin erosion at the crossover frequency.

Appendix C Test equipment and measurement of efficiency and light load performance

The converter input power is measured with a wattmeter, taking simultaneous readings of the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument, so it samples the current and voltage and converts them into digital forms. The digital samples are then multiplied to give the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher, depending on the instrument used). The reading gives the average measured power over a short time interval short period of time (1 s typ.).

The following figure shows the wattmeter connected to the UUT (unit under test) and the AC source, as well as the wattmeter internal block diagram.

Figure 38. Connections of the UUT to the wattmeter for power measurements



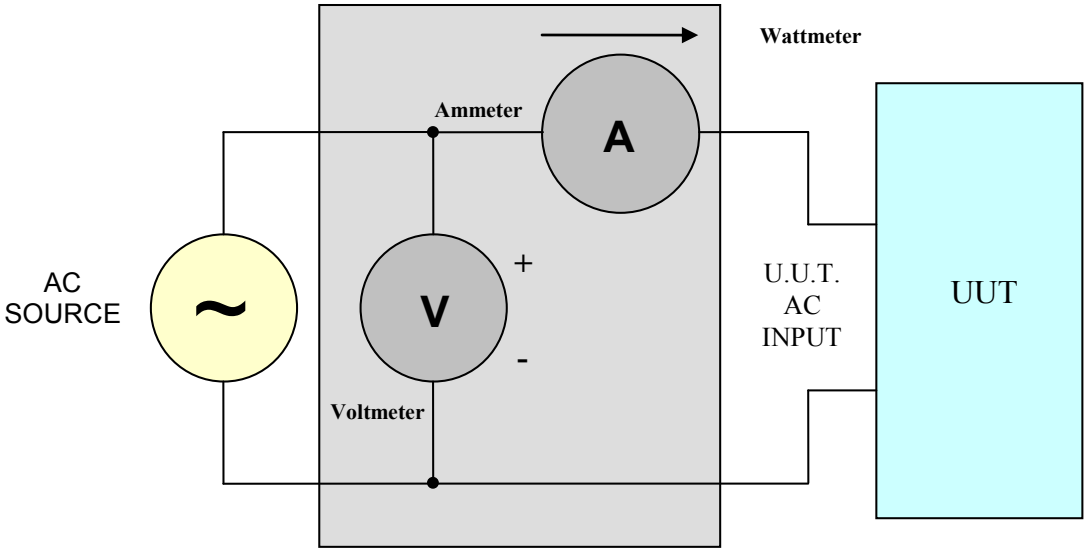
An electronic load is connected to the output of the power converter (UUT), allowing the setting and measurement of the load current of the converter, while the output voltage is measured by a voltmeter. The output power is the product of the load current and output voltage.

The ratio between the output power and the input power measured by the wattmeter is the efficiency of the converter. It is measured under different input and output conditions acting on the AC source and on the electronic load.

With reference to Figure 38. Connections of the UUT to the wattmeter for power measurements, the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

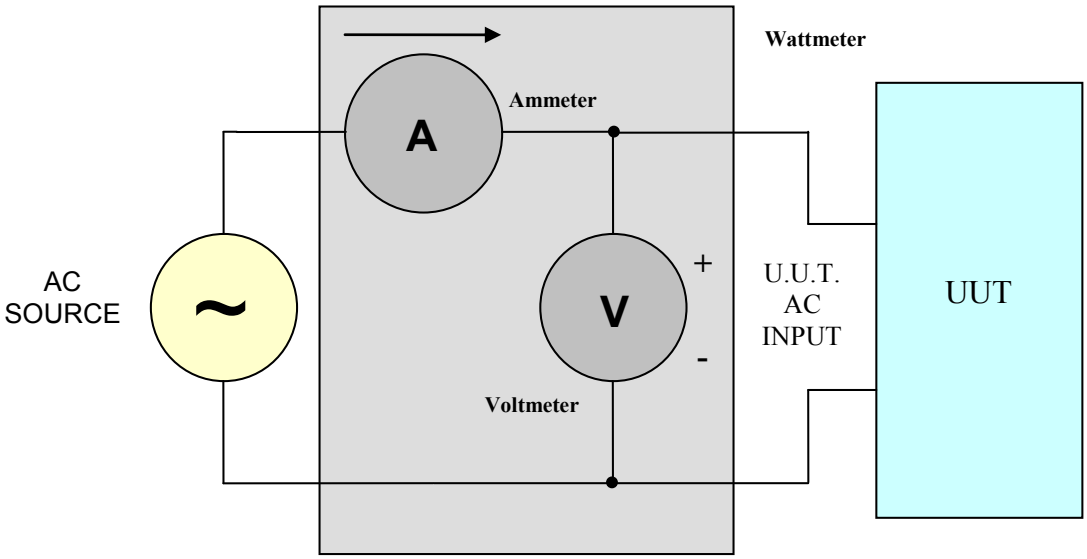
If the switch in Figure 38. Connections of the UUT to the wattmeter for power measurements is in position 1 (see the simplified scheme in Figure 39. Switch in position 1 - setting for standby measurements) this voltage drop causes a measured input voltage higher than the input voltage at the UUT input that obviously affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example, when we are measuring the input power of a UUT in the light-load condition).

Figure 39. **Switch in position 1 - setting for standby measurements**



For high UUT input currents, the voltage drop can be relevant (compared to the UUT real input voltage), so in this case the switch in Figure 38. Connections of the UUT to the wattmeter for power measurements can be set to position 2 (see simplified scheme in Figure 40. Switch in position 2 - setting for efficiency measurements) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 40. **Switch in position 2 - setting for efficiency measurements**



The voltage across the voltmeter causes a leakage current inside the voltmeter itself (that is not ideal). If the switch in Figure 38. Connections of the UUT to the wattmeter for power measurements is in position 2 (see simplified scheme in Figure 40. Switch in position 2 - setting for efficiency measurements), the voltmeter leakage current is measured by the ammeter together with the UUT input current, causing a measurement error. The error is negligible if the UUT input current is much higher than the voltmeter leakage. If the UUT input current is not much higher than the voltmeter leakage current, it is probably better to set the switch in Figure 38. Connections of the UUT to the wattmeter for power measurements to position 1.

If you are not sure which measurement scheme is more suitable, you can try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT shall be operated at 100% of nameplate output current output for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the ac input power shall be monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period.

If ac input power is not stable over a 5-minute period, the average power or accumulated energy shall be measured over time for both ac input and dc output.

Some wattmeter models allow integrating the measured input power over a time interval and then measuring the energy absorbed by the UUT during that time, from which the average input power is calculated.

Revision history

Table 10. **Document revision history**

Date	Version	Changes
02-Nov-2020	1	Initial release.

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