STM32MP13x MPU product line discrete power supply hardware integration

Introduction

This application note applies to the STM32MP13x MPU product line devices, henceforward referred to as STM32MP13x to ease the reading of this document. It is usually powered by the STPMIC1 power management IC companion chip, which is fully featured to supply complete applications

This application note describes an alternative solution to supply power to STM32MP13x MPUs with discrete regulators. Only applications supporting the core chipset are covered (STM32MP13x, DDR, and flash memory).

This document is intended for product architects and designers who require information about hardware integration and settings, and it focuses on:

- Reference design block diagram
- Discrete power supply topologies
- Power up, power down management
- Low power mode and reset management (crash recovery)
- Voltage regulator module (VRM) electrical specification for supplying the STM32MP13x power rail.

1 General information

This document applies to STM32MP13x single-core Arm®-based microprocessors.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Overview

This application note applies to all STM32MP13x devices, which have a large feature set and stringent power-supply requirements.

It focuses on the core chipset supplies (STM32MP13x, DDR, and flash memory) with the following assumptions:

- DC input power source from main power supply: 5.2 V typical (4 V to 5.5 V).
- DDR3L or lpDDR2/3 without bus termination resistors.
- A boot device that can be either a 3.3 V or 1.8 V powered eMMC or a 3.3 V powered NAND or NOR or a SD-card
- 1 x USB-A HS port host and 1x USB-C HS port supporting USB Power Delivery.

The regulator electrical specifications provided in this document are only applicable when the STM32MP13x decoupling scheme (refer to [1]) and layout recommendations are carefully followed.

Power consumption figures provided in this application note are illustrative examples only, and must not be used as a reference. For information regarding power consumption, refer to [7] and the related product datasheet [5].

The STM32MP13x electrical and timing data provided in this application note is for illustration only, and must not be used as a reference. Refer to the relevant STM32MP13x product datasheet.

2.1 Reference documents

Table 1. Reference documents

Document number	Title
STMicroelectronics documents.(1)	
[1]	*Getting started with STM32MP13 Series hardware development (AN5474)*
[2]	*STPMIC1: Highly integrated power management IC for micro processor units (DS12792)*
[3]	*STM32MP13x product lines using low-power modes (AN5565)*
[4]	*STM32MP13xx reference manual (RM0475)*
[5]	*STM32MP135C/F: Arm® Cortex®-A7 up to 1 GHz, LCD-TFT, camera interface, 2×ETH, 2×CAN FD, 2×ADC, 24 timers, audio, crypto and adv. security (DS13483)*
[6]	*STM32MP1 Series lifetime estimates (AN5438)*
[7]	*STM32MP13x product lines system power consumption (AN5787)*
[8]	*DDR memory routing guidelines for STM32MP13x product lines (AN5692)*

1. Refer to www.st.com

3 Glossary

Table 2. Glossary

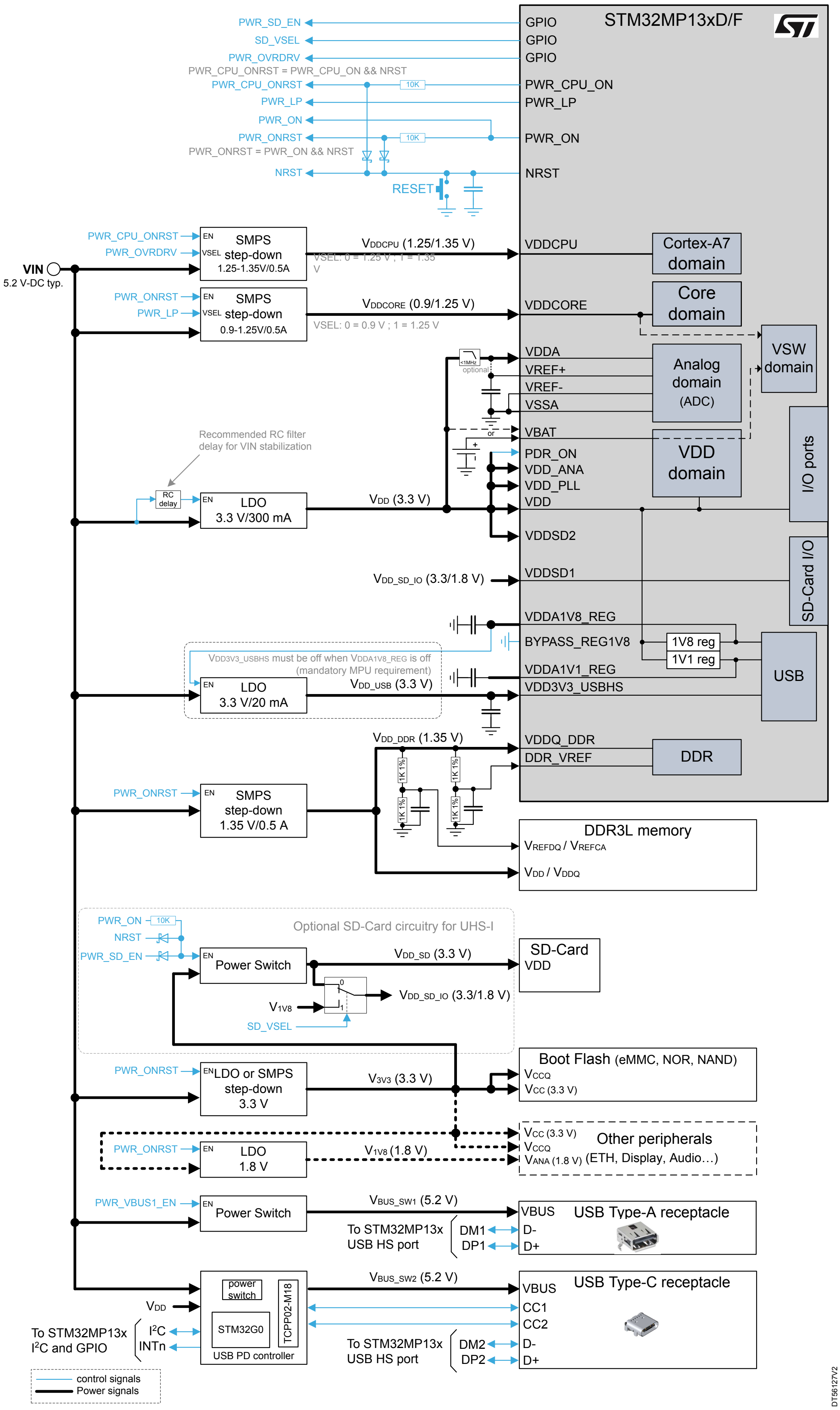
Term	Definition
FSBL	First stage boot loader
HSI	High-speed internal oscillator
IC	Integrated Circuit
LDO	Low drop out. a linear regulator in this document.
MPU	Micro-processor unit. Referring to STM32MP13x devices in this document
PD	Power Delivery
POR	Power-on reset
RC	Discrete resistor-capacitor network
RCC	STM32MP13x reset and clock control
SMPS	Switched-mode power supply.
UHS-I	SD card ultra-high-speed I mode
VRM	Voltage regulator module. In this document, a VRM is either a step-down SMPS or an LDO, including their related discrete components.

4 Discrete power supplies topologies

4.1 STM32MP13xD/F Run overdrive mode with DDR3L, boot flash, SD-card UHS-I, USB-A host, and USB-C PD

The reference design shown in Figure 1 targets an application powered from the main supply adapter composed of an STM32MP13x supporting Run overdrive mode with DDR3L, a boot flash, an SD-Card interface compatible with UHS-I mode, a USB2.0 HS Type-A host port, and a USB2.0 HS Type-C Power Delivery port. The boot flash can be either eMMC, NAND, NOR, or SD card. Other peripherals like Ethernet, audio, and display are also included to illustrate the application. The main peripheral interfaces work with I/O voltage at 3.3 V

Figure 1. STM32MP13x with DDR3L, boot flash, SD card UHS-I, USB-A host, and USB-C PD



Note: The following are not shown in the diagram:
- *MPU decoupling scheme is not shown (refer to [1])*
- *SMPS and LDO regulator product part numbers and discrete components are not shown, but their electrical specifications are detailed in §6 Voltage Regulator Module specification.*
- *VIN source and related protections, such as ESD, EMI filtering, and over-voltage are not shown.*

Note: Power supply options:
- *If SD-card UHS-I mode is not required, the SD-card can be powered from V_{3V3} (hot plug). So, the SD-card power switch ($_{VDD\_SD}$) and power multiplexer ($V_{DD\_SD\_IO}$) can be removed.*
- *If no USB port is required, the V_{DD_USB} LDO can be removed*
- *The V_{1V8} LDO is included to illustrate the analog peripheral supply source. The V_{1V8} voltage is also required to supply MPU's SD-card I/Os (VDDSD1) when SD-card runs in UHS-I mode.*

4.1.1 Input voltage

These application examples are powered from a 5.2 V typical DC voltage source (VIN).

This voltage is compatible with the power supply USB host ports range (from 4.75V to 5.5V at the USB receptacle). If a USB host port is not required, then VIN typical voltage can be extended with a larger range (such as 4.0 V to 5.5 V) compatible with application regulators:
- Linear regulators (LDOs)
- Non-isolated step-down SMPS

Alternatively, this application might be powered by a higher input voltage, such as 12 V. In that case, discrete regulators with suitable rated input voltage are used. For input voltages higher than 12 V - typically industrial applications - use of pre-regulation topology is recommended. For example, the use of a 24-to-5 V step-down SMPS for pre-regulation to generate VIN, followed by the topology defined in this example. Pre-regulation is recommended to avoid working the step-down SMPS with a very low-duty cycle.

The minimum VIN voltage must be higher than the highest voltage used in the application. In this application, 3.3 V is the highest voltage required by the application (to supply $V_{DD,}$ V_{3V3}, and V_{DD_USB}) for applications without USB host port (else, 5.2 V for application with USB host port). Considering the ideal regulator (no dropout) and ideal power source, the minimum VIN might be 3.3 V. In real conditions, a reasonable 400 mV dropout for a 3.3 V regulator (working at full load) and a 300 mV drop on the VIN path (including DC and AC drop + margin) requires a minimum VIN voltage of about 4 V.

The maximum VIN voltage is limited by the regulator powered by VIN having the lowest maximum-rated input voltage. In this application, it is assumed to be 5.5 V.

4.1.2 Power distribution and regulators topology recommendation

LDO or SMPS regulator topology selection is a trade-off between simplicity of integration versus power-efficiency performance:
- LDO: simplicity of integration, low noise; but poor power efficiency (thermal heating)
- SMPS: good power efficiency (lower thermal heating than LDO); complex to integrate, higher noise than LDO (switching activity).

For an application powered from a DC source, typically powered from AC to DC wall adaptor, power efficiency is less critical than in battery applications. Nevertheless, thermal heating remains an important criterion and must be minimized as much as possible. This is especially so when the application runs the most power-consuming use case.

Reciprocally, an application in Standby mode must have regulators with a low quiescent current for those kept on; and regulators with low leakage current for those turned off.

Regulator topologies must be selected accordingly:

VDD power domain (3.3 V):

V_{DD} is the reference design main I/O voltage domain used by the MPU and peripherals.

For the V_{DD} power domain, the LDO topology is a good compromise between power losses, voltage noise, and cost:
- The V_{DD} / VIN voltage ratio is 0.66 (3.3 V / 5 V) LDO power efficiency is approximately 66%, quasi-constant.

- Average current consumption is low, even for complex use cases. It is typically below an average worst-case current of 100 mA (50 mA assumed) and never exceeds 200 mA (assuming a 300 mA peak very worst case to allow some margin).
- Current consumption in Stop and Standby modes is very low: around 10 and 3.65 µA respectively (refer to [5] for details and conditions)

With LDO topology power efficiency is ~66% (~VDD/VIN ratio) and ~90% with an SMPS Step-down converter. Power losses are 85 mW with an LDO and 18 mW with an SMPS converter (assuming 50 mA power consumption). For both, it is negligible in terms of thermal heating compared to other power domains.

In Stop mode, power losses are equivalent between an LDO and a step-down SMPS, because common step-down SMPS converter power efficiency decrease under light load.

In Standby mode, power losses are higher with an SMPS compared to an LDO. An SMPS usually has a higher quiescent current than an LDO, and an LDO has no switching losses.

VDDA and VREF power domains (3.3 V):

The V_{DDA} pin supplies the ADC and the voltage reference buffer (VREFBUF) to generate the V_{REF+} reference voltage of the ADC.

The ADC performance is directly impacted by the noise level from the V_{REF+} source, but also by the VDDA source noise level (due to the VDDA power supply rejection ratio).

If VDDA is powered from the VDD power source, a low pass filter with low DC impedance might be inserted in between the VDD power source and VDDA depending on the required ADC performance.

V_{REF+} must only be connected to the VDD power source if limited ADC performance is expected.

V_{DDCORE} power domain (0.9 V - 1.25 V):

V_{DDCORE} is the main MPU digital power domain.

For the V_{DDCORE} power domain, step-down SMPS topology is recommended for power efficiency as this is one of the highest power-consumption domains in the application.

For V_{DDCORE}, LDO topology is not recommended due to the ratio between V_{DDCORE} and VIN of about 0.25 (1.25 V / 5 V). With an LDO, power efficiency might be as low as 25%, meaning significantly more energy is consumed by the LDO converter than the energy consumed by the MPU itself.

V_{DDCORE} regulator needs to manage two voltage settings for supporting LPLV-Stop2 and Run modes, respectively at 0.9 and 1.25 V.

V_{DDCPU} power domain (1.25 V – 1.35 V):

V_{DDCPU} is the MPU Arm® Cortex®-A7 CPU digital power domain.

For the V_{DDCPU} power domain, step-down SMPS topology is recommended for the same reason as for V_{DDCORE}.

The STM32MP13xD and STM32MP13xF devices have an enhanced consumer mission profile (refer to [6]). This profile allows the Arm® Cortex®-A7 CPU clock frequency to run up to 1 GHz (refer to [5] for details and limitations).

The V_{DDCPU} supply voltage must be increased to the Run overdrive mode value when the CPU frequency (Fmpuss_ck) operates above 650 MHz (refer to [5]). When it operates in Run mode at 650 MHz or below, the V_{DDCPU} supply voltage must be set back to the nominal Run mode value. Refer to Section 5.3 STM32MP15xD and STM32MP15xF Run overdrive mode management for a detailed procedure to switch between Run mode and Run overdrive mode.

Consequently, the V_{DDCPU}'s Voltage Regulator Module needs to manage two voltage settings for switching between Run mode and Run overdrive mode, respectively 1.25 and 1.35 V.

VDD_DDR (1.35 V), VREF_DDR (0.675 V) power domains:

V_{DD_DDR} is dedicated to DDR3L volatile memory IC power supply (VDD and VDDQ) and the MPU DDR interface voltage domain (VDDQ_DDR)

For the V_{DD_DDR} power domain, step-down SMPS topology is recommended for the same reason as for V_{DDCORE}.

V_{REF_DDR} is dedicated to DDR3L volatile memory IC reference voltage (VREFQ/VREFCA) and MPU DDR reference voltage (DDR_VREF) at $V_{DD\_DDR}/2$.

For the V_{REF_DDR} power domain, a voltage divider topology is recommended. It is composed of two resistors having the same value (example: 1 kΩ +/- 1%) referenced from V_{DD_DDR} to generate the V_{REF_DDR} at V_{DD_DDR} / 2.

There is one voltage divider for the DDR3L volatile memory IC power supply (VREFQ/VREFCA) and one voltage divider for the MPU DDR interface voltage domain (DDR_VREF).

Note: In the reference design in Figure 1, there is no VTT_DDR (Fly-by topology termination) since usually only one memory chip is needed for 16-bit DDR3 configuration.

VDD_USB power domains (3.3 V):

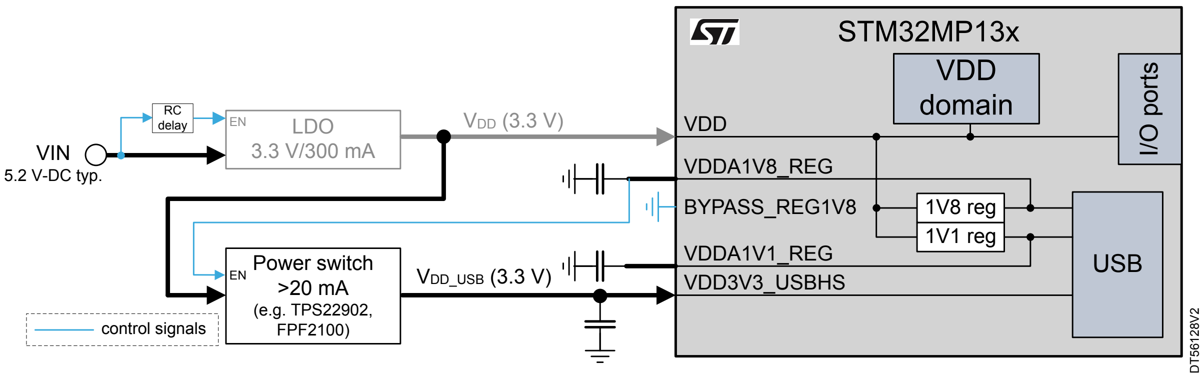
VDD_USB is dedicated to supplying power to the MPU USB PHY (VDD3V3_USBHS). The VDD3V3_USBHS power consumption is less than 11.5 mA typical (20 mA is assumed to allow some margin).

VDD3V3_USBHS must not be present unless VDDA1V8_REG is present, otherwise permanent MPU damage might occur (refer to *[5]* for details). VDD3V3_USBHS cannot be connected directly to VDD as VDD is always present before VDDA1V8_REG.

To accommodate this constraint, VDD3V3_USBHS must be enabled by VDDA1V8_REG. V_{DD_USB} is enabled when VDD1V8_REG is enabled, hence by default at power-on. Different power supply options are possible:

- Dedicated LDO (recommended): refer to Figure 1
- Integrated power switch/load switch: refer to Figure 2
- Discrete power switch: refer to Figure 3

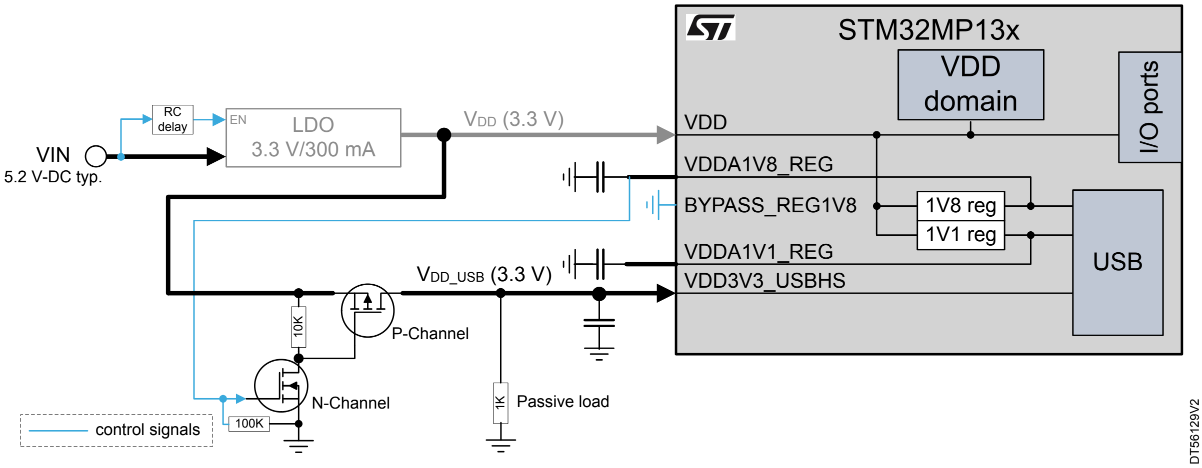
Figure 2. Supply VDD3V3_USBHS with integrated power switch



The power switch (load switch) main electrical criteria:

- The ON-resistance must be low enough to guarantee that V_{DD_USB} never drops below 3.07 V. Typically below 3.25Ω if VDD has +/- 5% tolerance Ron < ((3.3 V - 5%) – 3.07 V) / 20 mA = 3.25 Ω
- EN_V_{IH} min threshold (active high) must be below 1.65 V (VDDA1V8_REG min) to ensure that the power switch turns on in all conditions.
- An integrated output discharge resistor is recommended to discharge the V_{DD_USB} decoupling capacitor when the power switch is disabled

Figure 3. **Supply VDD3V3_USBHS with a discrete power switch**



This discrete power switch is composed of one P-Channel power MOSFET and one N-Channel MOSFET. The P-Channel acts as a power switch to drain current from V_{DD} to V_{DD_USB} to supply VDD3V3_USBHS. The P-Channel gate is driven by the N-Channel MOSFET which acts as an open drain to reverse P-Channel polarity. The N-Channel gate is driven by VDDA1V8_REG voltage. The 1KOhms passive load is added to discharge decoupling capacitors on VDD3V3_USBHS; continuously consuming 3.3 mA when V_{DD_USB} is enabled.

Discrete power switch main electrical characteristics:

- P-Channel MOSFET:
- V_{DSS} and V_{GSS} > -3.3 V
- I_D min: -20 mA
- I_D peak >> -20 mA (peak current when charging VDD3V3_USBHS decoupling capacitor)
- $R_{DS(ON)}$ < 3.25 Ω at V_{GS} = -3.3 V
  - N-Channel MOSFET:
- V_{DSS} > 3.3 V
- V_{GSS} > 1.8 V
- I_D min: 10 mA
- $R_{DS(ON)}$ < 100 Ω at V_{GS} = 1.8 V

V_{3V3} and V_{1V8} power domains:

For V_{D3V3} and V_{1V8} power domains, voltage and regulator topology depend on the final application. In the application illustrated in Figure 1, it is assumed that all peripherals can be supplied from a 3.3 V voltage source. V_{1V8} is an optional supply source to supply specific peripherals such as analog audio codec. In the application shown in Figure 1, V_{1V8} is specifically used to supply the SD-card MPU GPIOs (VDDSD1) when the SD-card device runs in UHS-I mode.

SD card power domains (V_{DD_SD} and $V_{DD\_SD\_IO}$):

In the application illustrated in Figure 1, the SD-card interface supports UHS-I mode.

The SD-card device is powered by V_{DD_SD} voltage from the V_{3V3} power domain via a power switch allowing to power on/off the SD-card device at runtime. The power switch is required to perform a power cycle on the SD-card device specifically to reset the SD-card device from UHS-I mode to Default speed mode. It is typically required when the MPU's SD card software driver requires the restart of the SD card (by asserting PWR_SD_EN signal low to high) or during a system reset (when NRST is asserted).

The $V_{DD\_SD\_IO}$ power domain is dedicated to supplying the MPU VDDSD1 I/Os domain. VDD_SD_IO is powered from a power multiplexor allowing $V_{DD\_SD\_IO}$ to switch dynamically from V_{DD_SD} voltage (3.3 V) to V_{1V8} (1.8 V).

- $V_{DD\_SD\_IO}$ = 3.3 V when the SD card operates in Default speed mode (reset state)
- $V_{DD\_SD\_IO}$ = 1.8 V when the SD card operates in UHS-I mode

The signal SD_VSEL illustrated in Figure 1, is controlled from an MPU GPIO by the MPU SD card software driver to control the power multiplexor for switching $V_{DD\_SD\_IO}$ from 3.3 to 1.8 V when the SD card is going from the Default speed mode to UHS-I mode:

When the UHS-I mode is requested, the software sends a command to the SD-card device to internally change its GPIOs to 1.8 V. Then the software changes the $V_{DD\_SD\_IO}$ voltage from 3.3 V to 1.8 V by setting the V_SEL signal to HIGH. The software can then change the SDMMC1 GPIO to high-drive HSLV mode by setting the SYSCFG_HSLVENxR register to 0x1018. In SYSCFG_HSLVENxR, x=4 for SDMMC1 (or x=5 if SDMMC2 is used).

Caution: SYSCFG_HSLVENxR must not be set to HSLV before $V_{DD\_SD\_IO}$ voltage is set to 1.8 V or the device might be damaged.

Note: A discrete pull-down resistor is recommended on the SD_VSEL signal to guarantee VDD_SD_IO = 3.3 V at reset state

If the SD card is powered off by software (PWR_SD_EN = ‘0’), the software must first reset SYSCFG_HSLVENxR before setting $V_{DD\_SD\_IO}$ to 3.3 V (V_SEL LOW). Then, the software can power on the V_{DD_SD} voltage (PWR_SD_EN = ‘1’)

In case of system reset (NRST asserted), the SYSCFG_HSLVENxR HSLV content is automatically reset, and SD_VSEL and PWR_SD_EN GPIOs go in high impedance. When NRST is released, the SD-Card is automatically powered on (the EN signal of the SD-card power switch goes HIGH) and VDD_SD_IO is automatically set to 3.3 V (SD_VSEL is pulled down by a discrete pull-down resistor).

Consequently, the application illustrated in Figure 1 allows the MPU to boot over the SD-card interface or reboot safely after a system reset (NRST assertion)

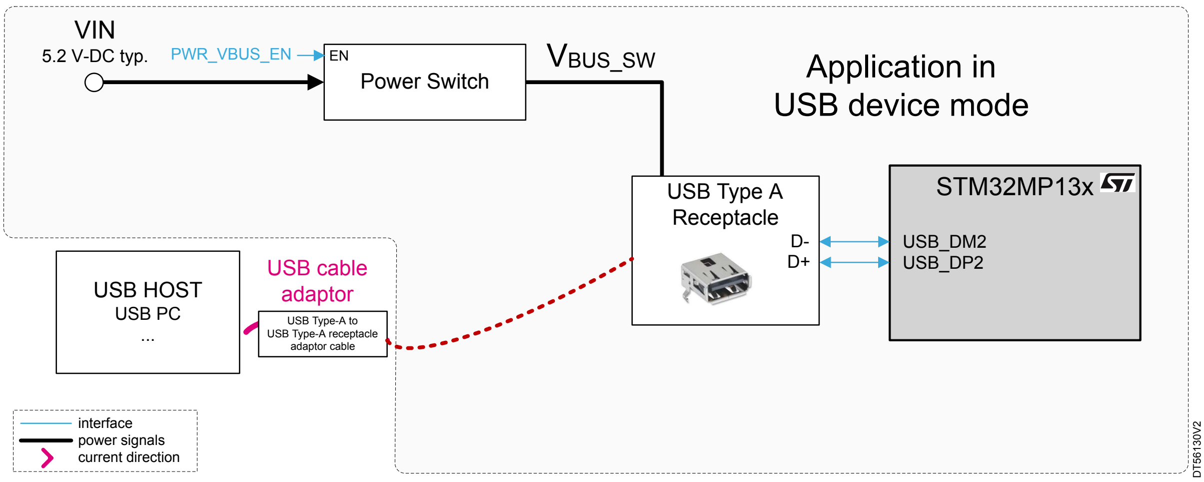
V_{BUS_SW1} and V_{BUS_SW2} power domains:

In the application illustrated in Figure 1, the V_{BUS_SW1} dedicates the power domains to power supply the Type-A USB high-speed host port, and the V_{BUS_SW2} dedicates the power domain to power supply the USB Type-C® high-speed Dual Role Data, Dual Role Power port.

Both V_{BUS_SW1} and V_{BUS_SW2} are powered from VIN via independent power switches at 5.2 V. The 5.2 V voltage is defined to be compliant with the USB V_{BUS} specification range (from 4.75 to 5.5 V at the USB connector level) at full load including losses through power switches.

Flashing through USB with Type-A connector

Figure 4. Flashing through USB with Type-A connector



For applications that have only a Type-A receptacle USB port, it is still possible to perform serial boot over the USB on the MPU application. This can be done in USB device mode.

This specific Boot mode is different from the classical one that uses the USB Type-C or the USB Type-B receptacle. To support this specific Boot mode, there are two requirements:

- A USB Type-A receptacle is used in USB device mode
- A dedicated non-USB compliant Type-A to Type-A plug cable is required.

The host PC USB Type-A receptacle must be connected on one side of the dedicated cable while the other side is connected to the MPU device USB Type-A receptacle.

Note: If V_{BUS} is interconnected inside the non-USB compliant Type-A to Type-A plug cable, then V_{BUS_SW} is powered from the USB host PC port. As most power switches do not have reverse voltage protection, the current passes through the power switch in the reverse direction making VIN powered from V_{BUS_SW}.

STM32CubeProgrammer is used on the host PC to flash the Linux distribution on the target MPU.

The MPU must be ready for USB/UART boot:

- Either the flash memory is empty: consequently, the MPU switches automatically in USB/UART boot mode
- Or boot pins must be set to force USB/UART boot mode (BOOT[2:0]='000' or '110')

In the above use case, the V_{BUS_SW} signal is not required to be connected to the MPU hence the boot ROM does not probe V_{BUS} to detect a host PC connection.

Flashing operation:

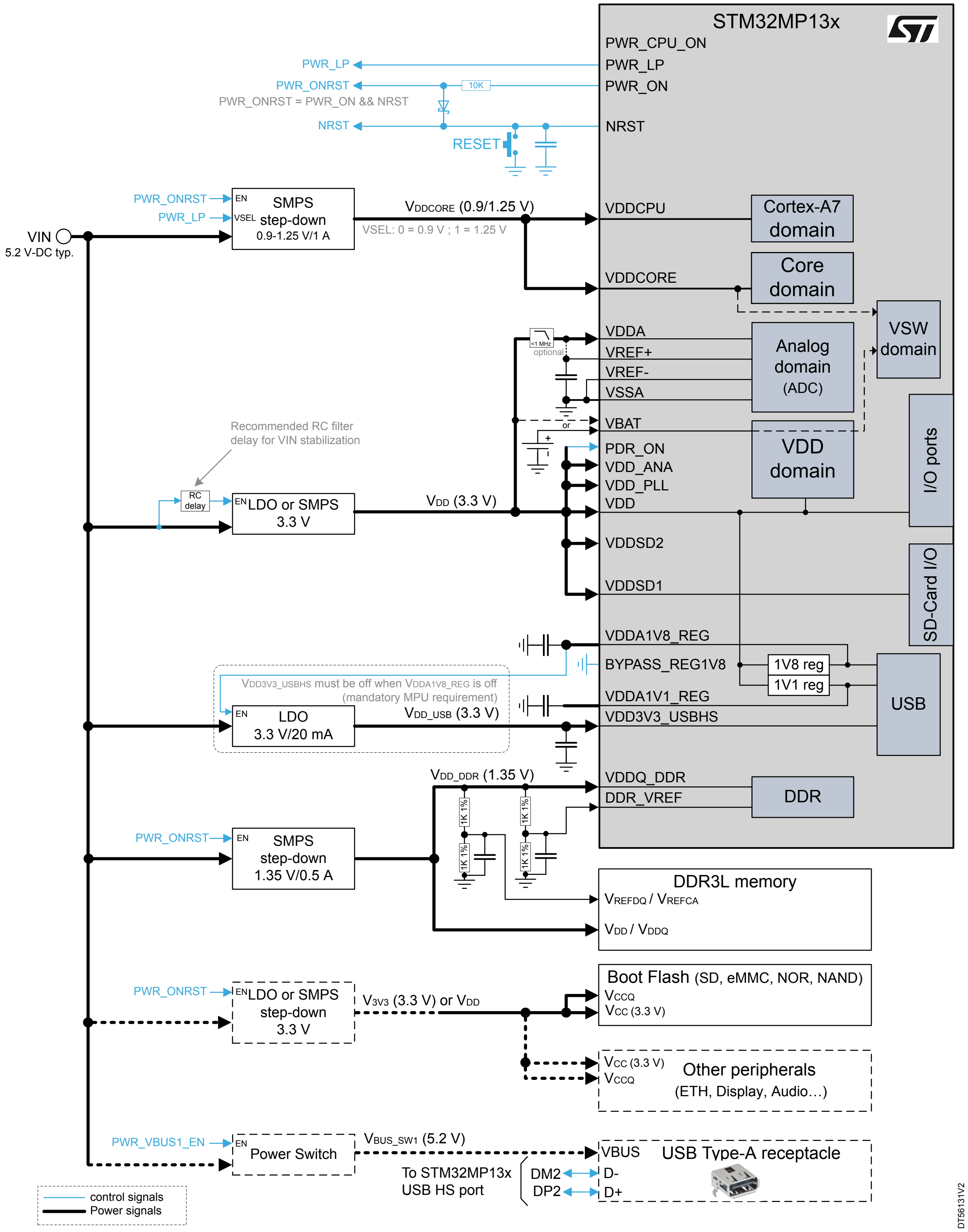
1. Initial conditions:
   – PC ready to enumerate USB DFU
   – Boot pin set to USB/UART mode if flash is not empty
   – The board power supply is OFF
   – USB cable connection between PC host and MPU board
2. Power supply is switched ON (or reset of the STM32MP13x MPU is asserted)
3. PC enumerates USB DFU
4. Flashing starts with STM32Cube Programmer

Once flashing is complete, the USB cable between the host PC and the MPU device must be disconnected. This must be done before booting the system in application mode from flash because the application might enable the USB host port voltage (V_{BUS_SW}) by setting PWR_VBUS_EN signal.

4.2 STM32MP13x low-cost with DDR3L, boot flash, and USB-A host

The reference design shown in Figure 5 targets a low-cost application powered from the main supply adapter composed of an STM32MP13x where V_{DDCORE} and V_{DDCPU} are merged, a DDR3L, a boot flash, an SD-Card, and a USB2.0 HS host port. The boot flash can be either eMMC, NAND, NOR, or SD card. Other peripherals like Ethernet, audio, and display are also included to illustrate the application. The main peripheral interfaces work with I/O voltage at 3.3 V.

Figure 5. Low-cost version V_{DDCPU} merged with V_{DDCORE} using single step-down SMPS



Note: The following are not shown in the diagram:

- *MPU decoupling scheme is not shown (refer to [1]).*
- *SMPS and LDO regulator product part numbers and discrete components are not shown, but their electrical specifications are detailed in Section 6 Voltage regulator module specification.*
- *VIN source and related protections, such as ESD, EMI filtering, and over-voltage are not shown.*

Note: In this configuration with V_{DDCPU} and V_{DDCORE} merged, LPLV-Stop2, and Run overdrive mode is not possible

Note: Power supply options:

- *If no USB port is required, the V_{DD_USB} LDO can be removed*
- *If Standby mode is not required, the V_{3V3} power domain (peripherals supply) can be merged with the V_{DD} power domain to allow removing the V_{3V3}'s VRM. Accordingly, boot flash and peripherals supplied from the merged V_{DD} / V_{3V3} power domains must be reset from a hardware signal (NRST), as the VDD power domain is an always-on supply.*

4.2.1 Input voltage

Refer to Section 4.1.1 Input voltage.

4.2.2 Power distribution and regulators topology recommendation

Similar to Section 4.1.2 Power distribution and regulators topology recommendation with following differences:

V_{DDCORE} power domain (0.9 V - 1.25 V):

In the application illustrated in Figure 5, the V_{DDCORE} power domain supplies both MPU V_{DDCORE} and V_{DDCPU}. Those are merged to save a step-down SMPS compared to the application illustrated in Figure 1.

In this application:

- The V_{DDCPU} supply is limited to the Run mode nominal voltage and consequently, the CPU frequency is limited to 650 MHz
- The LPLV-Stop2 is not supported
- The LPLV-Stop is supported

For the V_{DDCORE} power domain, step-down SMPS topology is recommended for power efficiency as this is one of the highest power-consumption domains in the application.

For V_{DDCORE}, LDO topology is not recommended due to the ratio between V_{DDCORE} and VIN of about 0.25 (1.25 V / 5 V). With an LDO, power efficiency might be as low as 25%, meaning significantly more energy is consumed by the LDO converter than the energy consumed by the MPU itself.

V_{DDCORE} regulator needs to manage two voltage settings for supporting LPLV-Stop and Run nominal modes, respectively at 0.9 and 1.25 V.

VDD_SD power domains (3.3 V):

In the application illustrated in Figure 5, the SD card is powered directly from the V_{3V3} power domain (hot plug) compared to the application illustrated in Figure 1. Consequently, the SD card can operate in Default speed mode only.

VDD and V3V3 power domains (3.3 V):

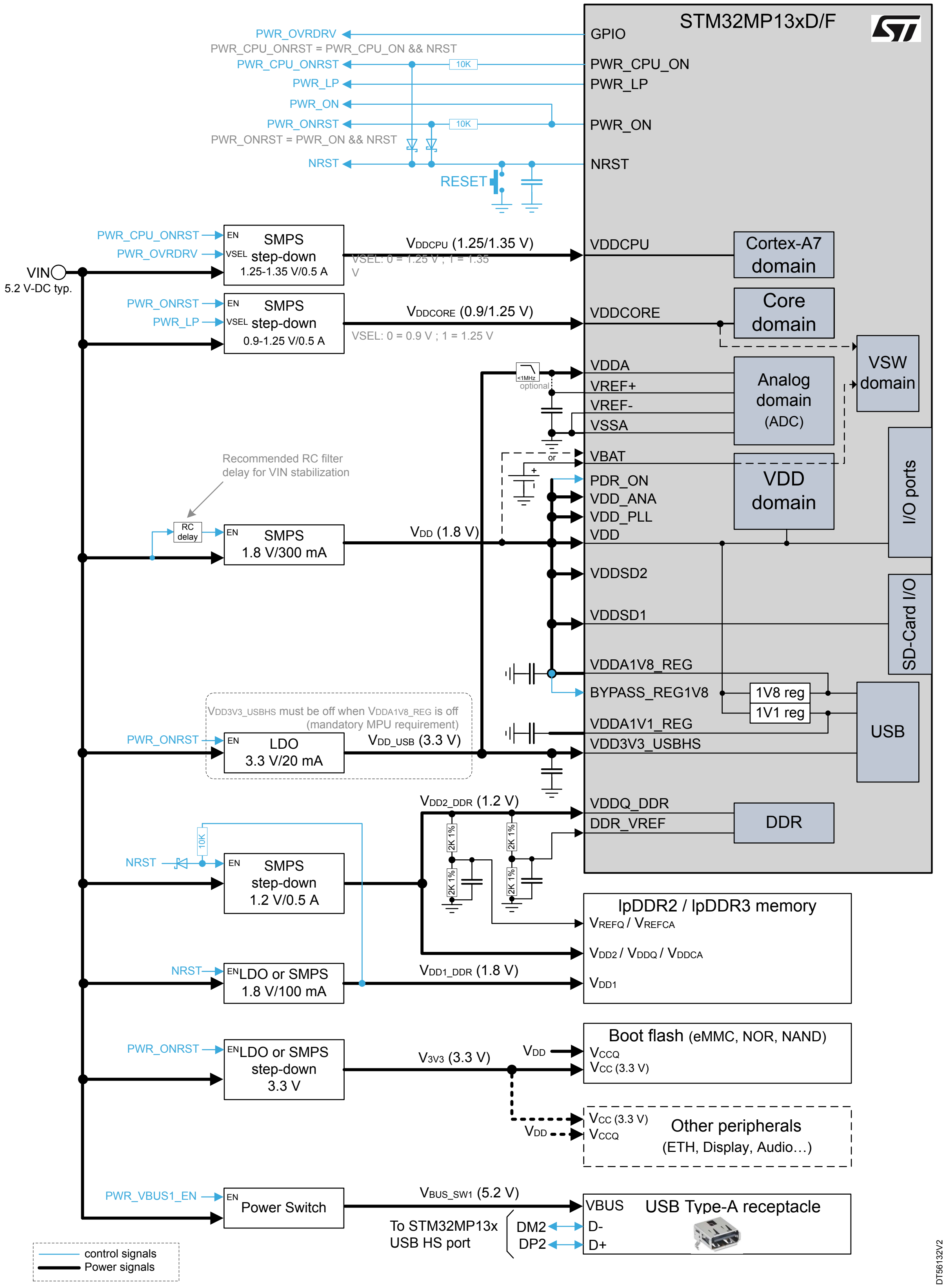
If very low power mode is not required in the application (typically the Standby mode), then V_{DD} and V_{3V3} can be merged to save one regulator. In that case, it is recommended to use a step-down SMPS to supply both V_{DD} and V_{3V3} power domains; making all peripherals (including boot flash) always powered.

In that case, it is required that all peripherals powered from this always-supply can restart/reboot in case of a system reset (NRST asserted). Accordingly, special attention is required for the boot flash peripheral.

4.3 STM32MP13xD/F Run overdrive mode with lpDDR2/3, boot flash, USB-A host, and I/Os voltage at 1.8 V

The reference design in Figure 6 targets an application powered by the main supply adapter composed of an STM32MP13x supporting Run overdrive mode with lpDDR2/3, a boot flash, and a USB2.0 HS Type-A host port. The boot flash can be either eMMC, NAND, NOR, or SD card. Other peripherals like Ethernet, audio, and display are also included to illustrate the application. The main peripheral interfaces work with an I/O voltage of 1.8 V.

Figure 6. STM32MP13x with lpDDR2/3, boot flash, and I/Os voltage at 1.8 V



Note: The following are not shown in the diagram:

- *MPU decoupling scheme is not shown (refer to [1])*
- *SMPS and LDO regulator product part numbers and discrete components are not shown, but their electrical specifications are detailed in §6 Voltage Regulator Module specification.*
- *VIN source and related protections, such as ESD, EMI filtering, and over-voltage are not shown.*

4.3.1 Input voltage

Refer to Section 4.1.1 Input voltage.

4.3.2 Regulators topology recommendation: LDO or SMPS

Similar to Section 4.1.2 Power distribution and regulators topology recommendation with following differences:

VDD power domain:

For the VDD power domain, step-down SMPS topology is recommended for power-efficiency reasons.

Nevertheless, LDO topology might be acceptable due to the low power consumption in this supply domain: With the LDO topology, power efficiency is approximately 36% (~VDD / VIN ratio) and it is about 90% with an SMPS step-down converter. Power losses are 160 mW with LDO and 18 mW with an SMPS converter respectively (assuming 50 mA power consumption). Depending on the application heat-dissipation capacity, if 60 mW in losses is acceptable, then an LDO can be used.

VDD_USB power domains:

VDD_USB is dedicated to supplying power to the MPU USB PHY (VDD3V3_USBHS). It must be powered from 3.07 to 3.6 V.

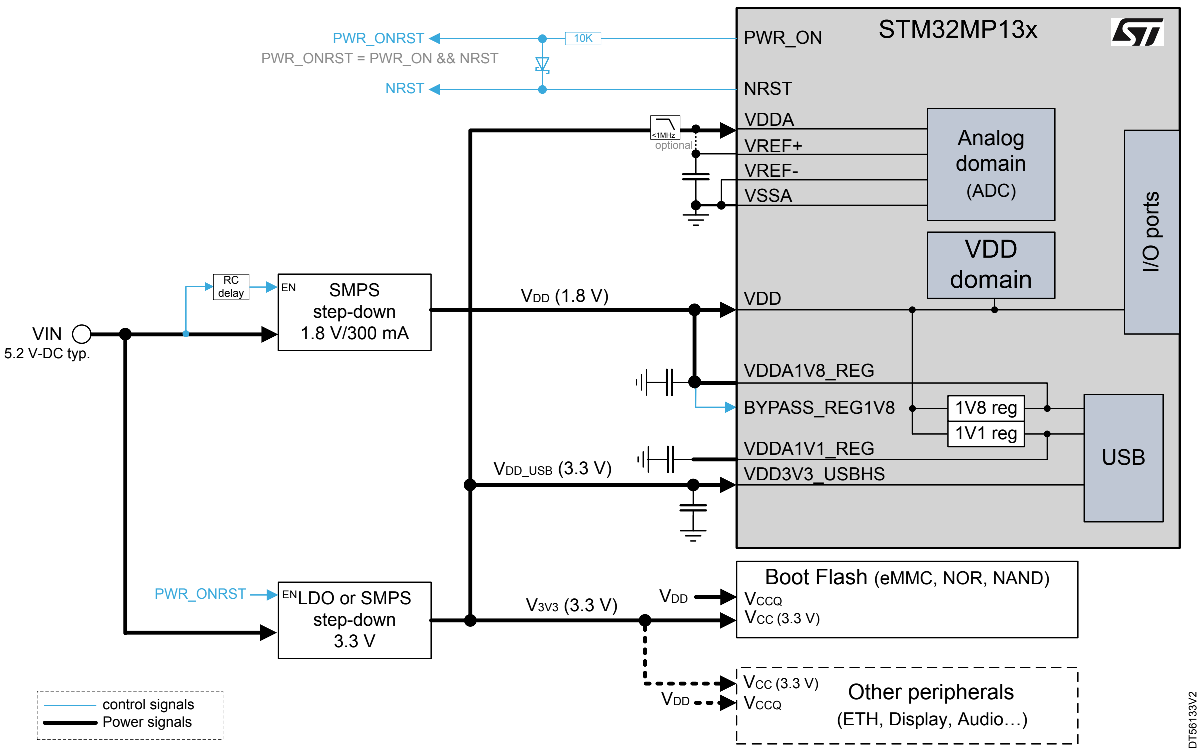
VDD3V3_USBHS power consumption is less than 11.5 mA typical (20 mA is assumed to allow some margin).

VDD3V3_USBHS must not be present unless VDDA1V8_REG is present, otherwise permanent MPU damage might occur (refer to *[5]* for details). VDD3V3_USBHS cannot be connected directly to VDD as VDD is always present before VDDA1V8_REG.

To accommodate this constraint, VDD3V3_USBHS must be synchronized with the PWR_ON or PWR_ONRST signal, as VDD is connected to VDDA1V8_REG and VDD rises first in the application (refer to Figure 6). Two power supply options are possible:

- Dedicated LDO (recommended): refer to Figure 6
- Reuse of the regulator supplying peripheral (V_{D3V3}): refer to Figure 7.

Figure 7. Supply VDD3V3_USBHS from V_{3V3}



The V_{3V3} power source can be used to supply VDD3V3_USBHS if the following conditions are respected:

- V_{3V3} voltage must be in VDD3V3_USBHS voltage tolerance (3.07 to 3.6 V).
- V_{3V3} (VDD3V3_USBHS) must not be present unless VDD (VDDA1V8_REG) is present.

So if the V_{3V3} regulator has the same voltage and is controlled through PWR_ONRST as in Figure 7, the two above constraints are fulfilled.

VDDA and VREF power domains:

The V_{DDA} pin supplies the ADC and the voltage reference buffer (VREFBUF) to generate the V_{REF+} reference voltage of the ADC.
The ADC performance is directly impacted by the noise level from the V_{REF+} source, but also by the VDDA source noise level (due to the VDDA power supply rejection ratio).
If the ADC is used in the application with reference voltage V_{REF+} higher than 2 V, then the V_{3V3} power source might be used to supply VDDA. A low pass filter with low DC impedance might be inserted in between the V_{3V3} power source and VDDA depending on the required ADC performance.
V_{REF+} might be connected to the V_{3V3} power source only if limited ADC performance is expected.

VDD1_DDR (1.8 V), VDD2_DDR (1.2 V) power domains:

V_{DD1_DDR} is dedicated to lpDDR2 or lpDDR3 volatile memory IC power supply (V_{DD1}).

V_{DD2_DDR} is dedicated to lpDDR2 or lpDDR3 volatile memory IC power supply (V_{DD2}, V_{DDQ}, and V_{DDCA}) and for the MPU DDR interface voltage domain (VDDQ_DDR)

V_{REF_DDR} is dedicated to lpDDR2 or lpDDR3 volatile memory IC reference voltage (V_{REFQ}/V_{REFCA}) and MPU DDR reference voltage (DDR_VREF) at $V_{DD2\_DDR}/2$.

For the V_{DD1_DDR} power domain, step-down SMPS topology is recommended. Nevertheless, LDO topology might be acceptable due to the low power consumption on this supply domain (less than 5 mA on average and ~30 mA max): With the LDO topology, power efficiency is approximately 36% (~V_{DD1_DDR} / VIN ratio) and it is about 90% with an SMPS step-down converter. Power losses are 16 mW with LDO and 1 mW with an SMPS converter respectively (assuming 5 mA power consumption). Depending on the application, if 16 mW in losses is acceptable, then an LDO can be used.

For the V_{DD2_DDR} power domain, step-down SMPS topology is recommended as with LDO topology, the power efficiency might be approximately 24% (~V_{DD2_DDR} / VIN ratio)

For the V_{REF_DDR} power domain, a voltage divider topology can be used. It is composed of two resistors having the same value (example: 2 KΩ or 2.2 KΩ +/-1%) referenced from V_{DD2_DDR} to generate the V_{REF_DDR} at V_{DD2_DDR} / 2. there is one voltage divider for the lpDDR2/3 volatile memory IC power supply (V_{REFQ}/V_{REFCA}) and one voltage divider for the MPU DDR interface voltage domain (DDR_VREF).

Caution: lpDDR2 and lpDDR3 have power-up and power-down sequences that must be followed. There are defined in JEDEC standard JESD209-2B and JESD209-3C respectively for lpDDR2 and lpDDR3.

According to Figure 6:

- $V_{DD1\_DDR} = V_{DD1}$
- $V_{DD2\_DDR} = V_{DD2} = V_{DDQ} = V_{DDCA}$
- $V_{REFQ} = V_{REFCA} = V_{DD2\_DDR} / 2$

lpDDR2/3 power-up constraints defined in JEDEC standards can be simplified as:

- Once V_{DD1_DDR} or V_{DD2_DDR} > 300 mV
- V_{DD1_DDR} must be greater than V_{DD2_DDR} - 200 mV

lpDDR2/3 power-down constraints defined in JEDEC standards can be simplified as:

- Once V_{DDx_min} > V_{DD1_DDR} or V_{DD2_DDR} > 300 mV
- V_{DD1_DDR} must be greater than V_{DD2_DDR} - 200 mV

Note: VDDx_min is the VDD1 minimum value or VDD2 minimum value specified in JEDEC.

The circuitry proposed in Figure 6 allows the control of the V_{DD1_DDR} and V_{DD2_DDR} regulators to fulfill the above electrical constraints:

<u>lpDDR2/3 power-up sequence:</u>

- While the NRST signal is asserted, both V_{DD1_DDR} and V_{DD2_DDR} regulators are off
- Once the NRST signal is released, the V_{DD1_DDR} regulator starts (V_{DD2_DDR} regulator keeps disabled)
- Once the V_{DD1_DDR} regulator reaches a defined output voltage (such as 1.6 V which is considered as enable threshold of the V_{DD2_DDR} regulator EN pin) V_{DD2_DDR} regulator starts
- V_{DD2_DDR} regulator output voltage rises with $V_{REFQ} = V_{DD2\_DDR} / 2$ at anytime

<u>lpDDR2/3 power-down sequence:</u>

- While the NRST signal is released, both V_{DD1_DDR} and V_{DD2_DDR} regulators are on
- Once the NRST signal is asserted or VIN is dropping, the V_{DD1_DDR} regulator stops, and the V_{DD1_DDR} output voltage is discharged or V_{DD1_DDR} output voltage follows VIN (minus the regulator dropout)
- Once the V_{DD1_DDR} regulator drops below a defined output voltage (such as 1.4 V considering 200 mV hysteresis on V_{DD2_DDR} regulator EN pin) V_{DD2_DDR} regulator is stopped
- V_{DD2_DDR} regulator output voltage drops with $V_{REFQ} = V_{DD2\_DDR} / 2$ at anytime

Note: V_{DD1_DDR} regulator and V_{DD2_DDR} regulator must have built-in discharge circuitry. It is required that the V_{DD2_DDR} regulator has faster discharge circuitry than the V_{DD1_DDR} regulator to fulfill power-down electrical constraints.

5 Power management

The following power modes are reviewed in the following sections:

- Operating modes
- Application power-up and power-down modes
- Low-power management mode
- User reset and crash recovery management
- Software management examples

5.1 Operating modes

The application can switch to different operating modes depending on the system's activity. The operating modes are managed by the MPU. The operating modes control the power management and the clock distribution (refer to details in [3]).

The three MPU output pins, PWR_ON, PWR_CPU_ON, and PWR_LP, are automatically controlled depending on the operating mode. They are used to control the application regulators:

- PWR_ON supply request signal (active high): Enables V_{DDCORE} and the application peripherals power supplies. It is active in Run, Stop, LPLV-Stop, and LPLV-Stop2 modes. It is inactive in Standby mode (and implicitly in VBAT and power-off mode when VDD is not present).
- PWR_CPU_ON supply request signal (active high): Enables V_{DDCPU}. It is active in Run, Stop, and LPLV-Stop modes. It is inactive in LPLV-Stop2 and Standby modes.
- PWR_LP low-power mode request signal (active low): It is used to request a regulator or a peripheral to enter a low-power state. It is active in LPLV-Stop, LPLV-Stop2, and Standby modes. It is inactive in the Run and the Stop mode.

Note: With discrete regulators application, LPCFG (PWR_ON pin configuration in PWR_CR1 register) must always be set to 0.

Table 3 summarizes power supply states for the application operating modes illustrated in Figure 1.

LP-Stop mode is not covered since LPLV-Stop or LPLV-Stop2 are more appropriate in the context of this AN.

Table 3. System operating modes

Operating mode	PWR_ON	PWR_CPU_ON	PWR_LP	Description	Notes
Run	1	1	1	V_{DD} power on V_{DDCORE}, V_{DDCPU}, power on, system clock on V_{3V3} power on, V_{DD_SD} power on/off DDR active/auto refresh	(1)(2)
Stop	1	1	1	V_{DD}, V_{DDCPU} power on V_{DDCORE} power on, system clock off V_{3V3} power on, V_{DD_SD} power on/off DDR active/auto refresh	(1)(2)
LPLV-Stop	1	1	0	V_{DD} power on V_{DDCORE} & V_{DDCPU} (merged) power on at lower voltage, system clock off V_{3V3} power on, V_{DD_SD} power on/off DDR self-refresh	(1)(3)
LPLV-Stop2	1	0	0	V_{DD} power on V_{DDCPU} power off V_{DDCORE} power on at lower voltage, system clock off V_{3V3} power on, V_{DD_SD} power on/off	(1)(4)

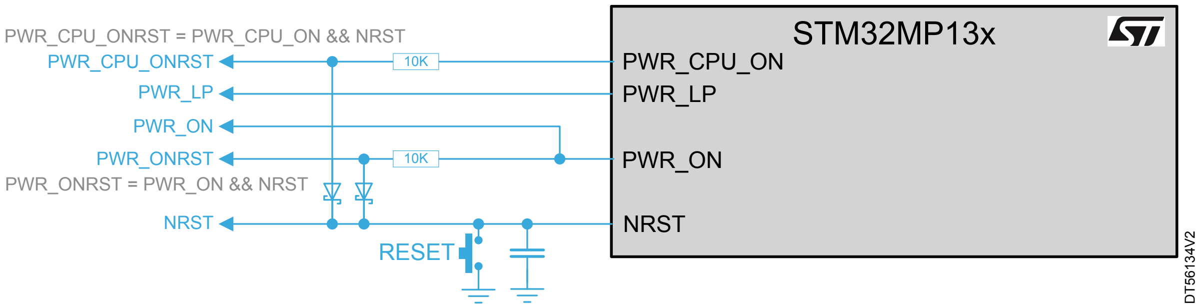
Operating mode	PWR_ON	PWR_CPU_ON	PWR_LP	Description	Notes
				DDR self-refresh	
Standby	0	0	0	V_{DD} power on V_{DDCORE}, V_{DDCPU} power off, system clock off V_{3V3} power off, V_{DD_SD} power off DDR off or self-refresh	(1)(5)
Power off or Coin-cell-VBAT	-	-	-	All power off; except the MPU VSW domain if Coin-cell-VBAT present	(6)

1. *Depending on the application, DDR volatile memory can be DDR3, DDR3L, lpDDR2, or lpDDR3.*
2. *The difference between Run and Stop modes is only based on the STM32MP1 Series microprocessor clock management. For power management, there is no difference between Run and Stop modes.*
3. *LPLV-Stop is relevant only when V_{DDCORE} and V_{DDCPU} are merged, like the application in Figure 5 where LPLV-Stop2 is not supported.*
4. *LPLV-Stop2 can be supported only when V_{DDCORE} and V_{DDCPU} are independent, like applications in Figure 1 and in Figure 6.*
5. *Depending on the application, DDR can be off in Standby mode, like applications in Figure 1; or DDR can be in self-refresh like the application in Figure 6.*
6. *To retain the content of the STM32MP1 Series microprocessor VSW domain (RTC, backup registers, backup RAM, and retention RAM) when VDD is turned off, the STM32MP1 Series microprocessor VBAT pin can be connected to an optional coin cell battery.*

5.1.1 Reset and crash recovery management circuitry

PWR_ONRST and PWR_CPU_ONRST are additional signals dedicated to the management of system reset and crash recovery at the application level. As shown in Figure 8, PWR_ONRST and PWR_CPU_ONRST signals are generated from PWR_ON and PWR_CPU_ON with NRST signal using a discrete logical “AND” circuitry.

Figure 8. PWR_ONRST and PWR_CPU_ONRST crash recovery management signal



The AND logic circuits are composed of a 10 kΩ resistor and a diode. Use of a Schottky diode such as BAT54 or BAT60 is recommended. The 10-kΩ value might be adapted according to the combined impedances of the regulators' EN input pin; especially if some or all of the regulator EN pins have built-in pull-down resistors.

The PWR_ONRST signal and the PWR_CPU_ONRST signal are equivalent to respectively the PWR_ON signal and the PWR_CPU_ON signal. However, if a reset occurs (NRST signal low pulse), the PWR_ONRST and PWR_CPU_ONRST signals go low, meaning that regulators controlled by those signals are turned OFF for the NRST low pulse duration, then are turned back ON after the reset is released to a high state.

This allows power cycling to be performed on peripherals. Power cycling is recommended to ensure that the correct restart and reset of peripherals is assured after an application reset occurs (NRST), especially for peripherals that do not have a reset input signal. Power cycling is especially recommended for peripheral boot devices/flash memory such as eMMC, NAND, NOR, and SD card.

MPU devices have a bidirectional pad reset (NRST) allowing the reset of external devices. If a crash occurs (iwdg1_out_rst or iwdg2_out_rst watchdog elapsing), a reset pulse is generated on the NRST signal. An identical pulse is generated on the PWR_ONRST signal to control the power cycling of the STM32MP13x core domain and the peripheral power supplies. An identical pulse is generated on the PWR_CPU_ONRST signal to control the power cycling of the STM32MP13x Arm® Cortex®-A7 CPU digital power domain. An example timing diagram is provided in Section 5.5 Crash recovery management.

Important: The MPU's RPCTL (Reset Pulse Control) allows control of the minimum pulse duration of the NRST pin. It must be enabled by the software at boot-up and set to the appropriate duration, for example, 31 ms by setting bitfield MRD[4:0] = 0x1F in the RCC_RDLSICR register.

This ensures that discrete regulator output voltages have enough time to drop before the pulse ends (transits to '1') and re-enables the regulators.

In Figure 9 through Figure 16, the VDDA1V8_REG level and the signal waveforms associated with its management are shown in light blue for clarity.

5.2 Power-up/power-down sequence and reset management

5.2.1 Power-up / power-down with V_{DDCORE} and V_{DDCPU} independent, DDR3L (Figure 1)

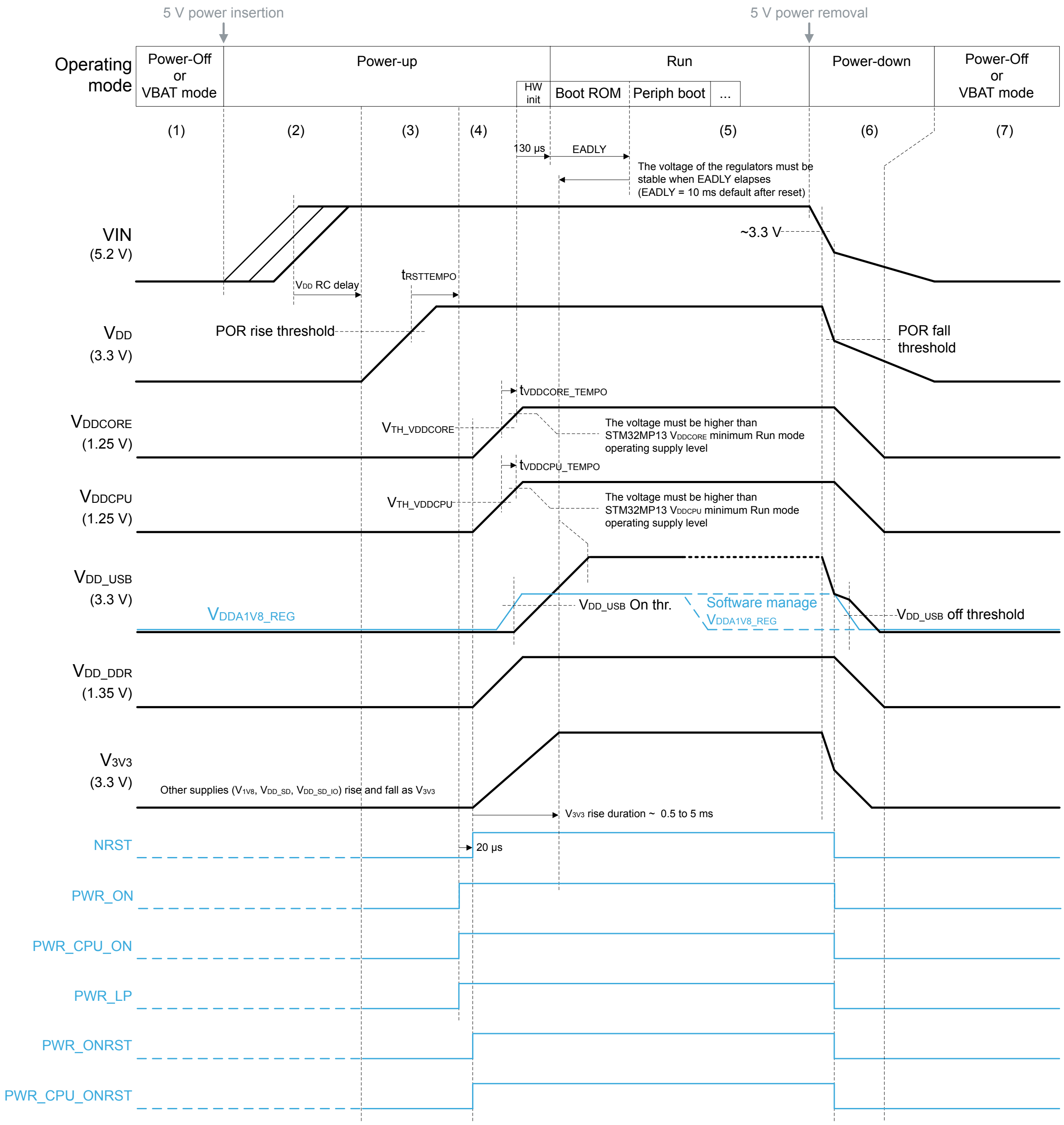
The power sequence described in this subsection is only applicable to Figure 1 having an independent power supply for V_{DDCORE} and V_{DDCPU} with a DDR3L volatile memory.

1. The application is not powered, or the MPU is in VBAT mode (powered from VBAT to supply the V_{SW} power domain).
2. A valid power supply source is connected to the application. The VIN voltage rises. After a delay, (defined by a passive R-C network), to allow the VIN voltage to stabilize, the V_{DD} regulator is enabled.
3. The V_{DD} voltage starts to rise:
   a. The NRST, PWR_ON, PWR_CPU_ON, and PWR_LP signals are set to LOW by the MPU, forcing the PWR_ONRST and PWR_CPU_ONRST signals to LOW.
   b. Once the V_{DD} supply is above the POR rising threshold level(1), a $t_{RSTTEMPO}$ (2) delay is started.
4. Once the $t_{RSTTEMPO}$ has elapsed, the PWR_ON, PWR_CPU_ON and PWR_LP signals are set high by the MPU:
   a. After $t_{RSTTEMPO}$ elapses, the MPU waits for 20 µs(3) before releasing the NRST signal, making PWR_ONRST and PWR_CPU_ONRST going to a high level. V_{DD_DDR}, V_{3V3}, V_{1V8}, V_{DD_SD} and $V_{DD\_SD\_IO}$ are enabled by PWR_ONRST signal and the V_{DD_DDR}, V_{3V3}, V_{1V8}, V_{DD_SD} and $V_{DD\_SD\_IO}$ voltages start to rise.
   b. V_{DDCORE} regulator is enabled by PWR_ONRST signal and V_{DDCORE} voltage starts to rise.
   c. V_{DDCPU} regulator is enabled by PWR_CPU_ONRST signal and V_{DDCPU} voltage starts to rise.
   d. Once the V_{DDCORE} voltage is above the $V_{TH\_VDDCORE}$ (4) rising threshold level, a $t_{VDDCORE\_TEMPO}$ (5) is started. As long as the $t_{VDDCORE\_TEMPO}$ has not elapsed, the MPU is kept in internal reset.
   e. Once the V_{DDCPU} voltage is above the V_{TH_VDDCPU} (6) rising threshold level, a t_{VDDCPU_TEMPO} (7) is started. As long as the t_{VDDCPU_TEMPO} has not elapsed, the CPU Cortex A7 is kept in internal reset.

5. Once the $t_{VDDCORE\_TEMPO}$ elapses, the MPU core domain is taken out of internal reset (V_{DDCORE_OK}):
   a. The V_{DDCORE} voltage must be higher than V_{DDCORE}[(8)] minimum Run mode operating supply level. This must be guaranteed by the V_{DDCORE} regulator slew rate.
   b. V_{DDA1V8_REG} internal regulator is enabled. When V_{DDA1V8_REG} voltage reaches the V_{DD_USB} regulator enable threshold, the V_{DD_USB} regulator is enabled
   c. The MPU performs internal hardware initialization (enabling HSI and option bytes loading with ~130 µs duration). EADLY[(9)] timer (10 ms) delay is started.
   d. When EADLY has elapsed and the $t_{VDDCCPU\_TEMPO}$ has elapsed, the CPU Cortex A7 is taken out of internal reset (V_{DDCPU_OK}) then the MPU enters Run mode. The Boot ROM starts accessing the external peripherals to load and execute the boot software.
   e. After the application has initialized, the software might enable the USB interface (V_{BUS_SW1}, V_{BUS_SW2})
6. Power supply source is removed from the application:
   a. The VIN voltage drop
   b. When the VIN voltage is close to $V_{DD,}$ V_{DD_USB}, and V_{3V3} (3.3 V), they start to drop in parallel with VIN.
   c. Once the V_{DD} supply is below the POR fall threshold[(10)], the MPU reset internally and disables V_{DDA1V8_REG}. NRST, PWR_ON, PWR_CPU_ON, and PWR_LP signals are set to LOW by the MPU. The PWR_ONRST and PWR_CPU_ONRST signals are forced low by the NRST, PWR_ON, and PWR_CPU_ON signals. The V_{DDCORE}, V_{DDCPU}, V_{DD_DDR}, and V_{3V3} regulators are disabled. $V_{DD\_SD,}$ $V_{DD\_SD\_IO}$, V_{BUS_SW1}, and V_{BUS_SW1} are disabled and fall, and V_{BUS} too. The current consumption of VIN drops, making VIN fall slowly. When the V_{DDA1V8_REG} voltage reaches the regulator disable threshold for V_{DD_USB}, the V_{DD_USB} regulator is disabled.
7. The application has no power or the MPU is in VBAT mode (powered from VBAT to supply V_{SW} power domain.

1. *POR rise threshold = V_{BOR0} rising edge = 1.67 V typ*
2. *$t_{RSTTEMPO}$ = 377 µs typ*
3. *Internal RCC delay of the MPU*
4. *$V_{TH\_VDDCORE}$ rising edge = 0.95 V min*
5. *$t_{VDDCORE\_TEMPO}$ = 200 µs min*
6. *V_{TH_VDDCPU} rising edge = 0.95 V min*
7. *t_{VDDCPU_TEMPO} = 200 µs min*
8. *V_{DDCORE} operating voltage = 1.21 V min*
9. *The EADLY timer prevents the Boot ROM from performing any access to the boot peripheral before it is ready when recovering from Standby mode. Typically, it waits for a stable voltage on the flash memory that is read by the Boot ROM to get the boot software. In this application, the default value (10 ms) is kept to wait for the V_{3V3} and V_{DD_USB} voltage to stabilize (refer to RM0475 [4] for more details).*
10. *POR fall threshold = V_{BOR0} falling edge = 1.63V typ (or = V_{BOR3} falling edge = 2.6 V max if option byte SELINBORH[0:1] = 11 (BOR = 2.7V))*

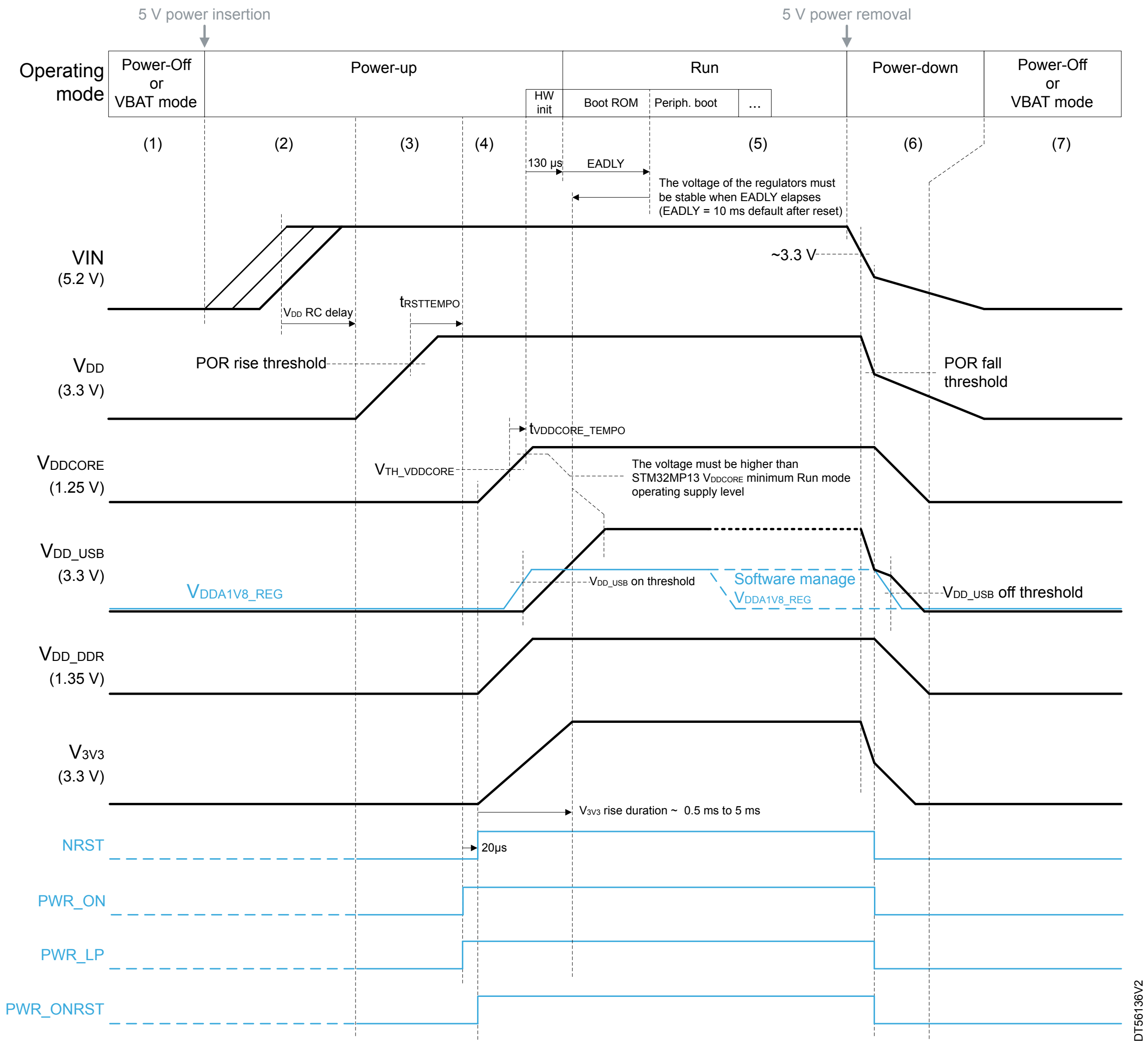
Figure 9. Power-up / power-down with V_{DDCORE} and V_{DDCPU} independent, DDR3L



5.2.2 Power-up / power-down with V_{DDCORE} and V_{DDCPU} merged, DDR3L (Figure 5)

The power sequence described in this subsection is only applicable to Figure 5 having V_{DDCORE} and V_{DDCPU} merged with a DDR3L volatile memory. The description of Figure 10 is not provided because it is very similar to Section 5.2.1 Power-up / power-down with V_{DDCORE} and V_{DDCPU} independent, DDR3L (Figure 1).

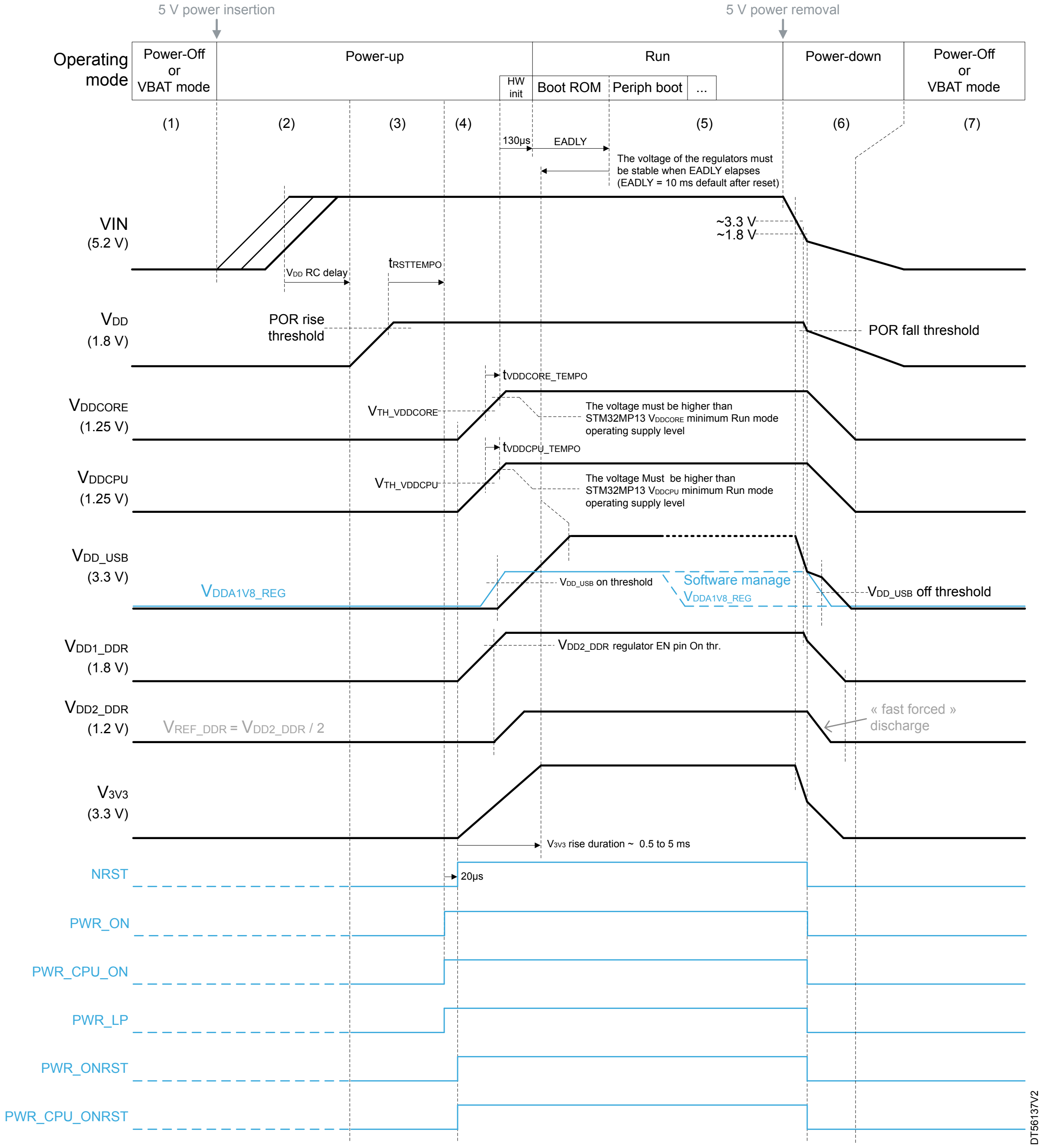
Figure 10. Power-up / power-down with V_{DDCORE} and V_{DDCPU} merged, DDR3L



5.2.3 Power-up / power-down with V_{DDCORE} and V_{DDCPU} independent, lpDDR2/3 (Figure 6)

The power sequence described in this subsection is only applicable to Figure 6 having V_{DDCORE} and V_{DDCPU} independent with an lpDDR2/3 volatile memory. The description of Figure 11 is not provided because it is very similar to Section 5.2.1 Power-up / power-down with V_{DDCORE} and V_{DDCPU} independent, DDR3L (Figure 1) except for VDD voltage at 1.8 V and an lpDDR2/3 instead of a DDR3L

Figure 11. Power-up / power-down with V_{DDCORE} and V_{DDCPU} independent, lpDDR2/3



5.3 STM32MP15xD and STM32MP15xF Run overdrive mode management

The STM32MP13xD and STM32MP13xF devices have an enhanced consumer mission profile (refer to [6]) which allows the Arm® Cortex®-A7 CPU to run at higher clock frequency (refer to [5] for details and limitations).

Accordingly, the V_{DDCCPU} supply voltage must be increased when the CPU frequency (Fmpuss_ck) operates above 650 MHz. Refer to the datasheet [5] for the V_{DDCPU} Run overdrive minimum voltage value. When it does not operate in the Run mode above 650 MHz, the V_{DDCPU} supply voltage must be set back to its nominal Run mode voltage.

The V_{DDCPU} voltage is increased by setting the PWR_OVRDRV signal to HIGH which controls the VSEL signal of the V_{DDCPU} VRM to set its output voltage to the Run overdrive mode voltage. Reciprocally, the V_{DDCPU} voltage is decreased by resetting the PWR_OVRDRV signal to '0' to set the V_{DDCPU} VRM output voltage to the Run mode.

When going from Run mode to Run overdrive mode above 650 MHz, V_{DDCPU} must be increased before the frequency.

When going from Run overdrive mode back to Run mode, the frequency must be decreased before the voltage.

When the Run overdrive mode is needed, the MPU_RAM_LOWSPEED bit in the MPU PWR_CR1 register must be managed by software in addition to the V_{DDCPU} voltage change.

The MPU_RAM_LOWSPEED bit must be reset (it is an action that software must manage) by respecting the two conditions below:

- After the V_{DDCPU} supply has reached the Run overdrive mode voltage range
- Before increasing the STM32MP13xD/F frequency into the overdrive frequency range.

The MPU_RAM_LOWSPEED bit must be set by respecting the two conditions below:

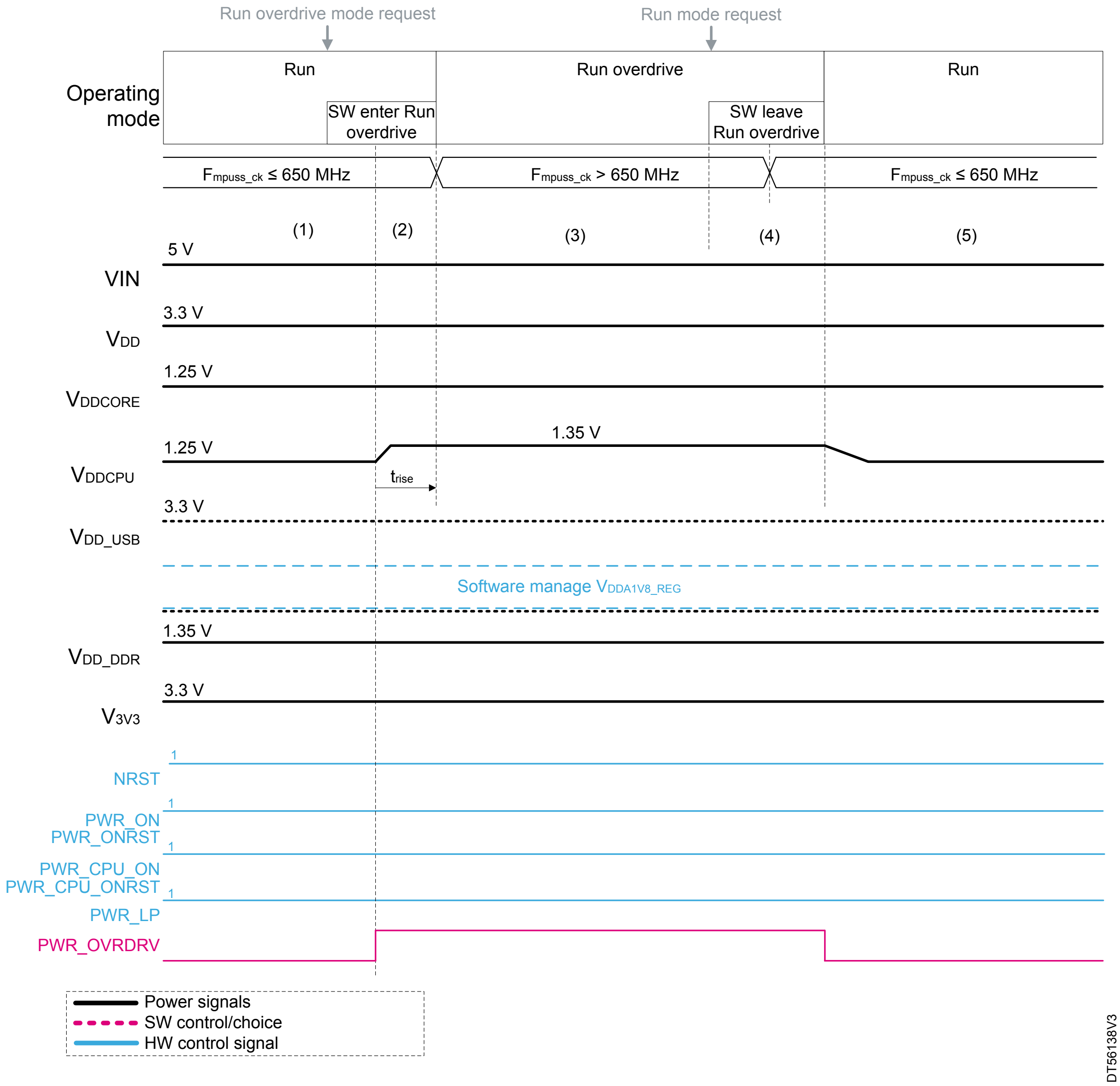
- After decreasing the MPU frequency into the standard frequency range
- Before decreasing the MPU voltage below the Run overdrive mode voltage range.

The application Run overdrive mode sequence is shown in Figure 12 according to the implementation shown in Figure 1.

1. The application is operating in Run mode with a CPU frequency below 650 MHz
2. When Run overdrive mode is requested:
   a. The software prepares to enter Run overdrive mode: it changes the V_{DDCPU} voltage level by setting PWR_OVRDRV signal to '1'.
   b. V_{DDCPU} voltage starts to rise.
   c. Software wait for t_{rise}[(1)].
3. Once V_{DDCPU} reaches the Run overdrive voltage (t_{rise} duration elapsed):
   a. The software resets the MPU_RAM_LOWSPEED bit.
   b. Then, the software increases the CPU frequency above 650 MHz. The system is now in Run overdrive mode above 650 MHz.
4. When the Run mode is requested:
   a. The software prepares to resume Run mode: It changes the CPU frequency to below or equal to 650 MHz
   b. Then, the software sets the MPU_RAM_LOWSPEED bit.
5. Once the bit MPU_RAM_LOWSPEED is set:
   a. The software decreases the V_{DDCPU} voltage level by setting the PWR_OVRDRV signal to LOW.
   b. The system is now in Run mode below 650 MHz.

1. Duration required for V_{DDCPU} regulator to rise from Run mode voltage to Run overdrive mode voltage. For example, assuming a regulator having 1 mV / µs, the software needs to wait for t_{rise} = 100 µs minimum to go from 1.25 to 1.35 V.

Figure 12. Run mode and Run overdrive mode sequence



5.3.1 Run overdrive mode low-cost alternative

The V_{DDCPU} can always be set at 1.35 V allowing the CPU to work in Run mode (CPU frequency lower than 650 MHz) and in Run overdrive mode (CPU frequency higher than 650 MHz).

This simplifies the V_{DDCPU} VRM design to manage a single output voltage (1.35 V) and to free the PWR_OVRDRV GPIO.

But always using V_{DDCPU} at 1.35 V does not guarantee lifetime (refer to [6]) and increases the CPU power consumption in Run mode (CPU frequency < 650 Mhz)

5.4 Low power mode management

Note: Stop mode concerns the MPU internal clock management without external power management. So, the Stop mode is not described in this section.

5.4.1 LPLV-Stop mode

As mentioned in Table 3, the LPLV-Stop mode is only relevant when V_{DDCORE} and V_{DDCPU} are merged. Accordingly, the sequence shown in Figure 13 is only applicable to the application shown in Figure 5.

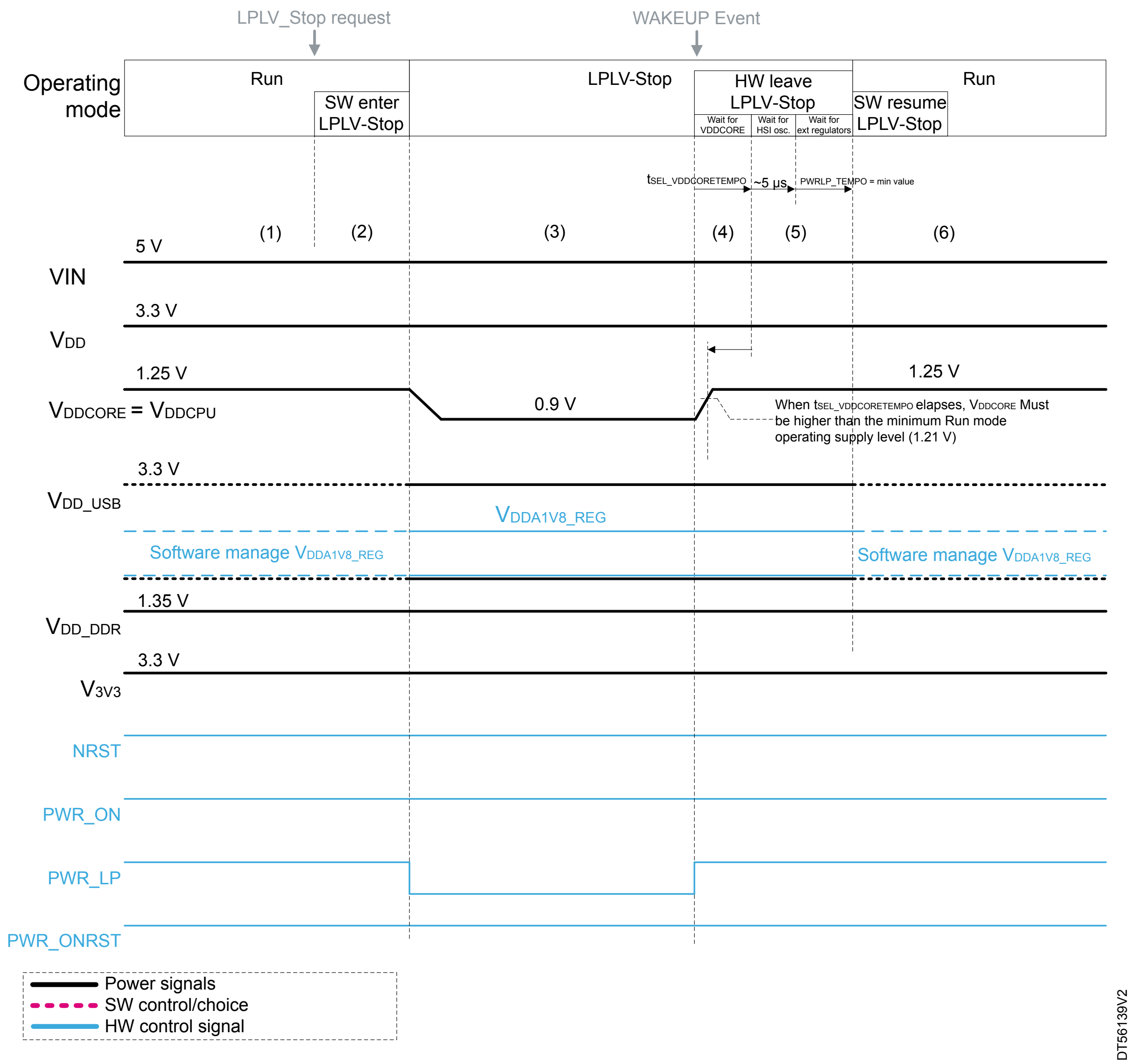
1. The application is powered and is working in Run operating mode.
2. When the LPLV_Stop operating mode is requested, the software prepares an LPLV_Stop entry process such as stopping some clocks, setting DDR to Self-Refresh, and setting PWRLP_TEMPO(1).
3. The MPU sets the LPDS and LVDS bit of the PWR_CR1 register to prepare to enter LPLV-Stop:
   a. The PWR_LP signal is deasserted when the MPU enters LPLV-Stop.
   b. Once the PWR_LP signal is deasserted, the V_{DDCORE} regulator VSEL input goes low making V_{DDCORE} voltage decreasing to reach the LPLV-Stop mode operating supply level (0.9 V)
4. On a wakeup event, the MPU leaves LPLV-Stop mode and asserts the PWR_LP signal:
   a. The MPU timer $t_{SEL\_VDDCORETEMPO}$ (2) is started to allow V_{DDCORE} voltage to reach the Run mode operating supply level.
   b. The V_{DDCORE} regulator VSEL input goes high making V_{DDCORE} voltage increase.
5. Once $t_{SEL\_VDDCORETEMPO}$ has elapsed:
   a. V_{DDCORE} must be higher than the minimum Run mode operating supply level(3) (refer to [4] and [5]).
   b. A clock restore process is performed in the MPU.
6. Once the MPU HSI clock oscillator is stable (~5 µs), the application goes into the Run mode (as the PWRLP_TEMPO timer set to min value) and the software resumes normal operations (such as restoring clocks and restoring DDR from self-refresh).

1. PWRLP_TEMPO is an STM32MP13x dedicated timer designed to wait for the regulator recovery when the application goes from low-power mode to Run mode. In this application, the PWRLP_TEMPO delay can be set to min value or bypassed (in bitfield PWRLP_DLY[21:16] of the RCC_PWRLPDLYCR register) as when $t_{SEL\_VDDCORETEMPO}$ elapsed, the V_{DDCORE} voltage must already be higher than minimum Run mode operating supply level.

2. $t_{SEL\_VDDCORETEMPO}$ 234 µs min (refer to [4]).

3. This constraint must be guaranteed by the design of the V_{DDCORE} regulator.

Figure 13. LPLV-Stop mode sequence



5.4.2 LPLV-Stop2 mode

As mentioned in Table 3, the LPLV-Stop2 mode is only possible when V_{DDCORE} and V_{DDCPU} are independent. Accordingly, the sequence shown in Figure 14 is only applicable to applications shown in Figure 1 and Figure 6. Only the LPLV-Stop2 mode sequence of application shown in Figure 1 is described in this subsection as the LPLV-Stop2 mode sequence is equivalent to the application shown in Figure 6

1. The application is powered and is working in Run operating mode.
2. When the LPLV-Stop2 operating mode is requested, the software prepares an LPLV-Stop2 entry process such as stopping some clocks, setting DDR to Self-Refresh, and setting PWRLP_TEMPO.
3. The MPU sets the LPDS, LVDS and STOP2 bit of the PWR_CR1 register to prepare entering LPLV-Stop2:
   a. The PWR_LP signal and the PWR_CPU_ON signal are deasserted when the MPU enters LPLV-Stop2.
   b. Once the PWR_LP signal is deasserted, the V_{DDCORE} regulator VSEL input goes low making V_{DDCORE} voltage decrease to reach the LPLV-Stop2 mode operating supply level (0.9 V).
   c. Once the PWR_CPU_ON signal is deasserted, the PWR_CPU_ONRST signal is deasserted in parallel and the regulator of the V_{DDCPU} goes off making the V_{DDCPU} voltage decrease to reach 0 V.

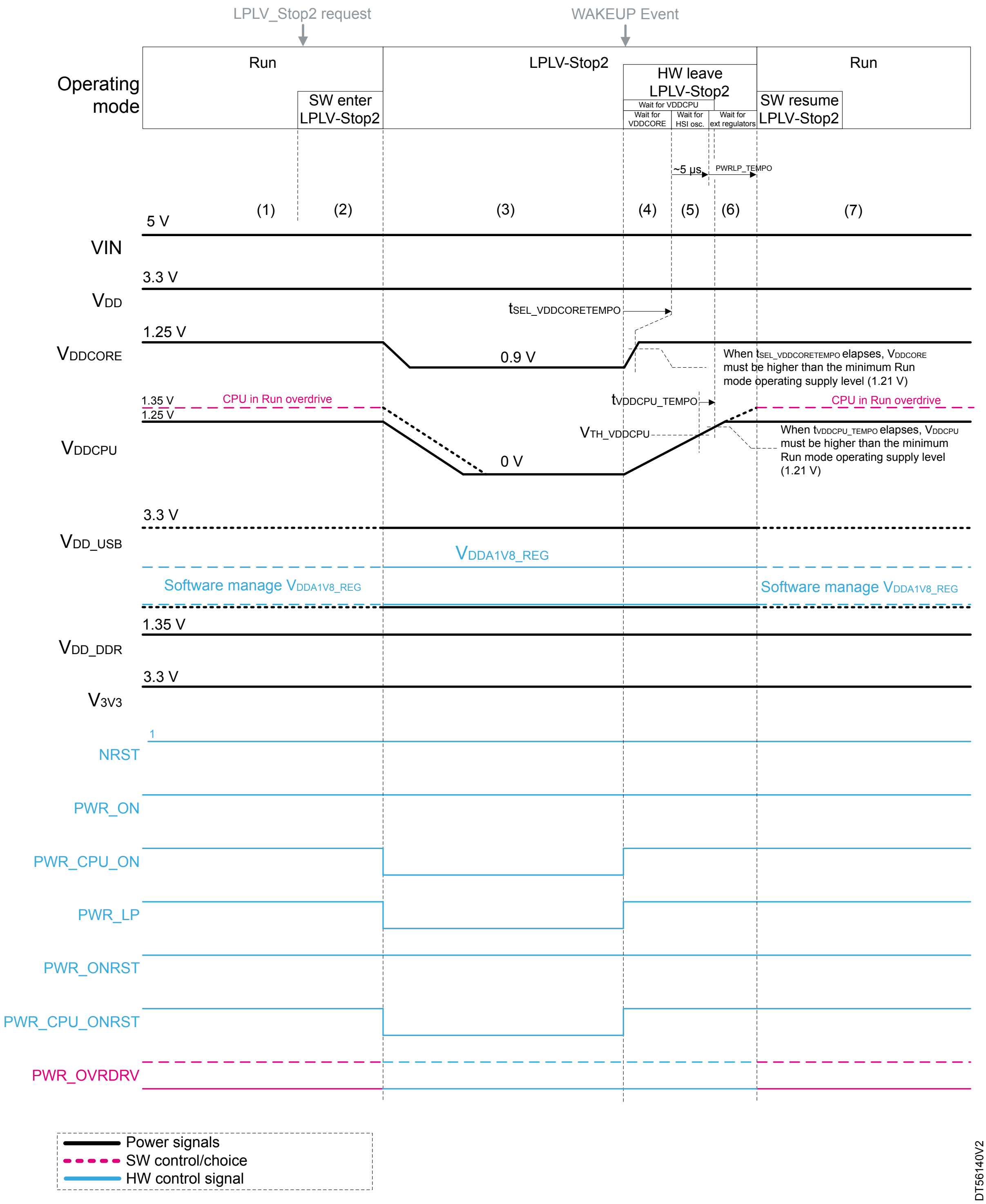
4. On a wakeup event, the MPU leaves LPLV-Stop mode and asserts the PWR_LP signal and the PWR_CPU_ON signal:
   a. The MPU timer $t_{SEL\_VDDCORETEMPO}$ (1) is started to allow V_{DDCORE} voltage to reach the Run mode operating supply level.
   b. Once the PWR_LP signal goes HIGH, the V_{DDCORE} regulator VSEL input goes high making V_{DDCORE} voltage increase.
   c. Once the PWR_CPU_ON signal goes HIGH, the PWR_CPU_ONRST goes HIGH in parallel and the V_{DDCPU} regulator goes on making V_{DDCPU} voltage increase.
5. Once $t_{SEL\_VDDCORETEMPO}$ has elapsed:
   a. The V_{DDCORE} must be higher than the minimum Run mode operating supply level(2) (refer to [4] and [5]).
   b. A clock restore process is performed in the MPU
   c. Once the MPU HSI clock oscillator is stable (~5 µs), the PWRLP_TEMPO timer is started.
6. Once the V_{DDCPU} voltage is above the V_{TH_VDDCPU} (3) rising threshold level, a t_{VDDCPU_TEMPO} (4) is started.
7. Once the t_{VDDCPU_TEMPO} and the PWRLP_TEMPO have both elapsed, the application goes into Run mode:
   a. The software resumes normal operations (such as restoring clocks and restoring DDR from self-refresh).
   b. The software might switch the CPU to Run overdrive mode (set the PWR_OVRDRV signal high, reset the MPU's MPU_RAM_LOW bit of PWR_CR1 register then increase the CPU frequency).

1. *$t_{SEL\_VDDCORETEMPO}$ 234 µs min (refer to [4]).*
2. *This constraint must be guaranteed by the design of the V_{DDCORE} regulator.*
3. *V_{TH_VDDCPU} rising edge = 0.95 V min*
4. *t_{VDDCPU_TEMPO} = 200 µs min*

Note: If the MPU goes in LPLV-Stop2 while it is running in CPU overdrive step 2 (V_{DDCPU} = 1.35 V as PWR_OVRDRV = 1) then, V_{DDCPU} goes back to CPU overdrive voltage when leaving LPLV-Stop2 step 4 and the CPU overdrive frequency is set back during the LPLV-Stop2 SW resume step 7.

Warning: *To manage a scenario where LPLV-Stop2 is very short, it is usually required to set PWRLP_TEMPO delay (PWRLP_DLY in RCC_PWRLPDLYCR register) equal to or higher than the V_{DDCPU} regulator soft-start delay (typically about 1 to 2 ms for common discrete step-down SMPS): In case of very short LPLV-Stop2 duration, the PWR_CPU_ON signal (controlling V_{DDCPU} regulator EN pin) pulses low for a very short duration. Depending on the V_{DDCPU} regulator model used in the application, its internal soft-start delay is usually rearmed once its EN pin goes low. Consequently, when a very short LPLV-Stop2 scenario occurs, the V_{DDCPU} regulator goes off then it goes back on immediately. In that case, the V_{DDCPU} voltage slightly decreases and keeps higher than the $V_{TH-VDDCPU}$ threshold, but it does not regulate until its internal reference voltage (following soft-start delay) crosses the regulator output voltage. In that case and if PWRLP_TEMPO delay is set to min value, the MPU goes into Run mode once $t_{SEL\_VDDCORETEMPO}$ and clock restore process is ended as V_{DDCPU} is ready (higher than $V_{TH-VDDCPU}$). Once the CPU runs, making load current on V_{DDCPU}, the V_{DDCPU} voltage drops below V_{DDCPU} minimum operating voltage making the CPU crash, due to the V_{DDCPU} regulator not being ready (soft-start ongoing).*

Figure 14. LPLV-Stop2 mode sequence



5.4.3 Standby mode with V_{DDCORE} and V_{DDCPU} independent, DDR3L (Figure 1)

The application Standby mode sequence is shown in Figure 15. Standby mode sequence according to the implementation shown in Figure 1. STM32MP13x with DDR3L, boot flash, SD card UHS-I, USB-A host, and USB-C PD having independent power supply for V_{DDCORE} and V_{DDCPU} with a DDR3L volatile memory.

In this application, the boot flash memory used by the boot ROM to read the boot software (for example FSBL) is powered from the V_{3V3} domain, and the DDR3L memory is powered OFF in Standby mode.

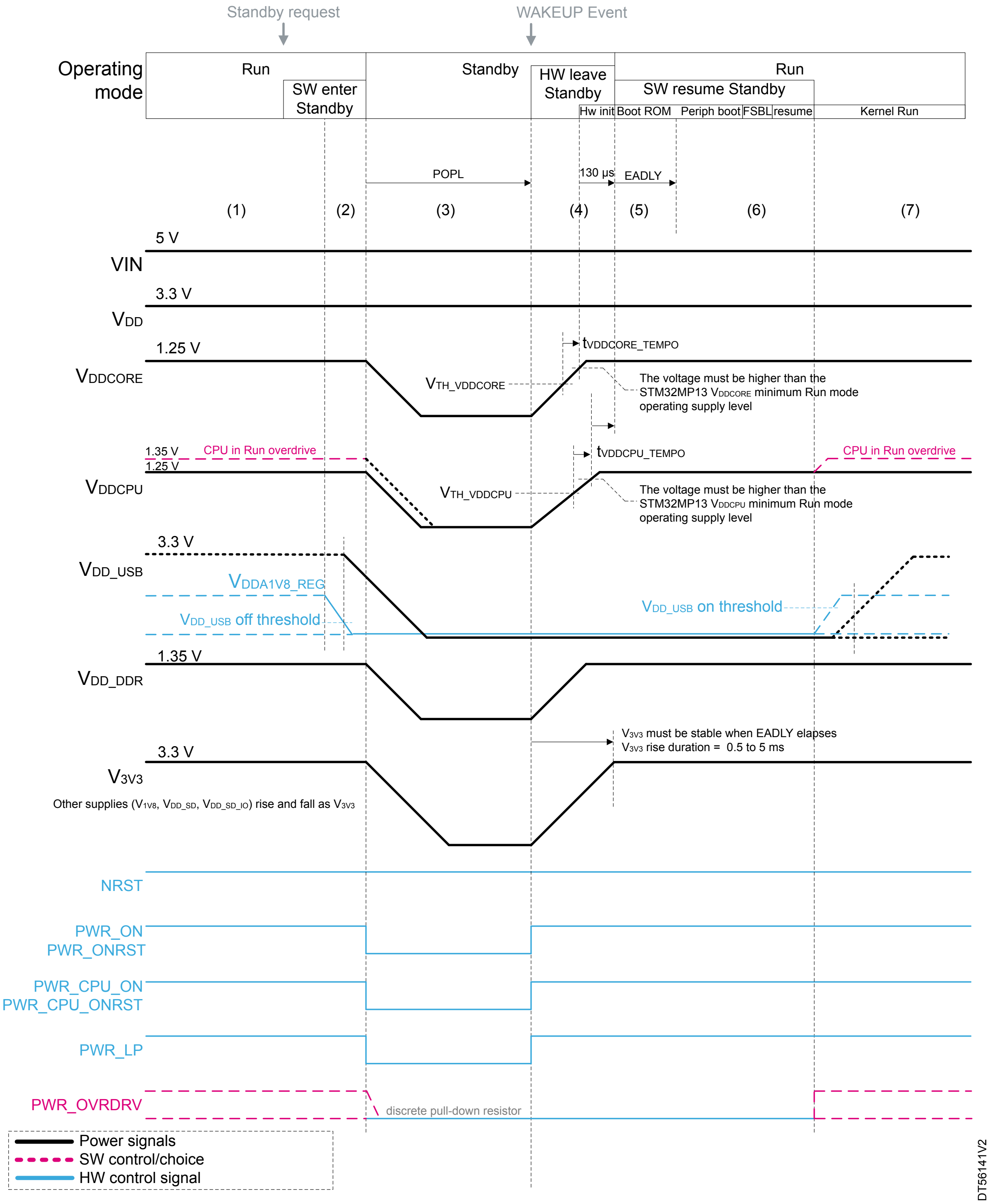
1. The application is powered and running. When Standby mode is requested, the software prepares for Standby entry (stops some clocks, …, sets POPL[1] and EADLY[2] timers, and so on)
2. The software might switch off USB power domains by turning off V_{DDA1V8_REG} making the V_{DD_USB} regulator switch off[3]. When the software is ready, the MPU enters Standby mode and the POPL timer starts automatically.
3. The PWR_ON, the PWR_CPU_ON and the PWR_LP signals are deasserted:
   a. The PWR_ONRST signal, the PWR_CPU_ONRST are forced low.
   b. V_{DDCORE} regulator is powered Off by PWR_ONRST signal
   c. V_{DDCPU} regulator is powered Off by PWR_CPU_ONRST signal
   d. V_{DD_DDR} and V_{3V3} regulators are powered off by the PWR_ONRST signal
4. On a wakeup event, the MPU leaves Standby mode[4], asserts the PWR_ON, the PWR_CPU_ON and the PWR_LP signals:
   a. The PWR_ONRST and the PWR_CPU_ONRST signals rise as NRST are high. V_{DD_DDR}, and V_{3V3} are enabled by the PWR_ONRST signal and the V_{DD_DDR}, and V_{3V3} voltages start to rise
   b. The V_{DDCORE} regulator is enabled by the PWR_ONRST signal and the V_{DDCORE} voltage starts to rise.
   c. The V_{DDCPU} regulator is enabled by the PWR_CPU_ONRST signal and the V_{DDCPU} voltage starts to rise.
   d. Once the V_{DDCORE} voltage is above the $V_{TH\_VDDCORE}$ rising minimum threshold, a $t_{VDDCORE\_TEMPO}$ delay is started to allow V_{DDCORE} voltage to reach the Run mode operating supply level.
   e. Once the $t_{VDDCORE\_TEMPO}$ elapsed[5], the MPU performs internal hardware initialization (enables the HSI and option-byte loading with 130 µs duration)
   f. Once the V_{DDCPU} voltage is above the V_{TH_VDDCPU} rising minimum threshold, a t_{VDDCPU_TEMPO} delay is started to allow V_{DDCPU} voltage to reach the Run mode operating supply level.
5. Once the internal hardware initialization ends and the t_{VDDCPU_TEMPO} has elapsed, the MPU is taken out of internal reset (V_{DDCORE_OK} and V_{DDCPU_OK}):
   a. The EADLY delay timer is started.
6. When EADLY has elapsed, the Boot ROM starts accessing external peripherals (flash memory) to load and execute the boot software. Implicitly, when EADLY has elapsed, all voltages of the regulators must be stable; especially V_{3V3} which is the power domain supplying flash memory:
   a. The Boot ROM reads (peripheral boot), verifies, and executes the FSBL.
   b. The software detects an “exit from Standby mode” and resumes the Kernel software accordingly.
7. Once the software has resumed:
   a. The software might switch the USB power domains on by turning V_{DDA1V8_REG} on and making the V_{DD_USB} regulator switch on, depending on the presence of USB devices.
   b. The software might switch the CPU to Run overdrive mode (set the PWR_OVRDRV signal high, reset the MPU’s MPU_RAM_LOW bit of PWR_CR1 register then increases the CPU frequency).

1. The STM32MP13x POPL timer allows the STM32MP13x to be kept on standby and to assert a PWR_ON signal low for a minimum duration. This action allows the peripheral regulators, the V_{DDCPU} regulator, and the V_{DDCORE} regulator to discharge their respective output voltage before restarting them. This is to ensure the peripherals restart properly if a wake-up event occurs just after the application goes into standby. The POPL timer must be set according to the regulator having the slowest falling voltage (for example, 10 ms is suggested for the application having a regulator with embedded output discharge).

2. The STM32MP13x EADLY timer is dedicated to preventing boot ROM from performing any access to the boot peripheral before it is ready when recovering from Standby mode. It waits for a stable voltage on the flash memory to ensure that the boot software is reliably read by the boot ROM. The flash memory can be the eMMC or the SD-Card. In this application, V_{3V3} rise time depends on the V_{3V3} regulator characteristics and control so the minimum EADLY must be set accordingly (eg: 5 ms is suggested for the application having a V_{3V3} regulator rising voltage in 5 ms)

3. *Alternatively, if V_{DDA1V8_REG} is not turned off by the software before entering Standby mode, it is automatically disabled by hardware at that time, turning V_{DD_USB} off. In that case, V_{DDA1V8_REG} is automatically turned on by the hardware when leaving Standby mode, turning V_{DD_USB} on.*
4. *The STM32MP13x waits for the POPL timer to elapse before leaving Standby mode; even if a wakeup event occurs before.*
5. *The V_{DDCORE} voltage must be higher than the minimum Run mode operating supply level (refer to [4] and [5]) This constraint must be guaranteed by the design of the V_{DDCORE} regulator.*

Figure 15. Standby mode sequence



5.4.4 Standby mode with V_{DDCORE} and V_{DDCPU} merged, DDR3L (Figure 5)

The application Standby mode sequence shown in Figure 5 having merged V_{DDCORE} and V_{DDCPU} power supplies and with a DDR3L has an equivalent sequence to the one in Section 5.4.3 Standby mode with V_{DDCORE} and V_{DDCPU} independent, DDR3L (Figure 1) with the following differences:

- V_{DDCPU} is merged with V_{DDCORE}. So V_{DDCPU} rises and falls at the same time as V_{DDCORE}
- CPU Run overdrive mode is not supported

5.4.5 Standby mode with V_{DDCORE} and V_{DDCPU} independent, lpDDR2/3 (Figure 6)

The application Standby mode sequence is shown in Figure 6. STM32MP13x with lpDDR2/3, boot flash, and I/Os voltage at 1.8 V and has V_{DDCORE} and V_{DDCPU} independent with an lpDDR2/3 volatile memory has an equivalent sequence to the one in Section 5.4.3 Standby mode with V_{DDCORE} and V_{DDCPU} independent, DDR3L (Figure 1) with the following difference:

- lpDDR2/3 keeps in self-refresh in Standby mode. So V_{DD1_DDR} and V_{DD2_DDR} are kept enabled in Standby mode.

5.5 Crash recovery management

5.5.1 Crash recovery management with V_{DDCORE} and V_{DDCPU} independent, lpDDR2/3 (Figure 6)

As shown in Section 5.1.1 Reset and crash recovery management circuitry, a discrete circuitry must be added to the design (refer to Figure 8) to perform a power cycling. This allows the MPU and peripherals to restart properly after a crash. This is especially suitable for flash memory, which does not have a reset input to restart it properly after a crash (Eg: SD-Card working in UHS-I mode must have a power cycling to go back to legacy mode allowing it to be booted from the MPU's bootROM).

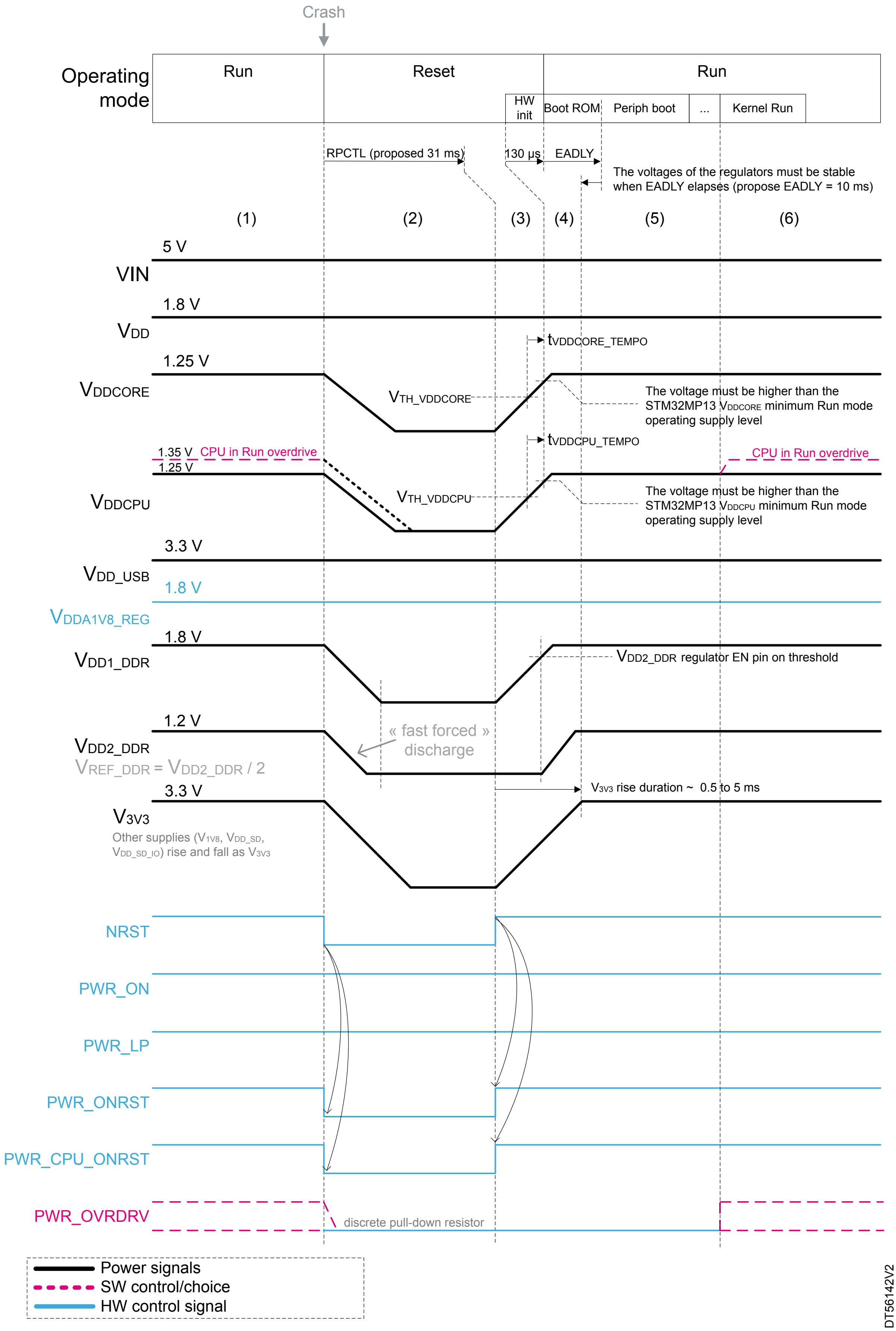
The sequence shown in Figure 16 illustrates a crash recovery sequence according to the implementation shown in Figure 6. The implementation of Figure 6 shows the most complex crash recovery sequence (highlighting the lpDDR2/3 power sequence constraints).

1. The application is powered and running. The RPCTL timer (refer to Section 5.1.1 Reset and crash recovery management circuitry) is set to 31 ms and EADLY to 10 ms during application initialization. A crash occurs (iwdg1_out_rst or iwdg2_out_rst watchdog elapsing) or an NRST pulse is performed from the user reset button.
2. The MPU asserts the NRST signal and the RPCTL timer starts:
   a. The PWR_ONRST and the PWR_CPU_ONRST signals are forced LOW by the NRST signal
   b. The V_{DD_CPU} regulator is powered off by the PWR_CPU_ONRST signal
   c. The V_{DD_CORE} regulator is powered off by the PWR_ ONRST signal
   d. The V_{DD1_DDR}, V_{DD2_DDR} (1) and V_{3V3} regulators are powered off by the PWR_ONRST signal
   e. The V_{DD_CPU}, V_{DD_CORE}, V_{DD1_DDR}, V_{DD2_DDR} and V_{3V3} voltages fall
3. The RPCTL timer elapses (after 31 ms):
   a. The MPU releases the NRST signal
   b. The PWR_ONRST signal and the PWR_CPU_ONRST signal rise.
   c. The V_{DD_CPU} regulator is powered on by the PWR_CPU_ONRST and the V_{DD_CPU} voltage starts to rise.
   d. The V_{DD_CORE} regulator is powered on by the PWR_ ONRST and the V_{DD_CORE} voltage starts to rise.
   e. The V_{DD1_DDR} and V_{3V3} regulators are powered on by the PWR_ONRST signal and the V_{DD1_DDR}, and V_{3V3} voltages start to rise
   f. Once the V_{DD1_DDR} voltage is above the V_{DD2_DDR} EN pin on threshold, the V_{DD2_DDR} regulator is powered on and the V_{DD2_DDR} voltage starts to rise.
   g. Once the V_{DDCPU} voltage is above the V_{TH_VDDCPU} rising threshold level, a t_{VDDCPU_TEMPO} is started.
   h. Once the V_{DDCORE} voltage is above the $V_{TH\_VDDCORE}$ rising threshold level, a $t_{VDDCORE\_TEMPO}$ is started.

4. Once the $t_{VDDCORE\_TEMPO}$ elapsed:
   a. The MPU performs an internal hardware initialization (enable HSI and option-byte loading with 130 µs duration)
   b. Once the internal hardware initialization ends and the t_{VDDCPU_TEMPO} has elapsed, the MPU is taken out of internal reset and entered in the Run mode, and the EADLY delay timer is started.
5. Once EADLY has elapsed, the Boot ROM starts accessing external peripherals (flash memory) to load and execute the boot software. Implicitly, when EADLY has elapsed, all the voltages of the regulators must be stable; especially V_{3V3} which is the power domain supplying flash memory:
   a. The Boot ROM reads (Periph boot), verifies and executes the FSBL, boot load then Kernel software
6. The Kernel software might switch the CPU in Run overdrive mode (set the PWR_OVRDRV signal high, reset the STM32MP13x's MPU_RAM_LOW bit of PWR_CR1 register then increase the CPU frequency).

1. By design, V_{DD2_DDR} has stronger discharge circuitry than V_{DD1_DDR}. Consequently, V_{DD2_DDR} voltage falls faster than V_{DD1_DDR}.

Figure 16. Crash recovery sequence



5.5.2 Crash recovery management with V_{DDCORE} and V_{DDCPU} independent, DDR3L (Figure 1)

The crash recovery sequence according to the implementation shown in Figure 1 is similar to the implementation illustrated in Section 5.5.1 Crash recovery management with V_{DDCORE} and V_{DDCPU} independent, lpDDR2/3 (Figure 6) with the following difference:

- DDR3L has a single power supply source controlled from PWR_ONRST. it is a similar diagram as VDD1_DDR on Figure 16 with 1.35 V for DDR3L instead of 1.8 V for lpDDR2/3.
- VDD node is 3.3 V in the implementation shown in Figure 1 (1.8 V in the implementation shown in Figure 6).

5.5.3 Crash recovery management with V_{DDCORE} and V_{DDCPU} merged, DDR3L (Figure 5)

The crash recovery sequence according to the implementation shown in Figure 5 is similar to the implementation illustrated in Section 5.5.1 Crash recovery management with V_{DDCORE} and V_{DDCPU} independent, lpDDR2/3 (Figure 6) with the following difference:

- In case of a crash, power cycling occurs on the V_{DDCORE} node (V_{DDCORE} and V_{DDCPU} merged) in the implementation shown in Figure 5. It is a similar diagram in Figure 16 with V_{DDCPU} renamed as V_{DDCORE}
- DDR3L has a single power supply source controlled from PWR_ONRST. It is a similar diagram as VDD1_DDR in Figure 16 with 1.35 V for DDR3L instead of 1.8 V for lpDDR2/3.
- VDD node is 3.3 V in the implementation shown in Figure 5 (1.8 V in the implementation shown in Figure 6).

6 Voltage regulator module specification

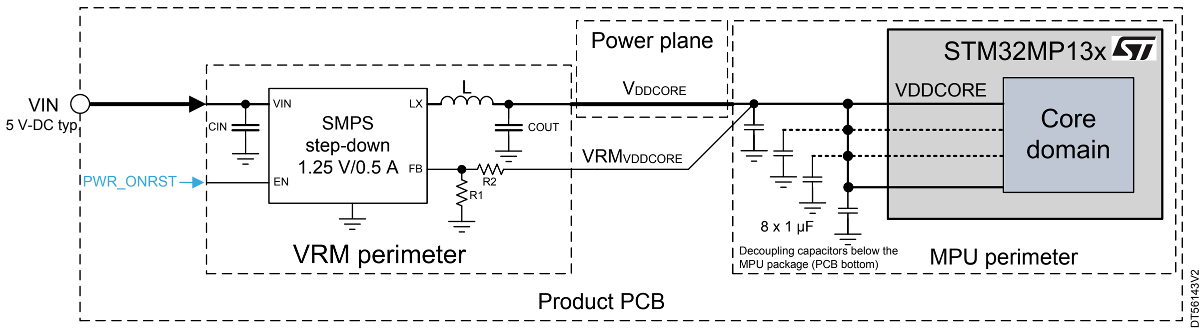
This section provides electrical specifications of the voltage regulator module (VRM) that supplies the MPU power domains.

The product designer must design the VRM according to these electrical specifications by selecting a regulator IC and the associated discrete components.

This section is only applicable if the MPU decoupling scheme (refer to [1]) and layout recommendations are carefully followed to minimize the impedance of the power delivery network (PDN).

Figure 17 illustrates a VRM supplying the MPU V_{DDCORE} power domain. In this illustration, the V_{DDCORE} VRM has no VSEL input to switch the V_{DDCORE} in low voltage during LPLV-Stop mode.

Figure 17. Voltage regulator module perimeter example



6.1 VRM specification for VDD (VDD_ANA, VDD_PLL) power domain

V_{DD} is the main supply for I/Os voltage interfaces and internal parts kept powered during Standby mode. V_{DD_ANA} and V_{DD_PLL} must be connected to V_{DD}. V_{DD} is usually 1.8 or 3.3 V and can be set in the 1.71 to 2 V or 2.7 to 3.6 V ranges.

V_{DDSD1} and V_{DDSD2} might be powered from VDD depending on the expected usage of the V_{DDSD1}/V_{DDSD2} I/Os usage.

This supply is always enabled as long as VIN voltage is present. Choosing a regulator with an EN pin is not necessary. Nevertheless, an EN pin might require a discrete RC filter to be added to delay the regulator startup for the input voltage stabilization.

Table 4. VRM specification for VDD power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
VRM_{VDD}	Output voltage range	Including VRM_{VDD-N}	2.7 1.71	3.3 1.8	3.6 2.0	V
$VRM_{VDD-ACC}$	Output voltage accuracy	including line regulation, load regulation and temperature variation	-5	-	+5	%
VRM_{VDD-N}	Output noise voltage	I_{OUT} = 5 mA to 200 mA f = 1 Hz to 5 MHz	-	-	30	mVp-p
VRM_{IDD}	Rated output current		200(1)	-	-	mA
$VRM_{VDD-TRANS}$	Load transient regulation	I_{OUT} = 5 to 50 mA or 50 to 5 mA in 1 µs	-	-	+/-30	mV

1. *VRM output current is only for the MPU power budget VDD power domain, including V_{DD_ANA} and V_{DD_PLL}. If the VDD VRM is also used to power supply the application peripherals, related additional current consumption must be added (refer to Section 4.1.2 Power distribution and regulators topology recommendation).*

6.2 VRM specification for V_{DDCORE} power domain

V_{DDCORE} is the main MPU digital power domain. Therefore, significant current load transients occur on the V_{DDCORE} supply. Accordingly, special attention to MPU decoupling capacitor placement and layout must be done to minimize the power delivery network impedance (refer to [1]).

This section illustrates applications of Section 4.1 STM32MP13xD/F Run overdrive mode with DDR3L, boot flash, SD-card UHS-I, USB-A host, and USB-C PD and the Section 4.3 STM32MP13xD/F Run overdrive mode with lpDDR2/3, boot flash, USB-A host, and I/Os voltage at 1.8 V.

Table 5. VRM specification for V_{DDCORE} power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
$VRM_{VDDCORE}$	Output voltage in Run mode	including line regulation, load regulation and temperature variation	1.21	1.25	1.29	V
$VRM_{VDDCORE-LPLV-STOP}$	Output voltage in LPLV-Stop or LPLV-Stop2	VRM's VSEL input = 0	0.85	0.9	$VRM_{VDDCORE}$	V
$VRM_{VDDCORE-RIPPLE}$	Output noise/ripple voltage	I_{OUT} = 1 mA to 500 mA f = 10 Hz to 5 MHz	-	-	30	mVp-p
VRM_{ICORE}	Rated output current		500	-	-	mA
$VRM_{VDDCORE-TRANS}$	Load transient regulation	I_{OUT} = 1 mA to 160 mA or 160 mA to 1 mA in 1 µs	-	-	+/-30 (1)	mV
$VRM_{VDDCORE-SR-PU}$	Output voltage slew rate at power-up	$VRM_{VDDCORE}$ from $V_{TH\_VDDCORE-Min}$ to $V_{DDCORE-Min}$	1.3(2)	-	-	V/ms
$VRM_{VDDCORE-SR-LPLV-Stop}$	Output voltage slew rate at LPLV-Stop exit	$VRM_{VDDCORE}$ from the rising edge of VRM's VSEL input to $V_{DDCORE-Min}$	1.55(3)	-	-	V/ms
$VRM_{VDDCORE-AD}$	Active output discharge	$VRM_{VDDCORE}$ from the falling edge of VRM's EN input to 10% of $VRM_{VDDCORE}$		10(4)	31	ms

1. *Voltage overshoot / undershoot caused by load transients must not go higher than $VRM_{VDDCORE}$ + $VRM_{VDDCORE-TRANS}$ for a negative transient current, and lower than $VRM_{VDDCORE}$ - $VRM_{VDDCORE-TRANS}$ for a positive current transient. Implicitly, output voltage noise/ripple ($VRM_{VDDCORE-RIPPLE}$) is included in the $VRM_{VDDCORE-TRANS}$ budget.*
2. *At power-up, once the VRM output voltage cross 0.95 V (STM32MP13's $V_{TH\_VDDCORE\ min}$), the VRM output voltage must be above $VRM_{VDDCORE}$ min in less than 200 µs (STM32MP13's $t_{VDDCORE\_TEMPO}$ min).*
3. *On the LPLV-Stop exit, the STM32MP13's PWR_LP signal goes from low to high. The VRM output voltage must rise from $VRM_{VDDCORE-LPLV-STOP\ min}$ to $VRMV_{VDDCORE\ min}$ in less than 234 µs (STM32MP13's $t_{SEL\_VDDCORETEMPO}$ min).*
4. *As V_{DDCORE} is turned OFF in Standby mode, a regulator having an EN pin is needed to support Standby mode. Additionally, the selection of a regulator with an active output discharge is recommended to allow a fast voltage decrease when the regulator is disabled. Accordingly, the MPU's POPL timer must be set with a value higher than $VRM_{VDDCORE-AD}$.*

Note: If LPLV-Stop mode is not required, the $VRM_{VDDCORE-LPLV-STOP}$ and the $VRM_{VDDCORE-SR-LPLV-Stop}$ parameters must be ignored.

6.2.1 $VRM_{VDDCORE}$ circuitry illustration for LPLV-Stop2 support

The VRM in Figure 18 has additional circuitry inserted into the feedback loop of the SMPS IC which allows it to control two output voltages This optional circuitry allows the switch of the V_{DDCORE} voltage between 1.25 V in Run mode and 0.9 V in LPLV-Stop2 mode.

Figure 18. $VRM_{VDDCORE}$ with scalable 1.25 / 0.9 V circuitry

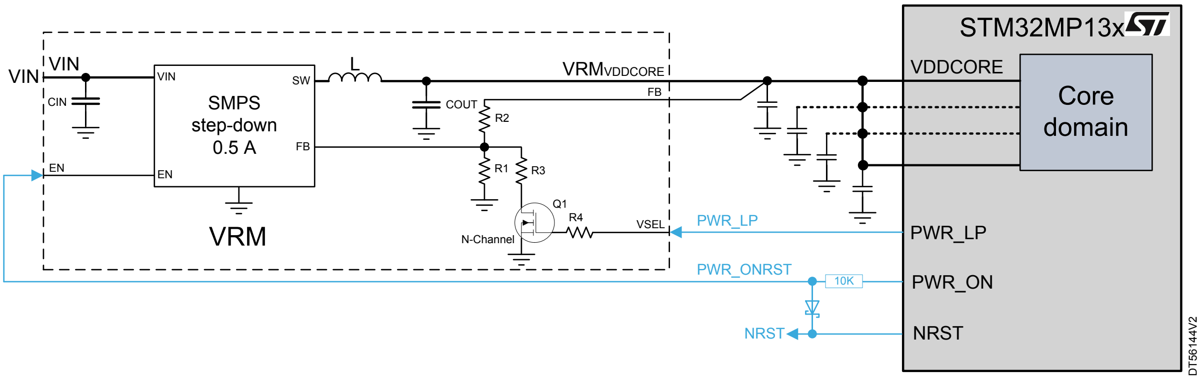


Table 6. VRM 1.25 / 0.9 V truth table

EN	VSEL	$VRM_{VDDCORE}$
0	-	0 V (OFF)
1	0	0.9 V
1	1	1.25 V

Vout (R1, R2, R3, R4) computation example:

Assumption: The step-down SMPS illustrated in Figure 18 has a feedback voltage equal to V_{BF} = 0.6 V

1. When VSEL = 0 (LPLV-Stop mode), the MOSFET Q1 is open and Q1 Drain node is floating. The output voltage $VRM_{VDDCORE}$ is minimum and is equal to:
   $VOUT_0 = (R1 + R2) / R1 \times V_{FB} = 0.9$ V
2. When VSEL = 1 (RUN mode), the MOSFET Q1 is closed and Q1 Drain node is grounded (Q1 R_{DSON} neglected comparing to R3 value). The output voltage $VRM_{VDDCORE}$ is maximum and is equal to:

$VOUT_1 = (R1//R3 + R2) / R1//R3 \times V_{FB} = 1.25$ V

R1 and R2 need to be selected first to reach $VOUT_0$ = 0.9 V output voltage. In this first step, choose an arbitrary value for R1 or R2.

In the second step, R3 must be selected to reach $VOUT_1$ = 1.25 V

R4 has a high value to increase the miller plate effect duration to slow the closing duration of the Q1 transistor. Nevertheless, the R4 value must be adapted to reach the $VRM_{VDDCORE-SR-LPLV-Stop}$ slew rate constraint.

Electrical parameters for Q1 MOSFET selection:

- N-Channel
- I_{DSS} << 2 µA (condition: Vds = 0.8 V, Vgs = 0 V)
- $V_{GS(threshold)}$ < 1.8 V (must be below PWR_LP I/O voltage; so below VDD voltage)
- I_D min > 2 µA
- V_{DS} > 0.8 V
- Crss recommended below 20 pF[(1)]

1. *To avoid energy transfers from PWR_LP signal to Q1 Gate to Drain (through Crss) to feedback node of IC during PWR_LP signal transition. This energy transfer can disturb the feedback node of IC making small overshoots and undershoots during PWR_LP signal transition for a few microseconds.*

6.3 VRM specification for V_{DDCPU} power domain with Run overdrive mode support

V_{DDCPU} is the STM32MP13x Arm® Cortex®-A7 CPU digital power domain. Therefore, significant current load transients occur on the V_{DDCPU} supply. Accordingly, special attention to MPU decoupling capacitor placement and layout must be done to minimize the power delivery network impedance (refer to [1]).

This section illustrates applications of Section 4.1 STM32MP13xD/F Run overdrive mode with DDR3L, boot flash, SD-card UHS-I, USB-A host, and USB-C PD and the Section 4.3 STM32MP13xD/F Run overdrive mode with lpDDR2/3, boot flash, USB-A host, and I/Os voltage at 1.8 V integrating the STM32MP13xD or the STM32MP13xF device having an enhanced consumer mission profile (refer to [6]). This profile allows the Arm® Cortex®-A7 CPU clock frequency run up to 1 GHz (refer to [5] for details and limitations).

Table 7. VRM specification for V_{DDCPU} power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
VRM_{VDDCPU}	Output voltage in Run mode	including line regulation, load regulation and temperature variation	1.21	1.25	1.29(1)	V
$VRM_{VDDCPU\text{-}OVRDRV}$	Output voltage in Run overdrive mode	including line regulation, load regulation and temperature variation	1.32	1.35	1.38	V
$VRM_{VDDCPU\text{-}RIPPLE}$	Output noise/ripple voltage	I_{OUT} = 1 mA to 500 mA f = 10 Hz to 5 MHz	-	-	30	mVp-p
VRM_{ICPU}	Rated output current		500	-	-	mA
$VRM_{VDDCPU\text{-}TRANS}$	Load transient regulation	I_{OUT} = 1 mA to 230 mA or 230 mA to 1 mA in 1 µs	-	-	+/-30(2)	mV
$VRM_{VDDCPU\text{-}SR\text{-}PU}$	Output voltage slew rate at power-up	VRM_{VDDCPU} from $V_{TH\_VDDCPU\text{-}Min}$ to $V_{DDCPU\text{-}Min}$	1.3 (3)	-	-	V/ms
$VRM_{VDDCPU\text{-}SR\text{-}OVRDRV}$	Output voltage slew rate Run/Run overdrive transition	VRM_{VDDCPU} from the rising edge of VSEL input of VRM to $V_{DDCPUOVRDRV\text{-}Min}$	1(4)	-	-	V/ms
$VRM_{VDDCPU\text{-}AD}$	Active output discharge	VRM_{VDDCPU} from the falling edge of VRM's EN input to 10% of VRM_{VDDCPU}	-	-	31(5)	ms

1. *The device is functional up to 1.38 V but using V_{DDCPU} > 1.29 V does not guarantee lifetime (refer to [6]) but simplifies the VRM design to manage a single V_{DDCPU} voltage at $VRM_{VDDCPU\text{-}OVRDRV}$ (refer to Section 5.3.1 Run overdrive mode low-cost alternative).*
2. *Voltage overshoot/undershoot caused by load transients must not go higher than VRM_{VDDCPU} + $VRM_{VDDCPU\text{-}TRANS}$ for a negative transient current, and lower than VRM_{VDDCPU} - $VRM_{VDDCPU\text{-}TRANS}$ for a positive current transient. Implicitly, output voltage noise/ripple ($VRM_{VDDCPU\text{-}RIPPLE}$) is included in the $VRM_{VDDCPU\text{-}TRANS}$ budget.*
3. *At power-up, once the VRM output voltage cross 0.95 V (STM32MP13's $V_{TH\_VDDCPU\ min}$), the VRM output voltage must be above VRM_{VDDCPU} min in less than 200 µs (STM32MP13's t_{VDDCPU_TEMPO} min). The VRM soft-start duration must be known to manage a very short LPLV-Stop2 use case by setting the MPU's PWRLP_TEMPO delay (refer to the warning note in Section 5.4.2 LPLV-Stop2 mode).*
4. *There is no specific constraint for the Run mode transition to Run overdrive mode voltage slew rate. Nevertheless, the rising duration (t_{rise}) must be known and set into the software to fulfill the sequence described in Section 5.3 STM32MP15xD and STM32MP15xF Run overdrive mode management.*
5. *V_{DDCPU} is turned OFF in LPLV-STOP2 mode in case of a crash. Accordingly, a regulator having an EN pin is needed to support those two cases. To support crash recovery management, the MPU's Reset Pulse Control must be enabled by setting the MRD timer with a value higher than $VRM_{VDDCPU\text{-}AD}$ (refer to Section 5.5 Crash recovery management).*

6.3.1 VRM_{VDDCPU} circuitry illustration for Run overdrive mode support with scalable 1.25 / 1.35 V

The VRM in Figure 19 has additional circuitry inserted into the feedback loop of the SMPS IC which allows it to control two output voltages This optional circuitry allows the switch of the V_{DDCPU} voltage between 1.25 V in Run mode and 1.35 V in Run overdrive mode.

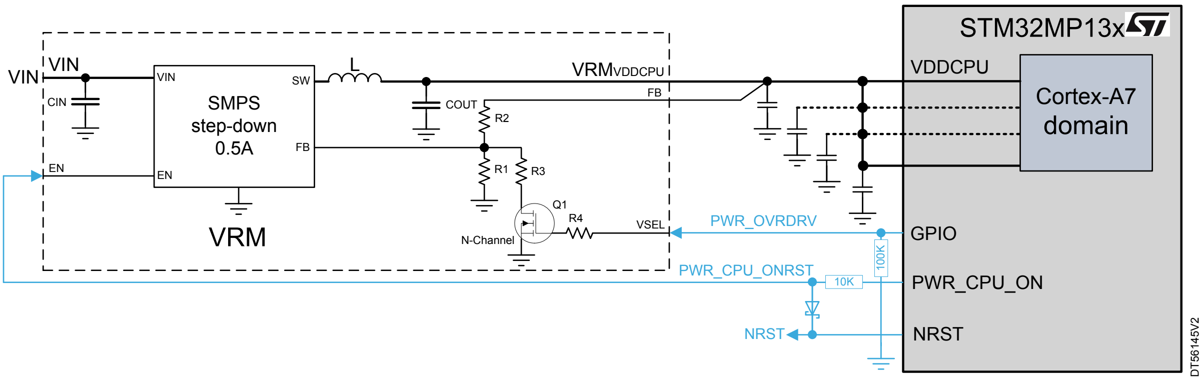


Figure 19. VRM$_{VDDCPU}$ with scalable 1.25 / 1.35 V circuitry

Table 8. VRM 1.25 / 1.35 V truth table

EN	VSEL	VRM$_{VDDCPU}$
0	-	0 V (OFF)
1	0	1.25 V
1	1	1.35 V

Vout (R1, R2, R3, R4) computation example:

Assumption: The step-down SMPS illustrated in Figure 19 has a feedback voltage equal to V_{BF} = 0.6 V

1. When VSEL = 0 (Run mode), the MOSFET Q1 is open and Q1 Drain node is floating. The output voltage VRM$_{VDDCPU}$ is minimum and is equal to:
   $VOUT_0$ = (R1 + R2) / R1 x V_{FB} = 1.25 V
2. When VSEL = 1 (RUN overdrive mode), the MOSFET Q1 is closed and Q1 Drain node is grounded (Q1 R_{DSON} neglected compared to R3 value). The output voltage VRM$_{VDDCPU}$ is maximum and is equal to:
   $VOUT_1$ = (R1//R3 + R2) / R1//R3 x V_{FB} = 1.35 V

R1 and R2 need to be selected first to reach $VOUT_0$ = 1.25 V output voltage. In this first step, choose an arbitrary value for R1 or R2.

In the second step, R3 must be selected to reach $VOUT_1$ = 1.35 V

R4 has a high value to increase the miller plate effect duration to slow the closing duration of the Q1 transistor. Nevertheless, the R4 value must be adapted to reach the VRM$_{VDDCORE-SR-LPLV-Stop}$ slew rate constraint.

Electrical parameters for Q1 MOSFET selection:

Same as Section 6.2.1 VRM$_{VDDCORE}$ circuitry illustration for LPLV-Stop2 support.

6.4 VRM specification for V_{DDCORE} and V_{DDCPU} merged

V_{DDCORE} and V_{DDCPU} are respectively the MPU digital power domain and the Arm® Cortex®-A7 CPU digital power domain. Therefore, significant current load transients can occur on the V_{DDCORE} and the V_{DDCPU} supplies at the same time. Accordingly, special attention to MPU decoupling capacitor placement and layout must be done to minimize the power delivery network impedance (refer to [1]).

This section illustrates applications of Section 4.2 STM32MP13x low-cost with DDR3L, boot flash, and USB-A host where V_{DDCORE} and V_{DDCPU} are merged at the PCB level, and they are power supplied from the same VRM.

In this section, V_{DDCORE} and $VRM_{VDDCORE}$ are referring to the VRM supplying both V_{DDCORE} and V_{DDCPU}

Table 9. VRM specification for V_{DDCORE} and V_{DDCPU} merged power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
$VRM_{VDDCORE}$	Output voltage in Run mode	including line regulation, load regulation and temperature variation	1.21	1.25	1.29	V
$VRM_{VDDCORE-LPLV-STOP}$	Output voltage in LPLV-Stop	VRM's VSEL input = 0	0.85	0.9	$VRM_{VDDCORE}$	V
$VRM_{VDDCORE-RIPPLE}$	Output noise/ripple voltage	I_{OUT} = 1 mA to 1 A f = 10 Hz to 5 MHz	-	-	30	mVp-p
VRM_{ICORE}	Rated output current		1000	-	-	mA
$VRM_{VDDCORE-TRANS}$	Load transient regulation	I_{OUT} = 2 mA to 350 mA or 350 mA to 2 mA in 1 µs	-	-	+/-30(1)	mV
$VRM_{VDDCORE-SR-PU}$	Output voltage slew rate at power-up	$VRM_{VDDCORE}$ from $V_{TH\_VDDCORE-Min}$ to $V_{DDCORE-Min}$	1.3(2)	-	-	V/ms
$VRM_{VDDCORE-SR-LPLV-Stop}$	Output voltage slew rate at LPLV-Stop exit	$VRM_{VDDCORE}$ from the rising edge of VRM's VSEL input to $V_{DDCORE-Min}$	1.55(3)	-	-	V/ms
$VRM_{VDDCORE-AD}$	Active output discharge	$VRM_{VDDCORE}$ from the falling edge of VRM's EN input to 10% of $VRM_{VDDCORE}$	-	-	31(4)	ms

1. *Voltage overshoot/undershoot caused by load transients must not go higher than $VRM_{VDDCORE}$ + $VRM_{VDDCORE-TRANS}$ for a negative transient current, and lower than $VRM_{VDDCORE}$ - $VRM_{VDDCORE-TRANS}$ for a positive current transient. Implicitly, output voltage noise/ripple ($VRM_{VDDCORE-RIPPLE}$) is included in the $VRM_{VDDCORE-TRANS}$ budget.*
2. *At power-up, once the VRM output voltage cross 0.95 V (STM32MP13's $V_{TH\_VDDCORE\ min}$), the VRM output voltage must be above $VRM_{VDDCORE}$ min in less than 200 µs (STM32MP13's $t_{VDDCORE\_TEMPO}$ min)*
3. *On the LPLV-Stop exit, the STM32MP13's PWR_LP signal goes from low to high. The VRM output voltage must rise from $VRM_{VDDCORE-LPLV-STOP\ min}$ to $VRMV_{VDDCORE\ min}$ in less than 234 µs (STM32MP13's $T_{SEL\_VDDCORETEMPO}$ min).*
4. *As V_{DDCORE} and V_{DDCPU} are turned OFF in Standby mode in case of a crash. Accordingly, a regulator having an EN pin is needed to support those two cases. For Standby mode, the MPU's POPL timer must be set with a value higher than $VRM_{VDDCORE-AD}$. For crash recovery management, the MPU's Reset Pulse Control must be enabled by setting the MRD timer with a value higher than $VRM_{VDDCORE-AD}$ (refer to Section 5.5 Crash recovery management).*

Note: If LPLV-Stop mode is not required, the $VRM_{VDDCORE-LPLV-STOP}$ and the $VRM_{VDDCORE-SR-LPLV-Stop}$ parameters must be ignored.

6.4.1 $VRM_{VDDCORE}$ circuitry illustration for LPLV-Stop support

The VRM in Figure 20 has additional circuitry inserted into the feedback loop of the SMPS IC which allows the control of two output voltages This optional circuitry allows the switch of the V_{DDCORE} / V_{DDCPU} voltages between 1.25 V in Run mode and 0.9 V in LPLV-Stop mode.

Figure 20. $VRM_{VDDCORE}$ with scalable 1.25 / 0.9 V circuitry (V_{DDCORE} and V_{DDCPU} merged)

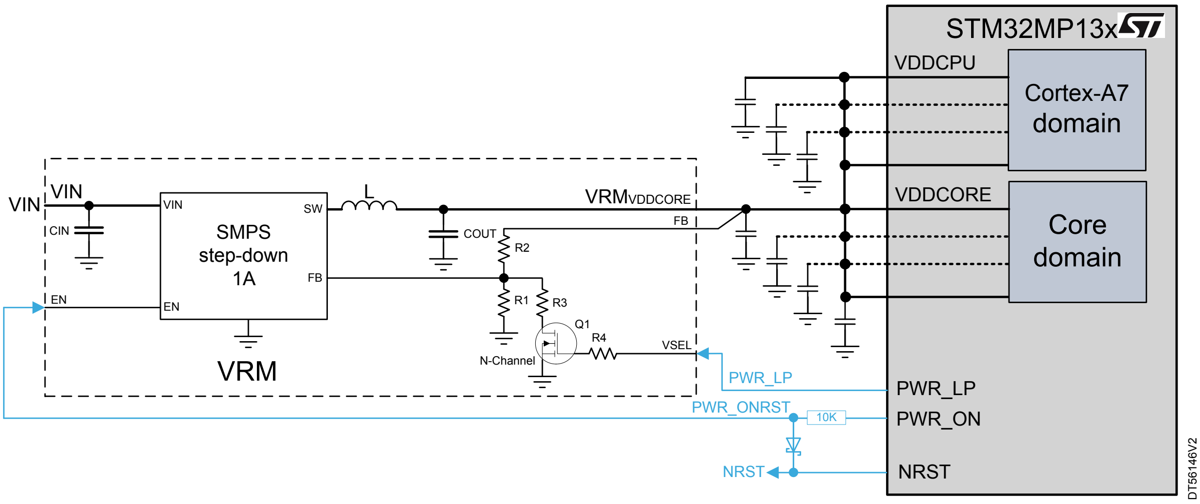


Table 10. VRM 1.25 / 0.9 V truth table (V_{DDCORE} and V_{DDCPU} merged)

EN	VSEL	$VRM_{VDDCORE}$
0	-	0 V (OFF)
1	0	0.9 V
1	1	1.25 V

Vout (R1, R2, R3, R4) computation example same as Section 6.2.1 $VRM_{VDDCORE}$ circuitry illustration for LPLV-Stop2 support.

Electrical parameters for Q1 MOSFET selection same as Section 6.2.1 $VRM_{VDDCORE}$ circuitry illustration for LPLV-Stop2 support.

6.5 VRM specification for VDDQ_DDR power domain

V_{DDQ_DDR} supplies the MPU's DDR IOs voltage interface. In addition to V_{DDQ_DDR}, the VRM must also supply the DDR ICs. Special attention on decoupling capacitor placement and layout must be done to minimize the power delivery network impedance for both the MPU VDDQ_DDR supply and DDR3L ICs. Refer to [1] and [8] for details.

This section illustrates applications of Section 4.1 STM32MP13xD/F Run overdrive mode with DDR3L, boot flash, SD-card UHS-I, USB-A host, and USB-C PD and the Section 4.2 STM32MP13x low-cost with DDR3L, boot flash, and USB-A host.

Assumptions:

- The DDR3L supply voltage is 1.283 V to 1.45 V and 1.35 V typ. (from JEDEC JESD79-3-1A)
- 1.425 V maximum DC value (from JEDEC JESD79-3-1A) = 1.35 V +5.5%
- VDDR max AC value = 25 mV (1.45 V – 1.425 V)
- Same value to be used for VDDR min AC
- 1.308 V minimum DC value (1.283 V + 0.025) = 1.35 V – 3.1%

Table 11. VRM specification for VDDQ_DDR and DDR3L IC power domain

Symbol	Parameter	Operating conditions	Min.	Typ	Max.	Unit
VRM_{VDDR}	Output voltage		-	1.35	-	V
$VRM_{VDDR-ACC}$	Output voltage accuracy	including line regulation, load regulation and temperature variation	-3 (-3.1)(1)	-	+3 (+5.5) (1)	%
$VRM_{VDDR-RIPPLE}$	Output noise/ripple voltage	I_{OUT} = 1 mA to 500 mA f = 10 Hz to 5 MHz	-	-	25	mVp-p
VRM_{IDDR}	Continuous output current		500	-	-	mA
$VRM_{VDDR-TRANS}$	Load transient regulation	I_{OUT} = 1 mA to 200 mA or 200 mA to 1 mA in 1 µs	-	-	+/-25(2)	mV
$VRM_{VDDR-SS}$	Soft start duration	Duration from EN pin rising (VRM_{VDDR} ~ 0) to 95% of VRM_{VDDR}	-	-	10(3)	ms
$VRM_{VDDR-AD}$	Active output discharge	VRM_{VDDR} from the falling edge of VRM's EN input to 10% of VRM_{VDDR}	-	-	31(4)	ms

1. *Values based on assumptions. Both are reduced to +/-3%*
2. *Voltage overshoot/undershoot caused by load transients must not be higher than VRM_{VDDR} + $VRM_{VDDR-TRANS}$ for a negative transient current and lower than VRM_{VDDR} - $VRM_{VDDR-TRANS}$ for a positive current transient. Implicitly, output voltage noise/ripple ($VRM_{VDDR-RIPPLE}$) is included in the $VRM_{VDDR-TRANS}$ budget.*
3. *10 ms is the reset value of the MPU EADLY timer. EADLY is a timer that is set by software to wait for the regulator voltage to be ready before entering the Run mode, as detailed in Section 5.2 Power-up/power-down sequence and reset management and Section 5.4 Low power mode management.*
4. *V_{DDQ_DDR} is turned OFF in Standby mode in case of a crash. Accordingly, a regulator having an EN pin is needed to support those two cases. For Standby mode, the MPU's POPL timer must be set with a value higher than $VRM_{VDDR-AD}$. For crash recovery management, the MPU's Reset Pulse Control must be enabled by setting the MRD timer with a value higher than $VRM_{VDDR-AD}$ (refer to Section 5.5 Crash recovery management).*

Revision history

Table 12. **Document revision history**

Date	Version	Changes
31-Jan-2023	1	Initial release.

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