Migrating from ST25DVxxK to ST25DVxxKC

Introduction

The purpose of this document is to explain the differences and the new features, and how to migrate from the ST25DVxxK to the new ST25DVxxKC dynamic tags.

This document concerns the devices listed in Table 1.

The ST25DVxxK and ST25DVxxKC are dual interface EEPROM devices, supporting I²C and ISO/IEC 15693 RF interfaces.

The ST25DVxxKC devices are the evolution of the ST25DVxxK, with high backward compatibility, along with new features:

- I²C programming speed increase
- I²C slave address selection
- I²C priority mode
- New GPO interrupts
- Improvement of RF commands

Features not mentioned in this document are to be considered identical between corresponding products.

Table 1. Applicable products

Type	Part number
ST25DVxxK	ST25DV04K ST25DV16K ST25DV64K
ST25DVxxKC	ST25DV04KC ST25DV16KC ST25DV64KC

1 Hardware considerations

ST25DVxxKC devices are pin-to-pin compatible with ST25DVxxK. They have the same packages, pinout, tuning capacitance and power supply.

Furthermore, data cycling, data retention and operating temperature ranges are identical between the ST25DVxxK and ST25DVxxKC products.

Therefore, ST25DVxxK can be replaced by ST25DVxxKC without any hardware changes.

2 RF operation

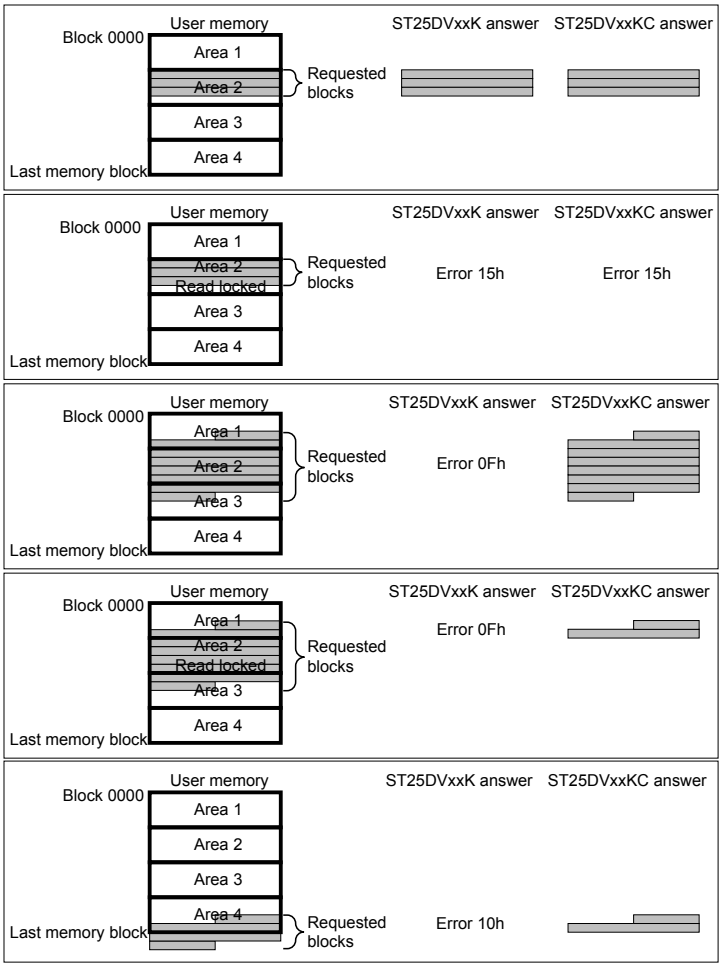
2.1 Read multiple blocks commands family

When reading multiple blocks, ST25DVxxK and ST25DVxxKC devices may give different results, depending on the required blocks:

- ST25DVxxK return blocks only if they are all readable, return an error if all requested blocks are not in the same area or if some requested data is out of memory
- ST25DVxxKC return all readable blocks until they reach an unreadable block, return an error only if no block is readable.

The difference in the responses is shown in the following figure.

Figure 1. Read multiple block differences between ST25DVxxK and ST25DVxxKC



This behavioral difference concerns four commands:

- Read multiple blocks (command code 23h)
- Extended read multiple blocks (command code 33h)
- Fast read multiple blocks (command code C3h)
- Fast extended read multiple blocks (command code C5h)

2.2 RF management

ST25DVxxK products have three RF modes of operation:

- Normal mode
- RF disable mode
- RF sleep mode

ST25DVxxKC products additionally feature RF off mode.

ST25DVxxK and ST25DVxxKC devices have the same RF disable and RF sleep modes. They are also entered and exited in the same way.

The differences between RF off mode and RF sleep mode in ST25DVxxKC devices are:

- Entry and exit through the special commands "I²C RFSwitchOff" and "I²C RFSwitchOn" (instead of writing on a dynamic register). See Section 3.2 I²C priority for more details.
- When in RF off mode, all RF security sessions are closed and ISO15693 state back to reset to ready while in RF sleep mode they are all maintained.

The RF off mode is switched on immediately, whatever the RF activity (except during a write RF).

An interrupt on the GPO pin (I²C_RF_OFF) can also be triggered on RF off activation, as explained in Section 4.2 I²C_RF_OFF interrupt.

To support the RF off mode, a new bit (b2, RF_OFF) has been added in the RF_MNGT_Dyn register. This bit is read-only and is modified only by the special “I²C RFSwitchOff” and “I²C RFSwitchOn” commands.

See Section 5 System configuration for more details.

3 I²C operation

3.1 I²C slave address selection

The ST25DVxxK products have fixed I²C slave devices addresses. These are configurable on ST25DVxxKC products.

As shown in Table 2 ST25DVxxK products have two different I²C slave device addresses:

Table 2. ST25DVxxK I²C slave device addresses

ST25DVxxK function	I²C device code				E2	E1	E0	R/W
	b7	b6	b5	b4	b3	b2	b1	b0
User memory	1	0	1	0	0	1	1	0/1
System memory					1			

ST25DVxxKC have four different I²C slave device addresses for four different functions. On top of this, the I²C device code bits and the E0 bit are programmable:

Table 3. ST25DVxxKC I²C slave device addresses

ST25DVxxKC function	I²C device code				E2	E1	E0	R/W
	b7	b6	b5	b4	b3	b2	b1	b0
User memory	I²C_DEVICE_CODE[3:0]				0	1	I²C_E0	0/1
System memory					1			
I²C RFSwitchON					0	0		0
I²C RFSwitchOFF					1			

I²C_DEVICE_CODE[3:0] and I²C_E0 can be programmed by writing in the I²C_CFG configuration register at system address 000Eh from I²C only.

See Section 5 System configuration for description of the I²C_CFG register.

Factory value of ST25DVxxKC I2C slave address for user memory and system memory access is the same of ST25DVxxK.

3.2 I²C priority

ST25DVxxKC products allow the user to stop current RF commands so that an I²C command can be executed immediately. ST25DVxxK products do not permit this interruption. This makes possible to prioritize the I²C interface over the RF interface at any time.

ST25DVxxKC accept special I²C commands “I²C RFSwitchOff” to set RF in off mode immediately and “I²C RFSwitchOn” to exit RF off mode.

ST25DVxxKC also provide an interrupt on the GPO pin (I²C_RF_OFF) to signal to the I²C master when the I²C gains priority (see Section 4.2 I²C_RF_OFF interrupt).

Application notes AN5262 and AN5624 (available on www.st.com) explain in detail the arbitration process between I²C and RF interface for ST25DVxxK, and ST25DVxxKC, respectively.

3.3 I²C write operation

In the ST25DVxxKC devices the programming speed of the EEPROM has been improved when writing from the I²C interface, resulting in an improvement of a factor four.

It is still possible to write 1 to 256 bytes in a single I²C command, but the way data are programmed in the EEPROM is different, leading to this increase of write speed.

In ST25DVxxK, data can be programmed in EEPROM by rows of 4 bytes in t_W (programming time for a row)

In ST25DVxxKC, data can be progrmamed in EEPROM by rows of 16 bytes in t_W.

The t_W, does not change between the two versions, and is around 5 ms depending on temperature (see ST25DVxxK and ST25DVxxKC datasheets for exact t_W values).

EEPROM programming cycle can be calculated using following C code, depending on I²C write start address and number of bytes to be written (max 256 bytes):

- `ST25DVxxK programming cycle = tw*(((start_address+nb_bytes_to_write-1)>>2)-(start_address>>2)+1);`
- `ST25DVxxKC programming cycle = tw*(((start_address+nb_bytes_to_write-1)>>4)-(start_address>>4)+1);`

ST25DVxxKC also provide an interrupt on the GPO pin (I²C_WRITE) at the completion of the I²C EEPROM programming cycle to inform the I²C master that the device is ready to receive a new I²C command (see Section 4.1 I²C_WRITE interrupt).

The following tables (where B indicates byte) show examples of difference in programming time when writing in EEPROM.

Table 4. ST25DVxxK: four rows to be programmed, 5 ms per row (20 ms total programming time)

I²C command: write 16 bytes starting at user memory address 0000h

I²C memory	0	1	2	3
0000h	B00	B01	B02	B03
0004h	B04	B05	B06	B07
0008h	B08	B09	B10	B11
000Ch	B12	B13	B14	B15
0010h	-	-	-	-
0014h	-	-	-	-
….	-	-	-	-

Table 5. ST25DVxxKC: one row to be programmed, 5 ms per row (5 ms programming time)

I²C command: write 16 bytes starting at user memory address 0000h

I²C memory	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000h	B00	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15
0010h	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0020h	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
….	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 6. ST25DVxxK: three rows to be programmed, 5 ms per row (15 ms total programming time)

I²C command: write 8 bytes starting at user memory address 000Ah

I²C memory	0	1	2	3
0000h	-	-	-	-
0004h	-	-	-	-
0008h	-	-	B00	B01
000Ch	B02	B03	B04	B05
0010h	B06	B07	-	-
0014h	-	-	-	-
….	-	-	-	-

Table 7. ST25DVxxKC: two rows to be programmed, 5 ms per row (10 ms programming time)

I²C command: write 8 bytes starting at user memory address 000Ah

I²C memory	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000h	-	-	-	-	-	-	-	-	-	-	B00	B01	B02	B03	B04	B05
0010h	B06	B07	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0020h	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
….	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

It is recommended to align I²C writes in user memory on address bit 2 (4-byte lines) in ST25DVxxK and on address bit 4 (16-byte lines) in ST25DVxxKC if write performance is important for the application.

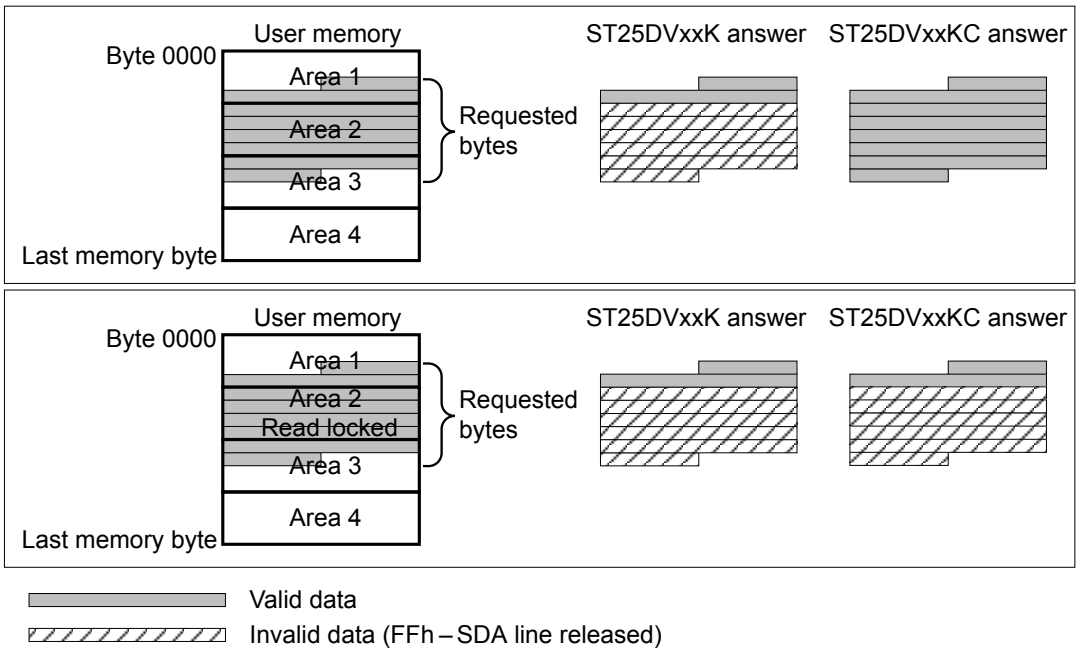
3.4 I²C read operation

When reading multiple bytes (I²C read sequential) the ST25DVxxK and ST25DVxxKC products may give different results:

- ST25DVxxK return all readable bytes, do not return data if next byte address is not in the same area or is out of memory (SDA line is released resulting in FFh value).
- ST25DVxxKC return all readable bytes, do not return data if next byte address is not readable (SDA line is released resulting in FFh value).

Figure 2 shows the difference.

Figure 2. I²C read sequential bytes differences between ST25DVxxK and ST25DVxxKC

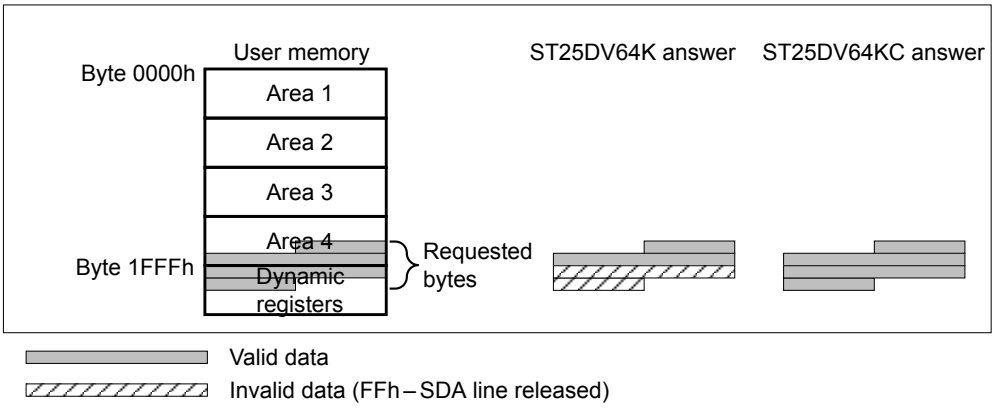


In ST25DV64KC, the end of the user memory (address 1FFFh) is followed by the dynamic register address (2000h) and the FTM mailbox (address 2008h). Therefore, if a sequential I²C read, starts before the end of the user memory, continues to read after the end of the user memory, it returns the contents of the dynamic registers. If the I²C sequential read continues reading after address 2008h, and if mailbox is enabled and not empty, mailbox content is returned as well.

In ST25DV64K, if an I²C read sequential starts before end of user memory, continues reading after end of user memory, it returns no data (SDA line is released and FFh is read).

The Figure 3 shows this difference:

Figure 3. I²C read sequential bytes differences when reaching end of user memory (in ST25DV64K)



4 GPO

ST25DVxxKC provide the same interrupts as ST25DVxxK products, but they also have two new interrupts that can be triggered on I²C events.

Therefore, the configuration of GPO interrupt is slightly different.

4.1 I²C_WRITE interrupt

The I²C_WRITE GPO interrupt is new in ST25DVxxKC and, if enabled, permits to emit a pulse on the GPO pin at the end of the I²C EEPROM programming cycle.

For more details on this specific interrupt, see the related datasheet section.

4.2 I²C_RF_OFF interrupt

The I²C_RF_OFF GPO interrupt is new in ST25DVxxKC and, if enabled, permits to emit a pulse on the GPO pin when RF is set OFF following an I²C RFSiwtchOff command.

For more details on this specific interrupt, see the related datasheet section.

4.3 GPO configuration

Due to the increased number of possible interrupts, the static configuration register of the ST25DVxxKC is now on two bytes (vs. one byte in ST25DVxxK).

This new static configuration register groups the enable bits for all interrupts and also the IT_TIME setting (in ST25DVxxK is in a separate configuration register).

See Section 5 System configuration for description of the GPO1 and GPO2 registers.

ST25DVxxK and ST25DVxxKC have the same dynamic GPO_CTRL_Dyn and IT_STS_Dyn registers.

5 System configuration

5.1 Device identification

IC_REF and UID are different in ST25DVxxK and ST25DVxxKC products.

5.1.1 IC_REF

Table 8. ST25DVxxK IC_REF content

Bit	Name	Function	Factory value
b7-b0	IC_REF	ISO/IEC 15693 IC reference	• ST25DV04K-IE: 24h • ST25DV16K-IE: 26h • ST25DV64K-IE: 26h • ST25DV04K-JF: 24h • ST25DV16K-JF: 26h • ST25DV64K-JF: 26h

Table 9. ST25DVxxKC IC_REF content

Bit	Name	Function	Factory value
b7-b0	IC_REF	ISO/IEC 15693 IC reference	• ST25DV04KC-IE: 50h • ST25DV16KC-IE: 51h • ST25DV64KC-IE: 51h • ST25DV04KC-JF: 50h • ST25DV16KC-JF: 51h • ST25DV64KC-JF: 51h

5.1.2 UID

Table 10. ST25DVxxK UID

UID							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
E0h	02h	• ST25DV04K-IE: 24h • ST25DV16K-IE: 26h • ST25DV64K-IE: 26h • ST25DV04K-JF: 25h • ST25DV16K-JF: 27h • ST25DV64K-JF: 27h	Unique serial number				

Table 11. ST25DVxxKC UID

UID							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
E0h	02h	• ST25DV04KC-IE: 50h • ST25DV16KC-IE: 51h • ST25DV64KC-IE: 51h • ST25DV04KC-JF: 52h • ST25DV16KC-JF: 53h • ST25DV64KC-JF: 53h	Unique serial number				

5.2 Static configuration registers

In Table 12 the differences of the static configuration registers between ST25DVxxK and ST25DVxxKC are in bold.

Table 12. System configuration memory map comparison

RF	I²C		ST25DVxxK	ST25DVxxKC
Address	Device select	Address		
00h	E2 = 1, E1 = 1	0000h	GPO	**GPO1**
01h	E2 = 1, E1 = 1	0001h	IT_TIME	**GPO2**
02h	E2 = 1, E1 = 1	0002h	EH_MODE	EH_MODE
03h	E2 = 1, E1 = 1	0003h	RF_MNGT	RF_MNGT
04h	E2 = 1, E1 = 1	0004h	RFA1SS	RFA1SS
05h	E2 = 1, E1 = 1	0005h	ENDA1	ENDA1
06h	E2 = 1, E1 = 1	0006h	RFA2SS	RFA2SS
07h	E2 = 1, E1 = 1	0007h	ENDA2	ENDA2
08h	E2 = 1, E1 = 1	0008h	RFA3SS	RFA3SS
09h	E2 = 1, E1 = 1	0009h	ENDA3	ENDA3
0Ah	E2 = 1, E1 = 1	000Ah	RFA4SS	RFA4SS
-	E2 = 1, E1 = 1	000Bh	I²CSS	I²CSS
-	E2 = 1, E1 = 1	000Ch	LOCK_CCFILE	LOCK_CCFILE
0Dh	E2 = 1, E1 = 1	000Dh	MB_MODE	**FTM**
0Eh	E2 = 1, E1 = 1	000Eh	MB_WDG	**I2C_CFG**
0Fh	E2 = 1, E1 = 1	000Fh	LOCK_CFG	LOCK_CFG

5.2.1 GPO vs GPO1 configuration register

Table 13. ST25DVxxK GPO configuration register access

RF access		I²C access	
Command	Type	Address	Type
Read configuration (cmd code A0h) @00h Write configuration (cmd code A1h) @00h	• R always • W if RF configuration security session is open and configuration not locked	E2 = 0, 0000h	• R always • W if I²C security session is open

Table 14. ST25DVxxK GPO configuration register content

Bit	Name	Function	Factory value
b0	RF_USER_EN	• 0: disabled • 1: GPO output level is controlled by manage GPO command (set/reset)	0b
b1	RF_ACTIVITY_EN	• 0: disabled • 1: GPO output level changes from RF command EOF to response EOF	0b
b2	RF_INTERRUPT_EN	• 0: disabled • 1: GPO output level is controlled by manage GPO command (pulse).	0b
b3	FIELD_CHANGE_EN	• 0: disabled • 1: A pulse is emitted on GPO, when RF field appears or disappears.	1b

Bit	Name	Function	Factory value
b4	RF_PUT_MSG_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF write message command.	0b
b5	RF_GET_MSG_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF read message command if end of message has been reached.	0b
b6	RF_WRITE_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF write operation in EEPROM.	0b
b7	GPO_EN	• 0: GPO output is disabled. GPO is High-Z (open drain version) or is tied to ground (CMOS version). • 1: GPO output is enabled. GPO outputs enabled interrupts	1b

Table 15. ST25DVxxKC GPO1 configuration register access

RF access		I²C access	
Command	**Type**	**Address**	**Type**
Read configuration (cmd code A0h) @00h Write configuration (cmd code A1h) @00h	• R always • W if RF configuration security session is open and configuration not locked	E2 = 0, E1 = 1, 0000h	• R always • W if I²C security session is open

Table 16. ST25DVxxKC GPO1 configuration register content

Bit	Name	Function	Factory value
b0	GPO_EN	• 0: GPO output is disabled. GPO is high-Z (open drain version) or is tied to ground (CMOS version). • 1: GPO output is enabled. GPO outputs enabled interrupts	1b
b1	RF_USER_EN	• 0: disabled • 1: GPO output level is controlled by manage GPO command (set/reset).	0b
b2	RF_ACTIVITY_EN	• 0: disabled • 1: GPO output level changes from RF command EOF to response EOF.	0b
b3	RF_INTERRUPT_EN	• 0: disabled • 1: GPO output level is controlled by manage GPO command (pulse).	0b
b4	FIELD_CHANGE_EN	• 0: disabled • 1: A pulse is emitted on GPO, when RF field appears or disappears.	1b
b5	RF_PUT_MSG_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF write message command.	0b
b6	RF_GET_MSG_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF read message command if end of message has been reached.	0b
b7	RF_WRITE_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF write operation in EEPROM.	0b

5.2.2 IT_TIME vs GPO2 configuration register

Table 17. ST25DVxxK IT_TIME configuration register access

RF access		I²C access	
Command	**Type**	**Address**	**Type**
Read configuration (cmd code A0h) @01h Write configuration (cmd code A1h) @01h	• R always • W if RF configuration security session is open and configuration not locked	E2 = 0, 0001h	• R always • W if I²C security session is open

Table 18. ST25DVxxK IT_TIME configuration register content

Bit	Name	Function	Factory value
b2-b0	IT_TIME	Pulse duration = 301 µs - IT_TIME x 37.65 µs ± 2 µs	011b
b7-b3	RFU		00000b

Table 19. ST25DVxxKC GPO2 configuration register access

RF access		I²C access	
Command	**Type**	**Address**	**Type**
Read configuration (cmd code A0h) @01h Write configuration (cmd code A1h) @01h	• R always • W if RF configuration security session is open and configuration not locked	E2 = 0, E1 = 1, 0001h	• R always • W if I²C security session is open

Table 20. ST25DVxxKC GPO2 configuration register content

Bit	Name	Function	Factory value
b0	I²C_WRITE_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid I²C write operation in EEPROM	0b
b1	I²C_RF_OFF_EN	• 0: disabled • 1: A pulse is emitted on GPO when I²C host has successfully switched the RF off	0b
b4-b2	IT_TIME	Pulse duration = 301 µs - IT_TIME x 37.65 µs ± 2 µs	011b
b7-b5	RFU		000b

5.2.3 MB_MODE vs FTM configuration register

Table 21. ST25DVxxK MB_MODE configuration register access

RF access		I²C access	
Command	**Type**	**Address**	**Type**
Read configuration (cmd code A0h) @0Dh Write configuration (cmd code A1h) @0Dh	• R always • W if RF configuration security session is open and configuration not locked	E2 = 0, 000Dh	• R always • W if I²C security session is open

Table 22. **ST25DVxxK MB_MODE configuration register content**

Bit	Name	Function	Factory value
b0	MB_MODE	• 0: Enabling fast transfer mode is forbidden. • 1: Enabling fast transfer mode is authorized.	0b
b7-b1	RFU		0000000b

Table 23. **ST25DVxxKC FTM configuration register access**

RF access		I²C access	
Command	Type	Address	Type
Read configuration (cmd code A0h) @0Dh Write configuration (cmd code A1h) @0Dh	• R always • W if RF configuration security session is open and configuration not locked	E2 = 0, E1 = 1, 000Dh	• R always • W if I²C security session is open

Table 24. **ST25DVxxKC FTM configuration register content**

Bit	Name	Function	Factory value
b0	MB_MODE	• 0: Enabling fast transfer mode is forbidden. • 1: Enabling fast transfer mode is authorized.	0b
b3-b1	MB_WDG	• Watchdog duration = 2 (MB_WDG-1) x 30 ms ± 6 ms • If MD_WDG = 0, then watchdog duration is infinite	000b
b7-b4	RFU		0000b

5.2.4 MB_WDG vs I²C_CFG configuration register

Table 25. **ST25DVxxK MB_WDG configuration register access**

RF access		I²C access	
Command	Type	Address	Type
Read configuration (cmd code A0h) @0Eh Write configuration (cmd code A1h) @0Eh	• R always • W if RF configuration security session is open and configuration not locked	E2 = 0, 000Eh	• R always • W if I²C security session is open

Table 26. **ST25DVxxK MB_WDG configuration register content**

Bit	Name	Function	Factory value
b2-b0	MB_WDG	• Watch dog duration = 2 (MB_WDG-1) x 30 ms ± 6 ms • If MD_WDG = 0, then watchdog duration is infinite	111b
b7-b3	RFU		00000b

Table 27. **ST25DVxxKC I²C_CFG configuration register access**

RF access		I²C access	
Command	Type	Address	Type
No access		E2 = 0, E1 = 1, 000Eh	• R always • W if I²C security session is open

Table 28. **ST25DVxxKC I²C_CFG configuration register content**

Bit	Name	Function	Factory value
b3-b0	I²C_DEVICE_CODE	Device code of I²C slave address	1010b
b4	I²C_E0	E0 bit of I²C slave address	1b
b5	I²C_RF_SWITCHOFF_EN	I²C RFSwitchOFF function enable	0b
b7-b6	RFU		00b

5.3 Dynamic registers

In Table 29 the differences of the dynamic configuration registers between ST25DVxxK and ST25DVxxKC are in bold.

Table 29. **Dynamic registers memory map comparison**

RF	I²C		ST25DVxxK	ST25DVxxKC
Address	Device select	Address		
00h	E2 = 0, E1 = 1	2000h	GPO_CTRL_Dyn	**GPO_CTRL_Dyn**
-	E2 = 0, E1 = 1	2001h	-	-
02h	E2 = 0, E1 = 1	2002h	EH_CTRL_Dyn	EH_CTRL_Dyn
-	E2 = 0, E1 = 1	2003h	RF_MNGT_Dyn	**RF_MNGT_Dyn**
-	E2 = 0, E1 = 1	2004h	I2C_SSO_Dyn	I2C_SSO_Dyn
-	E2 = 0, E1 = 1	2005h	IT_STS_Dyn	IT_STS_Dyn
0Dh	E2 = 0, E1 = 1	2006h	MB_CTRL_Dyn	MB_CTRL_Dyn
-	E2 = 0, E1 = 1	2007h	MB_LEN_Dyn	MB_LEN_Dyn

5.3.1 GPO_CTRL_Dyn configuration register

Table 30. ST25DVxxK GPO_CTRL_Dyn register access

RF access		I²C access	
Command	Type	Address	Type
Read dynamic configuration (cmd code ADh) @00h Fast read dynamic configuration (cmd code CDh) @00h	Read only	E2 = 0, 2000h	b7-b1: RO b0: R always, W always

Table 31. ST25DVxxK GPO_CTRL_Dyn register content

Bit	Name	Function	Factory value
b0	RF_USER_EN	• 0: disabled • 1: GPO output level is controlled by manage GPO command (set/reset).	0b
b1	RF_ACTIVITY_EN	• 0: disabled • 1: GPO output level changes from RF command EOF to response EOF.	0b
b2	RF_INTERRUPT_EN	• 0: disabled • 1: GPO output level is controlled by manage GPO command (pulse).	0b
b3	FIELD_CHANGE_EN	• 0: disabled • 1: A pulse is emitted on GPO, when RF field appears or disappears.	1b
b4	RF_PUT_MSG_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF write message command.	0b
b5	RF_GET_MSG_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF read message command if end of message has been reached.	0b
b6	RF_WRITE_EN	• 0: disabled • 1: A pulse is emitted on GPO at completion of valid RF write operation in EEPROM.	0b
b7	GPO_EN	• 0: GPO output is disabled. GPO is High-Z (open drain version) or is tied to ground (CMOS version). • 1: GPO output is enabled. GPO outputs enabled interrupts	1b

Table 32. ST25DVxxKC GPO_CTRL_Dyn register access

RF access		I²C access	
Command	Type	Address	Type
Read dynamic configuration (cmd code ADh) @00h Fast read dynamic configuration (cmd code CDh) @00h	Read only	E2 = 0, 2000h	b6-b0: RO b7 : R always, W always

Table 33. ST25DVxxKC GPO_CTRL_Dyn register content

Bit	Name	Function	Factory setting
b0	GPO_EN	• 0: GPO output is disabled. GPO is High-Z (open drain version) or is tied to ground (CMOS version). • 1: GPO output is enabled. GPO outputs enabled interrupts.	1b
b7-b1	RFU		0000000b

5.3.2 RF_MNGT_Dyn configuration register

Table 34. ST25DVxxK RF_MNGT_Dyn register access

RF access		I²C access	
Command	Type	Address	Type
No access		E2 = 0, 2003h	• R always • W always

Table 35. ST25DVxxK RF_MNGT_Dyn register content

Bit	Name	Function	Factory setting
b0	RF_DISABLE	• 0: RF mode is defined by RF_OFF and RF_SLEEP bits • 1: RF commands not executed (error 0Fh returned)	0b
b1	RF_SLEEP	• 0: RF mode is defined by RF_OFF and RF_DISABLE bits • 1: RF communication disabled (ST25DVxxKC remains silent)	0b
b7-b2	RFU		0000000b

Table 36. ST25DVxxKC RF_MNGT_Dyn register access

RF access		I²C access	
Command	Type	Address	Type
No access		E2 = 0, E1 = 1, 2003h	• R always • W always

Table 37. ST25DVxxKC RF_MNGT_Dyn register content

Bit	Name	Function	Factory setting
b0	RF_DISABLE	• 0: RF mode is defined by RF_OFF and RF_SLEEP bits • 1: RF commands not executed (error 0Fh returned)	0b
b1	RF_SLEEP	• 0: RF mode is defined by RF_OFF and RF_DISABLE bits • 1: RF communication disabled (ST25DVxxKC remains silent)	0b
b2	RF_OFF	• 0: RF mode is defined by RF_SLEEP and RF_DISABLE bits • 1: RF is reset, and communication disabled (RF security sessions and ISO15693 state are reset and ST25DVxxKC remains silent)	0b
b7-b3	RFU		0000000b

Revision history

Table 38. **Document revision history**

Date	Version	Changes
23-Jun-2021	1	Initial release.
25-Jul-2022	2	Updated: • Table 3. ST25DVxxKC I²C slave device addresses

Contents

1 **Hardware considerations** 2
2 **RF operation** 3
2.1 Read multiple blocks commands family 3
2.2 RF management 4
3 **I²C operation** 5
3.1 I²C slave address selection 5
3.2 I²C priority 5
3.3 I²C write operation 5
3.4 I²C read operation 7
4 **GPO** 9
4.1 I²C_WRITE interrupt 9
4.2 I²C_RF_OFF interrupt 9
4.3 GPO configuration 9
5 **System configuration** 10
5.1 Device identification 10
5.1.1 IC_REF 10
5.1.2 UID 10
5.2 Static configuration registers 11
5.2.1 GPO vs GPO1 configuration register 11
5.2.2 IT_TIME vs GPO2 configuration register 13
5.2.3 MB_MODE vs FTM configuration register 13
5.2.4 MB_WDG vs I²C_CFG configuration register 14
5.3 Dynamic registers 15
5.3.1 GPO_CTRL_Dyn configuration register 16
5.3.2 RF_MNGT_Dyn configuration register 17
Revision history 18
List of tables 20
List of figures 21

List of tables

Table 1. Applicable products . . . 1
Table 2. ST25DVxxK I²C slave device addresses . . . 5
Table 3. ST25DVxxKC I²C slave device addresses . . . 5
Table 4. ST25DVxxK: four rows to be programmed, 5 ms per row (20 ms total programming time) . . . 6
Table 5. ST25DVxxKC: one row to be programmed, 5 ms per row (5 ms programming time) . . . 6
Table 6. ST25DVxxK: three rows to be programmed, 5 ms per row (15 ms total programming time) . . . 7
Table 7. ST25DVxxKC: two rows to be programmed, 5 ms per row (10 ms programming time) . . . 7
Table 8. ST25DVxxK IC_REF content . . . 10
Table 9. ST25DVxxKC IC_REF content . . . 10
Table 10. ST25DVxxK UID . . . 10
Table 11. ST25DVxxKC UID . . . 10
Table 12. System configuration memory map comparison . . . 11
Table 13. ST25DVxxK GPO configuration register access . . . 11
Table 14. ST25DVxxK GPO configuration register content . . . 11
Table 15. ST25DVxxKC GPO1 configuration register access . . . 12
Table 16. ST25DVxxKC GPO1 configuration register content . . . 12
Table 17. ST25DVxxK IT_TIME configuration register access . . . 13
Table 18. ST25DVxxK IT_TIME configuration register content . . . 13
Table 19. ST25DVxxKC GPO2 configuration register access . . . 13
Table 20. ST25DVxxKC GPO2 configuration register content . . . 13
Table 21. ST25DVxxK MB_MODE configuration register access . . . 13
Table 22. ST25DVxxK MB_MODE configuration register content . . . 14
Table 23. ST25DVxxKC FTM configuration register access . . . 14
Table 24. ST25DVxxKC FTM configuration register content . . . 14
Table 25. ST25DVxxK MB_WDG configuration register access . . . 14
Table 26. ST25DVxxK MB_WDG configuration register content . . . 14
Table 27. ST25DVxxKC I²C_CFG configuration register access . . . 14
Table 28. ST25DVxxKC I²C_CFG configuration register content . . . 15
Table 29. Dynamic registers memory map comparison . . . 15
Table 30. ST25DVxxK GPO_CTRL_Dyn register access . . . 16
Table 31. ST25DVxxK GPO_CTRL_Dyn register content . . . 16
Table 32. ST25DVxxKC GPO_CTRL_Dyn register access . . . 16
Table 33. ST25DVxxKC GPO_CTRL_Dyn register content . . . 16
Table 34. ST25DVxxK RF_MNGT_Dyn register access . . . 17
Table 35. ST25DVxxK RF_MNGT_Dyn register content . . . 17
Table 36. ST25DVxxKC RF_MNGT_Dyn register access . . . 17
Table 37. ST25DVxxKC RF_MNGT_Dyn register content . . . 17
Table 38. Document revision history . . . 18

List of figures

Figure 1. Read multiple block differences between ST25DVxxK and ST25DVxxKC 3
Figure 2. I²C read sequential bytes differences between ST25DVxxK and ST25DVxxKC 8
Figure 3. I²C read sequential bytes differences when reaching end of user memory (in ST25DV64K) 8