AN5643
Application note

Migrating from M24LRxxE-R to ST25DVxxKC

Introduction

The M24LRxxE-R and ST25DVxxKC are dual EEPROM memory devices, supporting I^2C and ISO/IEC 15693 RF interfaces.

The ST25DVxxKC is a natural evolution of the M24LRxxE-R, proposing improved performance and new advanced features.

The purpose of this document is to explain how to migrate from the M24LRxxE-R dynamic tag to the new ST25DVxxKC dynamic tag.

New ST25DVxxKC features such as fast transfer mode, low power mode and RF management are not discussed in this document.

Table 1. Applicable products

Type	Part number
Dual interface EEPROM	M24LR04E-R M24LR16E-R M24LR64E-R ST25DV04KC ST25DV16KC ST25DV64KC

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1 Acronyms and notational conventions

Table 2. List of acronyms

Acronym	Definition
CC File	Capability container file as defined by the NFC Forum
EEPROM	Electrically-erasable programmable read-only memory
EOF	End of frame
I^2C	Inter-integrated circuit
IC	Integrated circuit
IC Ref	Integrated circuit reference
ISO	International organization for standardization
IEC	International electrotechnical commission
NFC	Near field communication standard defined by the NFC Forum
RF	Radio frequency
SOF	Start of frame
UID	Unique identifier
VCD	Vicinity coupling device
VICC	Vicinity integrated circuit card

1.1 Conventions

The following conventions and notations apply in this document unless otherwise stated.

1.1.1 Product family denomination

Product families are abbreviated as follows:

- **M24LR** refers to the complete family of products: M24LR04E-R, M24LR16E-R and M24LR64E-R.
- **ST25DVxxKC** refers to the complete family of products: ST25DV04KC-IE, ST25DV16KC-IE, ST25DV64KC-IE, ST25DV04KC-JF, ST25DV16KC-JF and ST25DV64KC-JF.
- **ST25DVxxKC-IE** refers to ST25DV04KC-IE, ST25DV16KC-IE and ST25DV64KC-IE devices.
- **ST25DVxxKC-JF** refers to ST25DV04KC-JF, ST25DV16KC-JF and ST25DV64KC-JF devices.

1.1.2 Binary number representation

Binary numbers are represented by strings of 0 and 1 digits, with the most significant bit (MSB) on the left, the least significant bit (LSB) on the right, and a ‘b’ suffix added at the end.

Example: 11110101b

1.1.3 Hexadecimal number representation

Hexadecimal numbers are represented by strings of numbers from 0 to 9 and letters from A to F, and an ‘h’ suffix added at the end. The most significant byte (MSB) is shown on the left and the least significant byte (LSB) on the right.

Example: F5h

1.1.4 Decimal number representation

Decimal numbers are represented without any trailing character.

Example: 245

2 M24LR and ST25DVxxKC product feature comparison

Table 3 lists the features of M24LR and ST25DVxxKC products. (For full details, refer also to the M24LR *[1]*, *[2]*, *[3]* and ST25DVxxKC *[4]* product datasheets.)

Table 3. Feature comparison summary

Feature	M24LR	ST25DVxxKC
Pinout	Same pinout	
Packages	SO8	
	TSSPO8	
	UFDFPN8	
	Wafer	NA
	NA	UFDFPN12 (ST25DVxxKC-JF only)
Tuning capacitance	27.5 pF	28.5 pF(1)
Wired power supply	1.8 V to 5.5 V	
I^2C interface	400 kHz maximum	1 MHz maximum
	Fixed device select address	Programmable device select address
	Current and random address byte read	
	Current and random address sequential read	
	Random address byte write	
	Page write 4 bytes maximum	Multiple write 256 bytes maximum (internally 16-byte page write)
	32-bit I^2C password special commands	64-bit I^2C password special commands

Table 3. Feature comparison summary (continued)

Feature	M24LR	ST25DVxxKC
Contactless interface (RF)	ISO/IEC 15693	Based on ISO/IEC 15693 (revision 2019) and NFC Forum Type 5 tag
	M24LR16E-R and M24LR64E-R only: Non ISO 15693 compliant commands for read and write block-memory access	NA
	M24LR16E-R and M24LR64E-R only: Non ISO 15693 compliant command for retrieving memory size	NA
	M24LR16E-R and M24LR64E-R only: Non ISO 15693 compliant response of Get multiple blocks security status command.	NA
	NA	Write multiple blocks commands (maximum 4 blocks)
	NA	Extended commands
	Inventory initiated feature	NA
	Proprietary fast read commands (downlink 53-Kbits/s)	
	RF block size of 4 bytes	
Memory organization	1-Kbit sectors	4 configurable areas (32-byte minimum size)
User memory protection	From RF: each sector individually protected in read and/or write by one of 3 possible RF passwords	From RF: each area individually protected in read and/or write by one of 3 possible RF passwords
	From I^2C: write protection with one I^2C password	From I^2C: read and write protection with one I^2C password
	32-bit RF and I^2C passwords	64-bit RF and I^2C passwords
	NA	Individual write protection of the first two memory blocks (CCfile)
System configuration protection	NA	From RF: write protection with one RF password
	NA	From I^2C: write protection with one I^2C password
	NA	64-bit RF and I^2C passwords
	NA	Possible definitive lock of configuration for RF write access
System configuration	From RF: custom commands to read and write configuration register and control byte	From RF: custom commands to read and write static configuration registers and to read and write dynamic configuration registers
	From I^2C: range address 2304-2336 with E2=1	From I^2C: static configuration range address 0000-0023 with E2=1, E1=1 dynamic configuration range address 2003-2007 with E2=0, E1=1

Table 3. Feature comparison summary (continued)

Feature	M24LR	ST25DVxxKC
Interrupt on RF events	Digital output pin (RFWIP/RFBusy) Open drain active low.	General purpose output pin (GPO) ST25DVxxKC-IE: Open drain active low ST25DVxxKC-JF: CMOS active high
	RF Busy: IT when M24LR is busy in RF mode (VCD SOF to M24LR EOF)	RF Activity: IT when ST25DVxxKC is answering to RF request (VCD EOF to ST25DVxxKC EOF)
	RF Write: IT during M24LR internal write time	RF Write: IT pulse after valid write
	NA	RF User: level set by RF command
	NA	RF Interrupt: pulse generated by RF command
	NA	Field change: IT pulse on RF field state change
	NA	RF put message: IT pulse after RF successfully write message
	NA	RF get message: IT pulse after RF successfully read message
	Status bit to indicate correct completion of I^2C write cycle	I^2C write: IT pulse at completion of I^2C write cycle
	-	I^2C RF off: IT pulse when RF interface is set off
	NA	IT status register for host to check IT event source
	NA	IT pulse duration configurable
Energy harvesting	Power delivered on VOUT output pin is limited depending on configuration	All power delivered on V_EH output pin.
	4 sink current level configurations	-
Fast transfer mode	NA	256-byte buffer for fast data transfer between host MCU and RF reader
RF management	NA	RF configurable as disable or sleep or off from host MCU
Low power mode	NA	LPD pin to trigger low power down mode(2)

1. Typical 28.5 pF value for the ST25DVxxKC is equivalent to what was specified in the M24LR datasheet as 27.5 pF. This change is related to a different measurement methodology between M24LR and ST25DVxxKC.
2. Only available on ST25DVxxKC-JF version.

3 Hardware considerations

M24LR and ST25DVxxKC-IE products are available in the same package versions. ST25DVxxKC-JF products are available in different packages.

Table 4. M24LR and ST25DVxxKC product package availability

Product	Package			
	SO8	TSSOP8	UFDFPN8	UFDFPN12
M24LRxxE-R	X	X	X	-
ST25DVxxKC-IE	X	X	X	-
ST25DVxxKC-JF	-	-	-	X

ST25DVxxKC-JF products are not pin-to-pin compatible with M24LR products.

ST25DVxxKC-IE and M24LR products are pin-to-pin compatible when using the same package. The signal correspondence is shown in *Table 5*.

Table 5. M24LR and ST25DVxxKC-IE signal correspondence

Pin number	M24LR Signal name	ST25DVxxKC-IE Corresponding signal name	Function	Direction
1	Vout	V_EH	Energy harvesting output	Analog output
2	AC0	AC0	Antenna coil	I/O
3	AC1	AC1	Antenna coil	I/O
4	Vss	VSS	Ground	-
5	SDA	SDA	Serial data	I/O
6	SCL	SCL	Serial clock	Input
7	RF WIP/BUSY	GPO	Digital interrupt output	Digital output
8	Vcc	VCC	Supply voltage	Power

M24LR and ST25DVxxKC products support the same power supply voltage range, as shown in *Table 6*.

Table 6. Supported power supply range

Power supply	M24LR	ST25DVxxKC	Unit
Vcc min.	1.8	1.8	V
Vcc max.	5.5	5.5	

M24LR and ST25DVxxKC products internal tuning capacitance, is shown in*Table 7*. Migrating from M24LR to ST25DVxxKC products doesn't require modification to antenna design.

Note: The typical 28.5 pF value for the ST25DVxxKC is equivalent to the M24LR datasheet value of 27.5 pF. This change is due to a different measurement methodology between M24LR and ST25DVxxKC products.

Table 7. Internal tuning capacitance

M24LR04E-R, M24LE16E-R, M24LR64E-R	St25DV04KC, ST25DV16KC, ST25DV64KC	Unit
27.5	28.5	pF

4 I²C operation

I²C operation differences between M24LR and ST25DVxxKC products are shown in *Table 8*.

Table 8. I²C operation differences between M24LR and ST25DVxxKC products

I²C feature	M24LR	ST25DVxxKC
Read current	Roll-over if end of memory is reached.	No roll over if end of memory is reached.
Sequential read	Roll-over if end of memory is reached.	No roll over if end of memory is reached.
Write multiple bytes	Limited to 4 bytes (page size) All bytes must address the same row of memory.	Limited to 256 bytes. Write fails if some data cross area boundaries.
Present password	Password is 32-bits long	Password is 64-bits long
Write password	Password is 32-bits long	Password is 64-bits long
I²C timeout on start condition	Min 40 ms	Min 29.6 ms

5 RF operations

M24LR and ST25DVxxKC products are based on the ISO/IEC 15693 standard. In addition, ST25DVxxKC products are compatible with ISO/IEC 15693 (revision 2019), and with NFC Forum Type 5 Tag.

M24LR and ST25DVxxKC products both address RF blocks of 4 bytes.

M24LR and ST25DVxxKC products are similar in their RF operations (protocol, modulations and timings), but they differ in their ISO/IEC 15693 standard command support and in their custom commands.

5.1 RF command list

Table 9 shows the differences in ISO/IEC 15693 standard commands supported by M24LR and ST25DVxxKC products.

Table 9. Comparison of ISO/IEC 15693 mandatory and optional commands supported in M24LR and ST25DVxxKC products

Command code	M24LR commands	ST25DVxxKC commands	Comment
01h	Inventory	Inventory	-
02h	Stay quiet	Stay quiet	-
20h	Read single block	Read single block	In M24LR16E-R and M24LR64E-R, this command request has a custom format.
21h	Write single block	Write single block	In M24LR16E-R and M24LR64E-R, this command request has a custom format.
22h	-	Lock block	-
23h	Read multiple blocks	Read multiple blocks	In M24LR16E-R and M24LR64E-R, this command request has a custom format. Limited to 32 blocks maximum in all M24LR versions.
24h	-	Write multiple blocks	-
25h	Select	Select	-
26h	Reset to ready	Reset to ready	-
27h	Write AFI	Write AFI	-
28h	Lock AFI	Lock AFI	-
29h	Write DSFID	Write DSFID	-
2Ah	Lock DSFID	Lock DSFID	-
2Bh	Get system info	Get system info	In M24LR16E-R and M24LR64E-R, the answer is formatted differently if Protocol_extenstion_flag = 1.

Table 9. Comparison of ISO/IEC 15693 mandatory and optional commands supported in M24LR and ST25DVxxKC products (continued)

Command code	M24LR commands	ST25DVxxKC commands	Comment
2Ch	Get multiple block SS	Get multiple block SS	In M24LR16E-R and M24LR64E-R, this command request has a custom format.
30h	-	Extended read single block	-
31h	-	Extended write single block	-
32h	-	Extended lock block	-
33h	-	Extended read multiple blocks	-
34h	-	Extended write multiple blocks	-
3Bh	-	Extended get system info	-
3Ch	-	Extended get multiple block SS	-

Table 10 shows the differences in custom commands supported by M24LR and ST25DVxxKC products.

Table 10. Comparison of custom commands supported in M24LR and ST25DVxxKC products

Cmd code	M24LR commands	ST25DVxxKC commands	Comment
A0h	Read configuration	Read configuration	Different command formatting and purpose between M24LR and ST25DVxxKC products
A1h	Write EH configuration	Write configuration	Different command formatting and purpose between M24LR and ST25DVxxKC products
A2h	Set reset EH configuration	-	-
A3h	Check EH enable	-	-
A4h	Write DO configuration	-	-
A9h	-	Manage GPO	-
AAh	-	Write message	-
ABh	-	Read message length	-
ACh	-	Read message	-
ADh	-	Read dynamic configuration	-
AEh	-	Write dynamic configuration	-
B1h	Write sector password	Write password	Different command formatting and purpose between M24LR and ST25DVxxKC products
B2h	Lock sector password	-	-

Table 10. Comparison of custom commands supported in M24LR and ST25DVxxKC products (continued)

Cmd code	M24LR commands	ST25DVxxKC commands	Comment
B3h	Present sector password	Present password	Different command formatting and purpose between M24LR and ST25DVxxKC products
C0h	Fast read single block	Fast read single block	In M24LR16E-R and M24LR64E-R, this command request has a different format than M24LR04E-R and ST25DVxxKC.
C1h	Fast inventory initiate	-	-
C2h	Fast initiate	-	-
C3h	Fast read multiple blocks	Fast read multiple blocks	In M24LR16E-R and M24LR64E-R, this command request has a different format than M24LR04E-R and ST25DVxxKC.
C4h	-	Fast extended read single block	-
C5h	-	Fast extended read multiple block	-
CAh	-	Fast write message	-
CBh	-	Fast read message length	-
CCh	-	Fast read message	-
CDh	-	Fast read dynamic config	-
CEh	-	Fast write dynamic config	-

6 User memory access from RF reader

RF user memory is addressed by blocks of 32 bits (4 bytes), both in M24LR and ST25DVxxKC products.

The maximum block address of RF user memory depends on the memory size of device. Depending on the number of blocks, 1 or 2 bytes are needed to code the block's memory address as shown in *Table 11*.

Table 11. Number of blocks per device in M24LR and ST25DVxxKC product families

Parameter	M24LR04E-R ST25DV04KC	M24LR16E-R ST25DV16KC	M24LR64E-R ST25DV64KC
Memory size	4 Kbits	16 Kbits	64 Kbits
Block size	4 bytes	4 bytes	4 bytes
Max block address	7Fh	1FFh	7FFh
Number of bytes used to code block addresses	1 byte	2 bytes	2 bytes
Product type	Low density	High density	High density

The ISO/IEC 15693 specification defines the read and write commands with a block number coded on 1 byte for low density devices (memory smaller than 256 blocks).

The third amendment of ISO/IEC 15693 defines the extended read and write commands with a block number coded on 2 bytes for high density devices (memory larger than 256 blocks).

M24LR16E-R and M24LR64E-R are high-density devices, but have been released before ISO/IEC 15693 amendment 3 publication and do not integrate extended read and write commands. Instead, they use custom read and write commands with block numbers coded on 2 bytes and the proprietary Protocol_extension_flag to address all memory blocks (see *Table 12*).

All ST25DVxxKC versions benefit from ISO/IEC 15693 amendment 3 for extended memory organization and can use extended commands to address all memory blocks.

Table 12. Addressing modes of M24LR and ST25DVxxKC devices

Parameter	M24LR04E-R	M24LR16E-R M24LR64E-R	ST25DV04KC ST25DV16KC ST25DV64KC
Addressing mode	Standard (1 byte)	Custom (2 bytes)	Standard(1) (1 byte) and extended (2 bytes)
Protocol_extension_flag	0	1	0

1. Standard mode cannot access blocks above address FFh (8 Kbits). Blocks above address FFh must be accessed in Extended mode.

In consequence, three migration paths exist, as shown in *Table 13*.

Table 13. Memory addressing migration paths

Original device	New device	Changes in reading and writing user memory blocks
M24LR04E-R	ST25DV04KC	No change
M24LR04E-R	ST25DV04KC ST25DV16KC ST25DV64KC	No change for reading and writing blocks below or equal to address FFh Extended read and write commands must be used for reading and writing blocks above address FFh, and can be used also for address below or equal to FFh
M24LR16E-R M24LR64E-R	ST25DV04KC ST25DV16KC ST25DV64KC	Different commands must be used for reading and writing blocks, whatever the address

Table 14: M24LR04KE-R (fast) read single block to *Table 29: ST25DVxxKC extended get multiple blocks security status* show differences in format of read and write block commands on M24LR and ST25DVxxKC products.

6.1 Read single block

If the option flag is not set, the response to read single block commands is identical between M24LR and ST25DVxxKC products.

If the option flag is set, the block security status byte of the response is different. See *Table 43: M24LR RF block security status response* and *Table 44: ST25DVxxKC RF block security status response* for the block security status byte format in M24LR and ST25DVxxKC products.

Table 14. M24LR04KE-R (fast) read single block

SOF	Request_flags	(Fast) read single block	UID (optional)	Block number	CRC16	EOF
-	xxxx0xxxb	(C0h) 20h	8 bytes	1 byte	2 bytes	-

Table 15. M24LR16E-R and M24LR64E-R (fast) read single block

SOF	Request_flags	(Fast) read sngle block	UID (optional)	Block number	CRC16	EOF
-	xxxx1xxxb	(C0h) 20h	8 bytes	2 bytes	2 bytes	-

Table 16. ST25DV04KC, ST25DV16KC, ST25SV64KC (fast) read single block(1)

SOF	Request_flags	(Fast) read single block(1)	UID (optional)	Block number	CRC16	EOF
-	xxxx0xxxb	(C0h) 20h	8 bytes	1 bytes	2 bytes	-

1. Blocks above address FFh cannot be read.

Table 17. ST25DVxxKC (fast) extended read single block

SOF	Request_flags	(Fast) extended read single block	UID (optional)	Block number	CRC16	EOF
-	xxxx0xxxb	(C4h) 30h	8 bytes	2 bytes	2 bytes	-

6.2 Write single block

Responses to write commands are identical between M24LR and ST25DVxxKC products.

Table 18. M24LR04KE-R write single block

SOF	Request_flags	Write single block	UID (optional)	Block number	Data	CRC16	EOF
-	xxxx0xxxb	21h	8 bytes	1 byte	4 bytes	2 bytes	-

Table 19. M24LR16E-R and M24LR64E-R write single block

SOF	Request_flags	Write single block	UID (optional)	Block number	Data	CRC16	EOF
-	xxxx1xxxb	21h	8 bytes	2 bytes	4 bytes	2 bytes	-

Table 20. ST25DVxxKC write single block

SOF	Request_flags	Write single block(1)	UID (optional)	Block number	Data	CRC16	EOF
-	xxxx0xxxb	21h	8 bytes	1 byte	4 bytes	2 bytes	-

1. Cannot write block above address FFh

Table 21. ST25DVxxKC extended write single block

SOF	Request_flags	Extended write single block	UID (optional)	Block number	Data	CRC16	EOF
-	xxxx0xxxb	31h	8 bytes	2 bytes	4 bytes	2 bytes	-

Additionally, in ST25DVxxKC products, write multiple blocks and extended write multiple blocks commands are available for writing multiple blocks, allowing a faster write process. However the number of blocks is limited to 4 (see the ST25DVxxKC datasheet *[4]*).

6.3 Read multiple blocks

If the option flag is not set, the response to read multiple block commands is identical between M24LR and ST25DVxxKC products.

If the option flag is set, the block security status byte of the response is different. See *Table 43: M24LR RF block security status response* and *Table 44: ST25DVxxKC RF block security status response* for block security status byte format in M24LR and ST25DVxxKC products.

Table 22. M24LR04E-R (fast) read multiple blocks

SOF	Request_flags	(Fast) read multiple blocks	UID (optional)	First block	Number of blocks	CRC16	EOF
-	xxxx0xxxb	(C3h) 23h	8 bytes	1 byte	1 byte(1)	2 bytes	-

1. Number of blocks is limited to 32 and all blocks must belong to same sector. Otherwise, error is 0Fh returned.

Table 23. M24LR16E-R and M24LR64E-R (fast) read multiple blocks

SOF	Request_flags	(Fast) read multiple blocks	UID (optional)	First block	Number of blocks	CRC16	EOF
-	Xxxx1xxxb	(C3h) 23h	8 bytes	2 bytes	1 byte(1)	2 bytes	-

1. Number of blocks is limited to 32 and all blocks must belong to same sector. Otherwise, error is 0Fh returned.

Table 24. ST25DVxxKC (fast) read multiple blocks(1)

SOF	Request_flags	(Fast) read multiple blocks	UID (optional)	First block	Number of blocks	CRC16	EOF
-	xxxx0xxxb	(C3h) 23h	8 bytes	1 byte	1 byte(2)	2 bytes	-

1. Can't read block above address FFh
2. Returns all blocks until it reaches a non readable block (read locked or out of memory).

Table 25. ST25DVxxKC (fast) extended read multiple blocks

SOF	Request_flags	(Fast) extended read multiple blocks	UID (optional)	First block	Number of blocks	CRC16	EOF
-	xxxx0xxxb	(C5h) 33h	8 bytes	2 bytes	2 bytes(1)	2 bytes	-

1. Returns all blocks until it reaches a non readable block (read locked or out of memory).

M24LR and ST25DVxxKC devices read multiple blocks commands differ in the number of blocks that can be read:

- **M24LR:** Read multiple blocks is limited to 32 blocks maximum located in the same sector.
- **ST25DVxxKC**: Read multiple blocks is limited to 256 blocks.
- **ST25DVxxKC:** Extended read multiple blocks is limited to the maximum memory size.

6.4 Get multiple blocks security status

The block security status byte response of multiple-block security status commands is different between M24LR and ST25DVxxKC products. See *Table 43: M24LR RF block security status response* and *Table 44: ST25DVxxKC RF block security status response* for the block security status byte format in M24LR and ST25DVxxKC products.

Table 26. M24LR04E-R get multiple blocks security status

SOF	Request_flags	Get multiple blocks SS	UID (optional)	First block	Number of blocks	CRC16	EOF
-	xxxx0xxxb	2Ch	8 bytes	1 bytes	1 byte	2 bytes	-

Table 27. M24LR16E-R and M24LR64E-R get multiple blocks security status

SOF	Request_flags	Get multiple blocks SS	UID (optional)	First block	Number of blocks	CRC16	EOF
-	xxxx1xxxb	2Ch	8 bytes	2 bytes	2 bytes	2 bytes	-

Table 28. ST25DVxxKC get multiple blocks security status

SOF	Request_flags	Get multiple blocks SS(1)	UID (optional)	First block	Number of blocks	CRC16	EOF
-	xxxx0xxxb	2Ch	8 bytes	1 byte	1 byte	2 bytes	-

1. Can't access block above address FFh.

Table 29. ST25DVxxKC extended get multiple blocks security status

SOF	Request_flags	Extended get multiple blocks SS	UID (optional)	First block	Number of blocks	CRC16	EOF
-	xxxx0xxxb	3Ch	8 bytes	2 bytes	2 bytes	2 bytes	-

7 User memory organization and protection

M24LR and ST25DVxxKC products have different user memory organization and use different memory protection methods, both for RF and I^2C accesses.

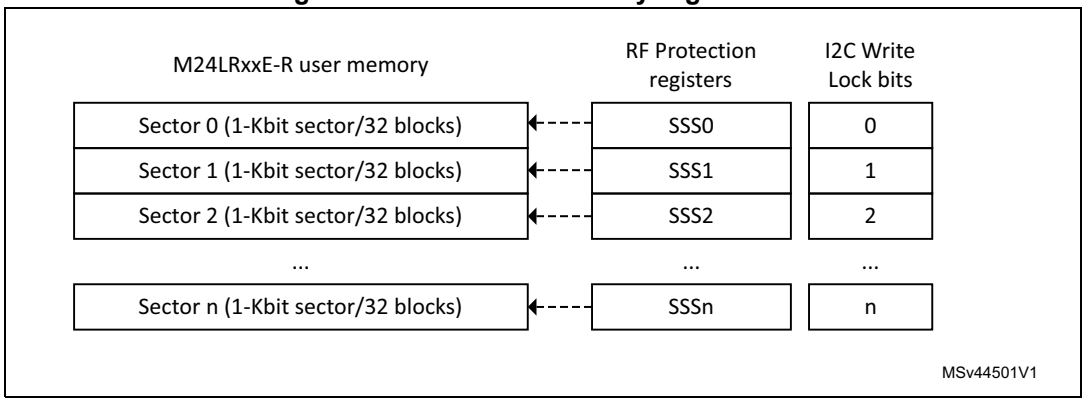
7.1 M24LR user memory organization and protection overview

M24LR product user memory is organized in sectors of 32 blocks (of 1 Kbits).

For RF access, each sector is assigned to a security status register (SSS0, SSS1, SS2 .. SSSn) and can be individually read and/or write access protected by one of three available 32-bit RF passwords.

For I^2C accesses, each sector can be write-protected with a write-lock bit and a 32-bit I^2C password.

Figure 1. M24LR user memory organization



7.2 ST25DVxxKC user memory organization and protection overview

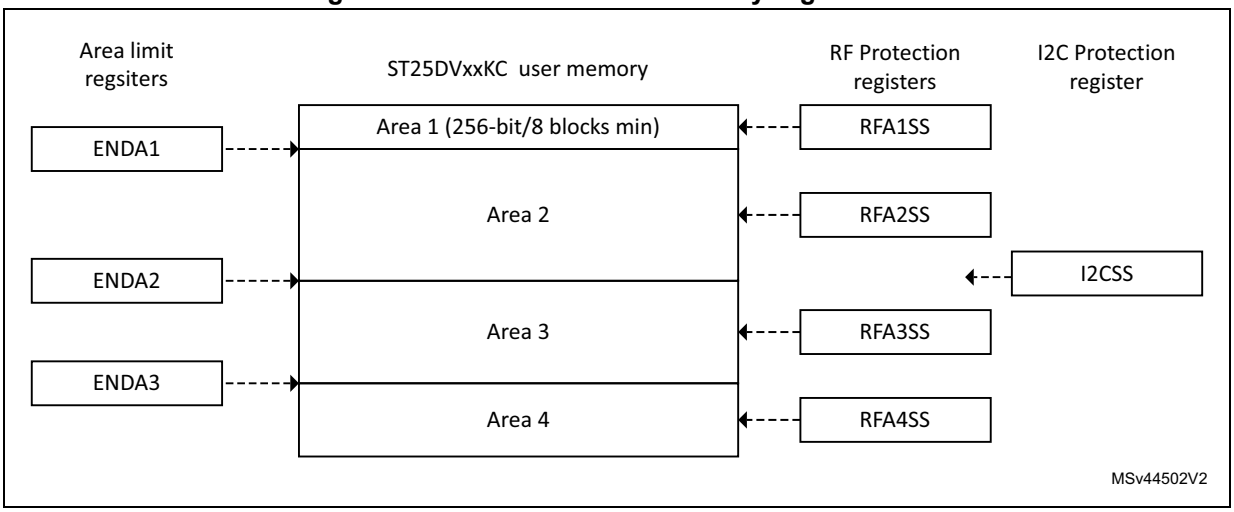
ST25DVxxKC user memory is organized in 4 size-configurable contiguous areas with a granularity of eight blocks (256 bits).

Area1 always starts at the first block of memory. Area4 always ends at the last block of memory. Three registers, ENDA1, ENDA2 and ENDA3 define Area1, Area2 and Area3 ends respectively. The minimum area size is eight blocks, up to a maximum area of the full memory size. By default, user memory is configured with one full memory size area.

For RF accesses, each area is assigned with a security status register (RFA1SS, RFA2SS, RFA3SS and RFA4SS) and can be individually read and/or write protected by one of three available 64-bit RF passwords.

For I^2C accesses, the I2CSS register is used to set individual read and/or write protection of each zone with one 64-bit I^2C password (while M24LR only has I^2C write protection).

Figure 2. ST25DVxxKC user memory organization



All sector protection capabilities of M24LR devices are available for ST25DVxxKC areas, except for area 1, which is always readable in ST25DVxxKC devices.

In addition, block 0 and block 1 of ST25DVxxKC can be individually write-protected, independently from area protection.

7.3 Security sessions

M24LR and ST25DVxxKC products provide protection of user memory and of some configuration registers. The RF user and I^2C host can access those protected places by opening security sessions with the help of passwords. Access is more restricted when security sessions are closed and less restricted when security sessions are opened.

Security sessions are slightly different between M24LR and ST25DVxxKC products, as shown in *Table 30*.

Table 30. Security sessions of M24LR versus ST25DVxxKC

Security sessions	Opened with	M24LR: access provided by opened security session	ST25DVxxKC: access provided by opened security session
RF user	RF pwd 1, 2 or 3(1)	RF user access to protected user memory(2)	
		RF user write access to RF password 1, 2 or 3(3)	
RF configuration	RF pwd 0	-	RF user write access to configuration registers
			RF user write access to RF password 0
I^2C	I^2C pwd	-	I^2C host access to protected user memory(2)
		I^2C host write access to sectors security registers	I^2C host write access to configuration registers
		I^2C host write access to I^2C password	I^2C host write access to I^2C password

1. Password number must be the same as the one selected for protection.
2. Depending on access rights in opened security session set for the corresponding memory block.
3. Write access to the password number corresponding to the password number presented.

Password length is different in M24LR and ST25DVxxKC products, as shown in *Table 31*. Default password values are 00000000h for M24LR and 0000000000000000h for ST25DVxxKC.

Table 31. Password lengths

Password	M24LR	ST25DVxxKC
RF password 0 (configuration)	-	64 bits
RF passwords 1, 2 and 3	32 bits	64 bits
I^2C password	32 bits	64 bits

Possible actions for security sessions are:

Open RF user security session:

- **M24LR**: Present sector password command with password number (1, 2 or 3) and a valid corresponding password.
- **ST25DVxxKC**: Present password command with password number (1, 2 or 3) and a valid corresponding password.

Write RF password:

- **M24LR**: Present sector password command with chosen password number (1, 2 or 3) and a valid corresponding password. Then Write Sector Password command with the same chosen password number (1, 2 or 3).
- **ST25DVxxKC**: Present password command with password number (0, 1, 2 or 3) and a valid corresponding password. Then write assword command with the same password number (0, 1, 2 or 3).

Close RF user security session:

- **M24LR and ST25DVxxKC**: Present password command with different password number or wrong password. Or remove tag from RF field (POR).

Open RF configuration security session:

- **M24LR**: No RF configuration security session.
- **ST25DVxxKC**: Present password command with password number 0 and valid password 0.

Close RF configuration security session:

- **M24LR**: No RF configuration security session.
- **ST25DVxxKC**: Present password command with different password number, or password number 0 and wrong password 0. Or remove tag from RF field (POR).

Open I^2C security session:

- **M24LR and ST25DVxxKC**: I^2C Present password command with valid password.

Write I^2C password:

- **M24LR and ST25DVxxKC**: I^2C Present password command with valid password. Then I^2C write password command.

Close I^2C security session:

- **M24LR and ST25DVxxKC**: I^2C Present password command with wrong password. Or remove tag power supply (POR).

In ST25DVxxKC devices, the I^2C host can read the current status (opened or closed) of the I^2C security session by reading the I2C_SSO_Dyn register.

Figure 3 and *Figure 4* show the differences in format of the I^2C present password and I^2C write password commands between M24LR and ST25DVxxKC products.

Figure 3. I^2C Present password in M24LR and ST25DVxxKC products

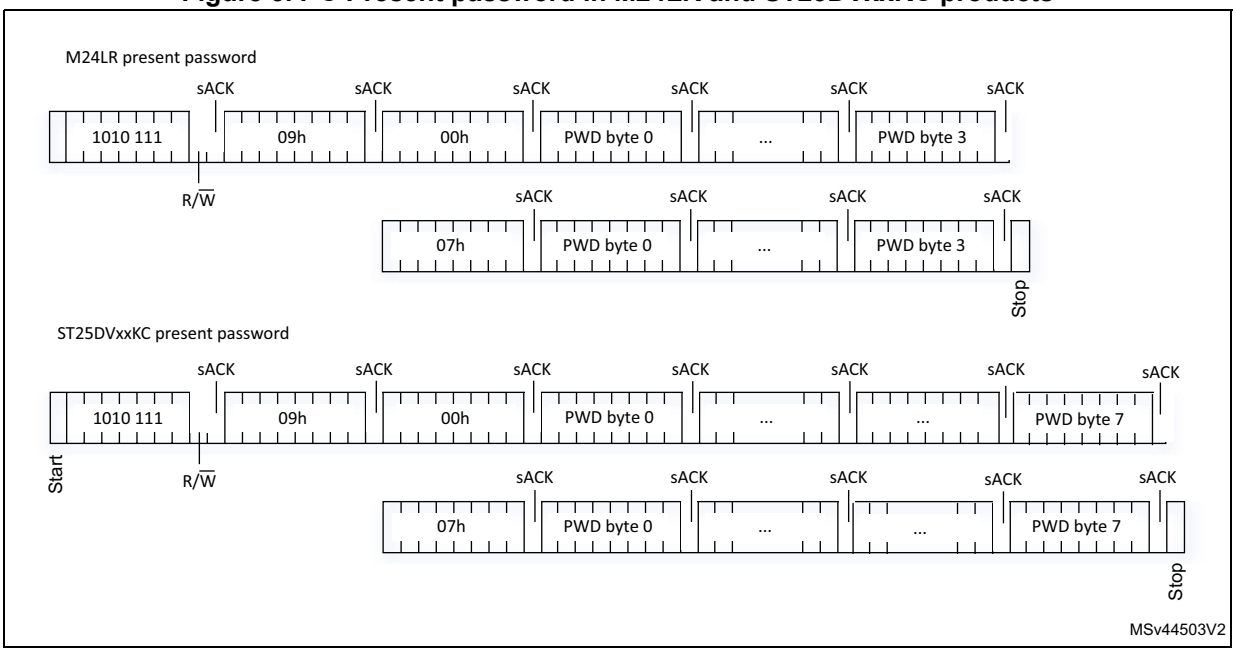


Figure 4. I²C write password in M24LR and ST25DVxxKC products

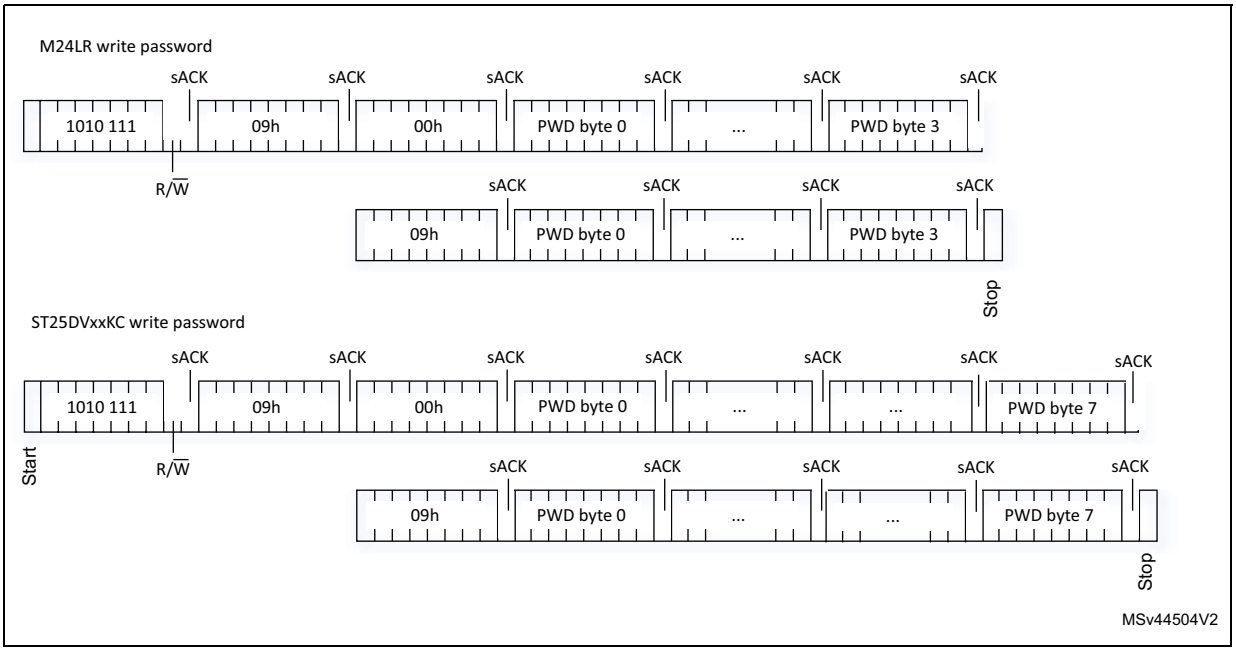


Table 32: M24LR write sector password command to *Table 35: ST25DVxxKC present password command* show the differences in format of RF present sector password, present password, write sector password and write password commands between M24LR and ST25DVxxKC devices.

Table 32. M24LR write sector password command

SOF	Request_flags	Write sector password	IC Mfg code	UID (optional)	Password number	Password	CRC16	EOF
-	1 byte	B1h	02h	8 bytes	1 byte	4 bytes	2 bytes	-

Table 33. ST25DVxxKC write password command

SOF	Request_flags	Write sector password	IC Mfg code	UID (optional)	Password number	Password	CRC16	EOF
-	1 byte	B1h	02h	8 bytes	1 byte	8 bytes	2 bytes	-

Table 34. M24LR present sector password command

SOF	Request_flags	Present sector password	IC Mfg code	UID (optional)	Password number	Password	CRC16	EOF
-	1 byte	B3h	02h	8 bytes	1 byte	4 bytes	2 bytes	-

Table 35. ST25DVxxKC present password command

SOF	Request_flags	Present password	IC Mfg code	UID (optional)	Password number	Password	CRC16	EOF
-	1 byte	B3h	02h	8 bytes	1 byte	8 bytes	2 bytes	-

7.4 ST25DVxxKC area size configuration

Area sizes can be adjusted independently of the protection setting. By default, only area 1 exists and fills the entire memory.

$ENDA_n$ registers define the limits of each area, with start of area 1 always being block 0, and end of area 4 always being the last block of memory.

Area size modifications must be done using the following procedure, respecting orders:

1. Ends of areas 3 and 2 must first be set to the end of memory while respecting the following order:
   a) If ENDA3 ≠ end of user memory, then set ENDA3 = end of memory; else, do not write ENDA3
   b) If ENDA2 ≠ end of user memory, then set ENDA2 = end of memory; else, do not write ENDA2.
2. Then, desired area limits can be set respecting the following order:
   a) Set new ENDA1 value
   b) Set new ENDA2 value, with ENDA2 > ENDA1
   c) Set new ENDA3 value, with ENDA3 > ENDA2.

Table 36. ST25DVxxKC registers related to area size configuration

RF access			Registers	I^2C access		
Command	Address	Type		Device select	Address	Type
Read configuration Write configuration	05h	R/W(1)	ENDA1	E2 = 1, E1 = 1	0005h	R/W(2)
	07h	R/W(1)	ENDA2	E2 = 1, E1 = 1	0007h	R/W(2)
	09h	R/W(1)	ENDA3	E2 = 1, E1 = 1	0009h	R/W(2)
	0Fh	R/W(1)	LOCK_CFG	E2 = 1, E1 = 1	000Fh	R/W(2)
No access	-		I2C_PWD	E2 = 1, E1 = 1	0900h	R(3)/W(4)
Present password Write password	00h	W0(5)	RF_PWD_0	-	No access	
No access	-		I2C_SSO_Dyn	E2 = 0, E1 = 1	2004h	R0

1. Write access is granted if an RF configuration security session is open and the configuration is not locked (LCK_CFG register equals to 0).
2. Write access only if I^2C security session is open.
3. Read access only if I^2C security session is open.
4. Write with I^2C write password command only if I^2C security session is open.
5. Write access only if corresponding RF security session is open.

Area end limit coding is defined as follows:

RF block address = 8 * $ENDA_n$ + 7 => $ENDA_n$ = int (RF block address / 8)

I^2C byte address = 32 * $ENDA_n$ + 31 => $ENDA_n$ = int (I^2C byte address / 32)

Note: The RF user must first open the RF configuration security session to write $ENDA_n$ registers. The I^2C host must first open an I^2C security session to write $ENDA_n$ registers.

7.5 RF user memory protection

7.5.1 RF user memory protection: M24LR registers

To manage sector protection from RF access, M24LR has one SSS (sector security status) register per sector and three RF passwords (RF_PWD1-3).

Table 37. M24LR registers related to RF user memory protection

RF			Registers	I^2C		
Command	Address	Type		Device select	Address	Type
Lock sector	00h to 1Fh	W0(1)	SSS0	E2 = 1	0000h	R/W(2)
	20h to 3Fh	W0(1)	SSS1	E2 = 1	0001h	R/W(2)
	..	W0(1)	..	E2 = 1	..	R/W(2)
	@Last block-31 to @last block	W0(1)	SSSn	E2 = 1	000nh	R/W(2)
No access	-		I2C_PWD	E2 = 1	0900h	R(3)/W(4)
Present sector PWD Write sector PWD	00h	W(5)	RF_PWD1	-	No access	
	01h	W(5)	RF_PWD2			
	02h	W(5)	RF_PWD3			

1. Write access only if sector is not already locked.
2. Write access only if I^2C security session is open.
3. Read access only if I^2C security session is open.
4. Write with I^2C write password command only if I^2C security session is open.
5. Write access only if corresponding RF security session is open.

Table 38. M24LR SSSn register description

SSSn			
Bit	**Name**	**Function**	**Factory value**
b0	Sector lock	0: sector n not locked 1: sector n locked	0b
b2-b1	Read/Write protection	00: sector n RF user security session can’t be opened by password 01: sector n RF user security session opened by RF_PWD_1 10: sector n RF user security session opened by RF_PWD_2 11: sector n RF user security session opened by RF_PWD_3	00b
b4-b3	Password control	00: sector n RF access: Read always allowed - write if RF user security session opened 01: sector n RF access: Read always allowed - write always allowed 10: sector n RF access: Read if RF security user session opened - write if RF user security session opened 11: sector n RF access: Read if RF user security session opened - write always forbidden	00b
b7-b5	RFU	-	000b

7.5.2 RF user memory protection: ST25DVxxKC registers

To manage area protection from RF accesses, ST25DVxxKC devices have three registers to determine the area limits ($ENDA_n$), one security status register per area (RFAnSS) and three RF passwords (RF_PWD1-3).

A register to lock the configuration (LOCK_CFG), a password to open RF configuration security session (RF_PWD_0), and a password to open I^2C security session are also involved in area protection.

Finally, a register to independently write-lock blocks 0 and/or 1 is available (LOCK_CCFILE).

Table 39. ST25DVxxKC registers related to RF user memory protection

RF access			Registers	I^2C access		
Command	Address	Type		Device select	Address	Type
Read configuration Write configuration	04h	R/W(1)	RFA1SS	E2 = 1, E1 = 1	0004h	R/W(2)
	06h	R/W(1)	RFA2SS	E2 = 1, E1 = 1	0006h	R/W(2)
	08h	R/W(1)	RFA3SS	E2 = 1, E1 = 1	0008h	R/W(2)
	0Ah	R/W(1)	RFA4SS	E2 = 1, E1 = 1	000Ah	R/W(2)
(Ext) get multi. BSS @00 or @01 (Ext) lock block	-	R/W(3)	LOCK_CCFILE	E2 = 1, E1 = 1	000Ch	R/W(2)
Read configuration Write configuration	0Fh	R/W(1)	LOCK_CFG	E2 = 1, E1 = 1	000Fh	R/W(2)
No access	-		I2C_PWD	E2 = 1, E1 = 1	0900h	R(4)/W(5)
Present password Write password	00h	W0(6)	RF_PWD_0	-	No access	
	01h	W0(6)	RF_PWD_1			
	02h	W0(6)	RF_PWD_2			
	03h	W0(6)	RF_PWD_3			
No access	-		I2C_SSO_Dyn	E2 = 0, E1 = 1	2004h	R0

1. Write access granted if RF configuration security session is open and configuration is not locked (LCK_CFG register equals to 0).
2. Write access only if I^2C security session is open.
3. Write access to bit 0 if Block 00h is not already locked and to bit 1 if Block 01h is not already locked.
4. Read access only if I^2C security session is open.
5. Write with I^2C write password command only if I^2C security session is open.
6. Write access only if corresponding RF security session is open.

Table 40. ST25DVxxKC RFAnSS register description

RFAnSS			
Bit	**NameL**	**Function**	**Factory value**
b1-b0	PWD_CTRL_An	00: Area n RF user security session can't be opened by password 01: Area n RF user security session opened by RF_PWD_1 10: Area n RF user security session opened by RF_PWD_2 11: Area n RF user security session opened by RF_PWD_3	00b
b3-b2	RW_PROTECTION_An	00: Area n RF access: Read allowed - write allowed 01: Area n RF access: Read allowed - write allowed if RF user security session opened 10: Area n RF access: Read allowed if RF security user session opened(1) - write allowed if RF user security session opened 11: Area n RF access: Read allowed if RF user security session opened(1) - write always forbidden	00b
b7-b4	RFU	-	0000b

1. Read always allowed for Area 1.

Password control bits (in the SSSn and RFAnSS registers) have the same signification in M24LR and ST25DVxxKC products.

7.5.3 M24LR and ST25DVxxKC RF user-memory protection equivalence

The equivalence of Read/Write protection bits (in the SSSn and RFAnSS registers) is summarized in *Table 41*.

Table 41. RF user memory protection equivalence

M24LR		Sector/Area access when user security session opened		Sector/Area access when user security session closed		ST25DVxxKC
Sector Lock	**R/W protection bits**					**R/W protection bits**
0	xx	Read	Write	Read	Write	00
1	00	Read	Write	Read	No write	01
1	01	Read	Write	Read	Write	00
1	10	Read	Write	No read	No write	10(1)
1	11	Read	No write	No read	No write	11(1)

1. Not allowed for area 1 (always readable).

The sector lock bit is not present in ST25DVxxKC devices. In M24LR devices, the sector lock bit prevents sector protection modification by an RF user. The same behavior can be achieved on ST25DVxxKC devices in two different ways:

- Using the configuration password (password 0) protection to prevent RF from modifying RFAnSS registers without presenting the correct password.
- Using the LOCK_CFG register (issuing a write configuration(@0Fh) command from RF or writing to the LOCK_CFG register from I^2C) to permanently prevent RF from modifying RFAnSS registers (this also locks all configuration registers for RF access. It can be unlocked by I^2C only).

7.5.4 M24LR RF user memory protection configuration

Configuration by RF user

- **If the sector is already locked**, the RF user cannot change the sector protection (this can be done through the I^2C).
- **If the sector is not already locked**, the RF user can lock the sector by issuing a lock sector command (@Block, SSSn). The lock sector command must point to any block inside the target sector, and provide the desired SSS value.

Configuration by I^2C host

- The I^2C host must open the I^2C security session by issuing I^2C present password command.
- The I^2C host can then write any SSSn register using the I^2C write byte command (even if the block is locked).
- Optionally, the I^2C host can close the I^2C security session by issuing an I^2C present password command with the wrong I^2C password.

7.5.5 RF user memory protection configuration ST25DVxxKC

Configuration by an RF user

- **If the RF configuration is locked (LOCK_CFG register = 1)**, it is not possible to configure the area protection (this can be done through the I^2C interface).
- **If the RF configuration is not locked**:
  - The RF user must first open the RF configuration security session by issuing a present password (00h, RF_PWD_0) command with a valid RF password 0.
  - The RF user sets area protection by issuing a write configuration (@RFAnSS, SS) command to write into any RFAnSS register.
  - Optionally, the RF user can close the RF configuration security session by issuing a present password command with the wrong RF password 0 (or different password number, or remove tag from the field).

Configuration by an I²C host

- The I²C host must open the I²C security session by issuing I²C present password command.
- The I²C host can then write any RFAnSS register by an I²C write byte command.
- Optionally, the I²C host can close the I²C security session by issuing an I²C present password command with the wrong I²C password.

Blocks 0 and 1 are exceptions to this protection mechanism:

- The RF user can independently write-lock those two blocks on top of area1 protection, issuing an (ext) lock block (@00h/01h) command at block address 0 or 1.
- An RF user needs no password to lock blocks 0 and/or 1.
- Locking blocks 0 and/or 1 is possible even if the configuration is locked (LOCK_CFG=1). Locking blocks 0 and/or 1 is possible even if the area is write locked.
- Once locked, the RF user cannot unlock blocks 0 and/or 1 (can be done by I²C host).
- Unlocking area1 (through RFA1SS register) does not unlock blocks 0 and 1 if they have been locked through an (ext) lock block command or the LOCK_CCFILE register.
- The I²C host can independently write-lock/unlock those two independently of area1 protection, by writing to the LOCK_CCFILE register.
- An I²C security session must be opened to gain write access to LOCK_CCFILE register.
- Locking and unlocking blocks 0 and/or 1 is possible even if an area is write locked.

Table 42. LOCK_CCFILE register description

LOCK_CCFILE			
Bit	**Name**	**Function**	**Factory value**
b0	LCKBCK0	0: Block @ 00h is not write locked 1: Block @ 00h is write locked	0b
b1	LCKBCK1	0: Block @ 01h is not write locked 1: Block @ 01h is write locked	0b
b7-b2	RFU	-	000000b

7.5.6 Retrieve RF security status of a block

In M24LR devices, an RF user can read the block security status by issuing a get multiple blocks SS (@Block, NbBlocks) command, or (fast) read single block (@Block) and (fast) read multiple blocks (@Block, NbBlocks commands with the option flag set to 1. The block security status returned by M24LR devices is shown in *Table 43*.

Table 43. M24LR RF block security status response

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	Password control bits		Read/Write protection bits		Sector lock: 0: sector is not locked 1: sector is locked(1)

1. In M24LR devices, Get Multiple Blocks SS rolls over address 0 if the end of memory is reached. In ST25DVxxKC devices Get Multiple Blocks SS returns an error if the end of memory is reached.

In ST25DVxxKC devices, an RF user can read the block security status by issuing an (ext) get multiple blocks SS (@Block, NbBlocks) command, or (ext) (fast) read single block (@Block), (ext) (fast) read multiple blocks (@Block, NbBlocks) commands with the option flag set to 1. The block security status returned by ST25DVxxKC devices is shown in *Table 44*.

Table 44. ST25DVxxKC RF block security status response

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	Lock_flag: 0: block is not locked 1: block is locked(1)(2)

1. Lock_flag may be different if a security session is opened or closed.
2. In M24LR devices, if the SSSx register value is xxxxx011 (sector lock bit=1, R/W protection bits=01b), the meaning of the sector lock bit returned is 'write access to the SSSx register is locked, but read/write access to the sector is not locked'. This state cannot be reflected in the sector lock bit returned by ST25DVxxKC.

In order to obtain the same information as block security status of an M24LR device (Read/Write protection bits and password control bits), the ST25DVxxKC's RF user must read the RFAnSS registers of the corresponding area. The RF user can read the RFAnSS register by issuing a read configuration (@RFAnSS) command. The level of information is then equivalent.

Table 45. ST25DVxxKC RFAnSS register content

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	Read/Write protection bits		Password control bits	

Using the I^2C interface, RF sector/area security status information can be retrieved by reading the SSSn and RFAnSS registers, both in M24LR and ST25DVxxKC devices. Nevertheless, the lock_flag cannot be read through the I^2C interface of an ST25DVxxKC device, whereas the equivalent sector lock bit is available in the M24LR SSSn registers.

7.6 I²C user memory protection

7.6.1 I²C user memory protection: M24LR registers

To manage sector protection against I²C access, M24LR products have one I2C_Write_lock bit per sector and one I²C passwords (I2C_PWD).

Table 46. M24LR registers related to I²C user memory protection

RF			Registers	I²C		
Command	Address	Type		Device select	Address	Type
No access	-	-	I2C_Write_lock bits for sectors 7 to 0	E2 = 1	0800h	R/W(1)
			I2C_Write_lock bits for sectors 15 to 8	E2 = 1	0801h	R/W(1)
			..	E2 = 1	..	R/W(1)
			I2C_PWD	E2 = 1	0900h	R(2)/W(3)

1. Write access only if I²C security session is open.
2. Read access only if I²C security session is open.
3. Write with I²C write password command only if I²C security session is open.

7.6.2 I²C user memory protection: ST25DVxxKC registers

To manage area protection against I²C access, ST25DVxxKC products have three registers to determine area limits (EndAn), a security status register (I2CSS) and an I²C password (I2C_PWD).

A register (LOCK_CCFILE) to independently write-lock blocks 0 and/or 1 is also available.

Table 47. ST25DVxxKC registers related to I²C user memory protection

RF access			Registers	I²C access		
Command	Address	Type		Device select	Address	Type
No access	-	-	I2CSS	E2 = 1, E1 = 1	000Bh	R/W(1)
(Ext) get multi BSS @00 or @01 (Ext) lock block	-	R/W(2)	LOCK_CCFILE	E2 = 1, E1 = 1	000Ch	R/W(1)
No access	-		I2C_PWD	E2 = 1, E1 = 1	0900h	R(3)/W(4)
			I2C_SSO_Dyn	E2 = 0, E1 = 1	2004h	R0

1. Write access only if I²C security session is open.
2. Write access to bit 0 if block 00h is not already locked and to bit 1 if Block 01h is not already locked.
3. Read access only if I²C security session is open.
4. Write with I²C write password command only if I²C security session is open.

Table 48. I2CSS (I^2C Security Status) register description

I2CSS			
Bit	**Name**	**Function**	**Factory value**
b1-b0	RW_PROTECTION_A1	00: Area 1 I^2C access: Read allowed - write allowed 01: Area 1 I^2C access: Read allowed - write allowed if I^2C security session opened 10: Area 1 I^2C access: Read allowed - write allowed 11: Area 1 I^2C access: Read allowed - write allowed if I^2C security session opened	00b
b3-b2	RW_PROTECTION_A2	00: Area 2 I^2C access: Read allowed - write allowed 01: Area 2 I^2C access: Read allowed - write allowed if I^2C security session opened 10: Area 2 I^2C access: Read allowed if I^2C security session opened - write allowed 11: Area 2 I^2C access: Read allowed if I^2C security session opened - write allowed if I^2C security session opened	00b
b5-b4	RW_PROTECTION_A3	00: Area 3 I^2C access: Read allowed - write allowed 01: Area 3 I^2C access: Read allowed - write allowed if I^2C security session opened 10: Area 3 I^2C access: Read allowed if I^2C security session opened - write allowed 11: Area 3 I^2C access: Read allowed if I^2C security session opened - write allowed if I^2C security session opened	00b
b7-b6	RW_PROTECTION_A4	00: Area 4 I^2C access: Read allowed - write allowed 01: Area 4 I^2C access: Read allowed - write allowed if I^2C security session opened 10: Area 4 I^2C access: Read allowed if I^2C security session opened - write allowed 11: Area 4 I^2C access: Read allowed if I^2C security session opened - write allowed if I^2C security session opened	00b

7.6.3 I^2C user memory protection M24LR vs ST25DVxxKC

The equivalence of Read/Write protection bits (SSSn and RFAnSS registers) is summarized in *Table 49*.

The M24LR I^2C user memory can only be write protected. ST25DVxxKC I^2C user memory can be read-and/or write-protected.

Table 49. I²C user memory protection equivalence

M24LR	Sector/Area access when user security session opened		Sector/Area access when user security session closed		ST25DVxxKC
I2C_Write_Lock bit					I2CSS R/W protection bits
0	Read	Write	Read	Write	00
1	Read	Write	Read	No write	01
Not possible	Read	Write	No read	Write	10(1)
Not possible	Read	Write	No read	No write	11(1)

1. Not allowed for area 1 (always readable)

7.6.4 I²C user memory protection configuration for M24LR devices

Configuration by an I²C host:

- The I²C host must open the I²C security session by issuing an I2C present password command.
- The I²C host can then write I2C_write_lock bit of any sector by an I2C write byte command (even if block is locked).
- Optionally, the I²C host can close the I²C security session by issuing an I2C present password command with the wrong I²C password.

7.6.5 I²C user memory protection configuration for ST25DVxxKC devices

Configuration by an I²C host:

- The I²C host must open the I²C security session by issuing an I²C present password command.
- The I²C host can then write any I2CSS register by an I²C write byte command.
- Optionally, the I²C host can close the I²C security session by issuing an I²C present password command with the wrong I²C password.

The first 8 bytes of I²C user memory (RF blocks 0 and 1) are exceptions to this protection mechanism. See *Section 7.5.5: RF user memory protection configuration ST25DVxxKC* for details about protection of RF blocks 0 and 1.

7.6.6 Retrieve I²C security status of a byte

On M24LR devices, the I²C host can retrieve a block security status by reading the I2C_Write_lock bit of the corresponding sector.

On ST25DVxxKC devices, the I²C host can retrieve a block security status by reading the I2CSS register to get security status of the corresponding area (see *Table 48: I2CSS (I²C Security Status) register description*).

In ST25DVxxKC devices, as blocks 0 and 1 can be locked independently of the area protection mechanism, the security status of bytes 0000h to 0007h can also be read in the LOCK_CCFILE register.

8 RF event interrupts

8.1 Comparison of RF event interrupt capabilities

M24LR devices can generate interrupts on the RFWIP/BUSY pin on the following RF events:

- **RF Busy**, output level low on RFWIP/BUSY indicates to the I^2C host that the M24LR is busy in RF mode.
- **RF write in progress**, output level low on RFWIP/BUSY indicates to the I^2C host that some data is written in RF mode.

ST25DVxxKC devices can generate an interrupt on the GPO pin on the following RF events:

- **RF_USER** , GPO output level is controlled by the manage GPO command.
- **RF_ACTIVITY**, output level (low for open-drain version, or high for CMOS version) on GPO indicates to the I2C host that the ST25DVxxKC has some activity in RF mode.
- **RF_INTERRUPT**: an output pulse on GPO is generated by the manage GPO command (a low pulse for open drain version, or a high pulse for CMOS version).
- **FIELD_CHANGE**, an output pulse on GPO is generated when an RF field appears or disappears.
- **RF_PUT_MSG**, an output pulse on GPO is generated at the completion of a valid (fast) write message command.
- **RF_GET_MSG**: an output pulse on GPO can is generated at the completion of a valid (fast) read message command.
- **RF_WRITE**: an output pulse on GPO is generated on completion of a valid RF write operation. The pulse duration is configurable.

ST25DVxxKC devices can also generate an interrupt on the GPO pin on the following I^2C events:

- I^2C_WRITE: a pulse is generated on GPO output at completion of the programing cycle of a valid I2C write in EEPROM
- I^2C_RF_OFF: a pulse is generated on GPO output when RF is set OFF by the I^2C master.

It is not possible to disable interrupts on the RF WIP/BUSY pin of M24LR devices. It is possible to disable interrupts on the GPO pin in ST25DVxxKC devices. Furthermore, M24LR interrupts are exclusive, whereas ST25DVxxKC interrupts are cumulative.

Note: The closest replacement for the M24LR RF busy function is ST25DVxxKC's RF_ACTIVITY function.

The closest replacement for the M24LR RF write in progress function is ST25DVxxKC's RF_ WRITE function.

The ST25DVxxKC has two flavors of GPO output: open drain or CMOS. Open drain is active low and CMOS is active high. In order to reproduce the same behavior as the M24LR, an open-drain version of the ST25DVxxKC is preferred.

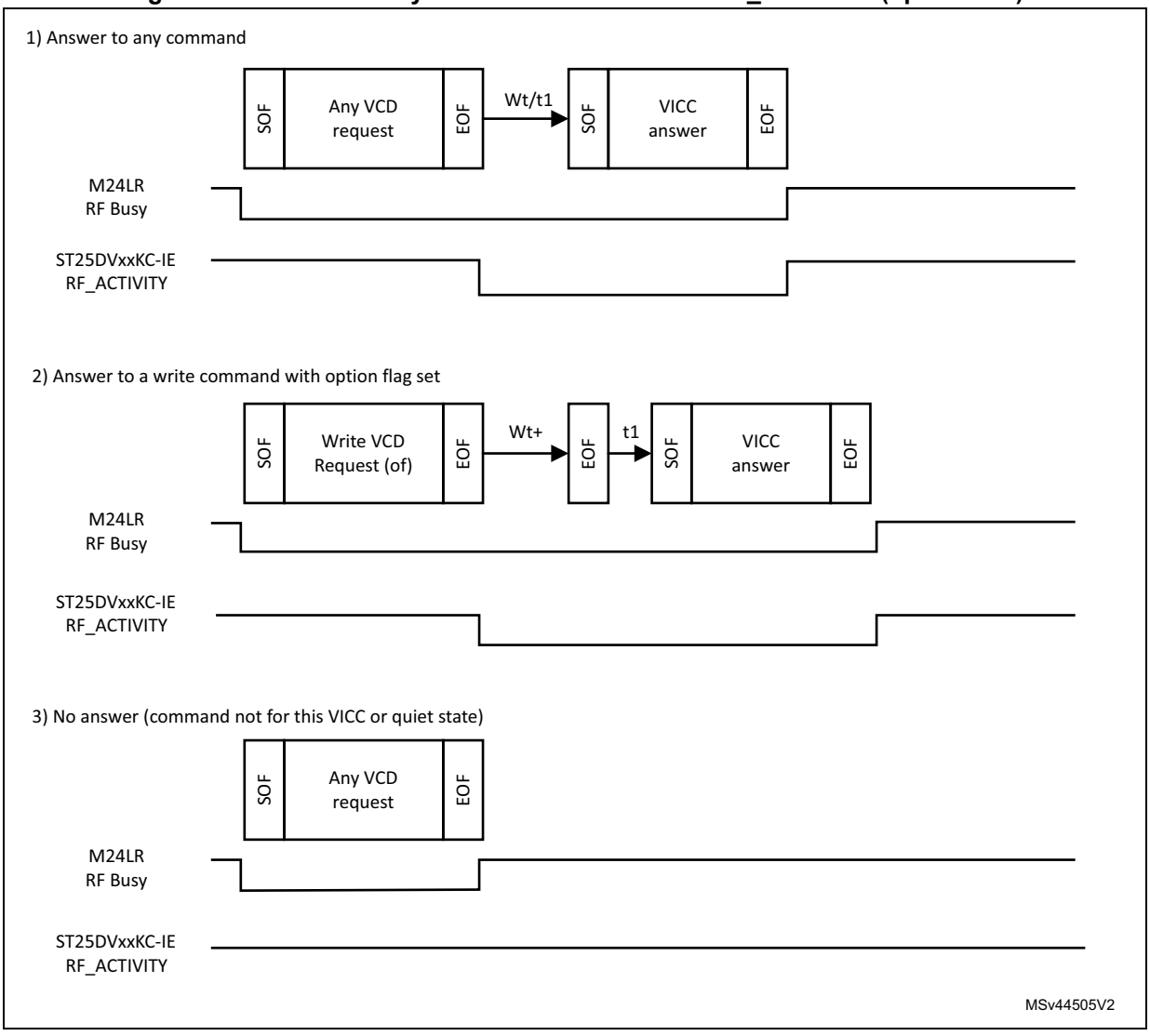
8.1.1 M24LR RF Busy versus ST25DVxxKC RF_ACTIVITY

The M24LR RF busy pin is active from the VCD request SOF until the M24LR answer EOF, whatever the answer. If the M24LR doesn't answer to the request, RF BUSY is active from the VCD request SOF until the VCD request EOF.

The ST25DVxxKC RF_ACTIVITY signal (available through the GPO pin) is active from VCD request EOF to the ST25DVxxKC answer EOF, whatever the answer. If the ST25DVxxKC doesn't answer the request, the GPO pin stays high (open drain). No interrupt is generated.

Differences between the two functions are summarized in *Figure 5*.

Figure 5. M24LR RF Busy versus ST25DVxxKC-IE RF_ACTIVITY (open drain)



To achieve similar behavior to M24LR products, only RF_ACTIVITY should be enabled, as more than one interrupt can be enabled on the GPO pin of the ST25DVxxKC.

8.1.2 M24LR RF write in progress versus ST25DVxxKC RF_WRITE

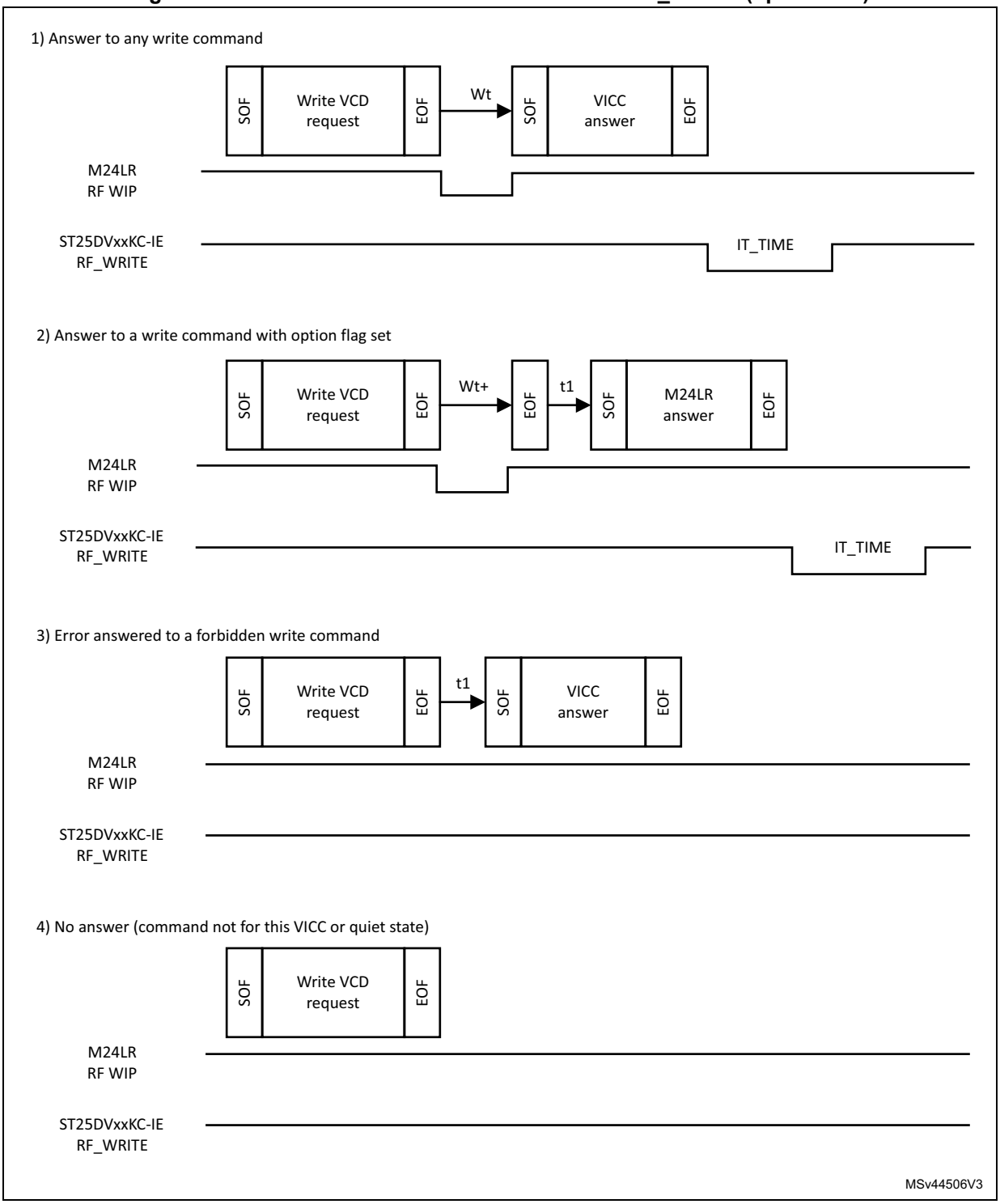
The M24LR RF WIP pin is active from the VCD write request EOF until the M24LR answer SOF. If the option flag is set in the VCD write request, the RF WIP pin is active until the VCD sends an EOF. If the VCD sends a forbidden write or if the M24LR doesn't answer the request, RF WIP stays high.

The ST25DVxxKC RF_WRITE is active for a duration defined in register IT_TIME, starting at the ST25DVxxKC answer EOF, for any write command (with or without the option flag set). If a VCD sends a forbidden write or if the ST25DVxxKC doesn't answer the request, the RF_WRITE signal stays high (open drain).

Note: On ST25DVxxKC devices, (fast) write dynamic configuration and (fast) write message commands do not trigger the RF_WRITE interrupt, as they do not write any data in EEPROM.

Differences between the two functions are summarized in *Figure 6*.

Figure 6. M24LR RF WIP versus ST25DVxxKC-IE RF_WRITE (open drain)



8.1.3 Other ST25DVxxKC RF event interrupts

Other ST25DVxxKC interrupts, their usage and configuration are detailed in the ST25DVxxKC datasheet *[4]*.

8.2 M24LR RF event interrupts: M24LR registers

To manage RF interrupts, M24LR devices have one configuration byte, that is always accessible.

Table 50. M24LR registers related to RF event interrupt

RF access			Registers	I^2C access		
Command	Address	Type		Device select	Address	Type
Read configuration Write EH configuration Write DO configuration	-	R/W	Configuration byte	E2 = 1	0910h	R/W

Bit 3 of the configuration byte selects which interrupt is associated to the RFWIP/BUSY pin.

Table 51. M24LR Configuration byte

Configuration byte			
Bit	Name	Function	Factory value
b1-b0	EH_cfg	EH fan-out configuration	00b
b2	EH_mode	0: EH is enabled after power ON 1: EH is disabled after power ON	1b
b3	RF WIP/BUSY	0: RF busy mode 1: RF write in progress mode	0b
b7-b4	RFU	-	1111b

8.3 RF event interrupts: ST25DVxxKC registers

To manage RF interrupts, ST25DVxxKC devices have two static registers (GPO, IT_TIME) and two dynamic registers (GPO_CTRL_Dyn, IT_STS_Dyn). Registers to manage I^2C and RF configuration security sessions are also involved.

Table 52. ST25DVxxKC registers related to RF event interrupt

RF access			Registers	I^2C access		
Command	Address	Type		Device select	Address	Type
Read configuration Write configuration	00h	R/W(1)	GPO1	E2 = 1, E1 = 1	0000h	R/W(2)
	01h	R/W(1)	GPO2	E2 = 1, E1 = 1	0001h	R/W(2)
	0Fh	R/W(1)	LOCK_CFG	E2 = 1, E1 = 1	000Fh	R/W(2)
No access	-	-	I2C_PWD	E2 = 1, E1 = 1	0900h	R(3)/W(4)
Present password Write password	-	W0(5)	RF_PWD_0	-	No access	
(Fast) read dynamic configuration	00h	R0	GPO_CTRL_Dyn	E2=0, E1 = 1	2000h	R/W
No access	-		I2C_SSO_Dyn	E2=0, E1 = 1	2004h	R0
			IT_STS_Dyn	E2=0, E1 = 1	2005h	R0

1. Write access granted if RF configuration security session is open and configuration is not locked (LCK_CFG register equals to 0).
2. Write access only if I^2C security session is open.
3. Read access only if I^2C security session is open.
4. Write with I^2C write password command only if I^2C security session is open.
5. Write access only if RF configuration security session is open.

The GPO1 static register selects which RF interrupt is enabled. The GPO_EN bit, when set to 0, disables the GPO output (but not interrupts, which are still reflected in the IT_STS_Dyn register).

Table 53. ST25DVxxKC GPO1 register

GPO1			
Bit	**Name**	**Function**	**Factory value**
b0	GPO_EN	0: The GPO output is disabled. Its state is High-Z (open drain), or 0 (CMOS) 1: The GPO output is enabled. It outputs the enabled interrupts.	1b
b1	RF_USER_EN	0: disabled 1: GPO output level is controlled by manage GPO Command (set/reset)	0b
b2	RF_ACTIVITY_EN	0: disabled 1: GPO output level changes from RF command EOF to response EOF	0b
b3	RF_INTERRUPT_EN	0: disabled 1: GPO output level is controlled by manage GPO Command (pulse)	0b
b4	FIELD_CHANGE_EN	0: disabled 1: a pulse is emitted on GPO when RF field appears or disappears.	1b
b5	RF_PUT_MSG_EN	0: disabled 1: a pulse is emitted on GPO at completion of valid RF write message command.	0b
b6	RF_GET_MSG_EN	0: disabled 1: a pulse is emitted on GPO at completion of valid RF read message command and end of message has been reached.	0b
b7	RF_WRITE_EN	0: disabled 1: a pulse is emitted on GPO at completion of valid RF write operation in EEPROM.	0b

The GPO2 register selects which I^2C interrupts are enabled and sets the duration of the interrupt pulse (for RF_INTERRUPT, FIELD_DETECT, RF_PUT_MSG, RF_GET_MSG and RF_WRITE, I2C_WRITE and I2C_RF_OFF interrupts).

Table 54. ST25DVxxKC GPO2 register

GPO2			
Bit	**Name**	**Function**	**Factory value**
b0	I2C_WRITE_EN	0: Disabled 1: A pulse is emitted on GPO at the end of valid I^2C write operation in EEPROM	0b
b1	I2C_RF_OFF_EN	0: Disabled 1: A pulse is emitted on GPO when I^2C host has successfully switched the RF off	0b
b4 -b2	IT_TIME	Pulse duration = 301 us - IT_TIME * 37.65 us +/- 2 us	011b
b7-b5	RFU	-	000b

The GPO_CTRL_Dyn dynamic register allows the I^2C host to dynamically disable/enable interrupts on the GPO output. It can be used, for example, if the I^2C host is not to be woken up. It is copied from the GPO/GPO_EN bit after device power ON, and is volatile (reset to default value after POR)

Table 55. ST25DVxxKC GPO_CTRL_Dyn register

GPO_CTRL_Dyn			
Bit	**Name**	**Function**	**Factory value**
b6-b0	RFU	-	0b
b7	GPO_EN	0: The GPO output is disabled. Its state is High-Z (open drain), or 0 (CMOS) 1: The GPO output is enabled. It outputs the enabled interrupts.	1b

The IT_STS_dyn dynamic register gives the interrupt status. It can be read by the I^2C host to check which RF event has generated an interrupt on the GPO pin. Reading this register resets all bits. It is a volatile register (reset after POR). If the GPO output is disabled (GPO_EN=0), enabled interrupts still trigger the corresponding IT_STS_Dyn bits.

Table 56. ST25DVxxKC IT_STS_Dyn register

IT_STS_Dyn			
Bit	**Name**	**Function**	**Factory value**
b0	RF_USER	0: Manage GPO reset GPO 1: Manage GPO set GPO	0b
b1	RF_ACTIVITY	0: no RF access 1: RF access	0b

Table 56. ST25DVxxKC IT_STS_Dyn register (continued)

IT_STS_Dyn			
Bit	**Name**	**Function**	**Factory value**
b2	RF_INTERRUPT	0: Manage GPO no interrupt request 1: Manage GPO interrupt request	0b
b3	FIELD_FALLING	0: No field falling 1: Field falling	0b
b4	FIELD_RISING	0: No field rising 1: Field rising	0b
b5	RF_PUT_MSG	0: No message put in mailbox 1: Message put in mailbox	0b
b6	RF_GET_MSG	0: No message read from mailbox 1: Message read from mailbox and end of message has been reached	0b
b7	RF_WRITE	0: no write in EEPROM 1: write in EEPROM	0b

8.4 RF event interrupt configuration: M24LR

Configuration by RF user:

- An RF user can configure which event triggers interrupts on the RFWIP/BUSY pin by issuing a write DO configuration command, with bit 3 of the configuration byte set to the desired value.
- No password is required.

Configuration from I^2C host:

- The I^2C host can configure which event triggers interrupts on pin RFWIP/BUSY by writing the desired value to bit 3 of the configuration byte (@0910h).
- No password is required.

8.5 RF event interrupt configuration: ST25DVxxKC

Configuration by RF user:

- If the RF configuration is locked (LOCK_CFG register = 1), it is not possible to configure RF events.
- If the RF configuration is not locked:
  - The RF user must first open an RF configuration security session by issuing a present password(00h, RF_PWD_0) command with valid RF password 0.
  - The RF user can configure interrupts by issuing a write configuration (@GPO1) to enable events in the GPO1 register. Several RF events can be selected at a time. The GPO_EN bit must be set to 1 in order to enable GPO output.
  - Optionally, the RF user can close the RF configuration security session by issuing a present password command with the wrong RF password 0 (or a different password number, or remove tag from the field).

Configuration from I^2C host:

- The I^2C host must open the I^2C security session by issuing an I^2C present password command.
- The I^2C host can configure interrupts by writing to the GPO1 register. The GPO_EN bit must be set to 1 in order to enable the GPO output.
- Optionally, the I^2C host can close the I^2C security session by issuing an I^2C present password command with the wrong I^2C password.

Temporary enable or disable of the GPO output from the I^2C host:

- The ^2C host can temporarily enable and disable the GPO output by writing the GPO_EN bit in GPO_CTRL_Dyn register.
- No password is required (Write is possible while I^2C security session is closed).
- The change is volatile and doesn't survive a power off.

Checking interrupt status from I^2C host:

- After receiving an interrupt, the I^2C host can check the IT_STS_Dyn register to determine which RF event triggered the interrupt on the GPO pin.

9 Energy harvesting

In M24LR products, when energy harvesting is enabled, if the RF field delivers a minimum power and external devices do not exceed a maximum sink current, power is delivered on the Vout pin. This minimum power and sink current can be configured.

In ST25DVxxKC products, when energy harvesting is enabled, and if the RF field strength is sufficient, power is delivered on V_EH pin. Minimum power and sink current cannot be configured.

9.1 Energy harvesting: M24LR registers

To manage energy harvesting, M24LR devices have one configuration byte and one control register, both always accessible.

Table 57. M24LR registers related to energy harvesting

RF access			Registers	I^2C access		
Command	Address	Type		Device select	Address	Type
Read configuration Write EH configuration Write DO configuration	-	R/W	Configuration byte	E2=1	0910h	R/W
Check EH enable Set reset EH enable	-	R/W	Control register	E2=1	0920h	R/W

Bits 0 and 1 of the configuration byte control the working domain of M24LR energy harvesting. Bit 2 determines the energy harvesting default strategy after power-up. See *Table 51: M24LR Configuration byte* further details.

Bit 0 of the control register allows dynamic enabling or disabling of the energy harvesting output. At boot time, the value of bit 0 is set according to the EH_mode bit. The control register is a volatile register and is reset at POR.

Table 58. M24LR control register

Control register			
Bit	**Name**	**Function**	**Factory value**
b0	EH_Enable	0: disable energy harvesting 1: enable energy harvesting	Depends on EH_mode value
b1	FIELD_ON	0: RF power not sufficient to execute RF commands 1: RF power sufficient to execute RF commands (RO bit)	Depends on RF power
b6-b2	RFU	-	00000b
b7	T_PROG	0: reset to 0 after before each write cycle 1: indicate correct completion of write cycle. (RO bit.)	0b

9.2 Energy harvesting: ST25DVxxKC registers

To manage RF interrupts, ST25DVxxKC devices have one static register (EH_MODE) and one dynamic register (EH_CTRL_Dyn). Registers to manage I^2C and RF configuration security sessions are also involved.

Table 59. ST25DVxxKC registers related to energy harvesting

RF			Registers	I^2C		
Command	**Address**	**Type**		**Device select**	**Address**	**Type**
Read configuration Write configuration	02h	R/W(1)	EH_MODE	E2=1, E1 = 1	0002h	R/W(2)(3)
	0Fh	R/W(1)	LOCK_CFG	E2=1, E1 = 1	000Fh	R/W(2)(3)
No access			I2C_PWD	E2=1, E1 = 1	0900h	R(3)(4)/W(4)(5)
Present password Write password	00h	WO(5)	RF_PWD_0	No access		
(Fast) read dynamic configuration (Fast) write dynamic configuration	02h	R/W	EH_CTRL_Dyn	E2=0, E1 = 1	2002h	R/W

1. .Write access granted if RF system security session is open and system configuration is not locked (LCK_CFG register equals to 0)
2. Write access granted if I^2C system security session is open.
3. Read access granted if I^2C system security session is open.
4. Write access with I^2C write password command, only if I^2C system security session is open.
5. Write access only if RF configuration security session is open.

Note: Bit 0 of the EH_MODE register determines the energy harvesting default strategy after power-up.

The EH_MODE bit is equivalent to the EH_mode bit on M24LR devices.

Table 60. ST25DVxxKC EH_MODE register

EH_MODE			
Bit	**Name**	**Function**	**Factory value**
b0	EH_MODE	0: EH forced after boot 1: EH on demand only	1b
b7-b1	RFU	-	0000000b

Table 61. ST25DVxxKC EH_CTRL_Dyn register

EH_CTRL_Dyn			
Bit	**Name**	**Function**	**Factory value**
b0	EH_EN	0: Disable EH feature 1: Enable EH feature	0b
b1	EH_ON	0: EH feature is disabled 1: EH feature is enabled	0b
b2	FIELD_ON	0: RF field is not detected 1: RF field is present and ST25DVxxKC may communicate in RF	Depends on power source
b3	VCC_ON	0: No DC supply detected on VCC pin 1: VCC DC supply is present	Depends on power source
b4-b7	RFU	-	0b

Bit 0 of the EH_CTRL_Dyn register allows dynamic enabling or disabling of the energy harvesting output. At boot time, the value of bit 0 is set according to the EH_MODE bit. Bit 1 is a status bit that reflects the value of EH_EN bit. EH_CTRL_Dyn register is a volatile register and is reset at POR.

9.3 Energy harvesting configuration

9.3.1 Enabling energy harvesting at M24LR boot

Enabling energy harvesting at boot time by RF user:

- The RF user sets the default energy harvesting strategy at power-up by issuing a write EH configuration command, to write the EH_mode and EH_Cfg bits of the configuration byte.
- No password is required.

Enabling energy harvesting at boot from I^2C host:

- The I^2C host sets the default energy harvesting strategy at power-up by writing the EH_mode and EH_Cfg bits of the configuration byte.
- No password is required.

9.3.2 Enabling energy harvesting at ST25DVxxKC boot

Enabling energy harvesting at boot by RF user:

- If RF configuration is locked (LOCK_CFG register = 1), it is not possible to configure RF events.
- If RF configuration is not locked:
  - The RF user must first open an RF configuration security session by issuing a present password(00h, RF_PWD_0) command with a valid RF password 0.
  - The RF user sets the default energy harvesting strategy at power-up by issuing a write configuration(@EH_MODE, New_EH_MODE) command, to write the EH_MODE bit of the EH_MODE register.
  - Optionally, the RF user can close the RF configuration security session by issuing a present password command with the wrong RF password 0 (or a different password number, or remove tag from the field).

Enabling energy harvesting at boot time from I^2C host:

- The I^2C host must open the I^2C security session by issuing an I2C present password command.
- The I^2C host sets default energy harvesting strategy at power-up by writing the EH_MODE bit in the EH_MODE register.
- Optionally, the I^2C host can close the I^2C security session by issuing an I^2C present password command with the wrong I^2C password.

9.3.3 Temporarily enabling or disabling M24LR energy harvesting

Temporarily enabling or disabling energy harvesting by RF user:

- RF user can temporarily enable or disable energy harvesting by issuing a set reset EH enable command, to write the EH_Enable bit in the control register.
- No password is required.

Temporarily enabling or disabling energy harvesting from I^2C host:

- The I^2C host temporarily enables or disables energy harvesting by writing the EH_Enable bit in the control register.
- No password is required.

9.3.4 Temporarily enabling or disabling ST25DVxxKC energy harvesting

Temporarily enabling or disabling energy harvesting by RF user:

- The RF user can temporarily enable or disable energy harvesting by issuing a write dynamic configuration(@EH_CTRL_Dyn, New_EH_CTRL) command to write EH_EN bit in EH_CTRL_Dyn register.
- No password is required (RF configuration security session closed).

Temporarily enabling or disabling energy harvesting from I^2C host:

- In ST25DVxxKC devices, the I^2C host temporarily enables or disables energy harvesting by writing the EH_EN bit of the EH_CTRL_Dyn regsiter.
- No password is required.
- Change is volatile and doesn't survive a power off.

9.3.5 Checking if energy harvesting is delivering power M24LR

Checking if energy harvesting is delivering power by RF user:

- The RF user can check if energy harvesting is delivering power on Vout pin by issuing a check EH enable command to check the EH_Enable bit of the control register.

Checking if energy harvesting is delivering power from I^2C host:

- The I^2C host checks if energy harvesting is delivering power on the Vout pin, by reading the EH_Enable bit of the control register

9.3.6 Checking if energy harvesting is delivering power ST25DVxxKC

Checking if energy harvesting is delivering power by RF user:

- The RF user can check if energy harvesting is delivering power on the V_EH pin by issuing a read dynamic configuration (@EH_CTRL_Dyn) command to check the EH_ON bit of the EH_CTRL_Dyn regsiter.

Checking if energy harvesting is delivering power from I^2C host:

- The I^2C host checks if energy harvesting is delivering power on V_EH pin, by reading the EH_ON bit of the EH_CTRL_Dyn register.

10 Tag inventory

M24LR devices feature a special inventory-initiated procedure, which allows faster inventory sequence, in addition to the ISO/IEC 15693 standard inventory procedure.

This inventory initiated feature is no longer present in ST25DVxxKC devices, and the ISO/IEC 15693 standard inventory sequence must be used for these products.

11 Tag identification

There are two ways to identify STMicroelectronics ISO/IEC 15693 products:

- With the product code field of the UID
- With the IC reference.

Memory size can also be used to differentiate products.

11.1 Product codes

The product code field for M24LR and ST25DVxxKC devices is defined as shown in *Table 62*.

Table 62. M24LR and ST25DVxxKC product codes

Product	M24LR			ST25DVxxKC					
	04E-R	04K-IE	16K-IE	04K-IE	16K-IE	64K-IE	04K-JF	16K-JF	64K-JF
Product code	010110xxb	010011xxb	001011xxb	50h	51h	51h	52h	53h	53h

Using the I^2C, the user can directly read the product code at the address shown in *Table 64*.

Table 63. Product code field I^2C address

Device	M24LR	ST25DVxxKC
Product code field I^2C address	E2=1, 0919h	E2=1, E1 = 1, 001Dh

RF users can read the product code by issuing an Inventory command and analyzing the product code field of the UID.

The UID of the STMicroelectronics ISO/IEC 15693 products is defined *Table 65*.

Table 64. STMicroelectronics ISO/IEC 15693 products UID

UID	byte 7	byte 6	byte 5	byte 4 to 0
Value	E0h	02h(1)	Product code	IC manufacturer code

1. Manufacturer code 0x02 for STMicroelectronics

11.2 IC Ref and memory size

The IC ref definition for M24LR and ST25DVxxKC products is shown in *Table 66*.

Table 65. M24LR and ST25DVxxKC IC ref values

Product	M24LR			ST25DVxxKC					
	04E-R	16E-R	64E-R	04K-IE	16K-IE	64K-IE	04K-JF	16K-JF	64K-JF
IC Ref	5Ah	4Eh	5Eh	50h	51h	51h	50h	51h	51h

Using the I^2C, the user can directly read the IC Ref and memory size at addresses shown in *Table 67*.

Table 66. IC Ref and Memory size I^2C addresses

Device	M24LR04E-R	M24LR16E-R M24LR64E-R	ST25DVxxKC
IC ref I^2C address	E2=1, 091Ch	E2=1, 091Ch	E2=1, E1 = 1, 0017h
Memory size LSB	E2=1, 091Dh	E2=1, 091Dh	E2=1, E1 = 1, 0014h
Memory size MSB	-	E2=1, 091Eh	E2=1, E1 = 1, 0015h
Block size	E2=1, 091Eh	E2=1, 091Fh	E2=1, E1 = 1, 0016h

RF users can read the IC ref by issuing the get system information command in all versions of M24LR and ST25DVxxKC products.

In M24LR04E-R and ST25DV04KC devices, memory size can also be read with the same command.

In M24LR16E-R and M24LR64E-R devices, the user can read the memory size by issuing a get system information command with Protocol_extension_flag set to 1.

In ST25DV16KC and ST25DV64KC devices, the user can read the memory size by issuing an extended get system information command with bit 3 (VICC memory size) of the parameter request field set to 1.

This is summarized in *Table 67*, *Table 68*, *Table 69* and *Table 70*.

Table 67. M24LR04E-R and ST25DV04KC response to get system information command

SOF	Response_flags	Info_flags	UID	DSFID	AFI	Mem Size	IC ref	CRC16	EOF
-	00h	0Fh	8 bytes	1 byte	1 byte	037Fh	5Ah 50h	2 bytes	-

Table 68. M24LR16E-R and M24LR64E-R response to get system information command with Protocol_extension_flag=0

SOF	Response_flags	Info_flags	UID	DSFID	AFI	IC ref	CRC16	EOF
-	00h	0Bh	8 bytes	1 byte	1 byte	4Eh 5Eh	2 bytes	-

Table 69. M24LR16E-R and M24LR64E-R response to get system information command with Protocol_extension_flag=1

SOF	Response_flags	Info_flags	UID	DSFID	AFI	Mem Size	IC ref	CRC16	EOF
-	00h	0Fh	8 bytes	1 byte	1 byte	0301FFh 0307FFh	4Eh 5Eh	2 bytes	-

Table 70. ST25DV16KC and ST25DV64KC response to get system information command .

SOF	Response_flags	Info_flags	UID	DSFID	AFI	IC ref	CRC16	EOF
-	00h	0Bh	8 bytes	1 byte	1 byte	51h	2 bytes	-

Table 71. ST25DV16KC and ST25DV64KC response to extended get system information command(1)

SOF	Response_flags	Info_flags	UID	DSFID	AFI	Mem Size	IC ref	CRC16	EOF
-	00h	1Fh	8 bytes	1 byte	1 byte	0301FFh 0307FFh	51h	2 bytes	-

1. Response to an extended get system information command with parameter request field equal to 1Fh (DSFID, AFI, memory size, IC ref and MOI requested). Additional parameters can be requested in the parameter request field. See the ST25DVxxKC datasheet *[4]*.

12 ISO/IEC 15693 states

Changing the ISO/IEC 15693 state is done in the same way for M24LR and ST25DVxxKC products, using inventory, select, reset to ready and stay quiet commands. Refer to the ISO/IEC 15693-3 specification *[7]* for more details.

There are nevertheless differences in the following conditions:

- Initial state: Quiet.
- Command received:
  - Reset to ready
  - Request_flags: 001000xxb (option_flag =0, Address_flag=1, Select_flag=0, Inventory_flag=0)
  - UID: incorrect UID of the device included in the reset to ready command.

In the above conditions, the new state after a command is:

- M24LR switches to ready state
- ST25DVxxKC stays in quiet state.

13 Behavior when erroneous RF commands are received

M24LR and ST25DVxxKC products may behave differently when receiving commands with the wrong number of bytes, unknown command codes or commands with the wrong Request_flags. This can lead to some modification in error handling for the RF reader when migrating from M24LR to ST25DVxxKC products.

Depending on the issue in the command received, M24LR and ST25DVxxKC products can either respond with an error or stay quiet. *Table 72 Table 74* and *Table 74* show the difference in answering behavior between M24LR and ST25DVxxKC products in the cases of malformed commands, unknown command codes, and correct and incorrect flags in the Request_flags field.

Table 72. Behavior in case of malformed RF commands with too few or too many bytes (CRC OK)

Malformed Command	M24LR	ST25DVxxKC
Inventory	No answer	
Stay quiet	No answer	
Select	No answer	If too many bytes: error answered If too few bytes: no answer
Reset to ready	No answer	If too many bytes: error answered If too few bytes: no answer
Any other command	No answer	Error answered

Table 73. Behavior in case of unknown command code

Command	M24LR	ST25DVxxKC
Unknown command code	No answer	Error answered

Table 74. Behavior in case of good and wrong flags in the Request_flags field of the RF command (CRC OK)

Command[1] [2]	M24LR[3]	ST25DVxxKC[3]
Inventory	If Request_flags = xxxxx1xxb (inv) and device is not in quiet state: answer Any other case: no answer	
Stay quiet	No answer	
Select	If Request_flags = xx1xxxxxb (addr) and good UID provided: answer If Request_flags = xx1xx1xxb (addr + inv) and any UID provided: answer Any other case: no answer	If Request_flags = xxxxxxxxb and good UID provided: answer - Any other case: no answer
Reset to ready	If Request_flags = xx00x0xxb (no addr + no sel+no inv): answer If Request_flags = xx1xxxxxb (addr) and good UID provided: answer If Request_flags = xxx1xxxxb (sel) and good UID provided and device is in selected state: answer If Request_flags = xx1xx1xxb (addr + inv) and any UID provided: answer If Request_flags = xx00x1xxb (no addr + not sel+inv) and good UID provided and device is not in quiet state: answer Any other case: no answer	If Request_flags = xx00x0xxb (no addr + no sel + no inv) and device is not in selected state: answer If Request_flags = xx1xxxxxb (addr) and good UID provided: answer If Request_flags = xxx1xxxxb (sel) and good UID provided and device is in selected state: answer - - Any other case: no answer
Any other command	If Request_flags = xx00x0xxb (no addr+no sel + no inv) and device is not in quiet state: answer If Request_flags = xx1xxxxxb (addr) and good UID provided: answer If Request_flags = xxx1xxxxb (sel) and good UID provided and device is in selected state: answer If Request_flags = xx1xx1xxb (addr + inv) and any UID provided: answer If Request_flags = xx00x1xxb (no addr + not sel + inv) and good UID provided and device is not in quiet state: answer Any other case: no answer	If Request_flags = xx00x0xxb (no addr+no sel + no inv) and device is not in quiet state: answer If Request_flags = xx1xxxxxb (addr) and good UID provided: answer If Request_flags = xxx1xxxxb (sel) and good UID provided and device is in selected state: answer - - Any other case: no answer

1. Cases where address flag is set in Request_flags field and no UID is provided are considered as commands with too few bytes, and are treated in *Table 72: Behavior in case of malformed RF commands with too few or too many bytes (CRC OK)*.
2. Cases where address flag and selected flags are not set in Request_flags field and UID is provided are considered as commands with too many bytes, and are treated in *Table 72: Behavior in case of malformed RF commands with too few or too many bytes (CRC OK)*.
3. Bold text indicates cases where flags are correctly set.

14 NFC file format

NFC file format is defined in the NFC Forum Type 5 Tag specification *[8]*.

ST25DVxxKC products are based on the NFC Type 5 Tag specification, and thus support the NFC file format as described by the NFC Forum.

M24LR products were released prior to the NFC Forum Type 5 Tag specification, and some adaptation has to be made to support the CC file format in order to support high-density memory devices.

This is why M24LR16E-R and M24LR64K-R need to be formatted with a different CC file than ST25DVxxKC products.

Low density devices, M24LR04E-R, ST25DV04KC share the same CC file format.

Refer to application note AN3408 ‘Using LRIxx, LRISxx, M24LRxx-R and M24LRxxE-R products as NFC vicinity tags’ *[5]* for details of the CC file format to be used with M24LR16E-R and M24LR64E-R devices.

Refer also to the NFC Forum Type 5 Tag specification for the CC file standard format to be used with the M24LR04E-R and ST25DVxxKC product family.

15 Reference documents

Table 75. Reference documents

Reference	Revision	Title
[1]	Latest version	M24LR04E-R datasheet, STMicroelectronics
[2]		M24LR16E-R datasheet, STMicroelectronics
[3]		M24LR64E-R datasheet, STMicroelectronics
[4]		ST25DV04KC ST25DV16KC ST25DV64KC datasheet, STMicroelectronics
[5]		AN3408 (application note) ‘Using LRIxx, LRISxx, M24LRxx-R and M24LRxxE-R products as NFC vicinity tags’, STMicroelectronics
[6]		AN4054 (application note): ‘Comparison of RF addressing modes of low-density and high-density ISO/IEC 15693 devices’, STMicroelectronics
[7]		International standard ISO/IEC 15693-3: Identification cards - Contactless integrated circuit cards - Vicinity cards
[8]		Type 5 Tag specification, NFC Forum
[9]	Pre-release	Digital protocol - Technical specification, NFC Forum

16 Revision history

Table 76. Document revision history

Date	Revision	Changes
23-Jun-2021	1	Initial release