How to select a 32 MHz HSE oscillator for STM32WL5x/Ex MCUs

Introduction

This application note gives recommendations on the timing device selection to provide 32 MHz HSE clock to STM32WL series microcontrollers (MCUs). This is to guarantee requested performances at low bill of material (BOM) cost.

The main timing constraints to consider are linked to the following:

- targeted application
- modulation, protocols
- maximum output power
- temperature conditions
- STM32WL package, board/module layout

Once a board prototype is done, measurements are recommended using the methodology described in this document.

1 General information

The STM32WL Series microcontrollers are based on the Arm®Cortex®-M processor.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 1. Acronyms and abbreviations

Acronym	Definition
FM	Frequency modulation
FSK	Frequency-shift keying
LoRa®	Long-range radio technology
LoRaWAN®	LoRa wide-area network
RC	Region configuration
Timing device	XO or TXO
TCXO	Temperature compensated crystal oscillator
XO	Crystal oscillator

Reference documents

[1] Application note *Precise HSE frequency and startup time tuning for STM32 wireless MCUs* (AN5042)

[2] Application note *Optimized RF board layout for STM32WL Series* (AN5407)

[3] Data brief *Reference designs for STM32WL5x and STM32WLEx microcontrollers* (DB4597)

2 XO/TCXO comparison

The table below summarizes the main differences between XO (crystal oscillator) and TCXO (temperature compensated XO):

- An XO is more efficient on power consumption, startup time, and BOM cost.
- A TCXO is more efficient on frequency accuracy and frequency variation over temperature changes. It also removes layout constraints.

Table 2. XO/TCXO comparison

Parameter	XO	TCXO	Comments(1)
BOM cost	X	-	TCXO is approximately 5x more expensive than XO.
Power consumption	X	-	TCXO consumes approximately 10x more than XO.
Startup time(2)	X	-	TCXO needs approximately 10x more time than XO.
Frequency accuracy	-	X	TCXO is approximately 10x more accurate than XO.
Frequency drift	-	X	
PCB/module layout constraints	-	X	XO brings more implementation constraints than TCXO.

1. *Based on typical/average specifications.*
2. *Time needed to reach the target frequency within its tolerance range, and the rate of frequency variation range (in Hz/sec).*

3 XO/TCXO selection

This section provides some general guidelines but results depend on the application and the constraints.

If an XO is selected for one of the advantages listed in the previous section, the measurement methodology described in Section 6 Frequency drift measurement is strongly recommended to validate this choice.

In the rest of this document:

- The "ppm requirements" must be understood by cumulating the tolerance on both Tx and Rx sides.
- The gateway uses a highly accurate TCXO with, for example, a 3 ppm accuracy to be checked in the deployment.
- Bandwidths are double-side band (DSB).
- The ppm values are single-side band (SSB).

3.1 LoRa requirement

The table below shows that the allowed accuracy for HSE 32 MHz varies significantly with the bandwidth:

- For bandwidth ≥ 125 kHz, XO is always suitable.
- For bandwidth < 125 kHz, it depends on the maximum output power to be delivered.

Table 3. Absolute accuracy of LoRa radio clock for US915 bands

Bandwidth (kHz)	Accuracy of LoRa radio clock (ppm) for various US915 bands		
	SF5 to SF10	SF11	SF12
31.25	8.5		
62.5	17.1		
125	34.2		
250	68.3		50.0
500	136.3	100	50.0

3.2 FSK requirement

For given baudrate, frequency deviation, and Rx bandwidth, the following equation must be fulfilled:

$$\text{Re}\,ceiver\ bandwith\ (kHz) \geq baudrate(kbps) + 2 \times frequency\ \ deviation\ (kHz) + frequency\ error\ (kHz)$$

This gives the following frequency error:

$$Accuracy\ requirement\ (ppm) \geq \frac{(receiver\ bandwidth - baudrate - 2 \times frequency\ deviation)}{F_{rf} \times 1^6}$$

Table 4. Accuracy requirement of FSK radio clock for US915 bands

Baudrate (kbit/s)	Frequency deviation (kHz)	Receiver bandwidth (kHz)	Accuracy requirement (ppm)
0.6	0.8	4.8	1.4
1.2	5	19.5	4.5
4.8	5	23.4	4.7
50	25	117.3	9.5
50	25	156.2	30.7
150	62.5	312	20.2

This section does not give specifications depending on each protocol, but only general guidelines. Specific application requirements must be clarified, and the frequency drift measurement methodology described in Section 6 Frequency drift measurement must be applied to validate the design and timing device selection.

3.3 Sigfox™ requirement

The Sigfox certification requests a drift minimum. According to the zones and to the passage in the emission, the drift can be:

- in a transient of 30 Hz/s during 320 ms for RC1, RC3, and RC5
- in an established mode of 20 Hz/s during 1.76 s for RC2 and RC4

4 Implementation techniques

4.1 TCXO implementation

There are no specific constraints. Examples are described in reference designs detailed in [2] and [3].

4.2 XO implementation

When an XO is used, a thermal barrier must always be added (as described in the reference designs), in order to reduce the heating impact.

4.2.1 XO temperature compensation technique

Three independent parameters define the XO accuracy:

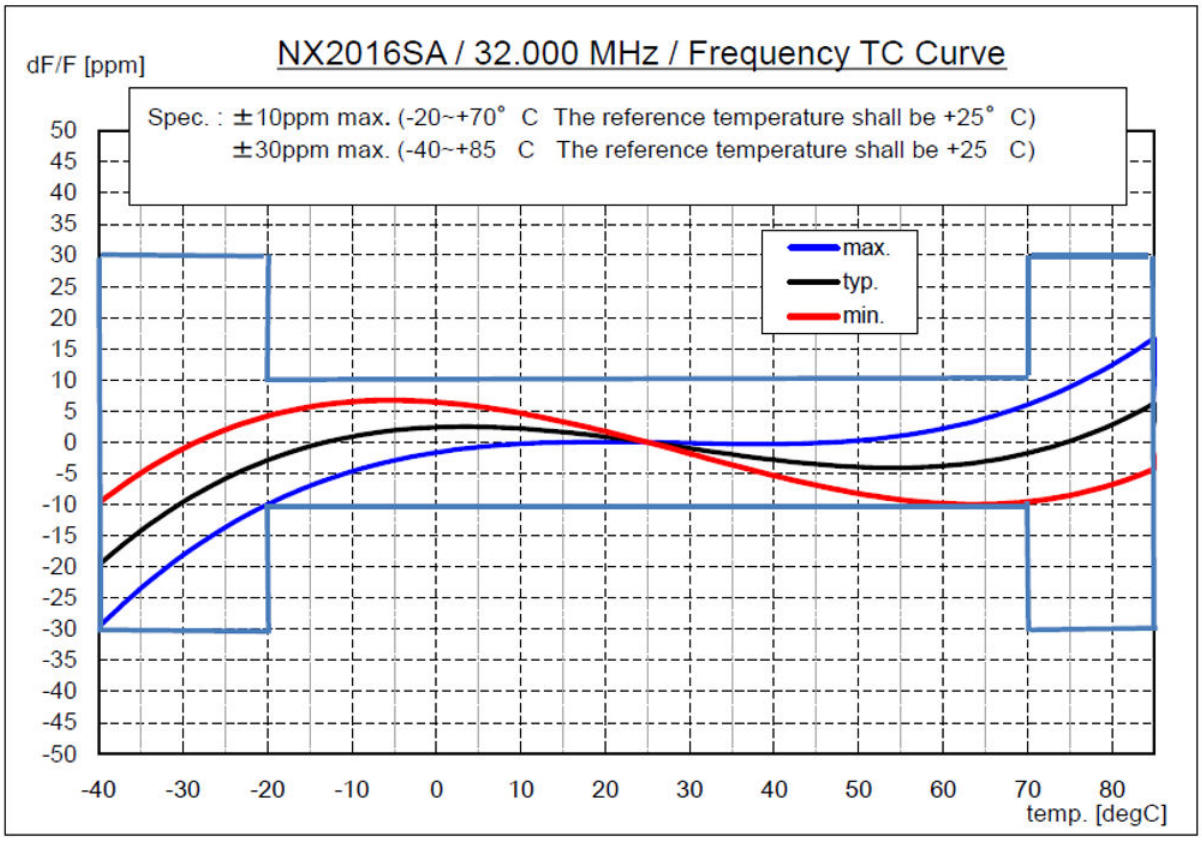
- the initial accuracy (typically ±10 ppm)
- the accuracy depending on temperature (typically ±10 ppm for -20 to +70°C, and ±30 ppm for -40 to +85°C)
- the aging accuracy (typically ±10 ppm)

Some internal capacitor banks can be used to fine-tune the reference frequency.

A 32 MHz calibration phase is recommended at production stage. This is done by storing a specific value in these capacitor banks. Figure 1 shows the frequency variation versus temperature.

To reduce the ±30 ppm accuracy that depends on temperature, the temperature is typically measured before each transmission with an internal or external temperature sensor. The impact of this correction depends if the user considers the worst cases specified in the XO datasheet, or only some points of the curve at the production phase.

Figure 1. XO frequency versus temperature



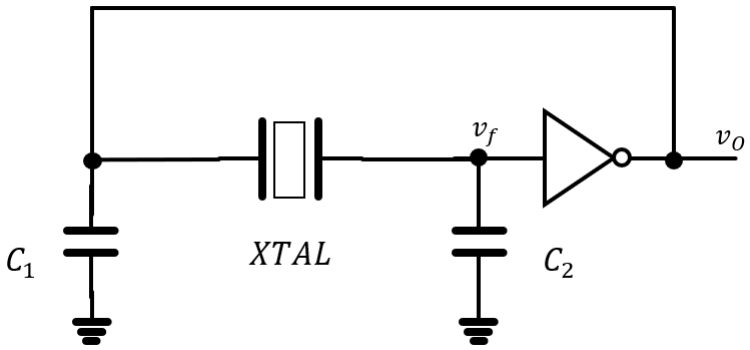
WIth this technique, an XO can be used from -40 to +85°C, even though it is specified out of the application specifications.

4.2.2 XO with external series capacitance

The XO frequency variation with temperature is due to:

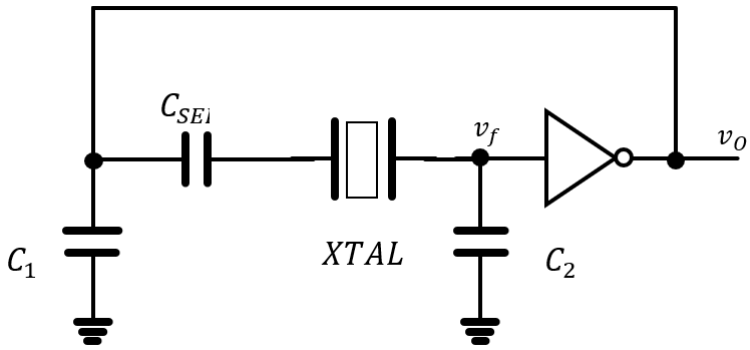
- the internal oscillator temperature sensitivity: can be decreased by increasing internal foot capacitances
- the external crystal temperature sensitivity: can be decreased by adding an external series capacitance (HSE calibration selects a higher internal capacitance value)

Figure 2. Standard XO implementation



$$C_L = \frac{C_1 C_2}{C_1 + C_2} + C_{STRAY} \quad where\ C_{STRAY}\ is\ 3\ or\ 6\ pF.$$

Figure 3. XO with external series capacitance



If $C_1 = C_2 = C_{Bank}$

So,

$$C_L = \frac{C_{Bank}(C_{STRAY} + C_{SERIE})}{2(C_{Bank} + C_{STRAY}) + C_{SERIE}}$$

$$C_{SERIE} = \frac{2C_L(C_{Bank} + C_{STRAY})}{C_{Bank} - C_L}$$

For:

$C_{Bank} > C_L$

A typical value of C_{SERIE} = 60 pF is recommended. It means $C_1 = C_2$ = 27 pF. The clock drift is then reduced by approximately 50%.

4.3 Implementation versus constraints

Depending on the application (modulation, temperature range, protocol, Tx output power), it is recommended to use some of the proposals described above. The table below summarizes the impact of the proposed implementation techniques versus the main constraints.

Table 5. Timing device implementation versus constraints

Implementation	Impact on main constraints		
	Tolerance	Frequency drift	Frequency rate
TCXO	+++	+++	+++
XO with thermal barrier	-	+	++
XO with external capacitance	-	++	++
XO with temperature compensation	++	-	-

5 Recommendations versus various protocols

Hypothesis:

- LoRa respects LoRaWAN protocol requirements.
- BPSK respects Sigfox protocol requirements.
- (G)FSK is based on other protocols with low requirements (to be checked vs the application protocol).
- XO implemented with thermal barrier (see [2]) and calibration for initial accuracy compensation.

5.1 STM32WL packages and thermal characteristics

STM32WL devices are available in UFBGA73 (5 x 5 mm) and UFQFPN48 (7 x 7 mm), with associated thermal characteristics detailed in the table below.

Table 6. STM32WL package thermal characteristics

Symbol	Parameter	Thermal characteristic (°C/w)
Θ_{JA}	Thermal resistance junction-ambient UFBGA73 UFQFPN48	 43.4 27.4
Θ_{JB}	Thermal resistance junction-board UFBGA73 UFQFPN48	 27.2 11.7
Θ_{JC}	Thermal resistance junction-top case UFBGA73 UFQFPN48	 11 8.5

5.2 STM32WL UFBGA73 package

5.2.1 EU868 and US915 bands

The table below summarizes the possibilities for carrier frequency between 860 and 930 MHz.

Note: TCXO is the recommended solution.

- Sigfox_LP (RC1, RC3c, RC5, RC6, RC7) is 100 bit/s uplink data rate.
- Sigfox_HP (RC2, RC4) is 600 bit/s uplink data rate.

Table 7. Recommendations for STM32WL UBGA73 for EU868 and US915

Temperature range (°C)	Tx output	Protocol	32 MHz timing device
-40 to +85	LP up to 15 dBm	LoRaWAN	XO
	HP up to 22 dBm		TCXO
	LP up to 15 dBm	Sigfox_LP	XO(1)
	HP up to 17 dBm	Sigfox_HP	XO(1)(2)
	HP up to 22 dBm		TCXO

1. *Sigfox certification is done at +25 °C. Nevertheless, it is recommended to make a firmware temperature compensation if the device is used below -20 °C and above 70 °C.*
2. *An additional external capacitance is recommended to reduce the frequency drift.*

5.2.2 CN470 and CN433 bands

The table below summarizes the possibilities for carrier frequency between 430 and 510 MHz.

Note: TCXO is the recommended solution.

Table 8. Recommendations for STM32WL UBGA73 for CN470 and CN433

Temperature range (°C)	Tx output	Protocol	32 MHz timing device
-40 to +85	LP up to 15 dBm	LoRaWAN	XO
	HP up to 22 dBm		TCXO
	LP up to 15 dBm	Sigfox_LP (RC1, RC3c, RC5, RC6, RC7)	XO(1)
	HP up to 17 dBm	Sigfox_HP (RC2, RC4)	XO(1)(2)
	HP up to 22 dBm		TCXO

1. *Sigfox certification is done at +25 °C. Nevertheless, it is recommended to make a firmware temperature compensation if the device is used below -20 °C and above 70 °C.*
2. *An additional external capacitance is recommended to reduce the frequency drift.*

5.3 STM32WL UFQFPN48 package

Implementing a solution based on a proper thermal barrier and a series capacitance make possible to use an XO for all use cases.

If there is no resource to fine-tune the layout and to measure the frequency drift in extreme conditions, it is recommended to use a TCXO.

6 Frequency drift measurement

This section proposes a methodology for frequency drift measurement on STM32WL devices to test them against LoRa frequency drift specification.

Instruments

- spectrum analyzer (SA, R and S FSV)
- temperature chamber (TC, Votsch VT4002)

Methodology

For an STM32WL MCU, the frequency drift after a certain time has to be measured (using an SA) versus temperatures between -40 and to 85°C (using a TC).

Before each SA frequency drift measurement, the device under test (DUT) must be present in the TC at the designated temperature. Tx is turned ON in continuous wave (unmodulated carrier) mode, at a certain frequency and output power level. Since the LoRa compliance is tested, frequency and power level settings given in the table below are the most important.

Table 9. Maximum measured output power use case

LoRa band	Carrier frequency (MHz)	Output power (Pout in dBm)
US	915	High-power mode, Pout_max at around 21dBm
EU high	868	Low-power mode, Pout_max at around 14dBm
EU low	434	
China low	490	High-power mode, Pout_max at around 17dBm

To measure the drift from its beginning, the SA drift measurement must be triggered by the RF output of the DUT, which is done by the SA trigger functionality. The SA starts measuring the carrier frequency offset (Hz) versus time (sec), using the FM analog demodulation of the SA, considering the SA settings listed below:

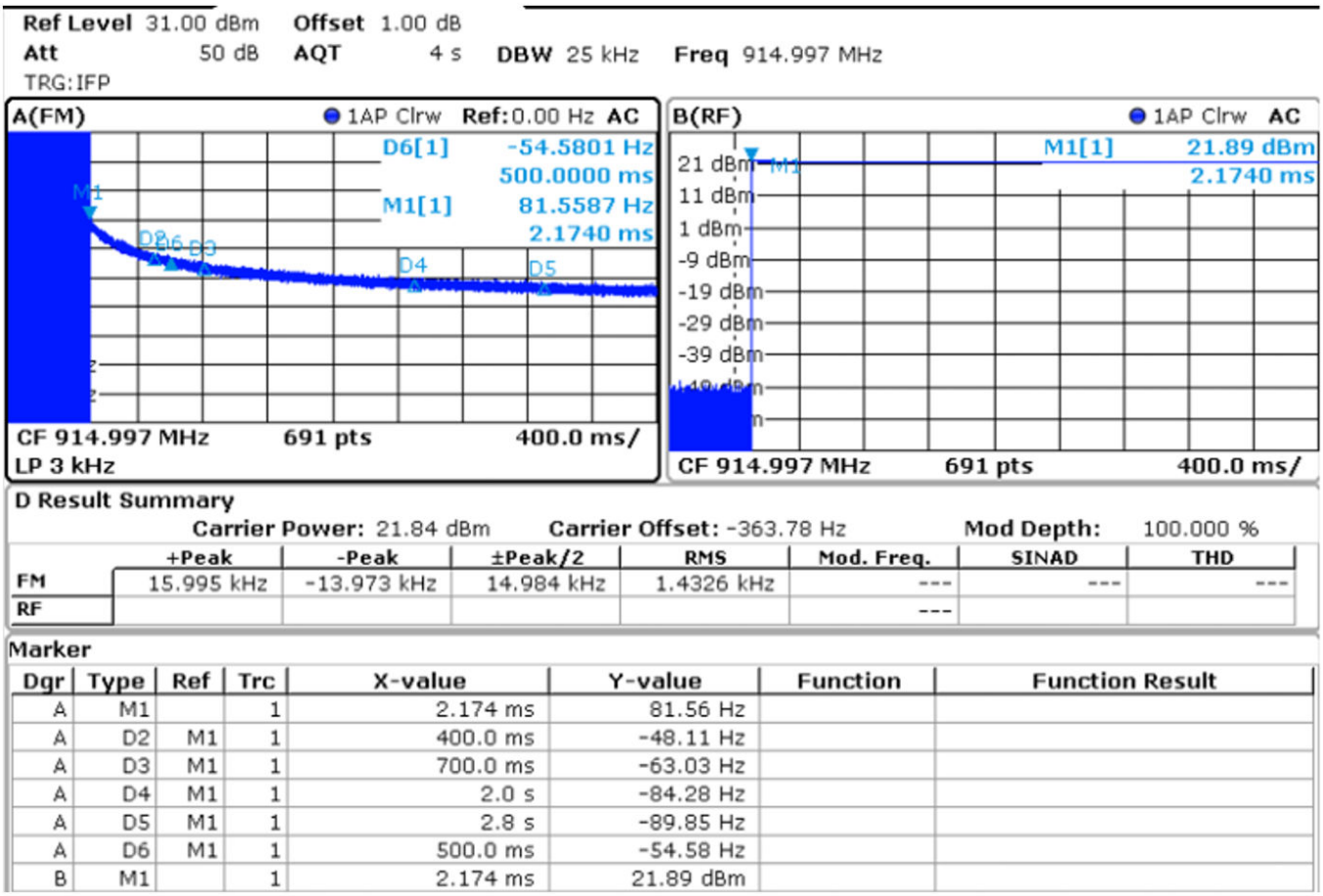
- SA mode: FM analog demodulation
- Deviation per division = 40 kHz
- Reference position = 50%
- Reference value = 0 Hz
- AF coupling = AC
- dBw (demodulation bandwidth) = 25 kHz
- Center frequency = carrier frequency (measured by the SA using the spectrum mode)
- Measurement time = 4 s
- AF filter: low pass at 3 kHz
- Trigger IF
- Trigger level = -10 dBm
- Trigger polarity: positive
- Trigger offset = -400 ms

The figure below shows measurement results on the SA screen:

- Upper left plot: frequency drift (40 Hz/division) versus time (400 ms/division)
  D2, D3, D4, and D5 markers are used to measure the drift in Hz after 0.4, 0.7, 2, and 2.8 seconds respectively. This is done to test drift values (Y-value in the Marker part at the bottom) versus LoRa frequency drift specification (±40.69 Hz after 400 and 700 ms for all spreading factors, and ±162.7 6Hz after 2 and 2.8 seconds for SF11/12 in low-data-rate optimize mode).
- Upper right plot: DUT measured output power

Note: On both plots, M1 is the start of drift measurement when the DUT Tx output jumps to Pout_max = 21.89 dBm (US band scenario). There is noise before M1.

Figure 4. STM32WL frequency versus temperature



D Result Summary

Carrier Power: 21.84 dBm Carrier Offset: -363.78 Hz Mod Depth: 100.000 %

	+Peak	-Peak	±Peak/2	RMS	Mod. Freq.	SINAD	THD
FM	15.995 kHz	-13.973 kHz	14.984 kHz	1.4326 kHz	---	---	---
RF					---		

Marker

Dgr	Type	Ref	Trc	X-value	Y-value	Function	Function Result
A	M1		1	2.174 ms	81.56 Hz		
A	D2	M1	1	400.0 ms	-48.11 Hz		
A	D3	M1	1	700.0 ms	-63.03 Hz		
A	D4	M1	1	2.0 s	-84.28 Hz		
A	D5	M1	1	2.8 s	-89.85 Hz		
A	D6	M1	1	500.0 ms	-54.58 Hz		
B	M1		1	2.174 ms	21.89 dBm		

Revision history

Table 10. **Document revision history**

Date	Version	Changes
24-Mar-2023	1	Initial release.
25-Sep-2023	2	Updated: • Title • Figure 4. STM32WL frequency versus temperature

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