

How to use VREFBUF peripheral on STM32 MCUs and MPUs

Introduction

The applicable STM32 series devices (see [Table 1](#)) embed a very precise buffered reference voltage VREFBUF that can be used:

- As an internal voltage reference, for peripherals like ADC or DAC
- As an external voltage reference, through the VREF+ pin.

The purpose of the VREFBUF peripheral is to provide an accurate reference voltage with limited changes over temperature variations, supply variations, or product lifetime.

The VREFBUF peripheral has several features like:

- Output voltage reference scale selection
- Output voltage reference Tuning/trimming
- Output mode control in order to use an internal or external reference.

The VREFBUF structure is based on a low-drop output regulator design with a compensation circuitry to optimize its accuracy within the application environment including the current load on VREF+.

Table 1. Applicable products

Type	Product Series/Lines ⁽¹⁾
Microcontrollers	STM32G0 series
	STM32G4 series
	STM32H5 series
	STM32H7 series
	STM32L4 series
	STM32L4+ series
	STM32L5 series
	STM32U5 series
	STM32WBx5 line
	STM32WL series
Microprocessors	STM32MP1 series

1. *This application note applies only to products with:*
 - *presence of a VREFBUF peripheral*
 - *VREF+ ball/pin not internally connected to VDD nor VDDA.**Refer to product datasheet.*

1 General information

This document applies to STM32 Arm[®]-based microprocessors and microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

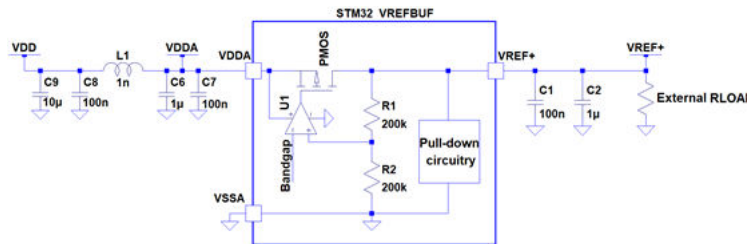


2 VREFBUF peripheral principle

The VREFBUF peripheral is a low-drop output regulator powered by the analog supply V_{DDA} . The VREFBUF output is always connected to the VREF+ pin and the associated external capacitors C1 and C2. The VREFBUF output and the VREF+ are always connected internally to the DAC and the ADC reference inputs. There are several output voltage scales available (depending on STM32 series) which can be fine-adjusted by the application with the peripheral bit registers (some scales are calibrated/trimmed during factory test).

Note: The VREF+ pin is double-bonded with V_{DDA} on some packages. In these packages the internal voltage reference buffer is not available.

Figure 1. STM32 VREFBUF peripheral simplified schematic



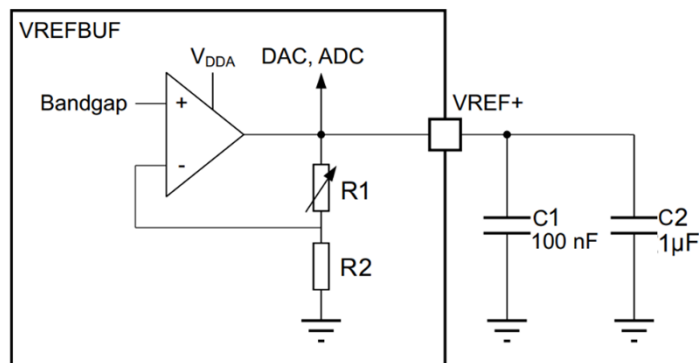
2.1 Principle and circuitry

The VREFBUF voltage regulator architecture is based on a regulation loop with an amplifier. A simplified model of the circuitry using a PMOS transistor is provided in the following figure. The output voltage regulation depends on the Bandgap voltage and the $R1/R2$ resistors according the following formula:

$$\text{VREFBUF output} = \text{Bandgap} \times \left(1 + \frac{R1}{R2}\right)$$

The $R1$ resistor is variable in order to provide the following features: output scale selection and trimming.

Figure 2. VREFBUF peripheral simplified principle



For example: the VREFBUF of the STM32G4 series supports three voltage scales: 2.048 V , 2.500 V and 2.900 V. The output voltage selection is performed changing the $R1$ resistor value. The selection of $R1$ value is performed with the VREFBUF register configuration. Considering VREFBUF bandgap voltage equals to 1.25 V, the following table shows the relationship between VREFBUF output voltage, Bandgap, and $R1/R2$ resistors for the STM32G4 series.

Table 2. STM32G4 series VREFBUF output with $R1$ and $R2$ resistors example

VREFBUF output voltage on VREF+ pin	Bandgap	$R1/R2$ ratio	$R1(k\Omega) / R2(k\Omega)$
2.048 V	1.25 V	0.6384	127.68 / 200

VREFBUF output voltage on VREF+ pin	Bandgap	R1/R2 ratio	R1(k Ω) / R2(k Ω)
2.500 V	1.25 V	1	200 / 200
2.900 V	1.25 V	1.32	264 / 200

2.2 Peripheral functional modes and status

The VREFBUF peripheral has several control bit registers available: ENVR, HIZ, VRS, VRR, and TRIM. The following paragraphs describe the behavior change on the peripheral.

2.2.1 ENVR and HIZ bits

- ENVR bit: simply enables or disables the VREFBUF peripheral.
- HIZ bit: enables or disables the VREFBUF output high impedance.

The following table describes the VREFBUF peripheral behavior with ENVR/HIZ bits.

Table 3. VREFBUF peripheral behavior with ENVR/HIZ bits

ENVR	HIZ	Mode	Description
0	0	Pull-down	VREFBUF is disabled, VREF+ pin is pulled down to V_{SSA} .
	1	External voltage reference	VREFBUF is disabled, VREF+ is an input floating pin. An external reference voltage can be connected for analog peripherals usage.
1	0	VREFBUF voltage reference	VREFBUF is enabled and buffering VREF+ pin with VREFBUF_OUT voltage.
	1	VREFBUF hold	VREFBUF is enabled without output buffer. Voltage on VREF+ pin is hold with the external capacitor. This is reducing VREFBUF power consumption.

2.2.2 VRS bits

- VRS bits: select the VREFBUF_OUT voltage reference scale.

The following table list the available VREFBUF output voltage scales for several STM32 series. The VRS size depends on the STM32 series.

Table 4. Example of VREFBUF output voltage per STM32 series

STM32 Series	VRS size (bits)	Available VREFBUF output voltage scale ⁽¹⁾ ⁽²⁾					
		1.5 V	1.8 V	2 V	2.5 V	2.9 V	-
STM32G0	1	-	-	0	0	-	-
STM32G4	2	-	-	0	0	0	-
STM32H5	3	-	0	0	0	-	-
STM32H7	3	0	0	0	0	-	-
STM32L4	1	-	-	0	0	-	-
STM32L4+	1	-	-	0	0	-	-
STM32L5	1	-	-	0	0	-	-
STM32U5	3	0	0	0	0	-	-
STM32WB	1	-	-	0	0	-	-
STM32WL	1	-	-	0	0	-	-
STM32MP1	3	0	0	0	0	-	-

1. 0 = available VREFBUF output voltage.

2. Refer to product datasheet for VREFBUF output voltage scale accuracy.

Table 5. STM32G4 series VREFBUF output voltage with VRS value

STM32 series	VRS[1:0]	VREFBUF output voltage on VREF+ pin
STM32G4	00	2.048V
	01	2.500V
	10	2.900V

2.2.3
VRR

- VRR bit (voltage reference ready) is set when the VREFBUF output voltage accuracy is within 1% of the selected voltage range. When HIZ bit is set, the VRR is stuck at 1 and therefore it is up to the application to ensure that VREFBUF_OUT voltage remains in the selected scale voltage limits.

2.2.4
TRIM

- TRIM bits control the VREFBUF adjustable trimming code.

3 VREFBUF constraints in application

The following sections describe the application constraints when VREFBUF is used.

3.1 VREFBUF trimming circuitry

STM32 peripherals like the ADC or the OPAMP may embed a self-calibration circuitry but some others like internal oscillators or VREFBUF require a measured trimming performed during factory process.

A specific parameter (output voltage for VREFBUF case) is adjusted by trimming, based on a register word value. The VREFBUF output voltage is trimmed at factory with different conditions depending on the STM32 series. The product datasheet provides the trimming temperature and voltage range details.

In most cases the parameter variation is linear with the register word and the default value for centered parameter is the median code. Each trimming register step changes the trimmed parameter with a given resolution step. For example, the VREFBUF typical trimming step is $\pm 0.05\%$ equivalent to 1.25 mV when VREFBUF output is 2.5 V (VRS = 1). If the calibration operation is correctly performed the adjusted parameter accuracy is within half of the trimming step.

The VREFBUF trimming operation needs the following steps to be completed:

1. Set median code value in the TRIM register and measure the VREFBUF output.
2. Calculate the difference between the measured voltage and the target voltage. Calculate the trimming code steps to apply.
 - a. Trim code to apply = median code – round nearest (ΔV / typical trim step voltage)
3. Apply the adjusted trimming code and measure again the VREFBUF output voltage to verify its accuracy after trimming.

The following table provides trimming operation steps examples.

Table 6. Trimming operation example for STM32G4 2.5 V VREFBUF output voltage

Example	Trimming step 1			Trimming step 2		Trimming step 3		Trimming results	
	Initial trimming code	Initial Voltage (mV)	ΔV vs 2.5 V (mV)	Trimming step correction	Adjusted trimming code	Trimmed Voltage (mV)	Voltage Accuracy (mV)	Trimming code Accuracy	
#1	32	2503.83	3.83	-3	29	2500.08	0.08	0.06	
#2	32	2498.28	-1.72	1	33	2499.53	-0.47	-0.38	
#3	32	2503.88	3.88	-3	29	2500.13	0.13	0.10	
#4	32	2497.53	-2.47	2	34	2500.03	0.03	0.03	
#5	32	2491.42	-8.58	7	39	2500.17	0.17	0.14	
#6	32	2498.85	-1.15	1	33	2500.10	0.10	0.08	

3.2 VREFBUF trimming with an external voltage and ADC

The VREFBUF output can be trimmed with the ADC peripheral and an external accurate voltage source. When the VREFBUF is used as ADC reference, there is a proportional/linear factor between the ADC input voltage and the ADC digital output:

$$\text{Digital output} = \text{int}\left(\frac{V_{in} \times 2^N}{V_{REF+}}\right) = \text{int}\left(\frac{V_{in} \times 2^{12}}{V_{REF+}}\right) \text{ with } V_{REF+} = V_{REFBUF} \text{ and } 12 \text{ bits ADC}$$

For example, assuming 1.800 V is applied at the input of the ADC, producing a digital output of 2961 LSB, the VREFBUF voltage is calculated as follows:

$$V_{REFBUF} = V_{in} \times \frac{2^N}{\text{digital output}} = 1.800 \times \frac{4096}{2953} = 2.4967 \text{ V}$$

There is no trimming correction to apply because the VREFBUF output is only 3.3 mV away from 2.5 V.

It is important to apply a high voltage input signal to minimize the ADC offset error, however the ADC gain error should be considered as well. The offset error can be cancelled and the VREFBUF estimation improved by performing the acquisition of 2 input voltages. The following table presents the accuracy performance of this method using various input voltage configurations.

Table 5 STM32 ADC digital output code /VREFBUF estimation

Table 7. STM32 ADC digital output code /VREFBUF estimation

Method	Input voltage (V)	ADC condition	ADC digital output (LSB)	VREFBUF voltage estimation (V)	Estimation error (mV) (real VREFBUF = 2.051 V)
Single point	0.1	Theoretical	200	2.048	3
	1.8		3595	2.0508	0.15
Two points	1.8 - 0.1 = 1.7		3595-200 = 3395	2.051	0.016
single point	0.1	ADC offset error=2 LSB	202	2.0277	23.3
	1.8	ADC gain error 2.5 LSB	3599	2.0486	2.43
Two points	1.8 - 0.1 = 1.7		3599-202 = 3397	2.04981	1.2

In order to get the most accurate estimation of the VREFBUF voltage via the STM32 ADC digital output, one can use 2 input voltage points to minimize the ADC offset error and achieve more accurate VREFBUF voltage calculation results.

3.3 VREFBUF trimming with the internal V_{REFINT} voltage and the ADC

Another interesting method to improve the VREFBUF trimming is to use the V_{REFINT} calibration (VREFINT_CAL) and the ADC peripheral. During the production process, the V_{REFINT} value is stored in the product memory for a given reference (V_{REF+} = 3.0 V ± 10m V for STM32G4 series) and a given temperature (30 °C ± 5°C for STM32G4 series).

One can calculate the VREFBUF voltage value directly from the following procedure:

1. Retrieve the V_{REFINT} conversion value result at VREFINT_CAL address:
 - a. The conversion value is 0x067B or 1659 in decimal
 - b. The equivalent voltage is $1659 \times (3 \text{ V} / 2^{12}) = 1.2151 \text{ V}$ with factory conditions (3 V and 30 °C)
2. Configure the 12-bit ADC peripheral and acquire the V_{REFINT} voltage while VREFBUF is the ADC reference.
3. Retrieve the V_{REFINT} average conversion value:
 - a. The average conversion value is 1989.2 (10 acquisition samples) 0x067B or 1659 in decimal
 - b. Calculating VREFBUF voltage from the equation: $1989.2 \times (VREFBUF / 2^{12}) = 1.2151 \text{ V}$
 - c. $VREFBUF = (1.2151 / 1989.2) \times 2^{12} = 2.5020 \text{ V}$

With this simple firmware operation, the VREFBUF voltage can be simply retrieved using the ADC peripheral and the V_{REFINT} calibrated input.

3.4 Minimum VDDA supply voltage

The VREFBUF peripheral circuitry is based on a low-drop voltage regulator. To operate normally and provide an accurate output, the VREFBUF supply voltage (V_{DDA}) must remain within a few hundred of millivolts around its nominal value. When the supply voltage drops under the minimum supply margin, the VREFBUF operates in degraded mode and the VREFBUF output voltage follows the V_{DDA} supply drop. The minimum voltage margin (indicated in the product datasheet) depends on the temperature, the silicon process, and the output current load. The following table presents the degraded mode parameter for STM32G4 series when VREFBUF output is 2.5 V and according V_{DDA} supply variations and output current load.

Table 8. VREFBUF degraded mode example

VREFBUF supply	VREFBUF OUTPUT (VRS = 1)	Operation mode
$1.65\text{V} \leq V_{DDA} \leq 2.8 \text{ V}$	$\min(V_{DDA} - 250 \text{ mV}, 2.5 \text{ V})$	Degraded
$V_{DDA} \geq 2.8 \text{ V}$	2.5 V	Normal

3.5 VREFBUF output decreases when VRS changes

The VREFBUF circuitry is designed to drive/source current only. If in the application the VREFBUF output voltage decrease with VRS change, it is important to proceed with the following operation in order to obtain the correct and accurate output voltage:

- Disable VREFBUF with HIZ = 0 to discharge the output voltage on VREF+ with the VREFBUF V_{SSA} pulldown.
- Configure the VRS register value.
- Enable the VREFBUF with HIZ = 1 and monitor the VRR bit status until the output reaches the requested level.

4 VREFBUF application examples

The following section describes analog oriented applications using the VREFBUF reference peripheral with analog-to-digital converter (ADC), digital-to-analog converter (DAC) or a resistor voltage divider.

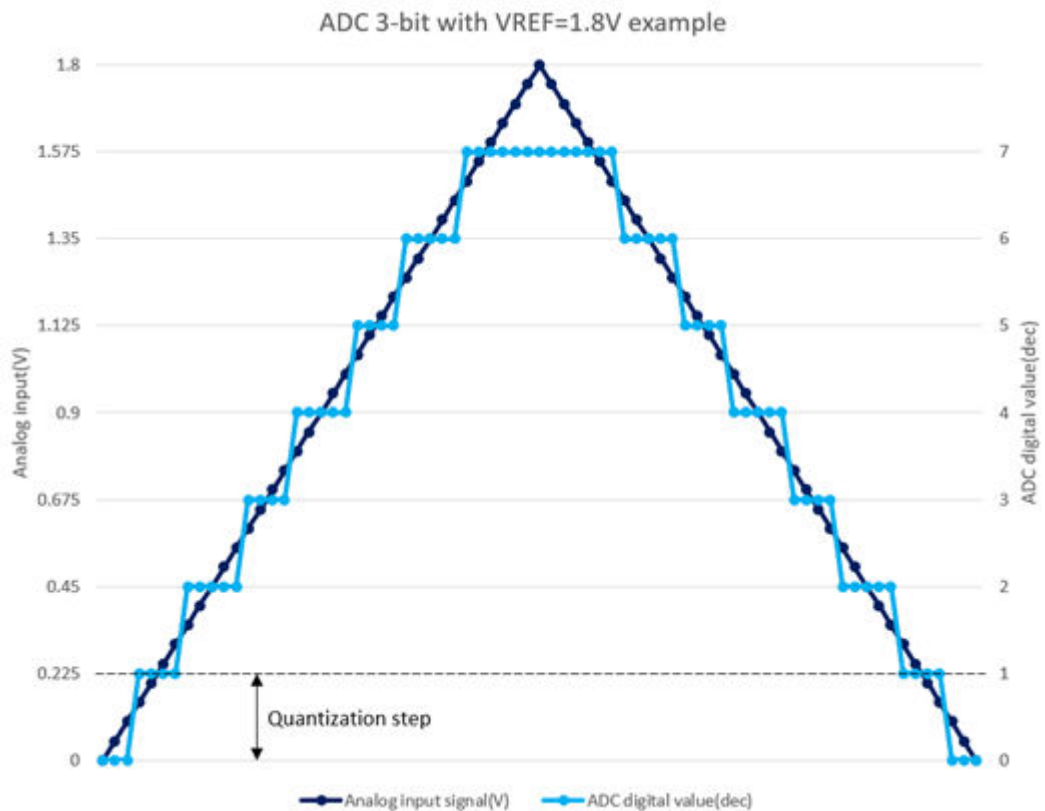
4.1 VREFBUF used as ADC reference for analog signal acquisition

Converting an analog signal to digital values with the ADC requires an accurate analog reference voltage to define the quantization step amplitude: it is a key parameter of the ADC. When the input signal voltage variation exceeds the quantization step amplitude, the less significant bit of the digital value is incremented/decremented.

The quantization step formula is $VREF/2^n$ where n is the number of bits of the ADC. For example, an ADC with 1.8 V reference voltage and 16-bit resolution: quantization step = $1.8\text{ V}/2^{16} = 27.466\text{ }\mu\text{V}$.

The following figure shows this behavior for a 3-bit ADC, $VREF = 1.8\text{ V}$ and a quantization step = 225 mV. When the input increases over a multiple of the quantization step, the digital value is increased and when the input voltage decreases over a multiple of the quantization step, the digital value is decreased.

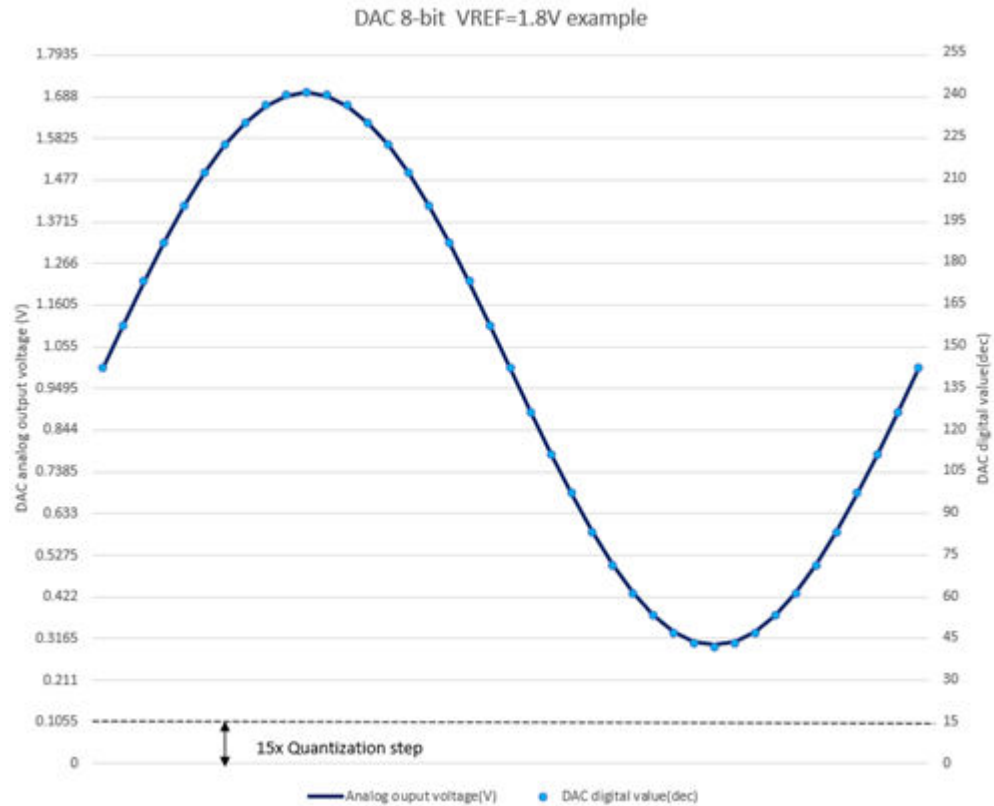
Figure 3. ADC 3-bit quantization step example



For this application case the ADC reference (VREF+ pin) is internally connected to the VREFBUF output and no external connection between pins is required. Only external capacitors are required on VREF+ pin.

4.2 VREFBUF used as DAC reference for signal generation application

The DAC peripheral is used to generate analog signals from digital values. As the ADC principle, a quantization step amplitude voltage ($VREF/2^n = 1.8\text{ V}/2^8 = 7.03\text{ mV}$ for 8-bit DAC) is required to convert a digital value to an output signal in the analog domain. The quantization step amplitude is computed from the DAC reference voltage and the DAC bit resolution.

Figure 4. DAC 8-bit quantization step example


For this application case the DAC reference (VREF+ pin) is internally connected to the VREFBUF output and no external connection between pins is required.

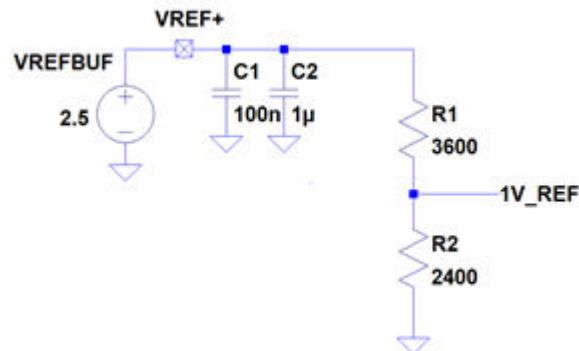
4.3 VREFBUF used as voltage reference with a voltage divider

There are many other applications where the VREFBUF could be used thanks to its driving current capability (few mA). Other reference voltage values could be obtained using a voltage bridge divider connected to the VREF+ pin.

The following schematic shows how to build a 1 V reference voltage from VREFBUF/VREF+ pin.

A simple voltage divider circuitry with two resistors is used to obtain the desired 1 V reference voltage.

$$1 V_{VREF} = 2.5 V_{VREFBUF} \times \frac{R2}{R1 + R2} = 2.5 \times \frac{2400}{3600 + 2400} = 2.5 \times \frac{2400}{6000} = 1 V$$

Figure 5. 1 V reference voltage from VREFBUF divided


The resistor bridge divider is loading the VREFBUF output and the maximum VREFBUF load capability should be respected. With this example, the static current load is $0.415 \text{ mA} = 2.5 \text{ V} / (3600 + 2400)$. In STM32G4 series datasheet, the maximum static load is 6 mA which is higher than the application load: the external circuitry choice is correct.

4.4 VREFBUF used as voltage reference with thermal sensor

Another VREFBUF application usage is relative to the thermal sensors found, for example, in batteries, computer motherboards, or heating/cooling systems. This temperature sensor circuit could simply consist of a voltage divider between a resistor and a negative-temperature-coefficient thermistor (NTC). When the temperature is increasing, the NTC thermistor impedance is decreasing.

Figure 6. Example of a generic NTC thermistor impedance versus temperature

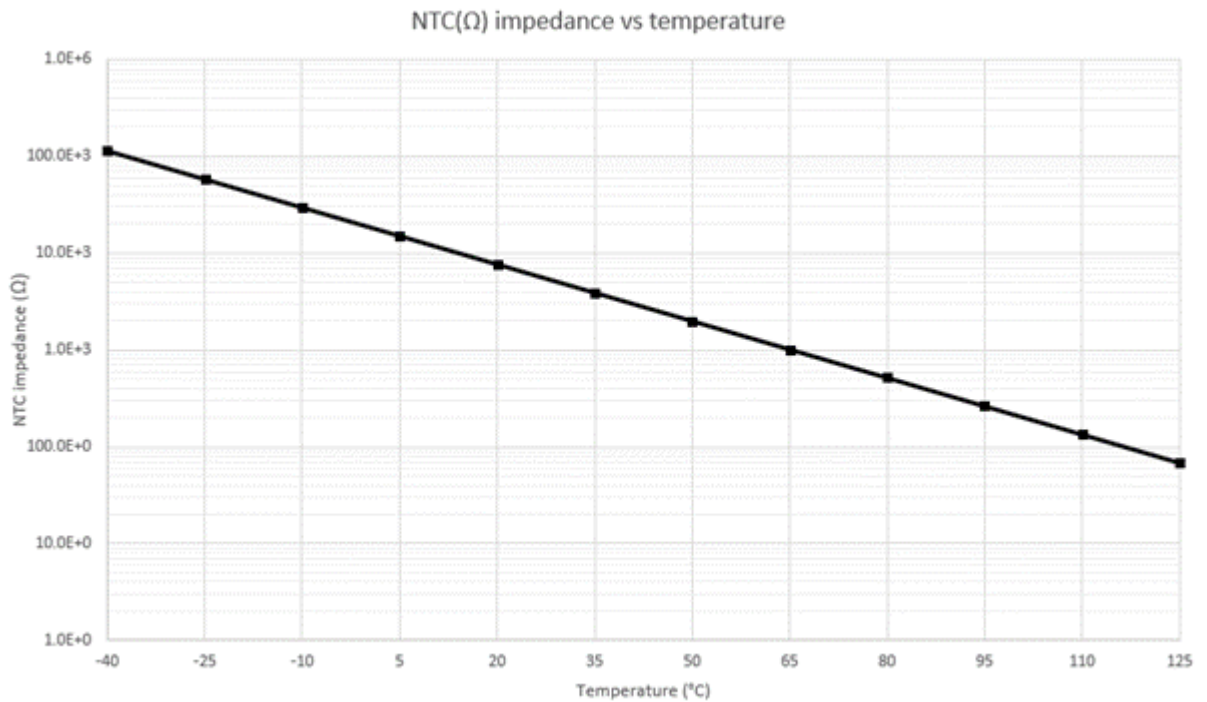
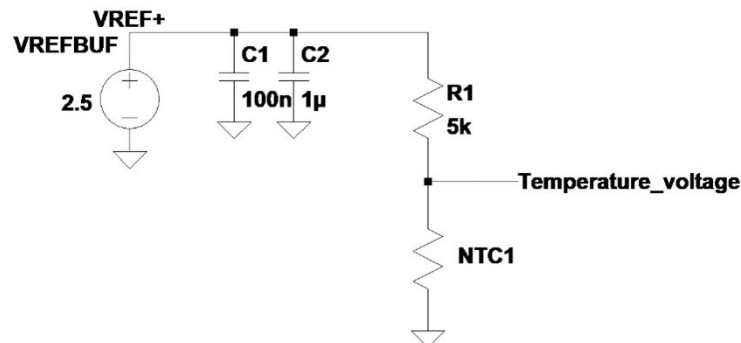


Figure 7. NTC thermistor voltage divider with VREFBUF peripheral



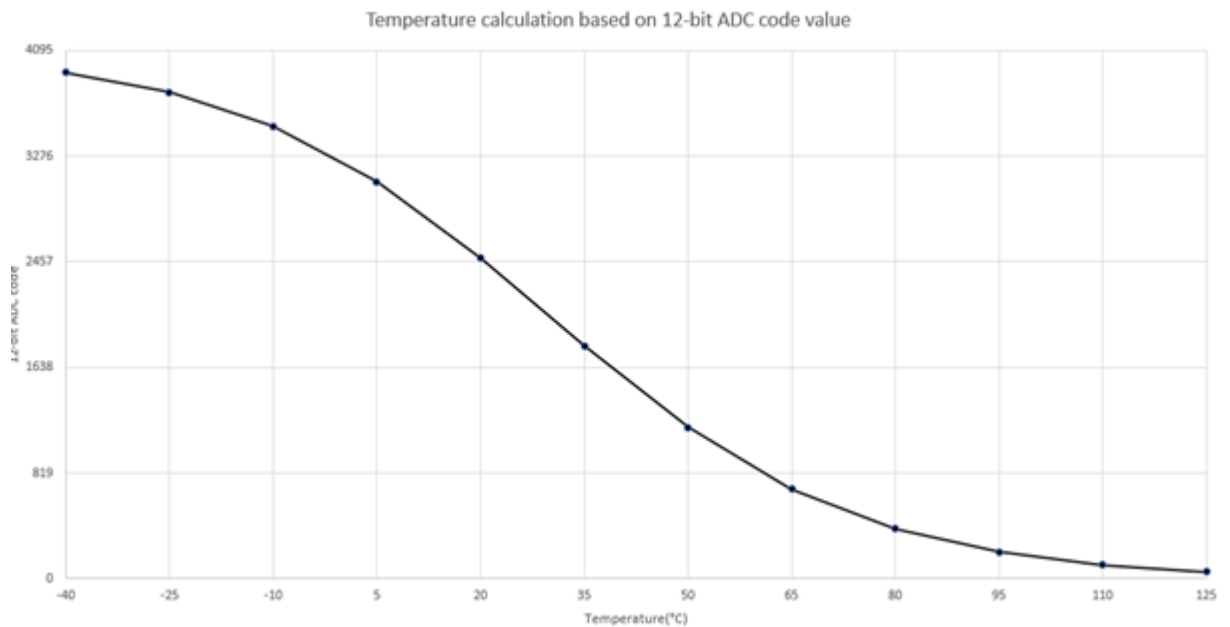
If one connects the Temperature_voltage signal to a STM32 12-bit ADC input, the following table represents the digitalized temperature characteristic values (ADC VREF is VREFBUF = 2.5 V).

Table 9. Temperature / STM32 12-bit ADC code summary

T°C	NTC1(Ω)	R1(Ω)	Temperature voltage (mV)	STM32 12-bit ADC code
-40	114943.3	5000	2395.784	3925
-25	58524.1	5000	2303.224	3773
-10	29797.9	5000	2140.783	3507
5	15171.8	5000	1880.323	3080
20	7724.8	5000	1517.666	2486
35	3933.1	5000	1100.71	1803
50	2002.6	5000	714.9487	1171
65	1019.6	5000	423.4501	693
80	519.2	5000	235.179	385
95	264.3	5000	125.5153	205
110	134.6	5000	65.53578	107
125	68.5	5000	33.78712	55

One can estimate the actual temperature value from the ADC code with the help of a polynomial calculation.

$$T^{\circ}\text{C} = C0 + C1 \times \text{ADC}_{\text{code}} + C2 \times \text{ADC}_{\text{code}}^2 + C3 \times \text{ADC}_{\text{code}}^3 + \dots$$

Figure 8. Table results and estimation curve from ADC code with a polynomial interpolation


The previous interpolation curve is obtained with the following coefficients:

Table 10. Polynomial coefficients of the interpolation function

C0	C1	C2	C3	C4	C5
3277.1	-32.104	-0.3492	0.0024	4e-5	-2e-7

With these coefficients, the accuracy of the estimation function is $\pm 4^{\circ}\text{C}$ with respect to the actual temperature.

This temperature sensor application accuracy is relative to the VREFBUF peripheral stability over supply voltage, temperature, and silicon process variations. To answer those constraints the peripheral has a specific regulator voltage architecture with a trimming feature.

Revision history

Table 11. Document revision history

Date	Version	Changes
24-Sep-2021	1	Initial release.
09-Dec-2021	2	Updated Table 1. Applicable products. Updated Table 4. Example of VREFBUF output voltage per STM32 series.
13-Jul-2023	3	Updated document title. Updated Table 1. Applicable products. Updated Figure 1. STM32 VREBUF peripheral simplified schematic. Updated Table 3. VREFBUF peripheral behavior with ENVR/HIZ bits. Updated Table 4. Example of VREFBUF output voltage per STM32 series.

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