AN5702

Application note

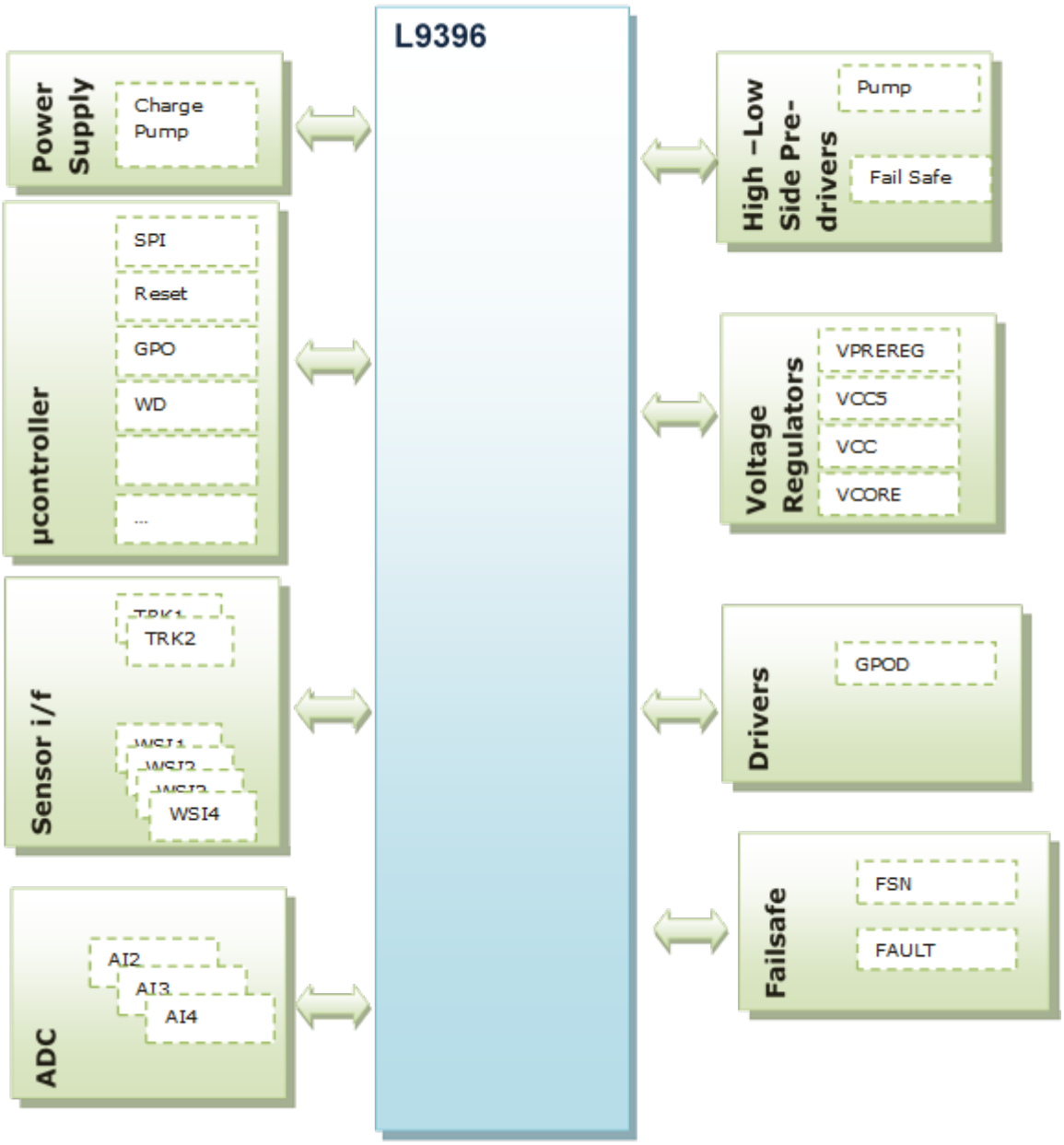
L9396 Configuration and layout

Introduction

This document describes how to configure the L9396 regulators for addressing different system scenarios.
The L9396-EVAL board is referenced.
Layout hints and recommendations for improving EMC performances will also be discussed.

1 Block diagram

Figure 1. **Application block diagram**

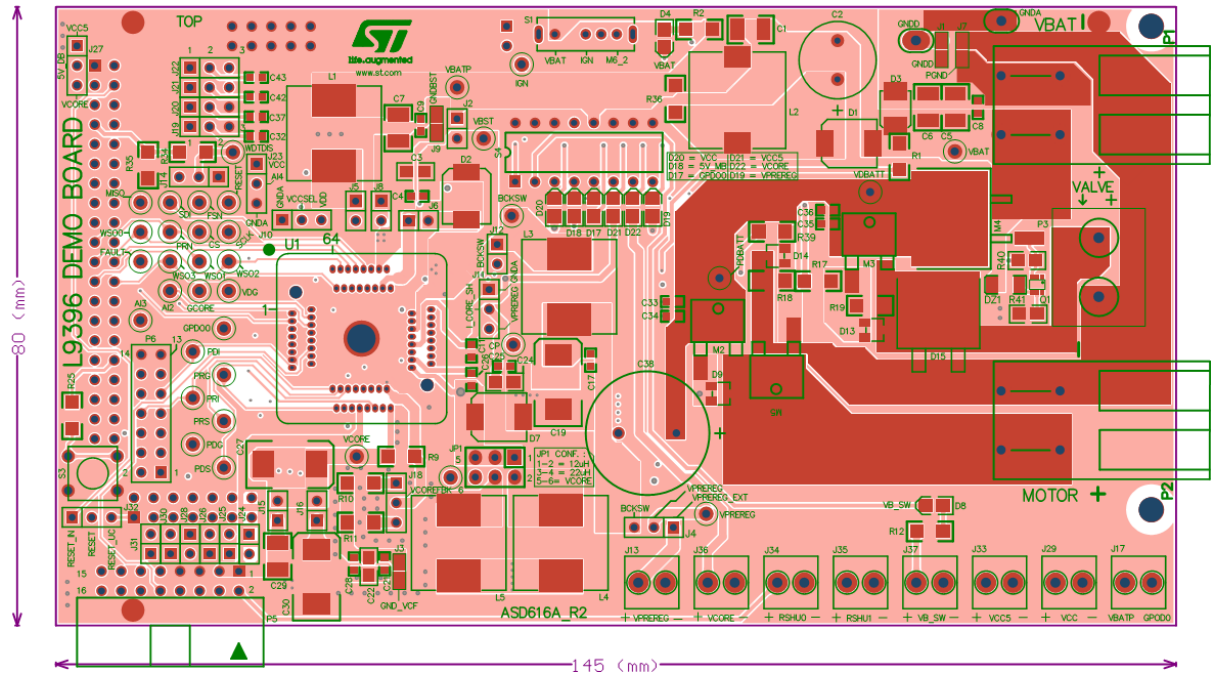


2 Device configuration

The L9396 device provides several configurable blocks in order to fit many application scenarios. The present paragraph is intended to help application engineer to properly setup the application when a particular scenario is needed.

As reference the L9396 demo board will be used.

Figure 2. Demo board



2.1 Input voltage regulator setup

2.1.1 BOOST

BOOST is used to guarantee operation at low battery (especially during cranking condition).

The block is capable of 300 mA @ VBST with VBATP = 4,5 V in order to avoid reset during the low battery event. The overall consumption from VBST should not exceed this value.

Figure 3. BOOST external circuit: schematic

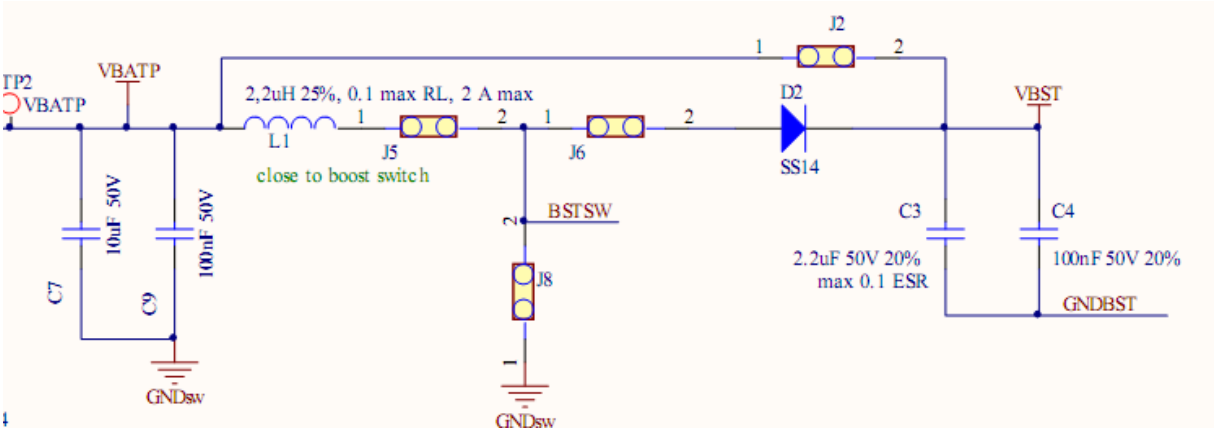
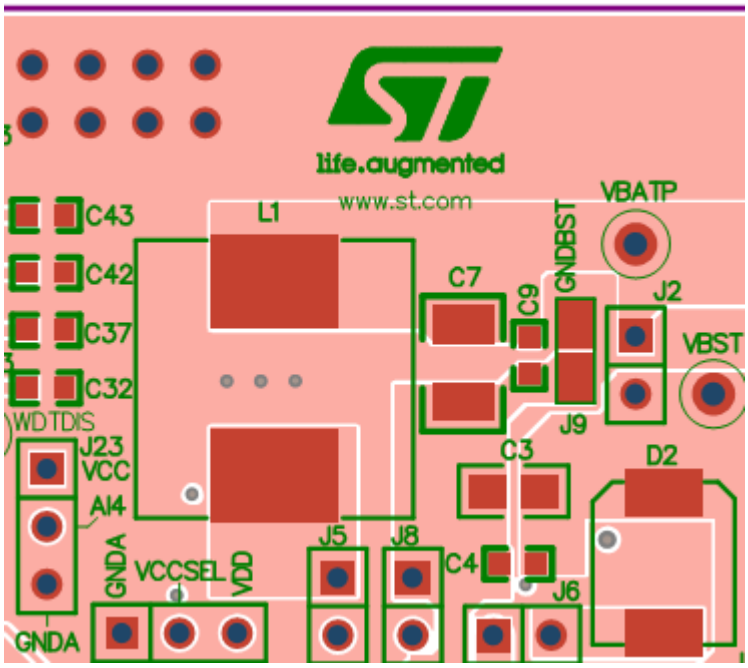


Figure 4. **BOOST external circuit: layout**



In case BOOST is needed components can be placed following the Table 1.
In case the BOOST is not needed, VBST could be simple shorted to VBATP and BSTSW must be tied to GND. Without BOOST the input battery can be still lowered until 6 V without getting RESET.

Table 1. **BOOST jumper configuration**

Name	Setup	Condition
J2	Open	VBST to be BOOSTED
	Close	VBST directly connected to VBST
J5	Open	Inductor not used
	Close	BOOST inductor connected
J6	Open	Diode not connected
	Close	BOOST diode used
J8	Open	BSTSW connected to external LD
	Close	BSTSW to GND to disable BOOST

2.2 Output voltage regulators setup

2.2.1 VPREREG

VPREREG is the regulated voltage used as supply for other regulators (WSS, tracking, VCC, VCC5, and VCORE).

In the Figure 5 and the Figure 6 the application circuit with reference to application board snapshot is shown.

Figure 5. VPREREG external circuit

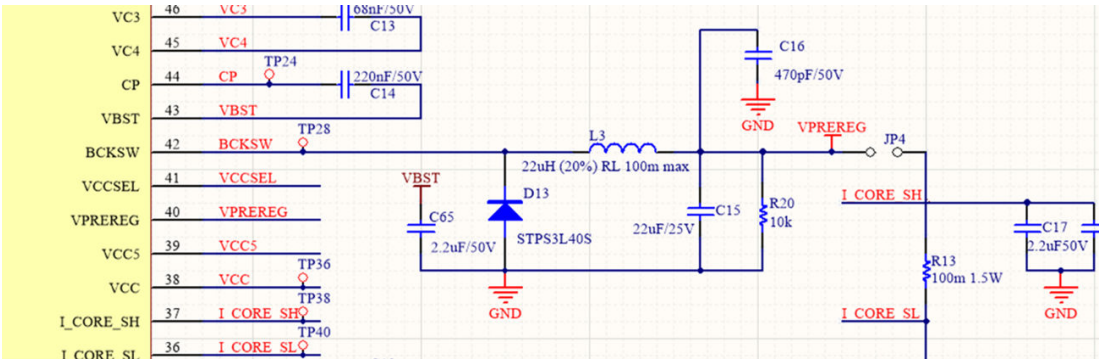
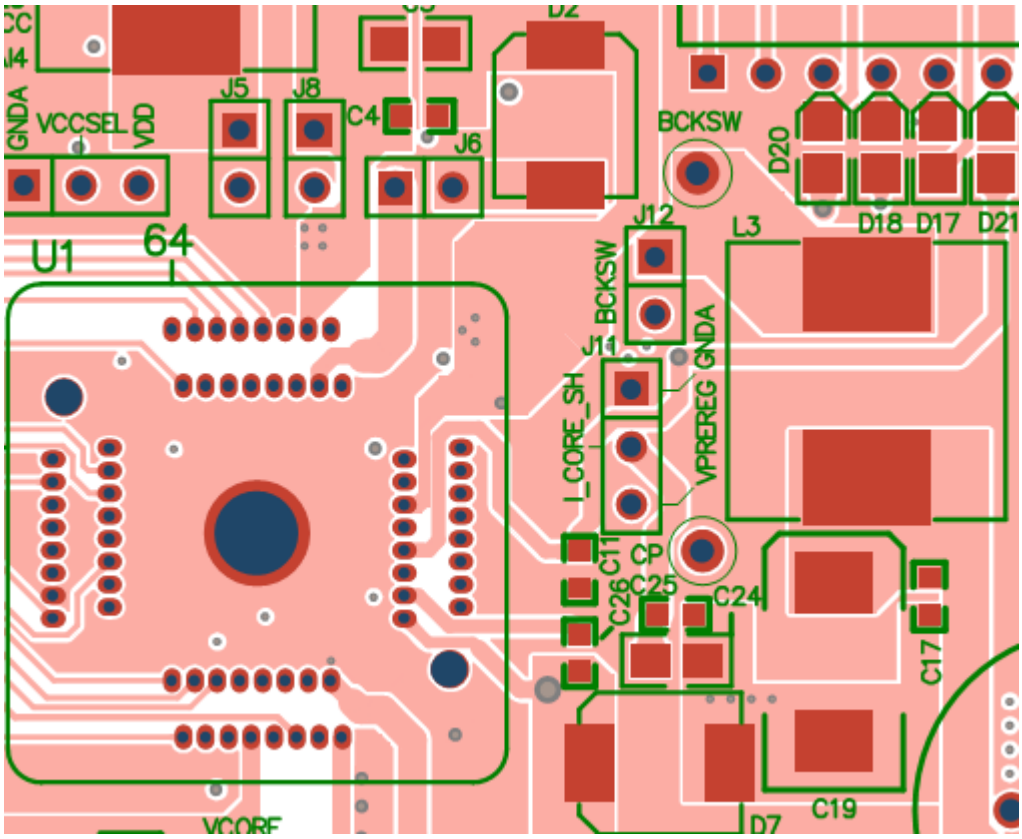


Figure 6. VPREREG configuration selection



The regulator default value is 6.5 V and is restored in reset condition.

If needed, the MCU can adjust the value to 7.2 V after RESET is released by setting via SPI the LSB in the register SYS_CONFIG_1.

VPREREG BUCK can be also completely disabled if not needed (see next dedicated section), but in this case also VCORE will be disabled.

The regulator was designed, qualified and validated to start the power-up sequence assuming that the VPREREG residual bias is close to 0 V. The effect of a residual voltage on VPREREG pin on the start-up sequence was not assessed during the device development.

To ensure that the VPREREG pin is close to 0 V, it is recommended to insert a pull-down resistor on the VPREREG pin (see R20, Figure 5).

The value suggested by ST for the pull-down resistor is 10k ohms, a value that comes from two considerations:

- The regulator can have two output values, 6.5 V or 7.2 V. With a 10k ohm pull-down resistor connected to the VPREREG node, there will be a current constantly flowing to ground equal to 650 µA (VPREREG = 6.5 V) or 720 µA (VPREREG = 7.2 V).
- The pull-down resistor (R20) is in parallel with the output capacitor of the regulator (C15, see Figure 5), causing a delay in the device's power-up.

To evaluate the power-on time of the regulator, it is necessary to calculate the time constant of the parallel R20// C15. C16 is in parallel with C15, but since its value is much smaller than C15, it can be ignored. The time constant considering R20 = 10 kΩ with the capacitor C15 = 22 µF is (R20 x C15) 0.22s.

Each customer can size the resistance value in according to their needs.

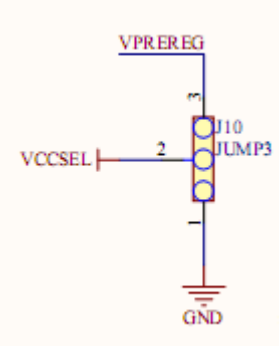
2.2.2 VCC

VCC is linear regulator with selectable output voltage between 3.3 V and 5 V and 2% tolerance.

At device power up VCCSEL is latched and if VCCSEL is less than 0.75 V then VCC works as a liner 3.3 V voltage regulator; while if VCCSEL is grater than 1.75 V then VCC has 5 V output.

In case 5 V is needed it is recommended to connect VCCSEL to VPREREG.

Figure 7. VCC external circuit and configuration selection



Note: VCC is also used internally as the reference voltage for microcontroller IO pin.

2.2.3 VCORE

VCORE is a voltage regulator that can work as linear, if SCORE is directly connected to VCORE, or buck, when external inductor is present. VCOREFDBK voltage level is regulated to 0.8 V ± 2% (or ± 3% in case of buck configuration); as shown in the Figure 9 and the Figure 10 on the Application Board, the external feedback network values are chosen to generate a VCORE = 1.2 V or VCORE = 5 V depending on J18 jumper configuration.

CASE #1

$$VCORE = \frac{R_9 + R_{11}}{R_{11}} \times \text{VCOREFDBK} \cong 5V \quad (1)$$

CASE #2

$$VCORE = \frac{R_9 + R_{10}}{R_{10}} \times \text{VCOREFDBK} \cong 1.2V \quad (2)$$

Figure 8. VCORE external circuit in linear and buck mode

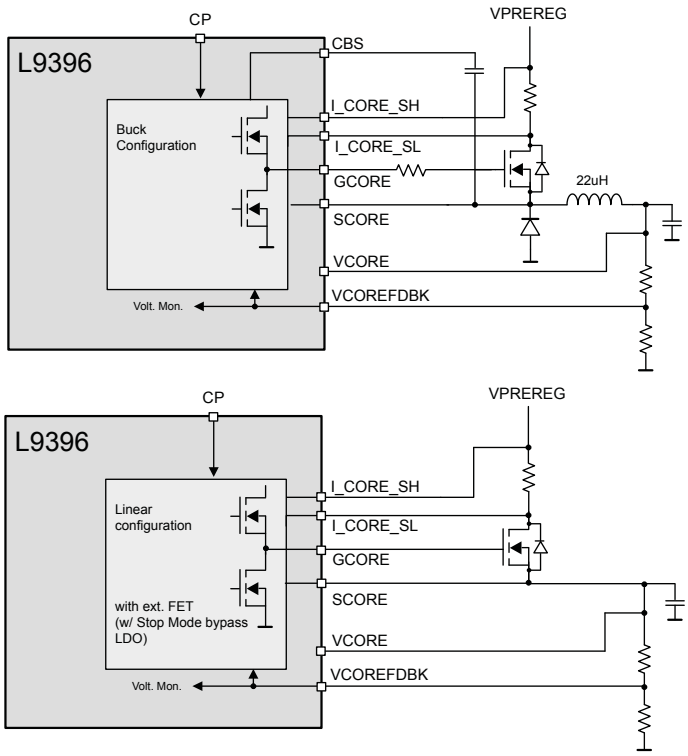


Figure 9. VCORE external circuit

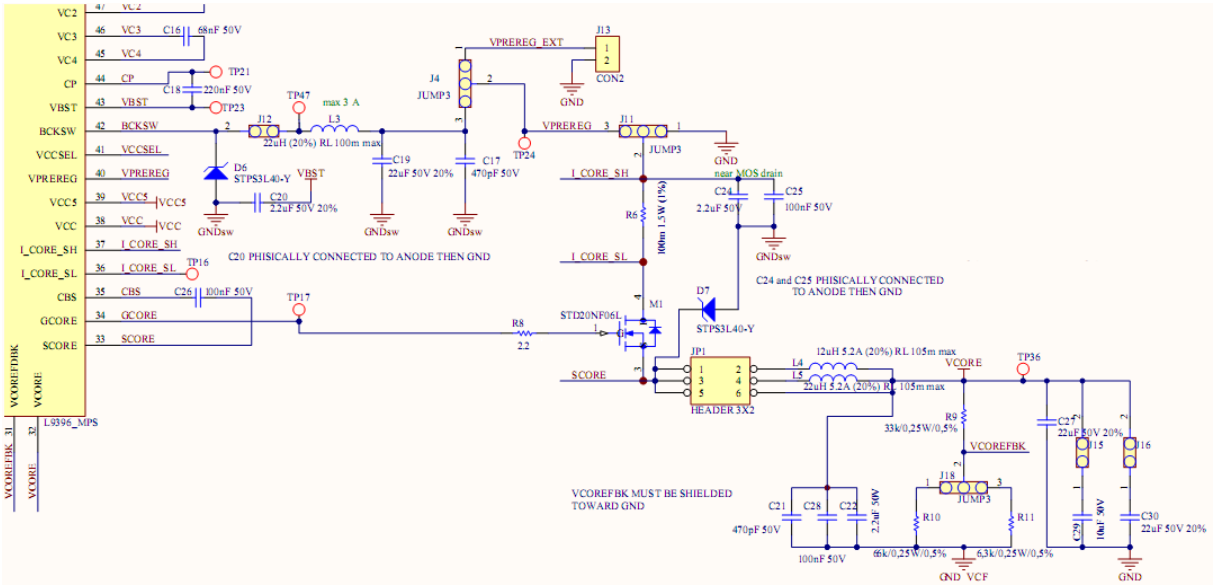


Figure 10. **VCORE configuration selection**

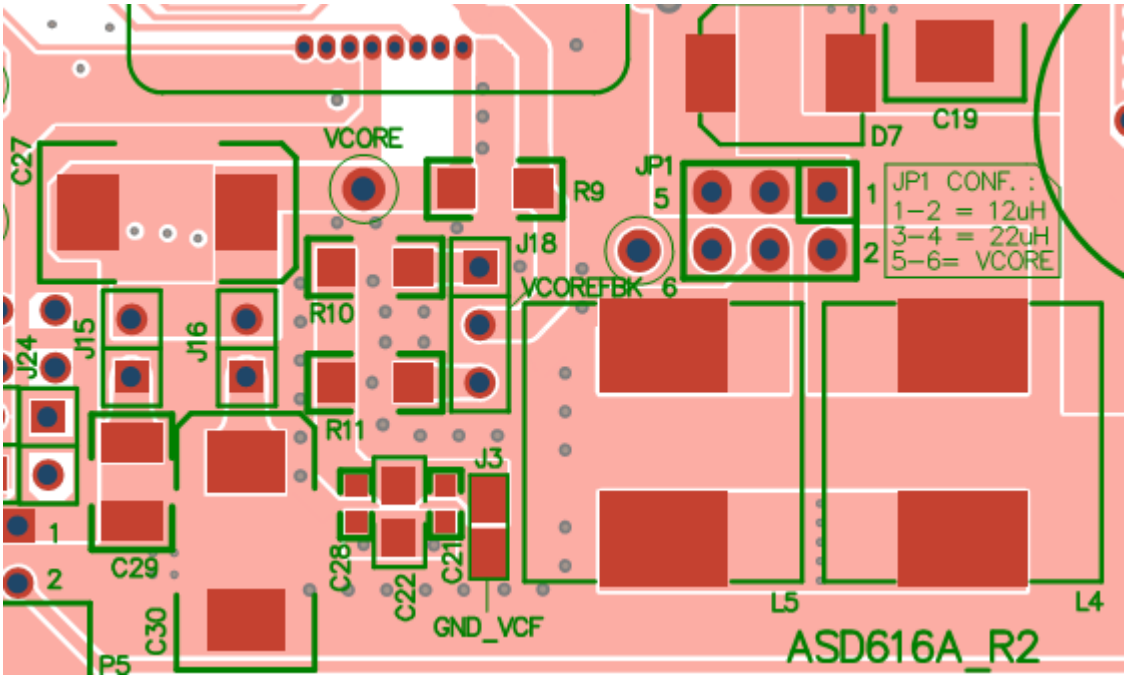


Table 2. **VCORE configuration based on jumpers**

Name	Setup	Condition	Note
J4	P1 to P2	VPREREG connected to ext. source	-
	P2 to P3	VPREREG connected to buck	
J11	P1 to P2	I_CORE_SH to GND	See buck regs disabled paragraph
	P2 to P3	VCORE buck connected to VPREREG	-
J15	Open	No C load	-
	Close	Additional 10 µF load on VCORE	To be used in linear mode
J16	Open	No C load	To be used in buck mode when VCORE = 1.2 V
	Close	Additional 22 µF load on VCORE	
JP1	P5 to P6 closed Others open	No Inductor	To be used in linear regulator mode
	P1 to P2 closed Others open	Inductor = 12 µH	To be used when buck regulator configured and VCORE = 1.2 V
	P3 to P4 closed Others open	Inductor = 22 µH	To be used when buck regulator configured and VCORE = 5 V
	P1 to P2 close P3 to P4 close P5 to P6 open	Inductor ≈ 8 µH	Not used
J18	P1 to P2	VCORE = 1.2 V	-
	P2 to P3	VCORE = 5 V	

Once the VCORE voltage is selected, the AI0 an AI1 inputs need to be configured according to the Table 3.

Table 3. VCORE voltage configuration selection

N	VCORE voltage	Pin setup(1)	
-	Nominal Value	AI0	AI1
1	3.3 V	Low	Low
2	5 V	Low	High
3	0.8 V to 5 V	High	Low

1. *Connection to VPREREG is recommended when a "High" is present inside this table.*

A minimum load of 10 mA should be placed when VCORE is used in BUCK mode and 70 mA in linear mode.

Besides if VCORE is configured as BUCK with output voltage at 3.3 V or 5 V, and a fast switch off / switch ON is applied for example through IGN, the automatic detection of BUCK circuit could not work when VCORE and SCORE pins have not time to discharge; if this happens, then VCORE MODE is latched as LINEAR and not as BUCK. The corresponding bit in the CONTROL_SUPPLY_1 is updated accordingly.

In case the application could face such case, it is recommended to apply a minimum load so that VCORE drops under 2.6 V before a new power up is present

$$Iload_{MIN} = \frac{C_{VCORE}(VCORE - 2.6)}{\Delta t_{MIN}} \quad (3)$$

Where Δt_{MIN} is the minimum time so that a new power up is needed. Besides MCU must always check the CONTROL_SUPPLY_1 bit in order to check the correctness of configured regulators and take proper actions (safe state) in case of issue.

There is also the possibility to completely disable VCORE regulator as shown in the following paragraph.

2.2.4 Unused regulators and VCORE configuration mode

In order to provide flexibility for the power management, the IC provides several voltage regulators.

In some applications, VPREREG and/or VCORE are not needed. In order to save money by reducing BOM, L9396 allow a useful mode in which no external component need to be connected to BUCK regulators.

The available setups are shown in the Table 4.

At device power up, regulator configuration is detected through pins state and applied; it is also latched inside IC in the registers SUPPLY_CONTROL_2, bit 16 VCORE_MONITOR TYPE and SUPPLY_CONTROL_2, bit 17 (VCORE OFF LATCHED) and bit 18 (BUCK OFF LATCHED).

Table 4. Unused regulator configuration

N	Regulators Configuration			Pin setup(1)		
-	VPREREG state	VCORE state	VCORE monitor	AI0	AI1	I_CORE_SH
1	Enabled	Enabled	VCORE_UV_L, VCORE_OV_L	Low	Low	High
2	Enabled	Enabled	VCORE_UV_H, VCORE_OV_H	Low	High	High
3	Enabled	Enabled	VCOREFDBK_UV, VCOREFDBK_OV	High	Low	High
4	Enabled	Disabled	NA	High	High	High
5	Disabled	Disabled	NA	Don't care	Don't care	Low

1. *Connection to VPREREG is recommended when a "High" is present inside this table.*

For example, if only VCORE needs to be disabled and BUCK VPREREG must be active, the following configuration can be used:

Table 5. VCORE unused configuration

Pin Name	Condition
AI0, AI1	Connected to high voltage
I_CORE_SH, I_CORE_SL	Connected to high voltage
GCORE, SCORE, CBS, VCORE	OPEN
VCOREFDBK	OPEN

When both VPREREG are not needed in the application, in order to have the minimum BOM cost, the following conditions described below should be used:

Table 6. VPREREG/VCORE unused configuration

Pin Name	Condition
BCKSW	OPEN
VPREREG	Connected to VBST
I_CORE_SH, I_CORE_SL	Connected to GND
GCORE, SCORE, CBS, VCORE	OPEN
VCOREFDBK	OPEN

2.3 Other configurations setup

2.3.1 Device pin configuration

The L9396 offers functional configurability for the following device pin:

- FAULT pin is a useful output which can be set as lamp driver or as interrupt (active high) through SPI
- GPOD0 is a LS driver which can be used for different purpose
- FSN pin is a very smart configurable output for failsafe usage

Device can be configured by writing the specific SPI registers associated with those outputs. After setting the relative bits, application may lock the writing of SAFE registers by WRITE_PROTECTION register writing.

Example 1 :

Suppose we need the following configurations: FAULT as lamp driver, GPOD0 as an ON/OFF driver.

After MCU startup and reset release, the following SPI registers should be written:

- ADV_CONFIG , bit 12 = 1
- SYS_CONFIG2, bit 11 = 1 , bit 13:12 = ”10”
- DRV_CONTROL, bit 18 = 1 (accepted only with WD Q&A served)

Note: WD PRN should be configured as described in the dedicated section in order to correctly execute the sequence.

2.3.2 Tracking regulator/WSS interface configuration

Tracking regulator or WSS interface can be selected by properly setting jumpers as shown in the Table 7 and the Table 8.

Tracking regulator configuration is possible only on RSU0/RSU1 as described in the following figure.

Figure 11. WSS/Track regulators schematic for channel 0

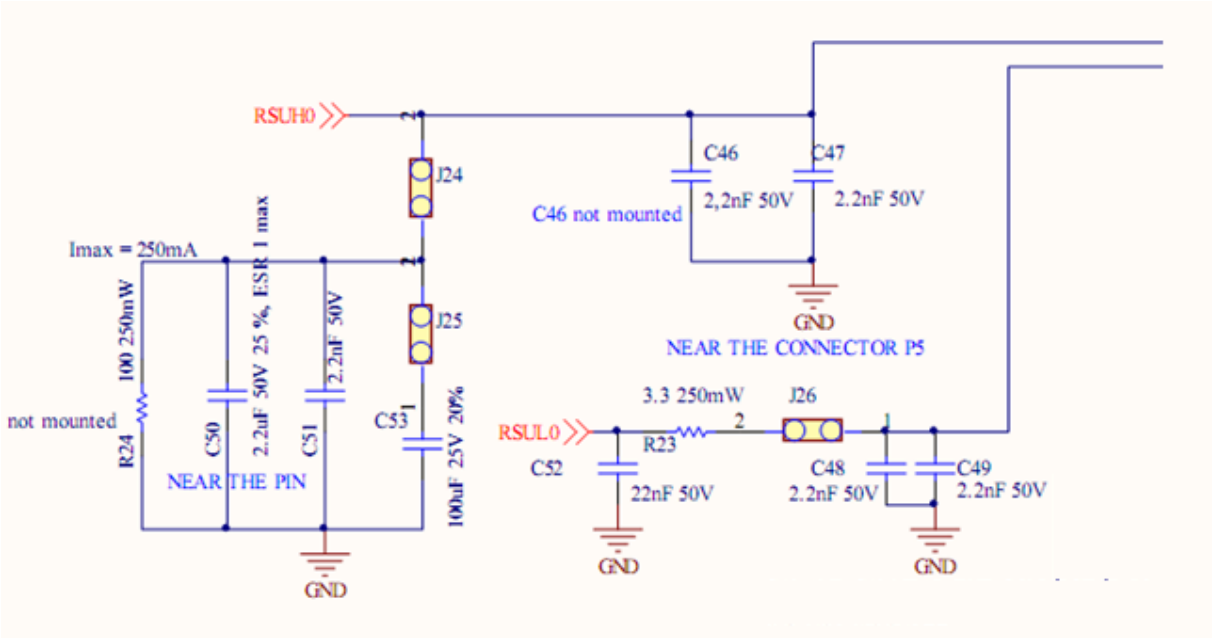


Figure 12. **WSS/Track regulators schematic for channel 1**

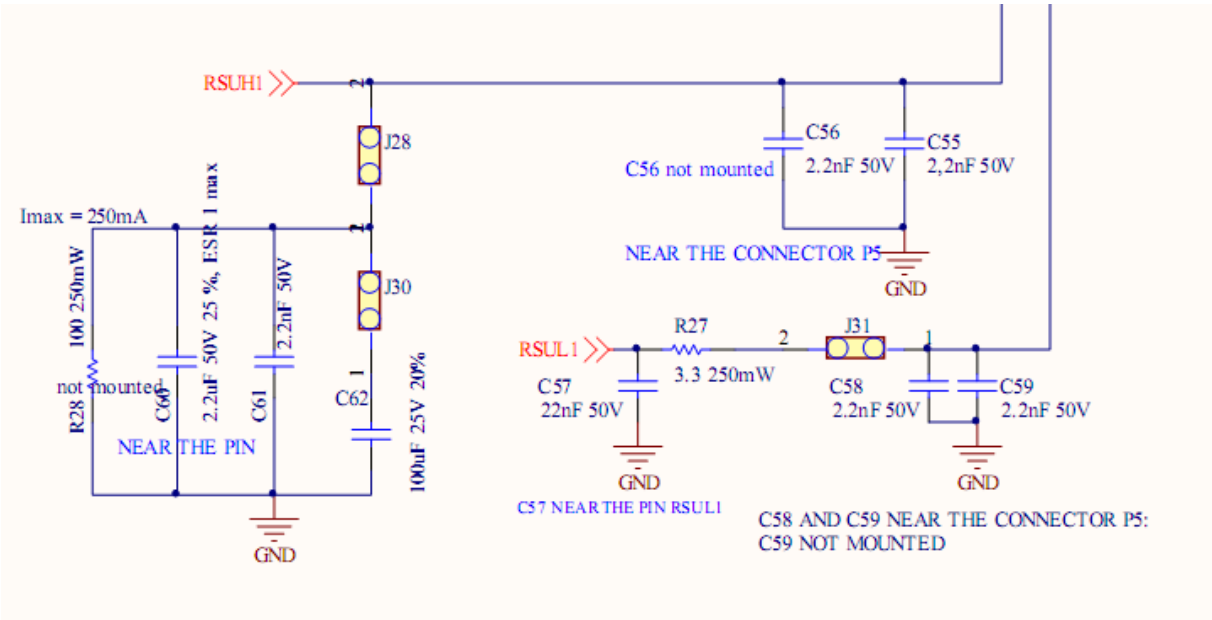


Table 7. **Tracking regulator channel 0 configuration based on jumpers**

Name	Setup	Condition	Note
J24	Open	No RC external Network on RSUH0 pin	External Network on RSUHx pin to be used when device is set as Tracking regulator. In this case RSULx is left unconnected.
	Close	RC external Network on RSUH0 pin	
J25	Open	No Additional load on RSUH0 pin	
	Close	Additional C load on RSUH0 pin	
J26	Open	RSUL0 not connected	
	Close	RSUL0 connected to WSS	

Table 8. **Tracking regulator channel 1 configuration based on jumpers**

Name	Setup	Condition	Note
J28	Open	No RC external Network on RSUH1 pin	External Network on RSUHx pin to be used when device is set as Tracking regulator. In this case RSULx is left unconnected.
	Close	RC external Network on RSUH1 pin	
J30	Open	No Additional load on RSUH1 pin	
	Close	Additional load on RSUH1 pin	
J31	Open	RSUL1 not connected	
	Close	RSUL1 connected to WSS	

If tracking regulators are needed, after RESET is released MCU should write SPI register CONFIGURATION 1 in order to enable the tracking regulators. In the same register it must also be written the reference tracking voltage between VCC/VCC5.

2.3.3 WD configuration

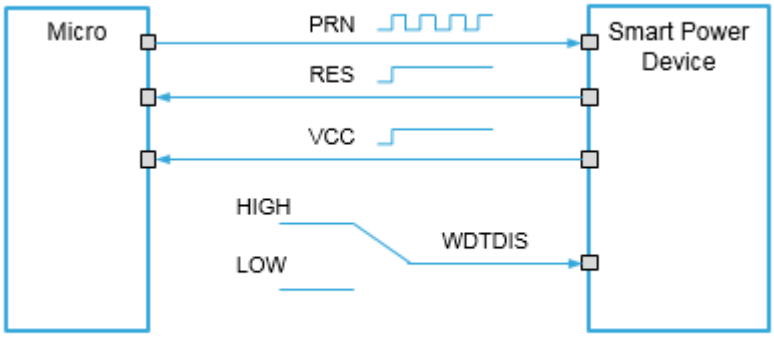
The L9396 have 2 configurable watchdogs in order to adapt to several safety levels:

- WD Q & A based on SPI
- WD PRN controlled by pin

The first watchdog is always needed in order to control drivers (pump motor, GPOD, FS driver, VBAT switch) while the second one can be disabled by setting WDTDIS to a voltage greater than 1.75 V.

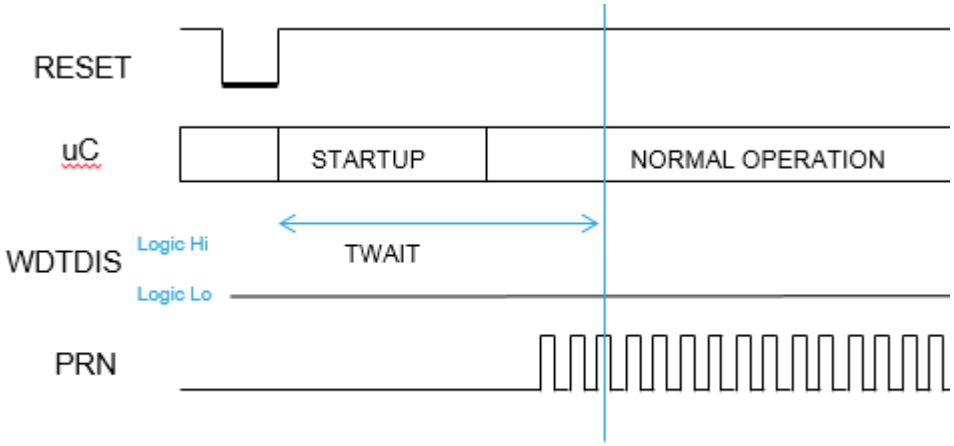
After power up the device need WD2 (if enabled) but not WD1; WD1 monitoring is activated after the first access to WD_SEED_ANSW register and from this point the device check for WD protocol.

Figure 13. WD2 connection diagram



The device gives the possibility to adjust the WD2 PRN frequencies according the application need. In case the desired values are different from the default ones, the MCU should adjust the ADV_CONFIG register (bit WD2_T_OFF and bit WD2_MAX_FREQ) before the TWAIT time (see the Figure 14).

Figure 14. WD2 timing diagram



2.3.4 ADC configuration

The L9396 integrates a 10 bit analog to digital converter which can be used to monitor both internal and external voltages and also device temperature.

The ADC operate outside reset and can be configured through ADC CONFIG register in order to average the input voltage before storing the value on device registers.

The setting of this feature to 8/16 samples is strongly recommended above all when BOOST regulator is used.

2.3.5 GPO

The GPO output is an integrated LS with different possible configurations depending on programmed values in GPO_DRIVER_CONFIG[1:0] bits in SYS_CONFIG_2 register.

The GPO COMMAND bit of DRV_CONTROL 1 register is used in ON/OFF mode, while for other configurations (eg. in PWM mode) is ignored because the driver command is generated automatically by a PWM generator.

The GPO DRIVER ENABLE bit of SYS_CONFIG2 works for all the configurations.

2.3.6 Unused configuration for RSUx, PUMP

In case RSU are not used the following settings need to be applied:

- RSUHx = OPEN
- RSULx = OPEN
- WSOx = OPEN

When PUMP is not needed the following setup is advised:

- PRI = PDI = GND
- PDG = PRG = OPEN
- PDS = PRS = GND
- PDBATT = OPEN

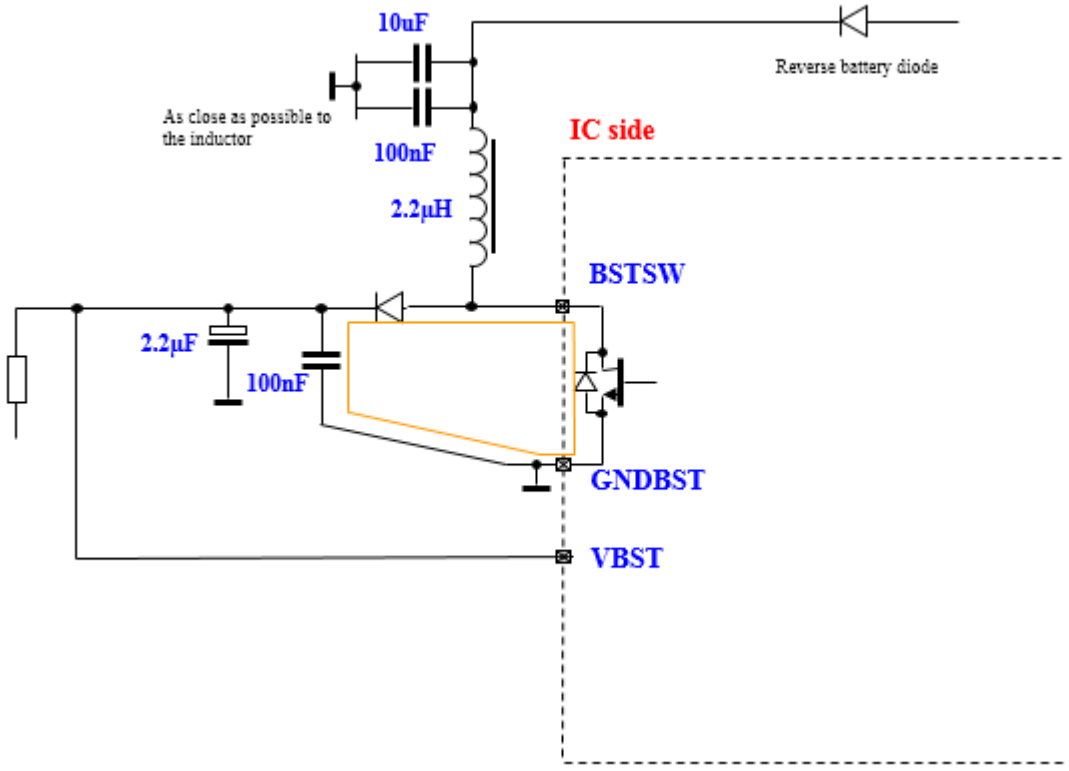
3 Note and suggestions on layout

3.1 PCB layout guideline

3.1.1 BOOST regulator

The BOOST regulator has a 2 MHz operating frequency and allow the usage of a 2.2 µH inductor. In order to improve EMC performances, the external components should be placed to make the area of the loop highlighted in orange as small as possible.

Figure 15. BOOST regulator layout indication

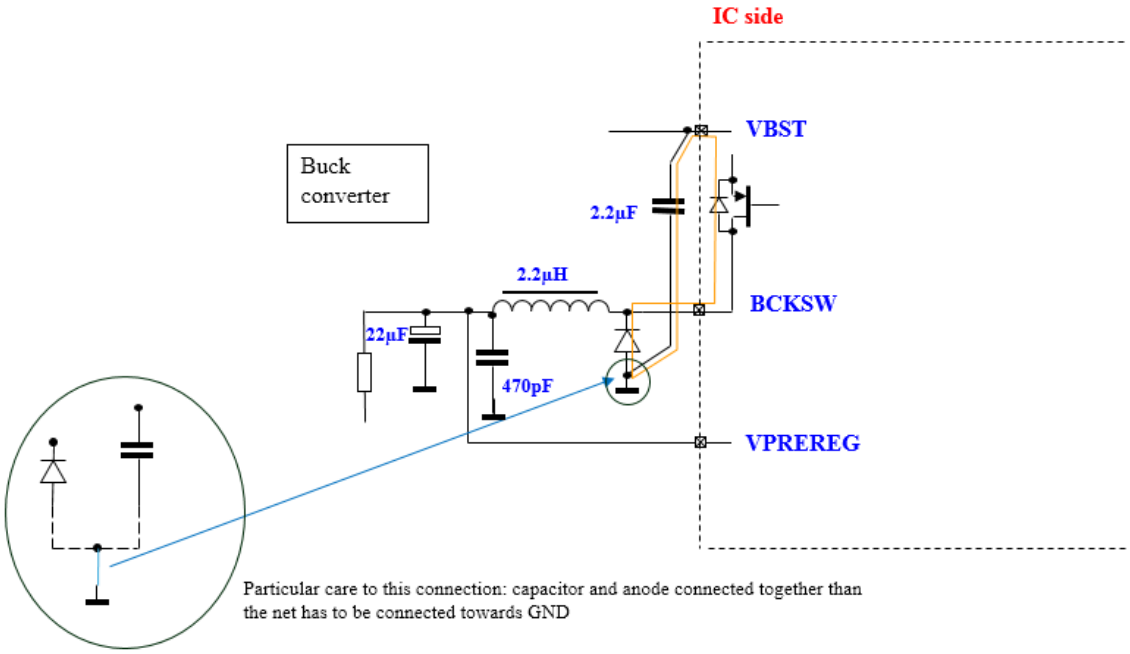


3.1.2 BUCK pre-regulator

Particular care should be put on the routing of the connection between the anode of the recirculation diode, the terminal of the noise bypass capacitor and the ground.

The connection should be realized not through independent paths but following the rule showed in the Figure 16.

Figure 16. VPREREG buck regulator layout suggestions



3.1.3 VCORE voltage regulator

In order to have high flexibility, VCORE has been implemented with an architecture compatible with both linear and buck configuration where the regulated voltage can be fully configurable through R1 and R2, external feedback resistors, in (0.8-5 V) range; the following guidelines refers to buck configuration which is the most critical from layout point of view; layout for linear case can be extrapolated as well.

In order to guarantee the performances reported in the datasheet for these regulators, particular attention should be done on managing external components placement and path routing.

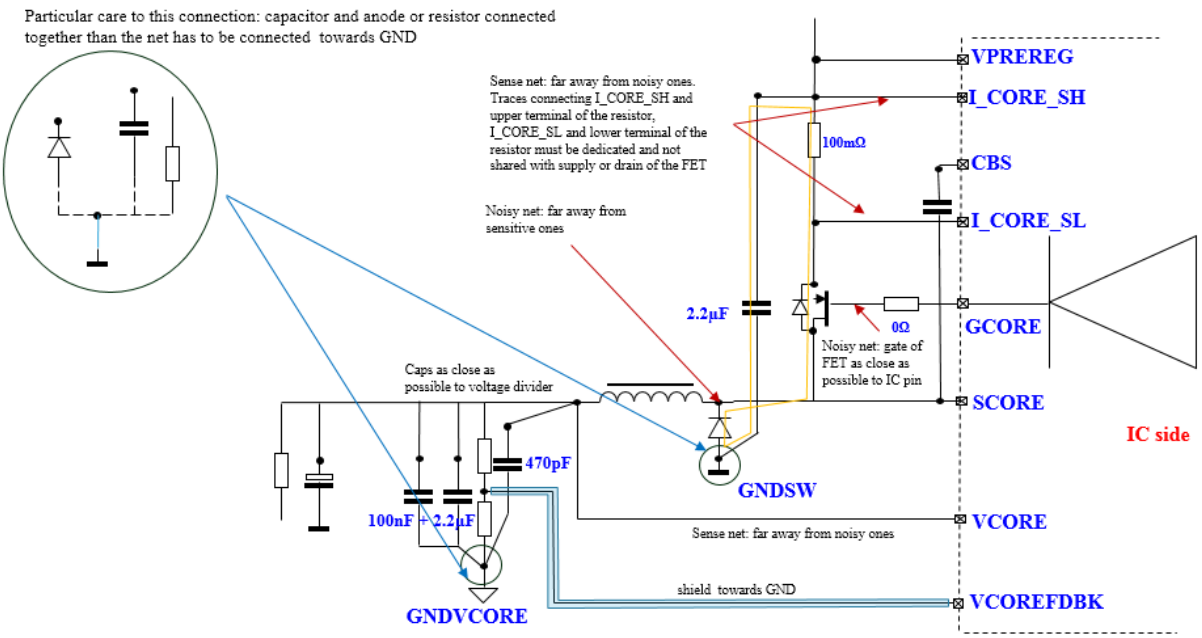
Particular care should be put on the routing of the connection between the anode of the recirculation diode, the terminal of the noise bypass capacitor and the ground. The connection should be realized not through independent paths but following the rule showed in the Figure 17.

In order to improve EMC performances, the external components should be placed to make the area of the loop highlighted in orange as small as possible.

In order to minimize parasitic effect of the path which connects GCORE to the gate terminal of the external FET, the FET should be placed as near as possible to IC pins.

Being the value of the regulated voltage depending on the voltage on VCOREFDBK, any accidental coupling effect on this net strongly affects the behavior of the regulator output. For this reason, ST recommends a dedicated ground connection for the external voltage divider, and to shield towards GND the path which connects the VCOREFDBK to the middle point of the voltage divider. For further improvements, a capacitor in parallel to the voltage divider can be mounted: the connection towards ground should be realized not through independent paths but following the rule showed below.

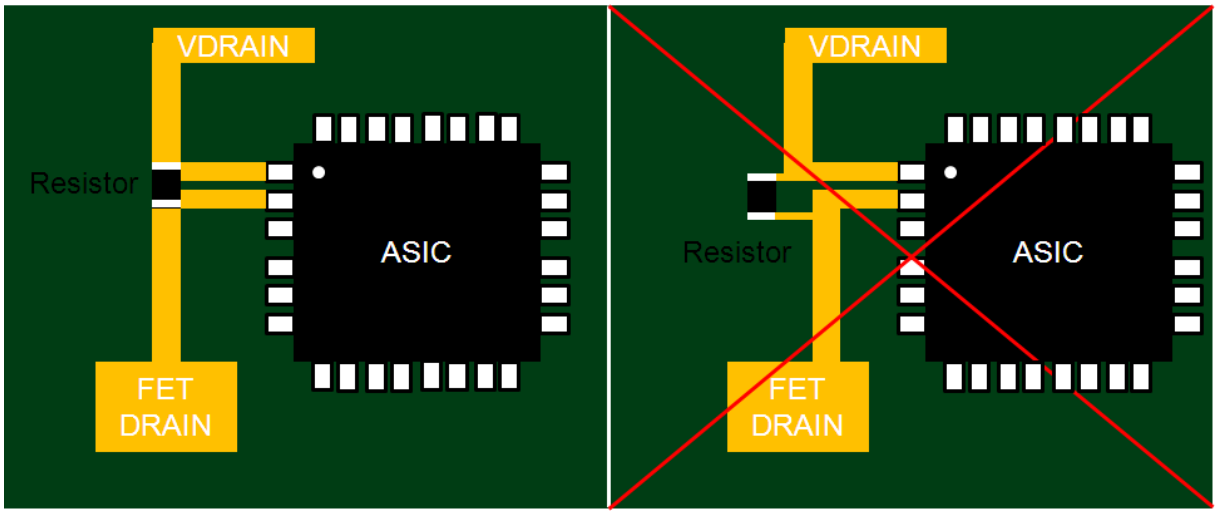
Figure 17. **VCORE buck regulator layout suggestions**



In order to achieve good performance in terms of precision, some rules should be followed for the placement and routing of the 100mohm resistor between I_CORE_SH and I_CORE_SL: these are sense nets and must be far away from noisy ones. Besides, traces connecting I_CORE_SH and upper terminal of the resistor, I_CORE_SL and lower terminal of the resistor must be dedicated and not shared with regulator supply (VDRAIN) and drain of the external FET.

For sake of clarification, an example is reported in the Figure 18: on the left side the connection is realized as per ST recommendation while in the right side isn't.

Figure 18. **VCORE buck regulator layout suggestions for external sense resistor**



3.1.4 Battery operating ranges

As specified in DS, L9396 is capable of operate up to 19 V of VB; however the device has been analyzed in order to understand the behavior during load dump and jump start pulses with the following result:

- For 18 V < VS < 28 V, device in jump start condition, all functions are guaranteed, parameter “ton/toff high side” degradated to 80 ns;
- For 28 V < VS < 35 V, device in load dump condition w/o application fault violating device AMR, functions are guaranteed and no damage.

3.1.5 STM8 microcontroller connector cross reference

The L9396 Demo Board provides the connection to the STM8 Evaluation board through the U2. On the Table 9 the cross reference connection table between L9396 Demo Board and the STM8 Evaluation board is shown. Note that not all the signals are physically connected.

Table 9. L9396 to STM8 cross connection

J27 L9396 to STM8 cross connection								
PIN #	A		B		C		D	
	L9396	STM8	L9396	STM8	L9396	STM8	L9396	STM8
1	5V_DB	5V_DB	RESET_UC	NRESET	n.c.		n.c.	
2	5V_MB	5V_Perm	n.c.		n.c.		n.c.	
3	FSN	PB0/AIN0/TIM1_NCC1	n.c.		n.c.		n.c.	
4	RESET_IN	PB1/AIN1/TIM1_NCC2	n.c.		n.c.		n.c.	
5	n.c.		n.c.		n.c.		n.c.	
6	n.c.		n.c.		n.c.		n.c.	
7	WDIS_AN	PB4/AIN4	n.c.		n.c.		n.c.	
8	VCORE	PB5/AIN5	n.c.		n.c.		n.c.	
9	VCC	PB6/AIN6	CS	PE5/SPI_NSS	n.c.		n.c.	
10	VDD	PB7/AIN7	SCLK	PC5/SPI_SCK	n.c.		n.c.	
11	n.c.		MOSI	PC6/SPI_MOSI	n.c.		n.c.	
12	n.c.		MISO	PC7/SPI_MISO PIU20 PIU20	n.c.		n.c.	
13	n.c.		ALT_CS	PE1/I2C_SCL	n.c.		n.c.	
14	n.c.		n.c.		n.c.		n.c.	
15	n.c.		n.c.		n.c.		n.c.	
16	n.c.		n.c.		n.c.		n.c.	
17	n.c.		n.c.		n.c.		n.c.	
18	n.c.		n.c.		n.c.		n.c.	
19	PRN	PA3/TIM2_CC3	n.c.		n.c.		n.c.	
20	n.c.		n.c.		n.c.		n.c.	
21	WSO0	PC1(HS)/TIM1_CC1	n.c.		n.c.		GND	
22	WSO1	PC2(HS)/TIM1_CC2	n.c.		n.c.		GND	
23	WSO2	PC3(HS)/TIM1_CC3	n.c.		n.c.		GND	
24	WSO3	PC4(HS)/TIM1_CC4	n.c.		n.c.		GND	
25	PRI	PD0(HS)/TIM3_CC2	n.c.		n.c.		GND	
26	PDI	PD2(HS)/TIM3_CC1	n.c.		n.c.		GND	
27	AI1_UC	PD3(HS)/TIM2_CC2	n.c.		n.c.		GND	
28	AI0_UC	PD4(HS)TIM2_CC1	n.c.		n.c.		GND	

J27 L9396 to STM8 cross connection								
PIN #	A		B		C		D	
	L9396	STM8	L9396	STM8	L9396	STM8	L9396	STM8
29	n.c.		n.c.		n.c.		GND	
30	n.c.		n.c.		n.c.		GND	
31	n.c.		n.c.		n.c.		n.c.	
32	WK_INT	PE4	n.c.		n.c.		n.c.	
33	GATE3/IGN	PH7/TIM1_NCC1	n.c.		n.c.		n.c.	
34	n.c.		n.c.		n.c.		n.c.	
35	n.c.		n.c.		n.c.		n.c.	
36	n.c.		n.c.		n.c.		n.c.	
37	FAULT	PH3	n.c.		n.c.		n.c.	
38	n.c.		n.c.		n.c.		n.c.	
39	n.c.		n.c.		n.c.		n.c.	
40	n.c.		n.c.		n.c.		n.c.	

3.1.6 Test point list

Table 10. Test point list

Name	Description
TP1	VBAT
TP2	VBATP
TP3	GND
TP4	FAULT
TP5	WSO3
TP6	WSO2
TP7	WSO1
TP8	CS
TP9	PRN
TP10	SCLK
TP11	MOSI
TP12	MISO
TP13	FSN
TP14	RESET
TP15	WSO0
TP16	I_CORE_SL
TP17	GCORE
TP18	VDG
TP19	AI1
TP20	AI0
TP21	CP
TP22	VDBATT

Name	Description
TP23	VBST
TP24	VPREREG
TP25	WDTDIS
TP26	AI3
TP27	AI2
TP28	IGN
TP34	GPOD0
TP35	PDI
TP36	VCORE
TP37	PRI
TP38	PRG
TP39	PRS
TP40	PDG
TP41	PDS
TP42	PDBATT
TP47	BCKSW
TP48	GNDD

Revision history

Table 11. **Document revision history**

Date	Version	Changes
09-Sep-2021	1	Initial release.
22-Sep-2025	2	Update Section 2.2.1.

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