Application note

L99LDLH32 – (O)LED supply voltage regulation

Introduction

The use of multichannel linear current regulator is often limited by the total power dissipation. In the device, the application can take into account the reasonable efforts for thermal management and heat spreading. As a general rule, assuming that the die pads of the QFN7x7 48L are connected through thermal vias to a continuous copper plane, the total power dissipation allowed in a single device is about 2.0 - 2.5 W. In order to stay within this power dissipation limit, it is essential to check the voltage drop on each of the 32 linear current regulators. The output current regulator, to ensure the correct operation at all operating temperature and current conditions, requires a minimum voltage drop (VOUTx_DROP). This minimum VOUTx_DROP must be ensured through the application of a sufficiently high precontroller supply voltage. Due to the number of channels and the sum of the current to be regulated, for efficiency reason, it is assumed that the pre regulator is a DC/DC switching converter. In overtemperature, the supply voltage required for the LEDs (O) could be higher or lower than the battery voltage. In this case, a converter with step-up & down capability is required, for example a SEPIC topology. In order to avoid excessive power dissipation, as already explained above, the power supply voltage of the pre regulator must be neither too low nor too high. Things get even more complicated because the voltage drop across (O) LED varies with the type, the current, the temperature and the aging. This complex situation, dependent on many variables, can be solved thanks to the L99LDLH32.

1 (O)LED supply voltage regulation

1.1 VREF_PRE_REG feature description

The L99LDLH32 features one analog pin (VREF_PRE_REG) providing a voltage proportional to the maximum output voltage of active channels plus the required drop voltage across the current regulator required for proper regulation. This signal can be used in combination with an analogue discrete circuit to directly close the feedback loop with an external DC/DC converter. This feature can be enabled or disabled by the VREF_PRE_REG configuration bit in the RAM respectively FTP memory map.

The VREF_PRE_REG generation is based on an algorithm able to verify which string has the highest drop voltage, adding a minimum drop on the integrated linear switches to grant the proper current regulation.

Two different kinds of regulation algorithm can be selected through a specific configuration bit in the NVM area section accessible in the STMicroelectronics testing flow: an open loop control - and a closed loop regulation algorithm for providing the analog feedback. While the open loop control method is the best solution when several L99LDLH32 devices share the same DC/DC regulator, the closed loop regulation algorithm is able to compensate even for tolerances of external components and can further minimize power dissipation. It works when only one L99LDLH32 is connected to the DC/DC regulator.

Both methods are deeper described in the following chapters.

1.1.1 Open loop control algorithm

The generated analog feedback is proportional to the sum of the highest (O)LED string voltage and the target output voltage drop (~1.4 V).

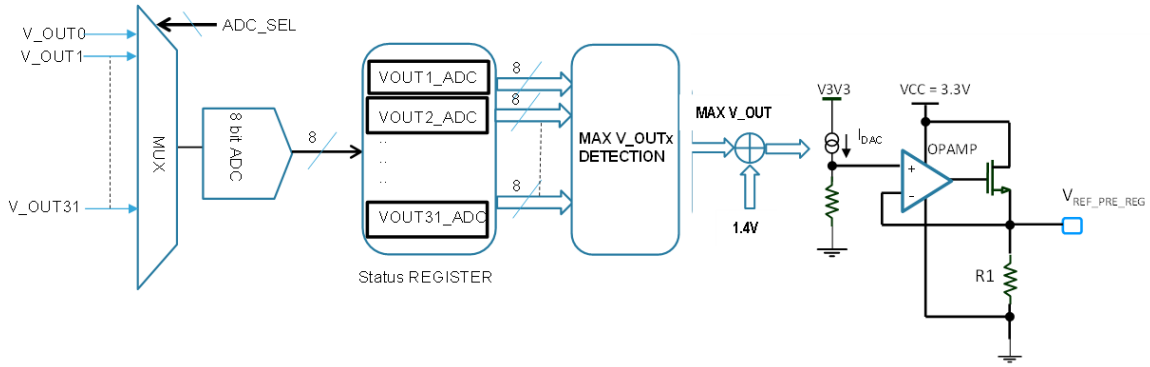
The result is expressed by the following equation:

Equation 1

$$V_{REF\_PRE\_REG} = K \times (V_{OUTMAX} + 1.4) \quad (1)$$

In L99LDLH32 the proportional “K” factor is equal to 0.05.

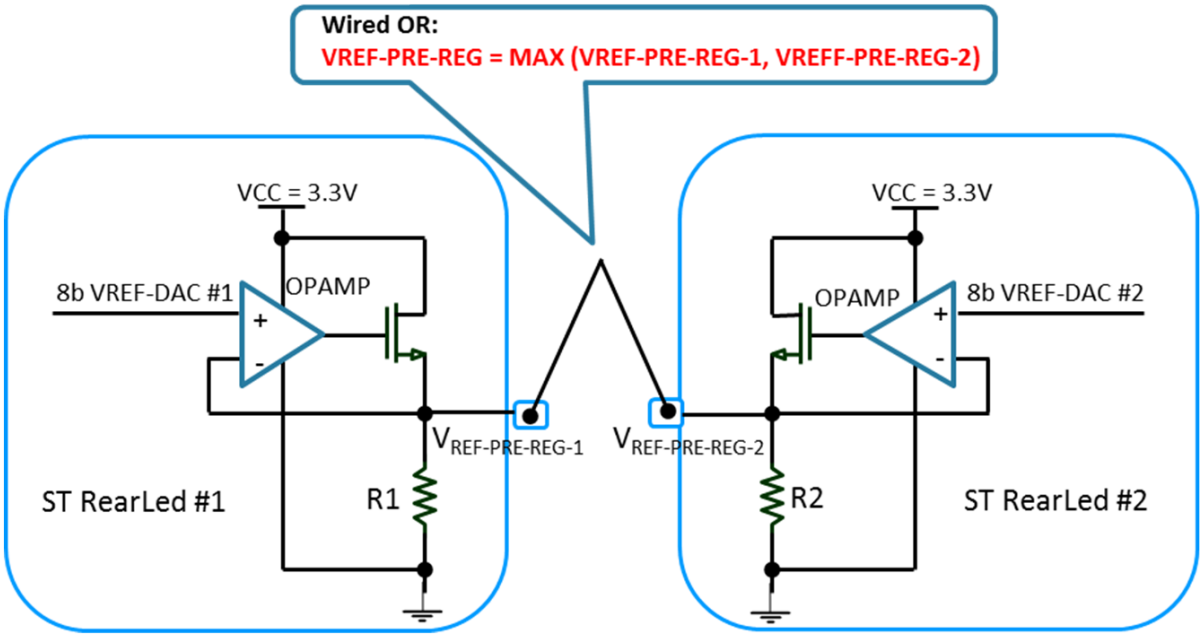
Figure 1. $V_{REF\_PRE\_REG}$ – generation concept



The output voltage of each of the maximum 32 active channels is sampled by the integrated ADC once during PWM on-phase every PWM period. The sampling is masked for all those channels with a PWM on-time shorter than t_DIAG_BLANK. The control block determines the maximum VOUT and adds the desired drop voltage (1.4 V). Finally, the VREF_PRE_REG voltage is calculated according to 1 and the output DAC is set accordingly.

As it can be seen from Figure 1. $V_{REF\_PRE\_REG}$ – generation concept, the VREF_PRE_REG output signal is buffered. For applications with a common DC/DC converter, this allows to wire-OR the VREF_PRE_REG output signal from several devices to provide only the highest reference voltage back to the DC/DC (see Figure 2. Wired-OR connection between two or more (O)LED drivers). The output with the highest VREF_PRE_REG, being applied also to the inverting pin of the other device with low reference, will force to depolarize the output MOS, disabling the buffer having the lower voltage.

Figure 2. **Wired-OR connection between two or more (O)LED drivers**



It is to be noted, regardless of the PWM frequency, that the VREF_PRE_REG signal is updated every 21 ms. This delay time has been introduced to make sure the VREF_PRE_REG signal is changed more slowly than the load regulation time constant of the DC/DC converter (bandwidth), thus avoiding interference of the DC/DC own regulator loop with this algorithm.

VREF_PRE_REG voltage operating range is between 0.0 V minimum and 2.0 V maximum.

Figure 3. $V_{REF\_PRE\_REG}$ - flow chart illustrates the working principle of the open loop algorithm. When the VREF_PRE_REG control bit in the device configuration #3 register is set, the algorithm is disabled and the maximum VREF_PRE_REG voltage is applied. If the VREF_PRE_REG control bit in the device configuration #3 register is cleared, the algorithm is enabled. Then, as long as all output channels are disabled and the algorithm is not running, a minimum VREF_PRE_REG voltage of 0.25 V is applied, in order:

1. not to interfere with running algorithm on other ICs sharing the same DC/DC voltage regulator
2. always ensure the DC/DC voltage regulator supplies a certain minimum voltage

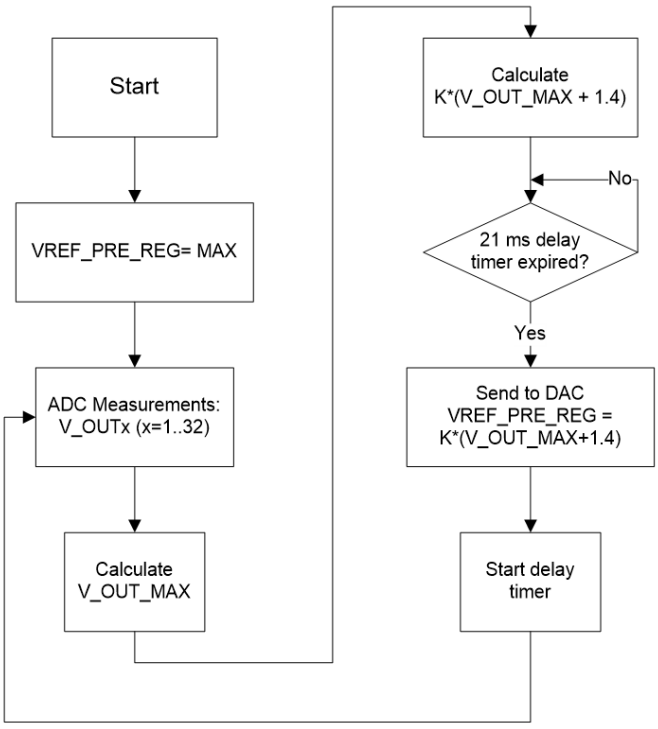
As soon as a channel is enabled, the VREF_PRE_REG voltage is set to its maximum value. This is done, because the forward voltage of the string connected to this channel cannot be known a priori, therefore the preregulator voltage is set to its maximum value to generate the maximum preregulator voltage to ensure a sufficient supply voltage is applied to the string.

A side remark: a condition when VREF_PRE_REG voltage is set to its maximum value can be detected by the application checking the VREF_PRE_REG_MAX status bit in the device status register #3.

Then, the output voltage of all active channels is measured and the maximum out of it is determined. Based on this value the device calculates VREF_PRE_REG voltage, checks if the 21 ms delay timer is expired and if this is the case, provides the calculated code to the DAC.

In case an open-load event occurs on any channel while the algorithm is running and while the device is validating the open-load condition, the algorithm restarts from the initial step, setting the VREF_PRE_REGx to the maximum value, trying to solve the open-load condition. Inactive channels and channels which are latched off due to a validated fault condition (open load, short-circuit, or short-circuit to GND) won´t be taken into account for the VOUT_MAX determination. If the on time during a PWM period of any channel is too short to allow ADC conversion (basically t_on < t_DIAG_BLANK + 3 µs), the VREF_PRE_REG voltage is set to its maximum value.

Figure 3. $V_{REF\_PRE\_REG}$ - flow chart



The device features a Power Good threshold supervision. This Power Good threshold supervises the VPRE_REG voltage (DC/DC regulator output voltage). When the Power Good threshold is reached, the open-load diagnostic is enabled, otherwise it remains disabled. Only when the VPRE_REG voltage is sufficiently high, the L99LDLH32 output current regulators can source the configured load current. If the VPRE_REG voltage is too low, a false open load failure could be detected. This is avoided by the Power Good threshold supervision. The VREF_PRE_REG open loop control algorithm may lead to situations in which VPRE_REG voltage is temporarily set below the configured Power Good threshold. To avoid application malfunction in such scenario, the following steps need to be applied:

1. the device autonomously disables the supervision of the Power Good threshold while the VREF_PRE_REG open loop control algorithm is running and VREF_PRE_REG is not set to VREF_PRE_REG_MAX. The PG_NOT_VPRE_REG bit in the device status register #3 won´t be refreshed as long as the algorithm is running
2. whenever PG_NOT_VPRE_REG is set, the application shall temporarily deactivate the Pre-Regulator control algorithm, by two consecutive UNICAST WRITE frames to disable and enable the VREF_PRE_REG bit.

Figure 4. $V_{REF\_PRE\_REG}$ - operating example

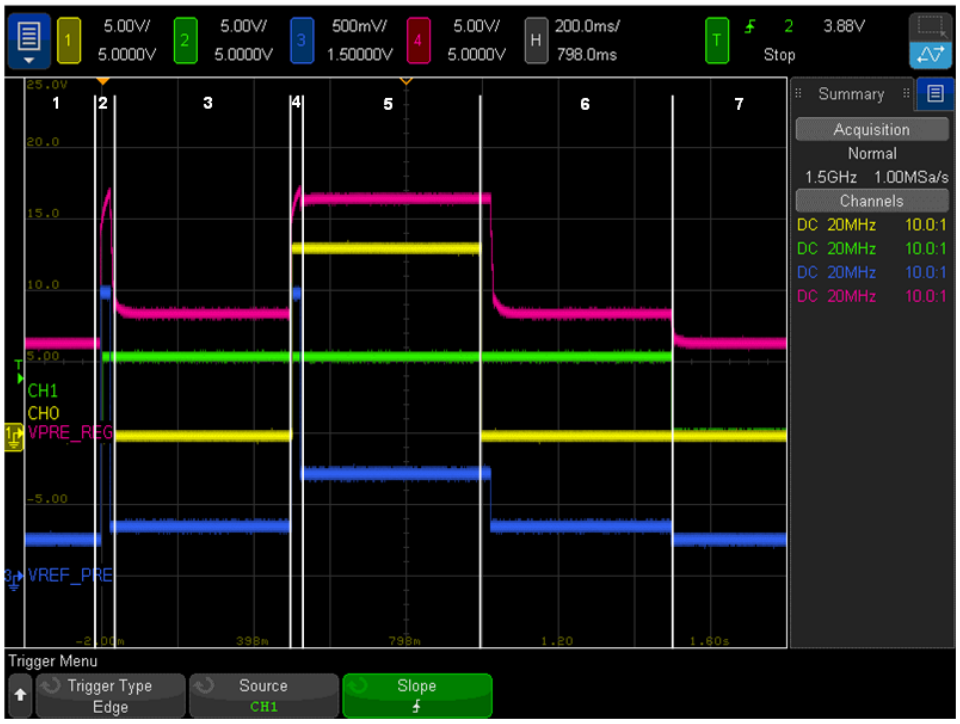
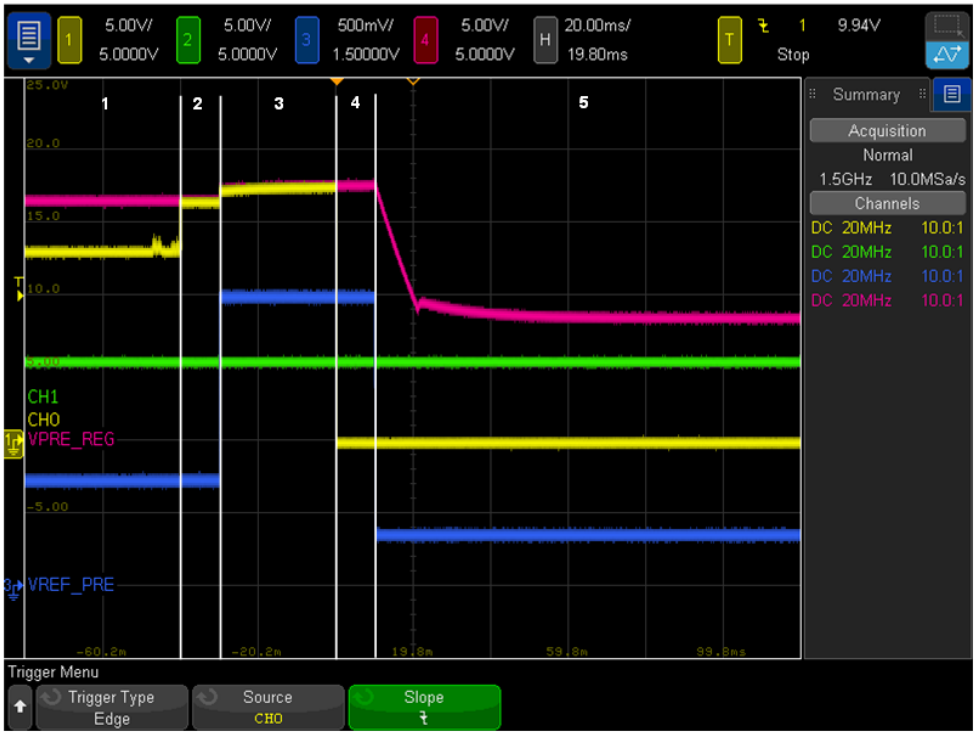


Figure 4. $V_{REF\_PRE\_REG}$ - operating example illustrates the working principle of the VREF_PRE_REG generation. In Phase 1 the open loop control algorithm is enabled, but all output channels are off. VREF_PRE_REG is set to its minimum voltage when algorithm is not running. Phase 2, channel 1 driving a short string is turned on. Consequently, VREF_PRE_REG is set to its maximum voltage, the DC/DC regulator tries to follow it. Phase 3, VOUT_MAX was determined and VREF_PRE_REG is set. Phase 4, channel 0 driving a long string is activated and VREF_PRE_REG voltage is set again to the maximum voltage. Phase 5, VOUT_MAX (now ch0) was determined and VREF_PRE_REG is set accordingly to Equation 1. Phase 6, channel 0 is turned off, and VREF_PRE_REG is reduced to optimize the Power Dissipation considering the active channel 1. Phase 7, channel 1 as last active channel is turned off, VREF_PRE_REG is set to its minimum when algorithm is not running.

Figure 5. $V_{REF\_PRE\_REG}$ - open load

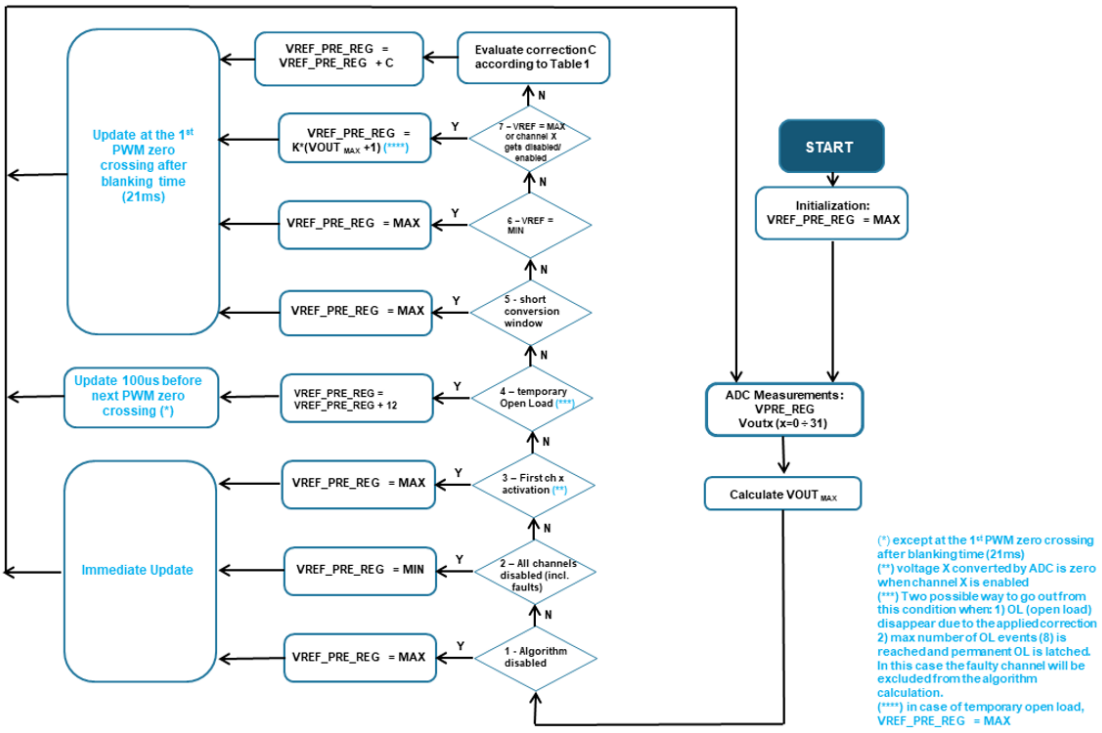


While actuator fault conditions like shorted (O)LEDs or short to GND can be easily managed by the control loop, in fact such fault conditions are “just” lead to a lower VOUT, an open load fault is more critical to handle. Figure 5. $V_{REF\_PRE\_REG}$ - open load depicts such situation: Phase 1: two channels, channel 1 with a short string and channel 0 with a long string are active with VREF_PRE_REG set to K*(VOUT_CH0 +1.4 V). Phase 2, an open load condition occurs at ch0, its output voltage is rising to the DC/DC regulator output voltage (VPRE_REG). Phase 3, the open loop control algorithm detected the open load condition and raised VREF_PRE_REG to its maximum voltage, VPRE_REG is increasing to its maximum voltage defined by the external circuit, while the output is maintained on as long as the temporary open load condition is validated/invalidated bounced by the device. Phase 4, the open load validation is completed by the device, the open load is confirmed as permanent fault and the corresponding channel is latched off. Phase 5, the open loop control algorithm sets the VREF_PRE_REG voltage accordingly, disregarding the latched channel(s).

1.1.2 Closed loop regulation algorithm

The closed loop regulation algorithm can be applied when only one L99LDLH32 device is supposed to control the DC/DC regulator output voltage. In comparison to the open load control algorithm there are some fundamental differences which are explained by means of the following figure.

Figure 6. Closed loop regulation flow chart



The initial steps are quite the same as in the open loop case. To avoid potential false Open Load generation, the external pre-regulator voltage has to be higher than the minimum supply voltage required by the highest LED string.

Then, at the start of the algorithm, the VREF_PRE_REG voltage is initialized to its maximum value setting the external pre-regulator to the maximum value. After this first step, the internal ADC measures the $VOUT_X$ of all active channels.

The maximum (O)LED voltage drop is coincident with the VOUT_MAX, so the engine calculates the maximum value among the $VOUT_X$ (x = from 0 to 31).

The next three steps are again like in the open loop concept, except when the VREF_PRE_REG voltage is updated always immediately, not waiting the elapse of the 21 ms delay timer.

The first major difference is the temporary open load handling. As soon as a temporary open load condition is detected, the drop voltage between pre-regulator output voltage (VPRE_REG) and the L99LDLH32 channel output voltage (VOUTx) drop below the VOL_TH threshold, a temporary open load event is triggered internally in the device and the open-load validation procedure is starting. During each PWM period, the drop voltage is measured again and, as long as the temporary open load condition is confirmed, the VREF_PRE_REG voltage is increased every PWM period by 94 mV. The process stops as soon as the VPRE_REG voltage is increased sufficiently to resolve the open load condition, or the open load validation process is completed by confirming the open load fault as permanent. In the latter case the channel is latched off and VREF_PRE_REG is set to its maximum (see step 7 of the flow chart).

If the on-time of any channel during a PWM period is too short to allow the ADC sampling of the output voltage, basically when t_ON < t_DIAG_BLANK, VREF_PRE_REG is set to the maximum value (flow chart step 5). The open loop formula is applied if condition 7 of the flow chart (Figure 6. Closed loop regulation flow chart) is fulfilled (regulator running at its maximum value) but only if all the previous conditions at the highest priority are not satisfied.

After this step, and in case none of the conditions 1 to 7 are matched, the difference (VPRE_REG – $VOUT_{MAX}$) is evaluated to determine a correction factor “C” as follows:

Table 1. Correction factor “C” for closing the loop

VPRE_REG – $VOUT_{MAX}$	Correction (C)
$<V_{OL\_TH}$	+94.1 mV
< 0.63 V	+31.4 mV
< 1.25 V	+7.8 mV
≤ 1.57 V	0
≤ 1.88 V	-7.8 mV
≤ 2.198 V	-15.6 mV
> 2.198 V	-31.4 mV

The value of VREF_PRE_REG is updated adding or subtracting the “C” value at the first PWM duty cycle after 21 ms of blanking time. This correction factor acts closing the feedback loop. Regardless of the tolerances of the external circuit components, the closed loop algorithm moves the VREF_PRE_REG voltage accordingly to generate a voltage drop of about 1.4 V across the channel with VOUT_MAX.

The following figure depicts the operating principle of the closed loop regulation algorithm based on an application example turning on/off sequentially a short and a long load string. The different steps of actions are explained in Table 2. Stepwise explanation. To challenge the capability of the closed loop algorithm to compensate even a significant error on the gain factor of the external circuit, a positive error of approximately 5 V was intentionally introduced in the circuit.

Figure 7. $V_{REF\_PRE\_REG}$ - operating example closed loop algorithm

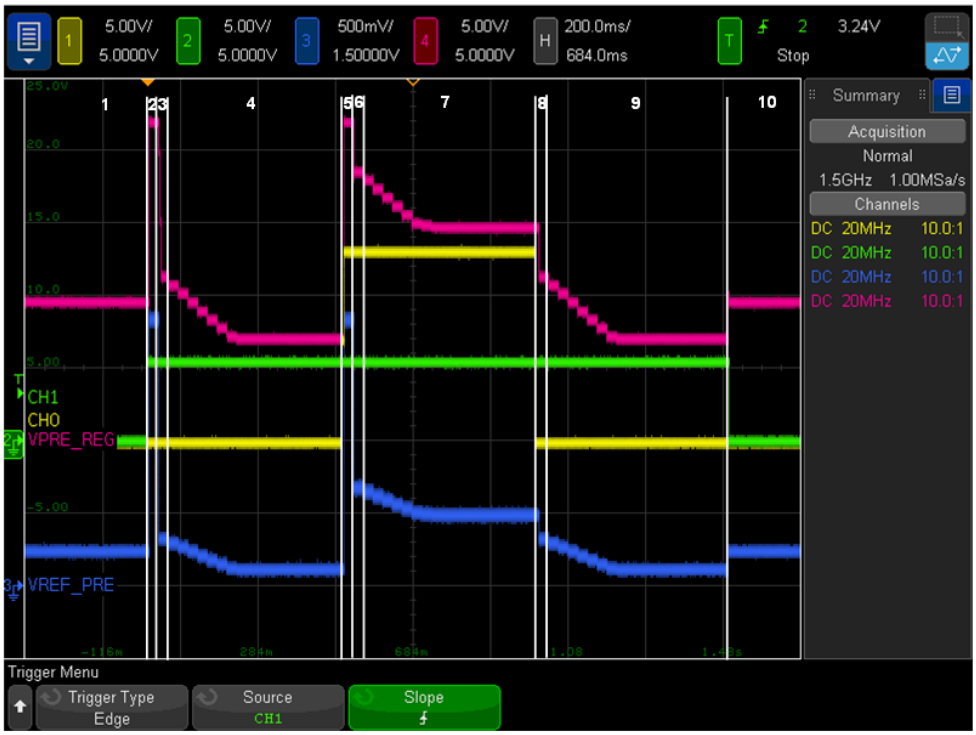


Table 2. Stepwise explanation

Step	Circuit behaviour
1	All channels off, VREF_PRE_REG set to minimum voltage when algorithm is not running according to condition 2 of the flow chart
2	Channel 1 short string turned on, VREF_PRE_REG set to maximum according to condition 3 of the flow chart
3	Open loop formula (Equation 1) applied according to condition 7 of the flow chart - ~ 7 V difference between VPRE_REG and VOUT_MAX
4	Closed loop adaptation with correction steps “C” applied. Circuit error is compensated by the loop. VPRE_REG – VOUT_MAX stepwise reduced to ~ 1.5 V
5	Channel 0 long string turned on, VREF_PRE_REG set to maximum according to condition 3 of the flow chart
6	Open loop formula (Equation 1) applied according to condition 7 of the flow chart - ~ 7 V difference between VPRE_REG and VOUT_MAX
7	Closed loop adaptation with correction steps “C” applied. Circuit error is compensated by the loop. VPRE_REG – VOUT_MAX stepwise reduced to ~ 1.5 V
8	Channel 0 long string is deactivated. Open loop formula (Equation 1) applied according to condition 7 of the flow chart - ~ 7 V difference between VPRE_REG and VOUT_MAX
9	Closed loop adaptation with correction steps “C” applied. Circuit error is compensated by the loop. VPRE_REG – VOUT_MAX stepwise reduced to ~ 1.5 V
10	Channel 1 short string is deactivated. All channels off. VREF_PRE_REG is set to minimum voltage when algorithm is not running according to condition 2 of the flow chart

How the closed loop control algorithm manages an open load fault case is illustrated in the following figure.

Figure 8. $V_{REF\_PRE\_REG}$ - operating example closed loop algorithm in open load

Table 3. **Stepwise explanation of previous figure**

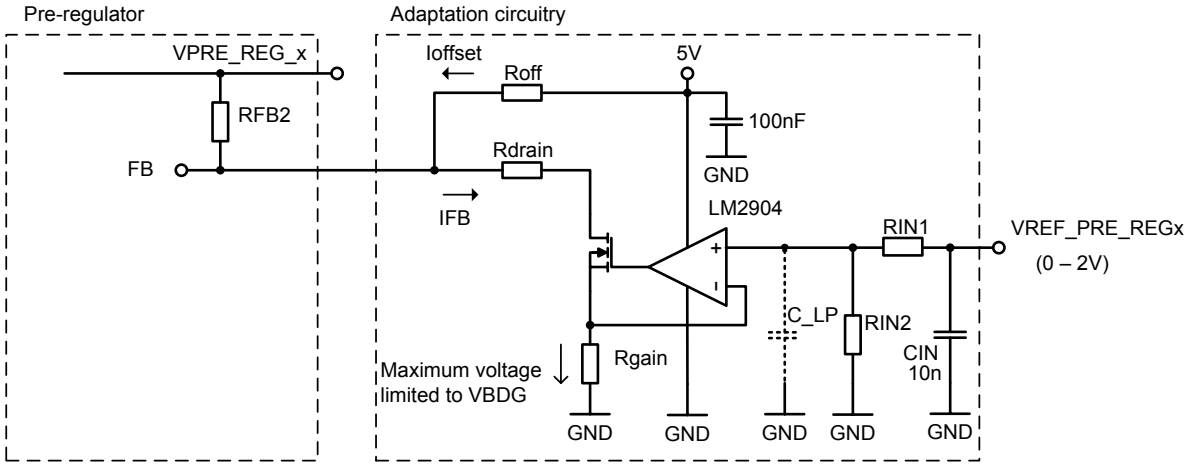
Step	Circuit behaviour
1	Channel 0 & 1 on, circuit in closed loop adaptation
2	Open Load on Channel 0. Open load validation procedure running in the device. VREF_PRE_REG is stepwise increased every PWM period
3	Open Load validated on Channel 0. Channel latched off. VREF_PRE_REG set to maximum
4	VREF_PRE_REG set according to open loop formula with Channel 1 as VOUT_MAX
5	Closed loop adaptation with correction steps “C” applied. Circuit error is compensated by the loop. VPRE_REG – VOUT_MAX stepwise reduced to ~ 1.5 V

1.2 HW design of feedback loop - circuit schematics

Most of the DC/DC regulators on the market do not offer an adjustable reference voltage accessible through a dedicated pin, but the majority of the devices offer a feedback pin. The voltage on this feedback pin is compared against a precise reference (in many cases the band gap voltage) and the error is amplified. If the feedback voltage is higher than the reference voltage, the DC/DC regulator tries to reduce its regulated output voltage and vice versa. Therefore, the VREF_PRE_REG voltage generated by the L99LDLH32 cannot be connected directly to the DC/DC regulator, but an external circuit is needed to convert the VREF_PRE_REG voltage into a feedback voltage.

1.2.1 Circuit schematics for open loop control algorithm

Figure 9. **Circuit schematics connecting $V_{REF\_PRE\_REG}$ signal(s) to feedback pin**



The adaptation circuitry works as voltage → current converter. The VREF_PRE_REG voltage, provided by the L99LDLH32 device(s), calculated as per Equation 1, is translated to a current sunk from the upper resistor of the feedback divider RFB2 (bottom resistor is not present) of the DC/DC (SEPIC) converter. The voltage → current conversion ratio is defined by the Rgain resistor and by the RIN1 and RIN2 divider on the input. This divider is required to keep the OPAmp non-inverting input voltage below the feedback voltage to allow proper regulation. To dimension the RIN divider properly, it has to be considered the internal impedance of the VREF_PRE_REG signal of ~ 700 Ω. The Rdrain limits the maximum possible feedback current and so limits the maximum SEPIC output voltage to the required level. The C_LP capacitor on the non-inverting input of the OPAmp is optional. Together with RIN1 it forms a low pass filter to slow down the feedback loop. Depending on the type of the DC/DC converter and its bandwidth it might be needed or not. As implementation guideline, the time constant of this low pass filter should not exceed 3 ms. The resistors should be dimensioned according to the following formulas:

Equation 2

$$R_{IN\_Ratio} = \frac{R_{IN2}}{R_{IN2} + R_{IN1} + 700\Omega} \quad (2)$$

Equation 3

$$R_{gain} = K \cdot R_{INRatio} \cdot R_{FB2} \quad (3)$$

Equation 4

$$R_{drain} = \frac{V_{FB} \cdot R_{FB2}}{V_{PRE\_REG\_MAX}} - R_{gain} \quad (4)$$

An additional offset current can be added by the R_{OFF} resistor in order to compensate the V_{FB} voltage shift of the FB node (so to align the 0V VREF_PRE_REG input to the 0V VPRE_REG output)

Equation 5

$$R_{OFF} = \frac{R_{FB2} \cdot (5V - V_{FB})}{V_{PRE\_REG\_MAX}} \quad (5)$$

Having defined those values, the VPRE_REG voltage is calculated as

Equation 6

$$V_{PRE\_REG} = VREF_{PRE\_reg} \cdot \frac{R_{INRatio} \cdot R_{FB2}}{R_{gain}} + V_{FB} - I_{offset} \cdot R_{FB2} \quad (6)$$

1.2.1.1 *Application example (1)*

Figure 10. Calculation of resistor dimensioning for application example

External adaptation circuitry - component value calculator			
VOFFSUPPLY	5	V	Offset resistor supply voltage (for Roff calculation)
VBDG	0,7	V	Reference voltage of external preregulator
VPRE_REG max.	18	V	Maximum output voltage of the pre-regulator (for Rdrain calculation)
K	0,05	-	K factor (0.1 for L99LDLL16, 0.05 for L99LDLH32)
RFB2	43	kohm	Upper resistor of feedback divider
RIN1	27	kohm	Upper resistor of control voltage divider
RIN2	33	kohm	Lower resistor of control voltage divider
Vref_pre impedance	0,7	kohm	Internal resistance of Vref_pre output
RIN_ratio	0,543657331	-	Control voltage divider ratio (out/in)
Rgain	1,168863262	kohm	Current sink shunt resistor
Roff	264,1428571	kohm	Offset current definition resistor
Rdrain	0,50335896	kohm	Maximum VPRE_REG voltage definition resistor

As it can be seen from the above calculation example, the offset resistor calculation results in a quite high number. As it often happens in automotive design, resistors higher than 100 k are not tolerated in circuit schematics. Therefore the offset resistor can be even skipped producing a small error.

Without this resistor, the SEPIC output voltage will be shifted by V_{FB} higher. A positive shift is anyway required, considering all the tolerances of components, since the circuitry must provide enough output voltage > (V_{OUT_MAX}+1.4 V) also in worst case combination of component tolerances. All these calculations are available in a separate calculator:

Figure 11. Tolerances for worst case calculation

Vref pre reg Impedance	40	% tolerance
RFB2	1	% tolerance
Bandgap	1	% tolerance
Voff_supply	3	% tolerance
Roff	1	% tolerance
Rgain	1	% tolerance
Rdrain	1	% tolerance
RIN1	1	% tolerance
RIN2	1	% tolerance
K	7	% tolerance
OpAmp offset	2	mV

Figure 12. Worst case SEPIC output voltage spread considering all tolerances

Vout (OLED)	8 V			
	min	typ	max	
Vref_pre (floating)	0,437 V	0,471 V	0,503 V	Vref_pre (floating)=(Vout+1.4)*k
V_Rgain	0,232 V	0,256 V	0,279 V	V_Rgain=Vref_pre*RIN2/(Vref_resistance+RIN1+RIN2)
IFB	0,209 mA	0,233 mA	0,256 mA	IFB=V_Rgain/Rgain
Ioffset	0,000 mA	0,000 mA	0,000 mA	Ioffset=(Voff_supply-Vbdg)/Roff
Vpre_reg	9,598 V	10,699 V	11,839 V	Vpre_reg=(IFB-Ioffset)*RFB2+VBDG
Vpre_reg_max	17,103 V	17,610 V	18,131 V	Vpre_reg_max=(VBDG/(Rgain+Rdrain)-(VOFFSUPPLY-VBDG)/Roff)*RFB_2+VBDG

	Vref_pre (floating) [V]			Vpre_reg [V]			Vpre_reg - Vout [V]			V_Rgain [V]			IFB [mA]		
Vout (OLED) [V]	min	typ	max	min	typ	max	min	typ	max	min	typ	max	min	typ	max
4	0,251	0,270	0,289	5,78	6,44	7,14	1,78	2,44	3,14	0,133	0,147	0,161	0,119	0,133	0,148
5	0,298	0,320	0,342	6,73	7,50	8,31	1,73	2,50	3,31	0,158	0,174	0,191	0,142	0,158	0,175
6	0,344	0,370	0,396	7,69	8,56	9,49	1,69	2,56	3,49	0,183	0,201	0,220	0,164	0,183	0,202
7	0,391	0,420	0,449	8,64	9,63	10,66	1,64	2,63	3,66	0,207	0,228	0,250	0,187	0,208	0,229
8	0,437	0,470	0,503	9,60	10,69	11,84	1,60	2,69	3,84	0,232	0,256	0,279	0,209	0,232	0,256
9	0,484	0,520	0,556	10,55	11,75	13,02	1,55	2,75	4,02	0,257	0,283	0,309	0,232	0,257	0,283
10	0,530	0,570	0,610	11,51	12,81	14,19	1,51	2,81	4,19	0,282	0,310	0,338	0,254	0,282	0,310
11	0,577	0,620	0,663	12,46	13,88	15,37	1,46	2,88	4,37	0,307	0,337	0,368	0,277	0,306	0,338
12	0,623	0,670	0,717	13,42	14,94	16,54	1,42	2,94	4,54	0,332	0,364	0,397	0,299	0,331	0,365
13	0,670	0,720	0,770	14,38	16,00	17,72	1,38	3,00	4,72	0,357	0,391	0,427	0,321	0,356	0,392
14	0,716	0,770	0,824	15,33	17,06	18,89	1,33	3,06	4,89	0,382	0,419	0,456	0,344	0,381	0,419
15	0,763	0,820	0,877	16,29	18,13	20,07	1,29	3,13	5,07	0,407	0,446	0,486	0,366	0,405	0,446
16	0,809	0,870	0,931	17,24	19,19	21,25	1,24	3,19	5,25	0,432	0,473	0,515	0,389	0,430	0,473
17	0,856	0,920	0,984	18,20	20,25	22,42	1,20	3,25	5,42	0,457	0,500	0,544	0,411	0,455	0,500
18	0,902	0,970	1,038	19,15	21,31	23,60	1,15	3,31	5,60	0,482	0,527	0,574	0,434	0,479	0,527
19	0,949	1,020	1,091	20,11	22,38	24,77	1,11	3,38	5,77	0,507	0,555	0,603	0,456	0,504	0,554
20	0,995	1,070	1,145	21,06	23,44	25,95	1,06	3,44	5,95	0,532	0,582	0,633	0,479	0,529	0,581

As seen in Figure 12. Worst case SEPIC output voltage spread considering all tolerances, the resistor values are calculated so that the worst case minimum SEPIC output voltage is ~1.4 V above V_{OUT} (OLED), to guarantee proper current regulation. A typical SEPIC voltage is then about 2.5 V/3 V above the V_{OUT}.

1.2.1.2 *Experimental circuit verification with SEPIC converter evaluation board*

Figure 13. Circuit Schematics with SEPIC topology

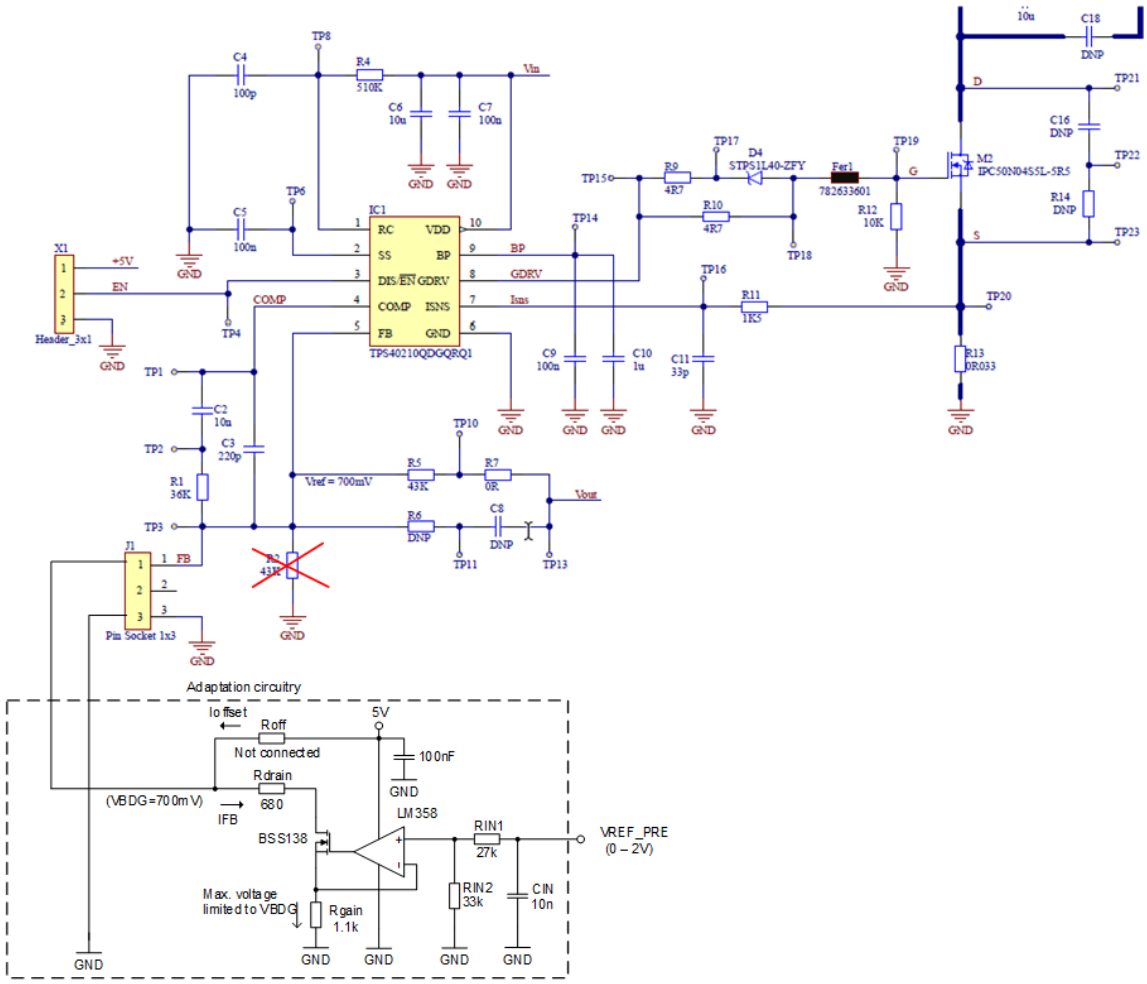
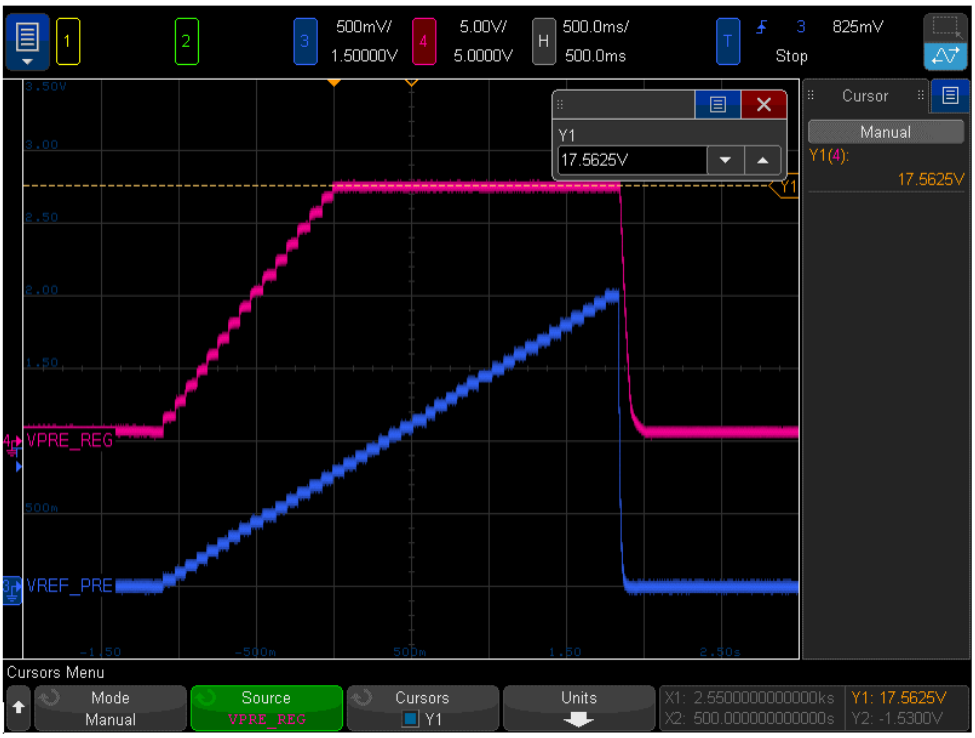


Table 4. V_{PRE_REG} vs VREF_PRE_REG measurement

VREF_PRE_REG [V]	Measured VPRE_REG [V]	Calculated VPRE_REG [V]
0.25	6.10	6.08
0.30	7.18	7.15
0.35	8.28	8.23
0.40	9.36	9.30
0.45	10.44	10.38
0.50	11.52	11.45
0.55	12.60	12.53
0.60	13.68	13.60
0.65	14.78	14.68
0.70	15.86	15.75
0.75	16.94	16.83
0.80	17.60	17.61

VREF_PRE_REG [V]	Measured VPRE_REG [V]	Calculated VPRE_REG [V]
0.85	17.60	17.61
0.90	17.60	17.61
0.95	17.60	17.61
1.00	17.60	17.61
1.05	17.60	17.61
1.10	17.60	17.61
1.15	17.60	17.61
1.20	17.60	17.61
1.25	17.60	17.61
1.30	17.60	17.61
1.35	17.60	17.61
1.40	17.60	17.61
1.45	17.60	17.61
1.50	17.60	17.61
1.55	17.60	17.61
1.60	17.60	17.61
1.65	17.60	17.61
1.70	17.60	17.61
1.75	17.60	17.61
1.80	17.60	17.61
1.85	17.60	17.61
1.90	17.60	17.61
1.95	17.60	17.61
2.00	17.60	17.61

Figure 14. V_{PRE_REG} vs VREF_PRE_REG measurements

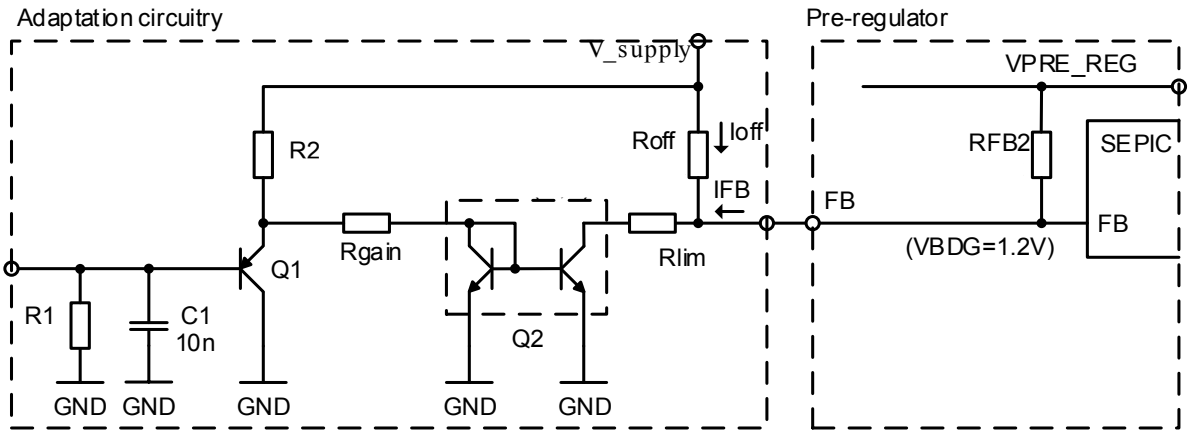


The measured SEPIC output voltage for a given VREF_PRE_REG input voltage perfectly corresponds to typical calculated values.

1.2.2 Circuit schematics for closed loop regulation algorithm

1.2.2.1 Low-cost solution with BJT devices

Figure 15. Circuit schematics connecting $V_{REF\_PRE\_REG}$ signal(s) to feedback pin



A low cost solution avoiding OpAmps has been targeted. The adaptation circuitry works as voltage → current converter. The VREF_PRE_REG input voltage is translated to current sunk from the upper resistor of the feedback divider RFB2 (bottom resistor is not present). The RFB2 value should not be selected too high in order to operate at higher current levels and so to minimize sensitivity to noise and leakages. An additional offset current is added by the Roff resistor in order to compensate the VFB voltage shift of the FB node (so to align the 0V VREF_PRE_REG input to the 0V VPRE_REG output).

The voltage → current conversion ratio is defined by the Rgain resistor. The Q1 transistor (emitter follower) acts as a level shifter shifting the VREF_PRE_REG voltage by one junction drop higher to be inside the operating range of the NPN current mirror and so to work in the whole VREF_PRE_REG voltage range. The current mirror is realized using a dual NPN transistor in one package which minimizes temperature difference between them. Even if the exact parameter matching is not guaranteed for this low cost type, it is still better than using individual transistors. The Rlim resistor in series with current mirror output is used for adjusting the maximum VPRE_REG voltage. The output current of the mirror is limited when the voltage drop across the RLIM reaches VBDG.

The resistors are to be dimensioned as follows:

Equation 7

$$R_{OFF} = \frac{R_{FB2} \cdot \left(V_{Supply} - V_{FB}\right)}{V_{FB}} \quad (7)$$

Equation 8

$$R_{lim} = \frac{\left(V_{FB} - V_{CE_{SAT}}(Q2)\right)}{\frac{V_{PRE\_REG_{MAX}} - V_{FB}}{R_{FB2}} + \frac{V_{supply} - V_{FB}}{R_{off}}} \quad (8)$$

V_CE_SAT is the saturation collector emitter drop voltage across the NPN current mirror. To ensure Q1 is working properly as a level shifter a certain minimum collector current I_CE_Q1_min is needed. The collector current flowing through Q1 is lower when VREF_PRE_REG is set to its maximum, equal to 2 V.

Equation 9

$$\frac{\left(V_{supply} - 2V - V_{BE}(Q1)\right)}{R_2} - \frac{(2V - V_{BE}(Q1) - V_{BE}(Q2))}{R_{gain}} > I_{CE}min(Q1) \quad (9)$$

With

Equation 10

$$R_{gain} \cong K \cdot R_{FB2} = 0.05 \cdot R_{FB2} \quad (10)$$

The pull-down resistor R1 on the base of Q1 is needed to sink the base current of Q1 in all conditions while keeping the drop voltage below the VREF_PRE_REG voltage. This pull-down resistor is in parallel with the biasing resistor in the VREF_PRE_REG output stage (see Figure 2. Wired-OR connection between two or more (O)LED drivers). The maximum base current is expected when VREF_PRE_REG is at minimum voltage. It is to be noted that, the VREF_PRE_REG while the closed loop regulation is active, could drop even below 0.25 V. With 0.1 V as the bare minimum operating voltage for VREF_PRE_REG during closed loop operation, the dimension criteria for R1 becomes:

Equation 11

$$\frac{\left(V_{supply} - V_{BE}(Q1) - 0{,}1V\right)}{h_{FE}(Q1)^{*}R_2} \cdot \frac{R1 \cdot R_{bias}}{(R1 + R_{bias})} < 0{,}1V \quad (11)$$

R_{bias} is typically about 80 kΩ. From the above formula we can conclude as important design criteria to choose a pnp transistor with high gain h_{FE}.

On the other hand, as explained in the previous chapter, the VREF_PRE_REG voltage has an internal serial impedance of about 700 Ω, therefore another condition applies:

Equation 12

$$R1 \gg 700\Omega \quad (12)$$

in order to ensure a small error of VREF_PRE_REG at the base of Q1. A good value for R1 is in the range of 10/22 kΩ.

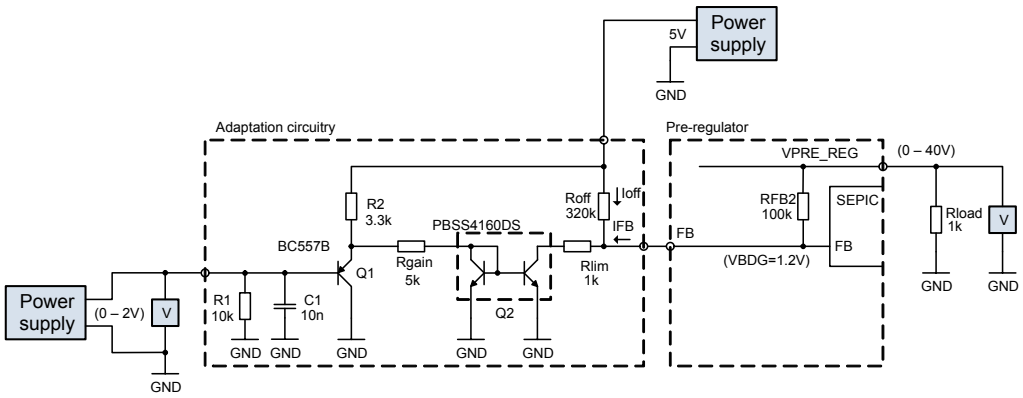
Having defined those values, the VPRE_REG voltage is calculated as

Equation 13

$$V_{PRE\_REG} = V_{REF\_PRE\_REG} \cdot \frac{R_{FB2}}{R_{gain}} + V_{FB} - I_{offset} \cdot R_{FB2} \quad (13)$$

1.2.2.1.1 Application example (2)

Figure 16. Circuit schematic connecting $V_{REF\_PRE\_REG}$ signal(s) to feedback pin



1.2.2.1.2 Experimental circuit verification with SEPIC converter evaluation board

This circuit was used to verify the linearity and possible offset between the VREF_PRE_REG input voltage and the VPRE_REG output voltage. External resistors were calculated according to the Equation 7, Equation 8 and Equation 10 Rlim was dimensioned to limit the maximum VPRE_REG at 20 V. Table 5. V_{PRE_REG} vs $V_{REF\_PRE\_REG}$ measurement reports the difference between the ideal Vout calculated per Equation 13 and Figure 17. VPRE_REG vs VREF_PRE_REG illustrates the results.

Table 5. V_{PRE_REG} vs $V_{REF\_PRE\_REG}$ measurement

VREF_PRE_REG [V]	VPRE_REG [V]	VPRE_REG_IDEAL [V]	Error [V]
0	3.3	0.0	3.3
0.1	4.9	2.0	2.9
0.2	6.6	4.0	2.6
0.3	8.3	6.0	2.3
0.4	10.1	8.0	2.1
0.5	11.8	10.0	1.8
0.6	13.6	12.0	1.6
0.7	15.4	14.0	1.4
0.8	17.1	16.0	1.1
0.9	18.8	18.0	0.8
1	20.3	20.0	0.3
1.1	21.0	20.5	0.5

VREF_PRE_REG [V]	VPRE_REG [V]	VPRE_REG_IDEAL [V]	Error [V]
1.2	21.3	21.0	0.3
1.3	21.5	21.0	0.5
1.4	21.6	21.0	0.6
1.5	21.7	21.0	0.7
1.6	21.8	21.0	0.8
1.7	21.8	21.0	0.8
1.8	21.9	21.0	0.9
1.9	21.9	21.0	0.9
2	22.0	21.0	1.0

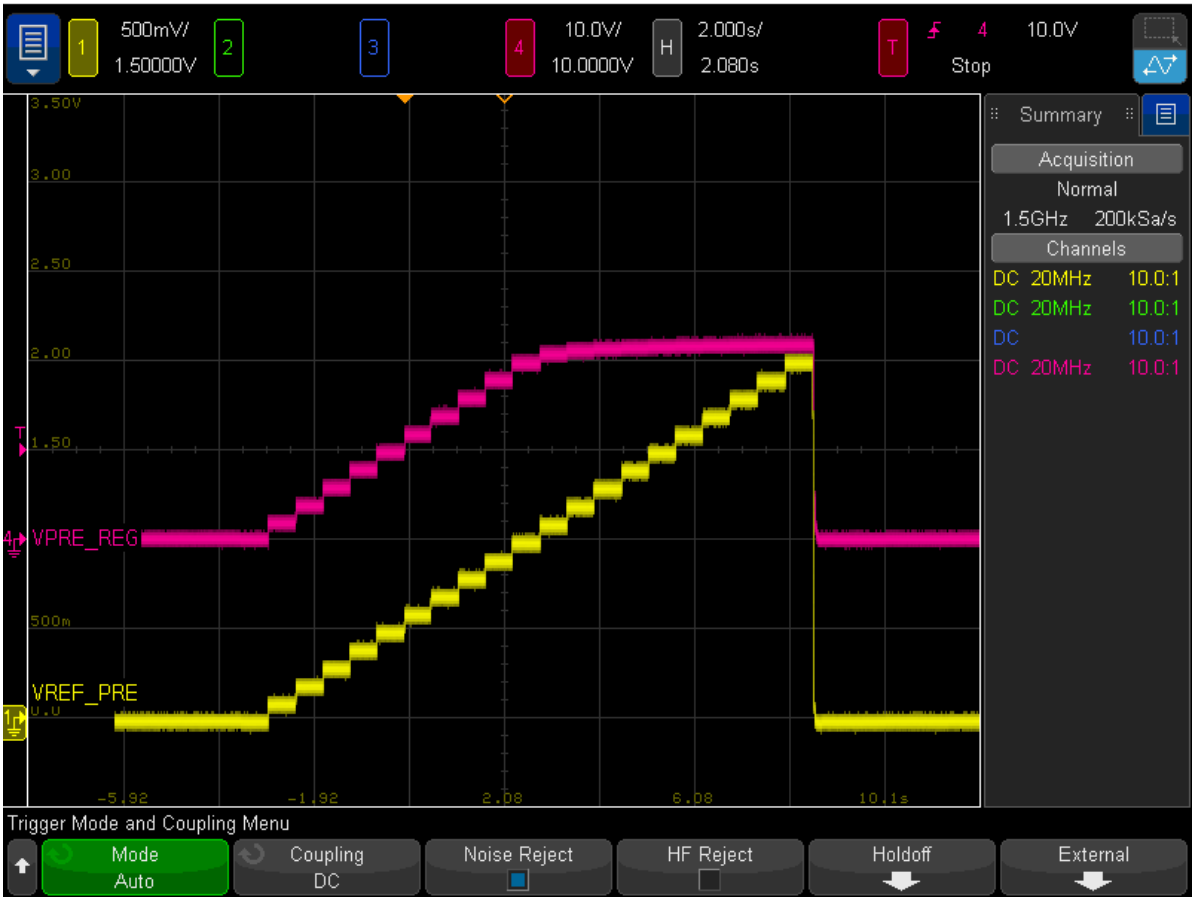
Figure 17. VPRE_REG vs VREF_PRE_REG

There is a certain offset and some nonlinearity vs the ideal characteristics. Besides the known tolerances of the external resistors, the feedback voltage, the supply voltage of the circuit, "hfe" matching error of "npn" current mirror, the major part of the errors comes from the V_{BE} mismatch between Q1 and Q2. Therefore Q1 and Q2 should be selected so to have similar or even identical V_{BE} considering the range of collector operating current. The difference at a certain operating point can be compensated by adapting the external component dimension following the formulas from Equation 7, Equation 8 and Equation 10 as shown in the following table and figure where Rgain has been reduced to 4.5 k and Roff to 76 k. Since the V_{BE} has a non-negligible temperature dependency of ~ 2 mV/K, it is important to position Q1 and Q2 in close proximity on the PCB to ensure identical operating temperature.

Table 6. V_{PRE_REG} vs $V_{REF\_PRE\_REG}$ measurement trimmed circuit

VREF_PRE_REG [V]	VPRE_REG [V]	VPRE_REG_IDEAL [V]	Error [V]
0	0.2	0.0	0.2
0.1	2.0	2.0	0.0
0.2	3.9	4.0	-0.1
0.3	5.9	6.0	-0.1
0.4	7.9	8.0	-0.1
0.5	9.9	10.0	-0.1
0.6	11.9	12.0	-0.1
0.7	14.0	14.0	0.0
0.8	16.0	16.0	0.0
0.9	18.0	18.0	0.0
1	19.9	20.0	-0.1
1.1	20.9	21.0	-0.1
1.2	21.3	21.0	0.3
1.3	21.5	21.0	0.5
1.4	21.6	21.0	0.6
1.5	21.7	21.0	0.7
1.6	21.8	21.0	0.8
1.7	21.8	21.0	0.8
1.8	21.9	21.0	0.9
1.9	21.9	21.0	0.9
2	21.9	21.0	0.9

Figure 18. **VPRE_REG vs VREF_PRE_REG trimmed circuit**



The trimming of the circuit certainly can be applied for experimental trials only, not for volume production. Therefore, the dimensioning of the external components has to be done so that the circuit will work properly in the whole temperature range and across all component tolerances. The boundary conditions to be met are:

- The circuit must guarantee a positive error, this means considering all tolerances, the generated VPRE_REG can only be higher, never lower than the targeted value. This is important to avoid dropouts of the regulated output voltage at channel turn on/off which could lead to a short visible brightness fluctuation.
- The maximum positive error must be limited in order to guarantee at the lowest regulated output voltage a regulated VREF_PRE_REG which stays always above the voltage drop across R1, Q1 base resistor

A calculator tool is available to facilitate the component dimensioning task considering worst case tolerances.

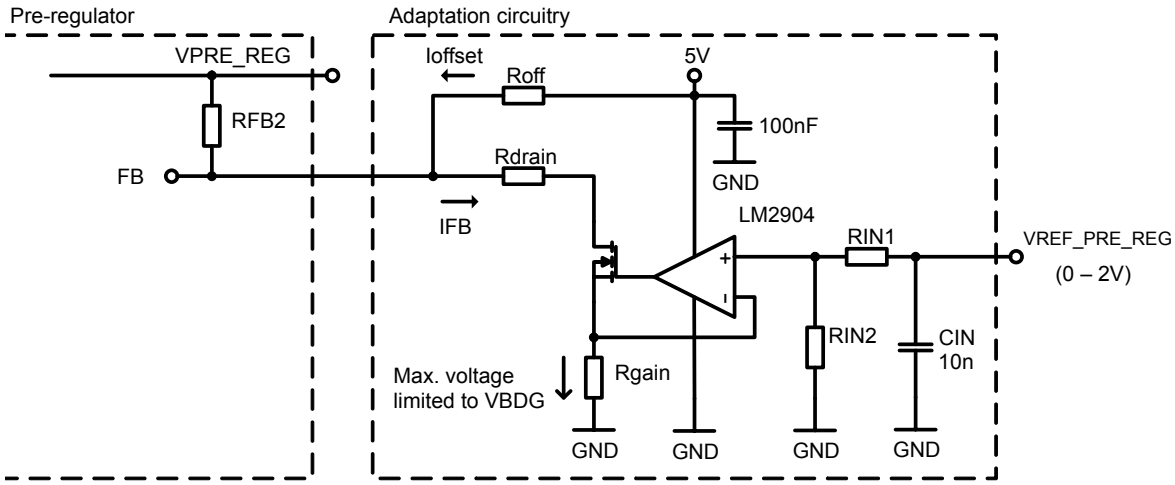
1.2.2.1.3 Further design and layout recommendations

- The NPN current mirror circuitry must be as close as possible to pre-regulator, to minimize the Feedback pin connection length, as it is the most sensitive point of the regulator. This signal should not be filtered otherwise it degrades the regulation loop performance
- The whole circuitry should be close to the SEPIC (distance between PNP and NPN current mirror should be minimized)
- The RFB2 resistor value should be maximum 100 kΩ. With higher value the current mirror will operate at very low current levels so it becomes more sensitive to noise and eventual leakage currents
- The 10 nF on PNP input is mandatory. Without this capacitor the VREF_PRE_REG signal is quite noisy. In case of longer distance the VREF_PRE_REG connection (>10 cm), it is possible place close to the device VREF_PRE_REG output, additional 10 nF capacitor.

1.2.2.2 *Circuit schematics with OpAmp*

Of course, the same circuit as proposed for the open loop control regulation can be used also when closed loop regulation is selected. This circuit has the advantage of lower tolerances and therefore higher precision (see Section 1.2.1). The component dimensioning requirements are less critical than for the BJT circuit, but still important.

Figure 19. Circuit schematics connecting $V_{REF\_PRE\_REG}$ signal to feedback pin



The same boundary conditions to be met are:

- The circuit must guarantee a positive error, this means considering all tolerances, the generated VPRE_REG can only be higher, never lower than the targeted value. This is important to avoid dropouts of the regulated output voltage at channel turn on/off which could lead to a short visible brightness fluctuation.
- The maximum positive error must be limited to guarantee at the lowest regulated output voltage a regulated VREF_PRE_REG which stays always above 100 mV

1.2.2.2.1 Application example (3)

Figure 20. Calculation of resistor dimensioning for application example

VOFFSUPPLY	5	V	Offset resistor supply voltage (for Roff calculation)
VBDG	1,2	V	Reference voltage of external preregulator
VPRE_REG max.	20	V	Maximum output voltage of the pre-regulator (for Rdrain calculation)
K	0,05	-	K factor (0.1 for L99LDLL16, 0.05 for L99LDLH32)
RFB2	43	kohm	Upper resistor of feedback divider
RIN1	27	kohm	Upper resistor of control voltage divider
RIN2	33	kohm	Lower resistor of control voltage divider
Vref_pre impedance	0,7	kohm	Internal resistance of Vref_pre output
RIN_ratio	0,543657331	-	Control voltage divider ratio (out/in)
Rgain	1,168863262	kohm	Current sink shunt resistor
Roff	136,1666667	kohm	Offset current definition resistor
Rdrain	1,411136738	kohm	Maximum VPRE_REG voltage definition resistor

As it can be seen from the above calculation example, the offset resistor calculation results in a quite high number. As it often happens in automotive design, resistors higher than 100 k are not tolerated in circuit schematics. Therefore the offset resistor can be even skipped producing a small error.

Without this resistor, the SEPIC output voltage will be shifted by V_{FB} higher. A positive shift is anyway required, as previously discussed. All these calculations are available in a separate calculator:

Figure 21. Tolerances for worst case calculation

Vref pre reg Impedance	40	% tolerance
RFB2	1	% tolerance
Bandgap	1	% tolerance
Voff_supply	3	% tolerance
Roff	1	% tolerance
Rgain	1	% tolerance
Rdrain	1	% tolerance
RIN1	1	% tolerance
RIN2	1	% tolerance
K	7	% tolerance
OpAmp offset	2	mV

Figure 22. Worst case SEPIC output voltage spread considering all tolerances

Vout (OLED)	4	V															
	min		typ		max												
Vref_pre (floating)	0,252	V	0,271	V	0,289	V		Vref_pre (floating)=(Vout+1.41)*k									
V_Rgain	0,133	V	0,147	V	0,162	V		V_Rgain=Vref_pre*RIN2/(Vref_resistance+RIN1+RIN2)									
IFB	0,120	mA	0,134	mA	0,148	mA		IFB=V_Rgain/Rgain									
Ioffset	0,000	mA	0,000	mA	0,000	mA		Ioffset=(Voff_supply-Vbdg)/Roff									
Vpre_reg	6,28	V	6,95	V	7,65	V		Vpre_reg=(IFB-Ioffset)*RFB2+VBDG									
Vpre_reg_max	20,45	V	21,05	V	21,66	V		Vpre_reg_max=(VBDG/(Rgain+Rdrain)-(VOFFSUPPLY-VBDG)/Roff)*RFB_2+VBDG									
	Vref_pre (floating) [V]			Vpre_reg [V]				Vpre_reg - Vout [V]			V_Rgain [V]			IFB [mA]		
Vout (OLED) [V]	min	typ	max	min	typ	max		min	typ	max	min	typ	max	min	typ	max	
4	0,252	0,271	0,289	6,28	6,95	7,65		2,28	2,95	3,65	0,132905	0,147059	0,161505	0,11963	0,13369	0,148306	
5	0,298	0,321	0,343	7,24	8,01	8,83		2,24	3,01	3,83	0,157845	0,174424	0,190988	0,142075	0,158402	0,17533	
6	0,345	0,371	0,396	8,19	9,07	10,00		2,19	3,07	4,00	0,182781	0,201425	0,220472	0,164521	0,183114	0,202454	
7	0,391	0,421	0,450	9,15	10,14	11,18		2,15	3,14	4,18	0,207715	0,228608	0,249953	0,186966	0,207825	0,22952	
8	0,438	0,471	0,503	10,10	11,20	12,36		2,10	3,20	4,36	0,232654	0,255791	0,279439	0,209411	0,232537	0,256601	
9	0,484	0,521	0,557	11,06	12,26	13,53		2,06	3,26	4,53	0,257593	0,282974	0,308923	0,231857	0,257249	0,283673	
10	0,531	0,571	0,610	12,01	13,32	14,71		2,01	3,32	4,71	0,28253	0,310157	0,338405	0,254302	0,28196	0,310745	
11	0,577	0,621	0,664	12,97	14,39	15,88		1,97	3,39	4,88	0,307467	0,337335	0,367885	0,276748	0,306672	0,337823	
12	0,624	0,671	0,717	13,92	15,45	17,06		1,92	3,45	5,06	0,332404	0,364524	0,397374	0,299193	0,331384	0,364896	
13	0,670	0,721	0,771	14,88	16,51	18,24		1,88	3,51	5,24	0,357341	0,391705	0,426856	0,321639	0,356096	0,39197	
14	0,717	0,771	0,824	15,84	17,57	19,41		1,84	3,57	5,41	0,382277	0,418888	0,456339	0,344084	0,380807	0,419044	
15	0,763	0,821	0,878	16,79	18,64	20,59		1,79	3,64	5,59	0,407214	0,446071	0,485824	0,366529	0,405519	0,446118	
16	0,810	0,871	0,931	17,75	19,70	21,76		1,75	3,70	5,76	0,432151	0,473254	0,515306	0,388975	0,430231	0,473193	
17	0,856	0,921	0,985	18,70	20,76	22,94		1,70	3,76	5,94	0,457088	0,500437	0,544789	0,41142	0,454943	0,500267	
18	0,903	0,971	1,038	19,66	21,83	24,11		1,66	3,83	6,11	0,482025	0,527619	0,574272	0,433866	0,479654	0,527339	
19	0,949	1,021	1,092	20,61	22,89	25,29		1,61	3,89	6,29	0,506962	0,554802	0,603756	0,456311	0,504366	0,554413	
20	0,996	1,071	1,145	21,57	23,95	26,47		1,57	3,95	6,47	0,531899	0,581985	0,633239	0,478757	0,529077	0,581487	
lowest Vref	0,183	V															

As seen in Figure 22, the resistor values are calculated so that the worst case minimum SEPIC output voltage is always > 1.4 V above V_{OUT} (OLED), to fulfill the first boundary design condition. The lowest possible VREF_PRE_REG voltage was calculated and confirmed to match with the requirements of the second boundary design condition. The dimensioning of the circuit can therefore be considered as robust against all considered tolerances and temperature variations.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
12-Oct-2021	1	Initial release.
04-Apr-2022	2	Confidentiality level changed from confidential data to public.

Contents