

# L9679E Cut-off Battery and Pyro Fuse

### Introduction

This document explains the features and benefits of the L9679E device in order to be used in the Pyro Fuse application: the device activates the Pyro Fuse that disconnects a battery from an electrical system, so that the battery will not become a source of ignition.

The main features are the flexible configuration, four PSI-5 sensor interfaces, high or low level diagnostic test, arming procedure following external safing engine, deployment profile selectable, 32 bits SPI communication.

Note

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.



# 1 Description

The L9679E is a chip solution targeted for cut-off battery market. This device is family compatible with the L9678, L9680 and L9679P devices: it has been designed as extension chip of the others, but if configured in the right way it can be used standalone.

#### 1.1 Main features

The main features are:

- System voltage diagnostics with integrated ADC Squib deployment drivers
  - 8 channel HSD/LSD
  - 25 V max deployment voltage
  - Various deployment profiles, 1.2 A/1.75 A, x \* 0.064 ms up to 4.032 ms
  - Current monitoring
  - R<sub>measure</sub>, STB, STG and Leakage diagnostics
  - High and Low Side driver FET tests
- Four-channel remote sensor interface for PSI-5 (synchronous mode)
- User customizable external safing logic
- Temperature sensor
- 32 bits SPI communications
- Operating temperature, -40 °C to 105 °C
- Packaging: 48 pins

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# 1.2 Application overview

The device has been designed for Airbag Application, but if correctly configured it can be used also for Pyro Fuse Application, i.e. to cut-off the battery from an electrical system.

In fact, in case of a crash, a short circuit on the battery due to damaged cables can lead to sparks and dangerous ignition or heat and moldering fires. Thus it is important to disconnect the electrical system from the battery using pyrotechnical safety battery terminals.

Pyro Fuse application circuit

These special Pyro Fuses have electrical characteristic like those of Airbag detonators. Some Pyro Fuses can require a bigger current to be triggered. In this case some deployment channels can be shorted and connected to the same load in order to obtain a total current higher than 2 A.

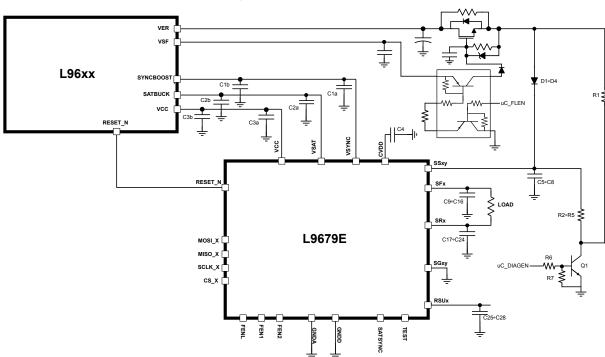


Figure 1. Application circuit

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# 2 Device configuration

The user shall configure the device following the Application Note AN5023, in particular for:

- Voltage Regulators
- Safing Logic
- Deployment
- Remote Sensor Interface (PSI-5 sensors)

Furthermore, the user could use the same document to know about:

- System Voltage Diagnostic
- Temperature Sensor

In the following section a deployment example will be shown.

### 2.1 Unused functions

In case some functions are not used, the correspondent pins have to be managed as in the Table 1.

Table 1. Unused functions management

| Pin                    | Action                         |
|------------------------|--------------------------------|
| RSU0, RSU1, RSU2, RSU3 | Open (by default they are off) |
| SATSYNC                | Connected to GND               |
| FENL                   | Connected to GND               |

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# 3 Deployment

The device main features are:

- 8 independent loops composed by 8 independent High Side and 8 independent Low Side.
- Dedicated ground connection for a couple of loops, SGxy.
- In case the Low Side SRx is shorted to ground, the deployment, if requested, is guaranteed to succeed.
- In any case, SSxy voltage has to be lower than 25 V.
- Both High Side and Low Side are equipped with a passive turn-off to guarantee that they are always in off state except when the deployment has to take place.

### 3.1 Deployment requirement

Deployment features are deployment current, deployment time and deployment expiration time. The deployment expiration time is the duration time in which the deploy command remains valid, once it is received, waiting for the arming signal.

These parameters are defined through the twelve registers DCR\_x, with x = 0-7, configurable in DIAG, SAFING and ARMING state and shown in the Table 2:

- \$06 DCR\_0 → channel 0
- \$07 DCR 1 → channel 1
- \$08 DCR 2 → channel 2
- \$09 DCR 3 → channel 3
- \$0A DCR\_4 → channel 4
- \$0B DCR\_5  $\rightarrow$  channel 5
- \$0C DCR 6 → channel 6
- \$0D DCR 7 → channel 7

All deployment configuration registers are reset by SSM reset.

(1) (2) 19:16 15:12 11:6 5:4 3:2 1:0 Deploy\_expire\_time Deploy current 00, 500 ms \$06 DCR\_0 00, 11 not used Deploy\_time W **(l)** 0 Х 01, 250 ms Х \$0D DCR\_7 = 0.064ms/count\*depl time ≤ 4.032ms 01, 1.75 A min 10. 125 ms 10, 1.2 A min 11, 0 ms

Table 2. DCR\_x register

The Deploy Time field allows the device to deploy for a maximum configurable time of 4.032 ms ( $64 \mu \text{s}$  step). Differently from the L9678, there is no inhibition of the combinations current/deployment time, so it is under user's responsibility to prevent excessive thermal heating in the squib driver section by setting the deploy parameters carefully.

For this reason, it is recommended to keep the SSxy voltage in the range as specified in the Table 3:

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<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

<sup>2.</sup> R = READ, W = WRITE



| Table 3. Relationshi | p between deploy | y current profile and SSxy | / voltage |
|----------------------|------------------|----------------------------|-----------|
|                      |                  |                            |           |

| Deploy Current Profile | DCR_Deploy_Time | Temperature range                | SSxy voltage         |
|------------------------|-----------------|----------------------------------|----------------------|
| 1.2 A/2 ms             | ≤ 34            | -40 °C ≤ T <sub>j</sub> ≤ 130 °C | 6 V ≤ SSxy ≤ 22.75 V |
| 1.2 A/2 IIIS           | ≥ 34            | -40 °C ≤ T <sub>j</sub> ≤ 150 °C | 6 V ≤ SSxy ≤ 21.5 V  |
| 1.2 A/3.2 ms           | ≤ 54            | -40 °C ≤ T <sub>j</sub> ≤ 130 °C | 6 V ≤ SSxy ≤ 20.1 V  |
| 1.2 A/3.2 IIIS         | ≥ 54            | -40 °C ≤ T <sub>j</sub> ≤ 150 °C | 6 V ≤ SSxy ≤ 19.3 V  |
| 1.75 A/0.5 ms          | ≤ 10            | -40 °C ≤ T <sub>j</sub> ≤ 150 °C | 9 V ≤ SSxy ≤ 25 V    |
| 1.75 A/0.7 ms          | ≤ 13            | -40 °C ≤ T <sub>j</sub> ≤ 130 °C | 9 V ≤ SSxy ≤ 23.75 V |
| 1.75 AVO.7 IIIS        | ≥ 13            | -40 °C ≤ T <sub>j</sub> ≤ 150 °C | 9 V ≤ SSxy ≤ 22.5 V  |
| 1.75 A/2 ms            | ≤ 34            | -40 °C ≤ T <sub>j</sub> ≤ 130 °C | 6 V ≤ SSxy ≤ 16.7 V  |
| 1.75 AVZ 1115          | ≥ 34            | -40 °C ≤ T <sub>j</sub> ≤ 150 °C | 6 V ≤ SSxy ≤ 16 V    |
| 1.2 A/3.2 ms           | ≤ 54            | -40 °C ≤ T <sub>j</sub> ≤ 130 °C | 6 V ≤ SSxy ≤ 14.7 V  |
| 1.2 7/3.2 1115         | = 54            | -40 °C ≤ T <sub>j</sub> ≤ 150 °C | 6 V ≤ SSxy ≤ 13.9 V  |

The parameters in each DCR\_x register have to be confirmed at least the first time the device has to deploy, even in case they are left at their default value; the deployment does not occur otherwise.

The status of each loop is monitored in the deployment status register DSR\_x, one for each channel (see the Table 4).

Table 4. DSR\_x register

|                          | (1) | (2) | 19:16 | 15   | 14  | 13 | 12  | 11:6 | 5:0                            |
|--------------------------|-----|-----|-------|--|---|----|---|------|--------------------------------|
| \$13 DSR_0<br>\$1A DSR_7 |     | R   | 0     | CHxDSX 0 depl not succesful 1 depl succesful | CHxSTAT 0 depl not in progress 1 depl in progress | 0  | DCRxERR  0 depl conf accepted and stored  1 depl conf change not accepted because deploy is in progress | 0    | DEP_CHx_EXP_TIME<br>8 ms/count |

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- 2. R = READ, W = WRITE

Once deploy parameters have been set, it is required to assign the arming signals to deployment loops. This allows deploying different channels basing on the arming result.

The arming valid condition is assessed by using the 3 arming discrete input pins FEN1, FEN2 and FENL, that are active high.

The device allows two configurations:

- Config 1 (default): FENL is not used; FEN1 and FEN2 are enablers for any or all the loops, each input controlling both HS and LS of those loops.
- Config 2: FENL is used and enables all LSs; FEN1 and FEN2 enable for any or all the loops, controlling only HSs.

FEN1/2 input pins are assigned to the desired channels by means of the programmable loop matrix defined in the \$6E LOOP\_MATR\_ARM1 and \$6F LOOP\_MATR\_ARM2 registers (see the Table 5).

Table 5. LOOP\_MATR\_ARMx registers

|     |     | 19:16 | 15:8 | 7         | 6         | 5         | 4        | 3        | 2         | 1         | 0         |
|-----|-----|-------|------|-----------|-----------|-----------|----------|----------|-----------|-----------|-----------|
| MC  | OSI | -     | Х    | FENx L7   | FENx L6   | FENx L5   | FENx L4  | EENv I 2 | FENx L2   | FENx L1   | FENx L0   |
| MIS | so  | 0     | 0    | I LINX_L/ | I LINX_LO | I LINX_L3 | FEINX_L4 | FENx_L3  | I LINX_LZ | I LINA_LI | I LIVA_LU |

Once fixed the deploy parameters, in order to satisfy a deploy request, the IC has to move in SAFING state.

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SAFING state is driven by specific SPI command (see the Table 6).

Once sent the command to move into the SAFING state, the verification of the IC's status is readable into the \$04 SYS\_STATE register.

Table 6. SPI commands to pass in SAFING state

|                   | (1) | (2) | 19:16 | 15:0                           |
|-------------------|-----|-----|-------|--------------------------------|
| \$31 SAFING STATE | D   | W   | 0     | \$ACAC<br>SAFING state command |

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- 2. R = READ, W = WRITE

In order to be able to deploy, the arming signals have to be serviced. Their state is readable in the \$6A ARM\_STATE register (see the Table 7).

Table 7. ARM\_STATE register

|      | 19:16 | 15:4 | 3    | 2    | 1    | 0 |
|------|-------|------|------|------|------|---|
| MOSI | -     | X    | Х    | X    | X    | X |
| MISO | 0     | 0    | FEN2 | FEN1 | FENL | 0 |

Deployment has to be enabled via SPI, writing DEPEN\_WR bits in the \$25 SPIDEPEN register (see the Table 8).

**Table 8. SPIDEPEN register** 

|               | (1)  | (2) | 19:16 | 15:0                             |  |  |
|---------------|------|-----|-------|----------------------------------|--|--|
|               |      |     |       | DEPEN_WR[15:0]/DEPEN_STATE[15:0] |  |  |
| \$13 SPIDEPEN | S, A | W/R | -     | \$0FF0 - DEP DISABLED            |  |  |
|               |      |     |       | \$F00F - DEP ENABLED             |  |  |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE

Deployment command request has to be received by the IC via the \$12 DEPCOM register (see the Table 9).

Once the deployment command has been received, the deploy time is elapsed, deploy success bit is set (CHxDSX bit) and deployment enable toggles into the DEP DISABLED.

The next deploy requires the DEPEN reconfigured again as ENABLED. This feature has to be considered in case of multiple deployment, after each of them, before the next deployment the correspondent bit DEPEN has to be set again.

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| Table 9. | DEPCOM | register |
|----------|--------|----------|
|----------|--------|----------|

|                       | (1) | (2) | 19:17 | 16 | 15:12 | 11  | 10 | 9         | 8         | 7         | 6          | 5            | 4            | 3           | 2         | 1       | 0      |
|-----------------------|-----|-----|-------|----|-------|---|----|-----------|-----------|-----------|------------|--------------|--------------|-------------|-----------|---------|--------|
| \$12 S,<br>DEPCOM A W | -   |     | 0     | x  | X     | X   | X  | CH7DEPREQ | CH6DEPREQ | CH5DEPREQ | CH4DEPREQ  | CH3DEPREQ    | CH2DEPREQ    | CH1DEPREQ   | CHODEPREQ |         |        |
|                       |     |     |       |    |       | 0 no change to dep ch x                           |    |           |           |           |            |              |              |             |           |         |        |
|                       |     |     |       |    |       |   |    |           | 1 if      | in ARMING | or SAFING  | G, clear and | d start expi | ration time | and DEPL  | OY_ENAB |        |
| \$12<br>DEDCOM        | _   | R   | _     |    | 0     | X   | X  | X         | X         | CH7DEP    | СН6DEP     | СН5DEP       | CH4DEP       | СНЗDEР      | CH2DEP    | CH1DEP  | СНОБЕР |
| DEPCOM                |     |     |       |    |       |   |    |           |           |           | 1 expirati | on timer er  | nabled, DEI  | PCOM still  | valid     |         |        |
|                       |     |     |       |    |       | 0 expiration timer disabled, DEPCOM no more valid |    |           |           |           |            |              |              |             |           |         |        |
| \$25                  | S,  | W/  |       |    |       | DEPEN_STATE[15:0]                                 |    |           |           |           |            |              |              |             |           |         |        |
| SPIDEPEN              | Α   | R   |       | _  |       | \$0FF0 - DEP DISABLED                             |    |           |           |           |            |              |              |             |           |         |        |

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Deployment status of each channel is readable in the DSR x registers (see the Table 4).

Each High Side (SFx) has a current comparator to indicate when the current flowing through is greater than the deployment current threshold (ITHDEPL = 90% IDEPLx). For each channel there is a timer (Current\_Mon\_Timer) that measures, with  $16~\mu s$  resolution, how long the current is at high level to let the microcontroller identifies if the deployment has been effective or not.

During a deploy event, if the current falls momentarily below the threshold, the timer stops (timer pause), and continues to count as the current turns high (see the Figure 2).

Current\_Mon\_Timer is refreshed upon read or when a new DEPCOM command on the channel is received. For this reason, the microcontroller reads the data in the DCMTSxy registers (see the Table 10) after the deployment event and before a new deployment command. The current measurement stops at the end of the deployment time.

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<sup>2.</sup> R = READ, W = WRITE

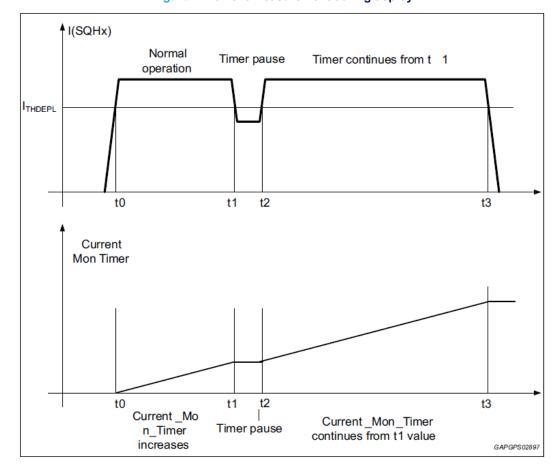


Figure 2. Current measurement during deploy

Table 10. DCMTSxy registers

|              | (1)          | (2) | 19:16 | 15:8  | 7:0                  |  |  |
|--------------|--------------|-----|-------|---|----------------------|--|--|
| ¢1E DOMTS01  | \$1F DCMTS01 |     |       | CURRENT MONITOR TIME  | CURRENT MONITOR TIME |  |  |
| \$22 DCMTS67 |              | R   | 0     | CH 1, 3, 5, 7   | CH 0, 2, 4, 6        |  |  |
|              |              |     |       | 16 μs increment while Deploy_curr > monitor threshold channel per channel |                      |  |  |

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- 2. R = READ, W = WRITE

Once the deployment is started, it can be interrupted by:

- Over-current in the Low Side.
- GND loss.
- SSM reset.
- · End of deployment time.

Successful deploy event is reported in the DEPOK bit of GSW (see the Table 11 and the Table 12). Such a flag is the "OR" of the eventual deployment success of all the eight channels.

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| Table 11. | Global | Status | Word - | <b>GSW</b> |
|-----------|--------|--------|--------|------------|
|-----------|--------|--------|--------|------------|

| MISO<br>BIT | 31     | 30    | 29         | 28         | 27         | 26       | 25  | 24       | 23       | 22      | 21      |
|-------------|--------|-------|------------|------------|------------|----------|-----|----------|----------|---------|---------|
| MISO        | SPIFLT | DEPOK | 0 (unused) | 0 (unused) | 0 (unused) | POWERFLT | FLT | CONVRDY2 | CONVRDY1 | ERR_WID | ERR_RID |
| GSW<br>BIT  | 10     | 9     | 8          | 7          | 6          | 5        | 4   | 3        | 2        | 1       | 0       |

Table 12. DEPOK in GSW

| GSW | MISO b[30] DEPOK = GSW b[9]  |
|-----|--|
|     | 0 = all DSR_x/CHxDS bit are = 0 (no deployment success on all channel) |
| -   | 1 = at least a deployment successfull on the channels                  |

In case the deploy success is equal to 1, this does not mean that the current is really passed through the squib for the programmed time. This bit means only that no inhibition of deployment has happened. The real evaluation about the deployment is through the channel current monitor time, i.e. DCMTS01÷DCMTS67 registers.

In case of a short to ground of the Low Side during the deployment, the current is limited by the High Side avoiding the device's damage. The same protection is available if an open load condition happens, followed by a short to ground of the Low Side.

## 3.2 Deployment driver protection

In order to avoid damaging the IC due to eventual free-wheeling, two protections are implemented:

- After a deployment, once the High Side is switched off, the Low Side is kept on for t<sub>DEL\_SD\_LS</sub> (50 μs min.) in order to allow fly-back.
- Once Low Side is switched off, a protection against the overvoltage through a clamp structure is implemented.

On the Low Side there is a current limitation and overcurrent protection circuit that attends limiting the current at  $I_{LIM\_SR}$  (2.2 A ÷ 4 A) and  $I_{OC\_SR}$  (2.2 A ÷ 4 A) respectively, avoiding, in case of pin short to battery, any damage. If the malfunction lasts over  $t_{FLT\_ILIM\_LS}$  (100  $\mu$ s typ), the whole channel (High and Low Side) is switched off until a new deployment command (via SPI\_DEPEN register) occurs.

The squib driver can stand the short to ground of the pins during the deployment, because the High Side current is limited by the High Side itself.

It can also manage the case of SRx short to ground after an open circuit, because it is able to detect the open circuit condition and then limiting the current overshoot as the open circuit disappears.

In case of squib's intermittence during deployment phase, current limitation is ensured by the Low Side current limitation,  $I_{LIM\_SR}$ . If the condition lasts longer than  $t_{FLT\_OS\_LS}$  (20  $\mu s$  max), the High Side is switched off for  $t_{OFF\_OS\_HS}$  (4  $\mu s$  ÷ 12  $\mu s$ ) and then on again.

This allows distinguish Open Load and Low Side short to battery cases and then properly manage them.

## 3.3 Deployment driver example

Since the FENL pin is used (FENL\_ACT = 1 in SYS\_CFG register), it is connected to 5 V (high level). Since all the deployment loops will be associated to FEN1, the FEN1 pin is pulled high.

The L9679E is the extension chip of the L96xx family, so the external Safing FET is driven by the main chip. In low cost application, where the L9679E is used standalone, it could be removed. In this case the application has a lower Safety level. To be sure not to damage the High Side MOSFETs it is suggested to set the SSxy source below 25 V.

The Table 13 reports a simple example showing the minimum SPI frames needed to configure the device and enable the deployment on all the channels.

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Table 13. Deployment SPI sequence

| Bit 15: 0 = Auto switch off disabled     Bit 14-11: X = Don't care     Bit 10: 0 = Short time     Bit 9: 0 = Long sync pulses shift duration     Bit 8: 0 = Long sync pulses shift duration     Bit 9: 0 = Long sync pulses shift duration     Bit 8: 0 = Long sync pulses shift duration     Bit 9: 0 = Long sync pulses shift duration     Bit 9: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit 14: 0 = Long sync pulses shift duration     Bit       | Register                | State | R/W | Data   | Notes   |
|--|-------------------------|-------|-----|--------|---|
| Bit 10: 0 = Short time   Bit 9: 0 = Long sync pulses shift duration   Bit 9: 0 = Long sync pulses shift duration   Bit 9: 0 = Long sync pulses shift duration   Bit 9: 0 = Long sync pulses shift duration   Bit 8: 4: X = Don't care   Bit 4: X = Don't care   Bit 4: X = Don't care   Bit 2: 0 X = Don't care   Bit 2: 0 X = Don't care   Bit 10: 0 = Short limit   W   0x3CC3   Frame to pass from Init to Diag   Part 10: 1 = The Point   Part 10: 1 =       |                         |       |     |        | Bit 15: 0 = Auto switch off disabled          |
| S01 SYS_CFG  |                         |       |     |        | Bit 14-11: X = Don't care                     |
| \$01 SYS_CFG   |                         |       |     |        | Bit 10: 0 = Short time                        |
| Bits 6-5: 00 = 4 sample other measure   Bit 4: X = Don't care   Bit 3: 1 = FENL enabled   Bit 2-0: X = Don't care   Bit 3: 1 = FENL enabled   Bit 2-0: X = Don't care   Bit 3: 1 = FENL enabled   Bit 2-0: X = Don't care   Bit 3: 1 = FENL enabled   Bit 2-0: X = Don't care   Bit 3: 1 = FENL enabled   Bit 2-0: X = Don't care   Bit 10-8: 001 = DIAG   |                         |       |     |        | Bit 9: 0 = Long sync pulses shift duration    |
| Bit 4: X = Don't care  | \$01 SYS_CFG            | Init  | W   | 0x0008 | Bits 8-7: 00 = 8 sample DC-squib-temp measure |
| Bit 3: 1 = FENL enabled   Bit 2-0: X = Don't care  |                         |       |     |        | Bits 6-5: 00 = 4 sample other measure         |
| Bit 2-0: X = Don't care  |                         |       |     |        | Bit 4: X = Don't care                         |
| \$04 SYS_STATE   |                         |       |     |        | Bit 3: 1 = FENL enabled                       |
| \$35 DIAG_STATE  |                         |       |     |        | Bit 2-0: X = Don't care                       |
| \$04 SYS_STATE   | \$04 SYS_STATE          | Init  | R   | -      | Bits 10÷8: 000 = INIT                         |
| Bit 15: X = Don't care   Bit 14: 0 = 1 mA squib pull down current, 450 μA VRCM leakage to GND threshold   Bit 13: X = Don't care   Bit 14: 0 = 1 mA squib pull down current, 450 μA VRCM leakage to GND threshold   Bit 13: X = Don't care   Bit 12: 0 = VSAT th set to 6.5 V   Bit 11+0: X = Don't care   Bit 15: 0 = VSAT > VSAT_OK  | \$35 DIAG_STATE         | Init  | W   | 0x3CC3 | Frame to pass from Init to Diag               |
| Sit 14: 0 = 1 mA squib pull down current, 450 μA VRCM leakage to GND threshold   | \$04 SYS_STATE          | Diag  | R   | -      | Bits 10÷8: 001 = DIAG                         |
| \$02 SYS_CTL  Diag  W  0x0000  Bit 13: X = Don't care Bit 12: 0 = VSAT th set to 6.5 V Bit 11+0: X = Don't care  Bit 12: 0 = VSAT_OK Bit 11+0: X = Don't care  Bit 15: 0 = VSAT_OK Bit 14: 0 = VSYNC > VSYNC_OK Bit 13-0: X = Don't care  \$00 FLTSR  Diag  R  Verify there are not faults Bits 15+8: X = Don't care Bits 15+12: X = |                         |       |     |        | Bit 15: X = Don't care                        |
| Bit 12: 0 = VSAT th set to 6.5 V   |                         |       |     |        |   |
| Bit 11+0: X = Don't care   | \$02 SYS_CTL            | Diag  | W   | 0x0000 | Bit 13: X = Don't care                        |
| \$05 POWER STATE  Diag  R  Bit 15: 0 = VSAT > VSAT_OK  Bit 14: 0 = VSYNC > VSYNC_OK  Bit 13-0: X = Don't care  \$00 FLTSR  Diag  Diag  Vox0FF  Bits 15+8: X = Don't care  Bits 15+8: X = Don't care  Bits 7+0: 1 = FEN1 assigned to 0+7 loops  Bits 15+12: X = Don't care  Bits 15+12: Don't care  Bits 15+12: Don't care  Bits 15+12: Don't care  B |                         |       |     |        | Bit 12: 0 = VSAT th set to 6.5 V              |
| \$05 POWER STATE  Diag  R  Bit 14: 0 = VSYNC > VSYNC_OK Bit 13-0: X = Don't care  \$00 FLTSR  Diag  R  Verify there are not faults  Bits 15+8: X = Don't care Bits 7+0: 1 = FEN1 assigned to 0+7 loops  Bits 15+12: X = Don't care Bits 15+12: X = Don't care Bits 15+12: X = Don't care Bits 11+6: 0x1001 = 576 µs (9*64 µs step)  Bits 15+2: 00 = 500 ms deploy expiration time Bits 1+0: X = Don't care  Bits 15+0: X = Don't care  Bits 15+0: X = Don't care  Bits 15+0: 00 = 500 ms deploy expiration time Bits 1+0: 00 = 500 ms deploy expiration time Bits 1+0: 00 = 600 print to the print  |                         |       |     |        | Bit 11÷0: X = Don't care                      |
| Bit 13-0: X = Don't care  \$00 FLTSR Diag R - Verify there are not faults  \$6E LOOP_MATRIX_ARM1 Diag W 0x00FF Bits 15+8: X = Don't care Bits 7+0: 1 = FEN1 assigned to 0+7 loops  Bits 15+12: X = Don't care Bits 15+12: X = Don't care Bits 15+12: X = Don't care Bits 11+6: 0x1001 = 576 µs (9*64 µs step)  Bits 3+2: 00 = 500 ms deploy current Bits 3+2: 00 = 500 ms deploy expiration time Bits 1+0: X = Don't care  Bit 15: 0 = deployment not successful Bit 14: 0 = deployment not in progress Bit 12: 0 = deployment configuration accepted Bits 5+0: deployment expiration timer value  \$31 SAFING_STATE Diag V 0xACAC Frame to pass from Diag to Safing \$04 SYS_STATE S R Bits 10+8: 010 = SAFING \$25 SPIDEPEN S, A W 0x00FF Unlock Code \$12 DEPCOM S, A W 0x00FF Bits 7+0: 0xFF = deploy requests for all channels \$25 SPIDEPEN S, A W 0x0FFO Lock Code  |                         |       |     |        | Bit 15: 0 = VSAT > VSAT_OK                    |
| \$00 FLTSR Diag R - Verify there are not faults  \$6E LOOP_MATRIX_ARM1 Diag W 0x00FF  Bits 15+8: X = Don't care  Bits 7+0: 1 = FEN1 assigned to 0+7 loops  Bits 15+12: X = Don't care  Bits 11+6: 0x1001 = 576 µs (9*64 µs step)  Bits 3+2: 00 = 500 ms deploy expiration time  Bits 1+0: X = Don't care  Bits 15+0: X = Don't care  Bits 1+0: X = Don't care  Bits 1+0: X = Don't care  Bit 15: 0 = deployment not successful  Bit 14: 0 = deployment not in progress  Bit 12: 0 = deployment configuration accepted  Bit 2: 0 = deployment expiration timer value  \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10+8: 010 = SAFING  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$12 DEPCOM S, A W 0x00FF Bits 7+0: 0xFF = deploy requests for all channels  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  | \$05 POWER STATE        | Diag  | R   | -      | Bit 14: 0 = VSYNC > VSYNC_OK                  |
| \$6E LOOP_MATRIX_ARM1 Diag W 0x00FF  Bits 15+8: X = Don't care Bits 7+0: 1 = FEN1 assigned to 0+7 loops  Bits 15+12: X = Don't care Bits 11+6: 0x1001 = 576 µs (9*64 µs step)  \$06 DCR_0 + \$0D DCR_7  Diag W 0x0250  Bits 5+4: 01 = 1.75 A deploy current Bits 3+2: 00 = 500 ms deploy expiration time Bits 1+0: X = Don't care  Bit 15: 0 = deployment not successful Bit 14: 0 = deployment not in progress Bit 12: 0 = deployment configuration accepted Bits 5+0: deployment expiration timer value  \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10+8: 010 = SAFING  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$12 DEPCOM S, A W 0x0FF0 Lock Code  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code   |                         |       |     |        | Bit 13-0: X = Don't care                      |
| \$6E LOOP_MATRIX_ARM1 Diag W 0x00FF Bits 7+0: 1 = FEN1 assigned to 0+7 loops  Bits 15+12: X = Don't care Bits 11+6: 0x1001 = 576 µs (9*64 µs step)  \$06 DCR_0 + \$0D DCR_7 Diag W 0x0250 Bits 5+4: 01 = 1.75 A deploy current Bits 3+2: 00 = 500 ms deploy expiration time Bits 1+0: X = Don't care  Bit 15: 0 = deployment not successful Bit 14: 0 = deployment configuration accepted Bits 5+0: deployment expiration timer value  \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10+8: 010 = SAFING  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$12 DEPCOM S, A W 0x0FF0 Bits 7+0: 0xFF = deploy requests for all channels  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  | \$00 FLTSR              | Diag  | R   | -      | Verify there are not faults                   |
| Bits 15+12: X = Don't care Bits 11+6: 0x1001 = 576 μs (9*64 μs step)  \$06 DCR_0 ÷ \$0D DCR_7 Diag W 0x0250  Bits 5+4: 01 = 1.75 A deploy current Bits 3+2: 00 = 500 ms deploy expiration time Bits 1+0: X = Don't care  Bit 15: 0 = deployment not successful Bit 14: 0 = deployment not in progress Bit 12: 0 = deployment configuration accepted Bits 5+0: deployment expiration timer value  \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10+8: 010 = SAFING  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$12 DEPCOM S, A W 0x0FF Bits 7+0: 0xFF = deploy requests for all channels \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  | \$6E LOOP_MATRIX_ARM1   | Diag  | W   | 0x00FF |   |
| Substraction   Sub      |                         |       |     |        | · ·   |
| \$06 DCR_0 ÷ \$0D DCR_7  Diag  W  0x0250  Bits 5÷4: 01 = 1.75 A deploy current  Bits 3÷2: 00 = 500 ms deploy expiration time  Bits 1+0: X = Don't care  Bit 15: 0 = deployment not successful  Bit 14: 0 = deployment configuration accepted  Bits 5÷0: deployment expiration timer value  \$31 SAFING_STATE  Diag  W  0xACAC  Frame to pass from Diag to Safing  \$04 SYS_STATE  S  R  Bits 10+8: 010 = SAFING  \$25 SPIDEPEN  S, A  W  0xOFF0  Unlock Code  \$12 DEPCOM  S, A  W  0x0FF0  Lock Code  \$25 SPIDEPEN  S, A  W  0x0FF0  Lock Code  \$12 DEPCOM  S, A  W  0x0FF0  Lock Code  |                         |       |     |        |   |
| Bits 3+2: 00 = 500 ms deploy expiration time  Bits 1+0: X = Don't care  Bit 15: 0 = deployment not successful  Bit 14: 0 = deployment not in progress  Bit 12: 0 = deployment configuration accepted  Bits 5+0: deployment expiration timer value  \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10+8: 010 = SAFING  \$25 SPIDEPEN S, A W 0xFF0 Lock Code  \$25 SPIDEPEN S, A W 0xF0F Unlock Code  \$12 DEPCOM S, A W 0x0FF0 Lock Code  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code   | #00 DOD 0 : #0D DOD 7   | D:    | 10/ | 00050  |   |
| Bits 1÷0: X = Don't care  Bit 15: 0 = deployment not successful  Bit 14: 0 = deployment not in progress  Bit 12: 0 = deployment configuration accepted  Bits 5÷0: deployment expiration timer value  \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10+8: 010 = SAFING  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$12 DEPCOM S, A W 0x0FF Bits 7÷0: 0xFF = deploy requests for all channels  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code   | \$06 DCR_0 ÷ \$0D DCR_7 | Diag  | VV  | 0x0250 |   |
| Bit 15: 0 = deployment not successful  Bit 14: 0 = deployment not in progress  Bit 12: 0 = deployment configuration accepted  Bits 5÷0: deployment expiration timer value  \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10÷8: 010 = SAFING  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$25 SPIDEPEN S, A W 0xF00F Unlock Code  \$12 DEPCOM S, A W 0x0FF0 Lock Code  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code   |                         |       |     |        |   |
| Bit 14: 0 = deployment not in progress Bit 12: 0 = deployment configuration accepted Bits 5+0: deployment expiration timer value  \$31 SAFING_STATE  |                         |       |     |        |   |
| Bit 12: 0 = deployment configuration accepted Bits 5÷0: deployment expiration timer value  \$31 SAFING_STATE  Diag  W  0xACAC  Frame to pass from Diag to Safing  \$04 SYS_STATE  S  R  Bits 10÷8: 010 = SAFING  \$25 SPIDEPEN  S, A  W  0x0FF0  Unlock Code  \$12 DEPCOM  S, A  W  0x0FF0  Lock Code  \$25 SPIDEPEN  S, A  W  0x0FF0  Lock Code  Lock Code  \$25 SPIDEPEN  S, A  W  0x0FF0  Lock Code  Lock Code  Lock Code  S25 SPIDEPEN  S, A  W  0x0FF0  Lock Code  Lock Code  |                         |       |     |        |   |
| Bits 5÷0: deployment expiration timer value  \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10÷8: 010 = SAFING  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$25 SPIDEPEN S, A W 0xF00F Unlock Code  \$12 DEPCOM S, A W 0x00FF Bits 7÷0: 0xFF = deploy requests for all channels  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code   | 13 DSR_0 ÷ \$1A DSR_7   | Diag  | R   | -      |   |
| \$31 SAFING_STATE Diag W 0xACAC Frame to pass from Diag to Safing  \$04 SYS_STATE S R - Bits 10÷8: 010 = SAFING  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  \$25 SPIDEPEN S, A W 0xF00F Unlock Code  \$12 DEPCOM S, A W 0x00FF Bits 7÷0: 0xFF = deploy requests for all channels  \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  |                         |       |     |        |   |
| \$04 SYS_STATE   | \$31 SAFING STATE       | Diag  | W   | 0xACAC |   |
| \$25 SPIDEPEN  | _                       | _     |     | -      |   |
| \$25 SPIDEPEN S, A W 0xF00F Unlock Code \$12 DEPCOM S, A W 0x00FF Bits 7÷0: 0xFF = deploy requests for all channels \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  | _                       |       |     | 0x0FF0 |   |
| \$12 DEPCOM S, A W 0x00FF Bits 7+0: 0xFF = deploy requests for all channels \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  |                         |       |     |        |   |
| \$25 SPIDEPEN S, A W 0x0FF0 Lock Code  |                         |       |     |        |   |
|  |                         |       |     |        |   |
|  | \$13 DSR_0 ÷ \$1A DSR_7 | S, A  | R   | _      | Bit 15: 1 = deployment successful             |

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### 3.3.1 Deployment waveforms

The Figure 3 and Figure 4 report some examples where a high current Pyro Fuse has been used and four channels have been put in parallel in order to achieve target current values for deployment to occur.

Referring to the Figure 1, the system has been setup with two different scenarios:

- With Safing FET, VER set to 33 V and VSF set to 25 V on main chip L96xx.
- Without Safing FET and VER set to 24 V on main chip L96xx.

The signals are the following:

- Blue = SRx
- Light blue = SFx
- Magenta = VER
- Green = Load current



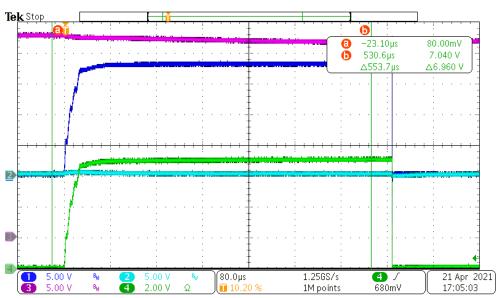
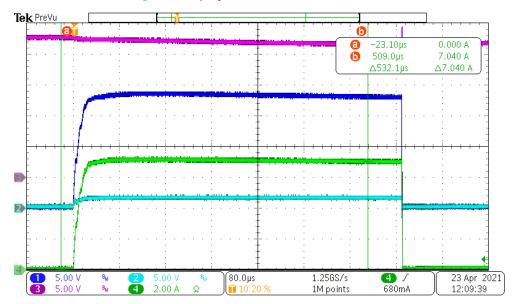


Figure 4. Deployment waveforms, VER = 24 V



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# 3.4 Arming command after deployment command

It is also possible to have a deployment event in a different way, i.e., first sending the SPI deploy command, then asserting the arming signal.

An example (watchdog disabled, deployment on Channel 0) is shown in the Table 14 and the Figure 5.

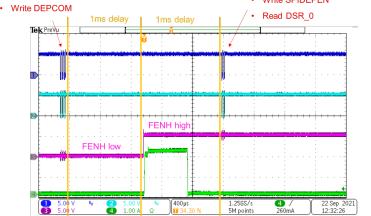
Table 14. Deploy event with Arming command after SPI deployment command

| Register read    | Register written                  | SPI frame (hex) |
|------------------|-----------------------------------|-----------------|
|                  | Configuration                     |                 |
| SYS_STATE        | SYS_CFG                           | 0x04020008      |
| SYS_CFG          | 1                                 | 0x01000000      |
| SYS_STATE        | 1                                 | 0x0400000       |
| SYS_STATE        | DIAG_STATE                        | 0x046A3CC3      |
| SYS_STATE        | 1                                 | 0x0400000       |
| POWER_STATE      | SYS_CTL                           | 0x05040000      |
| FLTSR            | 1                                 | 0x00010000      |
| LOOP_MATRIX_ARM1 | LOOP_MATRIX_ARM1                  | 0x6EDC0001      |
| DCR_0            | DCR_0                             | 0x060C0250      |
| SYS_STATE        | SAFING_STATE                      | 0x0463ACAC      |
| SYS_STATE        | 1                                 | 0x0400000       |
|                  | Deployment commands               |                 |
| SPIDEPEN         | SPIDEPEN                          | 0x254B0FF0      |
| SPIDEPEN         | SPIDEPEN                          | 0x254BF00F      |
| DEPCOM           | DEPCOM                            | 0x12240001      |
| 1                | ms delay - FENH high - 1 ms delay |                 |
| SPIDEPEN         | SPIDEPEN                          | 0x254B0FF0      |
| DSR_0            | 1                                 | 0x13000000      |

Figure 5. Deploy event with Arming command after SPI deployment command

• Write SPIDEPEN

Write SPIDEPEN



Write SPIDEPEN

Blue = SPI\_CLK Light blue = SPI\_MOSI Magenta = FENH Green = Load current

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# 4 Diagnostic

For all the channels the following diagnostics are implemented:

- High voltage leak test, for SFx and SRx oxide isolation
- VRCM test
- Leakage to battery/ground for SFx and SRx with/ without squib
- Loop to loop short diagnostic
- Squib resistance measurement leakage cancellation
- High squib resistance, 500  $\Omega$  ÷ 2000  $\Omega$
- SSxy, SFx,and VER voltage monitor
- Low Side FET diagnostic
- High Side FET diagnostic
- · Loss of ground
- · High Side Safing FET diagnostic
- Deployment timer diagnostic

In application cases where some channels are shorted and connected to the same load, the *Loop to loop short diagnostic* does not work.

These diagnostics data are elaborated by a 10 bits ADC converter.

Diagnostic can be performed in two ways:

- High level: the set-up for each requested measurement is managed by the device itself.
- Low level: the set-up for each requested measurement is managed by an external logic, step by step.

The choice of high or low level diagnostic is set via SPI (see the Table 15).

Table 15. High or Low level diagnostic

| \$38 LPDIAGREQ     | Config. in DIAG, SAFING, ARMING state |
|--------------------|---------------------------------------|
| DIAG LEVEL, bit 15 | 0 = low level                         |
| DIAG_LEVEL, bit 15 | 1 = high level                        |

The relevant blocks used for the diagnostic are reported in the Figure 6.

In particular there are a Voltage Regulator Current Monitor (VRCM) and three current generators that withstand diagnostic operations, ISRC (40 mA), ISINK (limit 70 mA) and Ipulldown (1 mA).

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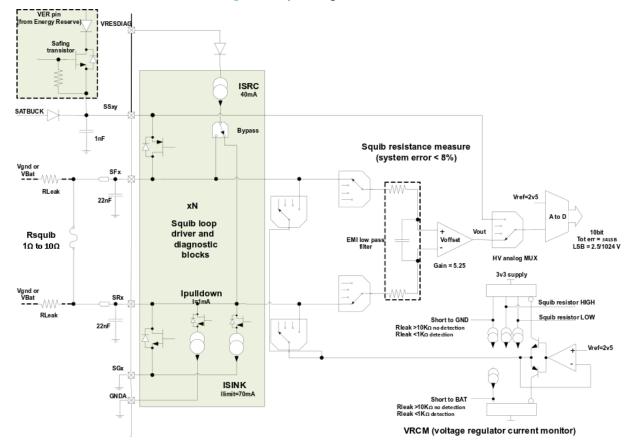


Figure 6. Squib diagnostic blocks

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# 4.1 Low level diagnostic

For a low level diagnostic, these steps shall be followed (see the Table 16):

- 1. If present, ER charge has to be previously turned on by the main chip; otherwise a max 25 V should be supplied.
- 2. Verify that the IC is in DIAG state reading register \$04.
- 3. Decide, writing the appropriate bit in reg. \$38, which diagnostic mode is used.

Table 16. Low level diagnostic

|                 | (1) | (2) | 15 | 14    | 13 | 12    | 11    | 10    | 9    | 8    | 7   | 6    | 5            | 4        | 3   | 2    | 1                          | 0   |   |
|-----------------|-----|-----|----|-------|----|-------|-------|-------|------|------|-----|------|--------------|----------|-----|------|----------------------------|-----|---|
|                 |     |     |    |       |    |       |       |       |      |      |     |      |              |          |     |      |                            |     | 14: PD&VRCM_SEL   |
|                 |     |     |    |       |    |       |       |       |      |      |     |      |              |          |     |      |                            |     | 0 = 1 mA pull down current and 450 μA VRCM leakage to GND threshold |
| \$02 SYS_CTL    | -   | w   | х  | 0/1   | х  | 0/1   | х     | х     | x    | x    | х   | x    | х            | Х        | x   | x    | X                          | х   | 1 = 5 mA pull down current and 2 mA VRCM leakage to GND threshold   |
|                 |     |     |    |       |    |       |       |       |      |      |     |      |              |          |     |      |                            |     | 12: VIN_TH_SEL depends on application                               |
|                 |     |     |    |       |    |       |       |       |      |      |     |      |              |          |     |      |                            |     | 0 = VSAT_OK = 6.5 V   |
|                 |     |     |    |       |    |       |       |       |      |      |     |      |              |          |     |      |                            |     | 1 = VSAT_OK = 8.1 V   |
| #04 CVC CTATE   |     | _   |    |       |    |       |       |       |      | 4    |     |      |              |          |     |      | 4                          |     | 10, 9, 8: 001 = DIAG  |
| \$04 SYS_STATE  |     | R   |    |       |    |       |       | 0     | 0    | 1    |     |      |              |          |     | 0    |                            | 0   | 2, 1, 0: 010 = RUN  |
| \$38 LPDIAGREQ  | (l) | W   | 0  |       |    | 14:0  | defin | e th  | e te | est, | see | ne   | xt c         | hap      | pte | s    |                            |     | 15:0 = low level diag   |
| \$37 LPDIAGSTAT |     |     |    |       |    |       |       |       |      |      |     |      |              |          |     |      |                            |     |   |
| (3) 19 18 17 16 |     | R   | 0  |       | •  | 14:0  | detin | ie th | e te | est, | see | e ne | xt c         | hap      | pte | °S   |                            |     | 15:0 = low level diag   |
| \$3X DIAGCTRL_X |     |     |    | .,    |    |       |       |       |      |      |     |      |              |          |     |      |                            |     |   |
| X = A, B, C, D  |     | W   |    | Х     | Х  | Х     | Х     | Х     | X    | X    | X   | '    | 6:0          | AD       | C a | ıddı | ress                       | SSS |   |
| (3) 19 18 17 16 |     |     |    | 10.40 |    | 0     |       | _     |      |      |     | 2.0  | <b>A D</b> ( | <b>~</b> |     | 14   |                            |     | 40.4  |
| 1               |     |     |    | 16:10 | AD | C add | ares  | S     |      |      | ٤   | 9:0  | AD(          | J r€     | esu | Ι    | 19:1 = conversion finished |     |   |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

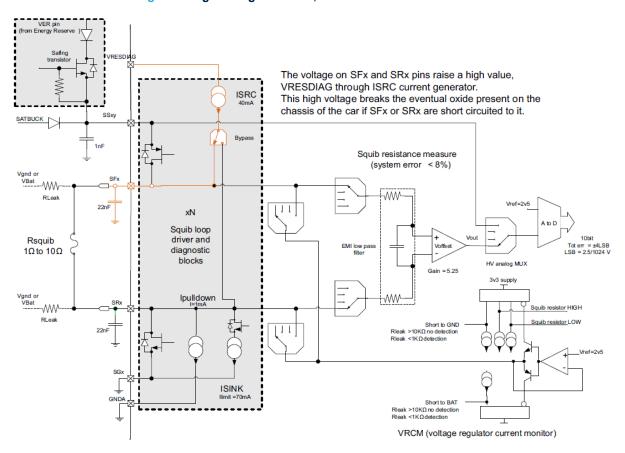
In low level mode, the IC performs the measurement, following the external requests. Each test set-up is driven, step by step, by the microcontroller, as the timing for the measurement.

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### 4.1.1 High voltage leak test, oxide isolation IC-car chassis

Figure 7. High voltage leak test, oxide isolation IC-car chassis



This test is mandatory and verifies that no leakages are present on the SFx or SRx pins when high voltage is applied. ISRC current generator is ON and addressed on SFx (see the Table 17).

If there is no leakage, SFx raises up to VSYNC and, being the impedance between SFx and SRx very low (squib connected), SRx follows SFx (see the Figure 7).

Confirmation of this is done through an ADC measurement request of the SFx voltage value.

Table 17. High voltage leak test, oxide isolation IC-car chassis - LPDIAGREQ register

|                | (1) | (2) | 15 | 14 | 13 | 12:11 | 10 | 9:8 | 7:4  | 3:0  |  |
|----------------|-----|-----|----|----|----|-------|----|-----|--|--|--|
|                |     |     |    |    |    | 12.11 |    | 0.0 | RES_MEAS_CHSEL<br>0000 = ch0<br>0001 = ch1<br>0010 = ch2                         | LEAK_CHSEL<br>0000 = ch0<br>0001 = ch1<br>0010 = ch2                             | 15: 0 = low level diag 14: 0 = ISRC = 40 mA 13: 1 = pull-down curr. OFF for all channels                     |
| \$38 LPDIAGREQ | (1) | W   | 0  | 0  | 1  | 01    | 0  | 00  | 0011 = ch3<br>0100 = ch4<br>0101 = ch5<br>0110 = ch6<br>0111 = ch7<br>1000 = ch8 | 0011 = ch3<br>0100 = ch4<br>0101 = ch5<br>0110 = ch6<br>0111 = ch7<br>1000 = ch8 | 12, 11: 01 = ISCR for RES_MEAS_CHSEL, OFF for the others 10: 0 = ISINK all OFF 9, 8: 00 = VRCM not connected |

1. I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

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<sup>2.</sup> R = READ, W = WRITE



SFx voltages and VSYNC are readable by the microcontroller through the ADC converter in the registers \$3X DIAGCTRL X, with X = A, B, C, D (see the Table 18).

Table 18. High voltage leak test, oxide isolation IC-car chassis - DIAGCTRL\_X registers

|     |                |      |      |          | (1) | (2) | 15       | 14  | 13     | 12    | 11 | 10 | 9   | 8    | 7                | 6:0                  |                             |  |  |  |  |
|-----|----------------|------|------|----------|-----|-----|----------|-----|--------|-------|----|----|-----|------|------------------|----------------------|-----------------------------|--|--|--|--|
|     |                |      |      |          |     |     |          |     |        |       |    |    |     |      |                  | ADCREQ_X             |                             |  |  |  |  |
|     |                |      |      |          |     |     |          |     |        |       |    |    |     |      |                  | \$25 = VSYNC         |                             |  |  |  |  |
|     |                |      |      |          |     |     |          |     |        |       |    |    |     |      |                  | \$46 = SF0           |                             |  |  |  |  |
|     |                |      |      |          |     |     |          |     |        |       |    |    |     |      |                  | \$47 = SF1           |                             |  |  |  |  |
|     | \$             | 3X E | OIAG | CTRL_X   | _   | W   | x        | Х   | Х      | Х     | Х  | Х  | Х   | Х    | Х                | \$48 = SF2           |                             |  |  |  |  |
|     |                | X =  | А, В | , C, D   | -   | VV  | ^        | ^   | ^      | ^     | ^  | ^  | ^   | ^    | ^                | \$49 = SF3           |                             |  |  |  |  |
|     |                |      |      |          |     |     |          |     |        |       |    |    |     |      |                  | \$4A = SF4           |                             |  |  |  |  |
|     |                |      |      |          |     |     |          |     |        |       |    |    |     |      |                  | \$4B = SF5           |                             |  |  |  |  |
|     |                |      |      |          |     |     |          |     |        |       |    |    |     |      |                  | \$4C = SF6           |                             |  |  |  |  |
|     |                |      |      |          |     |     |          |     |        |       |    |    |     |      |                  | \$4D = SF7           |                             |  |  |  |  |
| (3) | 19             | 18   | 17   | 16       |     |     |          |     |        |       |    |    |     |      |                  |                      | 19: 1 = conversion finished |  |  |  |  |
|     |                |      |      |          |     |     | ADCREQ_X |     |        |       |    |    |     |      |                  |                      |                             |  |  |  |  |
|     |                |      |      |          |     |     |          | \$2 | 25 = \ | /SYN  | IC |    |     |      |                  |                      |                             |  |  |  |  |
|     |                |      |      |          |     |     |          | ,   | \$46 = | SFC   | )  |    |     |      |                  |                      |                             |  |  |  |  |
|     |                |      |      |          |     |     |          | ,   | \$47 = | SF1   |    |    |     |      |                  |                      |                             |  |  |  |  |
|     | 1              | 0    |      | ADCREO V | _   | R   |          | ,   | \$48 = | SF2   | 2  |    | ļ , | DCI  | DEO              | _X 10 bit ADC result |                             |  |  |  |  |
|     | 1 0 0 ADCREQ_X |      |      |          |     | K   |          | ,   | \$49 = | SF3   | 3  |    | ′   | NDCI | \⊏Q <sub>.</sub> | _X TO bit ADC result |                             |  |  |  |  |
|     |                |      |      |          |     |     |          | 5   | \$4A = | = SF4 | ŀ  |    |     |      |                  |                      |                             |  |  |  |  |
|     |                |      |      |          |     |     |          | 5   | \$4B = | = SF5 | 5  |    |     |      |                  |                      |                             |  |  |  |  |
|     |                |      |      |          |     |     |          | 5   | \$4C = | = SF6 | 6  |    |     |      |                  |                      |                             |  |  |  |  |
|     |                |      |      |          |     |     |          | 5   | \$4D = | = SF7 | 7  |    |     |      |                  |                      |                             |  |  |  |  |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Once read the ADC measurement, to obtain the voltage value it is necessary to consider the divider ratio of the ADC. In case of SFx it is 15:1, in case of VSYNC it is 10:1.

As an example, consider the case where the VSYNC conversion has been requested and the readout of the ADC register is done. The voltage measured on VSYNC pin is 12 V.

ADC = 0b0111101100 = 0x1EC = 492

In order to obtain the result in Volt, being the ADC characteristic linear:

$$2.5 V: 1024 = x: ADC \rightarrow x = \frac{492 * 2.5 V}{1024} = 1.2 V$$
 (1)

Considering the divider ratio (DR), the result is:

$$VRESDIAG = x * DR = 1.2 V * 10 = 12 V$$
 (2)

#### Test result

In case of leakage on High Side (SFx) or Low Side (SRx), SFx voltage is not able to reach VSYNC and the microcontroller can detect the leakage problem, both on the High Side or on the Low Side, with no possibility, at this stage, to distinguish which of them is involved in the problem.

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#### 4.1.2 VRCM test validation

Before using VRCM block, used in many IC diagnostics, it is necessary a test for its validation. The test is done through short to battery and short to ground flag verification. Measurement set-up is composed by 2 steps, with VSYNC supplied.

#### 4.1.2.1 VRCM test - First step

VER p HS FET diagnostic: check VRCM functionality First we use ISRC current generator to check VRCM block ISRC Squib resistance measure (system error < 8%) Vgnd or VBat -WW Squib loop Rsquib driver and diagnostic 1Ω to 10Ω HV analog MUX Gain = 5.25 lpulldown -WW Short to GND Rleak >10KΩ no detection Rleak <1KΩdetection Squib resistor LOW 111 ISINK

Figure 8. VRCM test validation - First step

The first step (see the Figure 8) is verified through the LPDIAGREQ register (see the Table 19).

(1) | (2) | 15 | 14 | 13 | 12:11 | 10 | 9:8 7:4 3:0 RES\_MEAS\_CHSEL LEAK\_CHSEL 0000 = ch00000 = ch015: 0 = low level diag 0001 = ch10001 = ch114: 0 = ISRC = 40 mA 0010 = ch20010 = ch213: 1 = pull-down curr. OFF all ch 0011 = ch30011 = ch312, 11: 01 = ISCR for RES\_MEAS\_CHSEL, \$38 LPDIAGREQ (I) W 0 0 01 0 01 0100 = ch40100 = ch4OFF for the others 0101 = ch50101 = ch510: 0 = ISINK all OFF 0110 = ch60110 = ch69, 8: 01 = VRCM connected to SFx (LEAK\_CHSEL) 0111 = ch70111 = ch71000 = ch81000 = ch8

Table 19. VRCM test validation (first step) - LPDIAGREQ register

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 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING$ 

<sup>2.</sup> R = READ, W = WRITE



RES\_MEAS\_CHSEL, bit[7:4] and LEAK\_CHSEL, bit[3:0] must refer to the same channel.

#### Test 1 result

Being ISRC and VRCM connected to SFx, if VRCM works correctly, short to battery, readable in the LPDIAGSTAT register, is asserted for the channel selected (see the Table 20).

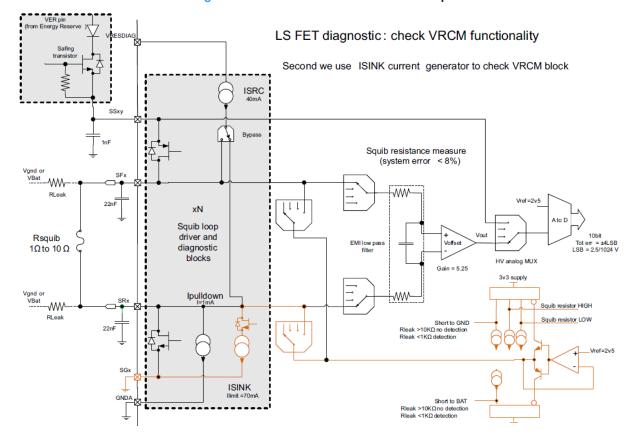
Table 20. VRCM test validation (first step) - LPDIAGSTAT register

|     |         |         |            |         | (1) | (2)    | 15:12      | 11:8   | 7 | 6 | 5 | 4 | 3:0   |   |
|-----|---------|---------|------------|---------|-----|--------|------------|--|---|---|---|---|---|---|
| (3) | 19<br>0 | 18<br>0 | GSTA<br>17 | 16<br>0 | (1) | R<br>R | 15:12<br>X | 11:8  RES_MEAS_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7 | 0 | 0 | 1 | 1 | 3:0  LEAK_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7 | 19: 0 = low level diag 7: 0 = no short between loops 6: 0 = STG not detected 5: 1 = STB detected 4: 1 = test on SFx |
|     |         |         |            |         |     |        |            | 1000 = ch8   |   |   |   |   | 1000 = ch8  |   |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

#### 4.1.2.2 VRCM test - Second step

Figure 9. VRCM test validation - Second step



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Once the first step of VRCM test is passed, it is possible to proceed with the second step (see the Figure 9), always through the LPDIAGREQ register (see the Table 21).

Table 21. VRCM test validation (second step) - LPDIAGREQ register

|                    | (1) | (2) | 15 | 14 | 13 | 12:11 | 10 | 9:8 | 7:4            | 3:0        |  |
|--------------------|-----|-----|----|----|----|-------|----|-----|----------------|------------|--|
|                    |     |     |    |    |    |       |    |     | RES_MEAS_CHSEL | LEAK_CHSEL |  |
|                    |     |     |    |    |    |       |    |     | 0000 = ch0     | 0000 = ch0 | 15: 0 = low level diag                       |
|                    |     |     |    |    |    |       |    |     | 0001 = ch1     | 0001 = ch1 | 14: 0 = ISRC = 40 mA                         |
|                    |     |     |    |    |    |       |    |     | 0010 = ch2     | 0010 = ch2 | 13: 1 = pull-down curr. OFF for all channels |
| \$38 LPDIAGREQ     | (I) | w   | 0  | 0  | 1  | 00    | 1  | 10  | 0011 = ch3     | 0011 = ch3 | 12, 11: 00 = ISRC OFF for all channels       |
| \$55 E. S (5.1.E.) | (., |     |    |    | ·  |       |    |     | 0100 = ch4     | 0100 = ch4 | 10: 1 = ISINK ON (RES_MES_CHSEL), OFF        |
|                    |     |     |    |    |    |       |    |     | 0101 = ch5     | 0101 = ch5 | for the others                               |
|                    |     |     |    |    |    |       |    |     | 0110 = ch6     | 0110 = ch6 | 9, 8: 10 = VRCM connected to SRx             |
|                    |     |     |    |    |    |       |    |     | 0111 = ch7     | 0111 = ch7 | (LEAK_CHSEL)                                 |
|                    |     |     |    |    |    |       |    |     | 1000 = ch8     | 1000 = ch8 |  |

 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING$ 

RES MEAS CHSEL, bit[7:4] and LEAK CHSEL, bit[3:0] must refer to the same channel.

#### Test 2 result

Being ISNK and VRCM connected to SRx, if VRCM works correctly, short to ground, readable in the LPDIAGSTAT register, is asserted for the channel selected (see the Table 22).

Table 22. VRCM test validation (second step) - LPDIAGSTAT register

|     |         |            |         |         | (1) | (2) | 15:12 | 11:8   | 7 | 6 | 5 | 4 | 3:0  |   |
|-----|---------|------------|---------|---------|-----|-----|-------|--|---|---|---|---|--|---|
| (3) | \$37 LI | PDIA<br>18 | 17<br>0 | 16<br>0 |     | R   | ×     | RES_MEAS_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7  1000 = ch8 | 0 | 1 | 0 | 0 | LEAK_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7  1000 = ch8 | 19: 0 = low level diag 7: 0 = no short between loops 6: 1 = STG detected 5: 0 = STB not detected 4: 0 = test on SRx |

 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING$ 

### Final result

If the second step of the VRCM test is passed too, the VRCM test is validated.

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<sup>2.</sup> R = READ, W = WRITE

<sup>2.</sup> R = READ, W = WRITE

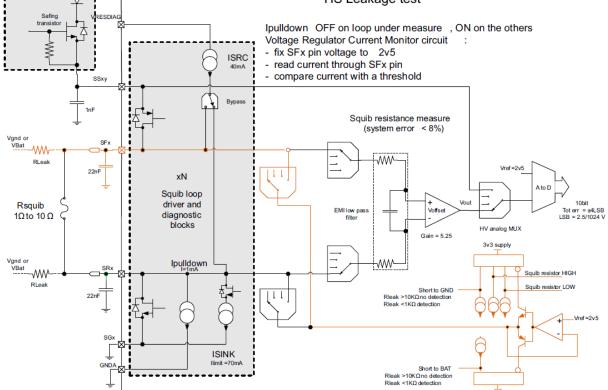
<sup>3.</sup> Further bit over the 16 standard.



#### 4.1.3 Leakage test - High Side

HS Leakage test Voltage Regulator Current Monitor circuit

Figure 10. Leakage test - High Side



ISRC and ISINK are kept off and VRCM is connected to SFx (see the Figure 10), chosen through the LEAK\_CHSEL bits in the LPDIAGREQ register (see the Table 23).

(1) (2) 15 14 13 12:11 10 9:8 7:4 3:0 RES MEAS CHSEL LEAK CHSEL 0000 = ch00000 = ch015: 0 = low level diag 0001 = ch10001 = ch114: 0 = ISRC = 40 mA 0010 = ch20010 = ch213: 0 = pull-down curr. OFF for VRCM ch; ON 0011 = ch30011 = ch3for the others \$38 LPDIAGREQ (I) W 0 0 01 0 0 00 0100 = ch40100 = ch412, 11: 00 = ISCR OFF for all channels 0101 = ch50101 = ch510: 0 = ISINK all OFF 0110 = ch60110 = ch69, 8: 01 = VRCM to SFx (LEAK\_CHSEL) 0111 = ch70111 = ch71000 = ch81000 = ch8

Table 23. Leakage test, High Side - LPDIAGREQ register

#### **Test result**

If there is no leakage on the High Side, SFx voltage is equal to VREF = 2.5 V and no current is detected by VRCM itself. SFx voltage is readable addressing the ADC read out on it. The registers involved in this operation are the four DIAGCTRL X (see the Table 24).

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<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

<sup>2.</sup> R = READ, W = WRITE

|     |    |    |    |                  | (1) | (2) | 15 | 14          | 13   | 12  | 11 | 10 | 9 | 8   | 7   | 6   | 5  | 4                                      | 3   | 2                                      | 1                          | 1   | 0 |                             |
|-----|----|----|----|------------------|-----|-----|----|-------------|--|---|----|----|---|-----|-----|-----|----|--|---|--|----------------------------|-----|---|-----------------------------|
|     | \$ |    |    | CTRL_X<br>, C, D | _   | w   | X  | X           | ×  | x   | ×  | x  | X | X   | X   |     |    | \$4<br>\$4<br>\$4<br>\$4<br>\$4<br>\$4 | CRI<br>6 = 17 = 18 = 19 = 18 = 18 = 18 = 18 = 18 = 18 | SFO<br>SFO<br>SFO<br>SFO<br>SFO<br>SFO | )<br>1<br>2<br>3<br>4<br>5 |     |   |                             |
| (3) | 19 | 18 | 17 | 16               |     |     |    |             |  |   |    |    |   |     |     |     |    |  |   |  |                            |     |   | 19: 1 = conversion finished |
|     | 1  | 0  | 0  | ADCREQ_X         | -   | R   |    | ;<br>;<br>; | \$46 =<br>\$47 =<br>\$48 =<br>\$49 =<br>\$4A =<br>\$4B = | EQ_:<br>= SF0<br>= SF1<br>= SF2<br>= SF3<br>= SF4<br>= SF5<br>= SF6 |    |    | , | ADC | CRE | Q_X | 10 | ) bi                                   | t AE  | OC r                                   | esı                        | ult |   |                             |

Table 24. Leakage test, High Side - DIAGCTRL\_X register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Once read the ADC measurement, to obtain the voltage value it is necessary to consider the divider ratio of the ADC, that is 15:1 in case of SFx.

In case of a leakage (to ground or to battery), VRCM will sink or source a current to maintain SFx at VREF. Therefore, STG or STB is set in the LPDIAGSTAT register (see the Table 25).

|     |         |            |            |       | (1) | (2)    | 15:12      | 11:8   | 7 | 6   | 5   | 4 | 3:0   |   |
|-----|---------|------------|------------|-------|-----|--------|------------|--|---|-----|-----|---|---|---|
| (3) | 19<br>0 | PDIA<br>18 | GST/<br>17 | AT 16 | (1) | R<br>R | 15:12<br>X | 11:8  RES_MEAS_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5 | 0 | 0/1 | 0/1 | 1 | 3:0  LEAK_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5 | 19: 0 = low level diag 7: 0 = no short between loops 6: 1 = STG if leak vs GND 5: 1 = STB if leak vs BATT |
|     |         |            |            |       |     |        |            | 0110 = ch6<br>0111 = ch7<br>1000 = ch8   |   |     |     |   | 0110 = ch6<br>0111 = ch7<br>1000 = ch8  | 4: 1 = test on SFx  |

Table 25. Leakage test, High Side - LPDIAGSTAT register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

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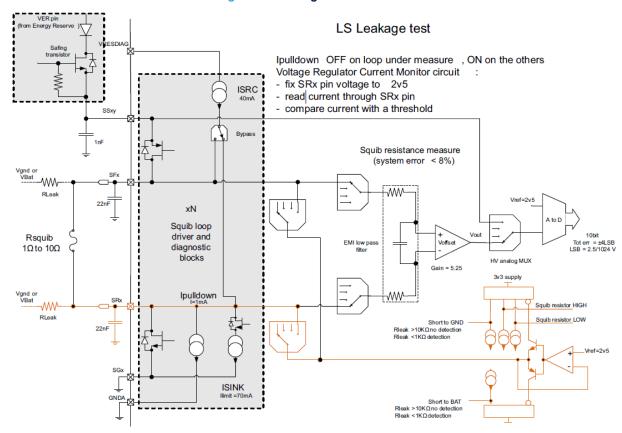
Pull-down current (1 mA) is active on all the channels except the one under analysis. So, the STG requires further investigation to understand if it comes from a real short to ground of the channel itself or it comes from a short between the channel itself and another one.

Note:

In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all the channels.

#### 4.1.4 Leakage test - Low Side

Figure 11. Leakage test - Low Side



ISRC and ISINK are kept off and VRCM is connected to SRx (see the Figure 11), chosen through the LEAK\_CHSEL bits in the LPDIAGREQ register (see the Table 26).

Table 26. Leakage test, Low Side - LPDIAGREQ register

|                       | (1) | (2) | 15 | 14 | 13 | 12:11 | 10 | 9:8 | 7:4            | 3:0        |  |
|-----------------------|-----|-----|----|----|----|-------|----|-----|----------------|------------|--|
|                       |     |     |    |    |    |       |    |     | RES_MEAS_CHSEL | LEAK_CHSEL |  |
|                       |     |     |    |    |    |       |    |     | 0000 = ch0     | 0000 = ch0 |  |
|                       |     |     |    |    |    |       |    |     | 0001 = ch1     | 0001 = ch1 | 15: 0 = low level diag                                     |
|                       |     |     |    |    |    |       |    |     | 0010 = ch2     | 0010 = ch2 | 14: 0 = ISRC = 40 mA                                       |
| \$38 LPDIAGREQ        | (I) | w   | 0  | 0  | 0  | 00    | 0  | 10  | 0011 = ch3     | 0011 = ch3 | 13: 0 = pull-down curr. OFF for VRCM ch; ON for the others |
| \$50 II 3 II 15 II 12 | (., |     |    |    |    |       |    |     | 0100 = ch4     | 0100 = ch4 | 12, 11: 00 = ISCR OFF for all channels                     |
|                       |     |     |    |    |    |       |    |     | 0101 = ch5     | 0101 = ch5 | 10: 0 = ISINK all OFF                                      |
|                       |     |     |    |    |    |       |    |     | 0110 = ch6     | 0110 = ch6 | 9, 8: 10 = VRCM to SRx                                     |
|                       |     |     |    |    |    |       |    |     | 0111 = ch7     | 0111 = ch7 |  |
|                       |     |     |    |    |    |       |    |     | 1000 = ch8     | 1000 = ch8 |  |

<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

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#### 2. R = READ, W = WRITE

#### **Test result**

If there is no leakage on the High Side, SRx voltage is equal to VREF = 2.5 V and no current is detected by VRCM itself.

Only if the squib is connected, SFx and SRx pins are at the same voltage, so SRx voltage is readable indirectly through SFx voltage, as done in case of High Side leakage test.

SFx voltage is readable addressing the ADC read out on it. The registers involved in this operation are the four DIAGCTRL X (see the Table 27).

(1) (2) 15 8 7 6 5 4 3 2 1 0 ADCREQ X \$46 = SF0 \$47 = SF1 \$48 = SF2 \$3X DIAGCTRL\_X  $X \mid X \mid X$ W Χ Χ Χ Χ Χ \$49 = SF3 Х X = A, B, C, D\$4A = SF4 \$4B = SF5 \$4C = SF6 \$4D = SF7 19 18 17 16 19: 1 = conversion finished ADCREQ\_X \$46 = SF0 \$47 = SF1 \$48 = SF2 R 0 ADCREQ\_X \$49 = SF3 ADCREQ\_X 10 bit ADC result \$4A = SF4 \$4B = SF5 \$4C = SF6 \$4D = SF7

Table 27. Leakage test, Low Side - DIAGCTRL\_X register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Once read the ADC measurement, to obtain the voltage value it is necessary to consider the divider ratio of the ADC, that is 15:1 in case of SFx.

If the squib between SFx and SRx pins is not connected, SRx voltage read out is not possible, as it is not mapped into the ADC request command.

In case of a leakage (to ground or to battery), VRCM will sink or source a current to maintain SFx at VREF. Therefore, STG or STB is set in the LPDIAGSTAT register (see the Table 28).

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|     |       |           |    |    | (1) | (2) | 15:12      | 11:8           | 7 | 6   | 5   | 4          | 3:0                           |                            |
|-----|-------|-----------|----|----|-----|-----|------------|----------------|---|-----|-----|------------|-------------------------------|----------------------------|
| \$  | 37 LF | PDIAGSTAT |    |    |     | R   |            | RES_MEAS_CHSEL |   |     |     |            | LEAK_CHSEL                    |                            |
| (3) | 19    | 18        | 17 | 16 |     | R   |            | 0000 = ch0     |   |     |     |            | 0000 = ch0                    |                            |
|     |       |           |    |    |     |     | 0001 = ch1 |                |   |     |     | 0001 = ch1 | 19: 0 = low level diag        |                            |
|     |       |           |    |    |     |     | 0010 = ch2 |                |   |     |     | 0010 = ch2 | 7: 0 = no short between loops |                            |
|     |       |           |    | 0  |     |     | Х          | 0011 = ch3     | 0 | 0/1 | 0/1 | 0          | 0011 = ch3                    | 6: 1 = STB if leak vs GND  |
|     | 0     | 0         | 0  |    |     |     |            | 0100 = ch4     |   |     |     |            | 0100 = ch4                    | 5: 1 = STB if leak vs BATT |
|     | 0     | U         | U  |    |     |     |            | 0101 = ch5     |   |     |     |            | 0101 = ch5                    | 4: 0 = test on SRx         |
|     |       |           |    |    |     |     | 0110 = ch6 |                |   |     |     | 0110 = ch6 |                               |                            |
|     |       |           |    |    |     |     | 0111 = ch7 |                |   |     |     | 0111 = ch7 |                               |                            |
|     |       |           |    |    |     |     | 1000 = ch8 |                |   |     |     | 1000 = ch8 |                               |                            |

Table 28. Leakage test, Low Side - LPDIAGSTAT register

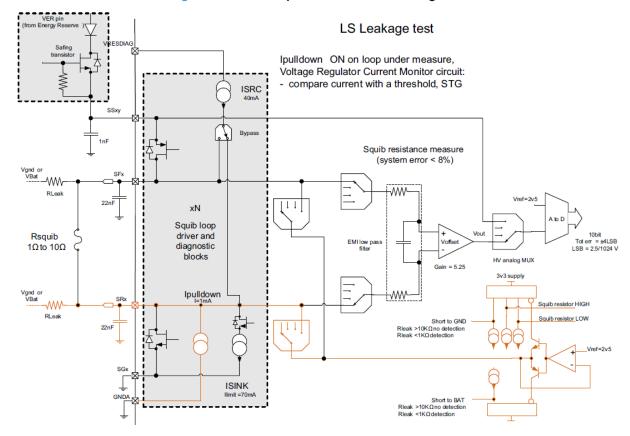
- $1. \quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING$
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Pull-down current (1 mA) is active on all the channels except the one under analysis. So, for the case of STG detection, further investigation is necessary to understand if it comes from a real short to ground of the channel or from a short of the channel with another one.

Note: In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all the channels.

#### 4.1.5 Leakage test - Low Side pulldown current

Figure 12. Low Side pulldown current - Leakage test



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After having verified that no HS/LS leakage is present, it is possible to verify if IPD is correctly working. VRCM is connected to SRx (see the Figure 12), chosen through the LEAK\_CHSEL. IPD is switched on for that channel (see the Table 29).

Table 29. Leakage test, Low Side pulldown current - LPDIAGREQ register

|                 | (1) | (2) | 15 | 14 | 13 | 12:11 | 10 | 9:8 | 7:4            | 3:0        |   |
|-----------------|-----|-----|----|----|----|-------|----|-----|----------------|------------|---|
|                 |     |     |    |    |    |       |    |     | RES_MEAS_CHSEL | LEAK_CHSEL |   |
|                 |     |     |    |    |    |       |    |     | 0000 = ch0     | 0000 = ch0 | 15: 0 = low level diag                      |
|                 |     |     |    |    |    |       |    |     | 0001 = ch1     | 0001 = ch1 | 14: 0 = ISRC = 40 mA                        |
|                 |     |     |    |    |    |       |    |     | 0010 = ch2     | 0010 = ch2 | 13: 0 = pull-down curr. OFF for VRCM ch; ON |
| \$38 LPDIAGREQ  | (1) | ۱۸/ | 0  | 0  | 0  | 00    | 0  | 11  | 0011 = ch3     | 0011 = ch3 | for the others                              |
| \$30 LF DIAGNEQ | (1) | VV  |    | 0  | U  | 00    | U  | 11  | 0100 = ch4     | 0100 = ch4 | 12, 11: 00 = ISCR OFF on all channels       |
|                 |     |     |    |    |    |       |    |     | 0101 = ch5     | 0101 = ch5 | 10: 0 = ISINK all OFF                       |
|                 |     |     |    |    |    |       |    |     | 0110 = ch6     | 0110 = ch6 | 9, 8: 11 = VRCM to SRx and IPD of SRx       |
|                 |     |     |    |    |    |       |    |     | 0111 = ch7     | 0111 = ch7 | enabled                                     |
|                 |     |     |    |    |    |       |    |     | 1000 = ch8     | 1000 = ch8 |   |

<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

#### **Test result**

If IPD is working, SRx voltage is equal to VOUT\_VRCM and VRCM shows STG (see the Table 30). If, in this condition, STG is not set, it means that there is something not correctly working in IPD.

Table 30. Leakage test, Low Side pulldown current - LPDIAGSTAT register

|     |    |      |            |    | (1) | (2)    | 15:12 | 11:8   | 7 | 6 | 5 | 4 | 3:0  |  |
|-----|----|------|------------|----|-----|--------|-------|--|---|---|---|---|--|--|
| (3) | 19 | PDIA | GSTA<br>17 | 16 |     | R<br>R |       | RES_MEAS_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2                               | • |   |   |   | LEAK_CHSEL<br>0000 = ch0<br>0001 = ch1<br>0010 = ch2                             | 19: 0 = low level diag   |
|     | 0  | 0    | 0          | 0  |     |        | X     | 0011 = ch3<br>0100 = ch4<br>0101 = ch5<br>0110 = ch6<br>0111 = ch7<br>1000 = ch8 | 0 | 1 | 0 | 0 | 0011 = ch3<br>0100 = ch4<br>0101 = ch5<br>0110 = ch6<br>0111 = ch7<br>1000 = ch8 | 7: 0 = no short between loops 6: 1 = STG detected 5: 0 = STB not detected 4: 0 = test on SRx |

<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

Note:

In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all the channels.

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<sup>2.</sup> R = READ, W = WRITE

<sup>2.</sup> R = READ, W = WRITE

<sup>3.</sup> Further bit over the 16 standard.



#### 4.1.6 Short between loops

Supposing the external load is connected, a short to ground flag of SRx or SFx can be read as:

- Short of the pin with SR or SF of another channel, both SR and SF
- Real short of the pin SRx or SFx to GND

Note:

In Pyro Fuse Application with channels shorted together, the short to ground should be a real short of SRx or SFx pin to GND. Moreover, a short to ground on a channel will be present on all the others.

In this test the pulldown current generators are switched off for all channels. If the STG is still present, it means a real STG of the channel under test.

The correspondent set up is done by setting the \$38 LPDIAGREQ properly (see the Table 31):

Table 31. Short between loops - LPDIAGREQ register

|                | (1) | (2) | 15 | 14 | 13 | 12:11 | 10 | 9:8 | 7:4   | 3:0   |   |
|----------------|-----|-----|----|----|----|-------|----|-----|---|---|---|
| \$38 LPDIAGREQ |     |     |    | 0  | 13 | 00    | 0  | 9:8 | 7:4  RES_MEAS_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7 | 3:0  LEAK_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7 | 15: 0 = low level diag  14: 0 = ISCR = 40 mA  13: 1 = pull-down curr. OFF for all channels  12, 11: 00 = ISCR OFF for all channels  10: 0 = ISINK all OFF  9, 8: 01 = VRCM to SFx  10 = VRCM to SRx |
|                |     |     |    |    |    |       |    |     | 1000 = ch8  | 1000 = ch8  |   |

<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

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<sup>2.</sup> R = READ, W = WRITE



# 4.1.6.1 High Side short to ground

Short between loop
SFi really STG

Short between loop
SFi really STG

Squib resistance measure
(system error < 8%)

Requib
10 10 10 0

Requib
10 10 10 0

Residence of the control of the

Figure 13. High Side short to ground

Ipulldown is OFF for all channels.

The VRCM circuit (see the Figure 13):

- Fixes SFx pin to 2.5 V.
- Reads the current through the SFx pin.
- Compares the current with a threshold.

The result is a STG on SFx.

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#### 4.1.6.2 Low Side short to ground

Short between loop
SRi really STG

Safing
Personal South Series South
Series South
Safing
Personal South Series South
Safing
Personal South Series South
Safing
South Series South
South Se

Figure 14. Low Side short to ground

Ipulldown is OFF for all channels.

The VRCM circuit (see the Figure 14):

- Fixes SRx pin to 2.5 V.
- Reads the current through the SRx pin.
- Compares the current with a threshold.

The result is a STG on SRx.

### 4.1.7 Squib resistance measurements

The IC allows measuring the squib resistance value in the range of 1  $\Omega$  ÷ 10  $\Omega$  with overall 8% precision.

This is a two-step process.

Note: In Pyro Fuse Application with channels shorted together, the squib resistance measurement should be the same on all the channels.

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#### 4.1.7.1 Squib resistance measurements - First step

1°step squib resistance measure: ISRC = 40mA ISRC SSxy Squib resistance measure (system error < 8%) Vref=2v5 22nl χN A to D Squib loop Rsquib driver and 1Ω to 10Ω diagnostic blocks Gain = 5.25 lpulldown ₩ Squib resistor LOW Short to GND ISINK Short to BAT

Figure 15. Squib resistance measurements - First step

Through this set-up (see the Figure 15):

- The ISRC is connected to the SFx.
- The squib is correctly connected between SFx and SRx.
- SRx is internally connected to ISINK that is able to sink the current.

The correspondent set up is done by setting the \$38 LPDIAGREQ properly (see the Table 32):

(1) (2) 15 14 13 12:11 10 9:8 7:4 3:0 RES\_MEAS\_CHSEL LEAK\_CHSEL 0000 = ch00000 = ch015: 0 = low level diag 0001 = ch10001 = ch114: 0 = ISRC = 40 mA 0010 = ch20010 = ch213: 1 = pull-down curr. OFF all ch 0011 = ch30011 = ch312, 11: 01 = ISCR (RES\_MEAS\_CH) ON, OFF \$38 LPDIAGREQ (I) W 0 00 0 1 01 1 0100 = ch40100 = ch4the others 0101 = ch50101 = ch510: 1 = ISINK (RES\_MEAS\_CH) ON, OFF the 0110 = ch60110 = ch69, 8: 00 = VRCM not connected 0111 = ch70111 = ch71000 = ch81000 = ch8

Table 32. Squib resistance measurements (first step) - LPDIAGREQ register

2. R = READ, W = WRITE

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 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING$ 



The first step of the measurement is the read out of the voltage between SFx and SRx that is named resistance into ADC addressing.

This parameter is readable by the microcontroller, via 10bit ADC, through a dedicated request.

The registers to be read are still the four DIAGCTRL\_X (see the Table 33):

Table 33. Squib resistance measurements (first step) - DIAGCTRL\_X register

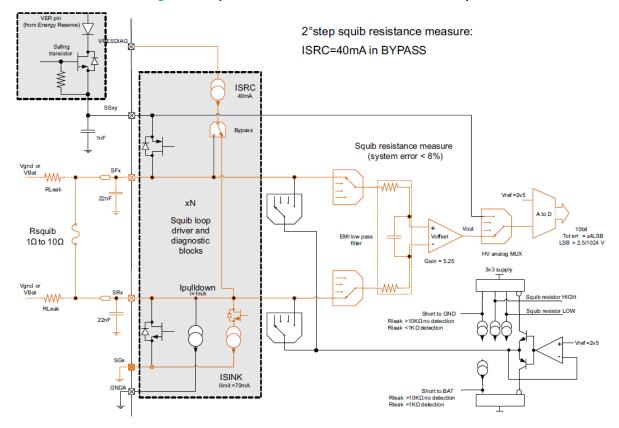
|     |    |    |          |                  | (1) | (2) | 15 | 14  | 13 | 12 | 11  | 10 | 9  | 8   | 7                       | 6 5 4 3 2 1 0                      |
|-----|----|----|----------|------------------|-----|-----|----|-----|----|----|-----|----|----|-----|-------------------------|------------------------------------|
|     | \$ |    |          | CTRL_X<br>, C, D | -   | W   | х  | X   | X  | Х  | Х   | X  | х  | x   | x                       | ADCREQ_X \$06 = squib x resistance |
| (3) | 19 | 18 | 17       | 16               |     |     |    |     |    |    |     |    |    |     |                         | 19: 1 = conversion finished        |
|     | 1  | 0  | ADCREQ_X | -                | R   | \$0 |    | DCR | _  |    | ice |    | Α[ | OCF | REQ_X 10 bit ADC result |                                    |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Once read the ADC measurement, to obtain the value it is necessary to consider the divider ratio of the ADC. In case of resistance x, it is 1:1.

#### 4.1.7.2 Squib resistance measurements - Second step

Figure 16. Squib resistance measurements - Second step



Through this set-up (see the Figure 16):

- The ISRC is connected to the SRx.
- The squib is correctly connected between SFx and SRx.
- SRx is internally connected to ISINK that is able to sink the current.

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The correspondent set up is done by setting the \$38 LPDIAGREQ properly (see the Table 34):

Table 34. Squib resistance measurements (second step) - LPDIAGREQ register

|                    | (1) | (2) | 15 | 14 | 13 | 12:11 | 10 | 9:8 | 7:4            | 3:0        |   |
|--------------------|-----|-----|----|----|----|-------|----|-----|----------------|------------|---|
|                    |     |     |    |    |    |       |    |     | RES_MEAS_CHSEL | LEAK_CHSEL |   |
|                    |     |     |    |    |    |       |    |     | 0000 = ch0     | 0000 = ch0 | 15: 0 = low level diag                  |
|                    |     |     |    |    |    |       |    |     | 0001 = ch1     | 0001 = ch1 | 14: 0 = ISRC = 40 mA                    |
|                    |     |     |    |    |    |       |    |     | 0010 = ch2     | 0010 = ch2 | 13: 1 = pull-down curr. OFF all ch      |
| \$38 LPDIAGREQ     | (I) | w   | 0  | 0  | 1  | 10    | 1  | 00  | 0011 = ch3     | 0011 = ch3 | 12, 11: 10 = bypass (RES_MEAS_CH) ON,   |
| QUO EI BII (GI LEG | (., | ··· |    |    |    | 10    |    |     | 0100 = ch4     | 0100 = ch4 | OFF the others                          |
|                    |     |     |    |    |    |       |    |     | 0101 = ch5     | 0101 = ch5 | 10: 1 = ISINK (RES_MEAS_CH) ON, OFF the |
|                    |     |     |    |    |    |       |    |     | 0110 = ch6     | 0110 = ch6 | others                                  |
|                    |     |     |    |    |    |       |    |     | 0111 = ch7     | 0111 = ch7 | 9, 8: 00 = VRCM not connected           |
|                    |     |     |    |    |    |       |    |     | 1000 = ch8     | 1000 = ch8 |   |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE

The second step of the measurement is the read out of the voltage between SFx and SRx, named resistance into ADC addressing.

This measurement considers the leakage that may be present on the SFx and SRx pins.

As the previous measurement, also this is readable by the microcontroller, via a 10-bit ADC, through the same dedicated request.

The registers to be read are still the four DIAGCTRL\_X.

Once read the ADC measurement, to obtain the value it is necessary to consider the divider ratio of the ADC. In case of resistance x, it is 1:1.

In LPDIAGSTAT it is possible to verify on which channel the resistance measurement has been performed (see the Table 35):

Table 35. Squib resistance measurements (second step) - LPDIAGSTAT register

|     |        |       |    |    | (1) | (2) | 15:12          | 11:8       | 7:4        | 3:0        |                        |
|-----|--------|-------|----|----|-----|-----|----------------|------------|------------|------------|------------------------|
|     | \$37 L | SSTAT | -  |    | R   |     | RES_MEAS_CHSEL |            | LEAK_CHSEL |            |                        |
| (3) | 19     | 18    | 17 | 16 |     | R   |                | 0000 = ch0 |            | 0000 = ch0 |                        |
|     |        |       |    |    |     |     |                | 0001 = ch1 |            | 0001 = ch1 |                        |
|     |        |       |    |    |     |     |                | 0010 = ch2 |            | 0010 = ch2 |                        |
|     |        |       |    |    |     |     | Х              | 0011 = ch3 | x          | 0011 = ch3 | 19: 0 = low level diag |
|     |        |       |    |    |     |     | ^              | 0100 = ch4 | ^          | 0100 = ch4 | 19. 0 – low level diag |
|     | 0      | 0     | 0  | 0  |     |     |                | 0101 = ch5 |            | 0101 = ch5 |                        |
|     |        |       |    |    |     |     |                | 0110 = ch6 |            | 0110 = ch6 |                        |
|     |        |       |    |    |     |     |                | 0111 = ch7 |            | 0111 = ch7 |                        |
|     |        |       |    |    |     |     |                | 1000 = ch8 |            | 1000 = ch8 |                        |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Having the microcontroller these two measurements (that are two voltage drops across SF and SR), the squib resistance is so calculated:

$$\Delta V_{OUT} = (SFx - SRx)_1 - (SFx - SRx)_2 \tag{3}$$

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$$R_{SQUIB} = \frac{\Delta V_{OUT}}{G * ISRC} \tag{4}$$

With:

- G = 5.25 ± 2% (differential amplifier gain)
- ISRC = 40 mA ± 5%

Immediately after the ADC read-out, ISRC is automatically switched OFF to reduce the power consumption.

#### **Example:**

- ADC<sub>1ST CONVERSION</sub> = 0b0100111000 = 312
- ADC<sub>2ND CONVERSION</sub> = 0b0010000001 = 129
- $\Delta_{ADC} = 312 129 = 183$

In order to obtain the result in Volt, being the ADC characteristic linear:

$$2.5 V: 1024 = x: \Delta_{ADC} \rightarrow x = \frac{183 * 2.5 V}{1024} = 0.44 V$$
 (5)

In order to obtain resistance value, considering typical factors:

$$R_{SQUIB} = \frac{x}{G*ISRC} = \frac{0.44 \, V}{5.25*40 \, mA} = 2.1 \, \Omega \tag{6}$$

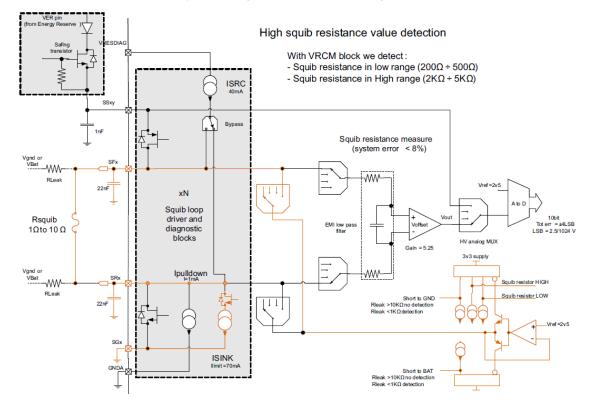
#### 4.1.8 High squib resistance diagnostic

The aim of the test is to understand if the squib resistor is below 200  $\Omega$ , between 500  $\Omega$  and 2 k $\Omega$ , or beyond 5 k $\Omega$ .

In case of a very high squib resistance, there is the possibility to set a lower ISRC current, through the ISRC\_CURR\_SEL bit, bit 14 in the \$LPDIAGREQ register. In this way, ADC maintains a good dynamic.

The Figure 17, referred to ISRC = 40 mA, is true also in case of ISRC = 8 mA.

Figure 17. High squib resistance diagnostic



Through this set-up (see the Figure 17):

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- The ISINK is connected to the SRx.
- The squib is correctly connected between SFx and SRx.
- SRx is internally connected to ISINK that can sink the current.

Note:

In Pyro Fuse Application with channels shorted together, the high squib resistance measurement should be the same on all the channels.

The correspondent set up is done by setting the \$38 LPDIAGREQ properly (see the Table 36).

Table 36. High squib resistance diagnostic - LPDIAGREQ register

|                | (1) | (2) | 15 | 14  | 13 | 12:11 | 10 | 9:8 | 7:4            | 3:0        |  |
|----------------|-----|-----|----|-----|----|-------|----|-----|----------------|------------|--|
|                |     |     |    |     |    |       |    |     | RES_MEAS_CHSEL | LEAK_CHSEL |  |
|                |     |     |    |     |    |       |    |     | 0000 = ch0     | 0000 = ch0 |  |
|                |     |     |    |     |    |       |    |     | 0001 = ch1     | 0001 = ch1 | 15: 0 = low level diag                       |
|                |     |     |    |     |    |       |    |     | 0010 = ch2     | 0010 = ch2 | 14: 0= ISRC = 40 mA, 1 = ISRC = 8 mA         |
|                |     |     |    |     |    |       |    |     | 0011 = ch3     | 0011 = ch3 | 13: 1 = pull-down curr. OFF for all channels |
| \$38 LPDIAGREQ | (1) | W   | 0  | 0/1 | 1  | 00    | 1  | 01  | 0100 = ch4     | 0100 = ch4 | 12, 11: 00 = ISCR OFF for all channels       |
|                |     |     |    |     |    |       |    |     | 0101 = ch5     | 0100 ch4   | 10: 1 = ISINK (RES_MEAS_CH) ON, OFF the      |
|                |     |     |    |     |    |       |    |     |                |            | others                                       |
|                |     |     |    |     |    |       |    |     | 0110 = ch6     | 0110 = ch6 | 9, 8: 01 = VRCM to SFx (LEAK CHSEL)          |
|                |     |     |    |     |    |       |    |     | 0111 = ch7     | 0111 = ch7 | , _ ,  |
|                |     |     |    |     |    |       |    |     | 1000 = ch8     | 1000 = ch8 |  |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE

ISINK and VRCM have to be addressed to the same channel, that means RES\_MEAS\_CHSEL (bit[7:4]) and LEAK CHSEL (bit[3:0]) are equal. If there is a wrong selection in the two fields there is no notice of the mistake.

Through this set-up, the VRCM is connected to SFx and ISINK to SRx. Current flowing through SFx is measured and compared with the ISRlow and ISRhigh (6 mA and 0.7 mA respectively) to identify in which range the resistor measured is.

- HSR HIGH =  $R_{SquibHigh}$  = 2  $k\Omega \div 5 k\Omega$
- HSR LOW =  $R_{SquibLow}$  = 200  $\Omega$  ÷ 500  $\Omega$

In case of low resistance value, as with 2  $\Omega$  load, VRCM sees a path from SRx and GND, so STG (very low impedance towards ground) could be detected (see the Table 37).

Read out of these bits has to be done before the next diagnostic request, because these bits are not latched.

Table 37. High squib resistance diagnostic - LPDIAGSTAT register

|                            |     |    | (1) | (2) | 15:14      | 13 | 12 | 11:8   | 7 | 6   | 5 | 4 | 3:0   |  |
|----------------------------|-----|----|-----|-----|------------|----|----|--|---|-----|---|---|---|--|
| \$37 LPDIA  (3) 19 18  0 0 | 7 1 | 00 |     | RR  | 15:14<br>X | 0  | 12 | 11:8  RES_MEAS_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7  1000 = ch8 | X | 0/1 | X | 1 | 3:0  LEAK_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7  1000 = ch8 | 19: 0 = low level diag 13: 0 = resis < HSR HIGH 1 = resis > HSR HIGH 12: 0 = resis < HSR LOW 1 = resis < HSR LOW 6: STG 1 = STG detected 4: 1 = VRCM to SFx: |

<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

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<sup>2.</sup> R = READ, W = WRITE



3. Further bit over the 16 standard.

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#### 4.1.9 High Side FET diagnostic

The test is possible only in the diagnostic phase.

Before running this test, VRCM has to be previously validated and leakage tests have to be already performed with no fails found. At this point, the HIGH SIDE FET test can be performed.

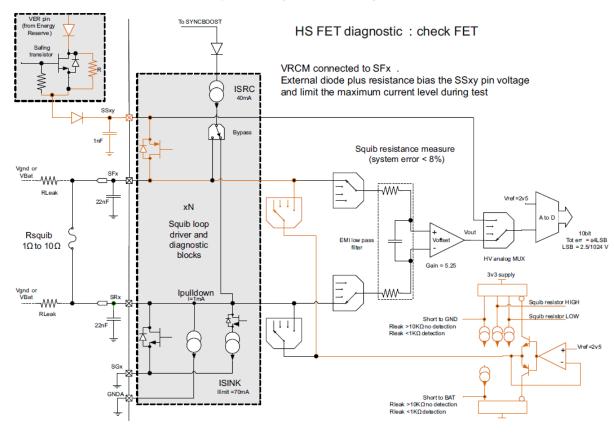


Figure 18. High Side FET diagnostic

ISRC and ISINK are kept off and VRCM is connected to SFx (see the Figure 18) through the LEAK\_CHSEL bits in the the LPDIAGREQ register (see the Table 38). The High Side FET test is enabled through the SYSDIAGREG register.

(1) (2) 15 14 13 12:11 10 9:8 7:4 3:0 RES\_MEAS\_CHSEL LEAK\_CHSEL 0000 = ch00000 = ch00001 = ch10001 = ch115: 0 = low level diag 0010 = ch20010 = ch214: 0 = ISRC = 40 mA 0011 = ch30011 = ch313: 1 = pull-down curr. OFF for all channels \$38 LPDIAGREQ (I) W 0 0 1 00 0 01 12, 11: 00 = ISCR OFF for all channels 0100 = ch40100 = ch410: 0 = ISINK all OFF 0101 = ch50101 = ch50110 = ch60110 = ch69, 8: 01 = VRCM to SFx (LEAK\_CHSEL) 0111 = ch70111 = ch71000 = ch81000 = ch8\$36 SYSDIAGREQ D W X Χ 1 1 0111: DSTEST = HSFET active

Table 38. High Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers

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 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING = no \ i$ 

<sup>2.</sup> R = READ, W = WRITE



#### **Test result**

The High Side FET test turns ON the HS power: if it turns ON correctly, SFx is connected to SSxy which is at VER voltage through the resistor R in parallel to the safing FET.

During the test, the device monitors the current flowing through VRCM.

If the High Side FET works properly, this current exceeds the thresholds  $I_{HSFET}$ , that is 1.8 mA  $\pm$  10%, and the channel is immediately turned off.

In case the current doesn't exceed the limit mentioned, after the time  $T_{FETTIMEOUT}$ , that is 200  $\mu$ s, the test is terminated, and the output is turned off.

During the T<sub>FETTIMEOUT</sub> period, FET activation is flagged through a bit, FETON, readable via SPI.

In any condition, the current in SFx doesn't exceed  $I_{SVRCM}$  ( $I_{LIM\_SRC}$  = -20 ÷ -10 mA and  $I_{LIM\_SNK}$  = 10 ÷ 20 mA), and during the FET test the energy provided to the squib is limited at  $E_{FETtest}$  (< 170  $\mu$ J).

|    |        |      |      |            | (1) | (2) | 15  | 14:12 | 11:8   | 7 | 6 | 5 | 4 | 3:0  |  |
|----|--------|------|------|------------|-----|-----|-----|-------|--|---|---|---|---|--|--|
|    | \$37 L | PDIA | GSTA | <b>Λ</b> Τ |     | R   |     |       | RES_MEAS_CHSEL   |   |   |   |   | LEAK_CHSEL   |  |
| (3 | 0 0    | 0    | 0    | 0          |     | R   | 0/1 | x     | 0000 = ch0<br>0001 = ch1<br>0010 = ch2<br>0011 = ch3<br>0100 = ch4<br>0101 = ch5<br>0110 = ch6<br>0111 = ch7<br>1000 = ch8 | 0 | 0 | 1 | 1 | 0000 = ch0<br>0001 = ch1<br>0010 = ch2<br>0011 = ch3<br>0100 = ch4<br>0101 = ch5<br>0110 = ch6<br>0111 = ch7<br>1000 = ch8 | 19: 0 = low level diag 15: 0 = FET OFF during diag 7: 0 = no short between loops 1 = FET ON during diag 6: 0 = STG not detected 5: 1 = STB detected 4: 1 = test on SFx |

Table 39. High Side FET diagnostic - LPDIAGSTAT register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Possible results for High Side FET test are (see the Table 39):

- STB = 1 and STG = 0 → ok.
- STB = 0 or STG = 1 → missing SSxy connection during FET test, or High Side not switched ON, or short to GND during FET test.

STG and STB, after FET test, are latched. They are cleared through a new LPDIAGREQ or a new SYSDIAGREQ.

Note:

- If VRCM is not previously connected to the SFx and the test is run, a dangerous condition could happen.
- In case of SRx shorted to GND, when the HS is turned ON, even if the current flowing through the squib is greater than IHSFET, the HS is not immediately turned off and the current flows through the squib until T<sub>FETTIMEOUT</sub> expires. This could determine an undesired deployment.

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#### 4.1.10 Low Side FET diagnostic

The test is possible only in the diagnostic phase.

Before running this test, VRCM has to be previously validated and leakage tests have to be already performed with no fails found. At this point, the LOW SIDE FET test can be performed.

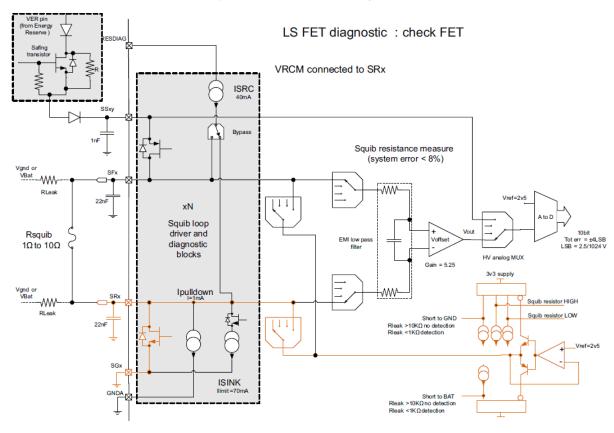


Figure 19. Low Side FET diagnostic

ISRC and ISINK are kept off and VRCM is connected to SRx (see the Figure 19) through the LEAK\_CHSEL bits in the LPDIAGREG register (see the Table 40). The Low Side FET test is enabled through the SYSDIAGREG register.

(1) (2) 15 14 13 12:11 10 9.8 7:4 3:0 RES\_MEAS\_CHSEL LEAK\_CHSEL 0000 = ch00000 = ch00001 = ch10001 = ch115: 0 = low level diag 0010 = ch20010 = ch214: 0 = ISRC = 40 mA 0011 = ch30011 = ch313: 1 = pull-down curr. OFF for all channels \$38 LPDIAGREQ (I) W 0 0 1 00 0 01 12. 11: 00 = ISCR OFF for all channels 0100 = ch40100 = ch410: 0 = ISINK all OFF 0101 = ch50101 = ch50110 = ch60110 = ch69, 8: 01 = VRCM to SFx (LEAK\_CHSEL) 0111 = ch70111 = ch71000 = ch81000 = ch8\$36 SYSDIAGREQ D W X  $X \mid X$  $X \mid X$ 0 0 0 1000: DSTEST = LSFET active

Table 40. Low Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers

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 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING = no \ i$ 

<sup>2.</sup> R = READ, W = WRITE



#### **Test result**

The Low Side FET test turns ON the LS power: if it turns ON correctly, SRx is connected to SGxy. During the test, the device monitors the current flowing through VRCM.

If the Low Side FET works properly, this current exceeds the thresholds  $I_{HSFET}$ , that is 1.8 mA  $\pm$  10%, and the channel is immediately turned off.

In case the current doesn't exceed the limit mentioned, after the time  $T_{FETTIMEOUT}$ , that is 200  $\mu$ s, the test is terminated, and the output is turned off.

During the T<sub>FETTIMEOUT</sub> period, FET activation is flagged through a bit, FETON, readable via SPI.

In any condition, the current in SRx doesn't exceed  $I_{SVRCM}$  ( $I_{LIM\_SRC}$  = -20 ÷ -10 mA and  $I_{LIM\_SNK}$  = 10 ÷ 20 mA), and during the FET test the energy provided to the squib is limited at  $E_{FETtest}$  (< 170  $\mu$ J).

|         |      |      |    | (1) | (2) | 15  | 14:12 | 11:8   | 7 | 6 | 5 | 4 | 3:0  |  |
|---------|------|------|----|-----|-----|-----|-------|--|---|---|---|---|--|--|
| \$37 LF | PDIA | GSTA | AΤ |     | R   |     |       | RES_MEAS_CHSEL   |   |   |   |   | LEAK_CHSEL   |  |
| 0       | 0    | 0    | 0  |     | R   | 0/1 | X     | 0000 = ch0<br>0001 = ch1<br>0010 = ch2<br>0011 = ch3<br>0100 = ch4<br>0101 = ch5<br>0110 = ch6<br>0111 = ch7<br>1000 = ch8 | 0 | 1 | 0 | 0 | 0000 = ch0<br>0001 = ch1<br>0010 = ch2<br>0011 = ch3<br>0100 = ch4<br>0101 = ch5<br>0110 = ch6<br>0111 = ch7<br>1000 = ch8 | 19: 0 = low level diag 15: 0 = FET OFF during diag 7: 0 = no short between loops 1 = FET ON during diag 6: 1 = STG detected 5: 0 = STB not detected 4: 0 = test on SRx |

Table 41. Low Side FET diagnostic - LPDIAGSTAT register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Possible results for Low Side FET test are (see the Table 41):

- STB = 0 and STG =  $1 \rightarrow ok$
- STB = 1 or STG = 0 → short to battery in Low Side, or Low Side not switched ON.

STG and STB, after FET test, are latched. They are cleared through a new LPDIAGREQ or a new SYSDIAGREQ.

Note:

- Ground loss (SGxy) is not detected through FET test because there is a diode between SGxy and the substrate.
- If VRCM is not previously connected to the SRx and the test is run, a dangerous condition could happen.
- In case of SFx shorted to SSxy, when the LS is turned ON, even if the current flowing through the squib is greater than I<sub>LSFET</sub>, the LS is not immediately turned off and the current flows through the squib until T<sub>FETTIMEOUT</sub> expires. This could determine an undesired deployment.
- In case of SRx shorted to SSxy, when the LS is turned ON, even if the current flowing through it is greater than I<sub>LSFET</sub>, the LS not immediately turned off and the current flows until T<sub>FETTIMEOUT</sub> expires. Such a high current could damage the LS power.

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## 4.1.11 Loss of ground

This test is based on the voltage of the ground pin, SGxy, during the squib resistor measurement or the High Side driver diagnostic.

Any voltage shift of the SGxy pin over  $V_{SGopen}$ , that is 400 to 800 mV, is considered loss of ground, readable in the LP\_GNDLOSS register (see the Table 42).

Table 42. Loss of ground - LP\_GNDLOSS register

|     |         |      |      |    | (1) | (2) | 15:8 | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |   |
|-----|---------|------|------|----|-----|-----|------|-----|-----|-----|-----|-----|-----|-----|-----|---|
|     | \$26 LF | P_GN | DLOS | S  |     | R   |      |     |     |     |     |     |     |     |     | 0 = no loss of ground                       |
| (3) | 19      | 18   | 17   | 16 |     | R   | 0    | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | 0 = no loss of ground<br>1 = loss of ground |
|     | 0       | 0    | 0    | 0  |     |     |      |     |     |     |     |     |     |     |     | 1 1000 of ground                            |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

GNDLOSSx is set considering t<sub>SGopen</sub> filter time (46 to 50 µs) and it is cleared upon read.

Four GND pins are available: SG01, SG23, SG45 and SG67. The IC is able to detect GND loss on CHx or CHy basing on the channel selected.

## 4.1.12 Safing FET diagnostic

The aim of the test is to verify the SSxy voltage level.

SSxy voltages are readable by the microcontroller through the ADC converter in the \$3X DIAGCTRL\_x registers (see the Table 43).

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|     |    |    |    |                   | (1) | (2) | 15 | 14  | 13   | 12  | 11                          | 10 | 9 | 8   | 7  | 6   | 5          | 5 4                                     | 3  | :                                | 2   | 1    | 0 |                             |
|-----|----|----|----|-------------------|-----|-----|----|-----|--|---|-----------------------------|----|---|-----|----|-----|------------|---|--|----------------------------------|---|------|---|-----------------------------|
|     | 9  |    |    | CTRL_X<br>s, C, D | -   | W   | ×  | ×   | ×  | x   | ×                           | ×  | X | Х   | X  |     |            | \$25<br>\$3<br>\$3<br>\$3<br>\$3<br>\$3 | = V<br>86 = 37 = 88 = 89 = 84 = 85 = 85 = 85 = 85 = 85 = 85 = 85 | SY<br>SS<br>SS<br>SS<br>SS<br>SS | 'NC<br>60<br>61<br>62<br>63<br>64<br>65<br>66 |      |   |                             |
| (3) | 19 | 18 | 17 | 16                |     |     |    |     |  |   |                             |    |   |     |    |     |            |   |  |                                  |   |      |   | 19: 1 = conversion finished |
|     | 1  | 0  | 0  | ADCREQ_X          | -   | R   |    | \$2 | 25 = \<br>\$36 = \<br>\$37 = \<br>\$38 = \<br>\$39 = \<br>\$3A = \<br>\$3B = \<br>\$3C = \ | REQ_<br>VSYN<br>= SS0<br>= SS1<br>= SS2<br>= SS3<br>= SS4<br>= SS5<br>= SS6 | IC<br>)<br>2<br>3<br>4<br>5 |    |   | ADC | RE | Q_) | <b>X</b> 1 | 0 b                                     | it AE  | ос                               | res   | sult | t |                             |

Table 43. Safing FET diagnostic - DIAGCTRL\_X register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Once read the ADC measurement, to obtain the voltage value it is necessary to consider the divider ratio of the ADC. In case of SSxy, it is 15:1.

#### 4.1.13 Deployment time diagnostic

The aim of the test is to pass to the microcontroller the deploy time information that the IC has stored with the previous SPI commands.

This test is possible only in DIAG state.

Table 44. Deployment time diagnostic - SYSDIAGREQ register

|                 | (1) | (2) | 15:8 | 7:4 | 3 | 2 | 1 | 0 |  |
|-----------------|-----|-----|------|-----|---|---|---|---|--|
| \$36 SYSDIAGREQ | D   | W   | Х    |     | 1 | 0 | 0 | 1 | 1001: DSTEST - Output timing on FENL pin |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE

Once the \$36 SYSDIAGREQ register is set for output timing on the FENL pin check, even if the test has been performed, it is not possible any modification in the deployment channel configuration (\$06 DCR0, \$07 DCR1, \$08 DCR2, \$09 DCR3 registers).

This feature prevents any modification in the deployment time and deployment current after the test has been performed and, therefore, it is no longer visible by the microcontroller.

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To modify again the deployment channel configuration (\$06 DCR0, \$07 DCR1, \$08 DCR2, \$09 DCR3 registers) it is first necessary to change the DSTEST request, and secondly to modify the deployment channel configuration itself as previously done.

#### **Test result**

Once the test is ongoing, a signal 0 V  $\rightarrow$  5 V/3.3 V (depending on VCC) is output on the FENL pin, which reports in sequence, from channel 0 to channel 7, the deployment time programmed, with a 8 ms delay between each channel. Starting from ch0, the FENL signal is high for the deploy time of ch0; then it remains low until the next pulse corresponding to the channel 1 occurs (8 ms delay between each pulse to start); the same happens up to channels 7.

The microcontroller can test the latest deployment time programmed in the DRCx registers measuring the duration of the high ARM pulse.

If the test is performed on a channel with no deployment time previously configured, the high FENL pulse lasts 8 µs.

If the combination time/current deployment programmed for a channel is wrong, then the combination time/current deployment turns back to the default value. In case the deployment time is monitored through the FENL signal, the default one is output.

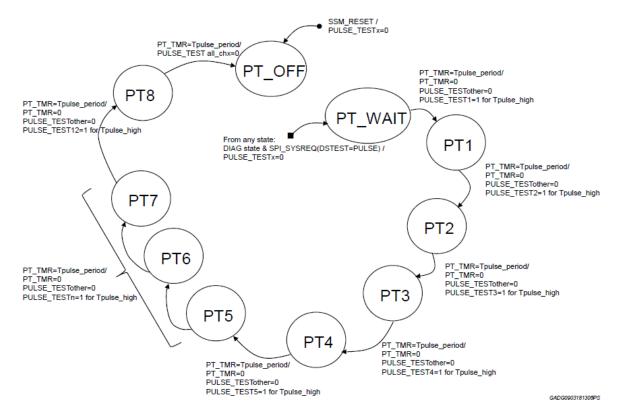


Figure 20. Deployment timer diagnostic sequence

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## 4.2 High level diagnostic

The device performs the measurement, as requested by the microcontroller, through the LPDIAGREQ register.

Based on the requests from the microcontroller, diagnostics run according to the set up described for the low level mode but each test set up is driven step by step by the IC itself.

The IC timing schedule is selected through the HI\_LEV\_DIAG\_TIME bit in INIT (see the Table 45):

Table 45. High level diagnostic

|                   | (1) | (2) | 15 | 14:13 | 12 | 11 | 10 | 9:8 | 7:5  | 4   | 3:0   |   |
|-------------------|-----|-----|----|-------|----|----|----|-----|--|-----|---|---|
| \$01 SYS_CFG      | I   | W   |    | X     | X  | X  | 0  |     |  |     |   | 10: HI_LEV_DIAG_TIME 0 = short time 1 = long time       |
| \$38<br>LPDIAGREQ | (1) | W   | 1  | X     | X  | X  | X  | ×   | HIGH_LEVEL_DIAG_SEL  000 = No diag sel  001 = VRCM Check  010 = Leakage Check  011 = Short Btw Loops Check  100 = Unused  101 = resistance range check  110 = resistance measurement  111 = FET test | SQP | LOOP_DIAG_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6  0111 = ch7  1000 = ch8 | 15: 1 = high level diag<br>4: SQP<br>0 = SRx<br>1 = SFx |

<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

In case of high level diagnostic selection, the IC automatically schedules the preparatory tasks to be eventually run in order to perform the required diagnostic.

The flow chart in the Figure 21 shows the time sequence implemented:

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<sup>2.</sup> R = READ, W = WRITE

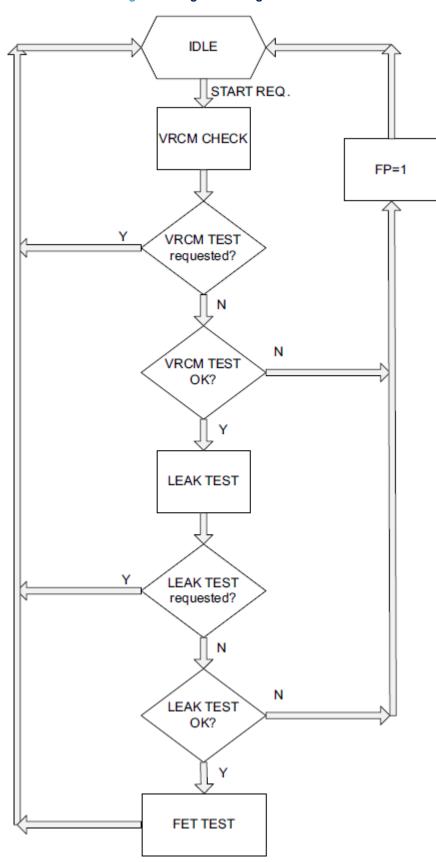


Figure 21. High level diagnostic flow

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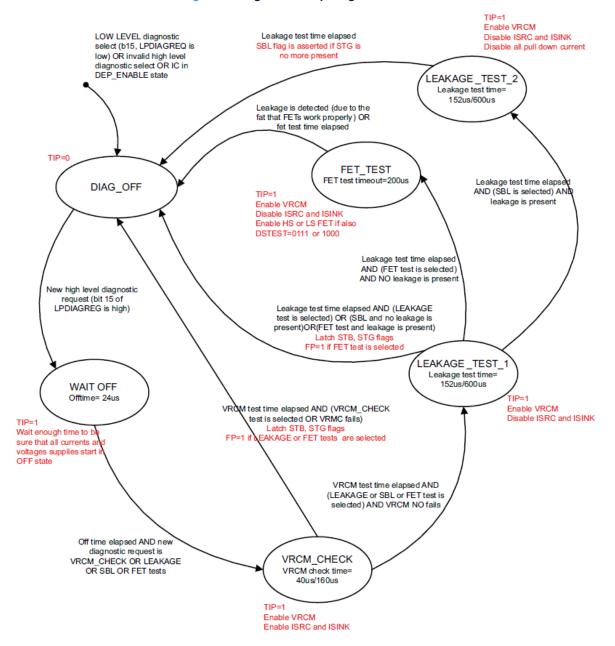


The FP bit in the LPDIAGSTAT register is available only in case of high level diagnostic selected. It is stuck at 0 otherwise.

Once a test which requires preliminary measurement phases is selected (i.e. leakage test and FET test), this bit is set if the diagnostic procedure has been stopped because of a fault recorded in such a preliminary step.

Two diagnostic flows are implemented, as shown in the Figure 22 and Figure 23:

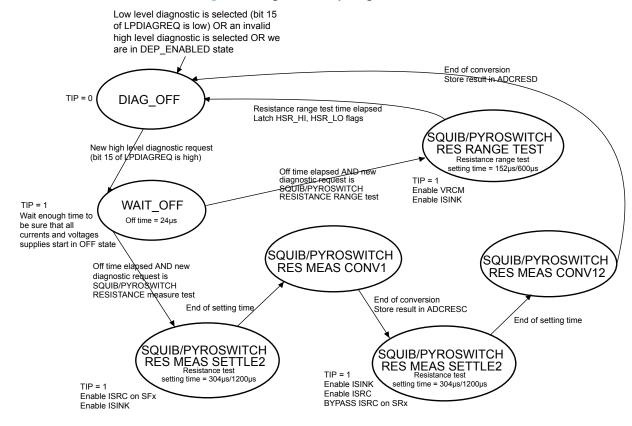
Figure 22. High level loop diagnostic flow 1



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Figure 23. High level loop diagnostic flow 2



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## 4.2.1 VRCM check - High Side

HS FET diagnostic: check VRCM functionality First we use ISRC current generator to check VRCM block ISRC SSx Вура Squib resistance measure (system error < 8%) WW Vref=2v5 χN A to D Squib loop 10bit Rsquib driver and Tot err = ±4LSB LSB = 2.5/1024 V 1Ωto 10Ω diagnostic blocks HV analog MUX Gain = 5.25 3v3 supply Vgnd or VBat lpulldown Squib resistor HIGH Short to GND Rleak >10KΩ no detection Rleak <1KΩ detection Squib resistor LOW 111 ISINK Short to BAT Rleak >10KΩ no detection Rleak <1KΩ detection

Figure 24. VRCM check - High Side (Diagnostic)

The correspondent set up (see the Figure 24) is done by setting the \$38 LPDIAGREQ register properly (see the Table 46).

15 14:8 7:5 4 3:0 LOOP DIAG CHSEL 0000 = ch00001 = ch10010 = ch2HIGH\_LEVEL\_DIAG\_SEL SQP 0011 = ch315: 1 = high level diag \$38 LPDIAGREQ Χ (l) W 1 001 = VRCM Check 0100 = ch44: 1 = SFx 1 0101 = ch50110 = ch60111 = ch71000 = ch8

Table 46. VRCM check, High Side - LPDIAGREQ register

The result of the diagnostic is readable in the \$37 LPDIAGSTAT register (see the Table 47) and shown in the Figure 25.

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<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

<sup>2.</sup> R = READ, W = WRITE



|     |      |      |      |     | (1) | (2) | 15:12 | 11:8                | 7 | 6 | 5 | 4 | 3:0        |                                    |
|-----|------|------|------|-----|-----|-----|-------|---------------------|---|---|---|---|------------|------------------------------------|
| \$  | 37 L | PDIA | GST/ | AT. |     | R   |       |                     |   |   |   |   | LEAK_CHSEL |                                    |
| (3) | 19   | 18   | 17   | 16  |     | R   |       |                     |   |   |   |   | 0000 = ch0 |                                    |
|     |      |      |      |     |     |     |       |                     |   |   |   |   | 0001 = ch1 | 19: 1 = high level diag            |
|     |      |      |      |     |     |     |       |                     |   |   |   |   | 0010 = ch2 | 18: 1 = high level diag is running |
|     |      |      |      |     |     |     | X     | HIGH_LEVEL_DIAG_SEL | 0 | 0 | 1 | 1 | 0011 = ch3 | 7: 0 = no short between loops      |
|     |      |      |      |     |     |     | ^     | 0001 = VRCM Check   | U | U | ' | ' | 0100 = ch4 | 6: 0 = STG not detected            |
|     | 1    | 0/1  | 0    | 0   |     |     |       |                     |   |   |   |   | 0101 = ch5 | 5: 1 = STB detected                |
|     |      |      |      |     |     |     |       |                     |   |   |   |   | 0110 = ch6 | 4: 1 = SFx                         |
|     |      |      |      |     |     |     |       |                     |   |   |   |   | 0111 = ch7 |                                    |
|     |      |      |      |     |     |     |       |                     |   |   |   |   | 1000 = ch8 |                                    |

Table 47. VRCM check, High Side - LPDIAGSTAT register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

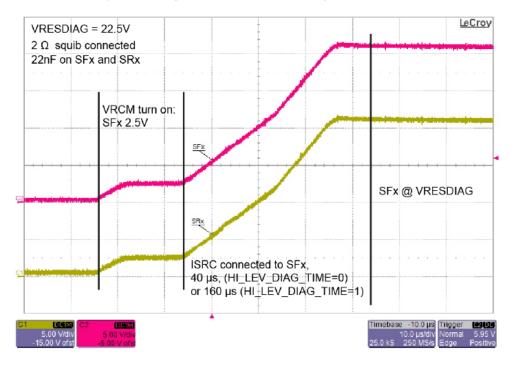


Figure 25. Diagnostic - VRCM check - High Side waveform

 $\label{lem:controller} \mbox{VRCM check, once required, is not run one shot on both HS and LS, but the microcontroller selects through the SQP bit the High Side or the Low Side.}$ 

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#### 4.2.2 VRCM check - Low Side

LS FET diagnostic: check VRCM functionality Second we use ISINK current generator to check VRCM block ISRC Bypass Squib resistance measure (system error < 8%) Vgnd or VBat -WW χN A to D Squib loop driver and Rsquib Tot err = ±4LSB LSB = 2.5/1024 V 1Ω to 10Ω diagnostic blocks HV analog MUX Gain = 5.25 3v3 supply Vgnd or VBat Ipulldown Squib resistor HIGH Short to GND Rleak >10KΩ no detection Rleak <1KΩ detection Squib resistor LOW 11 ISINK

Figure 26. VRCM check - Low Side (Diagnostic)

The correspondent set up (see the Figure 26) is done by setting the \$38 LPDIAGREQ register properly (see the Table 48).

(1) (2) 15 LOOP\_DIAG\_CHSEL 0000 = ch00001 = ch10010 = ch2HIGH\_LEVEL\_DIAG\_SEL SQP 0011 = ch315: 1 = high level diag \$38 LPDIAGREQ **(l)** W 1 Х 001 = VRCM Check 0100 = ch44: 0 = SRx 0 0101 = ch50110 = ch60111 = ch71000 = ch8

Table 48. VRCM check, Low Side - LPDIAGREQ register

Being ISRC and VRCM connected to SFx, if VRCM works correctly, short to battery, readable in the \$37 LPDIAGSTAT register, is asserted for the channel selected (see the Table 49).

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<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

<sup>2.</sup> R = READ, W = WRITE

|     |       |      |      |    | (1) | (2) | 15:12 | 11:8                | 7 | 6 | 5 | 4 | 3:0        |                                    |
|-----|-------|------|------|----|-----|-----|-------|---------------------|---|---|---|---|------------|------------------------------------|
| \$  | 37 LI | PDIA | GSTA | λT |     | R   |       |                     |   |   |   |   | LEAK_CHSEL |                                    |
| (3) | 19    | 18   | 17   | 16 |     | R   |       |                     |   |   |   |   | 0000 = ch0 |                                    |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 0001 = ch1 | 19: 1 = high level diag            |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 0010 = ch2 | 18: 1 = high level diag is running |
|     |       |      |      |    |     |     | Х     | HIGH_LEVEL_DIAG_SEL | 0 | 1 | 0 | 0 | 0011 = ch3 | 7: 0 = no short between loops      |
|     |       | 014  |      |    |     |     | ^     | 0001 = VRCM Check   | 0 | ' | U | U | 0100 = ch4 | 6: 1 = STG detected                |
|     | 1     | 0/1  | 0    | 0  |     |     |       |                     |   |   |   |   | 0101 = ch5 | 5: 0 = STB not detected            |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 0110 = ch6 | 4: 0 = SRx                         |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 0111 = ch7 |                                    |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 1000 = ch8 |                                    |

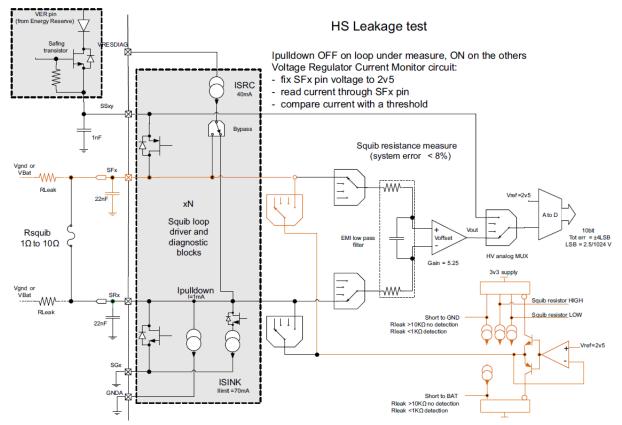
Table 49. VRCM check, Low Side - LPDIAGSTAT register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

VRCM check, once required, is not run one shot on both HS and LS, but the microcontroller selects through the SQP bit the High Side or the Low Side.

## 4.2.3 Leakage test - High Side

Figure 27. Leakage test - High Side (Diagnostic)



The correspondent set up (see the Figure 27) is done by setting the \$38 LPDIAGREQ register properly (see the Table 50).

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|                 |     |     |    |      |                     |     | •               |                         |
|-----------------|-----|-----|----|------|---------------------|-----|-----------------|-------------------------|
|                 | (1) | (2) | 15 | 14:8 | 7:5                 | 4   | 3:0             |                         |
|                 |     |     |    |      |                     |     | LOOP_DIAG_CHSEL |                         |
|                 |     |     |    |      |                     |     | 0000 = ch0      |                         |
|                 |     |     |    |      |                     |     | 0001 = ch1      |                         |
|                 |     |     |    |      |                     |     | 0010 = ch2      |                         |
| ¢20 I DDIA CDEO | //\ | W   | 1  | X    | HIGH_LEVEL_DIAG_SEL | SQP | 0011 = ch3      | 15: 1 = high level diag |
| \$38 LPDIAGREQ  | (1) | VV  | '  | ^    | 010 = leakage test  | 1   | 0100 = ch4      | 4: 1 = SFx              |
|                 |     |     |    |      |                     |     | 0101 = ch5      |                         |
|                 |     |     |    |      |                     |     | 0110 = ch6      |                         |
|                 |     |     |    |      |                     |     | 0111 = ch7      |                         |
|                 |     |     |    |      |                     |     | 1000 = ch8      |                         |

Table 50. Leakage test, High Side - LPDIAGREQ register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE

The result of the diagnostic is readable in the \$37 LPDIAGSTAT register (see the Table 51).

(1) (2) 15:12 11:8 7 6 5 4 3:0 R LEAK\_CHSEL \$37 LPDIAGSTAT 0000 = ch0(3) 19 18 17 16 R 0001 = ch119: 1 = high level diag 0010 = ch218: 1 = high level diag is running HIGH\_LEVEL\_DIAG\_SEL 0011 = ch37: 0 = no short between loops Χ 0 0 0 1 010 = LEAKAGE Check 0100 = ch46: 0 = STG not detected 1 0/1 0 0 0101 = ch55: 0 = STB not detected 0110 = ch64: 1 = SFx 0111 = ch71000 = ch8

Table 51. Leakage test, High Side - LPDIAGSTAT register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Depending on the value of the capacitors mounted on the ECU, the same high level diagnostic can be performed setting the HI\_LEV\_DIAG\_TIME bit in order to increase the time of the internal diagnostic finite state machine operation (see the Figure 28 and Figure 29).

This bit can be written only in INIT state.

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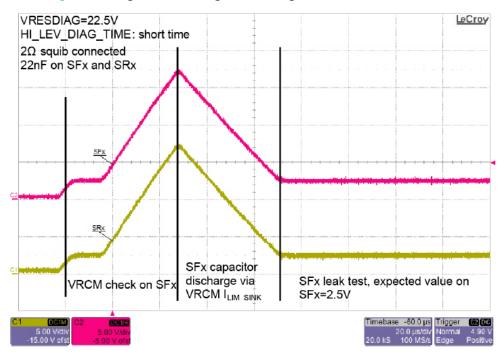


Figure 28. Diagnostic - Leakage check - High Side waveform, short time



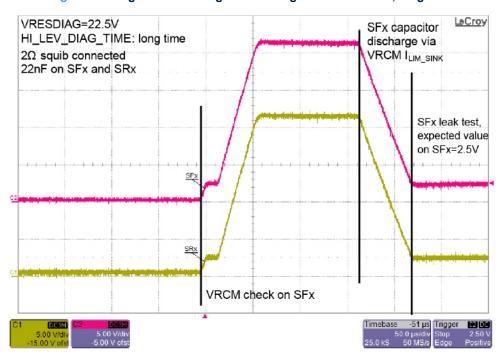


Table 52. Leakage test, High Side - SYS\_CFG register

|              | (1) | (2) | 15:13 | 12 | 11 | 10 | 9:1 | 0 |  |
|--------------|-----|-----|-------|----|----|----|-----|---|--|
| \$01 SYS_CFG | I   | W   |       | Х  |    | 1  |     |   | 10: HI_LEV_DIAG_TIME 0 = short time, 1 = long time |

 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING$ 

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<sup>2.</sup> R = READ, W = WRITE

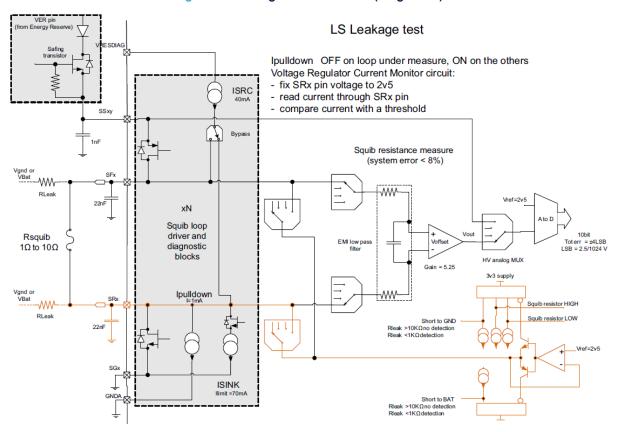


Note:

In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all the channels.

#### 4.2.4 Leakage test - Low Side

Figure 30. Leakage test - Low Side (Diagnostic)



The correspondent set up (see the Figure 30) is done by setting the \$38 LPDIAGREQ register properly (see the Table 53).

(1) (2) 15 14:8 7:5 3:0 4 LOOP\_DIAG\_CHSEL 0000 = ch00001 = ch10010 = ch2HIGH\_LEVEL\_DIAG\_SEL SQP 0011 = ch315: 1 = high level diag \$38 LPDIAGREQ (l) W 1 Χ 0100 = ch44: 0 = SRx 010 = leakage test 0 0101 = ch50110 = ch60111 = ch71000 = ch8

Table 53. Leakage test, Low Side - LPDIAGREQ register

The result of the diagnostic is readable in the \$37 LPDIAGSTAT register (see the Table 54):

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<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

<sup>2.</sup> R = READ, W = WRITE



Table 54. Leakage test, Low Side - LPDIAGSTAT register

|     |       |      |      |    | (1) | (2) | 15:12 | 11:8                | 7 | 6 | 5 | 4 | 3:0        |                                    |
|-----|-------|------|------|----|-----|-----|-------|---------------------|---|---|---|---|------------|------------------------------------|
| \$  | 37 LI | PDIA | GSTA | ΑT |     | R   |       |                     |   |   |   |   | LEAK_CHSEL |                                    |
| (3) | 19    | 18   | 17   | 16 |     | R   |       |                     |   |   |   |   | 0000 = ch0 |                                    |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 0001 = ch1 | 19: 1 = high level diag            |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 0010 = ch2 | 18: 1 = high level diag is running |
|     |       |      |      |    |     |     | x     | HIGH_LEVEL_DIAG_SEL | 0 | 0 | 0 | 0 | 0011 = ch3 | 7: 0 = no short between loops      |
|     |       |      |      |    |     |     | ^     | 010 = LEAKAGE Check | U | U | U | U | 0100 = ch4 | 6: 0 = STG not detected            |
|     | 1     | 0/1  | 0    | 0  |     |     |       |                     |   |   |   |   | 0101 = ch5 | 5: 0 = STB not detected            |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 0110 = ch6 | 4: 0 = SRx                         |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 0111 = ch7 |                                    |
|     |       |      |      |    |     |     |       |                     |   |   |   |   | 1000 = ch8 |                                    |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Note:

In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all the channels.

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#### 4.2.5 Short between loops

The correspondent set up is done by setting the \$38 LPDIAGREQ properly (see the Table 55).

Table 55. Short between loops - LPDIAGREQ register

|                | (1) | (2) | 15 | 14:8 | 7:5                      | 4   | 3:0             |                         |
|----------------|-----|-----|----|------|--------------------------|-----|-----------------|-------------------------|
|                |     |     |    |      |                          |     | LOOP_DIAG_CHSEL |                         |
|                |     |     |    |      |                          |     | 0000 = ch0      |                         |
|                |     |     |    |      |                          |     | 0001 = ch1      |                         |
|                |     |     |    |      |                          |     | 0010 = ch2      |                         |
| \$38 LPDIAGREQ | (1) | w   | 1  | X    | HIGH_LEVEL_DIAG_SEL      | SQP | 0011 = ch3      | 15: 1 = high level diag |
| 400 EI DIAGILE | (1) |     | '  |      | 011 = short between loop | 0/1 | 0100 = ch4      | 4: 0 = SRx, 1 = SFx     |
|                |     |     |    |      |                          |     | 0101 = ch5      |                         |
|                |     |     |    |      |                          |     | 0110 = ch6      |                         |
|                |     |     |    |      |                          |     | 0111 = ch7      |                         |
|                |     |     |    |      |                          |     | 1000 = ch8      |                         |

<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

The result of the diagnostic is readable in the \$37 LPDIAGSTAT register (see the Table 56).

Table 56. Short between loops - LPDIAGSTAT register

|     |                 |     | (1) | (2) | 15:12 | 11:8 | 7 | 6                   | 5                        | 4 | 3:0 |            |                     |                                    |                         |
|-----|-----------------|-----|-----|-----|-------|------|---|---------------------|--------------------------|---|-----|------------|---------------------|------------------------------------|-------------------------|
| \$  | \$37 LPDIAGSTAT |     |     | ΑT  |       | R    |   |                     |                          |   |     |            | LEAK_CHSEL          |                                    |                         |
| (3) | 19              | 18  | 17  | 16  |       | R    |   |                     |                          |   |     |            | 0000 = ch0          |                                    |                         |
|     |                 |     |     |     |       |      |   | HIGH_LEVEL_DIAG_SEL | 0                        | 0 |     |            | 0001 = ch1          | 19: 1 = high level diag            |                         |
|     |                 |     |     |     |       |      |   |                     |                          |   |     |            | 0010 = ch2          | 18: 1 = high level diag is running |                         |
|     |                 |     |     |     |       |      | x |                     |                          |   | 0   | 0/1        | 0011 = ch3          | 7: 0 = no short between loops      |                         |
|     |                 | 014 |     | 0 0 |       |      |   | ^                   | 011 = short between loop | U |     | U          | 0/1                 | 0100 = ch4                         | 6: 0 = STG not detected |
|     | 1               | 0/1 | 0 0 |     |       |      |   |                     |                          |   |     |            | 0101 = ch5          | 5: 0 = STB not detected            |                         |
|     |                 |     |     |     |       |      |   |                     |                          |   |     | 0110 = ch6 | 4: 0 = SRx, 1 = SFx |                                    |                         |
|     |                 |     |     |     |       |      |   |                     |                          |   |     |            | 0111 = ch7          |                                    |                         |
|     |                 |     |     |     |       |      |   |                     |                          |   |     |            | 1000 = ch8          |                                    |                         |

 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING$ 

Note:

In Pyro Fuse Application with channels shorted together, the short to ground should be a real short of SRx or SFx pin to GND. Moreover, a short to ground on a channel will be present on all the others.

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<sup>2.</sup> R = READ, W = WRITE

<sup>2.</sup> R = READ, W = WRITE

<sup>3.</sup> Further bit over the 16 standard.



## 4.2.6 Squib resistance range

High squib resistance value detection With VRCM block we detect: - Squib resistance in low range (200Ω ÷ 500Ω) - Squib resistance in High range (2KΩ ÷ 5KΩ) ISRC Squib resistance measure (system error < 8%) W χN A to D Sauib loop Rsquib driver and Tot err = ±4LSB LSB = 2.5/1024 V 1Ω to 10Ω diagnostic blocks HV analog MUX Gain = 5.25 3v3 supply **Ipulldown** Squib resistor HIGH -WV Short to GND Rleak >10KΩ no detection Rleak <1KΩ detection ISINK Short to BAT Rleak >10KΩ no detection Rleak <1KΩ detection

Figure 31. Squib resistance range (Diagnostic)

The correspondent set up (see the Figure 31) is done by setting the \$38 LPDIAGREQ register properly (see the Table 57).

(1) (2) 15 14:8 7:5 4 3:0 LOOP\_DIAG\_CHSEL 0000 = ch00001 = ch10010 = ch215: 1 = high level diag HIGH\_LEVEL\_DIAG\_SEL 0011 = ch3**SQP** \$38 LPDIAGREQ **(l)** W 1 Х 0100 = ch44: 1 = SFx 101 = squib res range 1 0101 = ch50110 = ch60111 = ch71000 = ch8

Table 57. Squib resistance range - LPDIAGREQ register

The result of the diagnostic in case of **2 Ω squib** is readable in the \$37 LPDIAGSTAT register (see the Table 58):

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<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

<sup>2.</sup> R = READ, W = WRITE



|      |      |      |     |    | (1) | (2) | 15:14 | 13 | 12 | 11:8                  | 7 | 6        | 5 | 4 | 3:0        |                                    |
|------|------|------|-----|----|-----|-----|-------|----|----|-----------------------|---|----------|---|---|------------|------------------------------------|
| \$37 | 7 LF | PDIA | GST | AT |     | R   |       |    |    |                       |   |          |   |   | LEAK_CHSEL |                                    |
| (3)  | 19   | 18   | 17  | 16 |     | R   |       |    |    |                       |   |          |   |   | 0000 = ch0 | 19: 1 = high level diag            |
| +    |      |      |     |    |     |     | -     |    |    |                       |   |          |   |   | 0001 = ch1 | 18: 1 = high level diag is running |
|      |      |      |     |    |     |     |       |    |    |                       |   |          |   |   | 0010 = ch2 | 13: 0 = HSR meas < HSR HIGH value  |
|      |      |      |     |    |     |     | x     | 0  | 1  | HIGH_LEVEL_DIAG_SEL   | 0 | 1        | 0 | 1 | 0011 = ch3 | 12: 1 = HSR meas < HSR LOW value   |
|      |      | 0/4  |     |    |     |     | ^     |    | '  | 101 = squib res range | 0 | <b>'</b> | U | ' | 0100 = ch4 | 7: 0 = no short between loops      |
|      | 1    | 0/1  | 0   | 0  |     |     |       |    |    |                       |   |          |   |   | 0101 = ch5 | 6: 1 = STG detected                |
|      |      |      |     |    |     |     |       |    |    |                       |   |          |   |   | 0110 = ch6 | 5: 0 = STB not detected            |
|      |      |      |     |    |     |     |       |    |    |                       |   |          |   |   | 0111 = ch7 | 4: 1 = SFx                         |
|      |      |      |     |    |     |     |       |    |    |                       |   |          |   |   | 1000 = ch8 |                                    |

Table 58. Squib resistance range - LPDIAGSTAT register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

The results could be the following:

- STG = 1 → the squib has a very low resistive value.
- SQP = 1 → VRCM is connected to the High Side.

Note: In Pyro Fuse Application with channels shorted together, the high squib resistance measurement should be the same on all the channels.

#### 4.2.7 Squib resistance measurement

The IC allows measuring the squib resistance value in the range of 1  $\div$  10  $\Omega$  with overall 8% precision.

Two steps of the measurement, described in the Figure 32 and Figure 33, are managed by the IC, which also makes ADC conversion results available.

Note: In Pyro Fuse Application with channels shorted together, the squib resistance measurement should be the same on all the channels.

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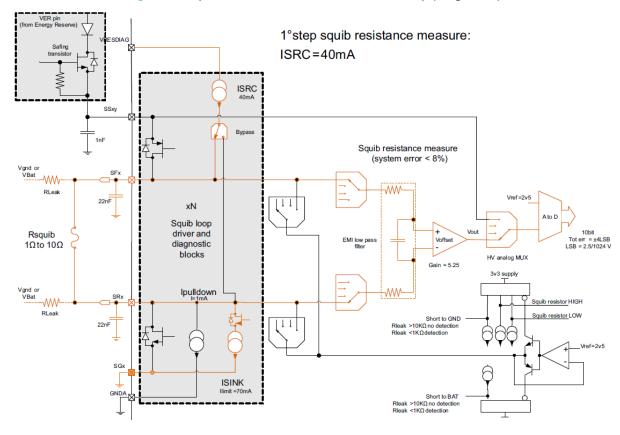
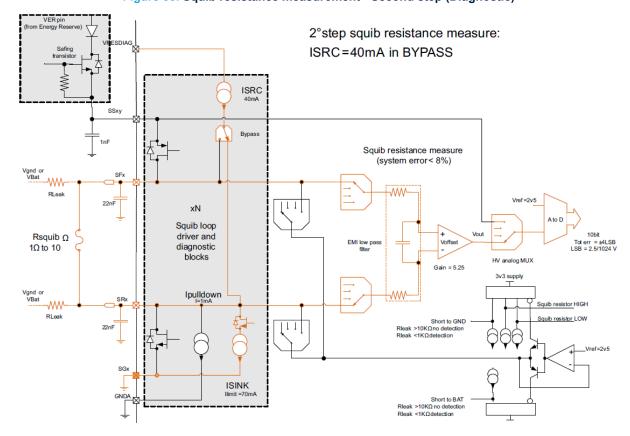


Figure 32. Squib resistance measurement - First step (Diagnostic)

Figure 33. Squib resistance measurement - Second step (Diagnostic)



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The correspondent set up is done by setting the \$38 LPDIAGREQ properly (see the Table 59).

|                | (1) | (2) | 15 | 14:8 | 7:5                   | 4 | 3:0             |                         |  |
|----------------|-----|-----|----|------|-----------------------|---|-----------------|-------------------------|--|
|                |     |     |    |      |                       |   | LOOP_DIAG_CHSEL |                         |  |
|                |     |     |    |      |                       |   | 0000 = ch0      |                         |  |
|                |     |     |    |      |                       |   | 0001 = ch1      |                         |  |
|                |     |     |    |      |                       |   | 0010 = ch2      |                         |  |
| \$38 LPDIAGREQ | (1) | W   | 1  | X    | HIGH_LEVEL_DIAG_SEL   | × | 0011 = ch3      | 15: 1 = high level diag |  |
| \$30 LPDIAGREQ | (1) | VV  | '  | ^    | 110 = squib res range |   | 0100 = ch4      | 15. T – High lever diag |  |
|                |     |     |    |      |                       |   | 0101 = ch5      |                         |  |
|                |     |     |    |      |                       |   | 0110 = ch6      |                         |  |
|                |     |     |    |      | 0111 = ch7            |   |                 |                         |  |
|                |     |     |    |      |                       |   | 1000 = ch8      |                         |  |

Table 59. Squib resistance measurement - LPDIAGREQ register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE

The IC triggers at the end of each step above an ADC conversion. Once the high level diagnostic has been performed, results of ADC conversions have to be read in the registers \$3C, \$3D DIAGCTRL\_X by selection of SQUIB resistance measurement (bit [6:0] = \$06).

The result of the first conversion,  $ADC_{1ST\ CONVERSION}$ , is stored in \$3C DIAGCTRL\_C. Instead, the result of the second conversion,  $ADC_{2ND\ CONVERSION}$ , is stored in \$3D DIAGCTRL\_D.

Once read the ADC measurement, to obtain the value it is necessary to consider the divider ratio of the ADC. In case of resistance x, it is 1:1.

Being two measurements, the squib resistance is so calculated:

$$\Delta V_{OUT} = (SFx - SRx)_1 - (SFx - SRx)_2 \tag{7}$$

$$R_{SQUIB} = \frac{\Delta V_{OUT}}{G * ISRC} \tag{8}$$

With:

- G = 5.25 ± 2% (differential amplifier gain)
- ISRC = 40 mA ± 5%

#### **Example:**

- ADC<sub>1ST CONVERSION</sub> = 0b0100111000 = 312
- ADC<sub>2ND CONVERSION</sub> = 0b0010000001 = 129
- $\Delta_{ADC} = 312 129 = 183$

In order to obtain the result in Volt, being the ADC characteristic linear:

$$2.5 V: 1024 = x: \Delta_{ADC} \rightarrow x = \frac{183 * 2.5 V}{1024} = 0.44 V$$
 (9)

In order to obtain resistance value, considering typical factors:

$$R_{SQUIB} = \frac{x}{G*ISRC} = \frac{0.44 \, V}{5.25*40 \, mA} = 2.1 \, \Omega \tag{10}$$

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## 4.2.8 High Side FET diagnostic

The test is possible only in the diagnostic phase.

Before running this test, the IC validates VRCM, then performs leakage test and in case of no failures, High Side FET test is performed.

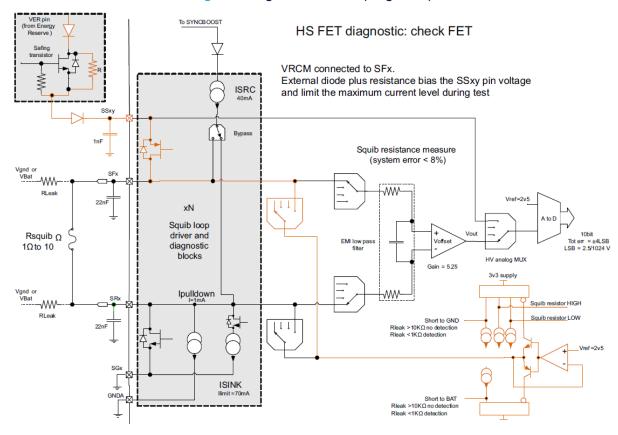


Figure 34. High Side FET test (Diagnostic)

The correspondent set up (see the Figure 34) is done by setting the \$38 LPDIAGREQ and \$36 SYSDIAGREQ registers (see the Table 60).

(1) (2) 15 14:8 7:5 3:0 4 LOOP\_DIAG\_\_CHSEL 0000 = ch00001 = ch10010 = ch2RES\_MEAS\_CHSEL SQP 0011 = ch315: 0 = high level diag \$38 LPDIAGREQ (I) W Χ 1 4: 1 = SFx 111 = FET test 1 0100 = ch40101 = ch50110 = ch60111 = ch71000 = ch8\$36 SYSDIAGREQ D W X Χ 0 1 1 0111: DSTEST = HSFET active

Table 60. High Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers

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 $<sup>1. \</sup>quad I = INIT, \ D = DIAG, \ S = SAFING, \ A = ARMING, \ - = ALL \ STATES, \ (I) = no \ in \ INIT, \ (D) = no \ in \ DIAG, \ (S) = no \ in \ SAFING, \ (A) = no \ in \ ARMING$ 

<sup>2.</sup> R = READ, W = WRITE



The High Side FET test turns ON the HS power: if it turns ON correctly, SFx is connected to SSxy which is at VER voltage through the resistor R in parallel to the safing FET.

During the test, the device monitors the current flowing through VRCM.

If the High Side FET works properly, this current exceeds the thresholds  $I_{HSFET}$ , that is 1.8 mA  $\pm$  10%, and the channel is immediately turned off.

In case the current does not exceed the limit mentioned, after the time  $T_{FETTIMEOUT}$ , that is 200  $\mu$ s, the test is terminated, and the output is turned off.

The result of the diagnostic is readable in the \$37 LPDIAGSTAT register (see the Table 61):

(1) (2) 15 14:12 11.8 7 6 5 4 3:0 \$37 LPDIAGSTAT R LEAK\_CHSEL 0000 = ch019 18 17 16 R 19: 1 = high level diag 0001 = ch118: 1 = high level diag is running 0010 = ch215: 1 = FET ON during diag 0011 = ch3RES\_MEAS\_CHSEL 0 0 1 1 0/1 Х 7: 0 = no short between loops 111 = FET test 0100 = ch46: 0 = STG not detected 1 0/1 0 0 0101 = ch55: 1 = STB detected 0110 = ch64: 1 = SFx 0111 = ch7 1000 = ch8

Table 61. High Side FET diagnostic - LPDIAGSTAT register

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Possible results for High Side FET test are:

- STB = 1 and STG =  $0 \rightarrow ok$ .
- STB = 0 or STG = 1 → missing SSxy connection during FET test, or High Side not switched ON, or short to GND during FET test.

STG and STB, after FET test, are latched. They are cleared through a new LPDIAGREQ or a new SYSDIAGREQ.

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#### 4.2.9 Low Side FET diagnostic

Before running this test, IC validates VRCM, then performs leakage test and in case of no failures, Low Side FET test is performed.

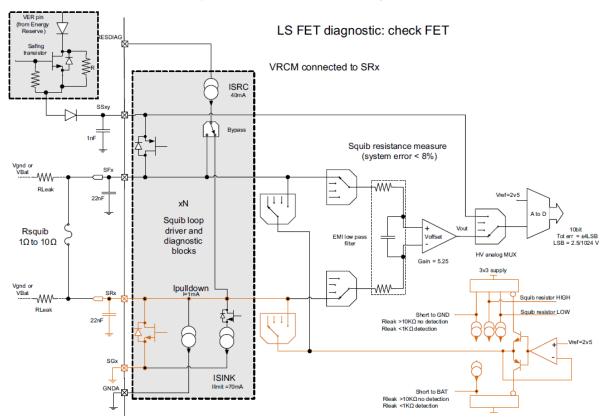


Figure 35. Low Side FET test (Diagnostic)

The orrespondent set up (see the Figure 35) is done by setting the \$38 LPDIAGREQ and \$36 SYSDIAGREQ registers (see the Table 62).

(1) (2) 15 14:8 7:5 3:0 LOOP\_DIAG\_\_CHSEL 0000 = ch00001 = ch10010 = ch2RES\_MEAS\_CHSEL SQP 0011 = ch315: 0 = high level diag \$38 LPDIAGREQ (I) W 1 Х 111 = FET test 0 0100 = ch44: 0 = SRx 0101 = ch50110 = ch60111 = ch71000 = ch80 0 \$36 SYSDIAGREQ D W Х Х 1000: DSTEST = LSFET active

Table 62. Low Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers

Low Side FET test turns ON the Low Side. If the Low Side turns ON correctly, SRx is connected to SGxy.

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<sup>1.</sup> I = INIT, D = DIAG, S = SAFING, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING

<sup>2.</sup> R = READ, W = WRITE



During the test, the device monitors the current flowing through VRCM.

If the FET works properly, this current exceeds the thresholds  $I_{LSFET}$ , that is 450  $\mu$ A  $\pm$  10%, and the channel is immediately turned off.

In case the current doesn't exceed the limit mentioned, after the time  $T_{FETTIMEOUT}$ , that is 200  $\mu$ s, the test is terminated, and the output is turned off.

The result of the diagnostic is readable in the \$37 LPDIAGSTAT register (see the Table 63).

Table 63. Low Side FET diagnostic - LPDIAGSTAT register

| \$37 LPDIAGSTAT R  (3) 19 18 17 16 R  O/1 X 0 1  RES_MEAS_CHSEL 111 = FET test  O 1 0 0   LEAK_CHSEL   0000 = ch0   0001 = ch1   0010 = ch2   0011 = ch3   0100 = ch4   0101 = ch5   0110 = ch6   0110 = ch6   0110 = ch6   0110 = ch6   0111 = ch7   0 = SRx |    |    |    | (1) (2) 15 14 1 |     |   | 13 | 12 | 11:8 | 7 | 6              | 5 | 4 | 3:0 |  |  |   |
|---|----|----|----|-----------------|-----|---|----|----|------|---|----------------|---|---|-----|--|--|---|
|   | 19 | 18 | 17 | 16              | (1) | R |    |    |      |   | RES_MEAS_CHSEL |   | 1 |     |  | LEAK_CHSEL  0000 = ch0  0001 = ch1  0010 = ch2  0011 = ch3  0100 = ch4  0101 = ch5  0110 = ch6 | 18: 1 = high level diag is running 15: 1 = FET ON during diag 7: 0 = no short between loops 6: 1 = STG detected 5: 0 = STB not detected |

- 1. I = INIT, D = DIAG, S = SAFING, A = ARMING, = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (A) = no in ARMING
- 2. R = READ, W = WRITE
- 3. Further bit over the 16 standard.

Possible results for Low Side FET test are:

- STB = 0 and STG =  $1 \rightarrow ok$
- STB = 1 or STG =  $0 \rightarrow$  short to battery in Low Side, or Low Side not switched ON.

STG & STB, after FET test, are latched. They are cleared through a new LPDIAGREQ or a new SYSDIAGREQ.

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# 5 Optimized application circuit

In the scenario of only one channel deployment, the application can be further simplified by:

- Connecting the SSxy directly to battery.
- Not using Remote Sensor interface.

In this case there is a consistent reduction in BOM cost, paying a loss in Safety level.

Table 64. Simplified BOM

| Component | Тур | Unit | Requirement | Notes                 |
|-----------|-----|------|-------------|-----------------------|
| C1a       | 100 | nF   | 35 V        | VSYNC input capacitor |
| C1b       | 2.2 | μF   | 35 V        | VSYNC input capacitor |
| C2a       | 100 | nF   | 25 V        | VSAT input capacitor  |
| C2b       | 2.2 | μF   | 25 V        | VSAT input capacitor  |
| СЗа       | 100 | nF   | 16 V        | VCC input capacitor   |
| C3b       | 2.2 | μF   | 16 V        | VCC input capacitor   |
| C4        | 100 | nF   | 16 V        | CVDD capacitor        |
| C5        | 10  | nF   | 25 V        | SS01 capacitor        |
| C9        | 22  | nF   | 25 V        | SF0 capacitor         |
| C17       | 22  | nF   | 25 V        | SR0 capacitor         |

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# **Revision history**

Table 65. Document revision history

| Date        | Version | Changes   |
|-------------|---------|---|
| 09-Nov-2021 | 1       | Initial release.  |
| 20-May-2024 | 2       | <ul> <li>Updated:</li> <li>Figure 1. Application circuit;</li> <li>Figure 23. High level loop diagnostic flow 2.</li> <li>Minor text changes in Section 4.2.3: Leakage test - High Side.</li> </ul> |
| 22-Jul-2025 | 3       | Figure 1. Application circuit and Table 64. Simplified BOM updated.   |

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