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Application note

WSS operation with ST L9396

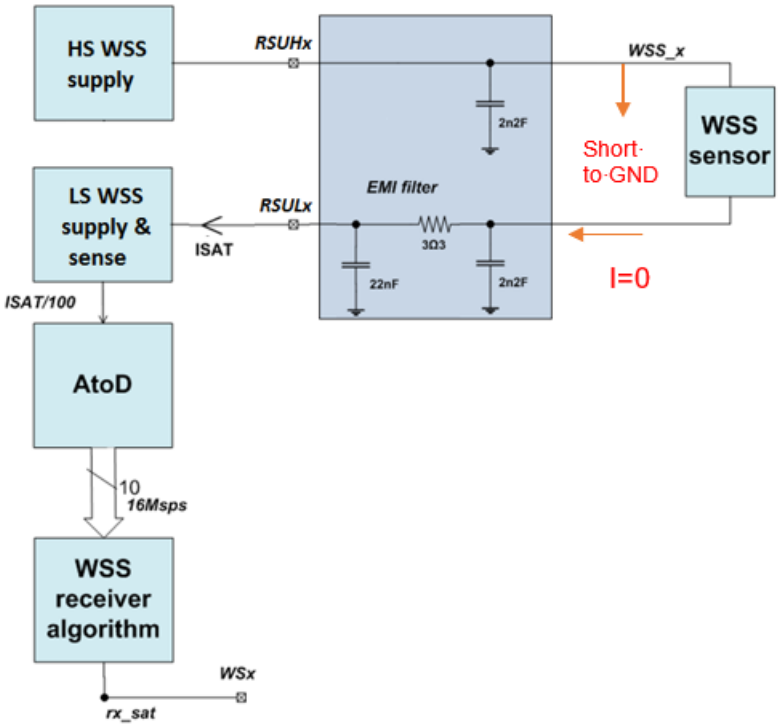
Introduction

This document is intended as an integration of the specification for wheel speed sensor interface (WSI) also referred as RSI (remote sensor interface). This document contains all the information needed to configure and enable each channel for a specific sensor type. In addition, the threshold evaluation formulas is reported and explained. All the involved registers are shown and several binary configuration examples are proposed. Moreover, a guideline to configure the WSI for all the wheel speed sensor (WSS) types has been drawn up.

1 ST L9396 wheel speed sensor interface (WSI)

L9396 is able to decode the signals coming from wheel speed sensor through an analog current sensing which works together with a fast ADC and a logic control unit, which allows to modulate the speed information on the WSOx pin. A simplified block diagram is shown in Figure 1.

Figure 1. WSI block scheme



The IC is able to operate with several sensors, in particular the following one have been considered:

- Standard active 2-level sensor (7/14 mA): Allegro ATS682LSH
- PWM encoded 2-level sensor (7/14 mA, 1 edge per tooth): Allegro ATS651LSH
- PWM encoded 2-level sensor (7/14 mA, 2 edges per tooth): Infineon TLE4942, BOSCH DF11
- VDA compliant 3-level sensor (7/14/28 mA): Philips KMI22/1

Each sensor is either able to provide simple information related to the speed of the rotating wheel through a frequency variation of the output-current signal (STD) or is able to provide further diagnostic through a duty cycle modulation (PWMs) or Manchester encoder (VDA). WSS that fits last description is also called AMR-based (see Note). Referring to AMR technology, the four available WSS types can be classified as follows:

- VDA compliant, 3-level WSS are AMR-based;
- PWM encoded, 2-level, 2 edges/tooth WSS are AMR-based;
- PWM encoded, 2-level, 1 edge/tooth WSS are not AMR-based;
- Standard active 2-level WSS are not AMR-based.

Note: AMR stands for “automated meter reading”. This technology includes all the sensing solutions that give not only a measure of a specific physical phenomenon, but also provide diagnostic information about the sensor itself to guarantee data reliability.

2 WSI registers

In this paragraph, the registers involved in normal operation and testing of the device are listed and described. Each register is characterized by a 7-bit address to be accessible via SPI; it can be readable/writable depending by its function in the WSI operation. Any data field has been filled according to this format:

- “0b” prefix indicates a binary configuration;
- “0x” prefix indicates a hexadecimal value;
- “0” indicates that all bits of the data field are set to ‘0’, regardless of the coding and of the data field length.

2.1 Sensor control register (RS_CTRL)

The RS_CTRL register stores remote sensor control field. The main properties of the register are hereby listed:

- Address: 0001011;
- Type: read/write.

Table 1. RS_CTRL register description

Data field	Description	Reset value	Reset event
Bit 5	INIT: allow access to all the configuration registers, including WSICTRL [0…3] data field. 0 => access denied 1 => access granted	0	SSM_RESET, LBIST
Bit 4	DIAG: allow access to WSITEST register. 0 => access denied 1 => access granted	0	SSM_RESET, LBIST
Bit [0..3]	CHxEN: channel “x”(1) output (DOUT) enable. 0 => DOUTx disabled 1 => DOUTx enabled	0x0	SSM_RESET, LBIST

1. *x = <data_field_index> +1.*

2.2 Sensor configuration registers (RS_CFG_0_1 and RS_CFG_2_3)

The RS_CFG_0_1 register stores the settings for channels 1 and 2. Any interface is configured by a 10-bit data field. The main properties of the register are hereby listed:

- Address: 00001100;
- Type: read/write.

Table 2. WSIRSCR0 register description

Data field	Description	Reset value	Reset event
Bit [16…19]	WSFILT[0…3]: WSO2 deglitch filter time selection. 0x0 => 8 µs 0xF => 15.5 µs LSB = 500 ns	0x2	SSM_RESET, LBIST
Bit 15	WSIPTEN: channel 2 pass-through mode enable (valid only for PWM encoded, 2 edges/tooth sensors). 0 => Pass-through disabled 1 => Pass-through enabled	0	SSM_RESET, LBIST

Data field	Description	Reset value	Reset event
Bit 14	SSDIS: WSO2 output disabled in case of standstill condition (valid only for PWM encoded, 2 edges/tooth sensors). 0 => WSO2 enabled during standstill 1 => WSO2 disabled during standstill	0	SSM_RESET, LBIST
Bit 13	WSI_FIX_THRESH: selection of fixed or auto-adjusting threshold algorithm for channel 2. 0 => auto-adaptive thresholds 1 => fixed thresholds	0	SSM_RESET, LBIST
Bit 12	DON'T CARE	0	SSM_RESET, LBIST
Bit 10-11	STS: sensor type selection for channel 2. 00 => two level, standard 01 => three level, VDA 10 => two level, PWM encoded, 2 edges/tooth 11 => two level, PWM encoded, 1 edge/tooth	0b00	SSM_RESET, LBIST
Bit [6…9]	WSFILT[0…3]: WSO1 deglitch filter time selection. 0x0 => 8 µs 0xF => 15.5 µs LSB = 500 ns	0x2	SSM_RESET, LBIST
Bit 5	WSIPTEN: channel 1 pass-through mode enable (valid only for PWM encoded sensors). 0 => Pass-trhough disabled 1 => Pass-through enabled	0	SSM_RESET, LBIST
Bit 4	SSDIS: DOUT1 output disabled in case of standstill condition (valid only for PWM encoded, 2 edges/tooth sensors). 0 => WSO1 enabled during standstill 1 => WSO1 disabled during standstill	0	SSM_RESET, LBIST
Bit 3	WSI_FIX_THRESH: selection of fixed or auto-adjusting threshold algorithm for channel 1. 0 => auto-adaptive thresholds 1 => fixed thresholds	0	SSM_RESET, LBIST
Bit 2	DON'T CARE	0	SSM_RESET, LBIST
Bit 0-1	STS: sensor type selection for channel 1. 00 => two level, standard 01 => three level, VDA 10 => two level, PWM encoded, 2 edges/tooth 11 => two level, PWM encoded, 1 edge/tooth	0b00	SSM_RESET, LBIST

The RS_CFG_2_3 register stores the settings for channels 3 and 4. Any interface is configured by a 10-bit data field. The main properties of the register are hereby listed:

- Address: 0001101;
- Type: read/write.

For register description, refer to Table 2. The [0…9] data field is related to channel 3, while the [10…19] accounts for channel 4.

For the deglitch time evaluation formula, refer to Section 4.3 .

2.3 WSI fixed thresholds configuration register (RS_AUX_CFG)

The RS_AUX_CFG register stores the parameters needed for calculating the fixed thresholds. The main properties of the register are hereby listed:

- Address: 0001110;
- Type: read/write.

Table 3. WSIAUXCONF register description

Data field	Description	Reset value	Reset event
Bit 18-19	DON'T CARE	0b00	SSM_RESET, LBIST
Bit [10…17]	WSI_OFFS_TH[0…7]: offset from first threshold in case of fixed thresholds algorithm selected. 0x00 => 4.968 mA 0xFF => 28.428 mA LSB = 92 µA	0x34	SSM_RESET, LBIST
Bit 8-9	DON'T CARE	0b00	SSM_RESET, LBIST
Bit [0…7]	WSI_FIRST_TH[0…7]: low threshold setting in case of fixed thresholds algorithm selected. 0x00 => 4.968 mA 0xFF => 28.428 mA LSB = 92 µA	0x33	SSM_RESET, LBIST

For the fixed thresholds evaluation formulas, refer to Section 4.1 .

2.4 WSI channel test register (WSS_TEST)

The WSS_TEST register stores static test configurator bit field. A static test for a selected channel output can be executed through this register. This is usually done at start-up in order to verify DOUTx signal integrity and detect eventual "stuck at" conditions. The main properties of the register are hereby listed:

- Address: 0001111;
- Type: read/write.

Table 4. WSITEST register description

Data field	Description	Reset value	Reset event
Bit [2…8]	Configuration range: select one WSOx output according to the following binary configuration 1010011 => WSO4 output 1010101 => WSO3 output 1011001 => WSO2 output 1010110 => WSO1 output All other configurations => test mode disabled	0b0000000	SSM_RESET, LBIST
Bit 1	DON'T CARE	0	SSM_RESET, LBIST
Bit 0	WSSTP: WSOx output test value. 0 => output for selected WSOx set 'high' 1 => output for selected WSOx set 'low'	0	SSM_RESET, LBIST

2.5 WSI base current and first swing registers (RS_DATA_RSDR_4…7)

The RS_DATA_RSDR_4 register stores the base current (I_{B0}) and the first swing (ΔI_{TH1}) values for channel 1. The auto-adjusting thresholds algorithm uses these measures to update the threshold (I_{TH1} and I_{TH2}) position. The main properties of the register are hereby listed:

- Address: 0010100;
- Type: read only.

Table 5. RS_DATA_RSDR4…7 register description

Data field	Description	Reset value	Reset event
Bit [10…19]	First swing (ΔI_{TH1})	0b0001001100	SSM_RESET, LBIST
Bit [0…9]	Base current (I_{B0})	0b0001001100	SSM_RESET, LBIST

The base current and first swing registers of the other channels only differ from the previous for the address.

The channel 2 (RS_DATA_RSDR_5) main properties of the register are hereby listed (for register description, refer to Table 5):

- Address: 0010101;
- Type: read only.

The channel 3 (RS_DATA_RSDR_6) main properties of the register are hereby listed (for register description, refer to Table 5):

- Address: 0010110;
- Type: read only.

The channel 4 (*RS_DATA_RSDR_7*) main properties of the register are hereby listed (for register description, refer to Table 5):

- Address: 0010111;
- Type: read only.

2.6 WSI second swing registers (RS_DATA_RSDR_8…11)

The RS_DATA_RSDR_8 register stores the second swing (ΔI_{TH2}) value for channel 1. The auto-adjusting thresholds algorithm uses this measure to update the second threshold (I_{TH2}) position.

The main properties of the register are hereby listed:

- Address: 00110000;
- Type: read only.

Table 6. RS_DATA_RSDR_8…11 register description

Data field	Description	Reset value	Reset event
Bit [0…9]	Second swing (ΔI_{TH2})	0b0010010111	SSM_RESET, LBIST

The second swing registers of the other channels only differ from the previous for the address.

The channel 2 (RS_DATA_RSDR_9) main properties of the register are hereby listed (for register description, refer to Table 6):

- Address: 00110001;
- Type: read only.

The channel 3 (RS_DATA_RSDR_10) main properties of the register are hereby listed (for register description, refer to Table 6):

- Address: 00110010;
- Type: read only.

The channel 4 (RS_DATA_RSDR_11) main properties of the register are hereby listed (for register description, refer to Table 6):

- Address: 00110011;
- Type: read only.

2.7 WSI sensor and fault data register

The sensor data and fault information are contained in five registers: the sensor and fault data registers (RS_DATA_RSDR0…3) and the LS fault register (RSU_STATUS).

The first set of registers gives information on both data and fault occurring on HS/LS (see the relative bit description) while the second one contains information on LS only.

2.7.1 RS_DATA_RSDR0…3

The RS_DATA_RSDR0 register stores information about the sensor data and status on channel 1. Data fields can have different meanings depending on the selected sensor type. Fault interpretation is the same for all WSS types instead. This register features also a dedicated CRC (cyclic redundancy check) field in order to prevent communication errors and to allow data integrity check.

The main properties of the register are hereby listed:

- Address: 0010000;
- Type: read only.

Table 7. Sensor data register description during normal operation (FLT = 0)

Data field	Description	Reset value	Reset event
Bit [17…19]	CRC[0…2]: CRC checksum. This value is calculated processing the [0…16] data field according to Equation 1.	Depends on the channel number (LCID)	SSM_RESET, LBIST
Bit 16	STDSTL: standstill indication (valid only for VDA and PWM encoded, 2 edges/tooth, WSS) 0 => standstill not detected 1 => standstill detected	0	SSM_RESET, LBIST
Bit 15	FLT: fault status. The data fields of the register can assume different meanings depending on the value of this bit. 0 => fault not detected 1 => fault detected (see Table 8)	1 (see Note 4.)	SSM_RESET, LBIST
Bit 14	Latch_DO: latched D0. Set when bit 0 has been decoded high in any of previous messages (valid only for VDA sensors). 0 => no faults in previous messages 1 => a prior data frame contained a fault	0	SSM_RESET, LBIST
Bit 12-13	LCID[0…1]: logical channel ID. 00 => channel 1 01 => channel 2 10 => channel 3 11 => channel 4	Depends on the channel number	SSM_RESET, LBIST

Data field	Description	Reset value	Reset event
Bit 0-11	DATA: data from wheel speed data decoder. These data fields can assume different formats. • VDA data format: – DATA[8…11]: Data bit counter. Stores the number of data bit available in the DATA[0…7] field. – DATA[0…7]: Data field. Contains the sensor message. • PWM data format: – DATA[9…11]: Not used. – DATA[0…8] pulse data bit: pulse length is encoded in this field with 5 µs typical resolution. • STD data format: field not used. The “FLT -> NODATA” condition is flagged.	See Note 4.	SSM_RESET, LBIST

When a fault occurs, bit 15 (FLT) is set and the data fields of the register must be interpreted in a different way, as shown in Table 8.

Table 8. Sensor data register description during fault occurrence (FLT = 1)

Data field	Description	Reset value	Reset event
Bit [17…19]	CRC[0…2]: CRC checksum. This value is calculated processing the [0…16] data field according to Equation 1.	Depends on the channel number (LCID)	SSM_RESET, LBIST
Bit 16	Not used.	0	SSM_RESET, LBIST
Bit 15	FLT: fault status. The data fields of the register can assume different meanings depending on the value of this bit. 0 => fault not detected 1 => fault detected	1 (see Note 4.)	SSM_RESET, LBIST
Bit 14	ON/OFF: channel on/off status. Cleared when STG bit is set together with the WSITEMP bit or when the channel is commanded off in the WSICTRL register. Set in all other faulty cases. 0 => channel is shutdown 1 => channel is powered on	0	SSM_RESET, LBIST
Bit 12-13	LCID[0…1]: logical channel ID. 00 => channel 1 01 => channel 2 10 => channel 3 11 => channel 4	Depends on the channel	SSM_RESET, LBIST
Bit 10-11	Not used.		SSM_RESET, LBIST
Bit 9	STG: short to ground. Set when current on RSUHx pin exceeds $I_{LIMTHHS}$ for a time period greater than $t_{ILIMTHHS}$ (see Note 5.). 0 => short to ground not detected 1 => short to ground detected	0	SSM_RESET, LBIST
Bit 8	STB: short to battery. Set when voltage on RSUHx pin increases above VPREREG for a time period greater than t_{STBTH} (see Note 6.). 0 => short to battery not detected	0	SSM_RESET, LBIST

Data field	Description	Reset value	Reset event
	1 => short to battery detected		
Bit 7	CURRENT_HI: leakage to battery. Set when current on RSULx exceeds $I_{THVBATP}$ for a time period greater than t_{FLT_LKG} (see Note 7. and Note10.) 0 => leakage to ground not detected 1 => leakage to ground detected	0	SSM_RESET, LBIST
Bit 6	OPENDET: open detection. Set when current on RSULx stands below I_{THOPEN} for a time period greater than t_{FLT_OPEN} (see Note 8.) 0 => open not detected 1 => open detected	0	SSM_RESET, LBIST
Bit 5	WSITEMP: overtemperature. Set when temperature exceeds T_{SD_TRK} for a time period greater than $t_{SD\_DEGLITCH}$ (see Note 8.). 0 => overtemperature not detected 1 => overtemperature detected	0	SSM_RESET, LBIST
Bit 4	INVALID: invalid data. Set when parity error is detected in VDA sensors' data frame. 0 => parity error not detected 1 => parity error detected	0	SSM_RESET, LBIST
Bit 3	NODATA: empty buffer. Set when the DATA field is empty (see Note 4. and Table 7). 0 => buffer not empty 1 => buffer empty	1	SSM_RESET, LBIST
Bit 2	PULSE OVERFLOW: pulse length overflow. Set when the pulse duration counter overflows (only for PWM sensors). 0 => pulse overflow not detected 1 => pulse overflow detected	0	SSM_RESET, LBIST
Bit 0-1	Not used.	0	SSM_RESET, LBIST

The CRC checksum is calculated implementing the following combinatorial approach:

Equation 1–CRC evaluation formulas

$$\begin{cases} CRC[2] = CRC_{ext}[0] \oplus D[0] \oplus D[1] \oplus D[3] \oplus D[6] \oplus D[7] \oplus D[8] \oplus D[10] \oplus D[13] \oplus D[14] \oplus D[15] \\ CRC[1] = CRC_{ext}[2] \oplus D[0] \oplus D[1] \oplus D[2] \oplus D[4] \oplus D[7] \oplus D[8] \oplus D[9] \oplus D[11] \oplus D[14] \oplus D[15] \oplus D[16] \\ CRC[0] = CRC_{ext}[1] \oplus CRC_{ext}[0] \oplus D[0] \oplus D[2] \oplus D[5] \oplus D[6] \oplus D[7] \oplus D[9] \oplus D[12] \oplus D[13] \oplus D[14] \oplus D[16] \end{cases} \quad (1)$$

In the Equation 1 the initial seeds are represented by the $CRC_{ext}[n]$ terms and are all equal to '1', while D[n] inputs are related to the RS_DATA_RSDR_x[n] generic bit. "XOR" function of a chain (for example $\oplus B \oplus C \oplus D$...) is "true" when an odd number of inputs is true, "false" otherwise.

The CRC checksum can also be evaluated using a polynomial approach with the following parameters for the algorithm:

- Polynomial $g(x) = x^3 + x + 1$, whose hexadecimal equivalent code is "0xB";
- Number of CRC bit: 3;
- Initial seed: all ones;
- Input word length: 17 bit;
- LSB first;
- Additional left shift number: 3.

The algorithm is structured as follows:

1. Shift the 17-bit input word left by 3 bit;
2. Flip the word;
3. Invert first (N-1) bit (see Note 3.);
4. Apply standard CRC evaluation procedure (see Note 4.).

The first three steps are implemented to perform input word preconditioning. An example of CRC evaluation is provided in the Table 9.

- The RS_DATA_RSDR_x register value (CRC included): “0x40900”;
- Input word (register value-excluding CRC data field): “00000100100000000”;

Table 9. Example of CRC evaluation

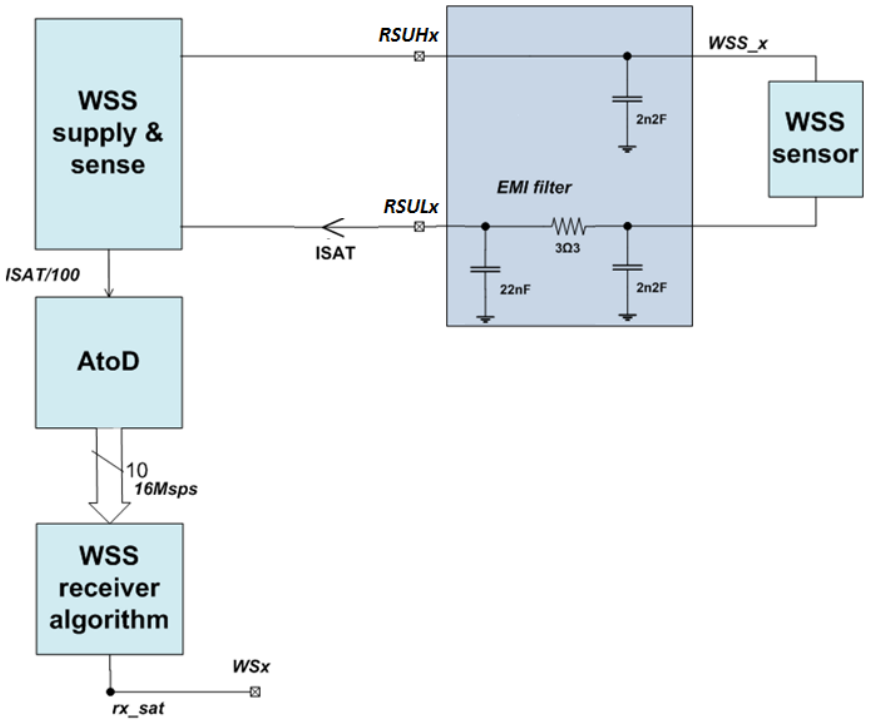
Word computation	Action
00000100100000000	Shift the 17-bit input word left by 3 bit
00000100100000000000	Flip the word
00000000000100100000	Invert first 3 bit
11100000000100100000	Shift the 20-bit input word left by 3 bit (see Note 2.).
11100000000100100000000 10110000000000000000000	XOR and shift polynomial
01010000000100100000000 01011000000000000000000	XOR and shift polynomial
00001000000100100000000 00101100000000000000000	Shift only
00001000000100100000000 00010110000000000000000	Shift only
00001000000100100000000 00001011000000000000000	XOR and shift polynomial
00000110001001000000000 00000101100000000000000	Shift only
00000110001001000000000 00000010110000000000000	XOR and shift polynomial
00000011101001000000000 00000001011000000000000	XOR and shift polynomial
00000000101100100000000 00000000101100000000000	XOR and shift polynomial
00000000000000100000000 00000000010110000000000	Shift only
00000000000000100000000 00000000001011000000000	Shift only
00000000000000100000000 00000000000101100000000	Shift only
00000000000000100000000 00000000000010110000000	Shift only
00000000000000100000000 00000000000001011000000	Shift only

Word computation	Action
00000000000000100000000 00000000000000101100000	XOR and shift polynomial
00000000000000001100000 00000000000000010110000	Shift only
00000000000000001100000 00000000000000001011000	XOR and shift polynomial
00000000000000000111000 00000000000000000101100	XOR and shift polynomial
00000000000000000010100 00000000000000000010110	XOR and shift polynomial
00000000000000000000010 00000000000000000001011	Shift only (end of CRC).
00000000000000000000010	CRC checksum is “010”

Note:

1. *The standard CRC evaluation procedure states that the input word must be initially shifted left by (N-1) bit, where N is the polynomial grade.*
2. *This is due to the CRC init being all ‘1’. N is the polynomial degree.*
3. *The standard CRC calculation procedure needs (M+N-1) steps, being M the length of the input frame and N the polynomial grade.*
4. *The sensor data register is configured in the status “FLT -> NODATA” after a reset event has occurred.*
5. *$I_{LIMTHHS}$ is between 40 mA and 60 mA and $t_{ILIMTHHS}$ = 550 ±50 µs. The filter time has been chosen in order to avoid false current limit detection for in-rush current that may happen at interface switch-on.*
6. *The short to battery threshold spans in the range [(VPREREG + 0.01) - (VPREREG + 0.1)] V, while the relative deglitch filter time (t_{STBTH}) spans in the range [10-15] µs.*
7. *Leakage to battery threshold is equal to $I_{THVBATP}$ = 15.3 ±9% mA, while the relative deglitch filter time (t_{FLT_LKG}) spans in the range [10-15] µs.*
8. *I_{THOPEN} = [1; 3.5] mA and t_{FLT_OPEN} = [10-15] µs.*
9. *The overtemperature threshold (T_{SD_TRK}) is between 175 °C and 200 °C, while the relative deglitch filter time ($t_{SD\_DEGLITCH}$) spans in the range [7.5-12.5] µs.*
10. *It is very important to understand the meaning of open and current_hi flag. Because of the current-sensing mechanism implemented into the LS pin of the interface, they do not lead to an immediate fault identification. For example, short to ground on HS and sensor open fault, both lead to a small current measured by the IC, but the reason of such a small current is quite different depending on the specific fault occurred. The same happens in case of short to battery on RSUHx: this leads to high current in the interface but also to LS_OVC (which is reported in the RSU_STATUS register).*

Figure 2. **WSI block diagram**



Sensor data registers of the other channels only differ from the previous for the address.

The channel 2 (RS_DATA_RSDR_1) main properties of the register are hereby listed (for register description, refer to Table 7 and Table 8):

- Address: 0010001;
- Type: read only.

The channel 3 (RS_DATA_RSDR_2) main properties of the register are hereby listed (for register description, refer to Table 7 and Table 8):

- Address: 0010010;
- Type: read only.

The channel 4 (RS_DATA_RSDR_3) main properties of the register are hereby listed (for register description, refer to Table 7 and Table 8):

- Address: 0010011;
- Type: read only.

2.7.2 LS fault register RSU_STATUS

The RSU_STATUS register stores the overcurrent information and the short to ground for the RSULx pins.

The main properties of the register are hereby listed:

- Address: 000100;
- Type: read only; clear on read.

Table 10. **RS_DATA_RSDR4…7 register description**

Data field	Description	Reset value	Reset event
Bit [4…7]	RSULx overcurrent[Ch1 ... Ch4]	0b0000	POR
Bit [0…3]	RSULx short to ground[Ch1 ... Ch4]	0b0000	POR

3 WSI configuration procedure

This paragraph contains the correct procedures to follow for frequently executed operations like configuring the WSI for a specific sensor, enabling/disabling one or more channels or testing a channel.

3.1 WSI configuring for a specific sensor

In order to properly configure the wheel speed sensor interface for a specific sensor type, the following procedure must be executed:

1. Set INIT bit in the RS_CTRL register (see Table 1) in order to enable access to configuration registers;
2. Configure WSI behavior for each of the four channels:
   a. Configure channels 1-2 in RS_CFG_0_1 register (see Table 2):
      i. Consider the [0…9] data field for configuring channel 1:
         1. Choose sensor type by writing into [0…1] data field;
         2. Select the threshold evaluation method by writing bit 3 (WSI_FIX_THRESH) (see Section 4);
         3. Enable/disable the *"Standstill Disable"* feature by writing bit 4 (SSDIS) (see Note);
         4. Enable/disable the *"Pass-through"* feature by writing bit 5 (WSIPTEN)
         5. Set the deglitch filter time by writing into [6…9] data field (see Section 4.3);
      ii. Consider the [10…19] data field for configuring channel 2:
         1. Choose sensor type by writing into [10…11] data field;
         2. Select the threshold evaluation method by writing bit 13;
         3. Enable/disable the "Standstill disable" feature by writing bit 14;
         4. Enable/disable the "Pass-through" feature by writing bit 15;
         5. Set the deglitch filter time by writing into [16…19] data field;
   b. Configure channels 3-4 in RS_CFG_2_3 register (see Section 2.2). Follow the same procedure seen for channels 1 and 2.
   c. If fixed thresholds algorithm has been selected at step 2.1.1.2, set the threshold value in RS_AUX_CFG register (see Section 2.3);
3. Enable the desired channel(s) output by setting the corresponding CHxEN bit in RS_CTRL register.
4. Exit configuration mode by resetting INIT bit in RS_CTRL register.

Note: The channel output disable while in standstill feature (SSDIS) is only available for two level, PWM encoded, 2 edges/tooth WSS.

3.2 Enabling/disabling one or more channels

In order to enable/disable a specific channel output, follow the steps below:

1. Set INIT bit in RS_CTRL register (see Table 1) in order to enable access to configuration registers;
2. Enable/disable the desired channel(s) by setting/resetting the correspondent CHxEN bit in RS_CTRL register;
3. Exit configuration mode by resetting INIT bit in RS_CTRL register.

Attention: *Any attempt of writing into the RS_ CTRL register without having set INIT bit first is cause of the register reset and all the channel output are disabled.*

3.3 Testing channel output

This static test consists in transferring the WSSTP bit value on a selected channel output (WSOx). In order to test a channel, follow this procedure:

1. Set DIAG bit in RS_CTRL register (see Table 1) in order to enable access to WSS_TEST register;
2. Select the channel output (WSOx) to be tested by writing the proper binary configuration in the [2…8] data field (see Table 4);

3. Transfer the desired static pattern on the selected channel output by writing the WSSTP bit (see Table 4 and Note);
4. Exit test mode by resetting DIAG bit in RS_CTRL register.

Note: Selected channel output is set high by default at the beginning of the test.

4 Key formulas for thresholds and deglitch time calculation

In this paragraph, the thresholds configuration according to the two available algorithms is explained. The channel output (WSOx) deglitch filter time calculation is also shown. The trigger event that causes WSOx toggling depends on the selected operating mode:

- In normal mode, the channel output toggles every time the current crosses the threshold value with positive slope (see Note 1.);
- In pass-through mode, the channel output toggles every time the current crosses the threshold value with both positive and negative slope, thus reproducing the exact shape of the wheel speed pulse (see Note 2.).

Note:

1. *For two level WSS, the I_{TH1} must be considered as the trigger level. For three level WSS refer to I_{TH2} instead.*
2. *Pass-through mode is optionally available for PWM encoded WSS only. It is selected by default for two level standard sensors.*

4.1 Thresholds evaluation for the fixed thresholds algorithm

The fixed thresholds algorithm is so called because the thresholds are set at a user-defined value. For two level WSS, only one threshold (I_{TH1}) is needed to detect the wheel speed pulse. Three level WSS needs both I_{TH1} and I_{TH2} to be programmed.

The thresholds evaluation formula is shown in Equation 2; by inverting the equations, the values to be programmed in the RS_AUX_CONF register (see Table 3) can be obtained (see Equation 3).

Equation 2–Thresholds evaluation for the fixed thresholds algorithm

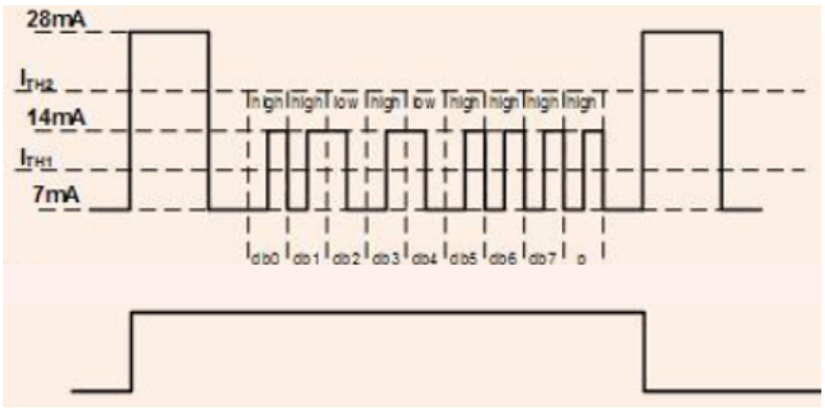
$$\begin{cases} I_{TH1} = RES^{*}(54 + RS\_AUX\_CONF[0...7]) \\ I_{TH2} = RES^{*}(108 + RS\_AUX\_CONF[0...7] + RS\_AUX\_CONF[10...17]) \end{cases} \quad (2)$$

Equation 3–Values to be programmed in the RS_AUX_CONF register to set the desired threshold values

$$\begin{cases} RS\_AUX\_CONF[0...7] = \frac{I_{TH1}}{RES} - 54 \\ RS\_AUX\_CONF[10...17] = \frac{I_{TH2}}{RES} - 108 - RS\_AUX\_CONF[0...7] \end{cases} \quad (3)$$

The resolution value (RES) is equal to 92 µA with a 9% tolerance.

Figure 3. Thresholds positioning for three level, VDA compliant, wheel speed sensors



Top: sensor output signal; bottom: channel output (DOUT) signal.

Both the thresholds must be placed in the middle of the current swings between the two or three different levels, as shown in Figure 3. This is meant to avoid spurious WSOx toggling caused by noise.

The two thresholds are calculated with the following criteria:

- The first threshold (I_{TH1}) spans in the range [4.968-28.428] mA (see Equation 2). This is obtained by adding a “54” offset value in order to prevent misplacing. Therefore, the first threshold is always positioned above the minimum current value allowed for normal operation (5 mA);
- The second threshold (I_{TH2}) (see Equation 2) spans in the range [(I_{TH1} + 4.968) - (I_{TH1} + 28.428)] mA. In fact, I_{TH2} equation could also be rewritten as follows:

Equation 4–Alternative method to calculate I_{TH2}.

$$I_{TH2} = RES^{*}(108 + RS\_AUX\_CONF[0...7] + RS\_AUX\_CONF[10...17]) = RES^{*}(54 + RS\_AUX\_CONF[0...7]) + RES^{*}(54 + RS\_AUX\_CONF[10...17]) = I_{TH1} + RES^{*}(54 + RS\_AUX\_CONF[10...17]) \quad (4)$$

Therefore, I_{TH2} is always positioned above I_{TH1}, which prevents the risk of thresholds inversion. The minimum distance between the two thresholds is equal to 4.968 mA, obtained by adding a “54” offset value in Equation 4.

The default values (see Table 3 and Note) for the thresholds are:

- $I_{TH1} = RES^{*}(54 + 51) = 9.66\,mA$;
- $I_{TH2} = RES^{*}(108 + 51 + 52) = 19.412\,mA$.

These values are optimized for a three level, VDA-compliant WSS. In fact, the first threshold stands in the middle of the current swing between the first two levels (7 mA–14 mA), while the second is placed in the middle between the second and the third level (28 mA).

Note: RS_AUX_CONF register reset values were programmed considering RES = 93.75 µA, which is the final desired value for resolution. Hence, the thresholds are placed respectively at 9.8 mA and 19.6 mA in the final revision.

4.2 Thresholds evaluation for the auto-adjusting thresholds algorithm

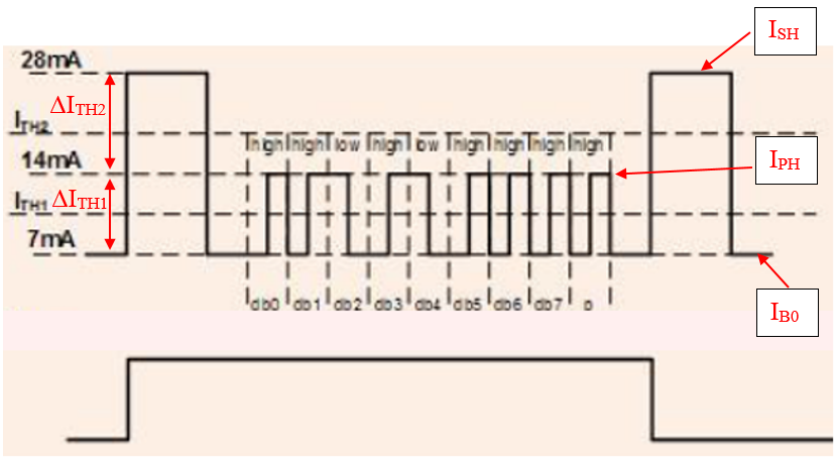
The auto-adjusting thresholds algorithm is so called because the threshold value is automatically determined by the ASIC in order to maintain them well placed in a dynamic scenario where the sensor DC current levels vary in time.

Temporary faulty conditions (soft short to battery or small leakage to ground) could affect the sensor current pattern, slightly shifting it upward or downward for a certain period. With sensor aging, these conditions can become permanent, still not being a serious issue if the current pattern remains limited in a “safe” window.

Choosing this algorithm it prevents the current pattern going into the so called “gray zone”, where WSO output behaves in an unpredictable, dangerous way. Therefore, normal operation can be guaranteed even under permanent minor faulty conditions.

With auto-adjusting thresholds algorithm selected, the ASIC is able to measure the following three parameters:

Figure 4. Parameters needed by the algorithm to update thresholds



Top: sensor output signal; bottom: channel output (DOUT) signal.

- The sensor base current level (I_{B0}), which can be tracked in the range [2.484–20.792] mA (see Note);
- The swing (ΔI_{TH1}) between the second DC level (I_{PH}) and the base current, which can be tracked in the range [4.968–9.2] mA;
- For three level WSS, the swing (ΔI_{TH2}) between the third DC level (I_{SH}) and I_{PH}, which can be tracked in the range [9.936–18.4] mA.

For each channel, the I_{B0} and ΔI_{TH1} measure are available in a dedicated register (see Section 2.5). The ΔI_{TH2} value is instead stored in a separate register (see Section 2.6). These registers can be read even if the fixed thresholds algorithm has been selected. Provided that many faults can be identified by polling a dedicated bit into sensor data register, this confers the microcontroller the capability to constantly monitor WSS status by polling the correspondent base current and swings registers in order to determine whether the current levels are in the normal operating window or not.

Having measured the three parameters above described, the ASIC is able to calculate the optimal position for the two thresholds according to the following formulas:

Equation 5–Thresholds evaluation formulas for auto-adjusting thresholds algorithm

$$\begin{cases} I_{TH1} = I_{B0} + \frac{\Delta I_{TH1}}{2} \\ I_{TH2} = I_{B0} + \Delta I_{TH1} + \frac{\Delta I_{TH2}}{2} \end{cases} \quad (5)$$

Observing Equation 5 and considering the parameters' definitions, it is easy to understand that the algorithm places each of the two thresholds in the middle of the relative current swing.

Note: If the base current goes below 2.484 mA, the open fault is detected and flagged in the sensor data register (RS_DATA_RSDR0…3, see paragraph Section 2.7). For all WSS types but the standard two level, if the base current exceeds 15.3 mA, the leakage to ground condition is detected and flagged in the sensor data register. For STD 2 level WSS, a comparator on instantaneous current has been implemented: if the sensor current exceeds 23 mA, the leakage to ground condition is detected and flagged in the sensor data register.

4.3 Channel output deglitch filter time selection

The output current of the sensor can be affected by a considerable noise on the channel (for example thermal noise on the parasitic resistance of the wire, flicker noise generated by integrated devices, etc.). In order to avoid spurious toggling of the channel output (WSOx) due to random crossings of the thresholds during current rise/fall time, a proper deglitch filter has been implemented. The filter time can be configured by programming the dedicated data field in the WSI configuration registers (see Section 2.2).

The WSOx toggles after the filter time has elapsed respect to the last threshold crossing. In order to determine the deglitch filter time, refer to the following Equation 6:

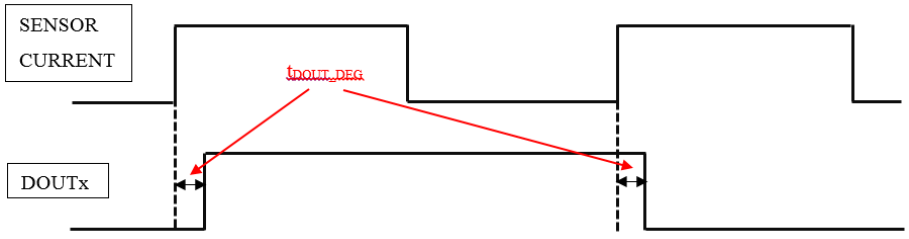
Equation 6–Channel output deglitch filter time evaluation

$$t_{DOUT\_DEG} = 8\mu s + WSIFILT[0...3]*8T_{CK} \quad (6)$$

Counter resolution is equal to T_{CLK} = 62.5 ns (f_{CK} = 16 MHz). The value of deglitch time spans in the range [8–15.5] µs.

An additional 2 µs latency related to current sensing and conversion blocks must be added to t_{DOUT_DEG}.

Figure 5. Example of deglitched WSOx toggling for 2 level, PWM encoded WSS



Revision history

Table 11. **Document revision history**

Date	Revision	Changes
21-Dec-2021	1	Initial release.

Contents

List of tables

List of figures