How to design a CCM PFC pre-regulator based on L4985/L4986

Introduction

This application note describes the main steps to design a continuous conduction mode (CCM) power factor corrector (PFC) pre-regulator based on the L4985/L4986 controller [1.] - [2.].

Figure 1. Typical application based on L4985.

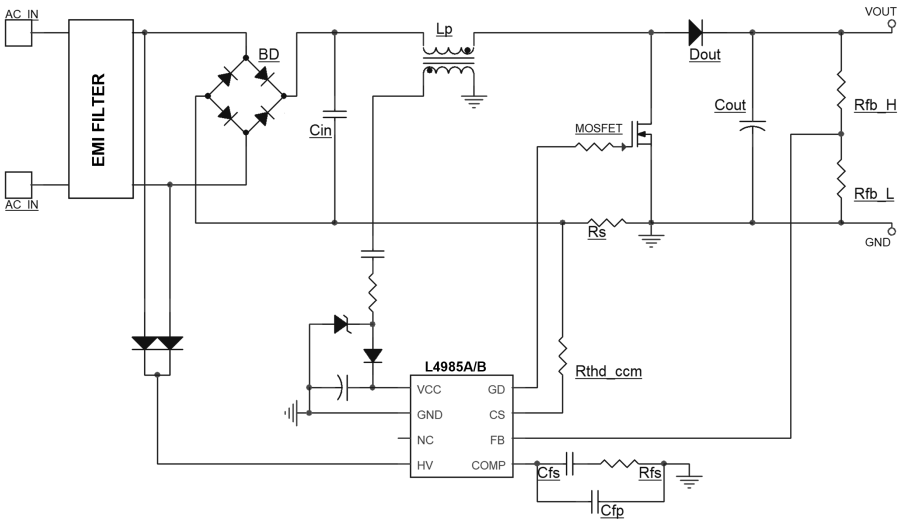
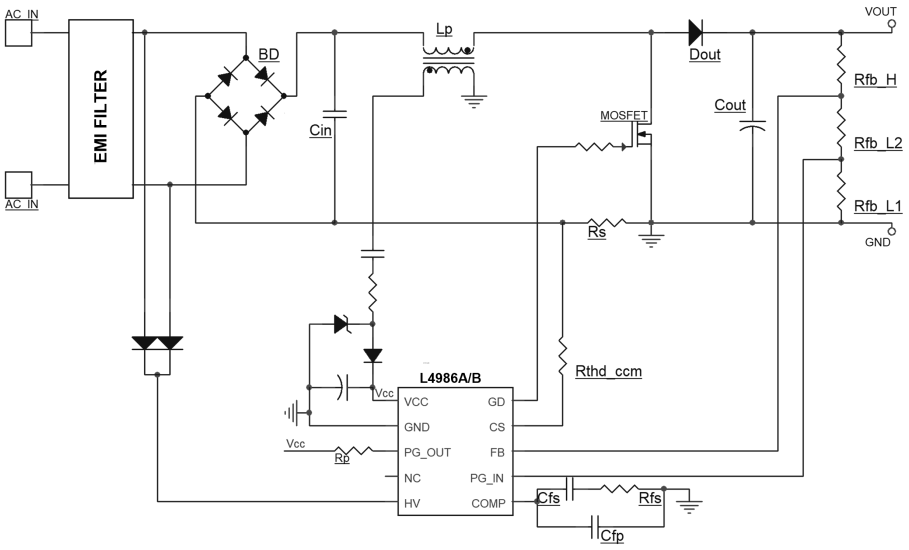


Figure 2. Typical application based on L4986.

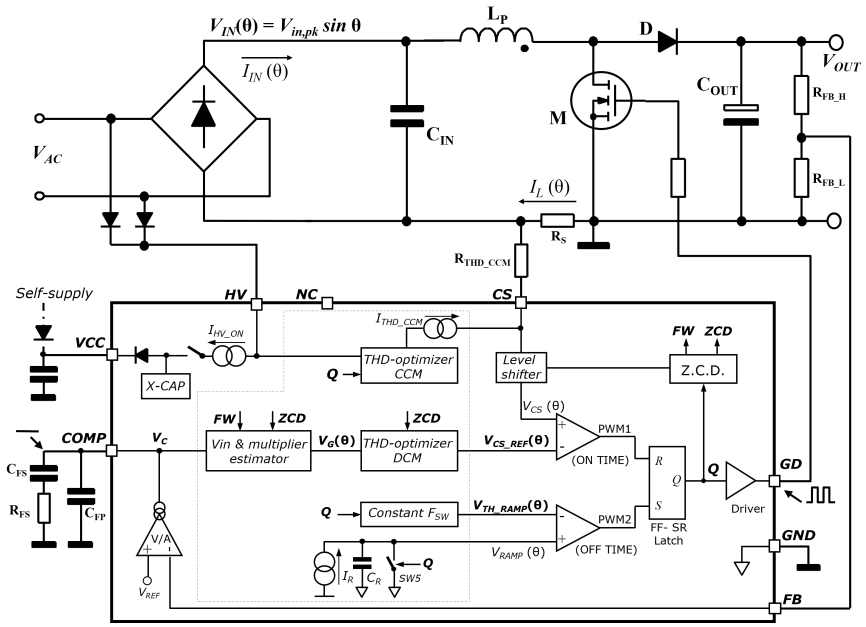


1 CCM PFC - L4985/6 control technique

The L4985/6 controllers [1.]-[2.] implement a conventional peak current-mode control based on fixed-off-time (FOT) control technique, with proprietary circuitries that permit to ideally achieve the same performance of the more complex/expensive average current-mode control.

Considering Figure 3, the power switch on-time (T_{ON}) is programmed by the output voltage control loop comparing the current sense signal V_{CS} with the internal current reference V_{CS_REF} to keep the V_{OUT} regulation; whereas the power switch off-time (T_{OFF}) is programmed by the "OFF-TIME modulator" circuitry to keep quasi-fixed the switching frequency F_{SW} in all operating conditions.

Figure 3. Control loop connections.



The trans-conductance Error Amplifier V/A compares a portion of the output voltage V_{OUT}, brought at its inverting input externally available on pin FB via the resistor divider R_{FB_H}-R_{FB_L}, with an accurate internal reference V_{REF} (2.5 V typ.) connected to the non-inverting input, and generates an error signal V_C proportional to their difference.

If the bandwidth of the error amplifier (essentially determined by the frequency compensation network connected between pin COMP and ground) is narrow enough as in all PFC converters – typically below 20 Hz – and a steady-state operation is assumed, the V_C error signal available at pin COMP can be regarded as a DC level (at least as a first approximation).

The V_C voltage is then used by the "Vin & multiplier estimator" circuitry [3.] that, based also on the FW and ZCD signals, generates a voltage expressed by:

Equation 1

$$V_G(\theta) = V_C \cdot K_1 \cdot \frac{V_{IN}(\theta)}{V_{OUT}}, \quad (1)$$

where K_1 is the circuitry gain (constant term) and $V_{IN}(\theta) = |V_{AC}(\theta)| = V_{in,pk} \cdot sin\,\theta$ (with $0 \le \theta \le \pi$, as a result of the rectification operated by the input bridge) is the instantaneous line input voltage.

Equation #1 shows as the $V_G(\theta)$ voltage is proportional to the $V_{IN}(\theta)$ input voltage and to the V_C control voltage like in a standard current-mode PFC, but without using the standard multiplier block and without the AC line sensing.

The $V_G(\theta)$ voltage is then managed by the “THD-DCM optimizer” circuitry that acts as a simple gain (K_2) in CCM operation, whereas in DCM operation it opportunely shapes the $V_G(\theta)$ voltage in order to achieve ideally sinusoidal input current. As reported in the datasheets [1.]-[2.], the internal current reference voltage $V_{CS\_REF}(\theta)$ can be expressed by:

Equation 2

(2)

$$V_{CS\_REF}(\theta) = V_G(\theta) \cdot K_2 \cdot \frac{T_{ON}(\theta) + T_{FW}(\theta) + T_R(\theta)}{T_{ON}(\theta) + T_{FW}(\theta)},$$

where during the $T_{FW}(\theta)$ and $T_R(\theta)$ time, the boost inductor L_P is demagnetizing or fully demagnetized respectively.

Replacing equation #1 in equation #2 results:

Equation 3

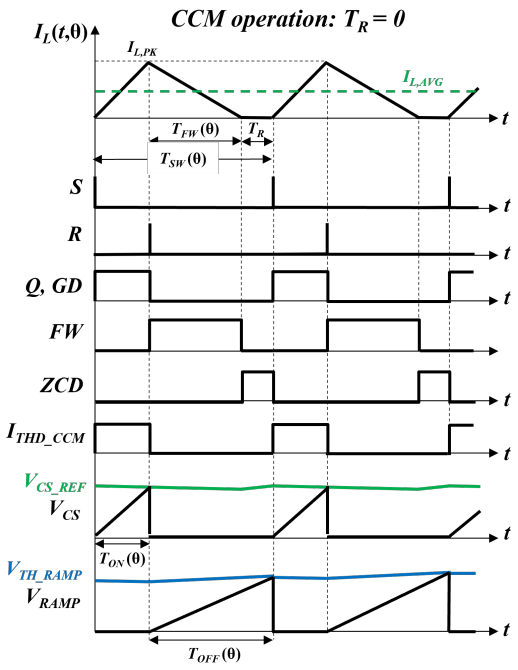
(3)

$$V_{CS\_REF}(\theta) = \frac{K_M}{V_{OUT}} \cdot V_C \cdot V_{IN}(\theta) \cdot \frac{T_{ON}(\theta) + T_{FW}(\theta) + T_R(\theta)}{T_{ON}(\theta) + T_{FW}(\theta)},$$

where $K_M = K_1 K_2$ is the equivalent multiplier gain (see electrical characteristic table in the L4985/L4986 datasheets for more details on www.st.com).

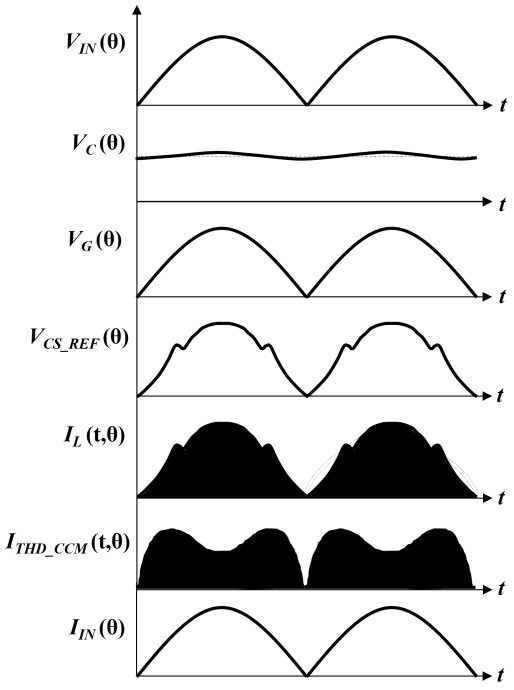
It is worth noting that when the converter operates in CCM operation ($T_R(\theta)=0$), the resulting current sense reference voltage is sinusoidal.

Figure 4. . Key waveforms of the circuit in figure 4 – switching cycle time scale.



Switching cycle time scale

Figure 5. Key waveforms of the circuit in figure 4 – Line cycle time scale.



Line cycle time scale

The internal current reference voltage $V_{CS\_REF}(\theta)$ is then compared with the current sense $V_{CS}(\theta)$ pin voltage (which is internally translated due to negative inductor current sensing) that is opportunely shaped by the “THD-CCM optimizer” sourcing the $I_{THD\_CCM}(\theta)$ current, to achieve sinusoidal input current in CCM operation.

As demonstrated in the datasheet, selecting the proper R_{THD_CCM} resistor, which is connected between the CS pin and the sensed voltage across R_S resistor, the resulting input current is:

Equation 4

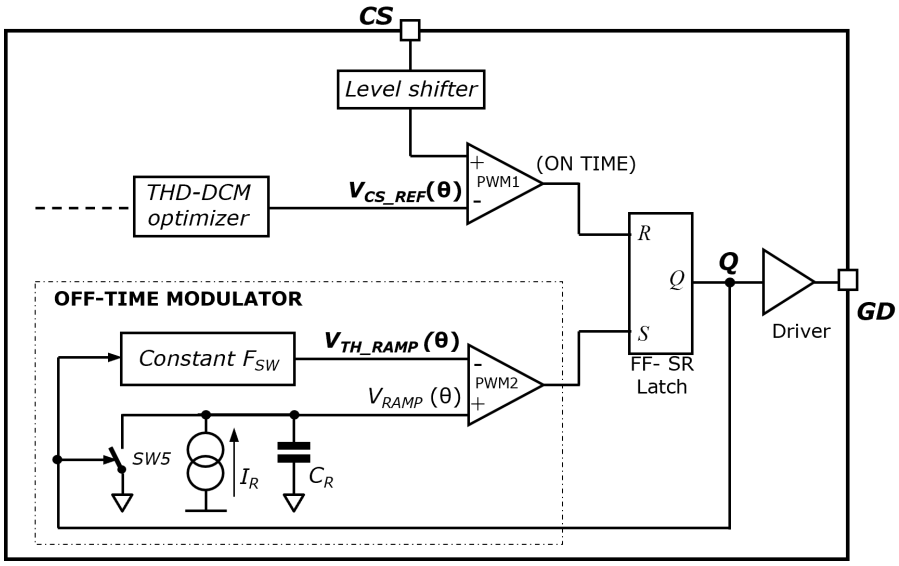
(4)

$$I_{IN}(\theta) = \frac{1}{R_S} \cdot \frac{K_M}{V_{OUT}} \cdot V_C \cdot V_{IN}(\theta),$$

which is sinusoidal and in phase with the $V_{IN}(\theta)$ input voltage (ideally zero-THD and unity-PF).

The power switch off-time (T_{OFF}) is determined by the OFF-TIME modulator [4.], which is able to achieve quasi-fixed switching frequency in all operating conditions (CCM and DCM operation) and independent from the input/output voltage, the load conditions and the converter's parasitic.

Figure 6. OFF-TIME modulator – details.



Referring to Figure 6, once the power switch on-time is ended (Q signal goes low) the internal switch SW5 is open and the constant current generator I_R starts to charge linearly the capacitor C_R. The resulting voltage V_{RAMP} is compared with the voltage V_{TH_RAMP}, which is opportunely generated by the "Constant F_{SW}" circuitry based on the Q signal duration (T_{ON}). As soon as the ramp voltage V_{RAMP} reaches the V_{TH_RAMP} voltage, the flip-flop is set and the external power switch is turned on (Q signal goes high).

In other words, the power switch off-time (T_{OFF}) is modulated based on the on-time information (T_{ON}) to keep cycle-by-cycle constant the resulting switching frequency (F_{SW}=1/T_{SW_TARGET}):

$T_{OFF} = T_{SW\_TARGET} - T_{ON}$.

Note: It is worth noting that near line zero-crossing the power switch on-time could be higher than T_{SW_TARGET} period, due to low input voltage, resulting in a lower switching frequency F_{SW} with respect to the desired target (65 KHz/130 KHz in A/B version respectively). An internal IC circuitry limits the maximum power switch on-time at T_{ON_MAX} (40 µs/20 µs typ. in A/B version respectively) limiting the minimum switching frequency (around 25 KHz/50 kHz typ. in A/B version respectively).

Figure 7. OFF-TIME modulator timing – switching cycle time scale.

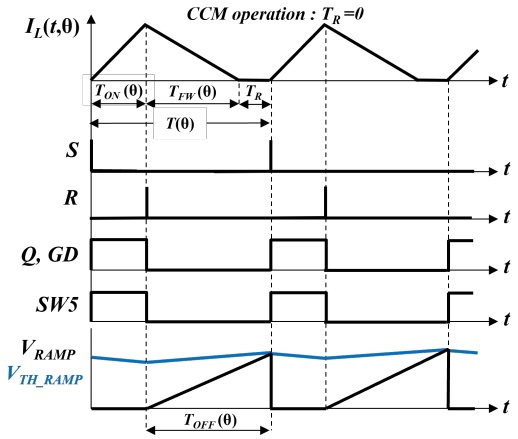
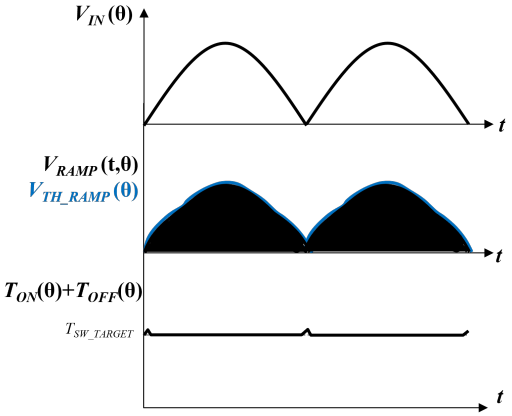


Figure 8. OFF-TIME modulator timing – line cycle time scale.



2 L4985/6 biasing circuitry

In the following section the selection of the components around the L4985/L4986 is described.

2.1 Output voltage divider resistors

In steady-state condition the FB pin is equal to the internal voltage reference V_{REF}, so the programmed output voltage V_{OUT} results:

Equation 5

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB\_H}}{R_{FB\_L}}\right), \quad (5)$$

where the upper resistor R_{FB_H} can be selected based on the maximum power dissipation P_d of the resistor divider network:

Equation 6

$$R_{FB\_H} \cong \frac{{V_{OUT}}^2}{P_d}. \quad (6)$$

The typical value of the R_{FB_H} resistor (which is typically composed by a series of resistors to sustain the high voltage drop V_{OUT}) is in the range of 1-10 MΩ to limit the power dissipation P_d at few tens mW.

The R_{FB_L} resistor is then selected based on the desired output voltage V_{OUT}:

Equation 7

$$R_{FB\_L} = R_{FB\_H} \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}. \quad (7)$$

2.2 Current sense resistor

The current sense circuitry, which is typically composed by the parallel of two or more resistors (film type) to sustain its own power dissipation, is placed on the GND return path and its equivalent resistor value R_S has to be opportunely selected to handle the maximum output power (P_{OUT_MAX}) also in the worst-case condition (e.g. at minimum input voltage $V_{AC\_RMS,min}$).

In particular, the R_S resistor value impacts on the voltage dynamics of pin CS and pin COMP.

Referring to the datasheet, the controller embeds an overcurrent comparator OCP1 that limits the peak inductor current implementing a cycle-by-cycle overcurrent protection. To maximize the dynamic of the CS voltage pin, the OCP1 is typically selected equal to the maximum output load considering the worst-case condition (minimum input voltage, minimum overcurrent internal threshold):

Equation 8

$$R_{S\_OCP1} = V_{CS\_OCP1,min} \cdot \frac{\eta \cdot V_{AC,min}}{\sqrt{2} \cdot P_{OUT,max}}, \quad (8)$$

where V_{CS_OCP1} is the internal overcurrent threshold and η the estimated converter's efficiency.

Still referring to the datasheet and starting from equation #4, it is possible to find the relationship between the control voltage V_C and the output load which is:

Equation 9

$$V_C = R_S \cdot \frac{1}{K_M} \cdot \frac{\frac{P_{OUT}}{\eta} \cdot V_{OUT}}{{V_{AC}}^2}. \quad (9)$$

Considering that the COMP pin voltage is V_C + 1V (typ.), the resulting current resistor that guarantees the respect of the dynamic of the pin COMP (e.g. voltage lower than the minimum upper saturation voltage $V_{COMP,min}$) is:

Equation 10

(10)

$$R_{S\_COMP} = \left(V_{COMP,min} - 1V\right) \cdot K_M \cdot \eta \cdot \frac{{V_{AC,min}}^2}{P_{OUT\_max} \cdot V_{OUT}} .$$

To guarantee both the previous two conditions, the current sense resistor R_S has to be selected equal or lower than the minimum:

Equation 11

(11)

$$R_S = \min\left(R_{S\_OCP1}, R_{S\_COMP}\right) .$$

2.3 THD-CCM optimizer resistor

The THD-CCM circuitry basically sources a current $I_{THD\_CCM}(\theta)$ from the CS pin during the power switch on-time (see L4985/L4986 datasheet for more details) to compensate the inductor current ripple optimizing the THD performance when the converter operates in CCM (e.g. in full-load condition). In fact, being a peak current mode control, a simple sinusoidal current reference cannot generate a sinusoidal input current (the input current is the average value of the inductor current in a switching cycle).

Referring to the datasheet, the R_{THD_CCM} resistor can be selected using

Equation 12

(12)

$$R_{THD\_CCM} = K_{CCM} \cdot \frac{R_S}{L_P},$$

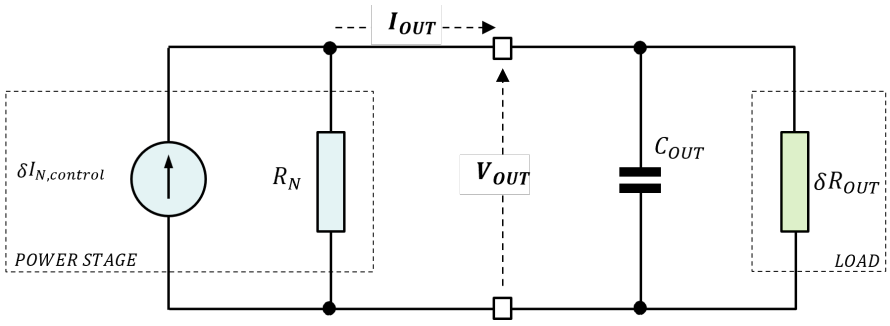
where L_P is the inductor value and K_{CCM} is the internal THD_CCM circuitry gain (0.55 typ.).

An optimization of the R_{THD_CCM} resistor value could be needed based on the real application parameters and it can be easily done starting from the previous calculated value.

2.4 Compensation network

Figure 9 shows the small signal model of the PFC converter, where the power stage has been represented with the equivalent Norton circuit and the ESR (Equivalent Series Resistance) of the output capacitor has been neglected (cross over frequency f_c of the PFC converter is much lower than ESR frequency zero $f_{z\_ESR} = 1 / 2\,\pi \cdot ESR \cdot C_{OUT}$).

Figure 9. Small signal model of the PFC converter.



The large signal control-to-output transfer function of the PFC converter based on the L4985/L4986 is:

Equation 13

(13)

$$I_{OUT} = V_C \cdot \frac{K_M}{2\,R_S} \cdot \frac{{V_{IN,pk}}^2}{{V_{OUT}}^2},$$

and then the equivalent Norton current generator results:

Equation 14

(14)

$$\delta I_N = \delta V_C \frac{\partial I_{OUT}}{\partial V_C} = \delta V_C \frac{K_M}{2\,R_s} \cdot \frac{{V_{IN,pk}}^2}{{V_{OUT}}^2}.$$

Still starting from equation #13, the equivalent Norton resistor results:

Equation 15

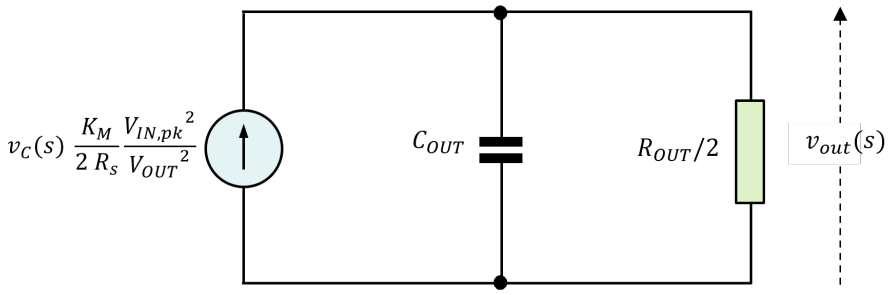
(15)

$$R_N = -\frac{\partial V_{OUT}}{\partial I_{OUT}} = \frac{R_{OUT}}{2}.$$

It is interesting to note that the equivalent Norton resistance is lower than in a standard multiplier-based PFC converter where R_N=R_{OUT}.

Figure 10 shows the equivalent small-signal model of the converters in the Laplace domain, assuming as output load a DC-DC converter: in this case the equivalent load resistance is negative and equal to the R_{OUT} that is the equivalent large signal load resistance ($\delta R_{OUT} = -R_{OUT} = -V_{OUT}/I_{OUT}$). As a result the equivalent output resistance is R_{OUT}/2 (R_N //-R_{OUT}).

Figure 10. Small signal model – control-to-output transfer function.



The control-to-output transfer function results:

Equation 16

(16)

$$G_{co}(s) = \frac{v_{out}(s)}{v_c(s)} = \frac{K_M}{2\,R_s} \cdot \frac{{V_{IN,pk}}^2}{{V_{OUT}}^2} \cdot \frac{R_{OUT}}{1 + s \cdot R_{OUT} \cdot C_{OUT}},$$

where it is interesting to note that the frequency pole $f_{p\_co} = 1\ /\ 2\,\pi\ R_{OUT}\,C_{OUT}$ depends on the load condition and the low-frequency gain depends on input/output voltage set-points. The previous equation can be rewritten in the form:

Equation 17

(17)

$$G_{co}(s) = \frac{G_o}{1 + s \cdot t_{p\_co}}$$

where $G_o = \frac{K_M}{2\,R_s} \cdot \frac{{V_{IN,pk}}^2}{{V_{OUT}}^2} \cdot R_{OUT}, t_{p\_co} = R_{OUT} \cdot C_{OUT}.$

The control loop compensation network (composed by the R_{FS}, C_{FS}, C_{FP} components) is placed between the COMP pin and GND as shown in Figure 11, and the transfer function is:

Equation 18

(18)

$$H(s) = \frac{v_c(s)}{v_{out}(s)} = g_{m\_EA} \cdot \frac{R_{FB\_L}}{R_{FB\_L} + R_{FB\_H}} \cdot \frac{1}{s \cdot (C_{FS} + C_{FP})} \cdot \frac{1 + s \cdot R_{FS} \cdot C_{FS}}{1 + s \cdot R_{FS} \cdot \left(\frac{C_{FS} \cdot C_{FP}}{C_{FS} + C_{FP}}\right)},$$

that can be rewritten in the form:

Equation 19

$$H(s) = \frac{H_o}{s} \cdot \frac{1 + s \cdot t_z}{1 + s \cdot t_p}, \quad (19)$$

where $H_o = \frac{g_{m\_EA} \cdot R_{FB\_L}}{\left(R_{FB_L} + R_{FB_H}\right)\left(C_{FS} + C_{FP}\right)}$, $t_z = R_{FS} \cdot C_{FS}, t_p = R_{FS} \cdot \frac{C_{FS} \cdot C_{FP}}{C_{FS} + C_{FP}}$.

Equation #19 shows as the transfer function introduces two poles (one in the origin to achieve the DC output regulation) and one zero. Equation #19 shows also that the compensation network transfer function has a non-zero gain at the second harmonic of the line frequency ($2 \cdot f_{LINE}$) and this introduces a third-harmonic distortion of the current reference. In other words, the output voltage ripple ΔV_{OUT} (at $2 \cdot f_{LINE}$) is not eliminated by the compensation network and so its present at the COMP pin voltage ($\Delta V_{COMP} = \Delta V_{OUT} \cdot |H(j\,2\pi \cdot (2 \cdot f_{LINE})| = \Delta V_{OUT} \cdot H_{2f}$) introducing a distortion of the current reference V_{CS_REF}.

Considering that the output voltage ripple (peak-to-peak) is:

Equation 20

$$\Delta V_{OUT} = \frac{I_{OUT}}{2\,\pi \cdot f_{LINE} \cdot C_{OUT}}, \quad (20)$$

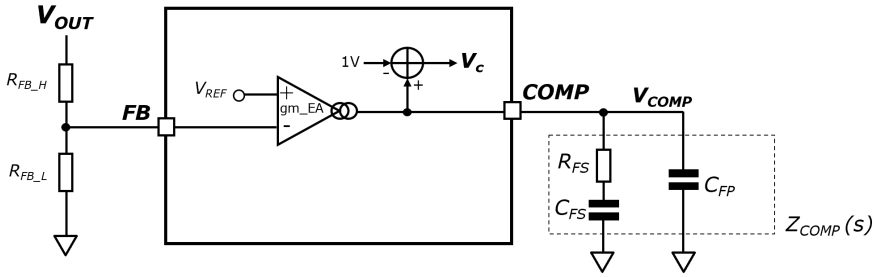
it is possible to demonstrate that the third-harmonic distortion of the current reference is given with a good approximation by:

Equation 21

$$D_3 = \frac{1}{2} \cdot \frac{\frac{\Delta V_{COMP}}{2}}{V_{COMP} - V_{C0}} = \frac{1}{2} \cdot \frac{\frac{\Delta V_{OUT}}{2} \cdot H_{2f}}{V_{COMP} - V_{C0}}, \quad (21)$$

where V_{C0} is the “zero-power” level of the control voltage ($V_{C0} = 1V$).

Figure 11. Compensation network.



The open loop transfer function then results:

Equation 22

$$F(s) = G_{co}(s) \cdot H(s) = \frac{G_o}{1 + s \cdot t_{p\_co}} \frac{H_o}{s} \cdot \frac{1 + s \cdot t_z}{1 + s \cdot t_p}, \quad (22)$$

and considering that s=jω, it can be rewritten in the form:

Equation 23

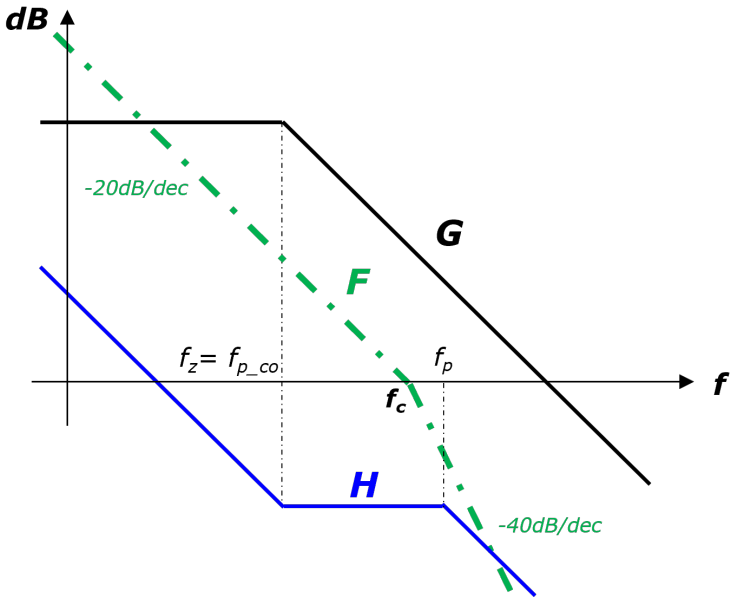
$$F(\mathrm{j}\omega) = \frac{G_o \cdot H_o}{\mathrm{j}\omega} \cdot \frac{1}{1 + \frac{\mathrm{j}\omega}{2\,\pi \cdot f_{p\_co}}} \cdot \frac{1 + \frac{\mathrm{j}\omega}{2\,\pi \cdot f_z}}{1 + \frac{\mathrm{j}\omega}{2\,\pi \cdot f_p}}, \quad (23)$$

To achieve a good closed-loop stability and THD performance, the compensation network is then designed using the following rules:

- $f_z = f_{p\_co}$, to compensate the pole of the control-to-output transfer function and achieve the system stability.

- $H_{2f} = \frac{2 \cdot D_3 \cdot (V_{COMP} - V_{C0})}{\Delta V_{OUT}/2}$, to set the maximum third-harmonic distortion D_3% (at the maximum input voltage condition).
- f_p position to achieve the desired phase-margin (Φ_m).

Figure 12. Asymptotic Bode Diagram - module.



Based on the previous considerations, and assuming $C_{FP} << C_{FS}$, the suggested compensation network results:

Equation 24

$$H_{2f} = \frac{2 \cdot D_3 \cdot (V_{COMP} - V_{Co})}{\Delta V_{OUT}/2} = \frac{2 \cdot D_3 \cdot V_C}{\Delta V_{OUT}/2}. \quad (24)$$

Equation 25

$$f_z = f_{p\_co} = \frac{1}{2\pi \cdot R_{OUT} \cdot C_{OUT}}. \quad (25)$$

Equation 26

$$f_p = \sqrt{\frac{f_z \cdot 2 f_{LINE} \cdot H_{2f} \cdot G_o \cdot tan\left(\frac{\pi}{180} \cdot \Phi_m\right)}{\sqrt{1 + \frac{1}{\left(tan\left(\frac{\pi}{180} \cdot \Phi_m\right)\right)^2}}}} \quad (26)$$

Equation 27

$$C_{FP} = \frac{g_{m\_EA} \cdot R_{FB\_L}}{R_{FB\_L} + R_{FB\_H}} \cdot \frac{1}{2\pi \cdot 2 f_{LINE} \cdot H_{2f}}. \quad (27)$$

Equation 28

$$C_{FS} = C_{FP} \cdot \frac{f_p - f_z}{f_z}. \quad (28)$$

Equation 29

$$R_{FS} = \frac{1}{2\pi \cdot f_z \cdot C_{FS}}. \quad (29)$$

2.5 Power good function

Referring to L4986, the controller provides the adjustable PGOOD function: the PFC output voltage is monitored by the PG_IN pin (#5) and accordingly a driving logic signal exiting from the PG_OUT pin (#6).

The PG_OUT (open drain) is actively pulled to ground once the IC is turned on and the FB pin voltage exceeds the internal threshold V_{PGOOD_ON} (2.375 V typ.). Then the controller starts to monitor the PG_IN pin and as soon as its voltage is lower than the internal threshold V_{PGOOD_OFF} (1.250 V typ.), the PG_OUT pin is set high impedance. As a result, the desired warning output voltage (V_{OUT_PGOFF}) can be programmed through the selection of the R_{FB_L1} resistor:

Equation 30

$$R_{FB\_L1} = \frac{V_{PGOOD\_OFF}}{V_{OUT\_PGOFF}} \cdot \left(R_{FB_H} + R_{FB_L}\right) \quad (30)$$

where R_{FB_H}+R_{FB_L} has already been selected based on the desired output voltage V_{OUT}, and the R_{FB_L2} resistor results:

Equation 31

$$R_{FB\_L2} = R_{FB\_L} - R_{FB_{L1}} \quad (31)$$

It is worth noting that the desired warning output voltage (V_{OUT_PGOFF}) can be selected between V_{OUT} and V_{OUT}/2.

2.6 External burst-mode function

The FB pin can be used to implement an external burst-mode (EBM), forcing the pin lower than the internal threshold $V_{FB\_FF/EBM}$ (500 mV typ.): the switching activity is stopped and the IC power consumption is reduced. The device restarts switching, without implementing the soft-start, as soon as the FB voltage exceeds the $V_{FB\_FF/EBM}$ threshold by 50 mV typ.

As reported in the L4985/L4986 datasheet, as soon as the device enters in the EBM state a weak pull-up current I_{FB_EBM} (100 µA typ.) is sourced from the FB pin to speed up the FB voltage rising edge when the external pull-down is released. In addition, once the FB voltage exceeds $V_{FB\_FF/EBM}$ + 50 mV the I_{FB_EBM} current of 100 µA is increased to 1 mA until the FB pin voltage reaches the final target of 2.5 V (internal V_{REF}).

Note: When using the EBM function, it is suggested to add a C_{FB} filter capacitor between FB pin and GND to control the FB pin voltage rise time to avoid excessive overshoot that decreases the output voltage regulation. Typical suggested value of the C_{FB} capacitor is 2.2 nF÷3.3 nF.

2.7 High-voltage startup

The integrated high-voltage startup current generator sources from the VCC pin a constant current I_{HV_ON} to charge the VCC filter capacitor up to the start-up threshold (V_{CC_ON}). As a result, the charging time is:

Equation 32

$$T_{VCC} = C_{VCC} \cdot \frac{V_{CC_{ON}}}{I_{HV_{ON}}}, \quad (32)$$

where typically the C_{VCC} capacitor is an electrolytic-type and in the range of 47 µF-220 µF. It is worth noting that the minimum value depends also on the maximum acceptable drop at the converter's startup when the self-supply winding does not provide energy.

The HV pin has to be connected to the AC input side (before the bridge rectifier) through two high-voltage diodes (e.g., S1M - 1000 V/1A).

2.8 Input line discharge

The high-voltage startup block includes the circuitry to discharge the X-capacitors of the EMI filter to a safe level, allowing the unit to meet safety regulations (such as IEC 61010-1 or IEC 62368-1) without using the traditional discharge resistor in parallel to the X-capacitors.

After a detection time T_{DECT_XCAP} (64 ms typ.) from the AC mains disconnection, the X-cap discharge operation is triggered and the internal HV current generator is turned on: a discharge current I_{HV_ON} (5 mA min.) is drawn from the HV pin ensuring the X-cap discharge until the voltage on the HV pin falls below a safe level (45 V max. V_{HV_MIN} parameter in the Electrical Characteristic table of the datasheet). The resulting total discharge time is:

Equation 33

$$T_{XCAP\_DIS,max} = T_{DECT\_XCAP} + C_{XCAP}\frac{\sqrt{2}\cdot V_{AC,max} - 45V}{I_{HV\_DIS,min}}. \quad (33)$$

2.9 VCC supply

The supply voltage of the device is initially provided by the internal high-voltage startup current generator (that charges the VCC pin up to the turn-on threshold V_{CC_ON}) and then has to be provided by the self-supply winding and/or other supply (e.g. from the auxiliary winding of the transformer in a second stage based on a resonant converter).

Note: It is worth remembering that the self-supply has to be designed to avoid the HV start-up intervention in the normal operation (e.g., V_{CC} pin voltage always higher than V_{CC_OFF} in all operating conditions) to avoid extra power consumption and a temperature increase of the IC.

2.10 Gate driver

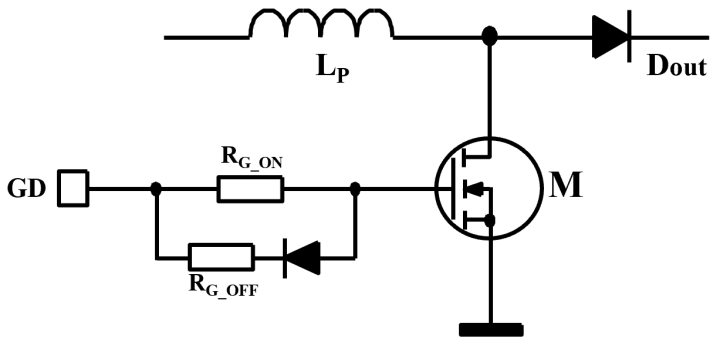
The GD pin is the output of the driver block and is able to drive an external power MOSFET with 0.7 A source and 1.5 A sink capability.

The high-level voltage of this pin (V_{OH}) is internally clamped at about 12 V to avoid excessive gate voltages in case the controller is supplied with a high V_{CC} value.

To avoid undesired switch-on of the external MOSFET due to some leakage current when the supply of the L4985/L4986 is below the UVLO threshold, an internal pull-down circuit holds the pin low (the circuit guarantees 1.1 V maximum at I_{SINK}=1 mA).

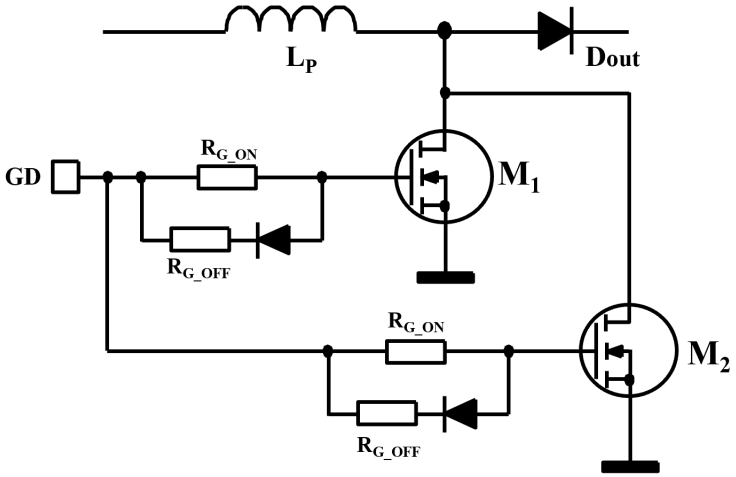
A gate resistor R_{G_ON} in series to GD pin is typically added to limit the high dv/dt at power MOSFET turn-on. To avoid excessive slowdown at power MOSFET turn-off, a second resistor R_{G_OFF} plus a signal diode can be used as shown in Figure 13.

Figure 13. Typical gate driver network



Note: When paralleling two power MOSFETs, a minimum value of the gate resistance (especially at the power MOSFET turns on, e.g. typically R_{G_ON} >15 Ω) is needed to avoid high frequency oscillation due to parasitic inductance (gate trace and internal gate MOSFET). It is also worth remembering that one resistor for each MOSFET has to be used as shown in Figure 14.

Figure 14. Typical gate driver network when paralleling two MOSFETs



3 Power stage design

This section describes the steps to design the components of the PFC boost power stage, based on the target specifications/requirements:

- AC line voltage range (rms): $V_{AC,min}$ ÷ $V_{AC,max}$
- Minimum line frequency: $f_{LINE,min}$
- Nominal output voltage: V_{OUT}
- Rated output power: $P_{OUT,max}$
- Expected efficiency: η
- Hold-up time and minimum output voltage: T_{hold}, $V_{OUT,min}$
- Switching frequency: F_{SW}
- Inductor ripple factor: K_r
- Maximum ambient temperature: $T_{amb,max}$

3.1 Bridge diode rectifier (BD)

The input rectifier bridge can use standard slow recovery, low-cost devices. Typically, a 600 V device is selected, to have good margin against mains surges, and with an average current capability higher than:

Equation 34

$$I_{pk,avg\_bridge} = \sqrt{2} \cdot I_{in,rms\_bridge} \ , \quad (34)$$

where the input RMS current I_{in,rms_bridge} is:

Equation 35

$$I_{in,rms\_bridge} = \frac{\sqrt{2}}{2} \cdot \frac{\frac{P_{OUT}}{\eta}}{V_{AC} \cdot PF}. \quad (35)$$

The rectifier bridge power dissipation can be estimated with the following formula:

Equation 36

$$P_{bridge} = 4 \cdot R_{diode} \cdot I_{in,rms\_bridge}^{\ 2} + 4 \cdot V_{th,diode} \cdot \left(\frac{2}{\pi} \cdot I_{in,rms\_bridge}\right), \quad (36)$$

where $V_{th,diode}$ and R_{diode} are respectively the threshold voltage and dynamic resistance of a single diode of the bridge, which can be found in the component datasheet.

Based on the total power losses value (P_{bridge}) and based on the maximum acceptable bridge-diode's junction temperature target (e.g. $T_{j\_bridge,max}$=125 °C), it is possible to calculate the maximum thermal resistance of the heatsink required to keep the bridge-diode's junction temperature below $T_{j\_bridge,max}$:

Equation 37

$$R_{th} \cong \frac{T_{j\_bridge,max} - T_{amb,max}}{P_{bridge}}. \quad (37)$$

Note: An NTC resistor limiting the current at turn-on is required to avoid overstress to the diode bridge.

3.2 Boost Inductor (L_p)

The boost inductor value (L_p) is selected based on the maximum current ripple factor (K_r), that is the ratio of the peak-to-peak current ripple amplitude to the "average" inductor current (cycle-by-cycle), at minimum line voltage ($V_{AC,min}$) and rated load ($P_{OUT,max}$):

Equation 38

(38)

$$K_r = \frac{\Delta I_L}{I_{L\_AVG}}.$$

The choice of the K_r is a trade-off between the inductor size and the stress on the switches, and typical range is between 30%-50%:

The maximum “average” inductor current $I_{L\_AVG\_max}$ can be estimated by (PF≅1):

Equation 39

(39)

$$I_{L_{AVG},max} \cong \sqrt{2} \cdot \frac{P_{IN,max}}{V_{AC,min}} = \sqrt{2} \cdot \frac{P_{OUT,max}}{\cdot V_{AC,min}}.$$

and the maximum inductor current ripple ($\Delta I_{L,max}$), estimated starting from the inductor volt-second relationship in CCM operation $V_{IN}T_{ON}=(V_{OUT}-V_{IN})T_{OFF}$, is:

Equation 40

(40)

$$\Delta I_{L,max} \cong \frac{\sqrt{2} \cdot V_{AC,min}}{L_P} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{AC,min}}{V_{OUT}}\right) \cdot \frac{1}{F_{SW}}$$

Replacing equation #38 and #39 in equation #40, and considering the worst-case condition also for the switching frequency, the suggested L_p results:

Equation 41

(41)

$$L_p = \eta \cdot \frac{{V_{AC\_min}}^2}{K_r \cdot F_{SW,min} \cdot P_{OUT\_max}} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{AC\_min}}{V_{OUT}}\right).$$

3.3 Input capacitor (C_{in})

The input filter capacitor (C_{in}), placed across the diode bridge output, smooths the high-frequency ripple and it sustains the maximum instantaneous input voltage. For wide range operation the minimum value of the input filter capacitor can be easily calculated using a practical formula based on the output power that the PFC delivers at full load:

Equation 42

(42)

$$C_{in\_min} = 2.5 \cdot 10^{-3} \cdot \frac{\mu F}{W} \cdot P_{OUT\_max} \quad ,$$

or it can be calculated based on the maximum acceptable voltage ripple:

Equation 43

(43)

$$C_{in\_ripple} = \frac{K_r \cdot \sqrt{2} \cdot P_{OUT,max}}{2\pi \cdot F_{SW} \cdot r \cdot \eta \cdot {V_{AC\_min}}^2},$$

where r is the coefficient ripple voltage.

The maximum value of this capacitor has to be not much higher than the previous values to avoid the distortion of the input mains current, due to the residual voltage retained by the capacitor that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

3.4 Output capacitor (C_{out})

The output bulk capacitor value (C_{out}) is selected based on the expected output voltage ripple and hold-up time (if requested). Neglecting the contribution of the ESR, as the capacitive reactance is dominant, the minimum value of the output capacitor to respect the ripple specification is:

Equation 44

(44)

$$C_{out\_ripple} = \frac{I_{OUT,max}}{2\,\pi \cdot f_{LINE,min} \cdot \Delta V_{OUT}},$$

where ΔV_{OUT} is output voltage ripple (peak-to-peak).

If the PFC stage has to guarantee a specified hold-up time (T_{hold}), the calculation of the output capacitor is different. The value of the capacitor when the line voltage drops out, needed to deliver the output power for a certain time T_{hold} until the output voltage reaches the required minimum voltage value (V_{OUT_MIN}) depends on the load and the value of the ripple. When V_{OUT_MIN} is reached, a 'power fail' is detected, stopping the downstream system supplied by the PFC. The worst-case for the hold-up time is at minimum input voltage and full load, with the line drop starting at the valley of the sine-varying ripple of the output voltage.

The minimum capacitor to respect the hold-up time then results:

Equation 45

$$C_{out\_holdup} = \frac{2 \cdot P_{OUT,max} \cdot T_{hold}}{\left(V_{OUT} - \frac{\Delta V_{OUT}}{2}\right)^2 - \left(V_{OUT\_MIN}\right)^2} , \quad (45)$$

To respect both conditions, then

$C_{out} > max\left(C_{out_{ripple}}, C_{out_{holdup}}\right)$.

3.5 Power MOSFET

Selection of the power MOSFETs (typically one or two in parallel) concerns mainly the equivalent on-resistance ($R_{DS(on)}$), that should be low in order to minimize conduction losses, without increasing the switching losses due to the MOSFET's equivalent output capacitance C_{oss}. To achieve high-efficiency both $R_{DS(on)}$ and the C_{oss} have to be taken into account, also considering the trade-off between cost versus performance.

The MOSFET breakdown voltage is selected considering the PFC nominal output voltage adding some margin (e.g., 20%) to guarantee reliable operation.

The total power losses of the MOSFETs are mainly given by the sum of conduction, switching and capacitive losses:

Equation 46

$$P_{loss}(V_{AC}, P_{OUT}) = P_{cond}(V_{AC}, P_{OUT}) + P_{sw}(V_{AC}, P_{OUT}) + P_{cap} , \quad (46)$$

where conduction (P_{cond}) and switching (P_{sw}) losses depend on the input voltage and output power condition. The worst-case occurs typically at minimum input voltage ($V_{AC,min}$) and maximum output power ($P_{OUT,max}$).

The conduction losses can be estimated with:

Equation 47

$$P_{cond}(V_{AC}, P_{OUT}) = R_{dson} \cdot I_{sw,rms}(V_{AC}, P_{OUT})^2 , \quad (47)$$

where the rms current into the switch is:

Equation 48

$$I_{sw,rms}(V_{AC}, P_{OUT}) = \frac{P_{OUT}/\eta}{\sqrt{2} \cdot V_{AC} \cdot PF} \cdot \sqrt{2 - \frac{16 \cdot \sqrt{2} \cdot V_{AC}}{3\pi \cdot V_{OUT}}} . \quad (48)$$

It is worth noting that normally in the datasheets the $R_{DS(on)}$ is given at ambient temperature (25 °C), then to properly calculate the conduction losses at the MOSFET junction operating temperature (e.g. T_j=100 °C), a multiplier factor should be taken into account. Multiplier factor that can be found on the datasheet looking at the normalized on-resistance versus temperature graph (e.g. typically a multiplier factor of 1.7 considering T_j=100 °C).

The switching losses are difficult to predict as they depend on the particular switching waveform, determined by many factors (driving current, gate resistors, MOSFET gate internal resistance, Vth, gate charge, total capacitance on the drain node including parasitic capacitances etc.).

A good approximation to determine the generic switching losses due to the MOSFET commutation occurring at turn-on and turn-off can be basically expressed by:

Equation 49

(49)

$$P_{sw} = \frac{1}{2} \cdot V_{DS} \cdot I_{DS} \cdot \left(t_{rise} + t_{fall}\right) \cdot F_{sw},$$

where V_{DS} is the drain-to-source of the MOSFET, I_D the average drain current and t_{rise} and t_{fall} refer to the rising and the falling edge of V_{DS}. Considering that I_D=$I_{SW,rms}$ and V_D=V_{OUT} results:

Equation 50

(50)

$$P_{sw}\left(V_{AC}\right) = \frac{1}{2} \cdot V_{OUT} \cdot I_{SW,rms}(V_{AC}) \cdot \left(t_{rise} + t_{fall}\right) \cdot F_{sw}\ .$$

First the average rising times of drain voltage can be estimated considering the total drain node capacitance (C_{OSS} – see MOSFET datasheet graph C_{OSS} vs. V_{DS}) and the average value of the peak current flowing through the inductor:

Equation 51

(51)

$$t_{rise} \cong \frac{C_D \cdot V_{DS}}{I_D} \cong \frac{C_D \cdot V_{OUT}}{\frac{1}{\pi} \cdot \int_0^{\pi} I_{L\_PK,max}} = C_D \cdot V_{OUT} \cdot \frac{V_{AC} \cdot PF}{\sqrt{2} \cdot P_{OUT}/\eta}$$

where C_D is the total capacitance afferent to the drain node ($C_D = C_{OSS} \cdot N_{mos} + C_{stray}$).

The average falling time depends on the driving current I_G (limited by the resistor R_{G_ON} placed on the gate), the MOSFET's total gate charge Q_G and the driving voltage V_{DR}. It can be estimated with the following relationship:

Equation 52

(52)

$$t_{fall} \cong \frac{Q_G}{8V} \cdot \left(\frac{R_{G\_ON}}{6.8} + R_{G\_MOS}\right),$$

where R_{G_MOS} is the intrinsic gate resistance of the power MOSFET.

To estimate the capacitive losses (P_{cap}), that is the losses due to the discharge of the total drain capacitance through the MOSFET at turn-on, this simple expression can be considered:

Equation 53

(53)

$$P_{cap} \cong \frac{1}{2} \cdot C_D \cdot {V_{OUT}}^2 \cdot F_{sw}\ ,$$

Finally, based on the total power losses value (results of equation #41) and based on the maximum acceptable MOSFET's junction temperature target (e.g. $T_{j\_mos,max}$=125 °C), it is possible to calculate the maximum thermal resistance of the heatsink required to keep the MOSFET's junction temperature below $T_{j\_mos,max}$:

Equation 54

(54)

$$R_{th} \cong \frac{T_{j\_mos,max} - T_{amb,max}}{P_{loss}}\ .$$

3.6 Boost diode (D_{out})

Following criteria similar to that used for MOSFET losses calculation, the output rectifier can be properly selected. A minimum breakdown voltage of 1.2·(V_{OUT}) and a current rating higher than 3·I_{OUT_MAX} can be considered for a rough selection of the rectifier. The correct selection is then confirmed by the thermal calculation, as the diode junction temperature needs to work within 125 °C. Since this circuit operates in the continuous current mode, the reverse recovery is experienced by the diode, and the MOSFET at turn-on has to carry also the boost diode minority carrier charge. Then to minimize the recovery losses an ultra-fast diode with low t_{rr} (reverse recovery time, the time required to deplete the stored charge) and Q_{rr} (reverse recovery charges, the charge that must be dissipated on the MOSFET) or a SiC rectifier has to be selected. The total diode losses are:

Equation 55

(55)

$$P_{diode} = P_{cond\_diode} + P_{rr\_diode}.$$

The conduction losses P_{cond_diode} can be estimated by:

Equation 56

(56)

$$P_{cond\_diode} = V_{th\_diode} \cdot I_{OUT} + R_{d\_diode} \cdot I_{D,rms}^{2} ,$$

where V_{th_diode} and R_{d_diode} are the rectifier threshold voltage/dynamic resistance respectively, and the diode RMS current can be estimated by:

Equation 57

(57)

$$I_{D,rms} = \frac{P_{OUT}/\eta}{\sqrt{2} \cdot V_{AC} \cdot PF} \cdot \sqrt{\frac{16 \cdot \sqrt{2} \cdot V_{AC}}{3\pi \cdot V_{OUT}}} .$$

The reverse recovery losses can be estimated by:

Equation 58

(58)

$$P_{rr} = V_R \cdot Q_{rr} \cdot F_{sw}$$

where V_R is the reverse voltage across the output diode when it stops conducting (V_R= V_{OUT}), and Q_{rr} the reverse recovery charges (see diode datasheet on www.st.com) that must be dissipated through the MOSFET.

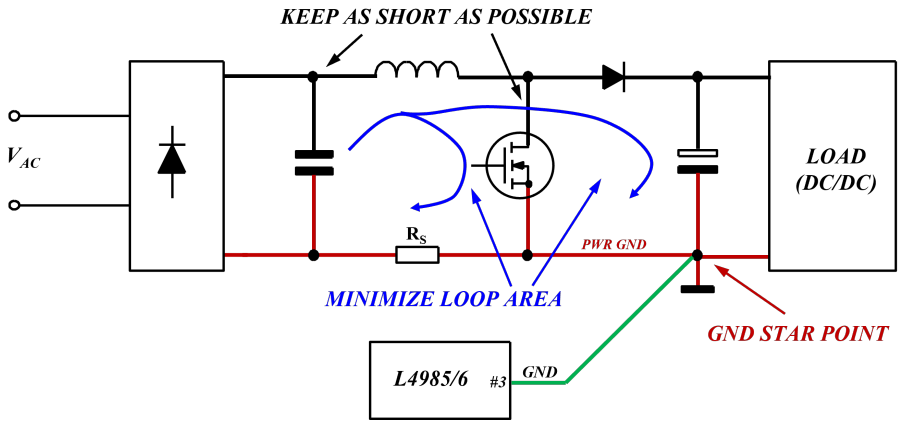
4 PCB layout guidelines

The L4985/L4986 does not need any special attention to the layout, only requiring that the general layout rules for any switching power converter be carefully applied.

Basic rules are listed here below:

- Keep the power and signal GND separated. Connect the return pins of the components carrying the high current switched at high frequency such as the PFC sense resistor, the PFC MOSFET source and the output capacitors as close as possible. This point is the GND star point. A downstream converter must be connected to this return point.
- Connect the GND pin (#3) to the GND star point making the connections as short as possible and using a track width suitable to minimize its impedance. Keep this connection separated from any other GND connection, especially if carrying high currents.
- Place the VCC ceramic filter capacitor (e.g., 100 nF÷1 µF) close to the L4985/6 controller, connecting it to the VCC pin (#1) and to the GND pin (#3).
- Minimize the length of the traces relevant to the boost inductor, MOSFET's drain, boost rectifier and the output capacitor.

Figure 15. Power section and GND connections.



- Keep signal components as close as possible to each relevant pin of L4985/L4986. Specifically, components and traces relevant to CS, FB, PG_IN and COMP pins have to be placed far from traces and connections carrying signals with high dV/dt, such as the MOSFET's drain.
- The tracks relevant to the whole net of the FB pin (#5 in L4985 and #7 in L4986) and PG_IN pin (#5 in L4986) have to be as short as possible and far from high dV/dt signal tracks. Because of its high impedance, the pin could pick up noise affecting the PFC operation. If an additional circuit is used to pull down the FB pin (e.g., to use the External Burst-Mode function), it has to be placed close to the pin itself.
- Place the high frequency ceramic filtering capacitor (e.g., 100 pF÷470 pF) of FB, PG_IN and CS pin close to L4985/L4986.
- The tracks relevant to the whole net of the HV pin (#8 in L4985 and #10 in L4986) have to be placed far from high dV/dt signal tracks. Because of its high impedance, the pin could pick up noise affecting the PFC operation (e.g., the THD-CCM optimizer performance).
- Connect heatsinks to power GND.
- Add an external shield to the boost inductor and connect it to power GND.

5 Design example

A 350 W wide-input range PFC circuit is considered, with the following target specifications:

- AC line voltage range (rms): $V_{AC,min}$ = 85 V, $V_{AC,max}$ = 265 V
- Minimum line frequency: $f_{LINE,min}$ = 47 Hz (nominal 50 Hz, 60 Hz)
- Nominal output voltage: V_{OUT} = 400 V
- Rated output power: $P_{OUT,max}$ = 350 W
- Rated output current: $I_{OUT,max}$ = 0.875 A
- Nominal switching frequency: F_{SW} = 65 kHz
- Expected efficiency at $V_{AC,min}$: η = 0.99
- Expected power factor at $V_{AC,min}$: η = 0.95
- Ripple input voltage coefficient: r = 5%
- Maximum output low-frequency ripple (peak-to-peak): ΔV_{OUT} = 15 V
- Hold-up time and minimum output voltage: T_{hold} = 10 ms, V_{OUT_MIN} = 340 V
- Inductor ripple factor: K_r = 0.35
- Warning output voltage: V_{OUT_PGOFF} = 300 V
- System stability: Φ_m = 45° (phase margin), D_3 = 4% (maximum third-harmonic distortion)
- Maximum ambient temperature: 50 °C

5.1 Power section

Bridge rectifier

Considering that the RMS current into the bridge diode is (from equation #35):

$$I_{in,rms\_bridge} = \frac{\sqrt{2}}{2} \cdot \frac{\frac{P_{OUT}}{\eta}}{V_{AC} \cdot PF} = \frac{\sqrt{2}}{2} \cdot \frac{\frac{350W}{0.93}}{90V \cdot 0.99} = 2.98\ A\ ,$$

the sinusoidal peak value of the AC current results (from equation #34):

$$I_{pk,avg\_bridge} = \sqrt{2} \cdot I_{in,rms\_bridge} = \sqrt{2}\ \cdot 2.98A\ = 4.24A\ ,$$

then a bridge diode D15XB60H is selected (600 V, 15 A/3.5 A). Assuming V_{th_diode} = 1 V and R_{diode} = 25 mΩ (from the device datasheet), the estimated total power dissipation of the bridge diode results (from equation #36):

$$P_{bridge} = 4 \cdot R_{diode} \cdot I_{in,rms\_bridge}{}^2 + 4 \cdot V_{th,diode} \cdot \left(\frac{2}{\pi} \cdot I_{in,rms_{bridge}}\right) = 4 \cdot 25m\Omega\ \cdot 2.98A^2 + 4 \cdot 1V \cdot \left(\frac{2}{\pi} \cdot 2.98A\right) = 8.47\ W\ .$$

To keep the junction temperature of the bridge diode below 125 °C ($T_{j\_bridge,max}$), a heatsink should be needed with a thermal resistance below (from equation #37):

$$R_{th} \cong \frac{T_{j\_bridge,max} - T_{amb,max}}{P_{bridge}} = \frac{125℃ - 50℃}{8.47W} = 8.8℃/W$$

Boost inductor

Considering an inductor ripple factor Kr=0.35, the required minimum boost inductor L_p results (from equation #41):

$$L_p = \eta \cdot \frac{V_{AC\_min}{}^2}{K_r \cdot F_{SW,min} \cdot P_{OUT\_max}} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{AC\_min}}{V_{OUT}}\right) = 0.93 \cdot \frac{90V^2}{0.35 \cdot 60kHz \cdot 350W} \cdot \left(1 - \frac{\sqrt{2} \cdot 90V}{400V}\right) = 699\ \mu H\ ,$$

A nominal inductor L_p=700 µH is selected.

Input capacitor

The minimum required input filter capacitor C_{IN} based on the practical formula is (from equation #42):

$C_{in\_min} = 2.5 \cdot 10^{-3} \cdot \frac{\mu F}{W} \cdot P_{OUT\_max} = 2.5 \cdot 10^{-3} \cdot \frac{\mu F}{W} \cdot 350W = 0.875\ \mu F$,

whereas to respect the input ripple voltage r of 5% is (from equation #43):

$$C_{in\_ripple} = \frac{K_r \cdot \sqrt{2} \cdot P_{OUT,max}}{2\pi \cdot F_{SW} \cdot r \cdot \eta \cdot {V_{AC\_min}}^2} = \frac{0.35 \cdot \sqrt{2} \cdot 350W}{2\pi \cdot 65kHz \cdot 0.05 \cdot 0.93 \cdot 90V^2} = 1.04\ \mu F .$$

A value of 1 µF/277 V_{AC} is selected.

Output capacitor

The minimum output capacitor C_{out} to achieve the desired voltage ripple is (from equation #44):

$$C_{out\_ripple} = \frac{I_{OUT,max}}{2\,\pi \cdot f_{LINE,min} \cdot \Delta V_{OUT}} = \frac{0.875A}{2\,\pi \cdot 47Hz \cdot 15V} = 197\ \mu F ,$$

and to achieve the desired hold-up time is (from equation #45):

$$C_{out\_holdup} = \frac{2 \cdot P_{OUT,max} \cdot T_{hold}}{\left(V_{OUT} - \frac{\Delta V_{OUT}}{2}\right)^2 - \left(V_{OUT\_MIN}\right)^2} = \frac{2 \cdot 350W \cdot 10ms}{\left(400V - \frac{15V}{2}\right)^2 - (340V)^2} = 182\ \mu F ,$$

A value of C_{out} = 200 µF is selected, using two capacitors of commercial value of 100 µF/450 V placed in parallel.

Power MOSFET

A 600 V/99 mΩ_{max} in TO-220FP power MOSFET is selected (STF36N60M6), as a good balance between the minimum break-down voltage (600 V) and static/dynamic performances ($R_{DS(on)}$/C_{oss}). Typically the maximum power losses are at minimum input voltage ($V_{AC,min}$), then the RMS current flowing into the power switch is (from equation #48):

$$I_{sw,rms} = \frac{P_{OUT}/\eta}{\sqrt{2} \cdot V_{AC} \cdot PF} \cdot \sqrt{2 - \frac{16 \cdot \sqrt{2} \cdot V_{AC}}{3\pi \cdot V_{OUT}}} = \frac{\frac{350W}{0.93}}{\sqrt{2} \cdot 90V \cdot 0.99} \cdot \sqrt{2 - \frac{16 \cdot \sqrt{2} \cdot 90}{3\pi \cdot 400V}} = 3.6\ A ,$$

then, considering 100 °C as maximum junction temperature of the power MOSFET (1.7 as multiplier factor for the $R_{DS(on)}$), the estimated conduction losses result (from equation #47):

$$P_{cond} = R_{dson} \cdot {I_{sw,rms}\left(V_{AC,min}, P_{OUT\_MAX}\right)}^2 = (99m\Omega \cdot 1.7) \cdot 3.6A^2 = 2.2\ W .$$

Assuming a stray capacitance of 100 pF and considering the typical C_{OSS} of the power MOSFET at 400 V (around 60 pF from the C_{OSS} vs. V_{DS} graph in the datasheet), the total capacitance afferent to the drain node is about 160 pF and the estimated rise time results (from equation #51):

$$t_{rise} \cong C_D \cdot V_{OUT} \cdot \frac{\frac{V_{AC} \cdot PF}{\sqrt{2} \cdot P_{OUT}}}{\eta} = 160pF \cdot 400V \cdot \frac{\frac{90V \cdot 0.99}{\sqrt{2} \cdot 350W}}{0.93} = 10.7\ ns$$

Considering the driving voltage V_R = 12 V, the total gate charge Q_G of the MOSFET is around 50 pF (see gate charge vs. gate-source voltage graph in the datasheet on www.st.com) and the intrinsic gate resistance R_{G_MOS} is 1.6 Ω typ.; assuming an external gate resistance R_{G_ON} of 6.8 Ω, the estimated fall time results (from equation #52):

$$t_{fall} \cong \frac{Q_G}{8V} \cdot \left(\frac{R_{G\_ON}}{6.8} + R_{G\_MOS}\right) = \frac{50nC}{8V} \cdot \left(\frac{6.8\Omega}{6.8} + 1.6\right) = 16.2\ ns .$$

The switching power losses, at the minimum input voltage, then results (from equation #50):

$$P_{sw} = \frac{1}{2} \cdot V_{OUT} \cdot I_{SW,rms}\left(V_{AC,min}\right) \cdot \left(t_{rise} + t_{fall}\right) \cdot F_{sw} = \frac{400V}{2} \cdot 3.6A \cdot (10.7ns + 16.2ns) \cdot 65kHz = 1.26\ W$$

The estimated capacitive losses (from equation #53) are:

$$P_{cap} \cong \frac{1}{2} \cdot C_D \cdot {V_{OUT}}^2 \cdot F_{sw} = \frac{1}{2} \cdot 160pF \cdot 400V^2 \cdot 65kHz = 0.83\ W$$

The total estimated losses for the power switch, at the minimum input voltage and maximum output power, are then (from equation#46):

$$P_{loss} = P_{cond}\left(V_{AC,min}, P_{OUT\_MAX}\right) + P_{sw}\left(V_{AC,min}, P_{OUT\_MAX}\right) + P_{cap} = 2.2W + 1.26W + 0.83W = 4.2\ W.$$

To keep the junction temperature of the MOSFET below 125 °C ($T_{j\_mos,max}$), a heatsink should be needed with a thermal resistance below (from equation #54):

$$R_{th} \cong \frac{T_{j\_mos,max} - T_{amb,max}}{P_{bridge}} = \frac{125°C - 50°C}{4.2W} = 17.8°C/W .$$

Output diode

Finally, considering the criteria for the output boost diode (minimum 1.2*V_{OUT} = 480 V and 3*I_{OUT_MAX} = 2.625 A), the silicon carbide STPSC8H065 (in TO-220 AC insulated package) is selected (650 V/8 A). Considering that the current flowing in the output diode is (from equation #57):

$$I_{D,rms} = \frac{P_{OUT}/\eta}{\sqrt{2}\cdot V_{AC}\cdot PF}\cdot\sqrt{\frac{16\cdot\sqrt{2}\cdot V_{AC}}{3\pi\cdot V_{OUT}}} = \frac{\frac{350W}{0.93}}{\sqrt{2}\cdot 90V\cdot 0.99}\cdot\sqrt{\frac{16\cdot\sqrt{2}\cdot 90V}{3\pi\cdot 400V}} = 2.2\ A\ ,$$

and that the threshold voltage/dynamic resistance are around 1.35 V/144 mΩ (from datasheet on www.st.com), the estimated conduction losses result (from equation #56):

$$P_{cond\_diode} = V_{th\_diode}\cdot I_{OUT} + R_{d\_diode}\cdot {I_{D,rms}}^2 = 1.35V\cdot 0.875A + 144m\Omega\cdot 2.2^2 = 1.87\text{W}.$$

The reverse recovery charge Q_{rr} is around 24 nC (see device datasheet on www.st.com), then the reverse recovery losses are (from equation #58):

$$P_{rr} = V_R\cdot Q_{rr}\cdot F_{sw} = 400V\cdot 24nC\cdot\ 65kHz = 0.62W.$$

Finally, the total diode losses are (from equation #55):

$$P_{diode} = P_{cond\_diode} + P_{rr\_diode} = 1.87W + 0.62W = 2.49W\ .$$

5.2 Biasing circuitry

Output resistors divider and power good setting

Assuming a power dissipation P_d of 25 mW for the output resistors divider, the upper resistor R_{FB_H} is (from equation #6):

$$R_{FB\_H}\ \cong\ \frac{{V_{OUT}}^2}{P_d} = \frac{400V^2}{25mW} = 6.4\ M\Omega$$

An equivalent resistor of 6.6 MΩ is selected (three resistors of 2.2 MΩ in series to sustain the high-voltage drop), then, considering that the L4985/L4986 reference voltage V_{REF} is 2.5 V typ., the lower resistor R_{FB_L} results (from equation #7):

$$R_{FB\_L} = R_{FB\_H}\cdot\frac{V_{REF}}{V_{OUT}-V_{REF}} = 6.6M\Omega\cdot\frac{2.5V}{400V-2.5V} = 41.50\ k\Omega$$

Considering the PGOOD requirements (PG_OUT pin released as soon as V_{OUT} lower than the output warning voltage V_{OUT_PGOFF}) and that the L4985/L4986 V_{PGOOD_OFF} threshold is 1.250 V typ., the lower resistor results (from equation #30):

$$R_{FB\_L1} = \frac{V_{PGOOD\_OFF}}{V_{OUT\_PGOFF}}\cdot\left(R_{FB\_H}+R_{FB\_L}\right) = \frac{1.250V}{300V}\cdot(6.6M\Omega + 41.5k\Omega) = 27.67\ k\Omega.$$

A value of 27.69 kΩ is selected (two resistors in parallel, 30kΩ // 360kΩ).

The lower resistor R_{FB_L2} then results (from equation #31):

$$R_{FB\_L2} = R_{FB\_L} - R_{FB\_L1} = 41.50k\Omega - 27.69\text{k}\Omega = 13.82\ \text{k}\Omega\ .$$

A value of 13.79 kΩ is selected (two resistors in parallel, 16kΩ // 100kΩ).

Current sense resistor

The minimum value of the OCP1 threshold is $V_{CS\_OCP1,min}$ = 0.47 V (from the L4985/L4986 datasheet), then to respect the dynamic of the CS pin the maximum current sense resistor should be (from equation #8):

$$R_{S\_OCP1} = V_{CS\_OCP1,min}\cdot\frac{\eta\cdot V_{AC,min}}{\sqrt{2}\cdot P_{OUT,max}} = 0.47V\cdot\frac{0.93\ \cdot 90V}{\sqrt{2}\cdot 350W} = 79\ m\Omega.$$

The minimum value of the upper COMP pin voltage $V_{COMP,min}$ is 5.0 V (from the L4985/L4986 datasheet), then to respect the dynamic of the COMP pin the maximum current sense resistor should be (from equation #10):

$$R_{S\_COMP} = \left(V_{COMP,min} - 1V\right)\cdot K_M\cdot\frac{{V_{AC,min}}^2}{P_{OUT\_max}\cdot V_{OUT}} = (5V-1V)\cdot 0.44\cdot\frac{90V^2}{350W\cdot 400V} = 101\ m\Omega.$$

where for the equivalent multiplier gain $K_M$for V_{AC} = 90 V is 0.44 (see L4985/L4986 datasheet).

An equivalent resistor of 73 mΩ is selected, composed by three resistors of 0.220Ω (Metal film resistor, 1W, 5%) in parallel to sustain the power dissipation

THD-CCM optimizer resistor

Considering the typical gain of the THD-CCM circuitry (K_{CCM} = 0.55 from the L4985/L4986 datasheet), then the optimizer resistor R_{THD_CCM} is (from equation #12):

$$R_{THD\_CCM} = K_{CCM} \cdot \frac{R_S}{L_P} = 0.55 \cdot \frac{73m\Omega}{700\mu H} = 57\ \Omega\,.$$

A value of 56 Ω is selected.

Compensation Network

The maximum output voltage ripple ΔV_{OUT} is (from equation #20):

$$\Delta V_{OUT} = \frac{I_{OUT\,.max}}{2\,\pi \cdot f_{LINE} \cdot C_{OUT}} = \frac{0.875A}{2\,\pi \cdot 47Hz \cdot 200\mu F} = 14.81\,V\,,$$

and the V_C control voltage set-point, calculated at the maximum input voltage and rated output power is (from equation #9):

$$V_C = R_S \cdot \frac{1}{K_M} \cdot \frac{\frac{P_{OUT}}{\eta} \cdot V_{OUT}}{{V_{AC}}^2} = 73m\Omega \cdot \frac{1}{0.1} \cdot \frac{\frac{350W}{0.93} \cdot 400V}{265V^2} = 1.56\,V$$

where the internal equivalent multiplier gain K_M for V_{AC} = 265 V is 0.1 (see L4985/L4986 datasheet on www.st.com).

Then, to limit the third-harmonic distortion D_3 at 4%, the compensation network gain at $2 \cdot f_{LINE}$ has to be (from equation #24):

$$H_{2f} = \frac{2 \cdot D_3 \cdot (V_{COMP} - V_{C0})}{\Delta V_{OUT}/2} = \frac{2 \cdot 0.04 \cdot 1.56V}{14.81V/2} = 0.016,$$

and the suggested C_{FP} capacitor results (from equation #27 and considering g_{m_EA} = 200 µS typ. from the L4985/L4986 datasheet on www.st.com):

$$C_{FP} = \frac{g_{m\_EA} \cdot R_{FB\_L}}{R_{FB\_L} + R_{FB\_H}} \cdot \frac{1}{2\pi \cdot 2f_{LINE} \cdot H_{2f}} = \frac{200\mu S \cdot 41.5k\Omega}{(41.5k\Omega + 6.6M\Omega)} \cdot \frac{1}{2\pi \cdot 2 \cdot 47Hz \cdot 0.016} = 132\,nF\,.$$

The selected value is C_{FP} = 150nF.

The suggested frequency of the zero for the compensation network is (from equation #25):

$$f_z = f_{p\_co} = \frac{1}{2\,\pi \cdot R_{OUT} \cdot C_{OUT}} = \frac{1}{2\,\pi \cdot 400V/0.875A \cdot 200\mu F} = 1.74\,Hz\,.$$

The dc-gain of the control-to-output function is (considering that K_M = 0.1 for V_{AC} = 265 V):

$$G_o = \frac{K_M}{2R_S} \cdot \frac{{V_{IN,pk}}^2}{{V_{OUT}}^2} \cdot R_{OUT} = \frac{0.1}{2 \cdot 73m\Omega} \cdot \frac{(\sqrt{2} \cdot 265V)^2}{400V^2} \left(\cdot \frac{400V}{0.875A} \right) = 274.8$$

then considering a phase margin Φ_m of 45°, the suggested frequency of the pole for compensation network is (from equation #26):

$$f_p = \sqrt{\frac{f_z \cdot 2\,f_{LINE} \cdot H_{2f} \cdot G_o \cdot tan\left(\frac{\pi}{180} \cdot \Phi_m\right)}{\sqrt{1 + \frac{1}{\left(tan\left(\frac{\pi}{180} \cdot \Phi_m\right)\right)^2}}}} = \sqrt{\frac{1.74Hz \cdot 2 \cdot 47Hz \cdot 0.016 \cdot 274.8 \cdot tan\left(\frac{\pi}{180} \cdot 45\right)}{\sqrt{1 + \frac{1}{\left(tan\left(\frac{\pi}{180} \cdot 45\right)\right)^2}}}} = 22.3\,Hz$$

the result suggested C_{FS} capacitor is (from equation #28):

$$C_{FS} = C_{FP} \cdot \frac{f_p - f_z}{f_z} = 150nF \cdot \frac{22.3Hz - 1.74Hz}{1.74Hz}\,. = 1776\,nF$$

The selected value is C_{FS} = 1500 nF.

Finally, the suggested R_{FS} resistor is (from equation #29):

$$R_{FS} = \frac{1}{2\,\pi \cdot f_z \cdot C_{FS}} = \frac{1}{2\,\pi \cdot 22.3Hz \cdot 1500nF} = 60.9\,k\Omega\ .$$

The selected value is R_{FS} = 62 kΩ.

6 Reference

1. L4985 datasheet - www.st.com
2. L4986 datasheet - www.st.com
3. G. Gritti, C. Adragna “Novel Approach to Current-mode Control in DCM/CCM Boundary Boost PFC”, Applied Power Electronics Conference and Exposition, 2016. APEC '16, Conference Proceedings 2016, pp. 564-571, March 2016.
4. G. Gritti, “Novel Adaptive Pulse Width Modulator provides Quasi-Fixed Switching Frequency in Constant On/Off-Time controlled regulators”, Applied Power Electronics Conference and Exposition, 2018. APEC '18, Conference Proceedings 2018, pp. 760-766, March 2018.

Revision history

Table 1. **Document revision history**

Date	Version	Changes
01-Dec-2021	1	Initial release.

Contents

List of tables

List of figures