AN5754

Application note

L9680 Cut-off Battery and Pyro Fuse

Introduction

This document explains the features and benefits of the L9680 device in order to be used in the Pyro Fuse application: the device activates the Pyro Fuse that disconnects a battery from an electrical system, so that the battery will not become a source of ignition.

The main features are the flexible configuration, availability of different voltage regulators, four PSI-5 sensor interfaces, four wheel speed sensor interfaces, nine DC sensors interface, three GPOs, high or low level diagnostic test, arming procedure following both internal or external safing engine, deployment profile selectable, 32 bits SPI communication.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

1 Description

The L9680 is an advanced system chip solution targeted for cut-off battery market. This device is family compatible with L9678, L9679P and L9679E devices.

Safety system integration is enabled through higher power supply currents and an integrated active wheel speed sensor interface. The active wheel speed interface is shared with the PSI-5 satellite interface to create a generic remote safety sensor interface compliant to both systems.

1.1 Main features

The main features are:

- Energy reserve voltage power supply - ERBOOST
  - High frequency boost regulator, 1.882 MHz
  - Output voltage user selectable, 23 V or 33 V ± 5%
  - Measurement of reserve capacitor value & ESR diagnostics
- Output voltage regulator power supply for PSI-5 SYNC pulse - SYNCBOOST
  - High frequency boost regulator, 1.882 MHz
  - Output voltage user selectable, 12 V or 14.75 V ± 5%
- Output voltage regulator power supply for remote sensors - SATBCK
  - High frequency buck converter, 1.882 MHz
  - Output voltage user selectable, 7.2 V or 9 V ± 4%
- Output voltage regulator power supply for logic - VCC
  - High frequency buck converter, 1.882 MHz
  - Output voltage user selectable via VCCSEL pin, 3.3 V or 5 V ± 4%
- Integrated crossover switch
  - Crossover performance 3 Ω - 912 mA max
  - Switch active output indicator
- Battery voltage monitor and shutdown control with wake-up control
- System voltage diagnostics with integrated ADC Squib deployment drivers
  - 12 channel HSD/LSD
  - 25 V max deployment voltage
  - Various deployment profiles, 1.2 A/1.75 A, x*0.064 ms up to 4.032 ms
  - Current monitoring
  - Rmeasure, STB, STG & Leakage diagnostics
  - High & Low Side driver FET tests
  - Safing FET test
- High Side safing switch regulator and enable control
- Four-channel interface for PSI-5 (synchronous mode) remote sensors and four channels interface for active wheel speed sensors
- Three-channel GPO, HSD or LSD configurable, with PWM 0-100% control
- Nine-channel interface for Hall-effect, resistive or switch sensors
- User customizable safing logic
- Specific disarm signal for passenger airbag (PSINHB)
- Temporal and Algorithmic Watchdog timers
- End of life disposal interface
- 32 bits SPI communications
- Minimum operating voltage = 5.5 V
- Operating temperature, -40 °C to 95 °C
- Packaging: 100 pin

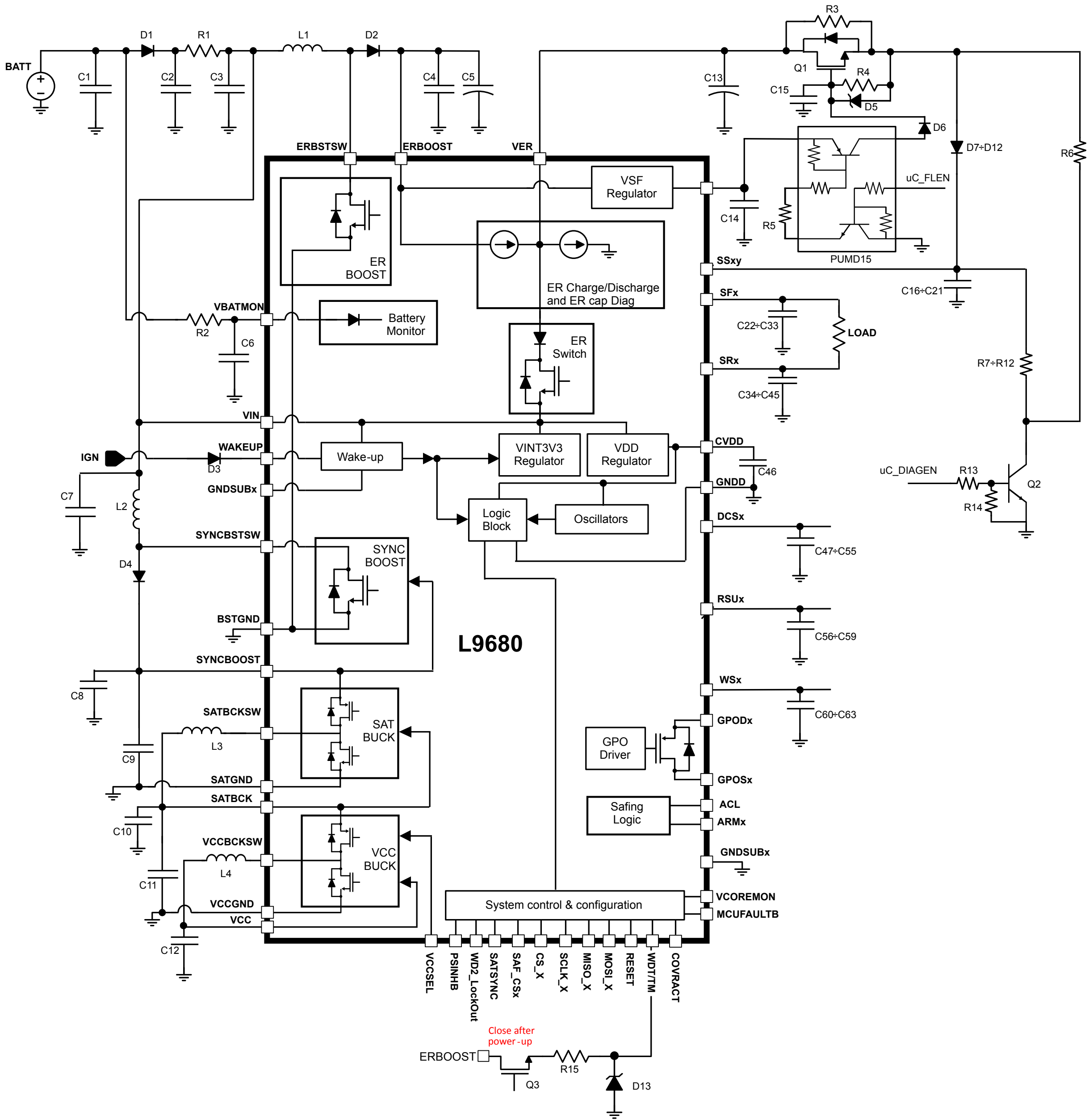
1.2 Application overview

The device has been designed for Airbag Application, but if correctly configured it can be used also for Pyro Fuse Application, i.e. to cut-off the battery from an electrical system.

In fact, in case of a crash, a short circuit on the battery due to damaged cables can lead to sparks and dangerous ignition or heat and moldering fires. Thus it is important to disconnect the electrical system from the battery using pyrotechnical safety battery terminals.

These special Pyro Fuses have electrical characteristics like those of Airbag detonators. Some Pyro Fuses can require a bigger current to be triggered. In this case some deployment channels can be shorted and connected to the same load in order to obtain a total current higher than 2 A.

Figure 1. Pyro Fuse application circuit



2 Device configuration

The user shall configure the device following the Application Note AN5023, in particular about:
- Voltage Regulators
- Safing Logic
- Deployment
- Remote Sensor Interface (wheel speed sensors or PSI-5 sensors)
- DC Sensor Interface
- GPO Drivers

Furthermore, the user could use the same document to know about:
- System Voltage Diagnostic
- Temperature Sensor

In the following section a deployment example will be shown.

2.1 Unused functions

In case some functions are not used, the correspondent pins have to be managed as in the Table 1.

Table 1. Unused functions management

Pin	Action
WS0, WS1, WS2, WS3	Open (by default they are off)
RSU0, RSU1, RSU2, RSU3	Open (by default they are off)
DCS0, DCS1, DCS2, DSCS3, DCS4, DCS5, DCS6, DCS7, DSCS8	Open (weak pull-down integrated)
GPOD0, GPOS0, GPOD1, GPOS1, GPOD2, GPOS2	Open (by default they are off)
SATSYNC	Connect to GND
VCOREMON	Connect to GND
MCUFAULTB	Connect to VCC
PSINHB	Connect to VCC (it is active low)
SAF_CS0, SAF_CS1, SAF_CS2, SAF_CS3	Connect to VCC (they are active low)
ACL	Connect to GND

3 Deployment

The features are:

- 12 independent loops composed by 12 independent High Side and 12 independent Low Side.
- In case the Low Side SRx is shorted to ground, the deployment, if requested, is guaranteed to succeed.
- In any case, SSxy voltage has to be lower than 25 V.
- Both High Side and Low Side are equipped with a passive turn-off to guarantee that they are always in off state except when the deployment has to take place.

3.1 Deployment requirement

Deployment features are deployment current, deployment time and deployment expiration time. The deployment expiration time is the duration time in which the deploy command remains valid, once it is received, waiting for the arming signal.

These parameters are defined through the twelve registers DCR_X, with X=0-B, configurable in DIAG, SAFING, SCRAP, and ARMING state, as shown in the Table 2:

- $06 DCR_0 → channel 0
- $07 DCR_1 → channel 1
- $08 DCR_2 → channel 2
- $09 DCR_3 → channel 3
- $0A DCR_4 → channel 4
- $0B DCR_5 → channel 5
- $0C DCR_6 → channel 6
- $0D DCR_7 → channel 7
- $0E DCR_8 → channel 8
- $0F DCR_9 → channel 9
- $10 DCR_A → channel A
- $11 DCR_B → channel B

All deployment configuration registers are reset by SSM reset.

Table 2. **DCR_x register**

	(1)	(2)	19:16	15:12	11:6	5:4	3:2	1	0
$06 DCR_0 to $11 DCR_B	(I)	W	-	X	Deploy_time = 0.064 ms/count * depl_time ≤ 4.032 ms	Deploy_current 00, 11 = not used 01 = 1.75 A min 10 =1.2 A min	Deploy_expire_time 00 = 500 ms 01 = 250 ms 10 = 125 ms 11 = 0 ms	X	PD_CURR_CSR

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The Deploy Time field allows the device to deploy for a maximum configurable time of 4.032 ms (64 µs each step).

Differently from the L9678 device, there is no inhibition of the combination 1.75A/2 ms, so it is under user's responsibility to prevent excessive thermal heating in the squib driver section by setting the deploy parameters carefully.

In case the deployment minimum current is set at 1.75 A, it is recommended:

- for deployment times between 0.7 ms and 2 ms, to limit the voltage drop across the pins to 17 V max.
- for deployment times up to 3.2 ms, to limit the voltage drop across the pins to 15 V max.

In case the deployment minimum current is set at 1.2 A, it is recommended:

- for deployment times between 2 ms and 3.2 ms, the voltage drop across the pins is limited to 22 V max.

The voltage values 15 V, 17 V, 22 V, relevant for long deploy time, depend on the squib resistance value being the voltage across the High Side power (SSxy - SFx(y)) roughly VSF - RSQUIB * I.

The parameters in each DCR_x register have to be confirmed at least the first time the device has to deploy, even in case they are left at their default value; the deployment does not occur otherwise.

The status of each loop is monitored in the DSR_X registers, one for each channel, as shown in the Table 3:

Table 3. DSR_x register

	(1)	(2)	19:16	15	14	13	12	11:6	5:0
$13 DSR_0 to $1E DSR_B		R	0	CHxDSX 0 depl not succesful 1 depl succesful	CHxSTAT 0 depl not in progress 1 depl in progress	0	DCRxERR 0 depl conf accepted and stored 1 depl conf change not accepted because deploy is in progress	0	DEP_CHx_EXP_TIME 8 ms/count

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

For each channel, the deploy requires:

- High Side and Low Side enabling.
- High Side and Low Side switching.

The Figure 2 and Figure 3. High Side and Low Side squib enable show the states of the IC and the signal paths which enable the High Side and Low Side MOSFETs.

Figure 2. System operating state diagram

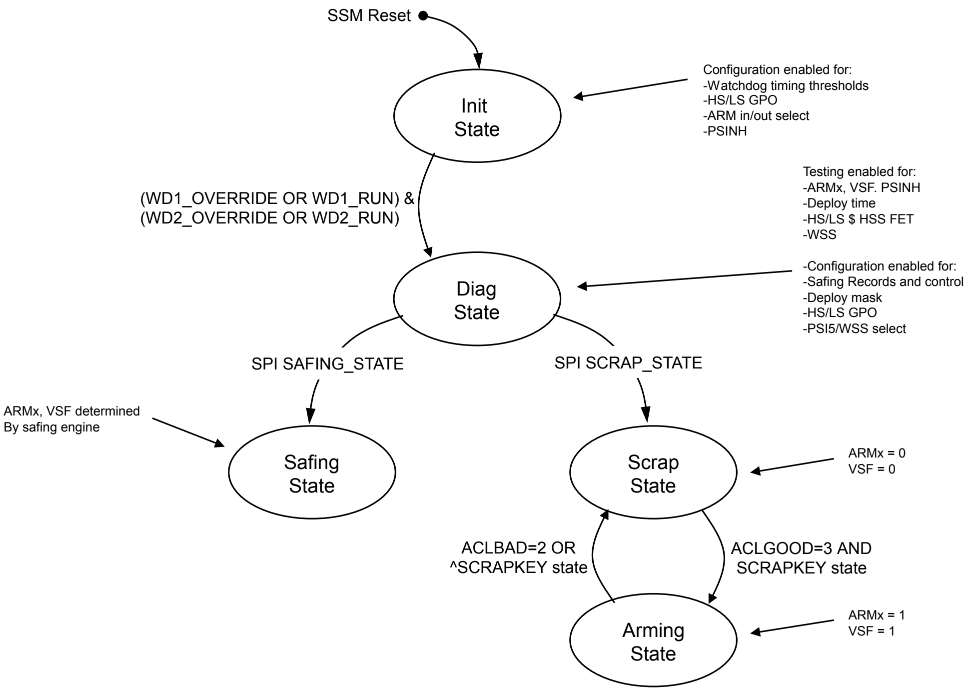
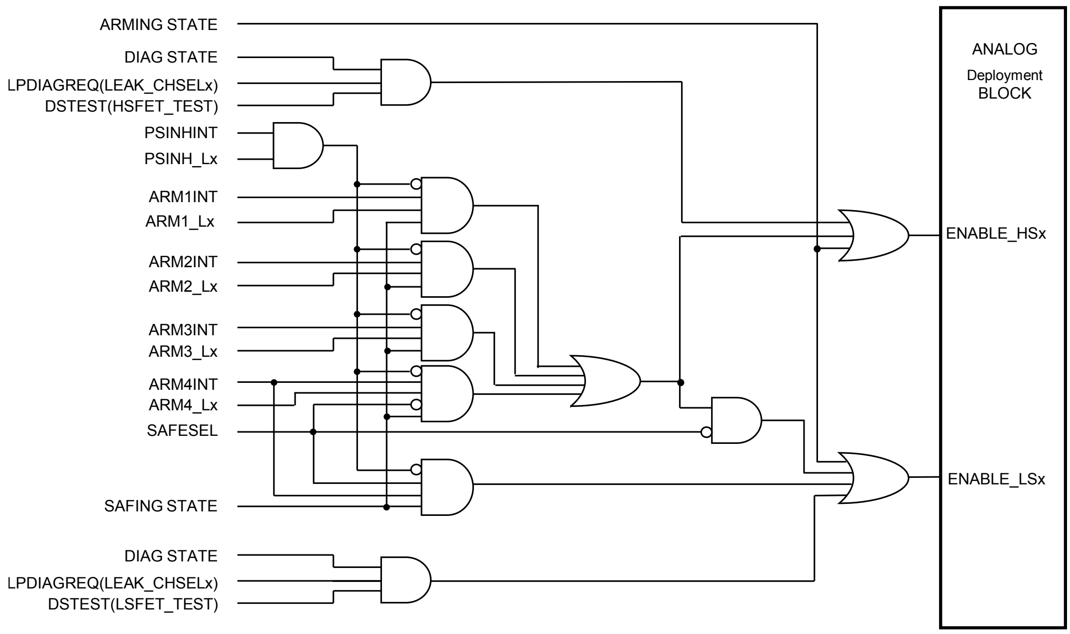


Figure 3. High Side and Low Side squib enable



3.1.1 Diagnostic state

In DIAGNOSTIC state it is possible to perform the High Side FET test and Low Side FET test.

These tests require a sequence of steps:

1. Select the channel (refer to the Table 4);
2. Select High Side FET test or Low Side FET test (refer to the Table 5).

Table 4. LPDIAGREQ register - LEAK_CHSEL bits

$38 LPDIAGREQ	Config in DIAG, SAFING, SCRAP, ARMING state
LEAK_CHSEL, bit[3:0]	0000 = CHANNEL 0 0001 = CHANNEL 1 0010 = CHANNEL 2 0011 = CHANNEL 3 0100 = Channel 4 0101 = Channel 5 0110 = Channel 6 0111 = Channel 7 1000 = Channel 8 1001 = Channel 9 1010 = Channel A 1011 = Channel B 0100 - 1111 None Selected

Table 5. SYSDIAGREQ register - DSTEST bits

$36 SYSDIAGREQ	Config in DIAG state
DSTEST, bit[3:0]	0111 = High Side FET test active 1000 = Low Side FET test active

Once deploy parameters have been set, it is required to assign the channels to deployment loops. This allows deploying different channels basing on the arming result.

The combination channels-deployment loop is fixed via SPI considering that external and internal arming is different, according to the SAFESEL bit (see the Table 6).

Table 6. SYS_CSF register - SAFESEL bit

$01 SYS_CFG	Config in INIT state
SAFESEL, bit[3]	0 = internal safing engine 1 = external safing engine (default)

In case of the **external safing engine** (SAFESEL = 1), three deployment loops are available, each of them associated to ARM1, ARM2, ARM3 pin to activate the High Sides, while ARM4 pin is common for all and is used to activate the Low Side FETs.

In case of **internal safing engine** (SAFESEL = 0), four deployment loops are available and defined in the LOOP_MATRIX_ARMx registers.

It is recommended to keep ARM1, ARM2, ARM3 and ARM4 in their inactive status (ARM1, ARM2 and ARM3 low, ARM4 high) to prevent that, in case of safing internal engine fault, the arming signal is set.

ARMx_Ly signals are used to link the ARMx signals to the deployment loop y through $6E LOOP_MATRIX_ARM1, $6F LOOP_MATRIX_ARM2, $70 LOOP_MATRIX_ARM3 and $71 LOOP_MATRIX_ARM4 registers (see the Table 7).

Table 7. DCR_x register

	(1)	(2)	19:16	15:12	11	10	9	8	7	6	5	4	3	2	1	0	
$6E LOOP_MATRIX_ARM1 $6F LOOP_MATRIX_ARM2 $70 LOOP_MATRIX_ARM3 $71 LOOP_MATRIX_ARM4	D	R	0	X	ARMx_LB	ARMx_LA	ARMx_L9	ARMx_L8	ARMx_L7	ARMx_L6	ARMx_L5	ARMx_L4	ARMx_L3	ARMx_L2	ARMx_L1	ARMx_L0	0 = ARMx not associated to loop y 1 = ARMx associated to loop y

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

3.1.2 SAFING and SCRAP states

Once fixed the deploy parameters, in order to satisfy a deploy request, the IC has to move in SAFING state or SCRAP state.

Both states are driven by specific SPI commands:

- SAFING state corresponds to the normal IC operation.
- SCRAP state corresponds to the operation at final disposal of the IC.

Once sent the command to move into SAFING or SCRAP state, the verification of the IC's status is readable into the $04 SYS_STATE register (see the Table 8).

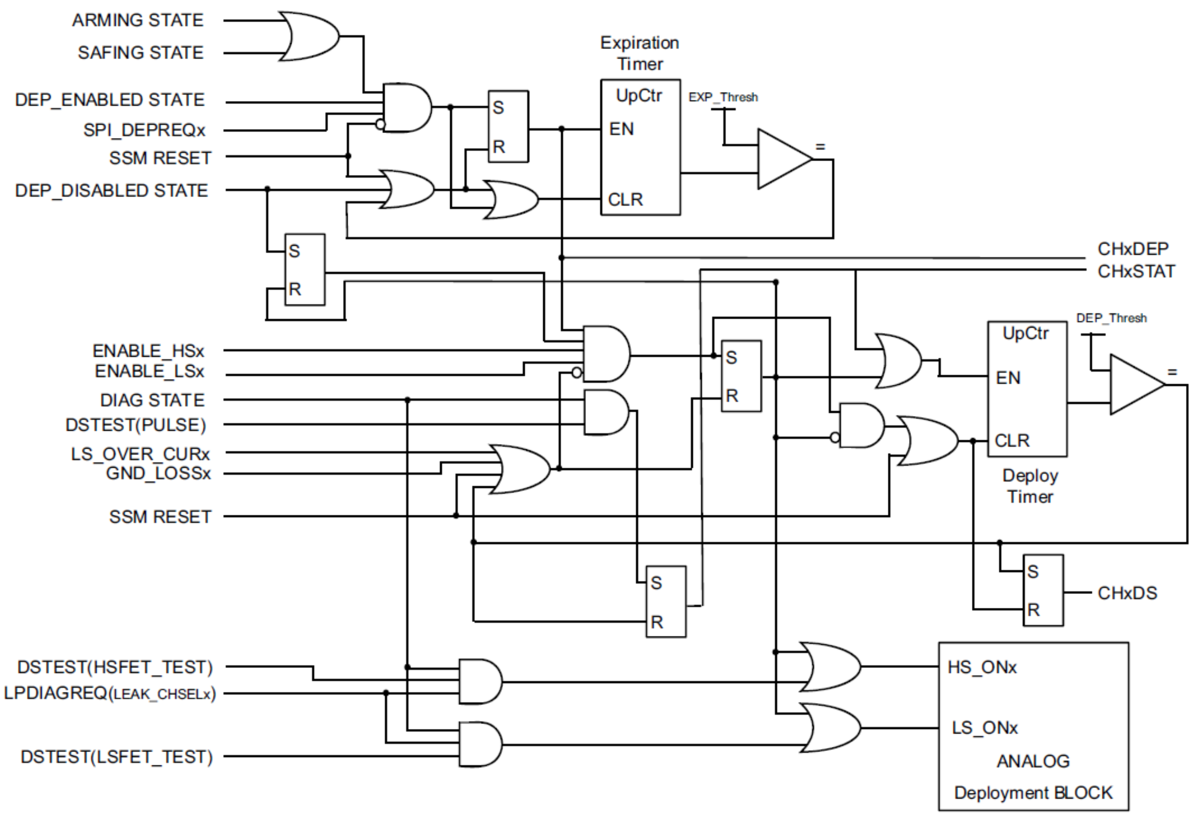
Table 8. **SPI commands to pass in SAFING state or SCRAP state**

	(1)	(2)	19:16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
$30 SCRAP STATE	D	W	-	0x3535																SCRAP state command
$31 SAFING STATE	D	W	-	0xACAC																SAFING state command
$04 SYS_STATE	-	R	-	0	-	-	-	-	OPER_CTL_STATE	-	-	-	-	-	-	-		POWER_CTL_STATE		10÷8: 010 = SAFING 011 = SCRAP 2÷0: 010 = RUN

1. I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING
2. R = READ, W = WRITE

3.1.3 Deployment driver

Figure 4. **Deployment driver control logic**



In order to be able to deploy, the arming signals have to be serviced, and their state is readable in the ARM_STATE register (see the Table 9).

Table 9. ARM_STATE register

	(1)	(2)	19:16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
$6A ARM_STATE	-	R	-	0						PSINHINT	PSIN_EXP_TIME	ACL_PIN_STATE	ACL_VALID	ARMINT_4	ARMINT_3	ARMINT_2	ARMINT_1	0	0	9: state of PSINHINT signal 8: state of PSINHINT expiration timer 7: echo of ACL pin 6: valid ACL detection 0 = cleared when ACL_BAD = 2 1 = set when ACL_GOOD = 3 5÷2: state of arming signals Result of safing engine in case of Internal Safing Engine Echo of ARMx pin in case of External Safing Engine

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The four ARMINT_x bits:
- Indicate the internal safing engine result if the internal safing machine has been selected.
- Are the echo of the four pins ARMx if the external safing engine has been selected.

Deployment has to be enabled via SPI, writing DEPEN_WR bits in SPIDEPEN register (see the Table 10).

Table 10. SPIDEPEN register

$25 SPIDEPEN	Config in SAFING and ARMING state
DEPEN_WR, bit[15:0]	0x0FF0 = LOCK enter deploy disable state 0xF00F = UNLOCK enter deploy enable state

Deployment command request has to be received by the IC via DEPCOM register (see the Table 11).

Table 11. DEPCOM register – CHxDEPREG bit

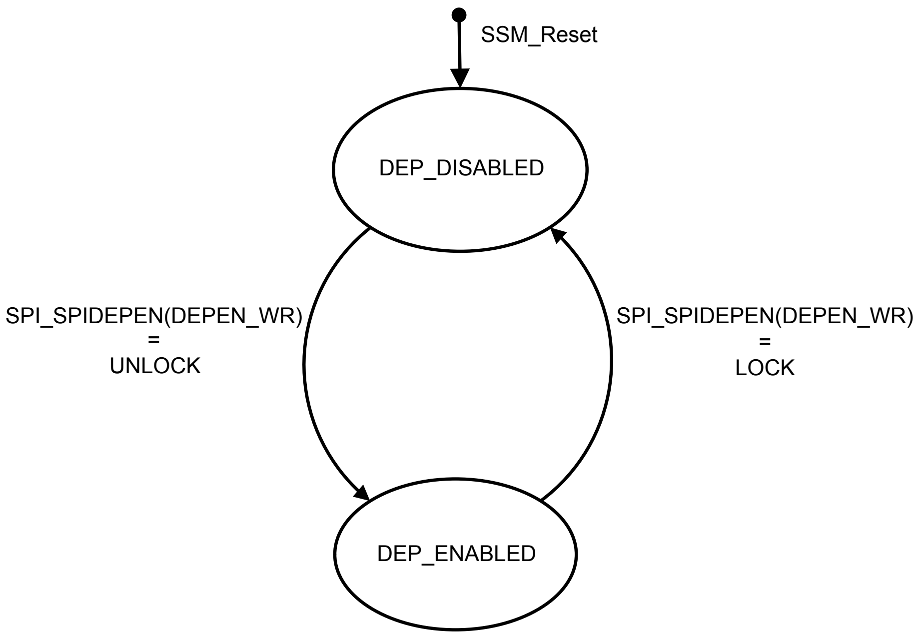
$12 DEPCOM	Config in SAFING and ARMING state
CHxDEPREG, bit[x]	0 = no change to deployment control channel x 1 = clear and start the expiration timer in ARMING, SAFING and DEP_ENABLED state

Once the deployment command has been received, the deploy time is elapsed, deploy success bit is set (CHxDSX bit) and deployment enable toggles into DEP DISABLED.

The next deploy requires the DEPEN reconfigured again as ENABLED. This feature has to be considered in case of multiple deployment, after each of them, before the next deployment the correspondent bit DEPEN has to be set again.

Deployment status of each channel is readable in the DSR_X registers (see the Table 3).

Figure 5. Deployment Enable/Disable



Once the deploy requirements are satisfied, the Expiration Time Counter starts.

This counter considers the feature of the IC to accept a deploy command even if the arming is not yet serviced. If the arm command occurs inside the expiration time, the deployment takes place otherwise the deployment command is discharged.

Dep_exp_time is defined in the DCR_x registers, together with the Deploy_timer and Dep_current.

Once the deployment is started, any DEP_EN = 0x0FF0 (i.e., deploy disable) is ignored. If the same command arrives before the deployment has been started, the deployment is really disabled and the deploy command ignored.

Each High Side (SFx) has a current comparator to indicate when the current flowing through is greater than the deployment current threshold (ITHDEPL = 90% IDEPLx). For each channel there is a timer (Current_Mon_Timer) that measures, with a 16 µs resolution, how long the current is at high level to let the microcontroller identify if the deployment has been effective or not (see the Table 12).

Table 12. DCMTSxy register

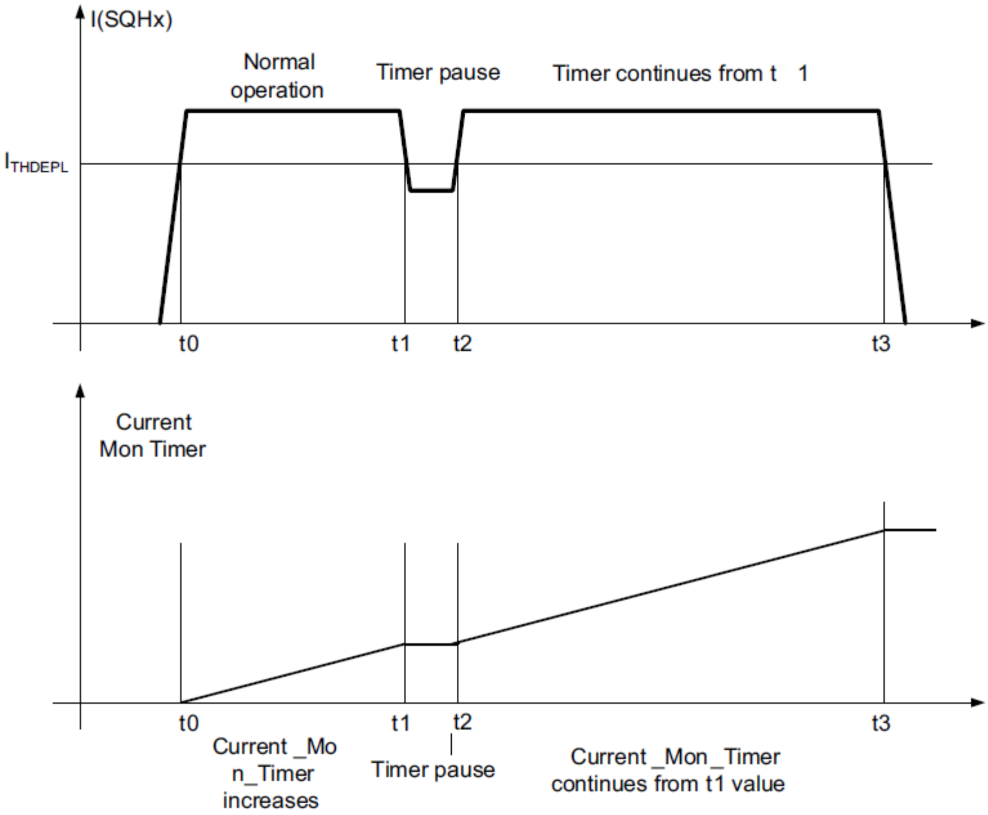
	(1)	(2)	19:16	15:8	7:0	
$1F DCMTS01 $20 DCMTS23 $21 DCMTS45 $22 DCMTS67 $23 DCMTS89 $24 DCMTSAB	-	-	R	Current_Mon_Timer_y[7:0]	Current_Mon_Timer_x[7:0]	x = 0, 2, 4, 6, 8, A y = 1, 3, 5, 7, 9, B 16 µs increment while Deploy_curr > monitor threshold channel per channel

1. I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING
2. R = READ, W = WRITE

During a deploy event, if the current falls momentarily below the threshold, the timer stops (timer pause), and continues to count as the current turns high (see the Figure 6).

Current_Mon_Timer is refreshed upon read or when a new DEPCOM command on the channel is received. For this reason, the microcontroller reads the data after the deployment event and before a new deployment command. The current measurement stops at the end of the deployment time.

Figure 6. Current measurement during deploy



Once the deployment is started, it can be interrupted by:

- Over-current in the Low Side.
- GND loss.
- SSM reset.
- End of deployment time.

The status of the deployment is reported in the DSR_x registers:

- CHxSTAT bit reports if the deployment is in progress or not.
- CHxDS bit reports if the deployment lasts for the programmed deploy time (deploy success).

The event is also reported in the GSW field (see the Table 13), DEPOK bit, that is the "OR" of the deployment success of all the twelve channels (see the Table 14).

Table 13. Global Status Word (GSW)

MISO bit	31	30	29	28	27	26	25	24	23	22	21
MISO	SPIFLT	DEPOK	RSFLT	WDTDIS_S	ERSTATE	POWERFLT	FLT	CONVRDY2	CONVRDY1	ERR_WID	ERR_RID
GSW bit	10	9	8	7	6	5	4	3	2	1	0

Table 14. DEPOK bit in GSW

GSW	MISO b[30] DEPOK = GSW b[9]

	0 = all DSR_x/CHxDS bits are equal to zero (no deployment success on all channels) 1 = at least a deployment successful on the channels

In case DEPOK = 1, this does not mean that the current is really passed through the squib for the programmed time. This bit means only that no inhibition of deployment has happened. The real evaluation is done through the channel current monitor time, i.e., DCMTS01÷DCMTSAB registers.

In case of a short to ground of the Low Side during the deployment, the current is limited by the High Side avoiding the device's damage. The same protection is available if an open load condition happens, followed by a short to ground of the Low Side.

3.2 Deployment driver protection

In order to avoid damaging the IC due to eventual free-wheeling, two protections are implemented:

- After a deployment, once the High Side is switched off, the Low Side is kept on for $t_{DEL\_SD\_LS}$ (50 µs min.) in order to allow fly-back.
- Once Low Side is switched off, a protection against the overvoltage through a clamp structure is implemented.

On the Low Side there is a current limitation and overcurrent protection circuit that attends limiting the current at I_{LIM_SR} (2.2 A ÷ 4 A) and I_{OC_SR} (2.2 A ÷ 4 A) respectively, avoiding, in case of pin short to battery, any damage. If the malfunction lasts over $t_{FLT\_ILIM\_LS}$ (100 µs typ), the whole channel (High and Low Side) is switched off until a new deployment command (via SPI_DEPEN register) occurs.

The squib driver can stand the short to ground of the pins during the deployment, because the High Side current is limited by the High Side itself.

It can also manage the case of SRx short to ground after an open circuit, because it is able to detect the open circuit condition and then limiting the current overshoot as the open circuit disappears.

In case of squib's intermittence during deployment phase, current limitation is ensured by the Low Side current limitation, I_{LIM_SR}. If the condition lasts longer than $t_{FLT\_OS\_LS}$ (20 µs max), the High Side is switched off for $t_{OFF\_OS\_HS}$ (4 µs ÷ 12 µs) and then on again.

This allows distinguish Open Load and Low Side short to battery cases and then properly manage them.

3.3 Deployment driver examples

Since the external safing engine is used (SAFESEL = 1), the ARM1 pin is connected to 5 V (high level) and the ARM4 pin is connected to ground (low level). All the deployment loops are associated to ARM1.

In low-cost applications the external Safing FET could be removed. In this case the application has a lower Safety level. To be sure not to damage the High Side MOSFETs it is suggested to set the ERBOOST and the ER cap charging voltage to 24 V.

3.3.1 With Watchdog Service routine disabled

The Table 15 reports a simple example showing the minimum SPI frames needed to configure the device and enable the deployment on all the channels when the Watchdog Service routine is disabled.

If the Watchdog function is useless, it can be disabled in two steps:

1. After power-up, pull the WDT pin to a voltage higher than 14 V ($V_{WD\_OVERRIDE\_th}$), for example as in the Figure 7.
2. Write the frame 0x3CC3 in the $35 WD Test Command register.

Figure 7. Watchdog override signal

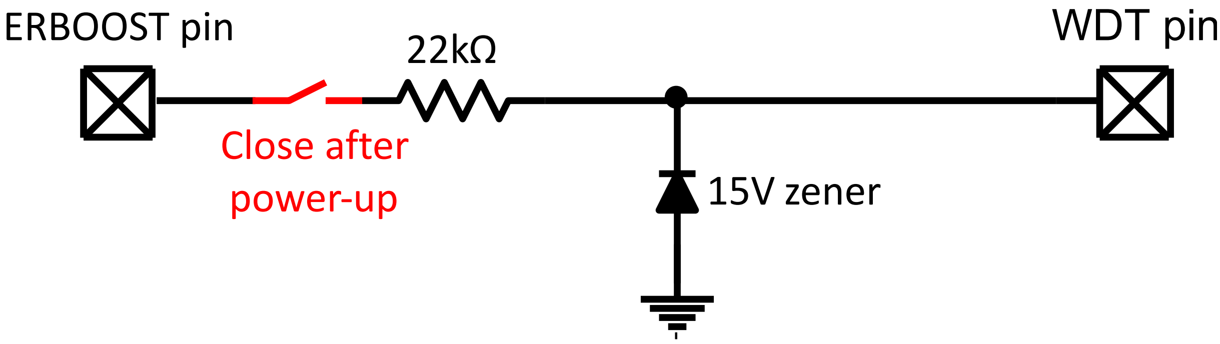


Table 15. Deployment SPI sequence without Watchdog routine

Register	State	R/W	Data	Notes
$01 SYS_CFG	Init	W	0x000D	Bit 15: 0 = Auto switch off disabled Bit 14: X = Don't care Bit 13: 0 = High OVC for SYNC Boost, SAT Buck and VCC Buck Bit 12: 0 = ER Boost is disabled in ER state Bit 11: 0 = Internal PSINH Bit 10: 0 = Short time Bit 9: 0 = Long sync pulses shift duration Bits 8-7: 00 = 8 sample DC-squib-temp measure Bits 6-5: 00 = 4 sample other measure Bit 4: 0 = Current mode for PSINH Bit 3: 1 = External safing engine Bit 2: 1 = VSF set to 25 V Bit 1: 0 = 1 µs filter time for VINGOOD Bit 0: 1 = Timeout disabled
$04 SYS_STATE	Init	R	-	Bits 10÷8: 000 = INIT Bits 2÷0: 010 = RUN
$35 WD_TEST	Init	W	0x3CC3	Non-latched WD Test Command
$04 SYS_STATE	Diag	R	-	Bits 10÷8: 001 = DIAG Bits 2÷0: 010 = RUN
$02 SYS_CTL	Diag	W	0x02E0	Bit 15: 0 = VIN comparator used to restart SYNC Boost in ER state Bit 14: 0 = 1 mA squib pull down current, 450 µA VRCM leakage to GND threshold Bit 13: 0 = SYNC Boost disabled in ER state Bit 12: 0 = VIN th set to 5.5 V Bit 11÷10: 00 = VBATMON th set to 6 V Bit 9: 1 = ER Boost set to 33 V Bit 8: X = Don't care Bit 7: 1 = ER Charge on Bit 6: 1 = ER Boost On Bit 5: 1 = SYNC Boost On Bit 4: 0 = No POWER OFF from SHUTDOWN Bit 3: X = Don't care

Register	State	R/W	Data	Notes
				Bit 2: 0 = Low current limit for ER switch Bit 1: 0 = Low voltage for SYNC Boost (12 V) Bit 0: 0 = Low voltage for SAT Buck (7.2 V)
$05 POWER STATE	Diag	R	-	Bit 19: 1 = WAKEUP > WU_on Bit 18: 0 = VBATMON > VBBAD Bit 17: 0 = VBATMON > VBGOOD Bit 16: 0 = VIN > VINBAD Bit 15: 0 = VIN > VINGOOD Bit 14: 0 = V_SYNCBOOST > SYNCBOOST_OK Bit 13: 0 = V_SATBUCK > SATBUCK_OK Bit 12: 0 = V_ERBOOST > ERBOOST_OK Bit 11: 0 = VCC > VCC_UV Bit 10: 0 = VCC < VCC_OV Bit 9: 0 = Don't care Bit 8: 1 = ER Boost on Bit 7: 1 = ER Charge on Bit 6: 0 = ER Low Current Discharge off Bit 5: 0 = ER High Current Discharge off Bit 4: 0 = ER Switch off Bit 3: 1 = SYNC Boost on Bit 2: 1 = SAT Buck on Bit 1: 1 = VCC on Bit 0: 0 = VSF off
$00 FLTSR	Diag	R	-	Verify there are not faults
$6E LOOP_MATRIX_ARM1	Diag	W	0x0FFF	Bits 15÷12: X = Don't care Bits 11÷0: 1 = ARM1 assigned to 0÷B loops
$06 DCR_0 ÷ $11 DCR_B	Diag	W	0x0250	Bits 15÷12: X = Don't care Bits 11÷6: 0x9 = 576 µs (9*64 µs step) Bits 5÷4: 01 = 1.75 A deploy current Bits 3÷2: 00 = 500 ms deploy expiration time Bits 1÷0: X = Don't care
$13 DSR_0 ÷ $1E DSR_B	Diag	R	-	Bit 15: 0 = deployment successful Bit 14: 0 = deployment not in progress Bits 13: 0 = correct time/current combination Bits 12: 0 = deployment configuration accepted Bits 5÷0: deployment expiration timer value
$31 SAFING_STATE	Diag	W	0xACAC	Frame to pass from DIAG to SAFING
$04 SYS_STATE	S	R	-	Bits 10÷8: 010 = SAFING Bits 2÷0: 010 = RUN
$25 SPIDEPEN	S, A	W	0x0FF0	Lock Code
$25 SPIDEPEN	S, A	W	0xF00F	Unlock Code
$12 DEPCOM	S, A	W	0x0FFF	Bits 11÷0: 0x0FFF = deploy requests for all channels
$25 SPIDEPEN	S, A	W	0x0FF0	Lock Code

Register	State	R/W	Data	Notes
$13 DSR_0 ÷ $1E DSR_B	S, A	R	-	Bit 15: 1 = deployment successful

3.3.2 With Watchdog Service routine enabled

The Table 16 reports a simple example showing the minimum SPI frames needed to configure the device and enable the deployment on all the channels when the Watchdog Service routine is enabled.

Table 16. Deployment SPI sequence with Watchdog routine

Register	State	R/W	Data	Notes
$01 SYS_CFG	Init	W	0x000D	Bit 15: 0 = Auto switch off disabled Bit 14: X = Don’t care Bit 13: 0 = High OVC for SYNC Boost, SAT Buck and VCC Buck Bit 12: 0 = ER Boost is disabled in ER state Bit 11: 0 = Internal PSINH Bit 10: 0 = Short time Bit 9: 0 = Long sync pulses shift duration Bits 8-7: 00 = 8 sample DC-squib-temp measure Bits 6-5: 00 = 4 sample other measure Bit 4: 0 = Current mode for PSINH Bit 3: 1 = External safing engine Bit 2: 1 = VSF set to 25 V Bit 1: 0 = 1 µs filter time for VINGOOD Bit 0: 1 = Timeout disabled
$04 SYS_STATE	Init	R	-	Bits 10÷8: 000 = INIT Bits 2÷0: 010 = RUN
$2A WDTCR	Init	W	0x3219	Bit 14: WD1_MODE = FAST Bits 13÷7: WDTMIN = 400 µs Bits 6÷0: WDT DELTA = 200 µs
$2C WD_STATE	Init	R	-	Bits 10÷8: WD1_STATE = INITIAL (000)
$2B WDIT	Init	W	-	Service watchdog following A/B/A…sequence
$04 SYS_STATE	Diag	R	-	Bits 10÷8: 001 = DIAG Bits 2÷0: 010 = RUN
$02 SYS_CTL	Diag	W	0x02E0	Bit 15: 0 = VIN comparator used to restart SYNC Boost in ER state Bit 14: 0 = 1 mA squib pull down current, 450 µA VRCM leakage to GND threshold Bit 13: 0 = SYNC Boost disabled in ER state Bit 12: 0 = VIN th set to 5.5 V Bit 11÷10: 00 = VBATMON th set to 6 V Bit 9: 1 = ER Boost set to 33 V Bit 8: X = Don’t care Bit 7: 1 = ER Charge on Bit 6: 1 = ER Boost On Bit 5: 1 = SYNC Boost On Bit 4: 0 = No POWER OFF from SHUTDOWN Bit 3: X = Don’t care Bit 2: 0 = Low current limit for ER switch Bit 1: 0 = Low voltage for SYNC Boost (12 V) Bit 0: 0 = Low voltage for SAT Buck (7.2 V)

Register	State	R/W	Data	Notes
$05 POWER STATE	Diag	R	-	Bit 19: 1 = WAKEUP > WU_on Bit 18: 0 = VBATMON > VBBAD Bit 17: 0 = VBATMON > VBGOOD Bit 16: 0 = VIN > VINBAD Bit 15: 0 = VIN > VINGOOD Bit 14: 0 = V_SYNCBOOST > SYNCBOOST_OK Bit 13: 0 = V_SATBUCK > SATBUCK_OK Bit 12: 0 = V_ERBOOST > ERBOOST_OK Bit 11: 0 = VCC > VCC_UV Bit 10: 0 = VCC < VCC_OV Bit 9: 0 = Don't care Bit 8: 1 = ER Boost on Bit 7: 1 = ER Charge on Bit 6: 0 = ER Low Current Discharge off Bit 5: 0 = ER High Current Discharge off Bit 4: 0 = ER Switch off Bit 3: 1 = SYNC Boost on Bit 2: 1 = SAT Buck on Bit 1: 1 = VCC on Bit 0: 0 = VSF off
$00 FLTSR	Diag	R	-	Verify there are not faults
$6E LOOP_MATRIX_ARM1	Diag	W	0x0FFF	Bits 15÷4: X = Don't care Bits 11÷0: 1 = ARM1 assigned to 0÷B loops
$06 DCR_0 ÷ $11 DCR_B	Diag	W	0x0250	Bits 15÷12: X = Don't care Bits 11÷6: 0x9 = 576 µs (9*64 µs step) Bits 5÷4: 01 = 1.75 A deploy current Bits 3÷2: 00 = 500 ms deploy expiration time Bits 1÷0: X = Don't care
$13 DSR_0 ÷ $1E DSR_B	Diag	R	-	Bit 15: 0 = deployment successful Bit 14: 0 = deployment not in progress Bits 13: 0 = correct time/current combination Bits 12: 0 = deployment configuration accepted Bits 5÷0: deployment expiration timer value
$31 SAFING_STATE	Diag	W	0xACAC	Frame to pass from DIAG to SAFING
$04 SYS_STATE	S	R	-	Bits 10÷8: 010 = SAFING Bits 2÷0: 010 = RUN
$25 SPIDEPEN	S, A	W	0x0FF0	Lock Code
$25 SPIDEPEN	S, A	W	0xF00F	Unlock Code
$12 DEPCOM	S, A	W	0x0FFF	Bits 11÷0: 0x0FFF = deploy requests for all channels
$25 SPIDEPEN	S, A	W	0x0FF0	Lock Code
$13 DSR_0 ÷ $1E DSR_B	S, A	R	-	Bit 15: 1 = deployment successful

3.3.3 Deployment waveforms

The Figure 8 and Figure 9 report some examples where a high current pyrofuse has been used and four channels have been put in parallel in order to achieve target current values for deployment to occur.

Referring to the Figure 1, the system has been setup with two different scenarios:

- With Safing FET, VER set to 33 V and VSF set to 25 V.
- Without Safing FET and VER set to 24 V.

The signals are the following:

- Blue = SRx
- Light blue = SFx
- Magenta = VER
- Green = Load current

Figure 8. Deployment waveforms, VER = 33 V

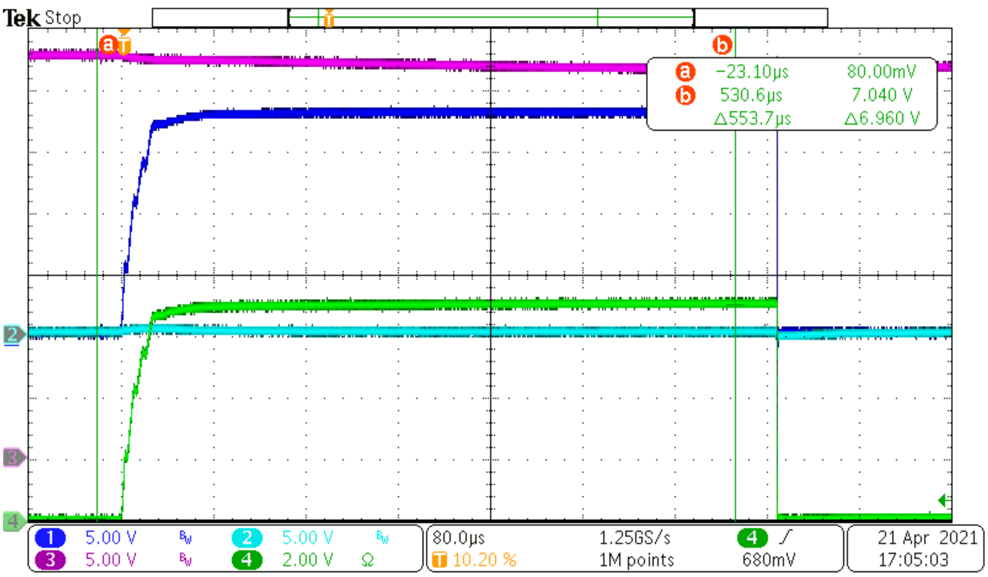
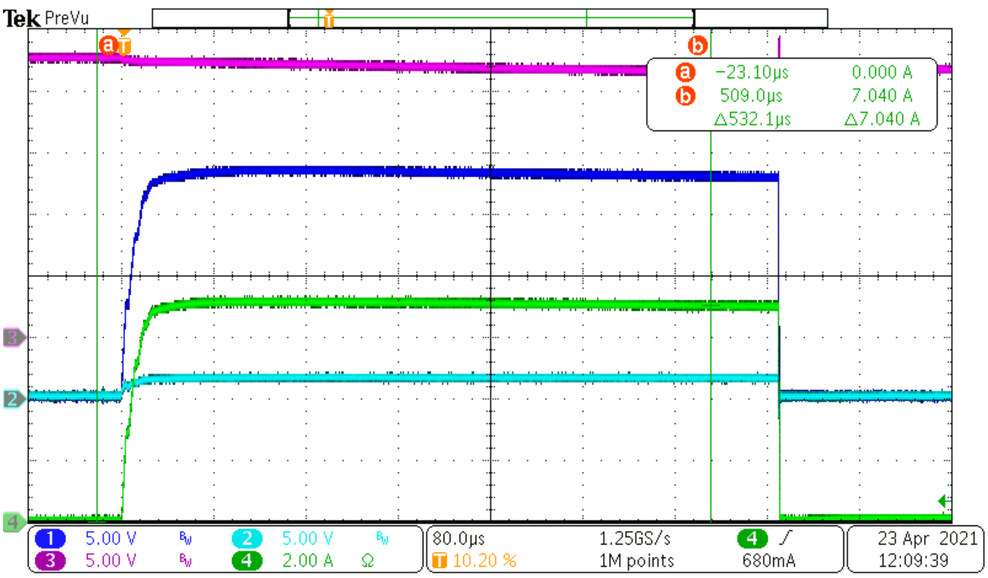


Figure 9. Deployment waveforms, VER = 24 V



3.4 Arming command after deployment command

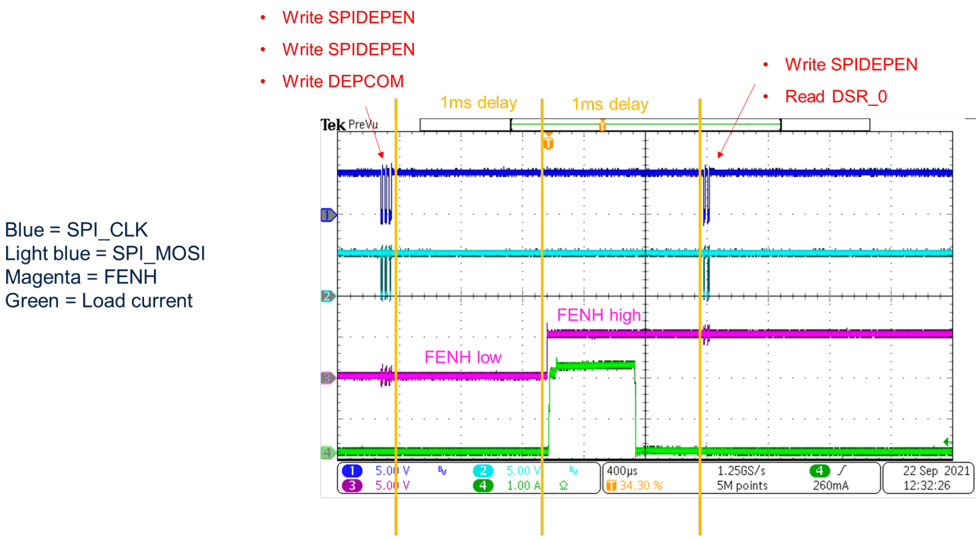
It is also possible to have a deployment event in a way different from the usual, i.e., first sending the SPI deploy command, then asserting the arming signal.

An example (watchdog disabled, deployment on Channel 0) is shown in the Table 17 and the Figure 10.

Table 17. Deploy event with Arming command after SPI deployment command

Register read	Register written	SPI frame (hex)
Configuration		
SYS_STATE	SYS_CFG	0x0413000D
SYS_CFG	/	0x01000000
SYS_STATE	/	0x04000000
SYS_STATE	WD1_TEST	0x046A3CC3
SYS_STATE	/	0x04000000
POWER_STATE	SYS_CTL	0x050402E0
FLTSR	/	0x00010000
LOOP_MATRIX_ARM1	LOOP_MATRIX_ARM1	0x6EDC0001
DCR_0	DCR_0	0x061D0250
SYS_STATE	SAFING_STATE	0x0463ACAC
SYS_STATE	/	0x04000000
Deployment commands		
SPIDEPEN	SPIDEPEN	0x254B0FF0
SPIDEPEN	SPIDEPEN	0x254BF00F
DEPCOM	DEPCOM	0x12240001
1 ms delay - FENH high - 1 ms delay		
SPIDEPEN	SPIDEPEN	0x254B0FF0
DSR_0	/	0x13000000

Figure 10. Deploy event with Arming command after SPI deployment command



4 Diagnostic

For all the channels the following diagnostics are implemented (elaborated by a 10-bit ADC converter):

- High voltage leak test, for SFx and SRx oxide isolation
- VRCM test
- Leakage to battery/ground for SFx and SRx with/ without squib
- Loop to loop short diagnostic
- Squib resistance measurement - leakage cancellation
- High squib resistance, 500 Ω ÷ 2000 Ω
- SSxy, SFx,and VER voltage monitor
- Low side FET diagnostic
- High Side FET diagnostic
- Loss of ground
- High Side Safing FET diagnostic
- Deployment timer diagnostic

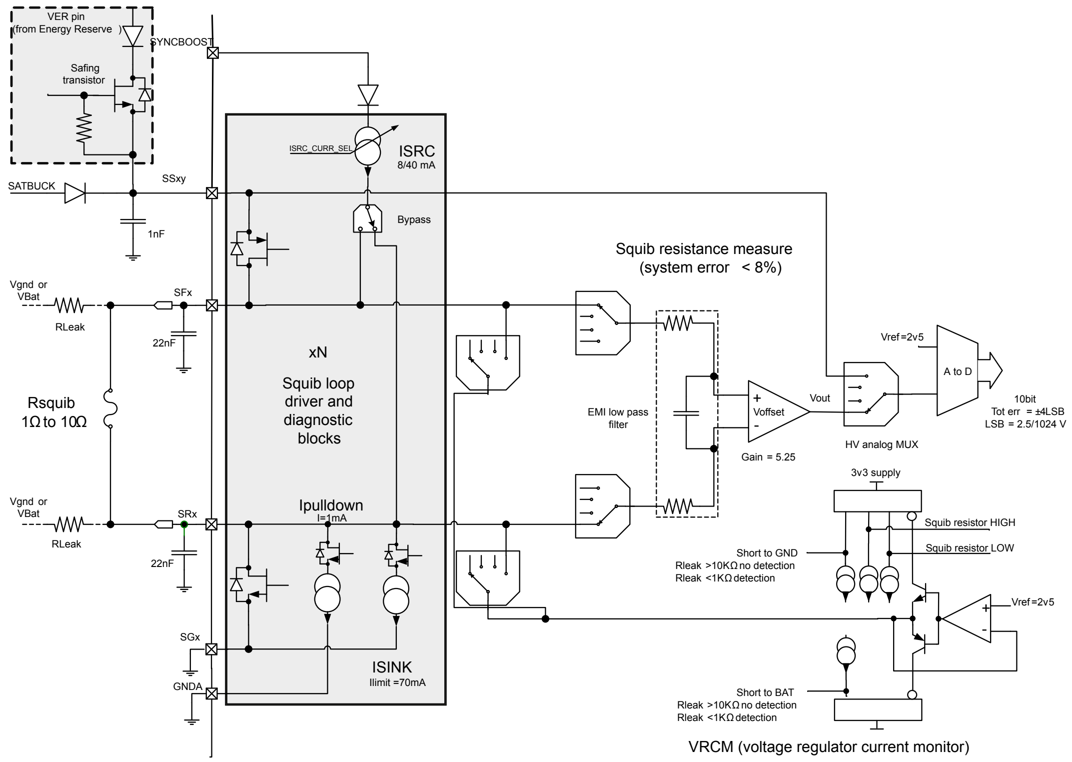
Diagnostic can be done in two ways, set in the LPDIAGREQ register via SPI:

- **High level (DIAG_LEVEL = 1)**: the set-up for each requested measurement is managed by the device itself.
- **Low level (DIAG_LEVEL = 0)**: the set-up for each requested measurement is managed by an external logic, step by step.

The relevant blocks used for the diagnostic are reported in the Figure 11.

In particular there are a Voltage Regulator Current Monitor (VRCM) and three current generators that withstand diagnostic operations, ISRC (40 mA), ISINK (limit 70 mA) and Ipulldown (1 mA).

Figure 11. Squib diagnostic blocks



4.1 Low level diagnostic

For a low level diagnostic, these steps shall be followed (see the Table 18):

1. ER charge has to be previously turned ON before running the diagnostic.
2. Verify that the IC is in DIAG state reading register $04.
3. Decide, writing the appropriate bit in reg. $38, which diagnostic mode is used.

Table 18. Low level diagnostic

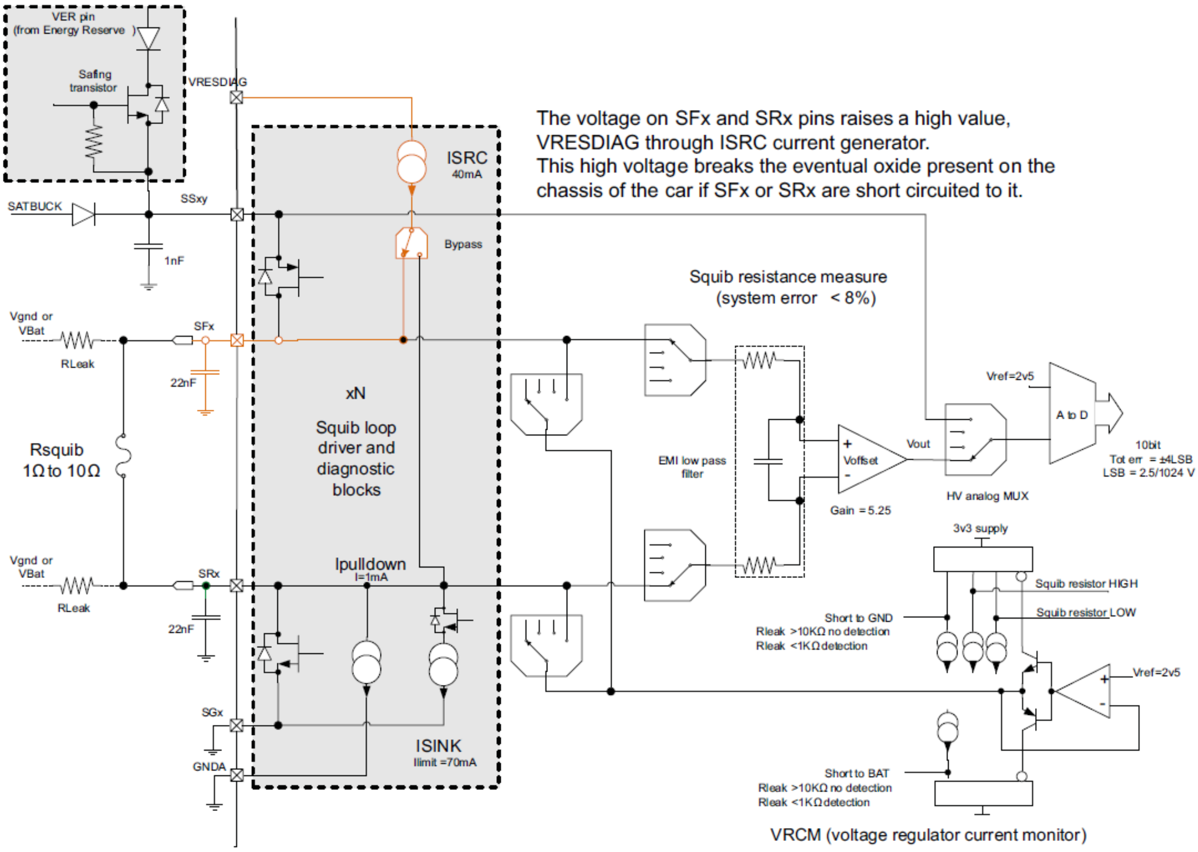
	(1)	(2)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
$02 SYS_CTL	(I)	W	0	0	0	0/1	00 01 10 11		0/1	01		1	0	0	X	X	X	X	15: RESTART_SYSBST_SEL (0 = VIN comp used, 1 = SYNCBST comp used) 14: PD&VRCM_SEL (0 = 1 mA pull-down and 450 µA VRCM leakage to GND, 1 = 5 mA pull-down and 2 mA VRCM leakage to GND) 13: KEEP_SYNCBST_ON (0 = SYNC Boost disabled in ER state, 1 = SYNC Boost active in ER state) 12: VIN_TH_SEL (0 = 5.25 V as VIN threshold, 1 = 6.3 V as VIN threshold) 11, 10: VBATMON_TH_SEL (00/11 = 5.75 V, 01 = 6.7 V, 10 = 7.75 V) 9: ER_BST_V (0 = 23 V, 1 = 33 V) 8, 7: ER_CUR_EN (00/11 = OFF, 01 = ER charge enabled, 10 = ER discharge enabled) 6: ER_BST_EN (0 = OFF, 1 = ON) 5: VSUP_EN (0 = OFF, 1 = ON) 4: SPI_OFF (0 = no effect, 1 = power off required) 3: ERSWITCH_LIM_SEL (0 = low current limit) 2: SYBST_V (0 = SYNC Boost set at 12 V, 1 = SYNC Boost set at 14.75 V) 1: SAT_V (0 = SAT Buck set at 7.2 V, 1 = SAT Buck set at 9 V)
$04 SYS_STATE		R						0	0	1						0	1	0	10, 9, 8: 001 = DIAG 2, 1, 0: 010 = RUN
$38 LPDIAGREQ	(I)	W	0	14÷0: Define the test															15: 0 = low level diag setup
$37 LPDIAGSTAT		R	0	14÷0: Define the test															15: 0 = low level diag
$3X DIAGCTRL_X X = A, B, C, D		W		X	X	X	X	X	X			6÷0: ADC address							
(3) 19 18 17 16 1			16÷0: ADC address						9÷0: ADC result										19: 1 = conversion finished

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

In low level mode, the IC performs the measurement following external requests. Each test set-up is driven, step by step, by the microcontroller, as the timing for the measurement.

4.1.1 High voltage leak test, oxide isolation IC-car chassis

Figure 12. High voltage leak test, oxide isolation IC-car chassis



This test is mandatory and verifies that no leakages are present on the SFx or SRx pins when high voltage is applied. ISRC current generator is ON and addressed on SFx (see the Table 19).

If there is no leakage, SFx rises up to SYNCBOOST and, being the impedance between SFx and SRx very low (squib connected), SRx follows SFx (see Figure 12).

Confirmation of this is done through an ADC measurement request of the SFx voltage value.

Table 19. High voltage leak test, oxide isolation IC-car chassis - LPDIAGREQ register

	[1]	[2]	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	1	01	0	00	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 1 = pull-down current off for all channels 12, 11: 01 = ISRC for RES_MEAS_CHSEL, off for the other channels 10: 0 = ISINK off for all channels 9, 8: 00 = VRCM not connected

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

SFx voltages and SYNCBOOST are readable by the microcontroller through the ADC converter in the registers $3X DIAGCTRL_X, with X = A, B, C, D (see the Table 20).

Table 20. High voltage leak test, oxide isolation IC-car chassis - DIAGCTRL_X registers

<table>
<tr><td colspan="5"></td><td>(1)</td><td>(2)</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6:0</td><td></td></tr>
<tr><td colspan="5">$3X DIAGCTRL_X
X = A, B, C, D</td><td>-</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>ADCREQ_X
$25 = SYNCBOOST
$46 = SF0
$47 = SF1
$48 = SF2
$49 = SF3
$4A = SF4
$4B = SF5
$4C = SF6
$4D = SF7
$4E = SF8
$4F = SF9
$50 = SFA
$51 = SFB</td><td rowspan="3">19: 1 = conversion finished</td></tr>
<tr><td>(3)</td><td>19</td><td>18</td><td>17</td><td>16</td><td colspan="12"></td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td><td>ADCREQ_X</td><td>-</td><td>R</td><td colspan="6">ADCREQ_X
$25 = SYNCBOOST
$46 = SF0
$47 = SF1
$48 = SF2
$49 = SF3
$4A = SF4
$4B = SF5
$4C = SF6
$4D = SF7
$4E = SF8
$4F = SF9
$50 = SFA
$51 = SFB</td><td colspan="4">ADCREQ_X 10 bit ADC result</td></tr>
</table>

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Once read the ADC measurement, to obtain the voltage value it is necessary to consider the divider ratio of the ADC. In case of SFx it is 15:1, in case of SYNCBOOST it is 10:1.

As an example, consider the case where the SYNCBOOST conversion has been requested and the readout of the ADC register is done. The voltage measured on SYNCBOOST pin is 12 V.

ADC = 0b0111101100 = 0x1EC = 492

In order to obtain the result in Volt, being the ADC characteristic linear:

$$2.5\,V : 1024 = x : ADC \rightarrow x = \frac{492 * 2.5\,V}{1024} = 1.2\,V \qquad (1)$$

Considering the divider ratio (DR), the result is:

$$SYNCBOOST = x * DR = 1.2\,V * 10 = 12\,V \quad (2)$$

Test result

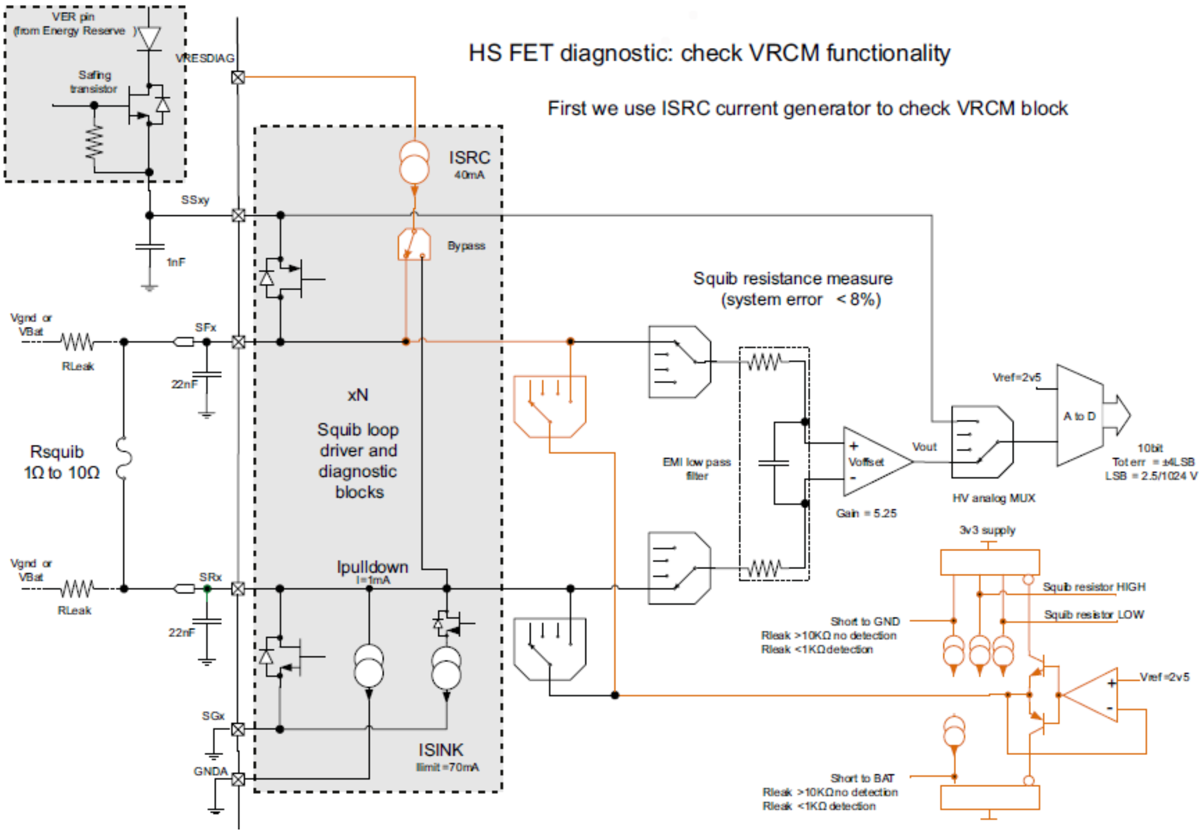
In case of leakage on High Side (SFx) or Low Side (SRx), SFx voltage is not able to reach SYNCBOOST and the microcontroller can detect the leakage problem, both on the High Side or on the Low Side, with no possibility, at this stage, to distinguish which of them is involved in the problem.

4.1.2 VRCM test validation

Before using VRCM block, used in many IC diagnostics, it is necessary a test for its validation. The test is done through short to battery and short to ground flag verification. Measurement set-up is composed by 2 steps, with SYNCBOOST supplied.

4.1.2.1 VRCM test - First step

Figure 13. VRCM test validation - First step



The first step (see the Figure 13) is verified through the LPDIAGREQ register (see the Table 21).

Table 21. VRCM test validation (first step) - LPDIAGREQ register

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	1	01	0	01	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 1 = pull-down current off for all channels 12, 11: 01 = ISRC for RES_MEAS_CHSEL, off for the other channels 10: 0 = ISINK off for all channels 9, 8: 01 = VRCM connected to SFx (LEAK_CHSEL channel)

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

RES_MEAS_CHSEL, bit[7:4] and LEAK_CHSEL, bit[3:0] must refer to the same channel.

Test 1 result

Being ISRC and VRCM connected to SFx, if VRCM works correctly, short to battery, readable in the LPDIAGSTAT register, is asserted for the channel selected (see the Table 22).

Table 22. VRCM test validation (first step) - LPDIAGSTAT register

<table>
<tr><th colspan="5"></th><th>(1)</th><th>(2)</th><th>15:12</th><th>11:8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3:0</th><th></th></tr>
<tr><td colspan="5">$37 LPDIAGSTAT</td><td rowspan="3"></td><td>R</td><td rowspan="3"></td><td rowspan="3">RES_MEAS_CHSEL
0000 = ch0
0001 = ch1
0010 = ch2
0011 = ch3
0100 = ch4
0101 = ch5
0110 = ch6
0111 = ch7
1000 = ch8
1001 = ch9
1010 = chA
1011 = chB
1100÷1111 = none</td><td rowspan="3">0</td><td rowspan="3">0</td><td rowspan="3">1</td><td rowspan="3">1</td><td rowspan="3">LEAK_CHSEL
0000 = ch0
0001 = ch1
0010 = ch2
0011 = ch3
0100 = ch4
0101 = ch5
0110 = ch6
0111 = ch7
1000 = ch8
1001 = ch9
1010 = chA
1011 = chB
1100÷1111 = none</td><td rowspan="3">19: 0 = low level diagnostic
7: 0 = no short between loops
6: 0 = STG not detected
5: 1 = STB detected
4: 1 = test on SFx</td></tr>
<tr><td>(3)</td><td>19</td><td>18</td><td>17</td><td>16</td><td>R</td></tr>
<tr><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td></td></tr>
</table>

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

4.1.2.2 VRCM test - Second step

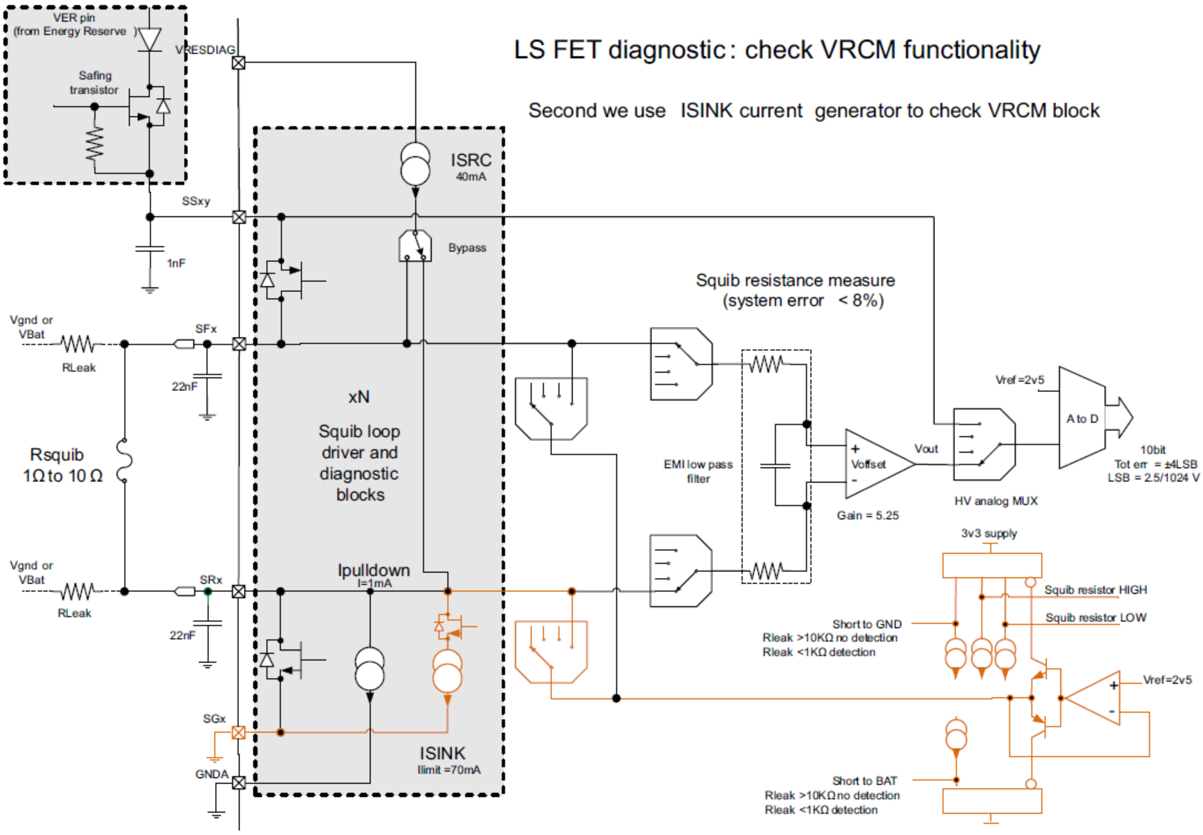


Figure 14. **VRCM test validation - Second step**

Once the first step of VRCM test is passed, it is possible to proceed with the second step (see the Figure 14), always through the LPDIAGREQ register (see the Table 23).

Table 23. VRCM test validation (second step) - LPDIAGREQ register

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	1	00	1	10	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 1 = pull-down current off for all channels 12, 11: 00 = ISRC off for all channels 10: 1 = ISINK on for RES_MEAS_CHSEL channel, off for the others 9, 8: 10 = VRCM connected to SRx (LEAK_CHSEL channel)

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

RES_MEAS_CHSEL, bit[7:4] and LEAK_CHSEL, bit[3:0] must refer to the same channel.

Test 2 result

Being ISNK and VRCM connected to SRx, if VRCM works correctly, short to ground, readable in the LPDIAGSTAT register, is asserted for the channel selected (see the Table 24).

Table 24. VRCM test validation (second step) - LPDIAGSTAT register

					(1)	(2)	15:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R		RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	0	1	0	0	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 0 = low level diagnostic 7: 0 = no short between loops 6: 1 = STG detected 5: 0 = STB not detected 4: 0 = test on SRx
(3)	19	18	17	16		R								
	0	0	0	0										

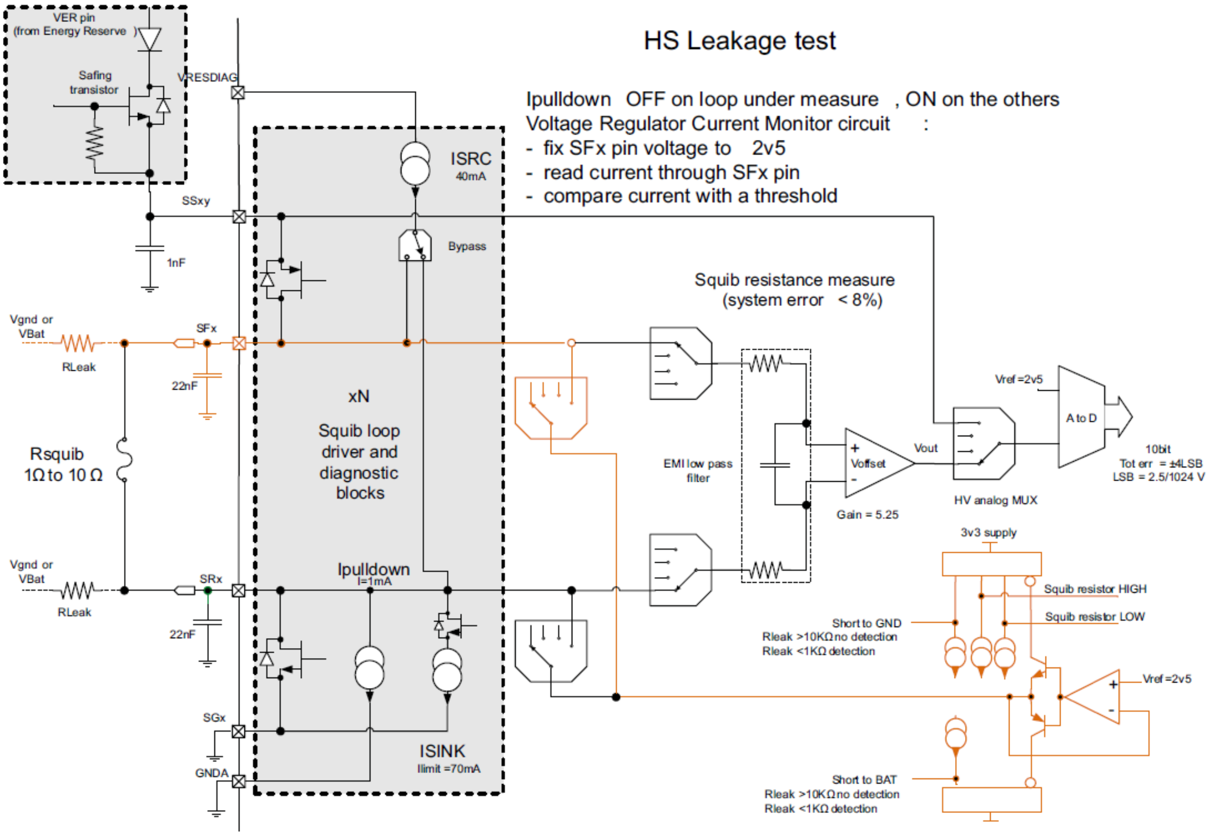
1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Final result

If the second step of the VRCM test is passed too, the VRCM test is validated.

4.1.3 Leakage test - High Side

Figure 15. **Leakage test - High Side**



ISRC and ISINK are kept off and VRCM is connected to SFx (see the Figure 15), chosen through the LEAK_CHSEL bits in the LPDIAGREQ register (see the Table 25).

Table 25. Leakage test, High Side - LPDIAGREQ register

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	0	00	0	01	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 0 = pull-down current off for VRCM channel, on for the others 12, 11: 00 = ISRC off for all channels 10: 0 = ISINK off for all channels 9, 8: 01 = VRCM connected to SFx (LEAK_CHSEL channel)

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Test result

If there is no leakage on the High Side, SFx voltage is equal to VREF = 2.5 V and no current is detected by VRCM itself. SFx voltage is readable addressing the ADC read out on it. The registers involved in this operation are the four DIAGCTRL_X (see the Table 26).

Table 26. **Leakage test, High Side - DIAGCTRL_X register**

<table>
<tr><td colspan="5"></td><td>(1)</td><td>(2)</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td></td></tr>
<tr><td colspan="5">$3X DIAGCTRL_X
X = A, B, C, D</td><td>-</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="7">ADCREQ_X
$46 = SF0
$47 = SF1
$48 = SF2
$49 = SF3
$4A = SF4
$4B = SF5
$4C = SF6
$4D = SF7
$4E = SF8
$4F = SF9
$50 = SFA
$51 = SFB</td><td></td></tr>
<tr><td>(3)</td><td>19</td><td>18</td><td>17</td><td>16</td><td rowspan="2">-</td><td rowspan="2">R</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td rowspan="2">19: 1 = conversion finished</td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td><td>ADCREQ_X</td><td colspan="6">ADCREQ_X
$46 = SF0
$47 = SF1
$48 = SF2
$49 = SF3
$4A = SF4
$4B = SF5
$4C = SF6
$4D = SF7
$4E = SF8
$4F = SF9
$50 = SFA
$51 = SFB</td><td colspan="10">ADCREQ_X 10 bit ADC result</td></tr>
</table>

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Once read the ADC measurement, to obtain the voltage value it is necessary to consider the divider ratio of the ADC, that is 15:1 in case of SFx and SYNCBOOST.

In case of a leakage (to ground or to battery), VRCM will sink or source a current to maintain SFx at VREF. As a consequence, STG or STB is set in the LPDIAGSTAT register (see the Table 27).

Table 27. Leakage test, High Side - LPDIAGSTAT register

					(1)	(2)	15:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R		RES_MEAS_CHSEL					LEAK_CHSEL	
(3)	19	18	17	16		R								
	0	0	0	0				0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	0	0/1	0/1	1	0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 0 = low level diagnostic 7: 0 = no short between loops 6: 1 = STG if leak vs GND 5: 1 = STB if leak vs BATT 4: 1 = test on SFx

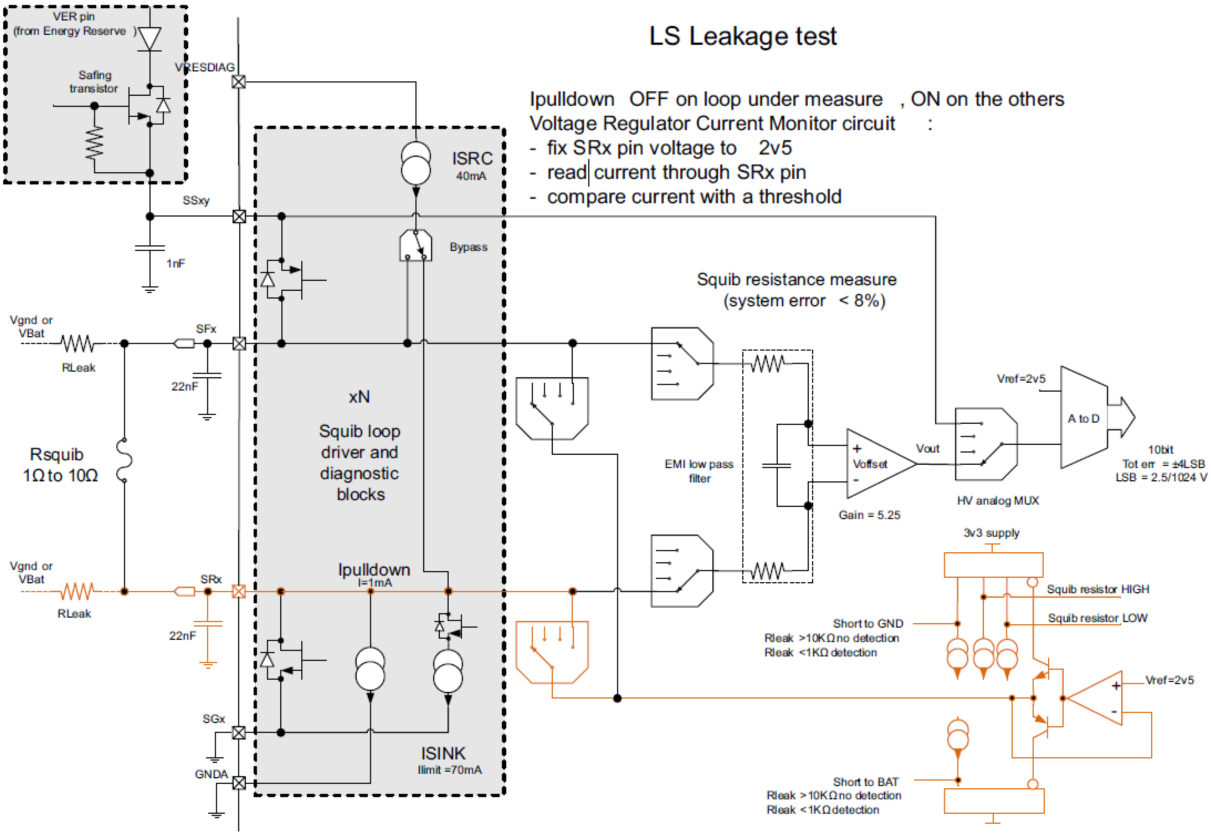
1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Pull-down current (1 mA) is active on all channels except the one under analysis. So, the STG requires further investigation to understand if it comes from a real short to ground of the channel itself or it comes from a short between the channel itself and another one.

Note: *In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all channels.*

4.1.4 Leakage test - Low Side

Figure 16. **Leakage test - Low Side**



ISRC and ISINK are kept off and VRCM is connected to SRx (see the Figure 16), through the LEAK_CHSEL bits in the LPDIAGREQ register (see the Table 28).

Table 28. **Leakage test, Low Side - LPDIAGREQ register**

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	0	00	0	10	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 0 = pull-down current off for VRCM channel, on for the others 12, 11: 00 = ISRC off for all channels 10: 0 = ISINK off for all channels 9, 8: 10 = VRCM connected to SRx (LEAK_CHSEL channel)

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Test result

If there is no leakage on the High Side, SRx voltage is equal to VREF = 2.5 V and no current is detected by VRCM itself.

Only if the squib is connected, SFx and SRx pins are at the same voltage, so SRx voltage is readable indirectly through SFx voltage, as done in case of High Side leakage test.

SFx voltage is readable addressing the ADC read out on it. The registers involved in this operation are the four DIAGCTRL_X (see the Table 29).

Table 29. Leakage test, Low Side - DIAGCTRL_X register

<table>
<tr><td colspan="5"></td><td>(1)</td><td>(2)</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td></td></tr>
<tr><td colspan="5">$3X DIAGCTRL_X
X = A, B, C, D</td><td>-</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="7">ADCREQ_X
$46 = SF0
$47 = SF1
$48 = SF2
$49 = SF3
$4A = SF4
$4B = SF5
$4C = SF6
$4D = SF7
$4E = SF8
$4F = SF9
$50 = SFA
$51 = SFB</td><td></td></tr>
<tr><td>(3)</td><td>19</td><td>18</td><td>17</td><td>16</td><td rowspan="2">-</td><td rowspan="2">R</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td rowspan="2">19: 1 = conversion finished</td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td><td>ADCREQ_X</td><td colspan="6">ADCREQ_X
$46 = SF0
$47 = SF1
$48 = SF2
$49 = SF3
$4A = SF4
$4B = SF5
$4C = SF6
$4D = SF7
$4E = SF8
$4F = SF9
$50 = SFA
$51 = SFB</td><td colspan="10">ADCREQ_X 10 bit ADC result</td></tr>
</table>

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Once read the ADC measurement, to obtain the voltage value it is necessary to consider the divider ratio of the ADC, that is 15:1 in case of SFx and SYNCBOOST.

If the squib between SFx and SRx pins is not connected, SRx voltage read out is not possible, as it is not mapped into the ADC request command.

In case of a leakage (to ground or to battery), VRCM will sink or source a current to maintain SFx at VREF. Therefore, STG or STB is set in the LPDIAGSTAT register (see the Table 30).

Table 30. Leakage test, Low Side - LPDIAGSTAT register

	(1)	(2)	15:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT		R		RES_MEAS_CHSEL					LEAK_CHSEL	
(3) 19 / 18 / 17 / 16		R		0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	X	0/1	0/1	0	0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 0 = LOW LEVEL 6: 1 = STB if leak vs GND 5: 1 = STB if leak vs BATT 4: 0 = test on SRx
0 / 0 / 0 / 0										

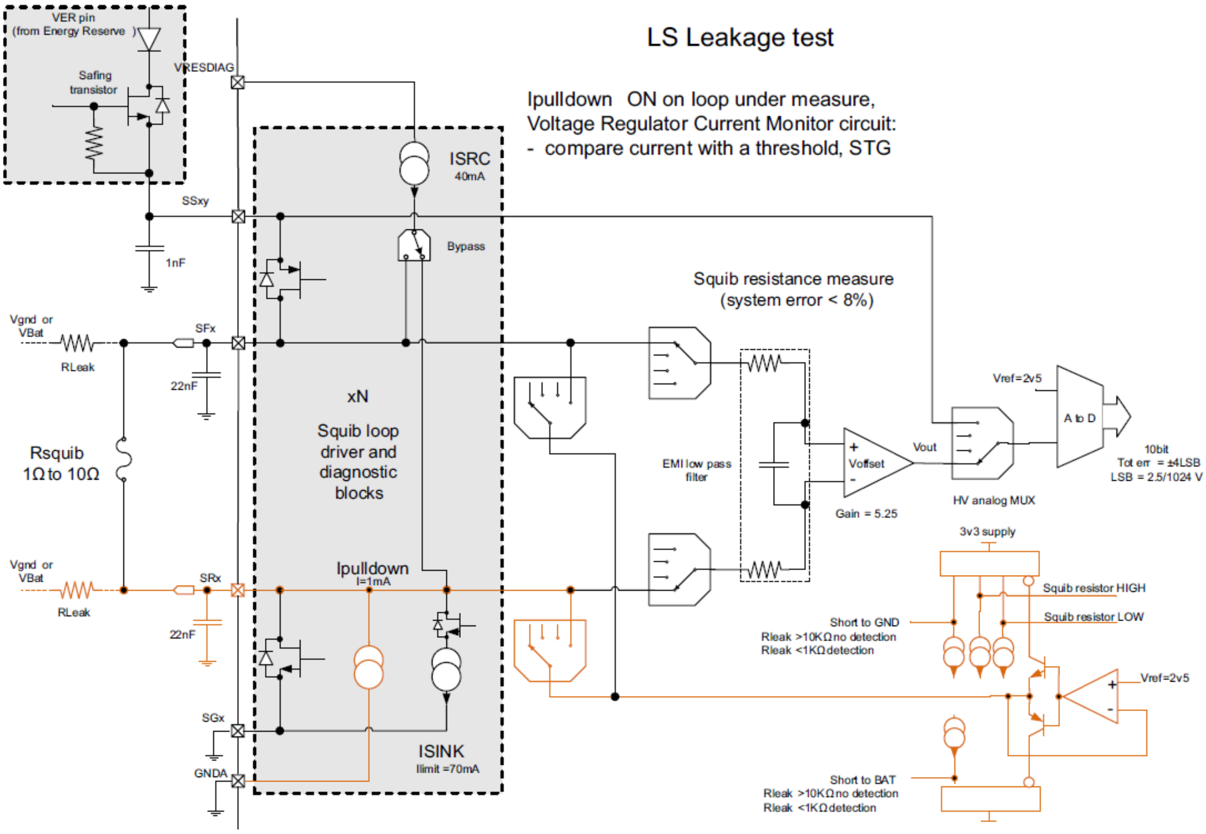
1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Pull-down current (1 mA) is active on all channels except the one under analysis. So, in case of STG detection, further investigation is necessary to understand if it comes from a real short to ground of the channel or from a short of the channel with another one.

Note: *In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all channels.*

4.1.5 Leakage test - Low Side pulldown current

Figure 17. Low Side pulldown current - Leakage test



After having verified that no HS/LS leakage is present, it is possible to verify if IPD is correctly working. VRCM is connected to SRx (see the Figure 17) through the LEAK_CHSEL bits in the LPDIAGREQ register and IPD is switched on for that channel (see the Table 31).

Table 31. **Leakage test, Low Side pulldown current - LPDIAGREQ register**

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	0	00	0	11	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 0 = pull-down current off for VRCM channel, on for the others 12, 11: 00 = ISRC off for all channels 10: 0 = ISINK off for all channels 9, 8: 11 = VRCM connected to SRx (LEAK_CHSEL channel) with pull-down current enabled

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Test result

If IPD is working, SRx voltage is equal to VOUT_VRCM and VRCM shows STG (see the Table 32).
If, in this condition, STG is not set, it means that there is something not correctly working in IPD.

Table 32. **Leakage test, Low Side pulldown current - LPDIAGSTAT register**

					(1)	(2)	15:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R		RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	0	1	0	0	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 0 = low level diagnostic 7: 0 = no short between loops 6: 1 = STG detected 5: 0 = STB not detected 4: 0 = test on SRx
(3)	19	18	17	16		R								
	0	0	0	0										

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Note: In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all channels.

4.1.6 Short between loops

Supposing the external load is connected, a short to ground flag of SRx or SFx can be read as:

- Short of the pin with SR or SF of another channel, both SR and SF
- Real short of the pin SRx or SFx to GND

Note: In Pyro Fuse Application with channels shorted together, the short to ground should be a real short of SRx or SFx pin to GND. Moreover, a short to ground on a channel will be present on all the others.

In this test the pulldown current generators are switched off for all channels. If the STG is still present, it means a real STG of the channel under test.

The correspondent set up is done by setting the $38 LPDIAGREQ properly (see the Table 33):

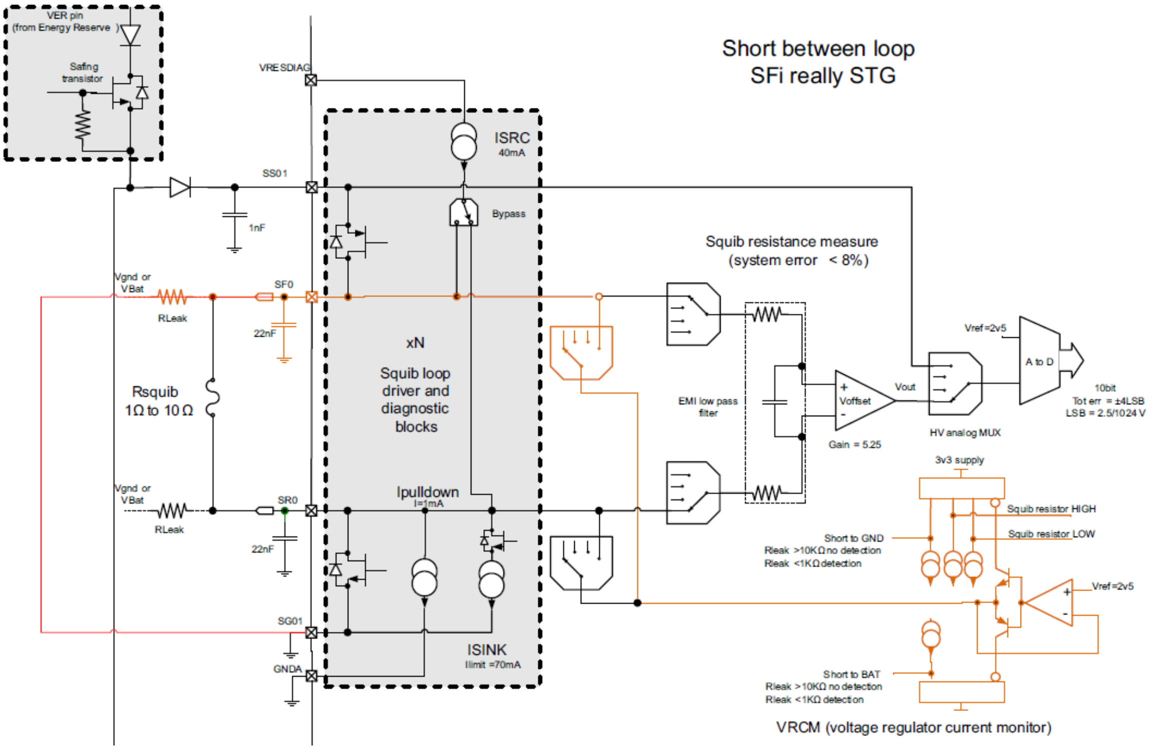
Table 33. Short between loops - LPDIAGREQ register

	(1)	(2)	15:14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	1	00	0	01 or 10	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 1 = pull-down current off for all channels 12, 11: 00 = ISRC off for all channels 10: 0 = ISINK off for all channels 9, 8: 01/10 = VRCM connected to SFx/SRx (LEAK_CHSEL channel)

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

4.1.6.1 High Side short to ground

Figure 18. High Side short to ground



Ipulldown is OFF for all channels.

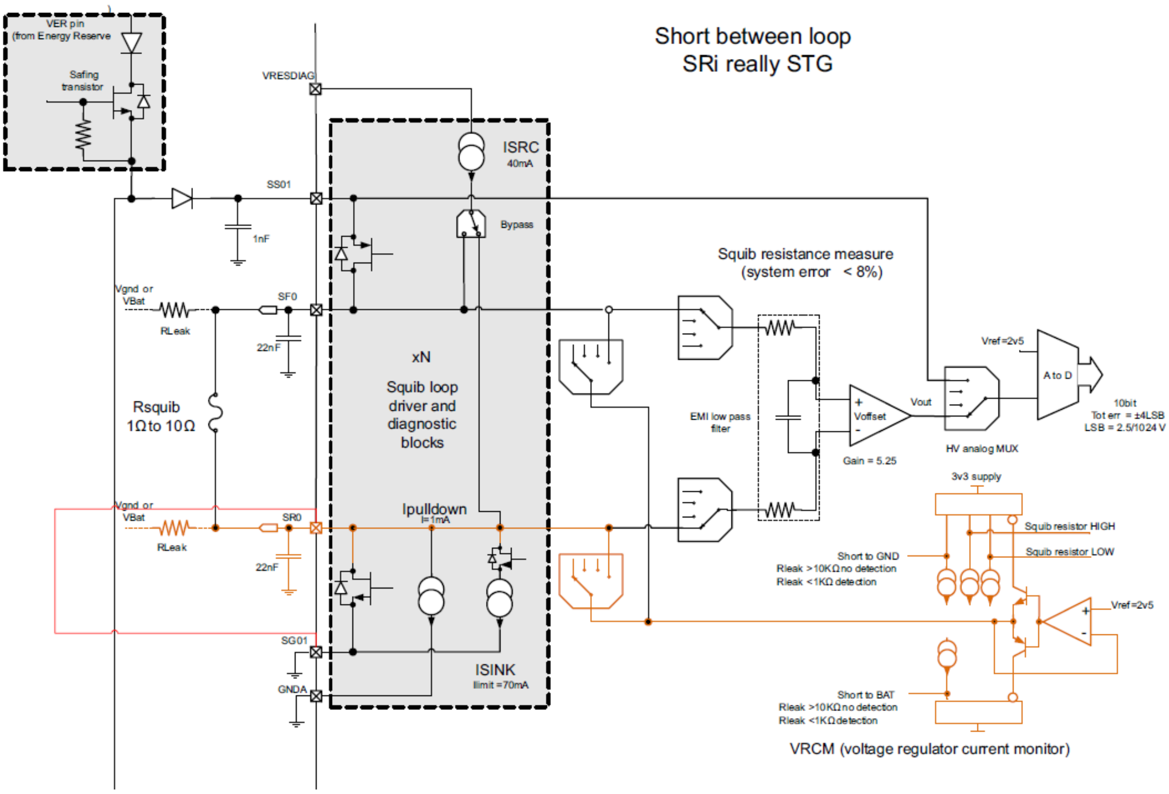
The VRCM circuit (see the Figure 18):

- Fixes SFx pin to 2.5 V.
- Reads the current through the SFx pin.
- Compares the current with a threshold.

The result is a STG on SFx.

4.1.6.2 *Low Side short to ground*

Figure 19. Low Side short to ground



Ipulldown is OFF for all channels.

The VRCM circuit (see the Figure 19):

- Fixes SRx pin to 2.5 V.
- Reads the current through the SRx pin.
- Compares the current with a threshold.

The result is a STG on SRx.

4.1.7 Squib resistance measurements

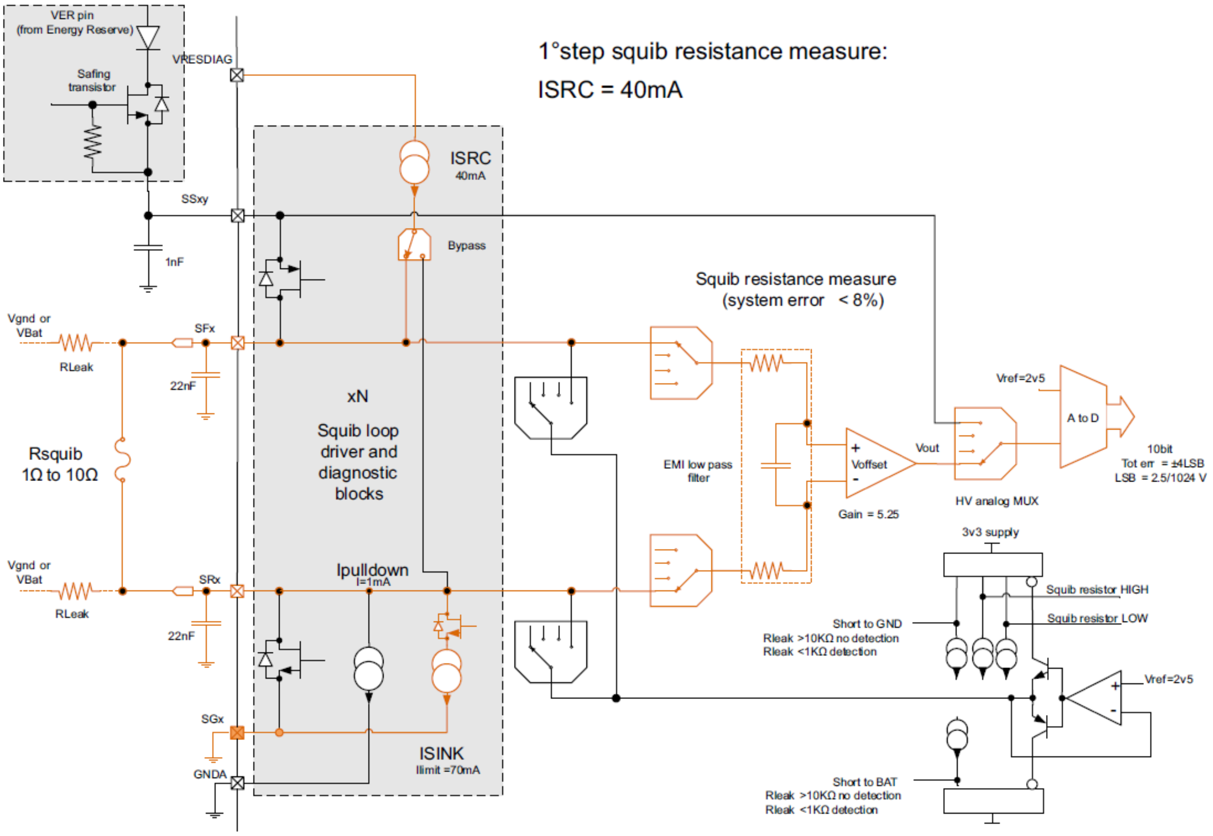
The IC allows measuring the squib resistance value in the range of 1 Ω ÷ 10 Ω with overall 8% precision.

This is a two-step process.

Note: *In Pyro Fuse Application with channels shorted together, the squib resistance measurement should be the same on all channels.*

4.1.7.1 *Squib resistance measurements - First step*

Figure 20. **Squib resistance measurements - First step**



Through this set-up (see the Figure 20):

- The ISRC is connected to the SFx.
- The squib is correctly connected between SFx and SRx.
- SRx is internally connected to ISINK that is able to sink the current.

The correspondent set up is done by setting the $38 LPDIAGREQ properly (see the Table 34):

Table 34. **Squib resistance measurements (first step) - LPDIAGREQ register**

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	1	01	1	00	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 1 = pull-down current off for all channels 12, 11: 01 = ISRC for RES_MEAS_CHSEL, off for the others 10: 1 = ISINK on for RES_MEAS_CHSEL, off for the others 9, 8: 00 = VRCM not connected

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The first step of the measurement is the read out of the voltage between SFx and SRx that is named resistance into ADC addressing.

This parameter is readable by the microcontroller, via 10bit ADC, through a dedicated request.

The registers to be read are still the four DIAGCTRL_X (see the Table 35).

Table 35. **Squib resistance measurements (first step) - DIAGCTRL_X register**

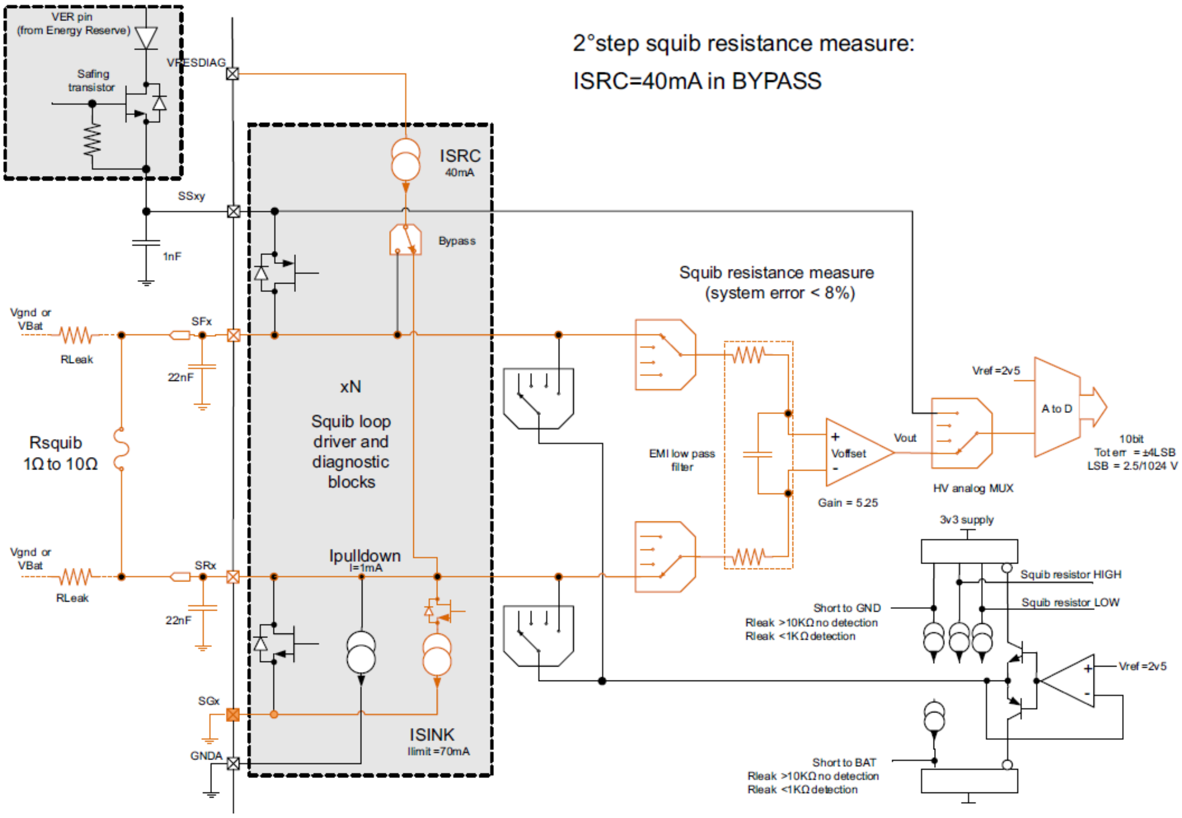
<table>
<tr><td colspan="5"></td><td>(1)</td><td>(2)</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td></td></tr>
<tr><td colspan="5">$3X DIAGCTRL_X
X = A, B, C, D</td><td>-</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="7">ADCREQ_X
$06 = squib x resistance</td><td rowspan="3">19: 1 = conversion finished</td></tr>
<tr><td>(3)</td><td>19</td><td>18</td><td>17</td><td>16</td><td rowspan="2">-</td><td rowspan="2">R</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td><td>ADCREQ_X</td><td colspan="6">ADCREQ_X
$06 = squib x resistance</td><td colspan="10">ADCREQ_X 10 bit ADC result</td></tr>
</table>

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Once read the ADC measurement, to obtain the value it is necessary to consider the divider ratio of the ADC. In case of resistance x, it is 1:1.

4.1.7.2 Squib resistance measurements - Second step

Figure 21. Squib resistance measurements - Second step



Through this set-up (see the Figure 21):

- The ISRC is connected to the SRx.
- The squib is correctly connected between SFx and SRx.
- SRx is internally connected to ISINK that is able to sink the current.

The correspondent set up is done by setting the $38 LPDIAGREQ properly (see the Table 36).

Table 36. Squib resistance measurements (second step) - LPDIAGREQ register

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	1	10	1	00	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 1 = pull-down current off for all channels 12, 11: 10 = bypass current on for RES_MEAS_CHSEL channel, off for the others 10: 1 = ISINK on for RES_MEAS_CHSEL channel, off for the others 9, 8: 00 = VRCM not connected

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The second step of the measurement is the read out of the voltage between SFx and SRx, named resistance into ADC addressing.

This measurement considers the leakage that may be present on the SFx and SRx pins.

As the previous measurement, also this is readable by the microcontroller, via a 10-bit ADC, through the same dedicated request.

The registers to be read are still the four DIAGCTRL_X.

Once read the ADC measurement, to obtain the value it is necessary to consider the divider ratio of the ADC. In case of resistance x, it is 1:1.

In LPDIAGSTAT it is possible to verify on which channel the resistance measurement has been performed (see the Table 37):

Table 37. Squib resistance measurements (second step) - LPDIAGSTAT register

					(1)	(2)	15:12	11:8	7:4	3:0	
$37 LPDIAGSTAT						R		RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	X	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 0 = low level diagnostic
(3)	19	18	17	16		R					
	0	0	0	0							

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Having the microcontroller these two measurements (that are two voltage drops across SF and SR), the squib resistance is so calculated:

$$\Delta V_{OUT} = (SFx - SRx)_1 - (SFx - SRx)_2 \tag{3}$$

$$R_{SQUIB} = \frac{\Delta V_{OUT}}{G * ISRC} \tag{4}$$

With:

- G = 5.25 ± 2% (differential amplifier gain)
- ISRC = 40 mA ± 5%

Immediately after the ADC read-out, ISRC is automatically switched OFF to reduce the power consumption.

Example:

- $ADC_{1ST\ CONVERSION}$ = 0b0100111000 = 312
- $ADC_{2ND\ CONVERSION}$ = 0b0010000001 = 129
- Δ_{ADC} = 312 - 129 = 183

In order to obtain the result in Volt, being the ADC characteristic linear:

$$2.5\,V : 1024 = x : \Delta_{ADC} \quad \rightarrow x = \frac{183 * 2.5\,V}{1024} = 0.44\,V \tag{5}$$

In order to obtain resistance value, considering typical factors:

$$R_{SQUIB} = \frac{x}{G * ISRC} = \frac{0.44\,V}{5.25 * 40\,mA} = 2.1\,\Omega \tag{6}$$

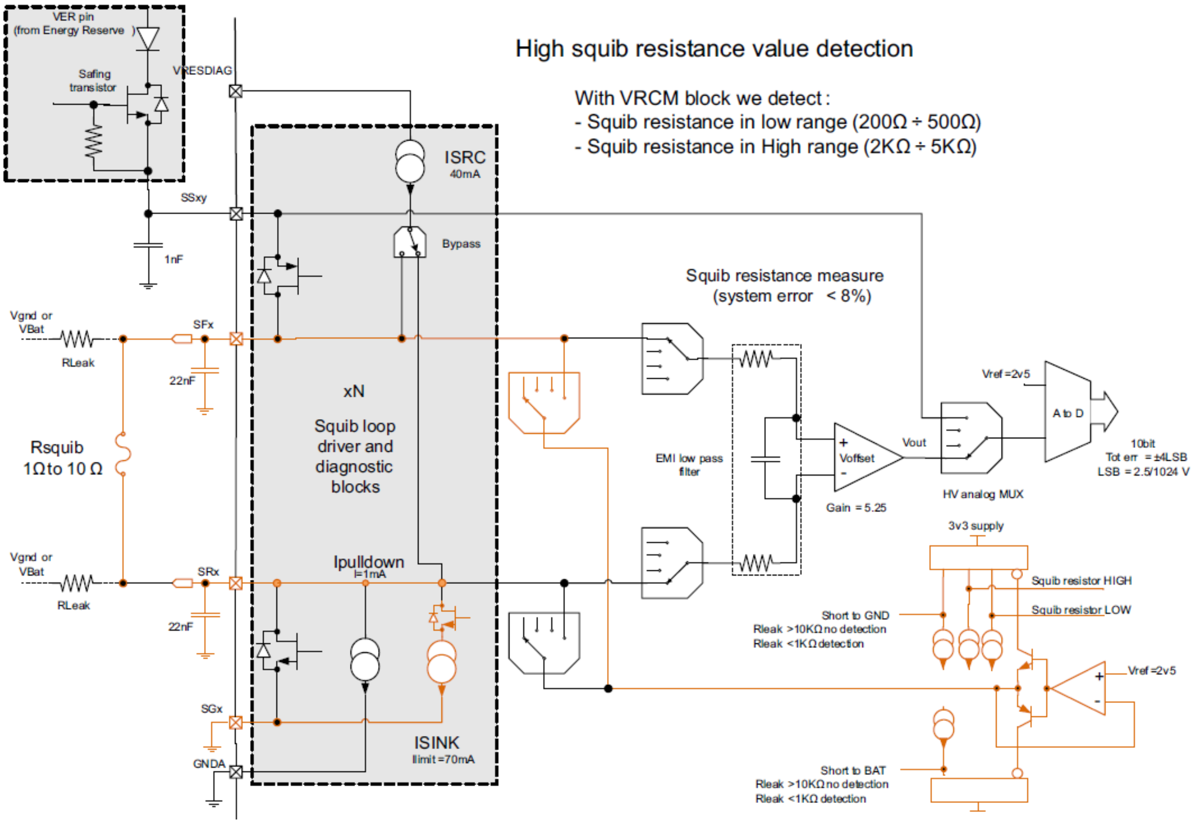
4.1.8 High squib resistance diagnostic

The aim of the test is to understand if the squib resistor is below 200 Ω, between 500 Ω and 2 kΩ, or beyond 5 kΩ.

In case of a very high squib resistance, there is the possibility to set a lower ISRC current, through the ISRC_CURR_SEL bit, bit 14 in the $38 LPDIAGREQ register. In this way, ADC maintains a good dynamic.

The Figure 22, referred to ISRC = 40 mA, is true also in case of ISRC = 8 mA.

Figure 22. High squib resistance diagnostic



Through this set-up (see the Figure 22):

- The ISINK is connected to the SRx.
- The squib is correctly connected between SFx and SRx.
- SRx is internally connected to ISINK that can sink the current.

Note: In Pyro Fuse Application with channels shorted together, the high squib resistance measurement should be the same on all channels.

The correspondent set up is done by setting the $38 LPDIAGREQ properly (see the Table 38):

Table 38. High squib resistance diagnostic - LPDIAGREQ register

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0/1	1	00	1	01	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA, 1 = ISRC = 8 mA 13: 1 = pull-down current off for all channels 12, 11: 00 = ISRC off for all channels 10: 1 = ISINK on for RES_MEAS_CHSEL channel, off for the others 9, 8: 01 = VRCM connected to SFx (LEAK_CHSEL channel)

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

ISINK and VRCM have to be addressed to the same channel, that means RES_MEAS_CHSEL (bit[7:4]) and LEAK_CHSEL (bit[3:0]) are equal. If there is a wrong selection in the two fields there is no notice of the mistake.

Through this set-up, the VRCM is connected to SFx and ISINK to SRx. Current flowing through SFx is measured and compared with the ISRlow and ISRhigh (6 mA and 0.7 mA respectively) thresholds to identify in which range the resistor measured is.

- HSR HIGH = $R_{SquibHigh}$ = 2 kΩ ÷ 5 kΩ
- HSR LOW = $R_{SquibLow}$ = 200 Ω ÷ 500 Ω

In case of low resistance value, as with 2 Ω load, VRCM sees a path from SRx and GND, so STG (very low impedance towards ground) could be detected (see the Table 39).

Read out of these bits has to be done before the next diagnostic request, because these bits are not latched.

Table 39. High squib resistance diagnostic - LPDIAGSTAT register

					(1)	(2)	15:14	13	12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R				RES_MEAS_CHSEL					LEAK_CHSEL	
(3)	19	18	17	16		R										
	0	0	0	0				0	1	0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	X	0/1	X	1	0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 0 = low level diagnostic 13: 0 = resis < HSR HIGH 1 = resis > HSR HIGH 12: 0 = resis < HSR LOW 1 = resis < HSR LOW 6: 1 = STG detected 4: 1 = VRCM to SFx

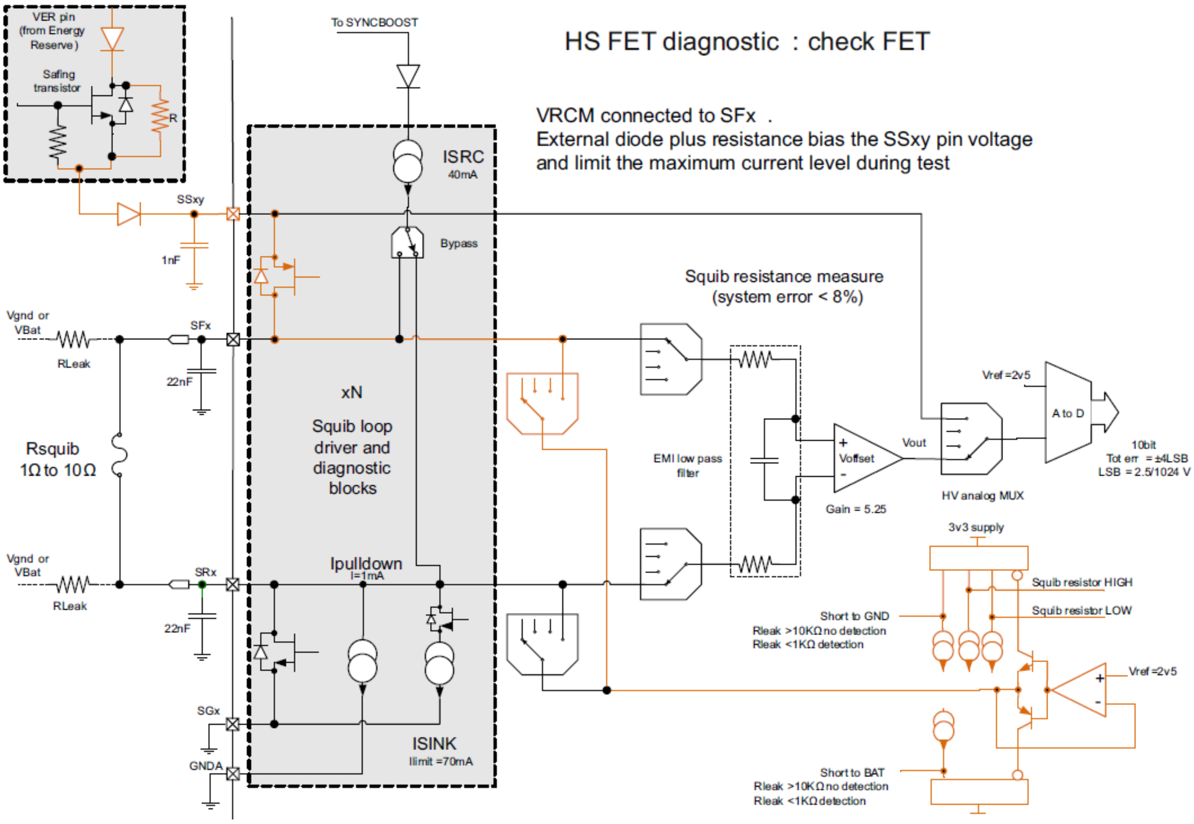
1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

4.1.9 High Side FET diagnostic

The test is possible only in the diagnostic phase.

Before running this test, VRCM has to be previously validated and leakage tests have to be already performed with no fails found. At this point, the HIGH SIDE FET test can be performed.

Figure 23. High Side FET diagnostic



ISRC and ISINK are kept off and VRCM is connected to SFx (see the Figure 23) through the LEAK_CHSEL bits in the LPDIAGREQ register (see the Table 40). The High Side FET test is enabled through the SYSDIAGREG register.

Table 40. High Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	1	00	0	01	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 1 = pull-down current off for all channels 12, 11: 00 = ISRC off for all channels 10: 0 = ISINK off for all channels 9, 8: 01 = VRCM connected to SFx (LEAK_CHSEL channel)
$36 SYSDIAGREQ	D	W	X	X	X	X	X	X		0 | 1 | 1 | 1	DSTEST: 0111 = HS FET active

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Test result

The High Side FET test turns ON the HS power: if it turns ON correctly, SFx is connected to SSxy which is at VER voltage through the resistor R in parallel to the safing FET.

During the test, the device monitors the current flowing through VRCM.

If the High Side FET works properly, this current exceeds the thresholds I_{HSFET}, that is 1.8 mA ± 10%, and the channel is immediately turned off.

In case the current doesn't exceed the limit mentioned, after the time $T_{FETTIMEOUT}$, that is 200 μs, the test is terminated, and the output is turned off.

During the $T_{FETTIMEOUT}$ period, FET activation is flagged through a bit, FETON, readable via SPI.

In any condition, the current in SFx doesn't exceed I_{SVRCM} (I_{LIM_SRC} = -20 ÷ -10 mA and I_{LIM_SNK} = 10 ÷ 20 mA), and during the FET test the energy provided to the squib is limited at $E_{FETtest}$ (< 170 μJ).

Table 41. High Side FET diagnostic - LPDIAGSTAT register

					(1)	(2)	15	14:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R			RES_MEAS_CHSEL					LEAK_CHSEL	
(3)	19	18	17	16		R									
	0	0	0	0			0/1		0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	0	0	1	1	0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 0 = low level diagnostic 15: 0 = FET off during diagnostic, 1 = FET on during diagnostic 7: 0 = no short between loops 6: 0 = STG not detected 5: 1 = STB detected 4: 1 = VRCM connected to SFx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Possible results for High Side FET test are (see the Table 41):

- STB = 1 and STG = 0 → ok.
- STB = 0 or STG = 1 → missing SSxy connection during FET test, or High Side not switched ON, or short to GND during FET test.

STG and STB, after FET test, are latched. They are cleared through a new LPDIAGREQ or a new SYSDIAGREQ.

Note:

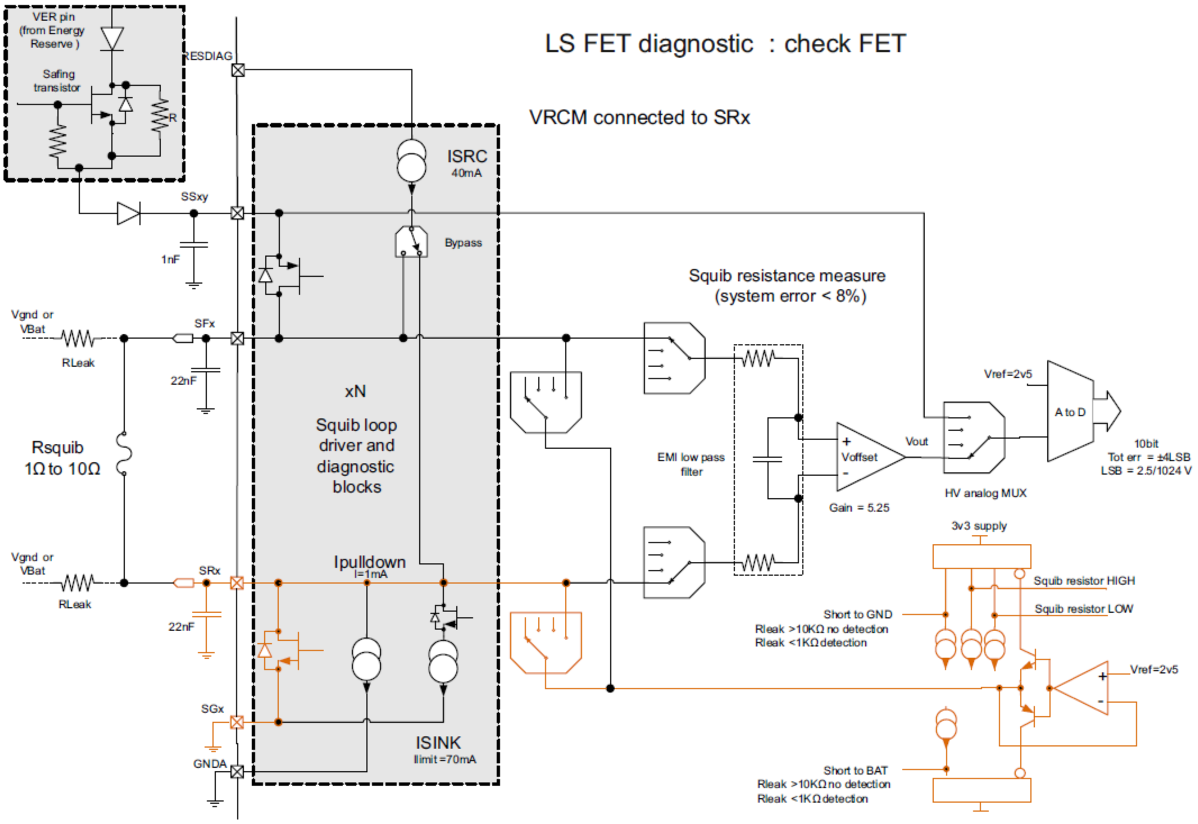
- *If VRCM is not previously connected to the SFx and the test is run, a dangerous condition could happen.*
- *In case of SRx shorted to GND, when the HS is turned ON, even if the current flowing through the squib is greater than IHSFET, the HS is not immediately turned off and the current flows through the squib until* $T_{FETTIMEOUT}$ *expires. This could determine an undesired deployment.*

4.1.10 Low Side FET diagnostic

The test is possible only in the diagnostic phase.

Before running this test, VRCM has to be previously validated and leakage tests have to be already performed with no fails found. At this point, the LOW SIDE FET test can be performed.

Figure 24. Low Side FET diagnostic



ISRC and ISINK are kept off and VRCM is connected to SRx (see the Figure 24) through the LEAK_CHSEL bits in the LPDIAGREG register (see the Table 42). The Low Side FET test is enabled through the SYSDIAGREG register.

Table 42. Low Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers

	(1)	(2)	15	14	13	12:11	10	9:8	7:4	3:0	
$38 LPDIAGREQ	(I)	W	0	0	1	00	0	10	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	LEAK_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 0 = low level diagnostic 14: 0 = ISRC = 40 mA 13: 1 = pull-down current off for all channels 12, 11: 00 = ISRC off for all channels 10: 0 = ISINK off for all channels 9, 8: 10 = VRCM connected to SRx (LEAK_CHSEL channel)
$36 SYSDIAGREQ	D	W	X	X	X	X	X	X		1 0 0 0	DTEST: 1000 = LS FET active

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Test result

The Low Side FET test turns ON the LS power: if it turns ON correctly, SRx is connected to SGxy.

During the test, the device monitors the current flowing through VRCM.

If the Low Side FET works properly, this current exceeds the thresholds I_{HSFET}, that is 1.8 mA ± 10%, and the channel is immediately turned off.

In case the current doesn't exceed the limit mentioned, after the time $T_{FETTIMEOUT}$, that is 200 µs, the test is terminated, and the output is turned off.

During the $T_{FETTIMEOUT}$ period, FET activation is flagged through a bit, FETON, readable via SPI.

In any condition, the current in SRx doesn't exceed I_{SVRCM} (I_{LIM_SRC} = -20 ÷ -10 mA and I_{LIM_SNK} = 10 ÷ 20 mA), and during the FET test the energy provided to the squib is limited at $E_{FETtest}$ (< 170 µJ).

Table 43. Low Side FET diagnostic - LPDIAGSTAT register

					(1)	(2)	15	14:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R			RES_MEAS_CHSEL					LEAK_CHSEL	
(3)	19	18	17	16		R									
	0	0	0	0			0/1		0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	0	1	0	0	0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 0 = low level diagnostic 15: 0 = FET off during diagnostic, 1 = FET on during diagnostic 7: 0 = no short between loops 6: 1 = STG detected 5: 0 = STB not detected 4: 0 = VRCM connected to SRx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Possible results for Low Side FET test are (see the Table 43):

- STB = 0 and STG = 1 → ok
- STB = 1 or STG = 0 → short to battery in Low Side, or Low Side not switched ON.

STG and STB, after FET test, are latched. They are cleared through a new LPDIAGREQ or a new SYSDIAGREQ.

Note:
- *Ground loss (SGxy) is not detected through FET test because there is a diode between SGxy and the substrate.*
- *If VRCM is not previously connected to the SRx and the test is run, a dangerous condition could happen.*
- *In case of SFx shorted to SSxy, when the LS is turned ON, even if the current flowing through the squib is greater than I_{LSFET}, the LS is not immediately turned off and the current flows through the squib until $T_{FETTIMEOUT}$ expires. This could determine an undesired deployment.*
- *In case of SRx shorted to SSxy, when the LS is turned ON, even if the current flowing through it is greater than I_{LSFET}, the LS not immediately turned off and the current flows until $T_{FETTIMEOUT}$ expires. Such a high current could damage the LS power.*

4.1.11 Loss of ground

This test is based on the voltage of the ground pin, SGxy, during the squib resistor measurement or the High Side driver diagnostic.

Any voltage shift of the SGxy pin over V_{SGopen}, that is 400 to 800 mV, is considered loss of ground, readable in the LP_GNDLOSS register (see the Table 44).

Table 44. Loss of ground - LP_GNDLOSS register

<table>
<tr><td colspan="5"></td><td>(1)</td><td>(2)</td><td>15:12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td></td></tr>
<tr><td colspan="5">$26 LP_GNDLOSS</td><td></td><td>R</td><td rowspan="3">0</td><td rowspan="3">CHB</td><td rowspan="3">CHA</td><td rowspan="3">CH9</td><td rowspan="3">CH8</td><td rowspan="3">CH7</td><td rowspan="3">CH6</td><td rowspan="3">CH5</td><td rowspan="3">CH4</td><td rowspan="3">CH3</td><td rowspan="3">CH2</td><td rowspan="3">CH1</td><td rowspan="3">CH0</td><td rowspan="3">0 = no loss of ground
1 = loss of ground</td></tr>
<tr><td>(3)</td><td>19</td><td>18</td><td>17</td><td>16</td><td></td><td>R</td></tr>
<tr><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td></td></tr>
</table>

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

GNDLOSSx is set considering tSGopen filter time (46 to 50 µs) and it is cleared upon read.

4.1.12 Safing FET diagnostic

The aim of the test is to verify the SSxy voltage level.

VSF is turned ON via SPI through the DSTEST bit of the $36 SYSDIAGREQ register (see the Table 45).

Table 45. Safing FET diagnostic - SYSDIAGREQ register

	(1)	(2)	15:4	3:0
$36 SYSDIAGREQ	D	W	X	DSTEST 0110 = VSF regulator active

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

VSF and SSxy voltages are readable by the microcontroller through the ADC converter in the $3X DIAGCTRL_x registers (see the Table 46).

Table 46. Safing FET diagnostic - DIAGCTRL_X register

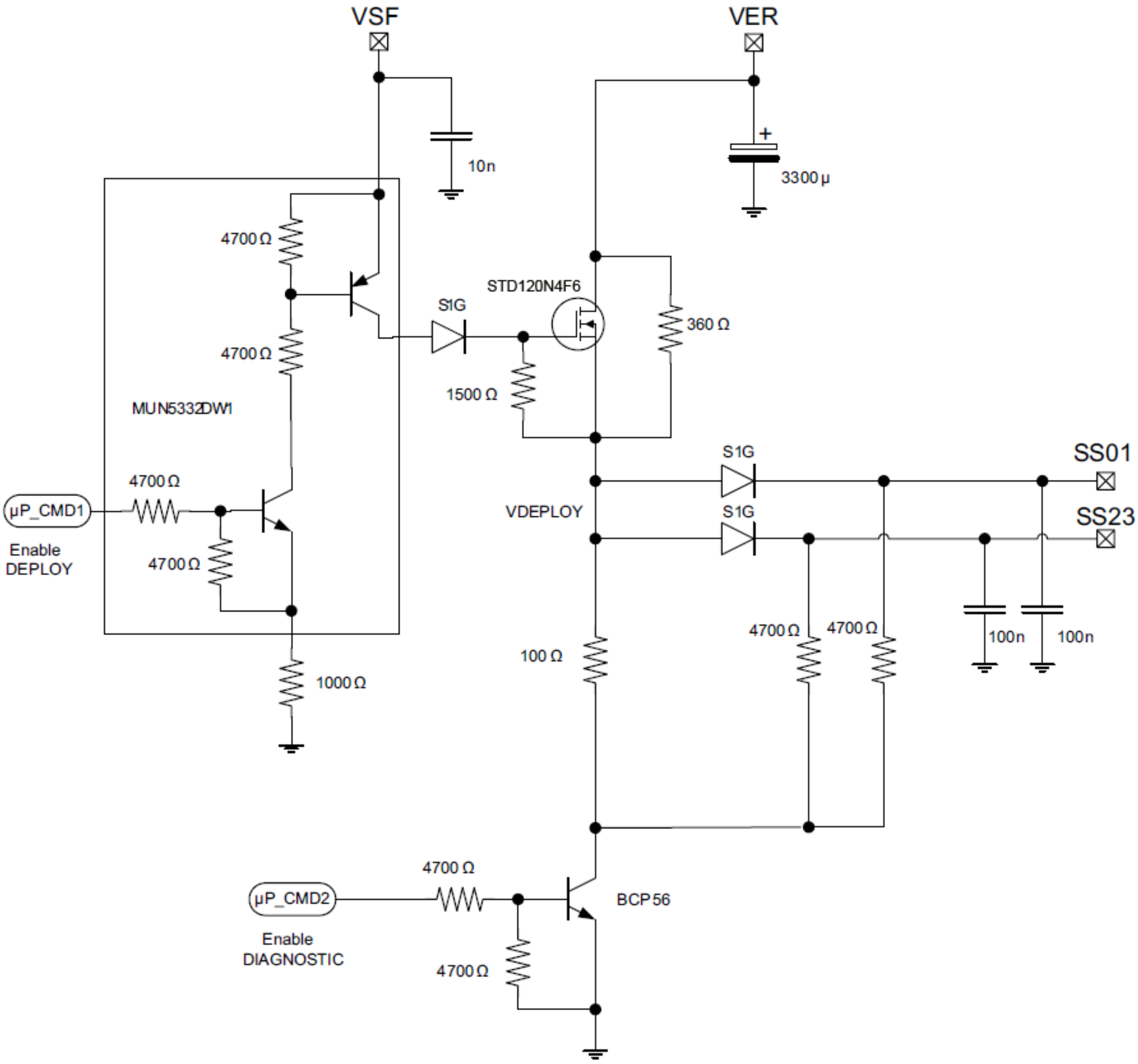
<table>
<tr><td colspan="5"></td><td>(1)</td><td>(2)</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td></td></tr>
<tr><td colspan="5">$3X DIAGCTRL_X
X = A, B, C, D</td><td>-</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="7">ADCREQ_X
$2A = VSF
$36 = SS0
$37 = SS1
$38 = SS2
$39 = SS3
$3A = SS4
$3B = SS5
$3C = SS6
$3D = SS7
$3E = SS8
$3F = SS9
$40 = SSA
$41 = SSB</td><td></td></tr>
<tr><td>(3)</td><td>19</td><td>18</td><td>17</td><td>16</td><td rowspan="2">-</td><td rowspan="2">R</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td rowspan="2">19: 1 = conversion finished</td></tr>
<tr><td></td><td>1</td><td>0</td><td>0</td><td>ADCREQ_X</td><td colspan="6">ADCREQ_X
$2A = VSF
$36 = SS0
$37 = SS1
$38 = SS2
$39 = SS3
$3A = SS4
$3B = SS5
$3C = SS6
$3D = SS7
$3E = SS8
$3F = SS9
$40 = SSA
$41 = SSB</td><td colspan="10">ADCREQ_X 10 bit ADC result</td></tr>
</table>

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Once read the ADC measurement, to obtain the voltage value it is necessary to consider the divider ratio of the ADC. In case of SSxy, it is 15:1.

In the Figure 25 a possible solution to perform the test is represented. Such a solution allows performing SAFING FET test only if the external reserve capacitor CER has been charged.

Figure 25. **Safing FET diagnostic**



It also requires an external component network and two commands from the microcontroller, µP_cmd1 and µP_com2. Depending on the status of the VSF (ON or OFF) and on the commands from the microcontroller, the cases described in the Figure 26 can occur.

Figure 26. **Safing FET diagnostic - Test cases**

VSF	µP_cmd1	µP_cmd2	SSxy pin voltage range = VDEPLOY – Vdiode =	normal operating
			= VSF-Vcesat-Vdiode-Vgs-Vdiode	
ON	1	1		FET reg and Diagnostic enabled
			10v 22v	
			= (VER-Vcesat)x100/(100+360)+Vcesat-Vdiode	
X	0	1		FET reg disabled, Diagnostic enabled
			4v 7v	
			= VER-Vdiode	
X	X	0		FET reg and Diagnostic disabled
			22.6v	

In the first case of the Figure 25, µp_cmd1 = µp_cmd2 = 1, so the external FET is working in voltage regulator mode (with VSF ON) and the voltage on the SSxy pin is:

$$V_{SSxy} = VSF - V_{CEsat} - V_{DIODE} - V_{GS} - V_{DIODE} \quad (7)$$

The expected value read on ADC, depending on all the parameter variations, is in the range of 10 V÷22 V.

In the second case, µp_cmd1=0, µp_cmd2=1, so the external FET is off and the voltage on the SSxy pin is:

$$V_{SSxy} = V_{CEsat} + (VER - V_{CEsat}) * \frac{100\,\Omega}{100\,\Omega - 360\,\Omega} - V_{DIODE} \quad (8)$$

The expected value read on ADC, depending on all the parameter variations, is in the range of 4 V÷7 V.

In the third case everything is disabled, so the voltage on SSxy is expected to be close to VER:

$$V_{SSxy} \approx VER - V_{DIODE} \quad (9)$$

In case of an ADC reading out of the expected range, it has to be considered as a faulty condition.

Once µp_cmd2 = 1, capacitors on the SSxy pins are discharged through the 4.7 kΩ resistor. This requires about 1ms to reach steady state, so a proper time should be elapsed before running the ADC conversion.

Besides, in order to guarantee more safety, it is possible to read the voltage on VDEPLOY net through a voltage divider which is sensed by ADC of the microcontroller.

In order to guarantee redundancy on safing FET enabling, two independent conditions must be verified. The assertion of the two conditions must come from two separate activation logics.

In the solution here presented, the first condition (VSF switch ON) comes from the IC in arming state, while the second one (µp_cmd1 asserted) comes from the microcontroller.

In case the ARMING algorithm is run by the microcontroller, the circuit which turns on the safing FET can be removed (both MUN5332DW1 and S1G diode):

- VSF can be connected directly to the FET gate.
- µp_cmd1 and µp_cmd2 can be used to drive ARMx and ARM4.

The values of the two resistors could be increased in order to reduce power dissipation.

Two guidances should be followed:

1. The resistors should be big enough to avoid to trigger inadvertent deployment due to short to ground/battery.
2. The resistors should be low to have a better precision when the ADC read is performed (bigger is the value, bigger is the uncertainty).

For example, 0805 1% thick film resistors can be used, 2 x 221 Ω and 2 x 110 Ω.

4.1.13 Deployment time diagnostic

The aim of the test is to pass to the microcontroller the deploy time information that the IC has stored with the previous SPI commands.

This test is possible only in DIAG state.

Table 47. Deployment time diagnostic - SYSDIAGREQ register

	(1)	(2)	15:4	3:0
$36 SYSDIAGREQ	D	W	X	DSTEST 1001 = output timing on ARM1 pin

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Once the $36 SYSDIAGREQ register is set for output timing on the ARM1 pin check (see the Table 47), even if the test has been performed, it is not possible any modification in the deployment channel configuration ($06 DCR_0 ÷ $11 DCR_B registers).

This feature prevents any modification in the deployment time and deployment current after the test has been performed and, therefore, it is no longer visible by the microcontroller.

To modify again the deployment channel configuration ($06 DCR0, $07 DCR1, $08 DCR2, $09 DCR3 registers) it is first necessary to change the DSTEST request, and secondly to modify the deployment channel configuration itself as previously done.

Test result

Once the test is ongoing, a signal 0 V → 5 V/3.3 V (depending on VCCSEL) is output on the ARM1 pin, which reports in sequence, from channel 0 to channel B, the deployment time programmed, with an 8ms delay between each channel. Starting from ch0, the ARM1 signal is high for the deploy time of ch0; then it remains low until the next pulse corresponding to the channel 1 occurs (8ms delay between each pulse to start); the same happens with all the other channels (see the Figure 27, Figure 28 and Figure 29).

The microcontroller can test the latest deployment time programmed in the DRCx registers measuring the duration of the high ARM1 pulse.

If the test is performed on a channel with no deployment time previously configured, the high ARM1 pulse lasts 8 µs.

If the combination time/current deployment programmed for a channel is wrong, then the combination time/current deployment turns back to the default value. In case the deployment time is monitored through the ARM1 signal, the default one is output.

Figure 27. Deployment time diagnostic sequence

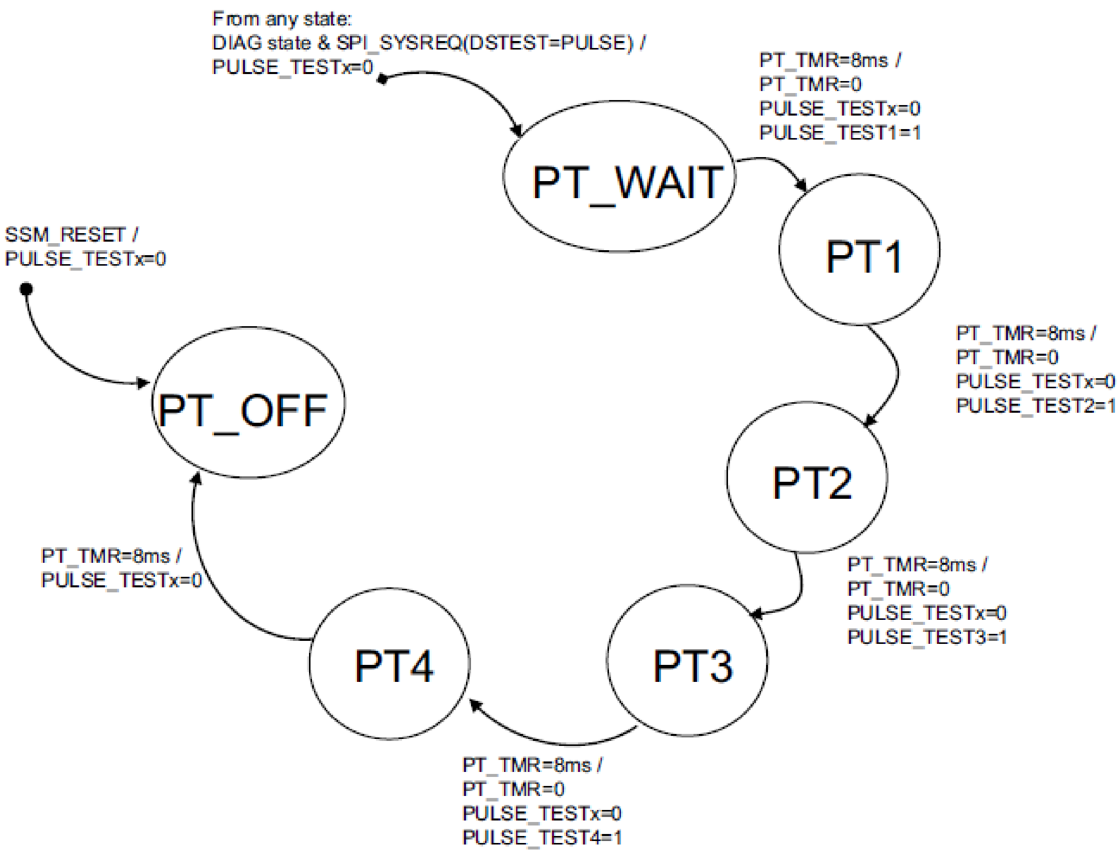


Figure 28. Deployment time - No configuration

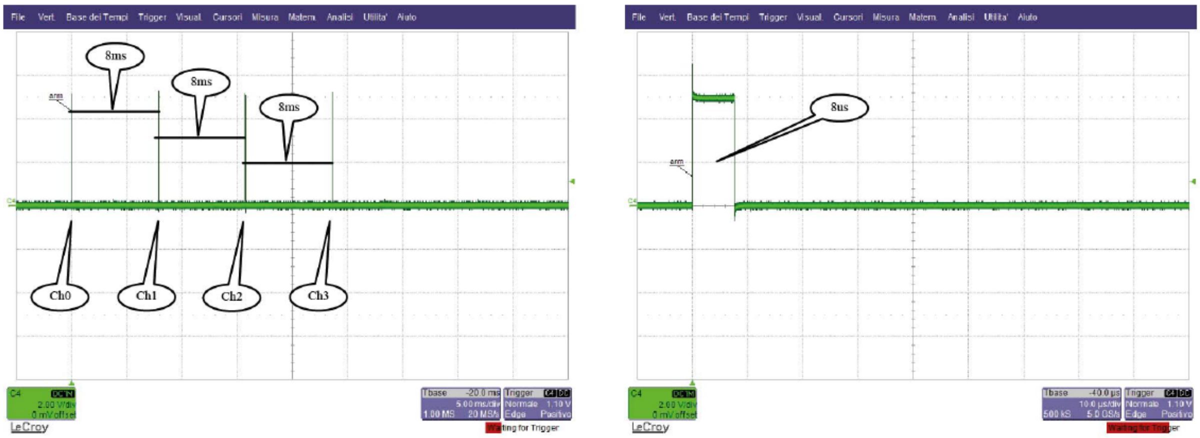
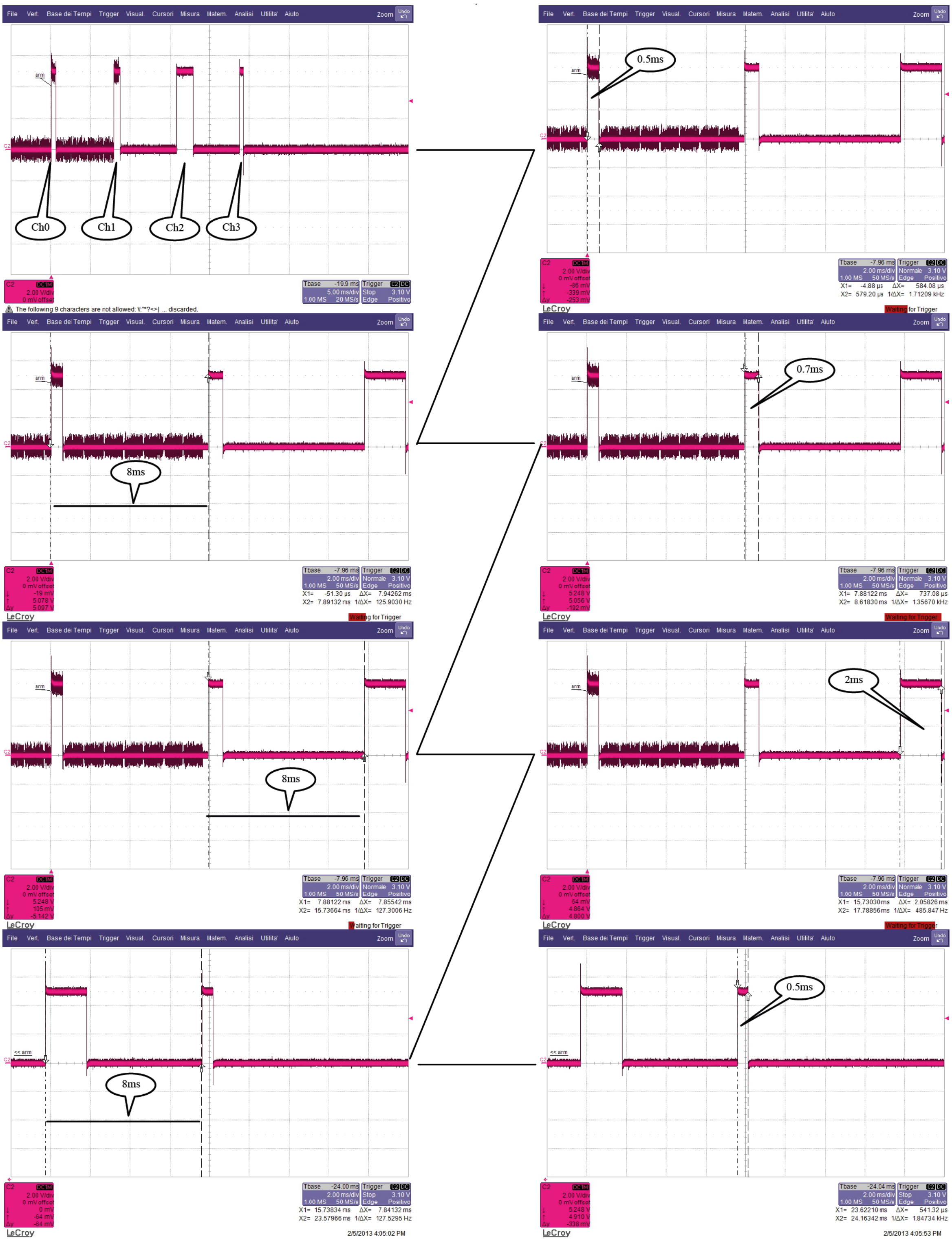


Figure 29. **Deployment Time**



Ch0: depl time=0.5ms, depl curr=1.2A,
Ch1: depl time=0.7ms, depl curr=1.2A,
Ch2: depl time=2ms, depl curr=1.2A,
Ch3: depl time=2ms, depl curr=1.75A→ turns to depl time=0.5ms, depl curr=1.2A

4.2 High level diagnostic

The device performs the measurement, as requested by the microcontroller, through the LPDIAGREQ register.

Based on the requests from the microcontroller, diagnostics run according to the setups described for the low level mode but each test set up is driven step by step by the IC itself.

The IC timing schedule is selected through the HI_LEV_DIAG_TIME bit in INIT (see the Table 48):

Table 48. High level diagnostic

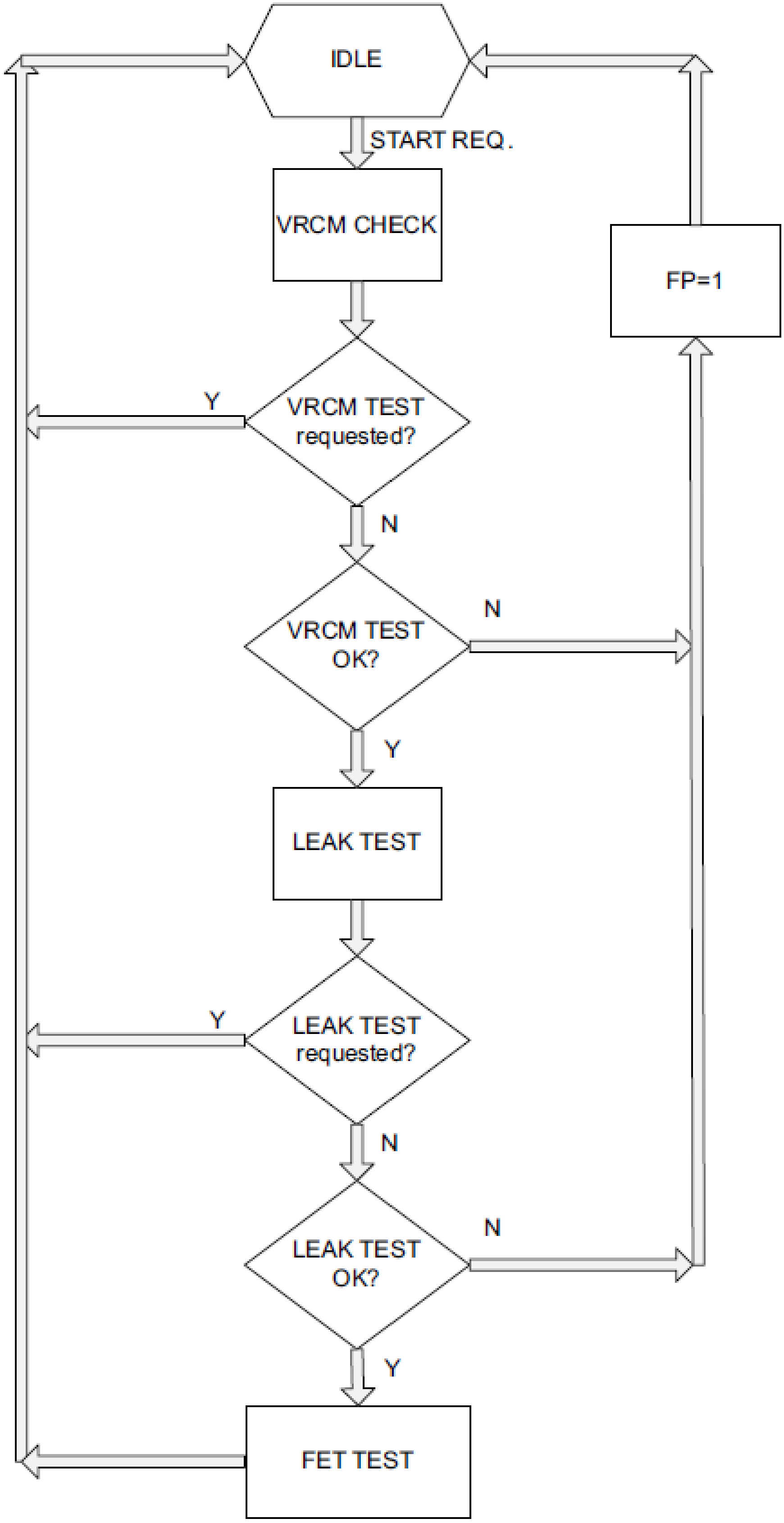
	(1)	(2)	15	14:11	10	9:8	7:5	4	3:0	
$01 SYS_CFG	I	W		X	0	X	X	X	X	10: HI_LEV_DIAG_TIME 0 = short time 1 = long time
$38 LPDIAGREQ	(I)	W	1	X	X	X	HIGH_LEVEL_DIAG_SEL 000 = no diag selected 001 = VRCM check 010 = leakage check 011 = short between loops check 100 = unused 101 = squib resistance range check 110 = squib res measure 111 = FET test	SQP	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 1 = high level diagnostic 4: 0 = leakage test on SRx, 1 = leakage test on SFx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

In case of high level diagnostic selection, the IC automatically schedules the preparatory tasks to be eventually run in order to perform the required diagnostic.

The flow chart in the Figure 30 shows the time sequence implemented:

Figure 30. High level diagnostic flow



The FP bit in the LPDIAGSTAT register is available only in case of high level diagnostic selected. It is stuck at 0 otherwise.

Once a test which requires preliminary measurement phases is selected (i.e. leakage test and FET test), this bit is set if the diagnostic procedure has been stopped because of a fault recorded in such a preliminary step.

Two diagnostic flows are implemented, as shown in the Figure 31 and Figure 32:

Figure 31. High level loop diagnostic flow 1

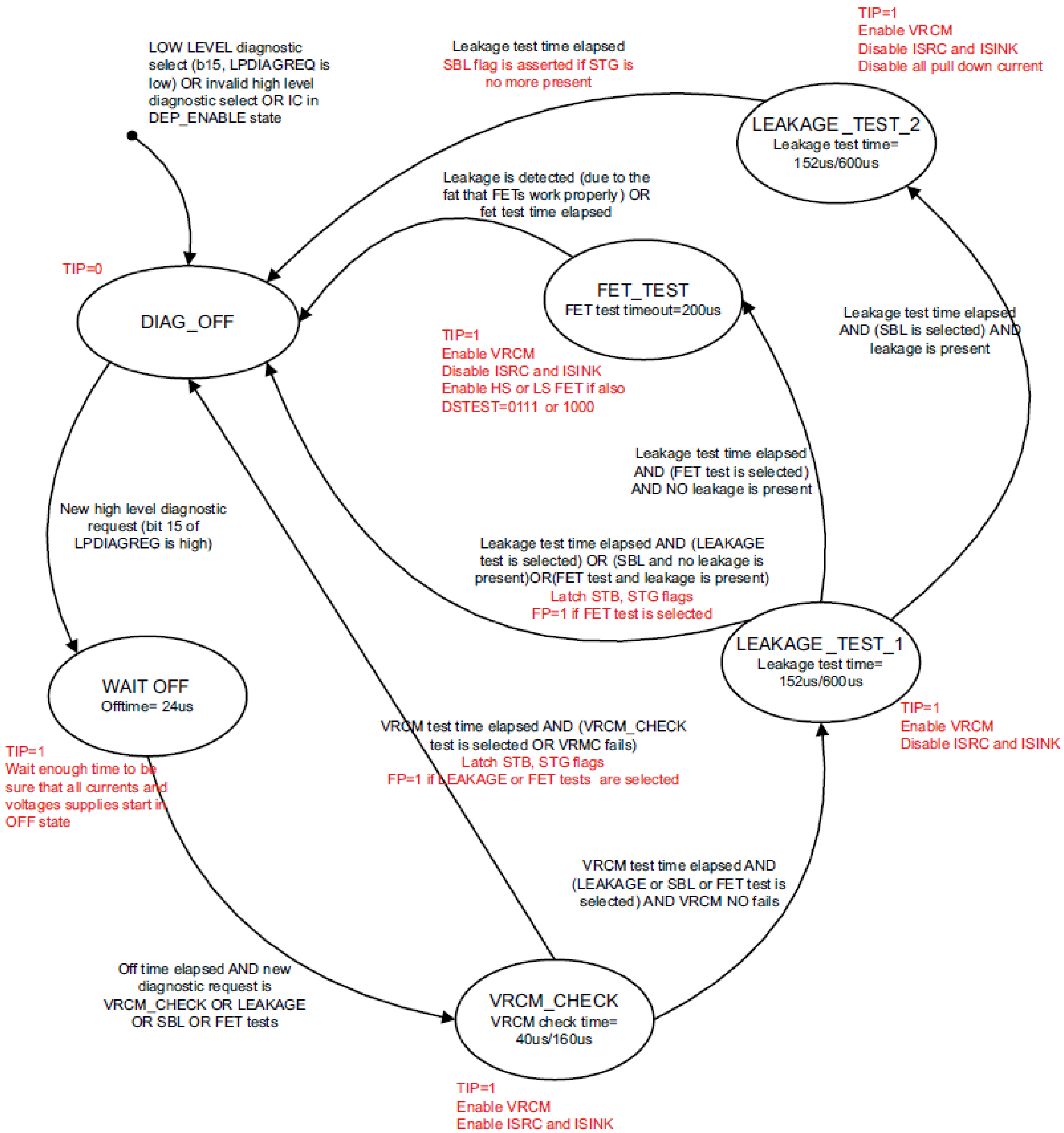
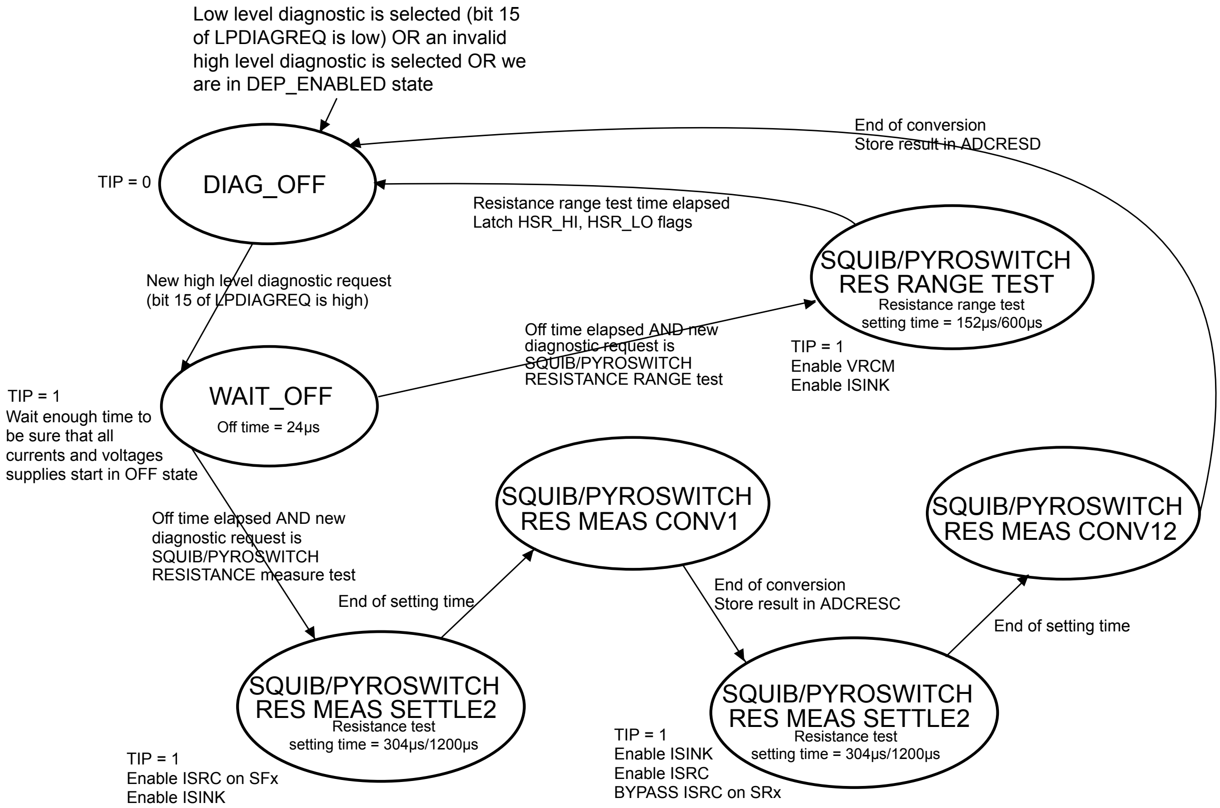
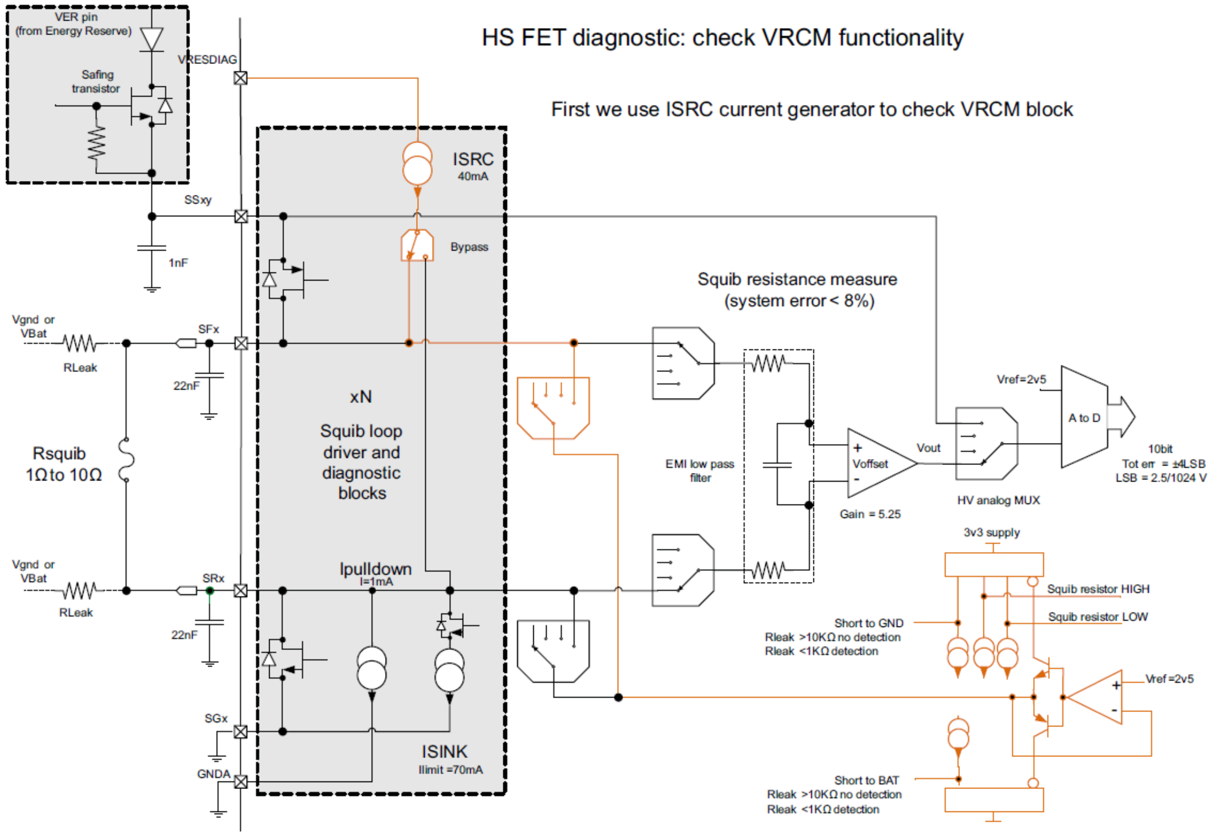


Figure 32. High level loop diagnostic flow 2



4.2.1 VRCM check - High Side

Figure 33. **VRCM check - High Side (Diagnostic)**



The correspondent set up (see the Figure 33) is done by setting the $38 LPDIAGREQ register properly (see the Table 49).

Table 49. **VRCM check, High Side - LPDIAGREQ register**

	(1)	(2)	15	14:8	7:5	4	3:0	
$38 LPDIAGREQ	(I)	W	1	X	HIGH_LEVEL_DIAG_SEL 001 = VRCM Check	1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 1 = high level diagnostic 4: 1 = leakage test on SFx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*

2. R = READ, W = WRITE

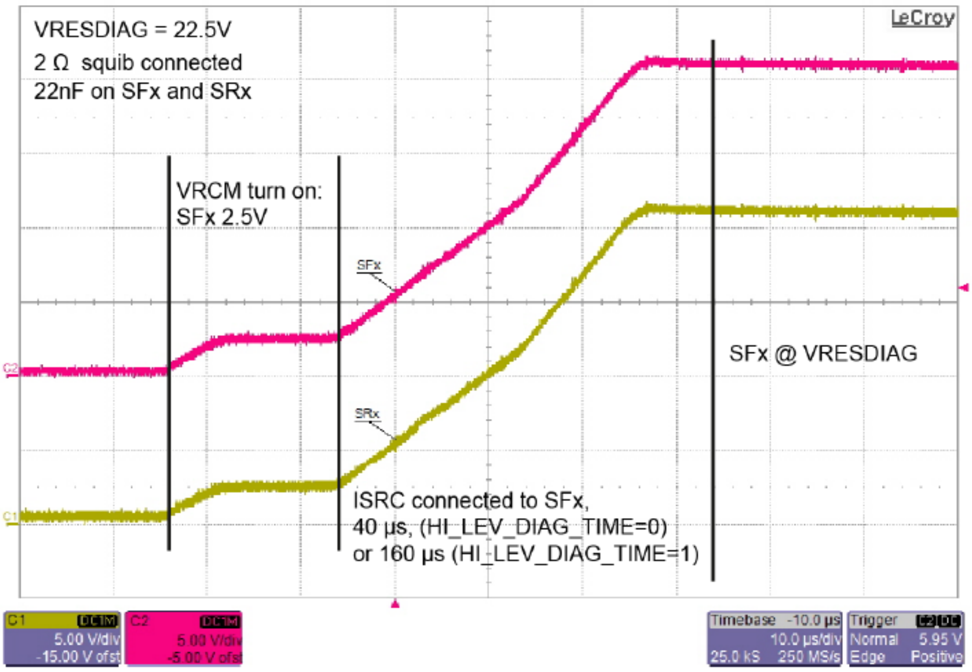
The result of the diagnostic is readable in the $37 LPDIAGSTAT register (see the Table 50) and shown in the Figure 34:

Table 50. VRCM check, High Side - LPDIAGSTAT register

					(1)	(2)	15:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R	X	HIGH_LEVEL_DIAG_SEL 0001 = VRCM Check	0	0	1	1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 =ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 1 = high level diagnostic 18: 1 = high level diag is running 7: 0 = no short between loops 6: 0 = STG not detected 5: 1 = STB detected 4: 1 = leakage test on SFx
(3)	19	18	17	16		R								
	1	0/1	0	0										

1. I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING
2. R = READ, W = WRITE
3. Further bit over the 16 standard.

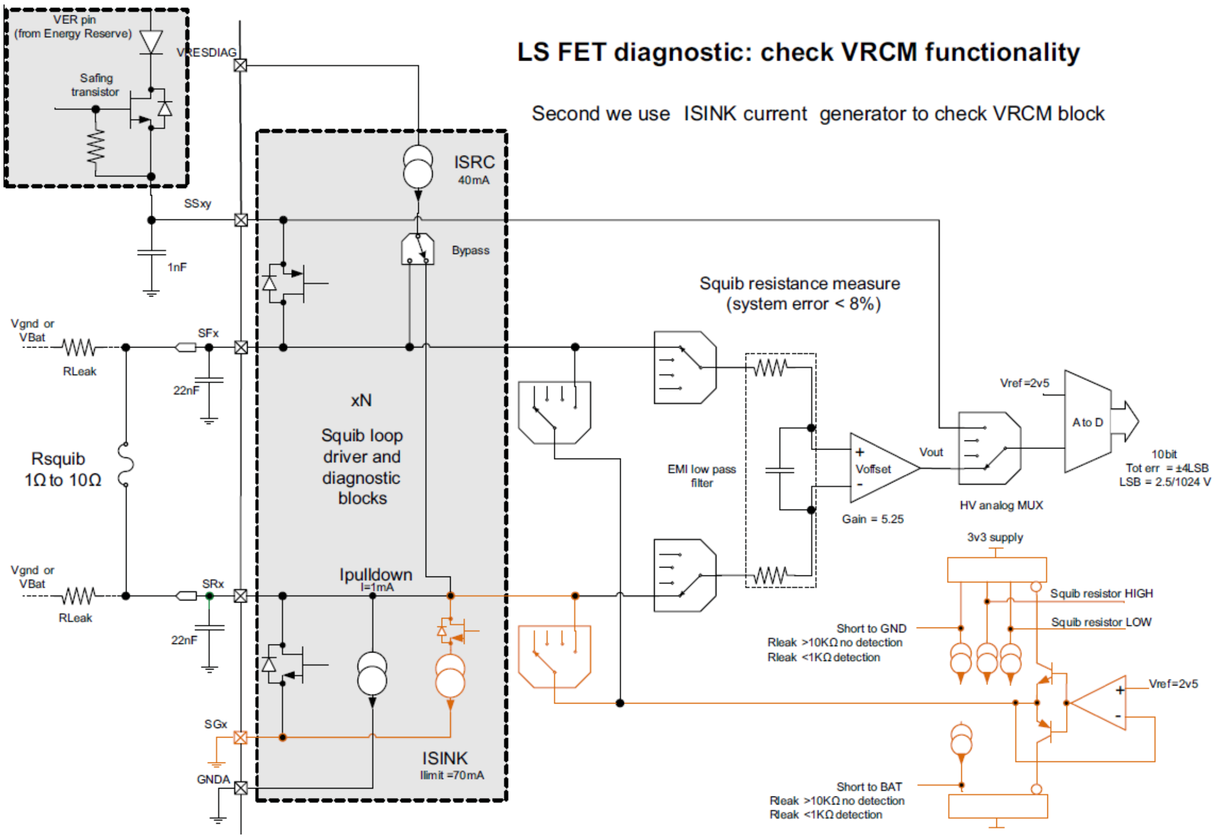
Figure 34. VRCM check - High Side waveform (Diagnostic)



VRCM check, once required, is not run one shot on both HS and LS, but the microcontroller selects through the SQP bit the High Side or the Low Side.

4.2.2 VRCM check - Low Side

Figure 35. VRCM check - Low Side (Diagnostic)



The correspondent set up (see the Figure 35) is done by setting the $38 LPDIAGREQ register properly (see the Table 51).

Table 51. VRCM check, Low Side - LPDIAGREQ register

	(1)	(2)	15	14:8	7:5	4	3:0	
$38 LPDIAGREQ	(I)	W	1	X	HIGH_LEVEL_DIAG_SEL 001 = VRCM Check	0	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 1 = high level diagnostic 4: 0 = leakage test on SRx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Being ISRC and VRCM connected to SFx, if VRCM works correctly, short to battery, readable in the $37 LPDIAGSTAT register, is asserted for the channel selected (see the Table 52).

Table 52. VRCM check, Low Side - LPDIAGSTAT register

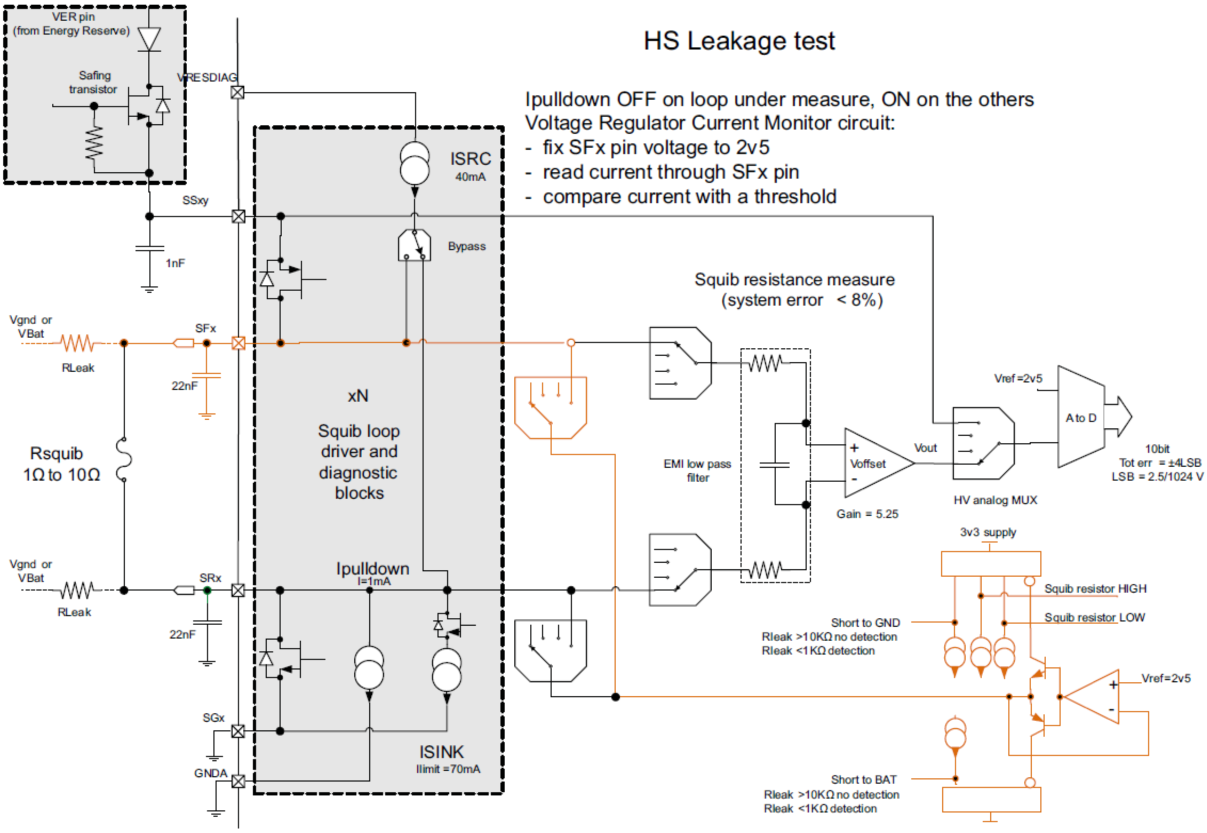
<table>
<tr><td colspan="5"></td><td>(1)</td><td>(2)</td><td>15:12</td><td>11:8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3:0</td><td></td></tr>
<tr><td colspan="5">$37 LPDIAGSTAT</td><td></td><td>R</td><td rowspan="3">X</td><td rowspan="3">HIGH_LEVEL_DIAG_SEL
0001 = VRCM Check</td><td rowspan="3">0</td><td rowspan="3">1</td><td rowspan="3">0</td><td rowspan="3">0</td><td rowspan="3">LOOP_DIAG_CHSEL
0000 = ch0
0001 = ch1
0010 = ch2
0011 = ch3
0100 = ch4
0101 = ch5
0110 = ch6
0111 = ch7
1000 = ch8
1001 = ch9
1010 = chA
1011 = chB
1100÷1111 = none</td><td rowspan="3">19: 1 = high level diagnostic
18: 1 = high level diag is running
7: 0 = no short between loops
6: 1 = STG detected
5: 0 = STB not detected
4: 0 = leakage test on SRx</td></tr>
<tr><td>(3)</td><td>19</td><td>18</td><td>17</td><td>16</td><td></td><td>R</td></tr>
<tr><td></td><td>1</td><td>0/1</td><td>0</td><td>0</td><td></td><td></td></tr>
</table>

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

VRCM check, once required, is not run one shot on both HS and LS, but the microcontroller selects through the SQP bit the High Side or the Low Side.

4.2.3 Leakage test - High Side

Figure 36. **Leakage test - High Side (Diagnostic)**



The correspondent set up (see the Figure 36) is done by setting the $38 LPDIAGREQ register properly (see the Table 53).

Table 53. Leakage test, High Side - LPDIAGREQ register

	(1)	(2)	15	14:8	7:5	4	3:0	
$38 LPDIAGREQ	(I)	W	1	X	HIGH_LEVEL_DIAG_SEL 010 = leakage test	1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 1 = high level diagnostic 4: 1 = leakage test on SFx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The result of the diagnostic is readable in the $37 LPDIAGSTAT register (see the Table 54):

Table 54. Leakage test, High Side - LPDIAGSTAT register

					(1)	(2)	15:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R	X	HIGH_LEVEL_DIAG_SEL 0010 = LEAKAGE Check	0	0	0	1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 1 = high level diagnostic 18: 1 = high level diag is running 16: 0 = no fault before test 15: 0 = FET off during diagnostic 7: 0 = no short between loops 6: 0 = STG not detected 5: 0 = STB not detected 4: 1 = leakage test on SFx
(3)	19	18	17	16		R								
	1	0/1	0	0										

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Depending on the value of the capacitors mounted on the ECU, the same high level diagnostic can be performed setting the HI_LEV_DIAG_TIME bit in order to increase the time of the internal diagnostic finite state machine operation (see the Figure 37 and Figure 38).

Figure 37. Leakage check - High Side waveform, short time (Diagnostic)

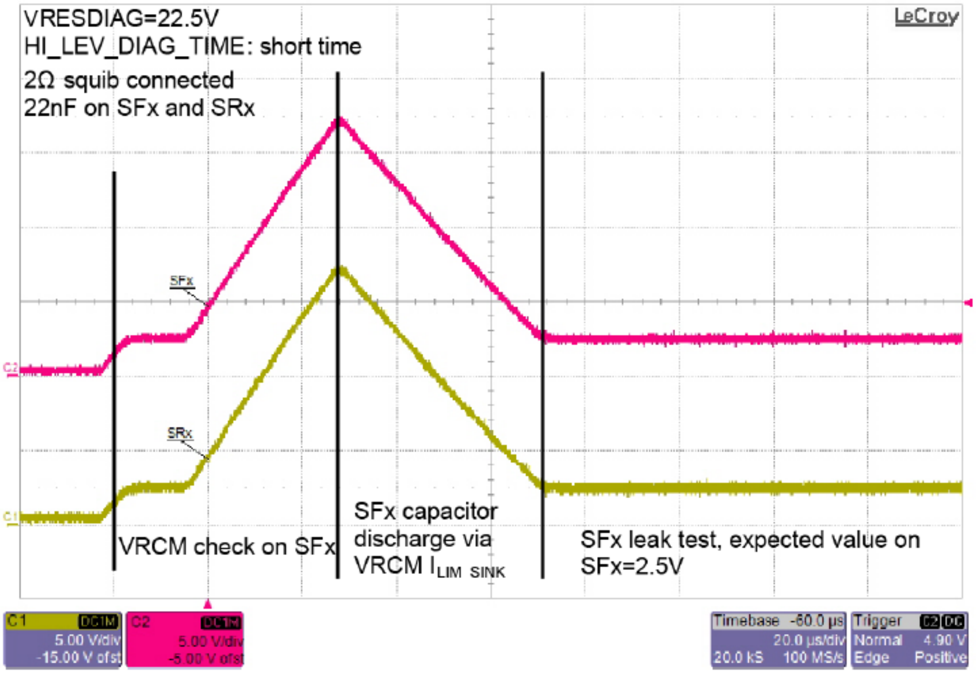
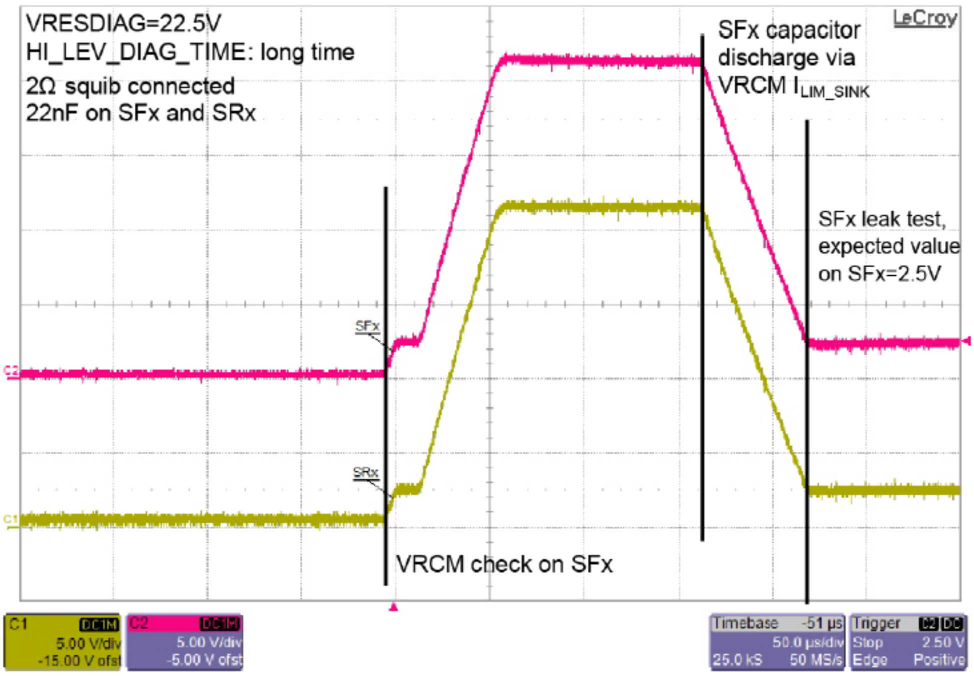


Figure 38. Leakage check - High Side waveform, long time (Diagnostic)



This bit can be written only in INIT state.

In case HI_LEV_DIAG_TIME has to be written, the microcontroller should do it before the RST activation after the initial 500 ms are expired.

This timeout could be disabled through bit WD1_TOVR in the $01 SYS_CFG register (see the Table 55).

Table 55. Leakage test, High Side - SYS_CFG register

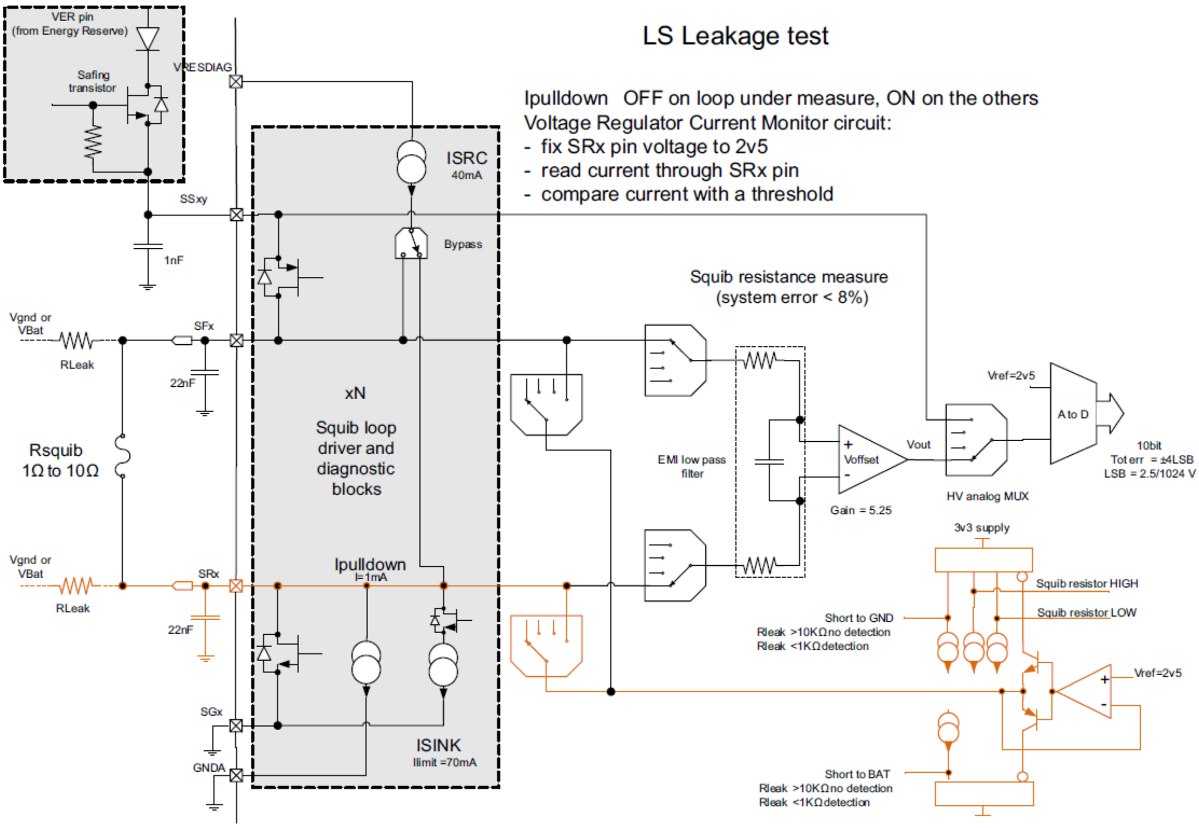
	(1)	(2)	15:13	12	11	10	9:1	0	
$01 SYS_CFG	I	W		X		1		1	10: HI_LEV_DIAG_TIME 0 = short time 1 = long time 0: WD1_TOVR 1 = timeout disabled

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Note: In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all the channels.

4.2.4 Leakage test - Low Side

Figure 39. Leakage test - Low Side (Diagnostic)



The correspondent set up (see the Figure 39) is done by setting the $38 LPDIAGREQ register properly (see the Table 56).

Table 56. **Leakage test, Low Side - LPDIAGREQ register**

	(1)	(2)	15	14:8	7:5	4	3:0	
$38 LPDIAGREQ	(I)	W	1	X	HIGH_LEVEL_DIAG_SEL 010 = leakage test	0	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 1 = high level diagnostic 4: 0 = leakage test on SRx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The result of the diagnostic is readable in the $37 LPDIAGSTAT register (see the Table 57).

Table 57. **Leakage test, Low Side - LPDIAGSTAT register**

					(1)	(2)	15:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R	X	HIGH_LEVEL_DIAG_SEL 0010 = leakage test	0	0	0	0	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 1 = high level diagnostic 18: 1 = high level diag is running 7: 0 = no short between loops 6: 0 = STG not detected 5: 0 = STB not detected 4: 0 = leakage test on SRx
(3)	19	18	17	16		R								
	1	0/1	0	0										

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Note: *In Pyro Fuse Application with channels shorted together, a leakage on a channel causes a fault on all the channels.*

4.2.5 Short between loops

The correspondent set up is done by setting the $38 LPDIAGREQ properly (see the Table 58).

Table 58. Short between loops - LPDIAGREQ register

	(1)	(2)	15	14:8	7:5	4	3:0	
$38 LPDIAGREQ	(I)	W	1	X	HIGH_LEVEL_DIAG_SEL 011 = short between loop	0/1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 1 = high level diagnostic 4: 0/1 = leakage test on SRx/SFx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The result of the diagnostic is readable in the $37 LPDIAGSTAT register (see the Table 59).

Table 59. Short between loops - LPDIAGSTAT register

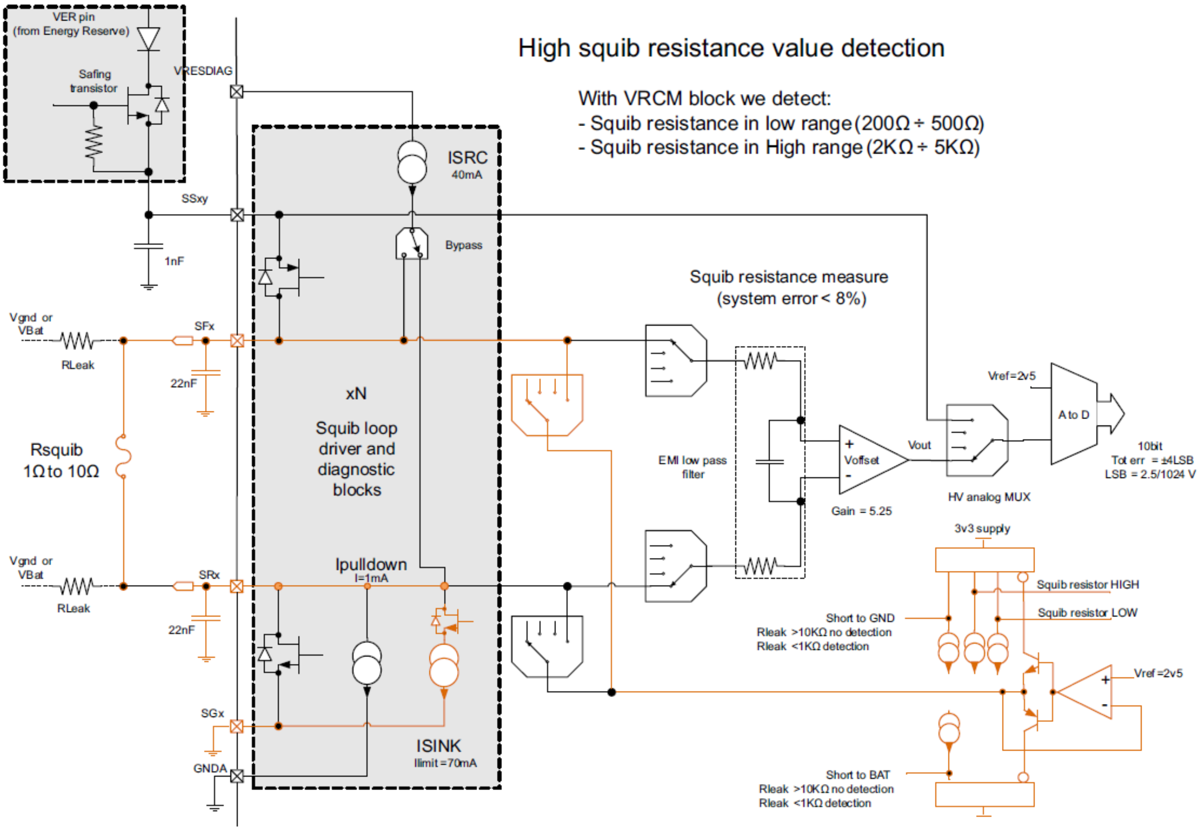
					(1)	(2)	15:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R								
(3)	19	18	17	16		R								
	1	0/1	0	0			X	HIGH_LEVEL_DIAG_SEL 0011 = short between loop	0	0	0	0/1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 1 = high level diagnostic 18: 1 = high level diag is running 7: 0 = no short between loops 6: 0 = STG not detected 5: 0 = STB not detected 4: 0/1 = leakage test on SRx/SFx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Note: In Pyro Fuse Application with channels shorted together, the short to ground should be a real short of SRx or SFx pin to GND. Moreover, a short to ground on a channel will be present on all the others.

4.2.6 Squib resistance range

Figure 40. Squib resistance range (Diagnostic)



The correspondent set up (see the Figure 40) is done by setting the $38 LPDIAGREQ register properly (see the Table 60).

Table 60. Squib resistance range - LPDIAGREQ register

	(1)	(2)	15	14:8	7:5	4	3:0	
$38 LPDIAGREQ	(I)	W	1	X	HIGH_LEVEL_DIAG_SEL 101 = squib res range	1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 1 = high level diagnostic 4: 1 = leakage test on SFx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The result of the diagnostic in case of **2 Ω squib** is readable in the $37 LPDIAGSTAT register (see the Table 61).

Table 61. Squib resistance range - LPDIAGSTAT register

					(1)	(2)	15	14	13	12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R											
(3)	19	18	17	16		R											
	1	0/1	0	0			0	X	0	1	HIGH_LEVEL_DIAG_SEL 0101 = squib res range check	0	1	0	1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 1 = high level diagnostic 18: 0 = high level diag not running 13: 0 = res meas < HSR high 12: 1 = res meas < HSR low 7: 0 = no short between loops 6: 1 = STG detected 5: 0 = STB not detected 4: 1 = leakage test on SFx

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

The results could be the following:

- STG = 1 → the squib has a very low resistive value.
- SQP = 1 → VRCM is connected to the High Side.

Note: In Pyro Fuse Application with channels shorted together, the high squib resistance measurement should be the same on all the channels.

4.2.7 Squib resistance measurement

The IC allows measuring the squib resistance value in the range of 1 ÷ 10 Ω with overall 8% precision.

Two steps of the measurement, described in the Figure 41 and Figure 42, are managed by the IC, which also makes ADC conversion results available.

Note: In Pyro Fuse Application with channels shorted together, the squib resistance measurement should be the same on all the channels.

Figure 41. Squib resistance measurement - First step (Diagnostic)

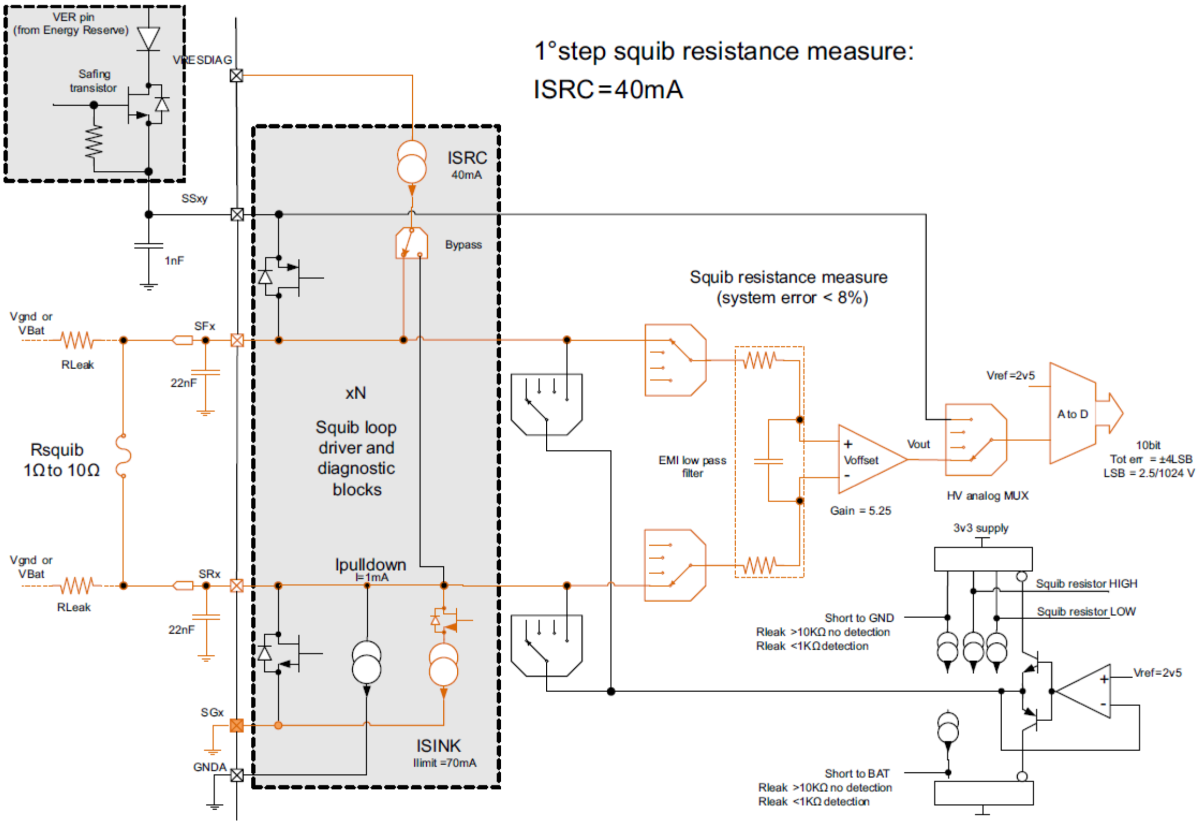
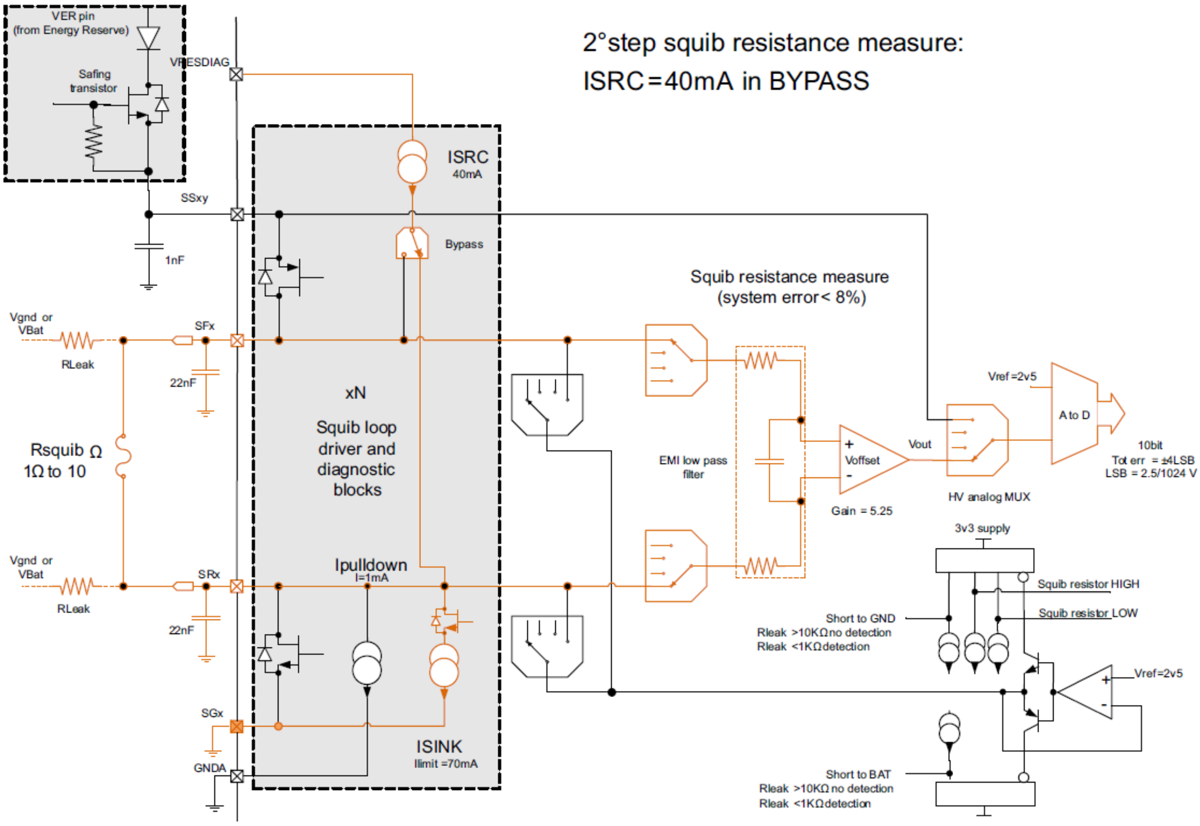


Figure 42. Squib resistance measurement - Second step (Diagnostic)



The correspondent set up is done by setting the $38 LPDIAGREQ properly (see the Table 62):

Table 62. Squib resistance measurement - LPDIAGREQ register

	(1)	(2)	15	14:8	7:5	4	3:0	
$38 LPDIAGREQ	(I)	W	1	X	HIGH_LEVEL_DIAG_SEL 110 = squib res meas	X	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	15: 1 = high level diagnostic

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The IC triggers at the end of each step above an ADC conversion. Once the high level diagnostic has been performed, results of ADC conversions have to be read in the registers $3C, $3D DIAGCTRL_x by selection of SQUIB resistance measurement (bit [6:0] = $06).

The result of the first conversion, $ADC_{1ST\ CONVERSION}$, is stored in $3C DIAGCTRL_C. Instead, the result of the second conversion, $ADC_{2ND\ CONVERSION}$, is stored in $3D DIAGCTRL_D.

Once read the ADC measurement, to obtain the value it is necessary to consider the divider ratio of the ADC. In case of resistance x, it is 1:1.

Being two measurements, the squib resistance is so calculated:

$$\Delta V_{OUT} = (SFx - SRx)_1 - (SFx - SRx)_2 \tag{10}$$

$$R_{SQUIB} = \frac{\Delta V_{OUT}}{G * ISRC} \tag{11}$$

With:

- G = 5.25 ± 2% (differential amplifier gain)
- ISRC = 40 mA ± 5%

Example:

- $ADC_{1ST\ CONVERSION}$ = 0b0100111000 = 312
- $ADC_{2ND\ CONVERSION}$ = 0b0010000001 = 129
- Δ_{ADC} = 312 - 129 = 183

In order to obtain the result in Volt, being the ADC characteristic linear:

$$2.5\,V : 1024 = x : \Delta_{ADC} \rightarrow x = \frac{183 * 2.5\,V}{1024} = 0.44\,V \tag{12}$$

In order to obtain resistance value, considering typical factors:

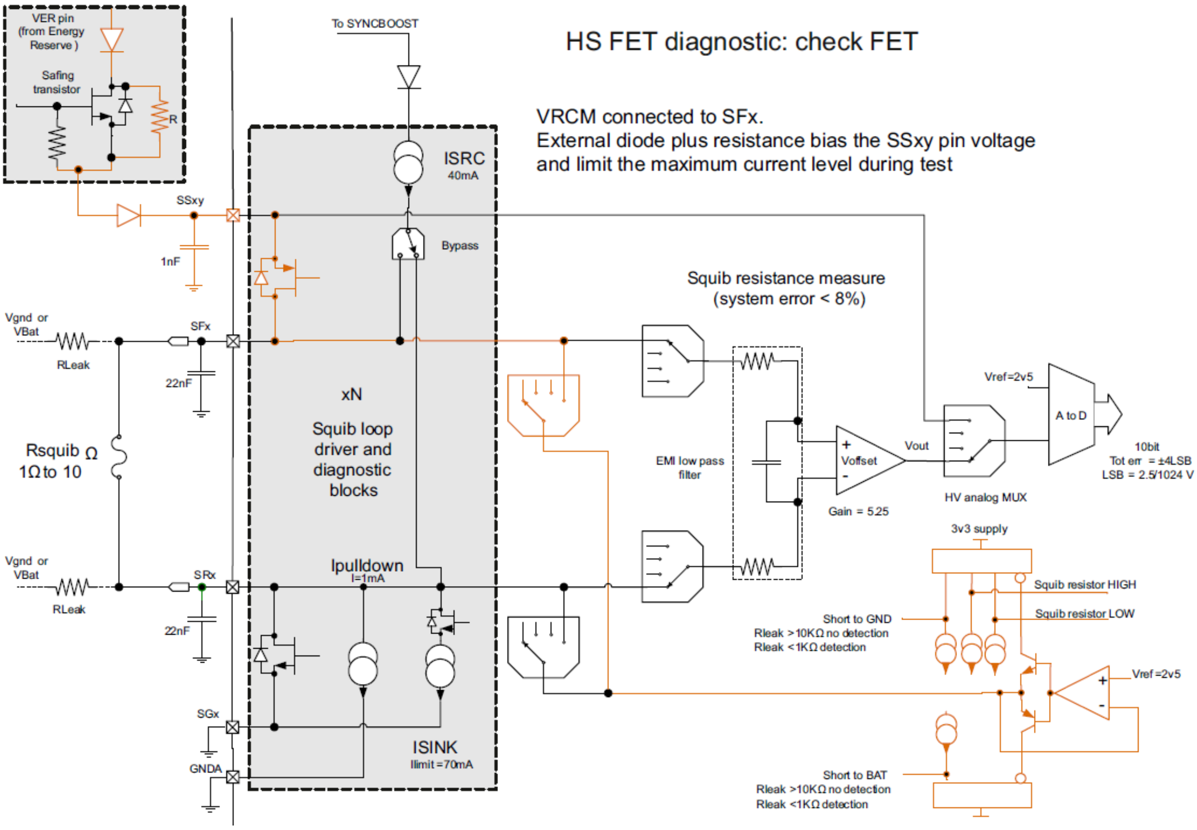
$$R_{SQUIB} = \frac{x}{G * ISRC} = \frac{0.44\,V}{5.25 * 40\,mA} = 2.1\,\Omega \tag{13}$$

4.2.8 High Side FET diagnostic

The test is possible only in the diagnostic phase.

Before running this test, the IC validates VRCM, then performs leakage test and in case of no failures, High Side FET test is performed.

Figure 43. High Side FET test (Diagnostic)



The correspondent set up (see the Figure 43) is done by setting the $38 LPDIAGREQ and $36 SYSDIAGREQ registers (see the Table 63).

Table 63. High Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers

	(1)	(2)	15	14:8	7:5	4	3:0				
$38 LPDIAGREQ	(I)	W	1	X	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	SQP 1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none				15: 1 = high level diagnostic 4: 1 = leakage test on SFx
$36 SYSDIAGREQ	D	W	X	X			0	1	1	1	DSTEST: 0111 = HS FET test active

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

The High Side FET test turns ON the HS power: if it turns ON correctly, SFx is connected to SSxy which is at VER voltage through the resistor R in parallel to the safing FET.

During the test, the device monitors the current flowing through VRCM.

If the High Side FET works properly, this current exceeds the thresholds I_{HSFET}, that is 1.8 mA ± 10%, and the channel is immediately turned off.

In case the current does not exceed the limit mentioned, after the time $T_{FETTIMEOUT}$, that is 200 µs, the test is terminated, and the output is turned off.

The result of the diagnostic is readable in the $37 LPDIAGSTAT register (see the Table 64. High Side FET diagnostic - LPDIAGSTAT register):

Table 64. High Side FET diagnostic - LPDIAGSTAT register

					(1)	(2)	15	14:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R	0/1	X	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	0	0	1	1	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 1 = high level diagnostic 18: 1 = high level diag is running 15: 1 = FET on during diagnostic 7: 0 = no short between loops 6: 0 = STG not detected 5: 1 = STB detected 4: 1 = leakage test on SFx
(3)	19	18	17	16		R									
	1	0/1	0	0											

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Possible results for High Side FET test are:

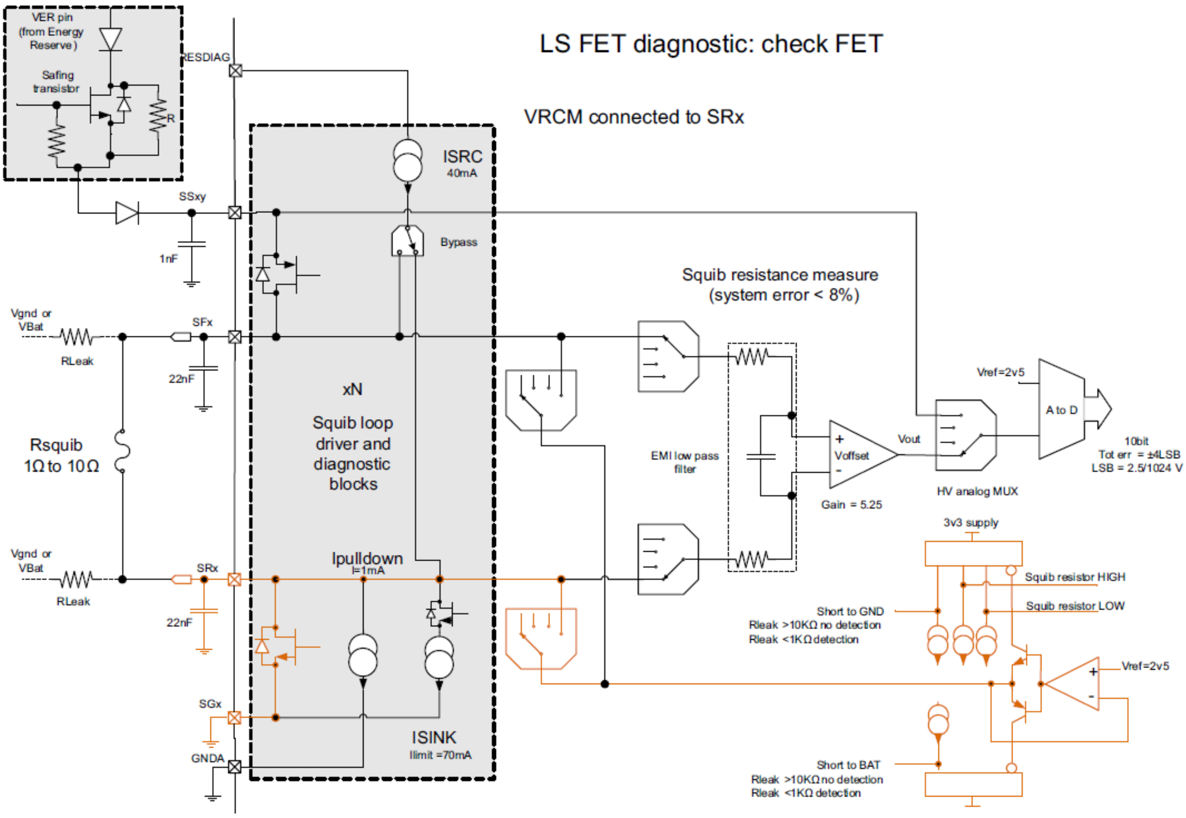
- STB = 1 and STG = 0 → ok.
- STB = 0 or STG = 1 → missing SSxy connection during FET test, or High Side not switched ON, or short to GND during FET test.

STG and STB, after FET test, are latched. They are cleared through a new LPDIAGREQ or a new SYSDIAGREQ.

4.2.9 Low Side FET diagnostic

Before running this test, IC validates VRCM, then performs leakage test and in case of no failures, Low Side FET test is performed.

Figure 44. Low Side FET test (Diagnostic)



The correspondent set up (see the Figure 44) is done by setting the $38 LPDIAGREQ and $36 SYSDIAGREQ registers (see the Table 65).

Table 65. Low Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers

	(1)	(2)	15	14:8	7:5	4	3:0				
$38 LPDIAGREQ	(I)	W	1	X	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	SQP 0	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none				15: 1 = high level diagnostic 4: 0 = leakage test on SRx
$36 SYSDIAGREQ	D	W	X	X			1	0	0	0	DSTEST: 1000 = LS FET test active

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*

Low Side FET test turns ON the Low Side. If the Low Side turns ON correctly, SRx is connected to SGxy.

During the test, the device monitors the current flowing through VRCM.

If the FET works properly, this current exceeds the thresholds I_{LSFET}, that is 450 µA ± 10%, and the channel is immediately turned off.

In case the current doesn't exceed the limit mentioned, after the time $T_{FETTIMEOUT}$, that is 200 µs, the test is terminated, and the output is turned off.

The result of the diagnostic is readable in the $37 LPDIAGSTAT register (see the Table 66).

Table 66. Low Side FET diagnostic - LPDIAGSTAT register

					(1)	(2)	15	14:12	11:8	7	6	5	4	3:0	
$37 LPDIAGSTAT						R	0/1	X	RES_MEAS_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	0	1	0	0	LOOP_DIAG_CHSEL 0000 = ch0 0001 = ch1 0010 = ch2 0011 = ch3 0100 = ch4 0101 = ch5 0110 = ch6 0111 = ch7 1000 = ch8 1001 = ch9 1010 = chA 1011 = chB 1100÷1111 = none	19: 1 = high level diagnostic 18: 1 = high level diag is running 15: 1 = FET on during diagnostic 7: 0 = no short between loops 6: 1 = STG detected 5: 0 = STB not detected 4: 0 = leakage test on SRx
(3)	19	18	17	16		R									
	1	0/1	0	0											

1. *I = INIT, D = DIAG, S = SAFING, C = SCRAP, A = ARMING, - = ALL STATES, (I) = no in INIT, (D) = no in DIAG, (S) = no in SAFING, (C) = no in SCRAP, (A) = no in ARMING*
2. *R = READ, W = WRITE*
3. *Further bit over the 16 standard.*

Possible results for Low Side FET test are:

- STB = 0 and STG = 1 → ok
- STB = 1 or STG = 0 → short to battery in Low Side, or Low Side not switched ON.

STG & STB, after FET test, are latched. They are cleared through a new LPDIAGREQ or a new SYSDIAGREQ.

5 Optimized application circuit

In the scenario of only one channel deployment (see the Figure 45), the application can be further simplified by:

- Removing the Energy Reserve capacitor.
- Removing the ERBOOST components (inductor, diode and capacitor). The ERBOOST regulator should be disabled by SPI setting to 0 the ER_BST_EN bit in the SYS_CTL register.
- Removing the External Safing FET.
- Connecting the SSxy directly to battery.
- Not using GPO drivers.
- Not using DC Sensor interface.
- Not using Remote Sensor interface.

In this case there is a consistent reduction in BOM cost (see the Table 67), paying a loss in Safety level.

Figure 45. Optimized application circuit

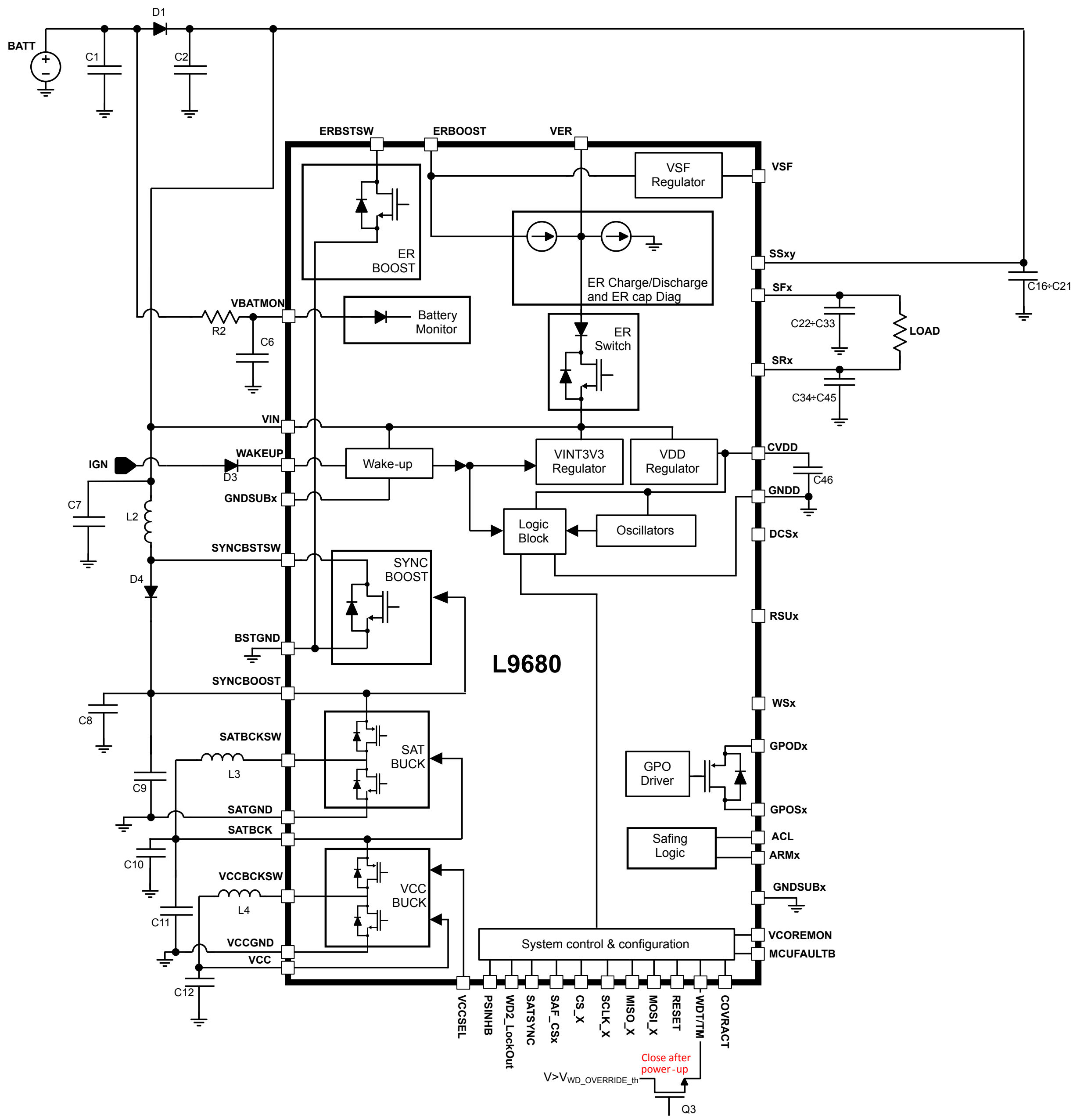


Table 67. **Simplified BOM**

Component	Typ	Unit	Requirement	Notes
C1	100	nF	50 V	Input capacitor (unprotected battery)
C2	2.2	μF	50 V	Input capacitor (protected battery)
C6	10	nF	25 V	VBATMON capacitor
C7	100	nF	50 V	SYNC Boost input capacitor
C8	47	μF	35 V	SYNC Boost output capacitor
C9	100	nF	50 V	SAT Buck input capacitor
C10	47	μF	35 V	SAT Buck output capacitor
C11	100	nF	50 V	VCC Buck input capacitor
C12	47	μF	16 V	VCC Buck output capacitor
C16 ÷ C21	10	nF	25 V	SSxy capacitor
C22 ÷ C33	22	nF	25 V	SFx capacitor
C34 ÷ C45	22	nF	25 V	SRx capacitor
C46	100	nF	50 V	CVDD output capacitor
D1	2	A	-	Reverse battery protection
D3	1	A	-	WAKEUP diode
D4	1	A	-	SYNC Boost diode
L2	4.7	μH	1 A	SYNC Boost inductor
L3	4.7	μH	1 A	SAT Buck inductor
L4	4.7	μH	1 A	VCC Buck inductor
R2	1	kΩ	100 mW	VBATMON current limit resistor
Q3	-	-	-	WDT/TM switch, see Section 3.3.1

Revision history

Table 68. Document revision history

Date	Version	Changes
10-Dec-2021	1	Initial release.
07-Jun-2022	2	Updated: • *Figure 1. Pyro Fuse application circuit*; • *Figure 45. Optimized application circuit*.
02-May-2023	3	Updated: • *Section 3.3.1: With Watchdog Service routine disabled*; • *Figure 7. Watchdog override signal*; • *Section 4.1.12: Safing FET diagnostic*.
21-May-2024	4	Updated: • Figure 1. Pyro Fuse application circuit; • Figure 32. High level loop diagnostic flow 2; • Figure 45. Optimized application circuit. Minor text changes in: • Table 1. Unused functions management; • Table 16. Deployment SPI sequence with Watchdog routine; • Section 4.2.3: Leakage test - High Side; • Table 67. Simplified BOM.
22-Jul-2025	5	Figure 1, Figure 7, Figure 45 and Table 67 updated.

Contents

1 Description 2
1.1 Main features 2
1.2 Application overview 3
2 Device configuration 4
2.1 Unused functions 4
3 Deployment 5
3.1 Deployment requirement 5
3.1.1 Diagnostic state 7
3.1.2 SAFING and SCRAP states 8
3.1.3 Deployment driver 9
3.2 Deployment driver protection 13
3.3 Deployment driver examples 13
3.3.1 With Watchdog Service routine disabled 13
3.3.2 With Watchdog Service routine enabled 17
3.3.3 Deployment waveforms 19
3.4 Arming command after deployment command 20
4 Diagnostic 21
4.1 Low level diagnostic 22
4.1.1 High voltage leak test, oxide isolation IC-car chassis 23
4.1.2 VRCM test validation 26
4.1.3 Leakage test - High Side 30
4.1.4 Leakage test - Low Side 34
4.1.5 Leakage test - Low Side pulldown current 38
4.1.6 Short between loops 40
4.1.7 Squib resistance measurements 42
4.1.8 High squib resistance diagnostic 48
4.1.9 High Side FET diagnostic 51
4.1.10 Low Side FET diagnostic 54
4.1.11 Loss of ground 57
4.1.12 Safing FET diagnostic 57
4.1.13 Deployment time diagnostic 60
4.2 High level diagnostic 64
4.2.1 VRCM check - High Side 68
4.2.2 VRCM check - Low Side 70
4.2.3 Leakage test - High Side 72

4.2.4 Leakage test - Low Side 75
4.2.5 Short between loops 77
4.2.6 Squib resistance range 78
4.2.7 Squib resistance measurement 80
4.2.8 High Side FET diagnostic 83
4.2.9 Low Side FET diagnostic 86

5 Optimized application circuit. 89

Revision history 91

List of tables

Table 1. Unused functions management 4
Table 2. DCR_x register 5
Table 3. DSR_x register 6
Table 4. LPDIAGREQ register - LEAK_CHSEL bits 7
Table 5. SYSDIAGREQ register - DSTEST bits 7
Table 6. SYS_CSF register - SAFESEL bit 8
Table 7. DCR_x register 8
Table 8. SPI commands to pass in SAFING state or SCRAP state 9
Table 9. ARM_STATE register 10
Table 10. SPIDEPEN register 10
Table 11. DEPCOM register – CHxDEPREG bit 10
Table 12. DCMTSxy register 11
Table 13. Global Status Word (GSW) 12
Table 14. DEPOK bit in GSW 12
Table 15. Deployment SPI sequence without Watchdog routine 14
Table 16. Deployment SPI sequence with Watchdog routine 17
Table 17. Deploy event with Arming command after SPI deployment command 20
Table 18. Low level diagnostic 22
Table 19. High voltage leak test, oxide isolation IC-car chassis - LPDIAGREQ register 24
Table 20. High voltage leak test, oxide isolation IC-car chassis - DIAGCTRL_X registers 25
Table 21. VRCM test validation (first step) - LPDIAGREQ register 27
Table 22. VRCM test validation (first step) - LPDIAGSTAT register 27
Table 23. VRCM test validation (second step) - LPDIAGREQ register 29
Table 24. VRCM test validation (second step) - LPDIAGSTAT register 29
Table 25. Leakage test, High Side - LPDIAGREQ register 31
Table 26. Leakage test, High Side - DIAGCTRL_X register 32
Table 27. Leakage test, High Side - LPDIAGSTAT register 33
Table 28. Leakage test, Low Side - LPDIAGREQ register 35
Table 29. Leakage test, Low Side - DIAGCTRL_X register 36
Table 30. Leakage test, Low Side - LPDIAGSTAT register 37
Table 31. Leakage test, Low Side pulldown current - LPDIAGREQ register 39
Table 32. Leakage test, Low Side pulldown current - LPDIAGSTAT register 39
Table 33. Short between loops - LPDIAGREQ register 40
Table 34. Squib resistance measurements (first step) - LPDIAGREQ register 44
Table 35. Squib resistance measurements (first step) - DIAGCTRL_X register 44
Table 36. Squib resistance measurements (second step) - LPDIAGREQ register 46
Table 37. Squib resistance measurements (second step) - LPDIAGSTAT register 47
Table 38. High squib resistance diagnostic - LPDIAGREQ register 49
Table 39. High squib resistance diagnostic - LPDIAGSTAT register 50
Table 40. High Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers 52
Table 41. High Side FET diagnostic - LPDIAGSTAT register 53
Table 42. Low Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers 55
Table 43. Low Side FET diagnostic - LPDIAGSTAT register 56
Table 44. Loss of ground - LP_GNDLOSS register 57
Table 45. Safing FET diagnostic - SYSDIAGREQ register 57
Table 46. Safing FET diagnostic - DIAGCTRL_X register 58
Table 47. Deployment time diagnostic - SYSDIAGREQ register 60
Table 48. High level diagnostic 64
Table 49. VRCM check, High Side - LPDIAGREQ register 68
Table 50. VRCM check, High Side - LPDIAGSTAT register 69
Table 51. VRCM check, Low Side - LPDIAGREQ register 71
Table 52. VRCM check, Low Side - LPDIAGSTAT register 71
Table 53. Leakage test, High Side - LPDIAGREQ register 73

Table 54. Leakage test, High Side - LPDIAGSTAT register . . . 73
Table 55. Leakage test, High Side - SYS_CFG register . . . 75
Table 56. Leakage test, Low Side - LPDIAGREQ register . . . 76
Table 57. Leakage test, Low Side - LPDIAGSTAT register . . . 76
Table 58. Short between loops - LPDIAGREQ register . . . 77
Table 59. Short between loops - LPDIAGSTAT register . . . 77
Table 60. Squib resistance range - LPDIAGREQ register . . . 79
Table 61. Squib resistance range - LPDIAGSTAT register . . . 79
Table 62. Squib resistance measurement - LPDIAGREQ register . . . 81
Table 63. High Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers . . . 84
Table 64. High Side FET diagnostic - LPDIAGSTAT register . . . 85
Table 65. Low Side FET diagnostic - LPDIAGREQ and SYSDIAGREQ registers . . . 87
Table 66. Low Side FET diagnostic - LPDIAGSTAT register . . . 88
Table 67. Simplified BOM . . . 90
Table 68. Document revision history . . . 91

List of figures

Figure 1. Pyro Fuse application circuit . . . 3
Figure 2. System operating state diagram . . . 6
Figure 3. High Side and Low Side squib enable . . . 7
Figure 4. Deployment driver control logic . . . 9
Figure 5. Deployment Enable/Disable . . . 11
Figure 6. Current measurement during deploy . . . 12
Figure 7. Watchdog override signal . . . 14
Figure 8. Deployment waveforms, VER = 33 V . . . 19
Figure 9. Deployment waveforms, VER = 24 V . . . 19
Figure 10. Deploy event with Arming command after SPI deployment command . . . 20
Figure 11. Squib diagnostic blocks . . . 21
Figure 12. High voltage leak test, oxide isolation IC-car chassis . . . 23
Figure 13. VRCM test validation - First step . . . 26
Figure 14. VRCM test validation - Second step . . . 28
Figure 15. Leakage test - High Side . . . 30
Figure 16. Leakage test - Low Side . . . 34
Figure 17. Low Side pulldown current - Leakage test . . . 38
Figure 18. High Side short to ground . . . 41
Figure 19. Low Side short to ground . . . 42
Figure 20. Squib resistance measurements - First step . . . 43
Figure 21. Squib resistance measurements - Second step . . . 45
Figure 22. High squib resistance diagnostic . . . 48
Figure 23. High Side FET diagnostic . . . 51
Figure 24. Low Side FET diagnostic . . . 54
Figure 25. Safing FET diagnostic . . . 59
Figure 26. Safing FET diagnostic - Test cases . . . 59
Figure 27. Deployment time diagnostic sequence . . . 61
Figure 28. Deployment time - No configuration . . . 62
Figure 29. Deployment Time . . . 63
Figure 30. High level diagnostic flow . . . 65
Figure 31. High level loop diagnostic flow 1 . . . 66
Figure 32. High level loop diagnostic flow 2 . . . 67
Figure 33. VRCM check - High Side (Diagnostic) . . . 68
Figure 34. VRCM check - High Side waveform (Diagnostic) . . . 69
Figure 35. VRCM check - Low Side (Diagnostic) . . . 70
Figure 36. Leakage test - High Side (Diagnostic) . . . 72
Figure 37. Leakage check - High Side waveform, short time (Diagnostic) . . . 74
Figure 38. Leakage check - High Side waveform, long time (Diagnostic) . . . 74
Figure 39. Leakage test - Low Side (Diagnostic) . . . 75
Figure 40. Squib resistance range (Diagnostic) . . . 78
Figure 41. Squib resistance measurement - First step (Diagnostic) . . . 80
Figure 42. Squib resistance measurement - Second step (Diagnostic) . . . 81
Figure 43. High Side FET test (Diagnostic) . . . 83
Figure 44. Low Side FET test (Diagnostic) . . . 86
Figure 45. Optimized application circuit . . . 89