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Application note

Migrating within STM32U5 series microcontrollers

Introduction

The ability to replace easily one microcontroller type with another from the same product series is an important asset for designers of STM32 microcontroller applications.

Migrating an application to a different microcontroller is often needed when product requirements grow. This places extra demands on new features, memory size, or increases the number of I/Os. Cost reduction objectives may be also a reason to switch to smaller components, and shrink the PCB area.

This application note analyzes the steps required to migrate an existing design between STM32U5 series microcontrollers.

The hardware and peripherals are the main aspects to be considered for the migration.

This document lists the full set of features available for STM32U5 series devices.

To benefit from this application note, the user should be familiar with the STM32 microcontroller documentation available on www.st.com.

1 General information

This application note applies to the STM32U5 series microcontrollers that are Arm®Cortex® core-based devices.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Reference documents

[1] Reference manual *STM32U5 series Arm®-based 32-bit MCUs* (RM0456)

[2] STM32U5 series datasheets and errata sheets

[3] Application note *Getting started with STM32U5 series MCU hardware development* (AN5373)

2 Hardware migration guide

To understand the migration within the STM32U5 series on the hardware part, refer to document [3].

Document [3] is intended for system designers who require a hardware implementation overview of the development board features, such as: power supply, package differences, clock management, reset control, boot mode settings, and debug management.

Document [3] details how to migrate within the STM32U5 series microcontrollers and describes the minimum hardware resources required to develop an application using these microcontrollers. Detailed reference design schematics are also contained in this document with descriptions of main components, interfaces, and modes.

3 Peripheral migration guide

3.1 STM32 product cross-compatibility

STM32 microcontrollers embed a set of peripherals, which can be classified in three groups:

- Peripherals that are common and identical to all products. Those peripherals have the same structure, registers, and controls bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- Peripherals that are shared by all products but have only minor differences (in general to support new features). Therefore, migrating from one product to another is easy and does not need any significant new development effort.
- Peripherals that have considerable changes from one product to another (new architecture or new features). The migration for this group of peripherals requires a new development at application level.

The table below summarizes the available peripherals in STM32U5 series microcontrollers as well as their compatibility.

Table 1. Peripheral compatibility analysis within STM32U5 series microcontrollers

Peripherals		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx	Compatibility	
						Software	Comments
Flash memory(1)	Size (bytes)	Up to 512K	Up to 2M	Up to 4M		Yes	-
	Bank	Dual				Yes	-
SRAM (Kbytes)(2)	SRAM1	192		768		Yes	The SRAM2 and SRAM3 are contiguous to the SRAM1 and the physical address remains 0x2000000 in STM32U5 series.
	SRAM2	64				Yes	
	SRAM3	N/A	512	832		Yes	
	SRAM4	16				Yes	Used for low-power background-autonomous mode in Stop 2 mode.
	SRAM5	N/A		832		Yes	New on STM32U59x/5Ax/5Fx/5Gx.
	SRAM6	N/A			512	Yes	Only on STM32U5Fx/5Gx.
	BKPSRAM	2				Yes	-
GTZC	Number of instances	2				Yes	-
	MPCWM resources	2	5	6		Mostly	New feature for HSPI on STM32U59x/5Ax/5Fx/5Gx.
	MPCBB resources	3	4	5	6	Mostly	New feature for SRAM5 and SRAM6 on STM32U59x/5Ax/5Fx/5Gx.
ICACHE	Size (Kbytes)	8		32		Yes	Same features
DCACHE (Kbytes)(3)	DCACHE1	4		16		Yes	Same features
	DCACHE2	N/A		16		No	New only on STM32U599/5A9/5Fx/5Gx for GPU2D.
PWR(4)		Yes				Yes	Additional supplies (V_{DDDSI}, $V_{DD11DSI}$, $V_{DD11USB}$) for STM32U59x/5Ax/5Fx/5Gx.

Peripherals	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx	Compatibility	
					Software	Comments
RCC[5]	Yes				Yes	New features on STM32U59x/5Ax/5Fx/5Gx: new HSPI1 kernel clock to manage the HSPI peripheral, new OTG_HS kernel clock to manage the USB High Speed. New features only on STM32U599/5A9/5Fx/5Gx: new clock for DSI and LTDC interfaces. Bits only on STM32U59x/5Ax/5Fx/5Gx: for the GPU2D, GFXMMU, GPIOJ, HSPI, USART6, I2C6, I2C5, DSI, LTDC, DCACHE2, and SRAM5. Bits only on STM32U5Fx/5Gx: for the JPEG, GFXTIM, and SRAM6.
CRS	Yes				Yes	Only an external HSE is used as input for the USB peripheral on STM32U59x/5Ax/5Fx/5Gx.
GPIOs number LPGPIOs number Wake-up pins I/Os down to 1.08 V	Up to 82 Up to 16 Up to 23 Up to 14	Up to 136 Up to 16 Up to 24 Up to 14	Up to 151 Up to 16 Up to 24 Up to 14	Up to 151 Up to 16 Up to 24 Up to 14	Yes	Additional I/Os port J on STM32U59x/5Ax/5Fx/5Gx.
SYSCFG[6]	Yes				Yes	New features for USB HS PHY and HSPI on STM32U59x/5Ax/5Fx/5Gx.
GPDMA[7]	Yes				Yes	New triggers and requests on STM32U59x/5Ax/5Fx/5Gx.
LPDMA	Yes				Yes	Same features
DMA2D	Yes				Yes	New triggers interconnection on STM32U59x/5Ax/5Fx/5Gx.
GFXMMU[8]	N/A		Up to 1		No	New peripheral on STM32U599/5A9/5Fx/5Gx.
GFXTIM[9]	N/A			Yes	No	New peripheral onSTM32U5Fx/5Gx.
NVIC (number)[10]	Up to 130 interrupts	Up to 141 interrupts	Up to 154 interrupts		Yes	New features on STM32U59x/5Ax/5Fx/5Gx.
EXTI	Yes				Yes	-
CRC	Yes				Yes	-
CORDIC	Yes				Yes	-
FMAC	Yes				Yes	-
FSMC	N/A	Yes			Yes	Same features[11]
OCTOSPI	1	2			Yes	Same features
OCTOSPIM	N/A	Yes			Yes	Same features
HSPI[12]	N/A		Up to 1		No	New peripheral on STM32U599/5A9/5Fx/5Gx[11].
Communication interfaces SAI	1	2			Yes	-[11]

Peripherals		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx	Compatibility	
						Software	Comments
Communication interfaces	I2C	4		6		Yes	New I2C5 and I2C6 on STM32U59x/5Ax/5Fx/5Gx[11].
	USART/UART	4	5	6		Yes	New USART6 on STM32U59x/5Ax/5Fx/5Gx.
	LPUART	1				Yes	-
	SPI	3				Yes	-
	FDCAN	1				Yes	-
	SDMMC	1	2			Yes	-
	MDF	1				Yes	Additional features for ADC2 on STM32U59x/5Ax/5Fx/5Gx.
	ADF	1				Yes	Additional features for ADC2 on STM32U59x/5Ax/5Fx/5Gx.
	DCMI	Yes				Yes	-[11]
	PSSI	Yes				Yes	-[11]
	USB[13]	FS with clock recovery system	OTG FS with clock recovery	OTG HS with embedded PHY clock		No	-
	USB Type-C®	N/A	Yes			Yes	-
DLYB		Yes				Yes	Same features
14-bit ADC	Instance	1		2		Yes	New ADC2 on STM32U59x/5Ax/5Fx/5Gx.
	Number of channels	Up to 20				Yes	-
12-bit ADC	Instance	1				Yes	-
	Number of channels	Up to 21	Up to 25			Yes	-
12-bit DAC		2				Yes	-
Internal voltage reference buffer		1				Yes	-
VREFBUF		1				Yes	-
Ultra-low-power comparator (COMP)		1	2			Yes	-
Operational amplifier (OPAMP)		1	2			Yes	-
LTDC[14]		N/A		Yes		No	New peripheral only for STM32U599/5A9/5Fx/5Gx[11].
DSI[15]		N/A		Yes		No	New peripheral only for STM32U599/5A9/5F9/5G9[11].
GPU2D[16]		N/A		Yes		No	New peripheral only for STM32U599/5A9/5Fx/5Gx. Vector graphics feature only available on STM32U5Fx/5Gx.
JPEG[17]		N/A			Yes	No	New peripheral onSTM32U5Fx/5Gx.
TSC		Yes				Yes	-

Peripherals		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx	Compatibility	
						Software	Comments
Number of capacitive sensing pins		Up to 20	Up to 24			Yes	-
Random generator (RNG)		Yes				Yes	-
AES		Yes				Yes	Feature only on STM32U545/585/5Ax/5Gx.
SAES		Yes				Yes	Feature only on STM32U545/585/5Ax/5Gx.
HASH		Yes				Yes	-
OTFDEC		Yes				Yes	Feature only on STM32U545/585/5Ax/5Gx.
PKA		Yes				Yes	Feature only on STM32U545/585/5Ax/5Gx.
Timers	Advanced control	2 (16 bits)				Mostly	New external trigger signals for ADC2.
	General purpose	3 (16bits) 4 (32 bits)				Mostly	New external trigger signals for DCMI and LTDC. Same features.
	Basic	2 (16 bits)				Yes	-
	Low power (LPTIM)	4 (16 bits)				Yes	-
	SysTick	2				Yes	-
	Infrared (IRTIM)	2				Yes	-
	Independent watchdog (IWDG)	1				Yes	-
	System window watchdog (WWDG)	1				Yes	-
RTC		Yes				Yes	-
Tamper	External pins	Up to 8				Yes	-
	Internal events	11				Yes	-

1. *Refer to Section 3.3 for more details.*
2. *Refer to Section 3.4 for more details.*
3. *Refer to Section 3.5 for more details.*
4. *Refer to Section 3.6 for more details.*
5. *Refer to Section 3.7 for more details.*
6. *Refer to Section 3.8 for more details.*
7. *Refer to Section 3.9 for more details.*
8. *Refer to Section 3.10 for more details.*
9. *Refer to Section 3.17 for more details.*
10. *Refer to Section 3.11 for more details.*
11. *Refer to datasheet for availability on specific packages.*
12. *Refer to Section 3.12 for more details.*
13. *Refer to Section 3.18 for more details.*
14. *Refer to Section 3.13 for more details.*

15. Refer to Section 3.14 for more details.
16. Refer to Section 3.15 for more details.
17. Refer to Section 3.16 for more details.

3.2 Memory mapping

The table below compares register boundary addresses of the peripherals for STM32U5 series microcontrollers.

Table 2. Peripheral register boundary addresses comparison

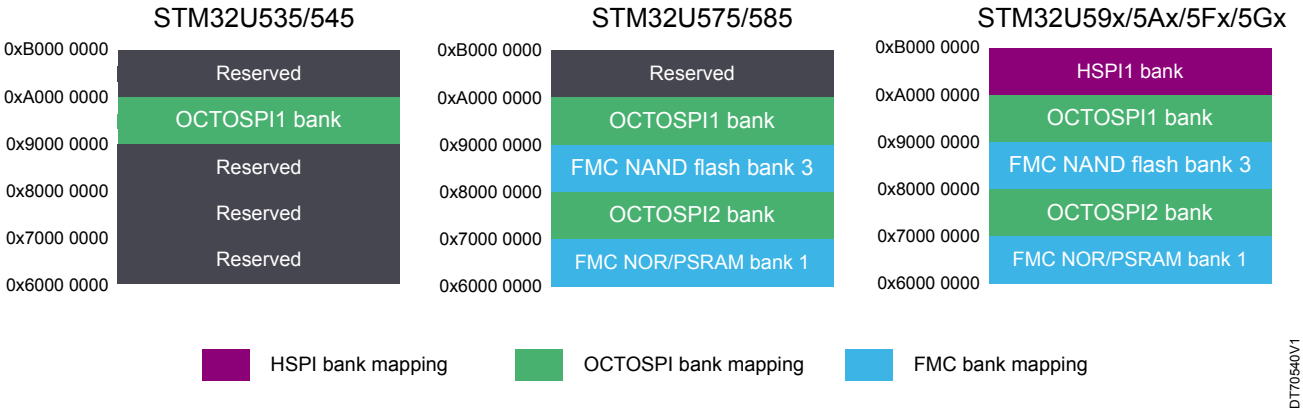
'-' means absent; 'X' means present

Bus	Peripherals	Nonsecure address	Secure address	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
AHB2	HSPI1	0x420D 3400 – 0x420D 37FF	0x520D 3400 – 0x520D 37FF	-	-	X	X
	OCTOSPI2	0x420D 2400 – 0x420D 27FF	0x520D 2400 – 0x520D 27FF	-	X	X	X
	FMC	0x420D 0400 – 0x420D 07FF	0x520D 0400 – 0x520D 07FF	-	X	X	X
	DLYBOS2	0x420C F400 – 0x420C F7FF	0x520C F400 – 0x520C F7FF	-	X	X	X
	SDMMC2	0x420C 8C00 – 0x420C 8FFF	0x520C 8C00 – 0x520C 8FFF	-	X	X	X
	DLYBSD2	0x420C 8800 – 0x420C 8BFF	0x520C 8800 – 0x520C 8BFF	-	X	X	X
	OTFDEC2	0x420C 5400 – 0x420C 57FF	0x520C 5400 – 0x520C 57FF	-	X	X	X
	OCTOSPIM	0x420C 4000 – 0x420C 43FF	0x520C 4000 – 0x520C 43FF	-	X	X	X
	OTG_HS	0x4204 0000 – 0x4205 FFFF	0x5204 0000 – 0x5205 FFFF	-	-	X	X
	OTG_FS	0x4204 0000 – 0x420B FFFF	0x5204 0000 – 0x520B FFFF	-	X	-	-
	GPIOJ	0x4202 2400 – 0x4202 27FF	0x5202 2400 – 0x5202 27FF	-	-	X	X
	GPIOI	0x4202 2000 – 0x4202 23FF	0x5202 2000 – 0x5202 23FF	-	X	X	X
	GPIOF	0x4202 1400 – 0x4202 17FF	0x5202 1400 – 0x5202 17FF	-	X	X	X
AHB1	GTZC1_MPCBB6	0x4003 3800 – 0x4003 3BFF	0x5003 3800 – 0x5003 3BFF	-	-	-	X
	GTZC1_MPCBB5	0x4003 3C00 – 0x4003 3FFF	0x5003 3C00 – 0x5003 3FFF	-	-	X	X
	GTZC1_MPCBB3	0x4003 3400 – 0x4003 37FF	0x5003 3400 – 0x5003 37FF	-	X	X	X
	DCACHE2	0x4003 1800 – 0x4003 1BFF	0x5003 1800 – 0x5003 1BFF	-	-	X	X
	GPU2D	0x4002 F000 – 0x4002 FFFF	0x5002 F000 – 0x5002 FFFF	-	-	X	X
	GFXMMU	0x4002 C000 – 0x4002 EFFF	0x5002 C000 – 0x5002 EFFF	-	-	X	X
	DMA2D	0x4002 B000 – 0x4002 BBFF	0x5002 B000 – 0x5002 BBFF	-	X	X	X
	JPEG	0x4002 A000 – 0x4002 AFFF	0x5002 A000 – 0x5002 AFFF	-	-	-	X
APB2	DSI	0x4001 6C00 – 0x4001 7BFF	0x5001 6C00 – 0x5001 7BFF	-	-	X	X
	LTDC	0x4001 6800 – 0x4001 6BFF	0x5001 6800 – 0x5001 6BFF	-	-	X	X
	GFXTIM	0x4001 6400 – 0x4001 67FF	0x5001 6400 – 0x5001 67FF	-	-	-	X
	USB RAM	0x4001 6400 – 0x4001 6BFF	0x5001 6400 – 0x5001 6BFF	X	-	-	-
	USB	0x4001 6000 – 0x4001 63FF	0x5001 6000 – 0x5001 63FF	X	-	-	-
	SAI2	0x4001 5800 – 0x4001 5BFF	0x5001 5800 – 0x5001 5BFF	-	X	X	X
APB1	UCPD1	0x4000 DC00 – 0x4000 DFFF	0x5000 DC00 – 0x5000 DFFF	-	X	X	X
	I2C6	0x4000 9C00 – 0x4000 9FFF	0x5000 9C00 – 0x5000 9FFF	-	-	X	X

Bus	Peripherals	Nonsecure address	Secure address	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
APB1	I2C5	0x4000 9800 – 0x4000 9BFF	0x5000 9800 – 0x5000 9BFF	-	-	X	X
	USART6	0x4000 6400 – 0x4000 67FF	0x5000 6400 – 0x5000 67FF	-	-	X	X
	USART2	0x4000 4400 – 0x4000 47FF	0x5000 4400 – 0x5000 47FF	-	X	X	X

The figure below presents the external memory-mapping differences for STM32U5 series microcontrollers.

Figure 1. External memory-mapping differences for STM32U5 series microcontrollers



3.3 Flash memory

The table below details the flash memory differences for STM32U5 series microcontrollers.

Table 3. Flash memory differences for STM32U5 series microcontrollers

Flash memory		STM32U535/545	STM32U575/585	STM32U59x/5Ax/5Fx/5Gx
Main/program flash memory		Up to 512 Kbytes Split in two banks Pages of 8 Kbytes per bank	Up to 2 Mbytes Split in two banks Pages of 8 Kbytes per bank	Up to 4 Mbytes Split in two banks Pages of 8 Kbytes per bank
Memory organization	Bank 1	0x800 0000 – 0x803 FFFF (for 512-Kbyte devices) 0x800 0000 – 0x801 FFFF (for 256-Kbyte devices) 0x800 0000 – 0x800 FFFF (for 128-Kbyte devices)	0x800 0000 – 0x80F FFFF (for 2-Mbyte devices) 0x800 0000 – 0x807 FFFF (for 1-Mbyte devices)	0x800 0000 – 0x81F FFFF (for 4-Mbyte devices) 0x800 0000 – 0x80F FFFF (for 2-Mbyte devices)
	Bank 2	0x804 0000 – 0x807 FFFF (for 512-Kbyte devices) 0x802 0000 – 0x803 FFFF (for 256-Kbyte devices) 0x801 0000 – 0x801 FFFF (for 128-Kbyte devices)	0x810 0000 – 0x81F FFFF (for 2-Mbyte devices) 0x808 0000 – 0x80F FFFF (for 1-Mbyte devices)	0x820 0000 – 0x83F FFFF (for 4-Mbyte devices) 0x810 0000 – 0x81F FFFF (for 2-Mbyte devices)
Features		Dual bank		

Flash memory	STM32U535/545	STM32U575/585	STM32U59x/5Ax/5Fx/5Gx
Features	Read while write (RWW)		
Read access	Read access of 128 bits (+ 9-bit ECC)		
Wait states	Up to four (depending on the supply voltage and the frequency)		
Protections	Write protection: two areas per bank Four levels of readout protection (RDP) Privileged block-based volatile areas with page granularity Secure protections when TrustZone® is activated: • up to two secure watermark-based nonvolatile areas • up to two secure hide protection areas • secure block-based volatile areas with page granularity		
One time programmable (OTP) memory	512 bytes		
Register interface	0x4002 2000 – 0x4002 23FF (nonsecure)		
	0x5002 2000 – 0x5002 23FF (secure)		

3.4 RAM memory

The table below details the RAM memory differences for STM32U5 series microcontrollers.

Table 4. RAM memory differences for STM32U5 series microcontrollers

RAM		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
Size	SRAM1	192 Kbytes		768 Kbytes	
	SRAM2	64 Kbytes			
	SRAM3	N/A	512 Kbytes	832 Kbytes	
	SRAM4	16 Kbytes			
	SRAM5	N/A		832 Kbytes	
	BKPSRAM	2 Kbytes			
Address	SRAM1	0x2000 0000 – 0x2002 FFFF (nonsecure) 0x3000 0000 – 0x3002 FFFF (secure)		0x2000 0000 – 0x200B FFFF (nonsecure) 0x3000 0000 – 0x300B FFFF (secure)	
	SRAM2	0x2003 0000 – 0x2003 FFFF (nonsecure) 0x3003 0000 – 0x3003 FFFF (secure)		0x200C 0000 – 0x200C FFFF (nonsecure) 0x300C 0000 – 0x300C FFFF (secure)	
	SRAM3	N/A	0x2004 0000 – 0x200B FFFF (nonsecure) 0x3004 0000 – 0x300B FFFF (secure)	0x200D 0000 – 0x2019 FFFF (nonsecure) 0x300D 0000 – 0x3019 FFFF (secure)	
	SRAM4	0x2800 0000 – 0x2800 3FFF (nonsecure) 0x3800 0000 – 0x3800 3FFF (secure)			
	SRAM5	N/A		0x201A 0000 – 0x2026 FFFF (nonsecure) 0x301A 0000 – 0x3026 FFFF (secure)	
Features	ECC on SRAM2, SRAM3(1), and BKPSRAM				
	Readout protection				
	Write protection 1-Kbyte granularity for SRAM2				
	Wait states configuration				
	Hardware erase with RDP regression				
	System reset erase				

RAM	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
Features	Hardware erase in tamper detection (SRAM2 and BKPSRAM)			

1. *SRAM3 is not available on STM32U535/545 devices.*

3.5 Data cache (DCACHE)

The table below details the data cache (DCACHE) differences for STM32U5 series microcontrollers.

Table 5. DCACHE differences for STM32U5 series microcontrollers

DCACHE		STM32U535/545/575/585	STM32U59x/5Ax/5Fx/5Gx
Number		1	2(1)
Features	Number of ways	2	4
	Cache size	4 Kbytes	16 Kbytes
	Cache line width	16 bytes	32 bytes
	Data size of AHB master interface	32 bits	
DCACHE registers	DCACHE_CMDRSADDRR	CMDSTARTADDR [31:4]	CMDSTARTADDR [31:5]
	DCACHE_CMDREADDRR	CMDENDADDR [31:4]	CMDENDADDR [31:5]

1. *DCACHE2 only available on STM32U599/5A9/5Fx/5Gx devices.*

Note: In STM32U599/5A9/5Fx/5Gx, the data cache 2 (DCACHE2) is placed on the AHB bus driven by the GPU2D M0 port.

3.6 Power control (PWR)

The table below details the power control (PWR) differences for STM32U5 series microcontrollers.

Table 6. PWR differences for STM32U5 series microcontrollers

'-' means absent; 'X' means present

Power control registers		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
PWR_CR1	Bit15: FORCE_USBPWR	-	-	X	X
	Bit13: SRAM6PD	-	-	-	X
	Bit12: SRAM5PD	-	-	X	X
	Bit 10: SRAM3PD	-	X	X	X
PWR_CR2	Bit 26: JPEGRAMPDS	-	-	-	X
	Bit 25: DSIRAMPDS	-	-	X	X
	Bit 24: GPRAMPDS	-	-	X	X
	Bits[23:16]: SRAM3PDSx	-	X	X	X
	Bit 10: DMA2DRAMPDS	-	X	X	X
	Bit 7: DC2RAMPDS	-	-	X	X
PWR_VOSR	Bit 21: VDD11USBDIS	-	-	X	X
	Bit 20: USBBOOSTEN	-	-	X	X

Power control registers		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
PWR_VOSR	Bit 19: USBPWREN	-	-	X	X
	Bit 13: USBBOOSTRDY	-	-	X	X
PWR_UCPDR	Bit 1: UCPD_STBY	-	X	X	X
	Bit 0: UCPD_DBDIS	-	X	X	X
PWR_PUCRF		-	X	X	X
PWR_PUCRI		-	Bits [7:0]: PUy	Bits [15:0]: PUy	Bits [15:0]: PUy
PWR_PUCRJ		-	-	X	X
PWR_CR4	Bits [28:16]: SRAM5PDSx	-	-	X	X
	Bits [14:10]: SRAM3PDSx	-	X	X	X
	Bits [7:0]: SRAM6PDSx	-	-	-	X

After reset, the regulator is the LDO, in range 4. Switching to SMPS provides lower consumption at high voltage. It is possible to switch from LDO to SMPS, or from SMPS to LDO in any range, by configuring the REGSEL bit in PWR_CR3.

On STM32U59x/5Ax/5Fx/5Gx devices only, when using the device at extended temperature ranges (from 85 °C to 125 °C), it is necessary to reduce the system frequency below 100 MHz before switching from LDO to SMPS. When exiting the Stop or Standby mode, the regulator is the same than when entering low-power modes. The voltage range is the range 4.

Dynamic voltage-scaling management

On STM32U59x/5Ax/5Fx/5Gx devices only, the maximum frequency increase or decrease in range 1 (1.2 V) is 80 MHz.

To increase the frequency in range 1 above 80 MHz, follow the steps below:

1. Divide the system clock by two, using the AHB prescaler (HPRE = 0b1000 in RCC_CFGR2).
2. Configure and enable the PLL1 if needed.
3. Select PLL1 as system clock source (SW = 0b11 in RCC_CFGR1).
4. Wait for 3 µs.
5. Set the AHB prescaler to 1 (HPRE = 0b0000 in RCC_CFGR2).

When running at frequencies higher than 80 MHz in range 1, follow the steps below to decrease the frequency:

1. Divide the system clock by two, using the AHB prescaler (HPRE = 0b1000 in RCC_CFGR2).
2. Wait for 3 µs.
3. Define the lower speed clock as system clock source.
4. Set the AHB prescaler back to 1 (HPRE = 0b0000 in RCC_CFGR2).

In the other ranges, there is no limitation during system frequency increase or decrease.

Peripheral voltage monitoring (PVM)

Due to the difference on the USB peripheral between the STM32U535/545/575/585 with a USB Full Speed (FS) and the STM32U59x/5Ax/5Fx/5Gx with a USB High Speed (HS), the following sequence must be done before using the USB OTG_HS peripheral on STM32U59x/5Ax/5Fx/5Gx devices:

1. If V_{DDUSB} is independent from V_{DD}:
   a. Enable the UVM by setting UVMEN bit in PWR_SVMCR.
   b. Wait for the UVM wake-up time.
   c. Wait until VDDUSBRDY bit is set in PWR_SVMSR.
   d. Disable the UVM for consumption saving (optional).
2. Set the USV bit in PWR_SVMCR to remove the V_{DDUSB} power isolation.
3. Make sure that the voltage scaling is in range 1 or range 2 (using VOS [1:0] bits in PWR_VOSR).
4. Make sure that the EPOD booster is in range 1 or range 2 (using PLL1MBOOST [3:0] in RCC_PLL1CFGR).
5. Enable the USB internal power by setting the USBPWREN and USBBOOSTEN bits in the PWR_VOSR.
6. Wait for USBBOOSTRDY in PWR_VOSR to be set.

USB power management in low-power modes

On STM32U59x/5Ax/5Fx/5Gx devices only, in Stop 0 and Stop 1 modes, it is possible to keep the OTG_HS configuration by leaving the USBPWREN bit set. This allows the OTG_HS to wake up the MCU from Stop mode. However, to decrease the power consumption, it is recommended to shut off the OTG_HS before entering Stop 0 or Stop 1 mode.

In Stop 2 and Stop 3 modes, it is not possible to keep the OTG_HS configuration. The OTG_HS must be shut off before entering Stop 2 or Stop 3 mode.

To shut off the OTG_HS before entering Stop mode, follow the steps below:

1. Clear the USNPWREN and USBBOOSTEN bits in PWR_VOSR.
2. Request entry in Stop mode.

Upon wake-up from Stop mode, and before configuring the OTG_HS:

1. Make sure that the voltage scaling is in range 1 or range 2 (using VOS [1:0] in PWR_VOSR).
2. Make sure that the EPOD booster clock is enabled using PLL1MBOOST [3:0] in RCC_PLL1CFGR.
3. Enable the USB internal power by setting the USBPWREN and USBBOOSTEN bits in PWR_VOSR.
4. Wait for USBBOOSTRDY in PWR_VOSR to be set.

3.7 Reset and clock control (RCC)

The table below details the RCC (reset and clock controller) differences for STM32U5 series microcontrollers.

Table 7. RCC differences for STM32U5 series microcontrollers

RCC	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
UCPD1	N/A	HSI16		
USARTx(1)	PCLK1 LSE HSI16 SYSCLK			
I2Cx(2)	PCLK1 HSI16 SYSCLK MSI kernel clock			
OCTOSPIx(3)	SYSCLK MSI kernel clock PLL1/Q PLL2/Q			
SAIx(3)	AUDIOCLK PLL1/P PLL2/P PLL3/P HSI16			
SDMMCx(3)	PLL1/P PLL1/Q PLL2/Q MSI kernel clock HSI48			
USB	MSI kernel clock HSI48 PLL1/Q PLL2/Q	N/A		
OTG_FS	N/A	MSI kernel clock HSI48 PLL1/Q PLL2/Q	N/A	
OTG_HS	N/A		HSE PLL1/P PLL1/2P HSE/2	
ADCx(4)	HCLK SYSCLK PLL2/R HSE HSI16 MSI kernel clock			
DAC1				
DAC1 sample and hold clock	LSI LSE			
HSPI	N/A		SYSCLK PLL1/Q PLL2/Q PLL3/R	
LTDC	N/A		PLL2/R PLL3/R	
DSI	N/A		PLL3/P HSE	
PLL	3 PLLs (PLL1, PLL2, PLL3)			

1. *x = 1, 3, 4, 5 for STM32U535/545*
   x = 1 to 5 for STM32U575/585
   x = 1 to 6 for STM32U59x/5Ax/5Fx/5Gx
2. *x = 1, 2, 4, 5 for STM32U535/545/575/585*
   x = 1, 2, 4, 5, 6 for STM32U59x/5Ax/5Fx/5Gx
3. *Refer to datasheet for availability.*
4. *x = 1, 4 for STM32U535/545/575/585*
   x = 1, 2, 4 for STM32U59x/5Ax/5Fx/5Gx

The table below highlights the RCC (reset and clock controller) registers differences for STM32U5 series microcontrollers.

Table 8. RCC registers differences for STM32U5 series microcontrollers

'-' means absent; 'X' means present

RCC registers		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
RCC_CFGR2	Bits [14:12]: DPRE	-	-	X	X
RCC_AHB1RSTR	Bit 20: GPU2DRST	-	-	X	X
	Bit 19: GFXMMURST	-	-	X	X
	Bit 18: DMA2DRST	-	X	X	X
	Bit 15: JPEGRST	-	-	-	X
RCC_AHB2RSTR1	Bit 28: SDMMC2RST	-	X	X	X
	Bit 24: OTFDEC2RST	-	X	X	X
	Bit 21: OCTOSPIMRST	-	X	X	X
	Bit 14: OTGRST (for OTG_FS)	-	X	X	X
	Bit 9: GPIOJRST	-	-	X	X
	Bit 8:GPIOIRST	-	X	X	X
	Bit 5:GPIOFRST	-	X	X	X
RCC_AHB2RSTR2	Bit 12: HSPI1RST	-	-	X	X
	Bit 8: OCTOSPI2RST	-	X	X	X
	Bit 0: FSMCRST	-	X	X	X
RCC_APB1RSTR1	Bit 25: USART6RST	-	-	X	X
	Bit 17: USART2RST	-	X	X	X
RCC_APB1RSTR2	Bit 23: UCPD1RST	-	X	X	X
	Bit 7: I2C6RST	-	-	X	X
	Bit 6: I2C5RST	-	-	X	X
RCC_APB2RSTR	Bit 27: DSIRST	-	-	X	X
	Bit 26: LTDCRST	-	-	X	X
	Bit 25:GFXTIMRST	-	-	-	X
	Bit 24: USBRST	X	-	-	-
	Bit 22: SAI2RST	-	X	X	X
RCC_AHB1ENR	Bit 21: DCACHE2EN	-	-	X	X
	Bit 20: GPU2DEN	-	-	X	X

RCC registers		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
RCC_AHB1ENR	Bit 19: GFXMMUEN	-	-	X	X
	Bit 18: DMA2DEN	-	X	X	X
	Bit 15: JPEGEN	-	-	-	X
RCC_AHB2ENR1	Bit 31: SRAM3EN	-	X	X	X
	Bit 28: SDMMC2EN	-	X	X	X
	Bit 24: OTFDEC2EN	-	X	X	X
	Bit 21: OCTOSPIMEN	-	X	X	X
	Bit 15: OTGHSPHYEN	-	-	X	X
	Bit 14: OTGEN	-	X	X	X
	Bit 9: GPIOJEN	-	-	X	X
	Bit 8: GPIOIEN	-	X	X	X
	Bit 5: GPIOFEN	-	X	X	X
RCC_AHB2ENR2	Bit 31: SRAM5EN	-	-	X	X
	Bit 30: SRAM6EN	-	-	-	X
	Bit 12: HSPIEN	-	-	X	X
	Bit 8: OCTOSPI2EN	-	X	X	X
	Bit 0: FSMCEN	-	X	X	X
RCC_APB1ENR1	Bit 25: USART6EN	-	-	X	X
	Bit 17: USART2EN	-	X	X	X
RCC_APB1ENR2	Bit 23: UCPD1EN	-	X	X	X
	Bit 7: I2C6EN	-	-	X	X
	Bit 6: I2C5EN	-	-	X	X
RCC_APB2ENR	Bit 27: DSIEN	-	-	X	X
	Bit 26: LTDCEN	-	-	X	X
	Bit 25: GFXTIMEN	-	-	-	X
	Bit 24: USBEN	X	-	-	-
	Bit 22: SAI2EN	-	X	X	X
RCC_AHB1SMENR	Bit 21: DCACHE2SMEN	-	-	X	X
	Bit 20: GPU2DSMEN	-	-	X	X
	Bit 19: GFXMMUSMEN	-	-	X	X
	Bit 18: DMA2DSMEN	-	X	X	X
	Bit 15: JPEGSMEN	-	-	-	X
RCC_AHB2SMENR1	Bit 31: SRAM3SMEN	-	X	X	X
	Bit 28: SDMMC2SMEN	-	X	X	X
	Bit 24: OTFDEC2SMEN	-	X	X	X
	Bit 21: OCTOSPIMSMEN	-	X	X	X
	Bit 15: OTGHSPHYSMEN	-	-	X	X

RCC registers		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
RCC_AHB2SMENR1	Bit 14: OTGSMEN	-	X	X	X
	Bit 9: GPIOJSMEN	-	-	X	X
	Bit 8: GPIOISMEN	-	X	X	X
	Bit 5: GPIOFSMEN	-	X	X	X
RCC_AHB2SMENR2	Bit 31: SRAM5SMEN	-	-	X	X
	Bit 30: SRAM6SMEN	-	-	-	X
	Bit 12: HSPI1SMEN	-	-	X	X
	Bit 8: OCTOSPI2SMEN	-	X	X	X
	Bit 0: FSMCSMEN	-	X	X	X
RCC_APB1SMENR1	Bit 25: USART6SMEN	-	-	X	X
	Bit 17: USART2SMEN	-	X	X	X
RCC_APB1SMENR2	Bit 23: UCPD1SMEN	-	X	X	X
	Bit 7: I2C6SMEN	-	-	X	X
RCC_APB1SMENR2	Bit 6: I2C5SMEN	-	-	X	X
RCC_APB2SMENR	Bit 27: DSISMEN	-	-	X	X
	Bit 26: LTDCSMEN	-	-	X	X
	Bit 25: GFXTIMSMEN	-	-	-	X
	Bit 24: USBSMEN	X	-	-	-
	Bit 22: SAI2SMEN	-	X	X	X
RCC_CCIPR1	Bits [3:2]: USART2SEL	-	X	X	X
RCC_CCIPR2	Bits [31:30]: OTGHSSEL	-	-	X	X
	Bits [27:26]: I2C6SEL	-	-	X	X
	Bits [25:24]: I2C5SEL	-	-	X	X
	Bits [23:22]: HSPI1SEL	-	-	X	X
	Bit 18: LTDCSEL	-	-	X	X
	Bits [17:16]: USART6SEL	-	-	X	X
	Bit 15: DSISEL	-	-	X	X
	Bits [10:8]: SAI2SEL	-	X	X	X

3.8 System configuration controller (SYSCFG)

The STM32U59x/5Ax/5Fx/5Gx microcontrollers have additional features on their system configuration controller (SYSCFG) to configure the USB_HS_PHY, and adjust the HSPI supply capacitance and internal SRAMs cacheability.

Configuring the OTG_HS_PHY

To use the OTG_HS PHY, the following configuration steps are required before the configuration of the OTG_HS.

1. Activate clocks in RCC clock gating registers for SYSCFG, OTG_HS, and OTG_HS PHY.
2. Configure the desired clock settings for OTG_HS PHY using CLKSEL bitfield in SYSCFG_OTGHSPHYCR.
3. Enable the OTG_HS PHY by setting EN bit in SYSCFG_OTGHSPHYCR.

Adjusting HSPI supply capacitance

The HSPI supply capacitance can be adjusted using the ENDCAP [1:0] control bits in the SYSCFG_CFGR1 register. If the HSPI alternate functions are not used, the ENDCAP [1:0] bitfield must be left at its reset value.

Internal SRAMs cacheability by DCACHE2

Since DCACHE2 is only addressed by the GPU2D M0 port, and because vector graphic algorithms can manipulate data on the M1 port, it is recommended to clear SRAMCACHED in SYSCFG_CFGR1 before activating the GPU2D, to avoid any cache coherency issues. Also, since internal SRAMs are accessible in zero wait state through the bus matrix, no performance degradation is expected.

3.9 General purpose direct memory access controller (GPDMA)

The STM32U5 series microcontrollers share the same GPDMA master interface. Due to the additional peripherals available on STM32U59x/5Ax/5Fx/5Gx microcontrollers, the GPDMA channels connections and requests corresponding to those peripherals are present only for STM32U59x/5Ax/5Fx/5Gx microcontrollers and left free for STM32U535/545/575/585 microcontrollers. The table below details the extra GPDMA features available on STM32U5 series microcontrollers.

Table 9. GPDMA register differences for STM32U5 series microcontrollers

'-' means absent; 'X' means present

GPDMA_CxTR2 register		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
TRIGSEL[5:0]	44: tim3_trgo(1)	-	-	X	X
	45: tim4_trgo(1)	-	-	X	X
	46: tim5_trgo(1)	-	-	X	X
	47: ltdc_li	-	-	X	X
	48: dsi_te	-	-	X	X
	49: dsi_er	-	-	X	X
	50: dma2d_tc	-	-	X	X
	51: dma2d_ctc	-	-	X	X
	52: dma2d_tw	-	-	X	X
	53: gpu2d_flag[0]	-	-	X	X
	54: gpu2d_flag[1]	-	-	X	X
	55: gpu2d_flag[2]	-	-	X	X
	56: gpu2d_flag[3]	-	-	X	X
	59: gfxtim_ev4	-	-	-	X
	60: gfxtim_ev3	-	-	-	X
	61: gfxtim_ev2	-	-	-	X
	62: gfxtim_ev1	-	-	-	X
	63: jpeg_eoc_trg	-	-	-	X
	64: jpeg_ifnf_trg	-	-	-	X
	65: jpeg_ift_trg	-	-	-	X
	66: jpeg_ofne_trg	-	-	-	X

GPDMA_CxTR2 register		STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
TRIGSEL[5:0]	67: jpeg_oft_trg	-	-	-	X
REQSEL[6:0]	26: usart2_rx_dma	-	X	X	X
	27: usart2_tx_dma	-	X	X	X
	38: sai2_a_dma	-	X	X	X
	39: sai2_b_dma	-	X	X	X
	41: octospi2_dma	-	X	X	X
	90: ucpd1_tx_dma	-	X	X	X
	91: ucpd1_rx_dma	-	X	X	X
	114: hspi1_dma	-	-	X	X
	115: i2c5_rx_dma	-	-	X	X
	116: i2c5_tx_dma	-	-	X	X
	117: i2c5_evc_dma	-	-	X	X
	118: i2c6_rx_dma	-	-	X	X
	119: i2c6_tx_dma	-	-	X	X
	120: i2c6_evc_dma	-	-	X	X
	121: usart6_rx_dma	-	-	X	X
	122: usart6_tx_dma	-	-	X	X
	123: adc2_dma	-	-	X	X
	124: jpeg_rx_dma	-	-	-	X
	125: jpeg_tx_dma	-	-	-	X

1. *Peripheral available on STM32U535/545/575/585 but new feature on STM32U59x/5Ax/5Fx/5Gx.*

3.10 Chrom-GRC (GFXMMU)

The GFXMMU peripheral is available only on STM32U599/5A9/5Fx/5Gx microcontrollers for customers who need graphical applications. It is a graphical memory management unit aimed to optimize the memory usage according to the display shape.

The GFXMMU allows up to 20% of graphic resources optimization.

Refer to dedicated datasheets and reference manual for more details on the GFXMMU features.

3.11 Nested vectored interrupt controller (NVIC)

The table below presents the interrupt vectors differences for STM32U5 series microcontrollers.

Table 10. Interrupt vectors differences for STM32U5 series microcontrollers

'-' means absent; 'X' means present

Position	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
62: USART2	-	X	X	X
75: FMC	-	X	X	X
79: SDMMC2	-	X	X	X
91: SAI2	-	X	X	X
106: UCPD1	-	X	X	X
120: OCTOSPI2	-	X	X	X
118: DMA2D	-	X	X	X
126: USART6	-	-	X	X
127: I2C5_ER	-	-	X	X
128: I2C5_EV	-	-	X	X
129: I2C6_ER	-	-	X	X
130: I2C6_EV	-	-	X	X
131: HSPI1	-	-	X	X
132: GPU2D_IRQ	-	-	X	X
133: GPU2D_IRQSYS	-	-	X	X
134: GFXMMU	-	-	X	X
135: LCD_TFT	-	-	X	X
136: LCD_TFT_ERR	-	-	X	X
137: DSIHOST	-	-	X	X
138: DCACHE2	-	-	X	X
139: GFXTIM	-	-	-	X
140: JPEG	-	-	-	X

3.12 Hexadeca-SPI interface (HSPI)

The HSPI peripheral is available only on STM32U599/5A9/5Fx/5Gx microcontrollers. It shares the same features than the Octo-SPI (OCTOSPI) peripheral in STM32U535/545/575/585 microcontrollers. The HSPI can support 16-bit SPI memories or two octal-SPI memories at the same time. The HSPI interface can reach a frequency up to 160 MHz compared to 93 MHz for the OCTOSPI. It targets single-, dual-, quad-, octal-SPI, or 16-bit SPI memories.

The HSPI can be configured in three modes: Indirect mode, automatic status-polling mode, and memory-mapped mode.

Refer to document [1] and dedicated datasheets for more details on the HSPI features.

3.13 LCD-TFT display controller (LTDC)

The LTDC peripheral is available only on STM32U599/5A9/5Fx/5Gx microcontrollers. It provides a parallel digital RGB (red, green, blue), signals for horizontal, vertical synchronization, a pixel clock, and data enable as output to interface directly to a variety of LCD and TFT panels.

The LTDC supports a 24-bit RGB parallel pixel output, two display layers with a dedicated FIFO (64x32-bit), and a color look-up table (CLUT) up to 256 color (256x24-bit) per layer.

Refer to document [1] and dedicated datasheets for more details on the LTDC features.

3.14 DSI host (DSI)

The DSI peripheral is available only on STM32U599/5A9/5Fx/5Gx devices. It is a digital core that implements all protocol functions defined in the MIPI DSI specification.

The DSI peripheral provides an interface between the system and the MIPI D-PHY, allowing the user to communicate with a DSI-compliant display.

It supports up to two D-PHY data lanes, noncontinuous clock in D-PHY clock lane and an ultra-low power mode with PLL disabled for additional power saving.

Refer to document [1] and dedicated datasheets for more details on the DSI features.

3.15 Neo-Chrom graphic processor (GPU2D)

The GPU2D peripheral is available only on STM32U599/5A9/5Fx/5Gx microcontrollers. It is a dedicated graphics processing unit accelerating numerous 2.5D graphics applications such as graphical user interface (GUI), menu display, or animations.

The GPU2D works together with an optimized software stack designed for state-of-the-art graphic rendering. It supports a multithreaded fragment (pixel) processing core with a VLIW (very-long instruction word) instruction and command list-based DMAs to minimize CPU overhead.

Refer to document [1] and dedicated datasheets for more details of the GPU2D features.

3.16 JPEG codec (JPEG)

The JPEG codec peripheral is available only on STM32U5Fx/5Gx devices. It is a hardware 8-bit image data stream encoder/decoder.

The JPEG supports:

- high-speed fully synchronous operation
- configurable as encoder or decoder
- single-clock-per-pixel encode/decode
- RGB, YCbCr, YCMK, and BW (gray-scale) image color space support
- 8-bit depth per image component at encode/decode
- JPEG header generator/parser with enable/disable
- four programmable quantization tables
- single-clock Huffman coding and decoding
- fully programmable Huffman tables (two ACs and two DCs)
- fully programmable minimum coded unit (MCU)
- concurrent input and output data stream interfaces

Refer to document [1] and dedicated datasheets for more details on the JPEG features.

3.17 Graphic timer (GFXTIM)

The graphic timer (GFXTIM) is available only on STM32U5Fx/5Gx microcontrollers. It is a graphic oriented timer allowing smart management of graphical events for frame or line counting.

The GFXTIM supports:

- integrated frame and line clock generation
- one absolute frame counter with one compare channel
- two auto-reload relative frame counters
- one line timer with two compare channels
- external tearing-effect line management and synchronization
- four programmable event generators with external trigger generation
- one watchdog counter

Refer to document [1] and dedicated datasheets for more details on the GFXTIM features.

3.18 USB peripheral (FS/OTG_FS/OTG_HS)

The table below details the USB differences for STM32U5 series microcontrollers.

Table 11. USB differences STM32U5 series microcontrollers

USB features		STM32U535/545	STM32U575/585	STM32U59x/5Ax/5Fx/5Gx
		FS (full-speed)	OTG_FS (full-speed)	OTG_HS (high-speed)
Speed	Host mode	12 Mb/s, 1.5 Mb/s		480 Mb/s, 12 Mb/s, 1.5 Mb/s
	Device mode	12 Mb/s		480 Mb/s, 12 Mb/s
Number of bidirectional endpoints		8	6	9
Host mode channels		12		16
Size of dedicated SRAM (Kbytes)		2	1.2	4
USB 2.0 support		Yes		
OTG revision supported		N/A	2.0	
Battery charging detection (BCD) support		Yes		
Embedded PHY		Yes		

Warning: *The USB start of frame (USB SOF) can no longer be used as input for the clock recovery system on STM32U59x/5Ax/5Fx/5Gx devices. It is mandatory to have an external HSE clock to use the USB peripheral, even in device mode.*

Revision history

Table 12. **Document revision history**

Date	Version	Changes
27-Feb-2023	1	Initial release.

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