Migrating from ST25R39xx to ST25R39xxB

Introduction

The ST25R39xxB NFC device is a pin-to-pin compatible update of the ST25R39xx, except for the capacitive sensing feature on CSI/CSO, which is not available on the ST25R39xxB.

It comprises several enhancements such as advanced wave shaping, transmit (Tx) driver stepping, and an updated EMD suppression support for EMVCo® 3.1a.

Table 1. Applicable products

Type	Part number
ST25R39xx	ST25R3916
	ST25R3917
	ST25R3920
ST25R39xxB	ST25R3916B
	ST25R3917B
	ST25R3920B

1 Terms and acronyms

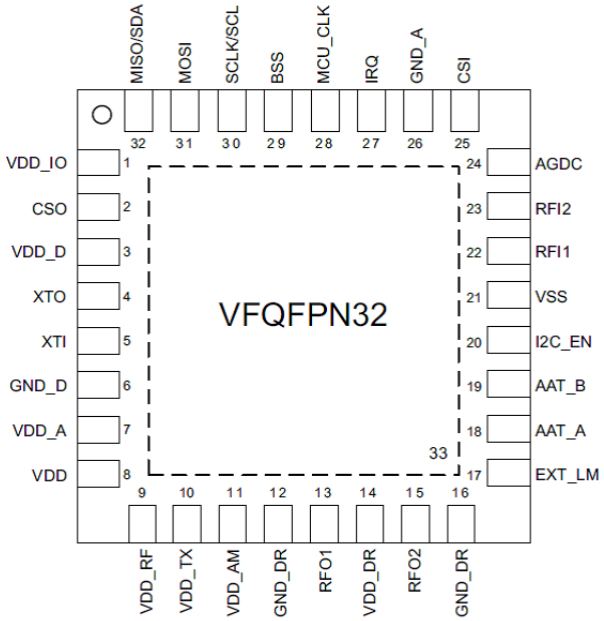
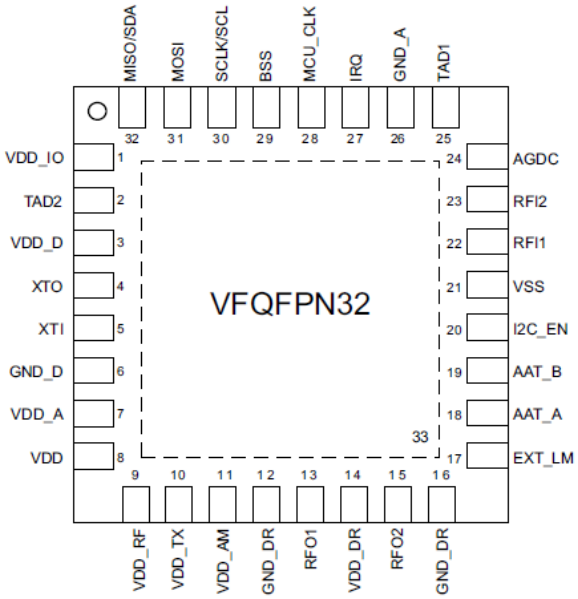
Table 2. Terms definition

Acronym	Definition
AAT	Automatic antenna tuning
ADC	Analog to digital converter
AP2P	Active P2P
AWS	Active wave shaping
CSO	Capacitance sense output
CSI	Capacitance sense input
DAC	Digital to analog converter
DPO	Dynamic power output
EMC	Electromagnetic compatibility
EMD	Electromagnetic disturbance
HW	Hardware
I²C	Inter-integrated circuit
IRQ	Interrupt request
MCU	Microcontroller
NFC	Near field communication
P2P	Peer to peer
PSRR	Power supply rejection ratio
PCB	Printed circuit board
RC	Resistive capacitive
RF	Radio frequency
RFAL	RF abstraction layer
Rx	Receive signal (from antenna to RFI)
SPI	Serial peripheral interface
SW	Software
Tx	Transmit signal (from RFO to antenna)

2 Pinout comparison

Both devices, ST25R39xx and ST25R39xxB, are pin-to-pin compatible, except for the capacitive sensing feature on CSI/CSO, which is not available on ST25R39xxB. Additional wave shaping features have been implemented in ST25R39xxB that require a change of the external connected VDD_AM capacitors. The capacitive sensor function has been removed and the corresponding pins are only available as test analog digital (TAD) pins.

Table 3. Pinout comparison between ST25R3916 and ST25R3916B

ST25R3916	ST25R3916B
	

3 ST25R39xxB changes

The ST25R39xxB has been improved and updated in the following domains:

- Advanced shaping of NFC-A, B, V, F modulation waveforms
- Finer granularity for stepping through Tx driver resistances
- AM modulation depth range increased
- EMD handling for EMVCo® 3.1a added
- Wakeup mechanism with varicaps using meas_tx_del settling time
- Removal of capacitive sensor
- Few changes in the register interface

4 Device behavior after power-on and VDD_AM capacitor usage

The ST25R39xxB is an improved version of the ST25R39xx device, which keeps most features of its predecessor. Hence, the new active wave-shaping features are not be automatically enabled after powering-on the ST25R39xxB device. The focus is to maintain the ST25R39xx behavior as far as the newly introduced features allow.

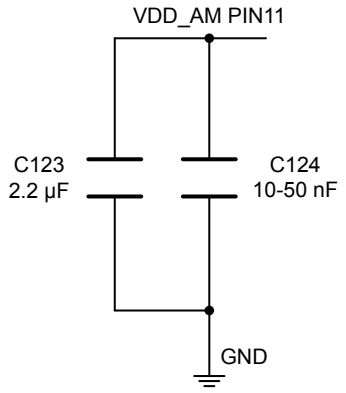
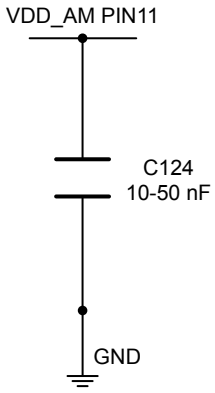
The existing procedures and the software for ST25R39xx can be reused with few warnings:

- Special care must be taken with the Tx driver register 0x28h.
- d_res, which is the driver range in bits, is extended, and any previous ST25R39xx setting cannot be applied one by one.
- The modulation index in the same register is increased from 0 to 82%.
- The am_mod setting, used with the ST25R39xx, does not produce in the same modulation index for the ST25R39xxB.

To use the ST25R39xxB specific wave shaping functionality (AWS), the logic must be enabled in the auxiliary modulation setting as well as the corresponding AWS registers. Additionally, the external VDD_AM capacitor must be selected in a range of 10-50 nF.

Note: Contrary to the recommendations for the ST25R39xx, do not insert a 2.2 µF capacitor on the VDD_AM pin when using AWS.

Table 4. Pinout comparison between ST25R39xx and ST25R39xxB

VDD_AM capacitor requirement for ST25R39xxB in ST25R39xx legacy mode	VDD_AM capacitor requirement for ST25R39xxB using new wave-shaping functionality (rgs_am=1)
	

5 Registers

Several new registers have been added to accommodate the new features and others have been removed. The following table gives an overview of the registers (The updated registers are highlighted in bold, and the removed ones have the text crossed out.

Table 5. Register space A

Register type	Address (hex)	Register space A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IO configuration	00	IO configuration register 1	single	rfo2	i2c_thd1	i2c_thd0	RFU	out_cl1	out_cl0	if_clk_off
	01	IO configuration register 2	sup3V	vspd_off	aat_en	miso_pd2	miso_pd1	io_drv_lvl	am_ref_rf	was: slow_up new: **act_amsink**
Operation control and mode definition	02	Operation control register	en	rx_en	rx_chn	rx_man	tx_en	wu	eb_fd_c1	en_fd_c0
	03	Mode definition register	targ	om3	om2	om1	om0	tr_am	nfc_ar1	nfc_ar0
	04	Bit rate definition register	RFU	RFU	tx_rate1	tx_rate0	RFU	RFU	rx_rate1	rx_rate0
Protocol configuration	05	ISO14443A and NFC 106 kb/s settings register	no_tx_par	no_rx_par	nfc_f0	p_len3	p_len2	p_len1	p_len0	antcl
	06	ISO14443B settings register 1	egt2	egt1	egt0	sof_0	sof_1	eof	half	RFU
	07	ISO14443B and Felica settings register	tr1_1	tr1_0	no_sof	no_eof	RFU	RFU	f_p1	f_p0
	08	NFCIP-1 passive target definition register	fdel3	fdel2	fdel1	fdel0	d_ac_ap2p	d_212/424_1r	RFU	d_106_ac_a
	09	Stream mode definition register	RFU	scf1	scf0	scp1	scp0	stx2	stx1	stx0
	0A	Auxiliary Definition register	no_crc_rx	RFU	nfc_id1	nfc_id0	mfaz_cl90	dis_corr	nfc_n1	nfc_n0
Receiver Configuration	0B	Receiver configuration register 1	ch_sel	lp2	lp1	lp0	z600k	h200	h80	z12k
	0C	Receiver configuration register 2	demod_mode	amd_sel	sqm_dyn	pulz_61	agc_en	agc_m	agc_alg	agc6_3
	0D	Receiver configuration register 3	rg1_am2	rg1_am1	rg1_am0	rg1_pm2	rg1_pm1	rg1_pm0	lf_en	lf_op
	0E	Receiver configuration register 4	rg2_am3	rg2_am2	rg2_am1	rg2_am0	rg2_pm3	rg2_pm2	rg2_pm1	rg2_pm0
Timer definition	0F	Mask receive timer register	mrt7	mrt6	mrt5	mrt4	mrt3	mrt2	mrt1	mrt0

Register type	Address (hex)	Register space A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Timer definition	10	No-response timer register 1	nrt15	nrt14	nrt13	nrt12	nrt11	nrt10	nrt9	nrt8
	11	No-response timer register 1	nrt7	nrt6	nrt5	nrt4	nrt3	nrt2	nrt1	nrt0
	12	Timer and EMV control register	gptc2	gptc1	gptc0	RFU	mrt_step	nrt_nfc	nrt_emv	nrt_step
	13	General purpose timer register 1	gpt15	gpt14	gpt13	gpt12	gpt11	gpt10	gpt9	gpt8
	14	General purpose timer register 2	gpt7	gpt6	gpt5	gpt4	gpt3	gpt2	gpt1	gpt0
	15	PPON2 field waiting register	ppt7	ppt6	ppt5	ppt4	ppt3	ppt2	ppt1	ppt0
Interrupt and associated reporting	16	Mask main interrupt register	M_osc	M_wl	M_rxs	M_rxe	M_txe	M_col	M_rx_rest	RFU
	17	Mask timer and NFC interrupt register	M_dct	M_nre	M_gpe	M_eon	M_eof	M_cac	M_cat	M_nfct
	18	Mask error and wake-up interrupt register	M_crc	M_par	M_err2	M_err1	M_wt	M_wam	M_wph	**was: M_wcap new: RFU**
	19	Mask passive target interrupt register	M_ppon2	M_sl_wl	M_apon	M_rxe_pta	M_wu_f	RFU	M_wu_A*	M_wu_a
	1A	Main interrupt register	I_osc	I_wl	I_rxs	I_rxe	I_txe	I_col	I_rx_rest	RFU
	1B	Timer and NFC interrupt register	I_dct	I_nre	I_gpe	I_eon	I_eof	I_cac	I_cat	I_nfct
	1C	Error and wake-up interrupt register	I_crc	I_par	I_err2	I_err1	I_wt	I_wam	I_wph	**was: I_wcap new: RFU**
	1D	Passive target interrupt register	I_ppon2	I_sl_wl	I_apon	I_rxe_pta	I_wu_f	RFU	I_wu_a*	I_wu_a
	1E	FIFO status register 1	fifo_b7	fifo_b6	fifo_b5	fifo_b4	fifo_b3	fifo_b2	fifo_b1	fifo_b0
	1F	FIFO status register 2	fifo_b9	fifo_b8	fifo_unf	fifo_ovr	fifo_lb2	fifo_lb1	fifo_lb0	np_lb
	20	Collision display register	c_byte3	c_byte2	c_byte1	c_byte0	c_bit2	c_bit1	c_bit0	c_pb
	21	Passive target display register	RFU	RFU	RFU	RFU	pta_state3	pta_state2	pta_state1	pta_state0
Definition of number of transmitted bytes	22	Number of transmitted bytes register 1	ntx12	ntx11	ntx10	ntx9	ntx8	ntx7	ntx6	ntx5
	23	Number of transmitted bytes register 2	ntx4	ntx3	ntx2	ntx1	ntx0	nbtx2	nbtx1	nbtx0
	24	Bit rate detection display register	RFU	RFU	nfc_rate1	nfc_rate0	ppt2_on	gpt_on	nrt_on	mrt_on
A/D converter output	25	A/D converter output register	ad7	ad6	ad5	ad4	ad3	ad2	ad1	ad0

Register type	Address (hex)	Register space A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Antenna calibration	26	Antenna tuning control register 1	aat_A_7	aat_A_6	aat_A_5	aat_A_4	aat_A_3	aat_A_2	aat_A_1	aat_A_0
	27	Antenna tuning control register 2	aat_B_7	aat_B_6	aat_B_5	aat_B_4	aat_B_3	aat_B_2	aat_B_1	aat_B_0
Antenna driver and modulation	28	TX driver register	am_mod 3	am_mod 2	am_mod 1	am_mod 0	d_res3	d_res2	d_res1	d_res0
	29	Passive target modulation reigster	ptm_res 3	ptm_res 2	ptm_res 1	ptm_res 0	pt_res3	pt_res2	pt_res1	pt_res0
External field detector threshold	2A	External field detector activation threshold register	RFU	trg_l2	trg_l1	trg_l0	rfe_t3	rfe_t2	rfe_t1	rfe_t0
	2B	External field detector deactivation threshold register	RFU	trg_ld2	trg_ld1	trg_ld0	rfe_td3	rfe_td2	rfe_td1	rfe_td0
Regulator	2C	Regulator voltage control register	reg_s	rege_3	rege_2	rege_1	rege_0	mpsv2	mpsv1	mpsv0
Receiver state display	2D	RSSI display register	rssi_am_ 3	rssi_am_ 2	rssi_am_ 1	rssi_am_ 0	rssi_pm3	rssi_pm2	rssi_pm1	rssi_pm0
	2E	Gain reduction state register	gs_am_3	gs_am_2	gs_am_1	gs_am_0	gs_pm_3	gs_pm_2	gs_pm_1	gs_pm_0
was: Capacitive sensor **new: Register removed**	**~~2F~~**	**~~Capacitive sensor control register~~**	**~~cs_mcal 4~~**	**~~cs_mcal 3~~**	**~~cs_mcal 2~~**	**~~cs_mcal 1~~**	**~~cs_mcal 0~~**	**~~cs_g2~~**	**~~cs_g1~~**	**~~cs_g0~~**
	~~30~~	**~~Capacitive sensor display register~~**	**~~cs_cal4~~**	**~~cs_cal3~~**	**~~cs_cal2~~**	**~~cs_cal1~~**	**~~cs_cal0~~**	**~~cs_cal_ end~~**	**~~cs_cal_ err~~**	**~~RFU~~**
Auxiliary display	31	Auxiliary Display register	a_cha	efd_o	tx_on	osc_ok	rx_on	rx_act	en_peer	en_ac
Wakeup	32	Wake-up timer control register	wur	wut2	wut1	wut0	wto	wam	wph	**was: wcap** **new: RFU**
	33	Amplitude measurement configuration register	am_d3	am_d2	am_d1	am_d0	am_aam	am_aew 1	am_aew 2	am_ae
	34	Amplitude measurement reference register	am_ref7	am_ref6	am_ref5	am_ref4	am_ref3	am_ref2	am_ref1	am_ref0
	35	Amplitude measurement auto-averaging display register	amd_aa d7	amd_aa d6	amd_aa d5	amd_aa d4	amd_aa d3	amd_aa d2	amd_aa d1	amd_aa d0
	36	Amplitude measurement display register	am_amd 7	am_amd 6	am_amd 5	am_amd 4	am_amd 3	am_amd 2	am_amd 1	am_amd 0
	37	Phase measurement configuration register	pm_d3	pm_d2	pm_d1	pm_d0	pm_aam	pm_aew 1	pm_aew 0	pm_ae
	38	Phase measurement reference register	pm_ref7	pm_ref6	pm_ref5	pm_ref4	pm_ref3	pm_ref2	pm_ref1	pm_ref0

Register type	Address (hex)	Register space A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Wakeup	39	Phase measurement auto-averaging display register	pm_aad 7	pm_aad 6	pm_aad 5	pm_aad 4	pm_aad 3	pm_aad 2	pm_aad 1	pm_aad 0
	3A	Phase measurement display register	pm_amd 7	pm_amd 6	pm_amd 5	pm_amd 4	pm_amd 3	pm_amd 2	pm_amd 1	pm_amd 0
	3B	**Measurement TX delay**	**m_phase_ana**	**m_amp_ana**	**RFU**	**RFU**	**RFU**	**RFU**	**RFU**	**meas_tx_del**
	~~3C~~	**~~Capacitance measurement reference register~~**	**~~cm_ref7~~**	**~~cm_ref6~~**	**~~cm_ref5~~**	**~~cm_ref4~~**	**~~cm_ref3~~**	**~~cm_ref2~~**	**~~cm_ref1~~**	**~~cm_ref0~~**
	~~3D~~	**~~Capacitance measurement auto-averaging display register~~**	**~~cm_aad 7~~**	**~~cm_aad 6~~**	**~~cm_aad 5~~**	**~~cm_aad 4~~**	**~~cm_aad 3~~**	**~~cm_aad 2~~**	**~~cm_aad 1~~**	**~~cm_aad 0~~**
	~~3E~~	**~~Capacitance measurement display register~~**	**~~cm_amd 7~~**	**~~cm_amd 7~~**	**~~cm_amd 7~~**	**~~cm_amd 7~~**	**~~cm_amd 7~~**	**~~cm_amd 7~~**	**~~cm_amd 7~~**	**~~cm_amd 7~~**
IC identity	3F	IC identity register	ic_type4	ic_type3	ic_type2	ic_type1	ic_type0	ic_rev2	ic_rev1	ic_rev0

Table 6. Register space B

Address (hex)	Register space B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
05	EMD suppression configuration register	emd_emv	rx_start_emv	RFU	RFU	emd_thld3	emd_thld2	emd_thld1	emd_thld0
06	Subcarrier start timer register	RFU	RFU	RFU	sst<4:0>	sst<4:0>	sst<4:0>	sst<4:0>	sst<4:0>
0B	P2P receiver configuration register 1	oof_fd	oof_r1	ook_rc0	ook_thd1	ook_thd0	ask_rc1	ask_rc0	ask_thd
0C	Correlator configuration register 1	corr_s7	corr_s6	corr_s5	corr_s4	corr_s3	corr_s2	corr_s1	corr_s0
0D	Correlator configuration register 2	**RFU**	**RFU**	RFU	RFU	RFU	RFU	corr_s9	corr_s8
0F	Squelch timer register	sqt7	sqt6	sqt5	sqt4	sqt3	sqt2	sqt1	sqt0
15	NFC field on guard timer register	nfc_gt7	nfc_gt6	nfc_gt5	nfc_gt4	nfc_gt3	nfc_gt2	nfc_gt1	nfc_gt0
28	Auxiliary modulation setting register	dis_reg_am	lm_ext_pol	lm_ext	lm_dri	res_am	**new: rgs_am**	RFU	RFU
29	TX driver timing register	d_rat_t3	d_rat_t2	d_rat_t1	d_rat_t0	d_tim_man	d_tim_m2	d_tim_m1	d_tim_m0
2A	Resistive AM modulation register	fa3_f	md_res6	md_res5	md_res4	md_res3	md_res2	md_res1	md_res0

Address (hex)	Register space B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2B	TX driver timing display register	d_rat_r3	d_rat_r2	d_rat_r1	d_rat_r0	RFU	d_tim_r2	d_tim_r1	d_tim_r0
2C	Regulator display register	reg_3	reg_2	reg_1	reg_0	RFU	RFU	RFU	i_lim
2E	**AWS Config 1**	**RFU**	**RFU**	**RFU**	**RFU**	**vddrf_cont**	**RFU**	**vddrf_rx_only**	**rgs_txonoff**
2F	**AWS Config 2**	**RFU**	**RFU**	**am_sym**	**en_modsink**	**am_filt3**	**am_filt2**	**am_filt1**	**am_filt0**
30	Overshoot protection configuration register 1	ov_tx_mode1	ov_tx_mode0	ov_pattern13	ov_pattern12	ov_pattern11	ov_pattern10	ov_pattern9	ov_pattern8
31	Overshoot protection configuration register 2	ov_pattern7	ov_pattern6	ov_pattern5	ov_pattern4	ov_pattern3	ov_pattern2	ov_pattern1	ov_pattern0
32	Undershoot protection configuration register 1	un_tx_mode1	un_tx_mode0	un_pattern13	un_pattern12	un_pattern11	un_pattern10	un_pattern9	un_pattern8
33	Undershoot protection configuration register 2	un_pattern7	un_pattern6	un_pattern5	un_pattern4	un_pattern3	un_pattern2	un_pattern1	un_pattern0
34	**AWS time 1**	**RFU**	**RFU**	**RFU**	**RFU**	**tmodsw1_3**	**tmodsw1_2**	**tmodsw1_1**	**tmodsw1_0**
35	**AWS time 2**	**tammode1_3**	**tammode1_2**	**tammode1_1**	**tammode1_0**	**tdres1_3**	**tdres1_2**	**tdres1_1**	**tdres1_0**
36	**AWS time 3**	**tentx1_3**	**tentx1_2**	**tentx1_1**	**tentx1_0**	**tmods2_3**	**tmods2_2**	**tmods2_1**	**tmods2_0**
37	**AWS time 4**	**RFU**	**RFU**	**RFU**	**RFU**	**tmodsw2_3**	**tmodsw2_2**	**tmodsw2_1**	**tmodsw2_0**
38	**AWS time 5**	**tdres2_3**	**tdres2_2**	**tdres2_1**	**tdres2_0**	**RFU**	**RFU**	**RFU**	**RFU**
39	**AWS RC Calibration readout**	**RFU**	**RFU**	**RFU**	**RFU**	**RFU**	**rc_cal_ro_2**	**rc_cal_ro_1**	**rc_cal_ro_0**

A portion of new registers have been added in the area called Space-A and Space-B.

In ST's official drivers (RFAL), the registers in Space-B have a flag (40h) on its address to indicate to address Space-B.

6 EMD handling for EMVCo 3.1a

From EMVCo 3.1a onwards, it is required to use the ST25R39xxB device in order to manage the updated EMD pattern.

7 Update of Tx driver register

The Tx output resistance can be adjusted in finer steps, especially from lowest resistance onwards, to permit small, and dynamic RF field adjustments in some applications such as EMVCo.

Table 7. Comparison between ST25R39xx and ST25R39xxB driver resistances

d_res<3:0>	ST25R39xx driver output resistance (normalized)	ST25R39xxB driver output resistance (normalized)
0	1.00	1.00
1	2.00	1.19
2	4.1	1.40
3	8.3	1.61
4	17.1	1.79
5	high-Z	2.02
6	-	2.49
7	-	2.94
8	-	3.41
9	-	4.06
10	-	5.95
11	-	8.26
12	-	17.1
13	-	36.6
14	-	51.2
15	-	high-Z

Furthermore, the am_mod range has been adapted, which is used for setting the modulation index for the different technologies.

Table 8. Comparison between ST25R39xx and ST25R39xxB modulation index

am_mod<3:0>	ST25R39xx modulation index %	ST25R39xxB modulation index %
0	5	0
1	6	8
2	7	10
3	8	11
4	9	12
5	10	13
6	11	14
7	12	15
8	13	20
9	14	25
10	15	30
11	17	40
12	19	50

am_mod<3:0>	ST25R39xx modulation index %	ST25R39xxB modulation index %
13	22	60
14	26	70
15	40	82

8 ST25R39xxB wake-up with varicaps

The ST25R39xxB can control the variable capacitors (VACs) via two internal DACs. The VACs have a certain settling time in the range of 5ms until the final capacitance value is reached. In the case of wake-up of ST25R39xxB in conjunction with VACs, it is required to wait until the capacitance value is settled. This time can be selected via meas_tx_del bits.

9 Migrating existing SW project

It is recommended the use of ST's NFC library (RFAL), which provides support for all required technologies, protocols, and including all existing ST25R devices (ST25R3911, ST25R3916, ST25R3916B, ST25R95).

This library is periodically updated to introduce new features, wider support of NFC devices, as well as fixes, and its compliance with the latest versions of the relevant standards is continuously ensured.

RFAL supports ST25R39xxB using the same source code of ST25R39xx. The selection of the device is done through the compiler, which defines both ST25R39xx and ST25R39xxB.

Revision history

Table 9. **Document revision history**

Date	Version	Changes
25-May-2022	1	Initial release.

Contents

List of tables