AN5792

Application note

VIPower M09 current sensing algorithms

Introduction

VIPower M09 SPI drivers have a complex priority manager for managing the temperature sense and current sensing for all outputs. There is a single analog to digital converter (ADC) that is multiplexed across all outputs and the thermal sensor. How and when that ADC is connected to each of these points is controlled by a priority handler. This application note is intended to further explain some of the nuances of the priority manager not fully covered in the extensive material found in the datasheet.

1 Functionality

M09 SPI drivers have a digital current sense feedback for each channel provided through an integrated 10-bit successive approximation register (SAR) ADC with 0.1% of full-scale range (FSR) accuracy. FSR would be considered as $I_{OUT\_SAT\_x}$ for each output. It is important to note that this accuracy is not the K factor accuracy. K factor accuracy includes all of the contributing tolerances in the current sensing chain. There is also a temperature sensor input to the ADC providing what is essentially the tab temperature of the driver.

There is a complex ADC priority handler that schedules when an ADC conversion occurs for each input.

1.1 Current sensing

At the beginning of a conversion, the current is sampled. This takes approximately 3 µs. After that, the ADC conversion begins and takes approximately 95 µs to complete. An output current is sensed based on two conditions:

- The output is ON
- The mode (asynchronous, or synchronous)

For the most accurate current sense conversion the output must be on for $t_{ON\_CS(min)}$. This allows for the current to be stable (not affected by rise or fall times) while sampling.

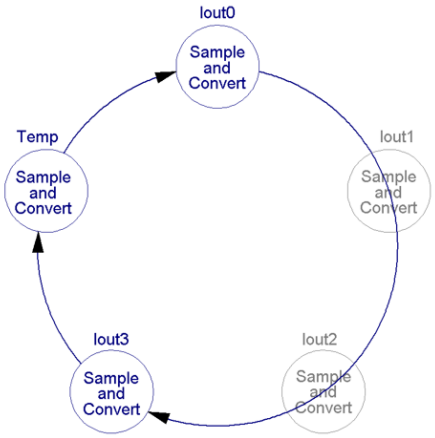
1.2 Temperature sensing

The frame or tab temperature is sensed in sequence with the current sensing in asynchronous mode. As in the current sensing, it also takes 3 µs to sample and ~95 µs to convert. Temperature sensing is more accurately associated with the tab, or lead frame, temperature.

1.3 Asynchronous mode

In asynchronous mode (or continuous mode), the sample and convert would occur sequentially for all outputs that are programmed ON as in the figure below.

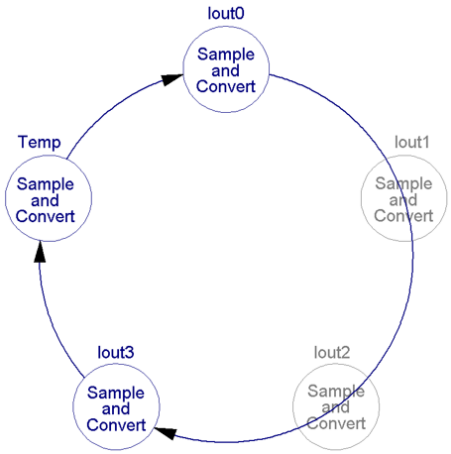
Figure 1. Continuous sampling sequencing all outputs on (four-output driver)



With all outputs ON and in continuous mode the total time to convert all channels is approximately 100 µs times the number of outputs ON + 100µs for the temperature conversion. For a four-output device that is approximately 500 µs.

When one or more outputs are OFF, the sequencer skips the OFF-State output and moves to the next. This looks like the next figure.

Figure 2. Continuous sampling sequentially with only two outputs ON



Because there are only two outputs ON in asynchronous mode in the previous figure, the conversion loop time is only ~300 µs. Temperature is always sampled in continuous mode. As a result, if all outputs are off, the temperature is sampled every ~100 µs.

1.3.1 Progressive average filter

The progressive average filter provides a 16-element rolling average of the current sensing. This option is only available for *asynchronous* mode current sensing. The 16-element rolling average uses a 16-sample average based on the following formula:

$$ADC_N = \frac{ADC_N - 1 \times 15 + ADC_i}{16}$$

Where:

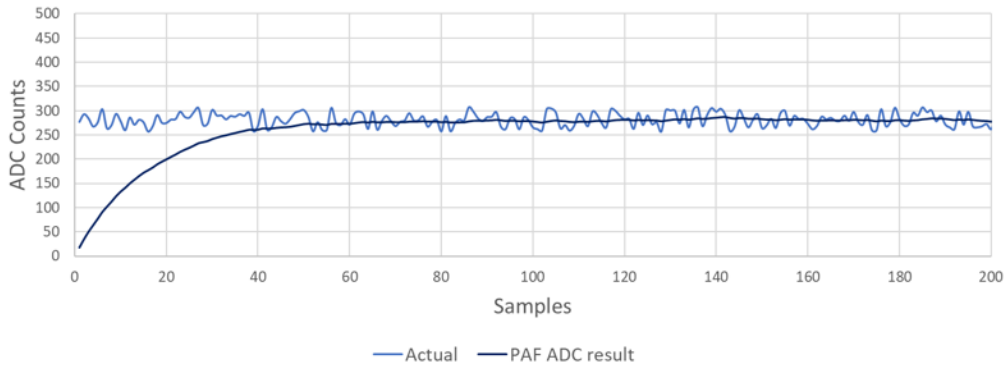
ADC_N = current running average

ADC_{N-1} = average from previous running average calculation

ADC_i = current ADC conversion

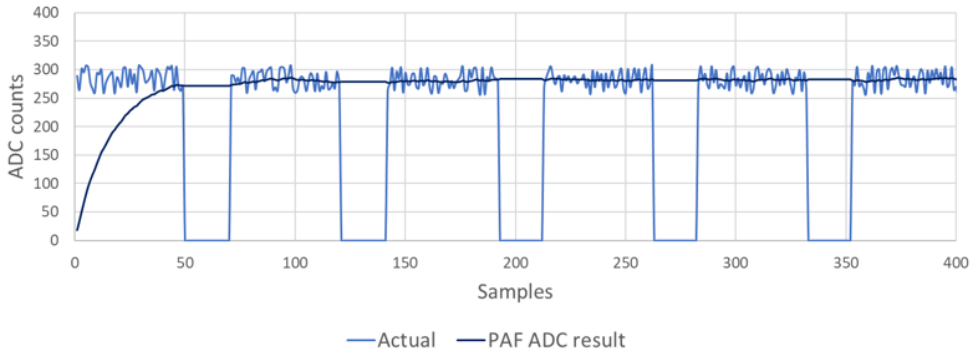
Note: When using the rolling average, the system requires approximately 50 conversions to establish a rolling average that has any meaning. The delay to 50 samples varies depending on the number of channels ON and in asynchronous mode.

Figure 3. Progressive average filter



In asynchronous mode, the sampling is only performed on the output when it is ON. That means the current sense feedback register will not change (return to 0) when the output is OFF.

Figure 4. **Progressive average filter with PWMming**



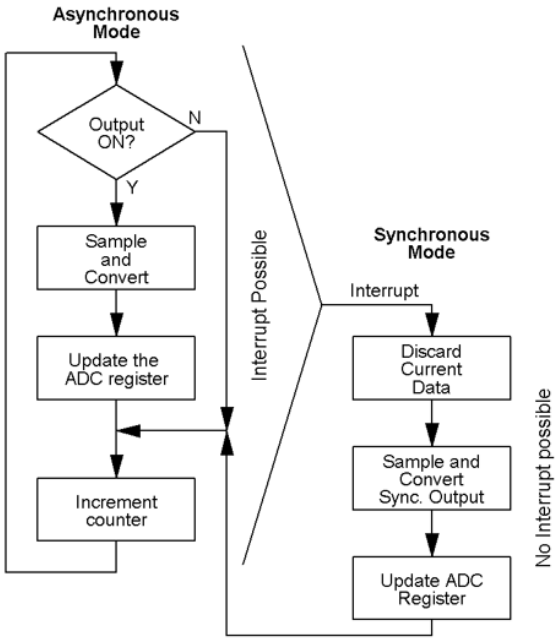
1.4 Synchronous mode

In synchronous sampling mode, the current is only sampled at programmed times while using the internal PWM generator. In synchronous sampling mode, sampling can be programmed to occur at turn on or at turn off.

When an output is programmed to be in synchronous sample mode the priority manager skips that output until the programmed time. If any outputs are set to run in synchronous mode, then the priority manager will continuously convert the tab temperature and any ON-state outputs set in continuous mode until a synchronous mode output condition (timing) is met. When a synchronous mode condition is met, all other conversion activities are interrupted and discarded to sample and converted into the synchronous mode output.

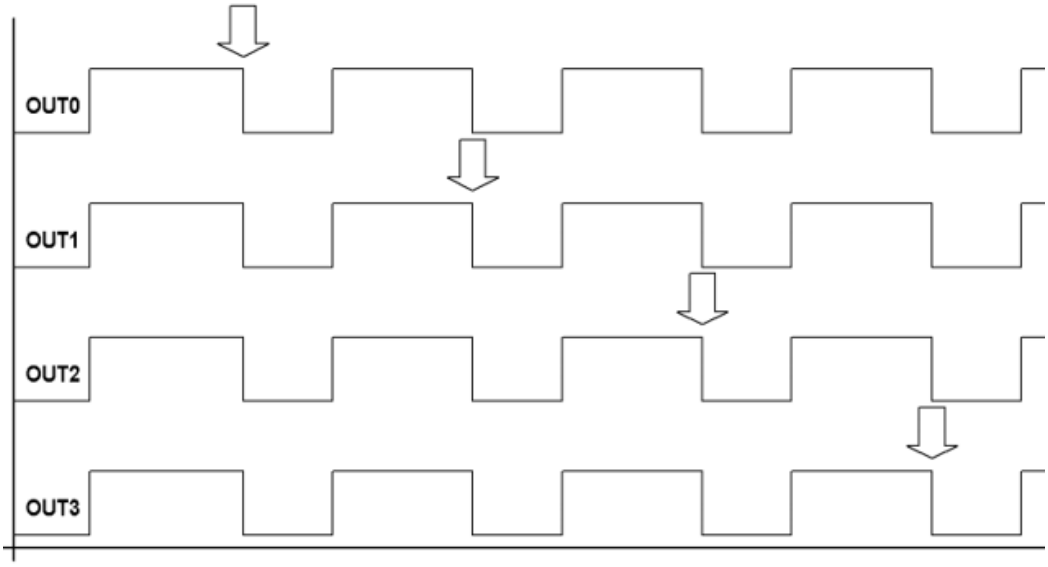
Once the synchronous mode sample and conversion is complete, the priority manager will move on to the next in line asynchronous conversion.

Figure 5. **Priority manager flow chart**



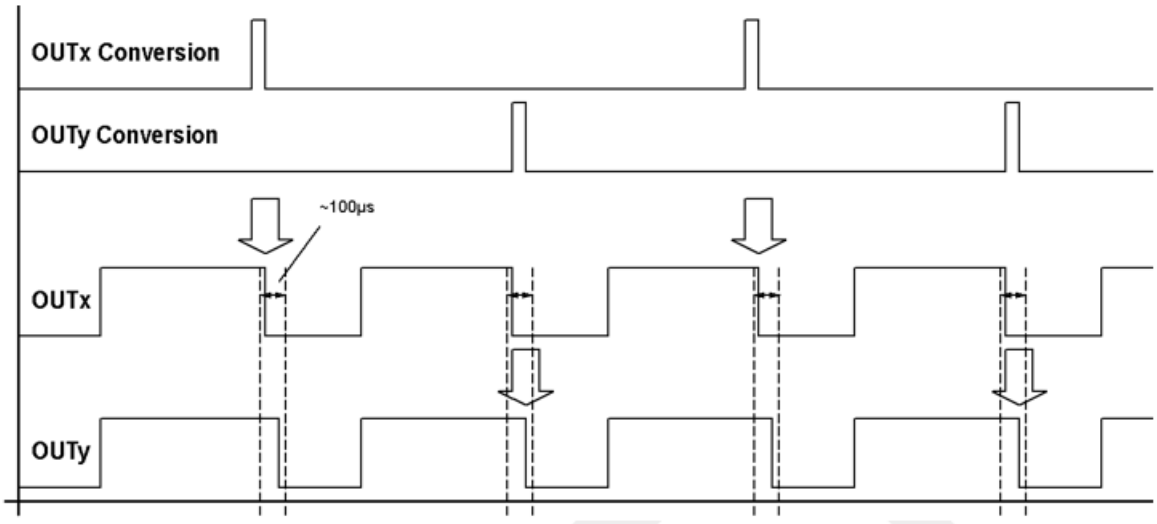
During multiple simultaneous conversions (same phase shift, frequency and sampling edge), all will be converted in order at each PWM cycle. Four outputs PWMming together, for example, will be converted one at a time over four PWM cycles.

Figure 6. **Synchronous current sampling**



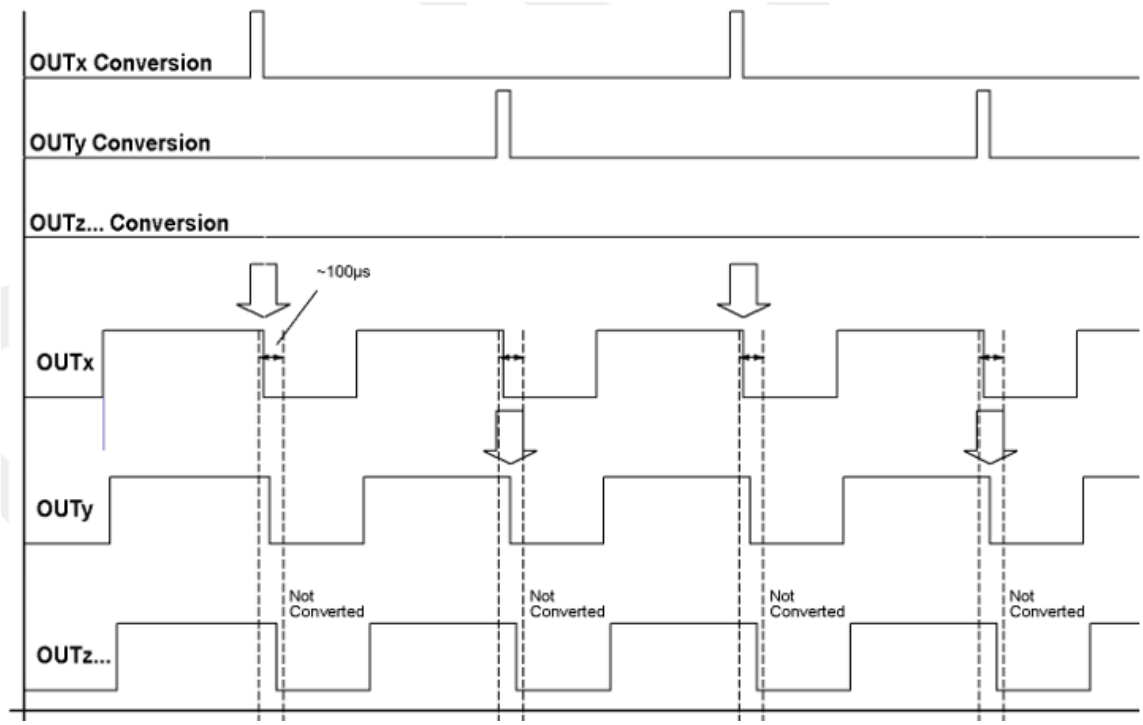
If a synchronous mode conversion is in progress and a second synchronous mode conversion request is made (not simultaneously driven), then the priority manager will convert them in every other PWM cycle.

Figure 7. **Synchronous output sampling**



If more than two synchronous mode conversions are requested within the first (or second) conversion window, then only the first two will ever be converted (alternately). Care should be taken to ensure that no more than two outputs will request a conversion in such a way as to prevent the remaining outputs from obtaining a current sense conversion.

Figure 8. **Multiple conversions within a single conversion window**

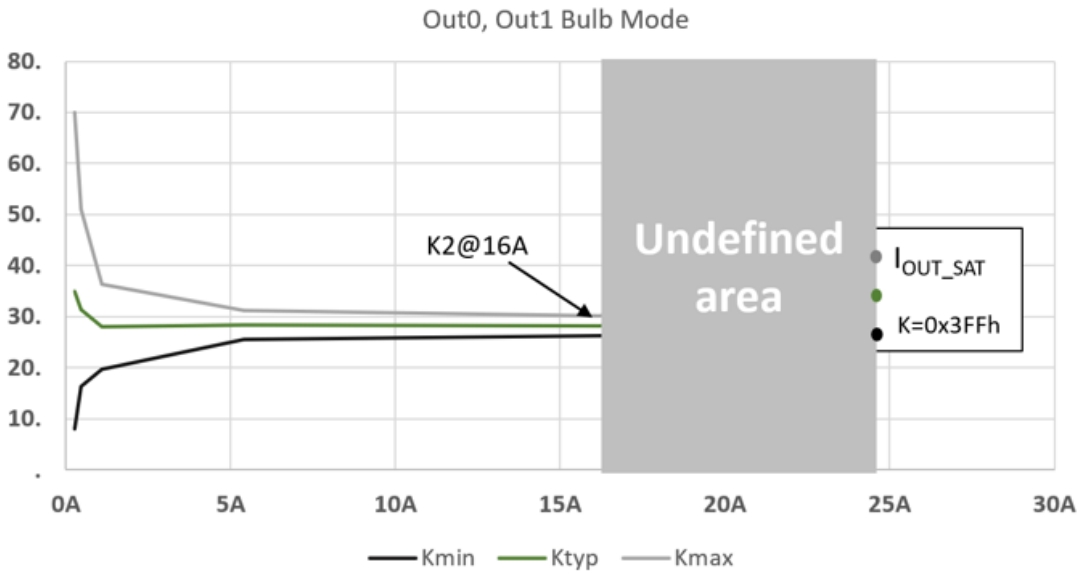


2 Valid data range

The full range of the 10-Bit ADC is 0x000 to 0x3FF. However, the K factor accuracy varies depending on where in that range the conversion is. The tolerance at lower currents is large enough to limit the valid low current conversions. The lowest current that can be converted and still reliably obtain something above 0x000h is defined by the I_{OUT_OFFSET} parameter. Any conversion below I_{OUT_OFFSET} may convert as a 0A current reading.

The highest reliable current reading is defined by K2. The current at K2 is typically three times the nominal running current designed for that output. The current readings above K2 are not characterized. Only the maximum current is guaranteed at $I_{OUT\_SAT\_x}$. The values between K2 and the $I_{OUT\_SAT\_x}$ are not defined.

Figure 9. K factors for VN9D5D20FN



3 Data registers

The SPI status registers associated with the ADC (temperature and current feedback) are always the same for all M0-9 SPI devices. Where there are less than 6 outputs those registers are not used.

Table 1. ADC registers

ADDR	Name	R/W/C	Description	Update	Default
28h	ADC0SR	Read	Digital current sense channel 0	continuous	0x0000
29h	ADC1SR	Read	Digital current sense channel 1	continuous	0x0000
2Ah	ADC2SR	Read	Digital current sense channel 2	continuous	0x0000
2Bh	ADC3SR	Read	Digital current sense channel 3	continuous	0x0000
2Ch	ADC4SR	Read	Digital current sense channel 4	continuous	0x0000
2Dh	ADC5SR	Read	Digital current sense channel 5	continuous	0x0000
31h	ADC9SR	Read	Digital frame temperature sense	continuous	0x0000

These read-only registers contain 16 bits,

- 10 bits for the ADC value (ADCxSR, Bits 13:4)
- 1 bit indicating if the output is commanded ON or OFF (SOCR, bit 2) *(not present in the digital frame temperature sense register, address 31h)*
- 1 bit indicating if the register has been refreshed since the last SPI read (UPDTSR, bit 1)
- Parity bit (bit 0)

Table 2. ADC register configuration

Bit#	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Desc.	RESERVED	RESERVED	ADCxSR9 (MSB)	ADCxSR8	ADCxSR7	ADCxSR6	ADCxSR5	ADCxSR4	ADCxSR3	ADCxSR2	ADCxSR1	ADCxSR0 (LSB)	RESERVED	SOCRx	UPDTSR	PARITY

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
04-Apr-2022	1	Initial release.

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